Bidirectional DC Voltage Conversion for Low Power Applications

Bidirektionale DC-Spannungswandlung für Kleinleistungsanwendungen

Conversion Bidirectionnelle de Tension DC pour Applications de Faible Puissance

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Abstract

Battery-powered mobile equipment is an important pillar of the electronic consumer market, especially since cellular phones and digital cameras have been introduced. However, all these mobile equipment have the same major weakness: their battery provides a limited operating time, which can only be increased in two ways. First, the energy density of the battery can be increased by developing new battery chemistries. Second, the battery energy can be used more efficiently by improving the energy management. This thesis focuses on the latter, and especially on the voltage conversion, which is used in mobile equipment. The novel concept exposed in this thesis consists in combining the voltage conversion unit with the battery management unit, thus building an *intelligent power converter* (IPC), that is integrated into the battery. This *intelligent battery* is able to provide a regulated and adjustable voltage directly to the mobile equipment, thus making it adaptable to every mobile equipment. Because the battery must also be recharged, the IPC must allow a bidirectional energy flow.

The IPC has been designed, simulated, laid-out and manufactured in a 0.18 µm mixed-signal CMOS technology from UMC. A full-custom design-flow using Cadence software was elaborated. In addition to the models provided by UMC, Monte-Carlo models were developed for simulating the impact of fabrication process variations. For the power part, electromigration design rule checks have been developed to ensure that metal overstress due to high current flows is avoided. The characteristics of the IPC are an operating voltage range between 1.2 V-3.6 V, an average load current up to 2000 mA, and an operating frequency in the range of 100 kHz-10 MHz.

Several novel solutions were developed for the IPC. First, since the direction of the energy flow is defined by the presence of a battery charger, a method was developed for detecting automatically the connection of a battery charger in parallel to the load. Second, a *continuous regulation loop* was developed, which enables highly efficient step-up and step-down conversion in both directions and at high switching frequencies. Third, *dynamic MOSFET sizing* was developed, to maximize the conversion efficiency when a light load is supplied. At switching frequencies above 1 MHz, this method provides more than 25% of absolute improvement in efficiency. Fourth, a current sensing method has been developed for estimating the average inductor current at switching frequencies up to 10 MHz. Fifth, an I^2C interface was implemented, to enable digital programming of the battery management.

Since the intelligent battery contains a battery management and provides an adjustable voltage, it can be easily replaced. This enables battery upgrading (e.g., different chemistry, higher energy density), so that the operating time of the mobile equipment is extended. The integration of electronics provides protection functions against shortcuts, overcharging, or also counterfeit.

Kurzfassung

Batteriebetriebene Mobilgeräte sind ein wichtiger Tragpfeiler des heutigen Markts, besonders seit Mobiltelefone und Digitalkameras eingeführt wurden. Allerdings haben Mobilgeräte einen Nachteil: die Batterie verfügt über eine begrenzte Kapazität, die nur auf zwei Wege erweitert werden kann. Der erste Weg besteht in der Entwicklung von neuen Batteriechemien, um die Energiedichte zu erhöhen. Der zweite Weg besteht in einer effizienteren Nutzung dieser Energie durch ein intelligenteres Energiemanagement. Diese Dissertation befasst sich mit dem zweiten Ansatz, und zwar mit der Spannungswandlung, die üblicherweise in Mobilgeräten benutzt wird. Ziel des vorgestellten Konzeptes ist es, den Spannungswandler mit dem Energiemanagement zu kombinieren, um damit einen *intelligenten Leistungswandler* (IPC) zu realisieren, der in die Batterie integriert wird. Diese *intelligente Batterie* liefert eine geregelte und einstellbare Spannung. Damit ist sie in jedem Mobilgerät einsetzbar. Der IPC muss einen bidirektionalen Energiefluss erlauben, um die Batterie aufladen zu können.

Der IPC wurde entwickelt und simuliert. Ein Layout wurde erstellt und in einer 0.18 µm-Mixed-signal CMOS-Technologie von UMC gefertigt. Ein auf Cadence-Software basierender Full-custom-Designfluss wurde erstellt. Zusätzlich zu den Modellen von UMC wurden Monte-Carlo-Modelle entwickelt, um die Variationen des Herstellungsprozesses bei den Simulationen berücksichtigen zu können. Um Elektromigration zu verhindern, wurden Designregeln geschrieben, damit eine Stromüberlastung der Metallverbindungen im Leistungsteil vermieden wird. Die technischen Daten des IPCs sind ein Betriebsspannungsbereich von 1,2 V-3,6 V, ein konstanter Laststrom bis zu 2000 mA und eine Betriebsfrequenz im Bereich von 100 kHz bis 10 MHz.

Mehrere neue Lösungen wurden für den IPC entwickelt. Erstens wurde eine Methode entwickelt, um ein Batterieladegerät zu erkennen, da die Richtung des Energieflusses durch die Anwesenheit dieses Ladegerät parallel zur Last bestimmt wird. Zweitens wurde eine *kontinuierliche Regelungsschleife* entwickelt, die es ermöglicht, bei hohen Frequenzen die gewandelte Spannung in beide Richtungen hoch- und herunterzusetzen. Drittens wurde eine *dynamische Einstellung der Weite des MOSFETs* entwickelt, um den Wirkungsgrad im Schwachlastbereich zu erhöhen. Bei Frequenzen über 1 MHz wurde eine absolute Wirkungsgraderhöhung von 25% erreicht. Viertens wurde für Betriebsfrequenzen bis 10 MHz eine Methode zur Abschätzung des Stromes durch die Induktivität entwickelt. Fünftens wurde eine digitale I^2C-Schnittstelle implementiert, um das Konfigurieren des Energiemanagementsystems zu ermöglichen.

Da die intelligente Batterie ein Batteriemanagementsystem enthält und eine einstellbare Spannung ausgibt, kann sie einfach ausgetauscht werden. Das Upgraden von Batterien wird möglich (z.B. andere Chemie, höhere Energiedichte), so dass die Betriebsdauer erweitert wird. Die Integration der Elektronik erlaubt es, zusätzlich Schutzfunktionen gegen Kurzschlüsse, Überladung oder Fälschungen unterzubringen.

Résumé

L'équipement mobile alimenté par batteries est un important pilier du marché actuel, notamment depuis que les téléphones portables et les appareils photo numériques y ont été introduits. Toutefois, les équipements mobiles ont l'inconvénient d'avoir une autonomie limitée qui ne peut être augmentée que de deux manières. La première consiste à augmenter la densité d'énergie de la batterie en développant de nouvelles chimies. La seconde consiste à utiliser cette énergie plus efficacement en en améliorant sa gestion. Cette thèse se focalise sur ce second point, et notamment sur la conversion de tension, largement utilisée dans l'équipement mobile. Le concept présenté dans cette thèse consiste à combiner le convertisseur de tension avec l'unité de gestion de l'énergie en constituant un *convertisseur de puissance intelligent* (IPC) intégré dans la batterie. Cette *batterie intelligente* est capable de fournir une tension régulée et ajustable, la rendant ainsi adaptable à tout équipement mobile. L'IPC doit cependant permettre un flux d'énergie bidirectionnel car la batterie doit pouvoir être rechargée.

L'IPC a été conçu, simulé, tracé dans le layout et fabriqué avec une finesse de gravure de 0.18 µm dans une technologie mixed-signal CMOS de UMC. Un design flow de type full-custom, basé sur les logiciels Cadence, a été élaboré. En plus des modèles fournis par UMC, des modèles de type Monte-Carlo ont été développés pour simuler l'impact des variations du process de fabrication. Contre l'électromigration, des règles de vérification du design ont été développées pour éviter la surcharge en courant des pistes métalliques dans la partie puissance. Les caractéristiques de l'IPC sont une plage de tension de fonctionnement de 1.2 V-3.6 V, un courant continu de charge de 2000 mA, et une fréquence de fonctionnement dans l'intervalle 100 kHz-10 MHz.

Plusieurs solutions nouvelles ont été développées pour l'IPC. Premièrement, comme la direction du flux d'énergie est définie par la présence d'un chargeur en parallèle avec la charge, une méthode pour détecter ce chargeur a été développée. Deuxièmement, une *boucle de régulation continue* a été développée. Elle permet d'augmenter ou de diminuer la tension à convertir dans les deux directions et à des fréquences élevées. Troisièmement, le *dimensionnement dynamique de MOSFET* a été développé pour maximiser l'efficacité de conversion lorsqu'une faible charge est alimentée. A des fréquences supérieures à 1 MHz, un gain en efficacité absolu de 25% est obtenu. Quatrièmement, une méthode d'estimation du courant moyen à travers l'inductance a été développée pour des fréquences jusqu'à 10 MHz. Cinquièmement, une interface I^2C a été implémentée pour permettre la configuration de l'unité de gestion de l'énergie.

Comme la batterie intelligente contient un système de management de batterie et offre une tension ajustable, elle peut être facilement remplacée. L'upgrade des batteries devient possible (différente chimie, plus grande densité d'énergie), et l'autonomie des équipements mobiles est allongée. L'intégration d'électronique permet l'ajout de fonctions de protection contre les courts-circuits, la surcharge ou encore la contrefaçon.

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Finally, the patience of my family and my friends was indispensable to preserve the balance in my life.

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"A pessimist sees the difficulty in every opportunity;
an optimist sees the opportunity in every difficulty."

Winston Churchill

"Auch aus Steinen, die dir in den Weg gelegt werden,
kannst du etwas Schönes bauen."

Erich Kästner

"Tout le monde savait que c'était impossible.
Il est venu un imbécile qui ne le savait pas et qui l'a fait."

Marcel Pagnol

Contents

List of Figures

List of Tables

List of Symbols

Θ_{JA}	(K/W)	Junction-to-air thermal resistance of a packaged circuit
Θ_{JC}	(K/W)	Junction-to-case thermal resistance of a packaged circuit
α	(-)	Process complexity factor
β	(%)	Transistor's width factor in dynamic MOSFET sizing
γ	(m^{-2})	Defect density in the considered CMOS technology
ρ_{bw}	($\Omega \cdot \mathrm{m}$)	Resistivity of the metal used in the bond wire
η	(%)	Power conversion efficiency of a DC-DC converter
$\eta_{\max}$	(%)	Maximum conversion efficiency of a DC-DC converter
$\Delta_{\max}(\eta)$	(%)	Maximum absolute gain in efficiency with DMS
$\mu,\ \mu_n,\ \mu_p$	($\mathrm{m}^2/\mathrm{V} \cdot \mathrm{s}$)	Carrier mobility in the channel of a MOSFET
A	(m^2)	Silicon area consumed by the design
C_i	(-)	Identification name of a capacitor
C_{GD}	(F)	Gate-drain (Miller) capacitance of a MOSFET
C_i	(F)	Capacitance value of the capacitor C_i
C_{load}	(F)	Capacity of the load filter capacitor
C_{out}	(F)	Capacity of the output filter capacitor
C_{ox}	(F/m^2)	Gate oxide capacitance per unit area
C_{SS}	(F)	Capacity of the soft-start capacitor
c_{D}	(€)	Silicon die price
c_{P}	(€)	Integrated circuit packaging costs
c_{T}	(€)	Integrated circuit testing costs
c_{W}	(€)	Silicon wafer price
D_i	(-)	Identification name of a diode
D	(%)	Duty cycle of a PWM signal
E_{drv}	(J)	Energy dissipated by the MOSFET gate drivers
f_{sw}	(Hz)	Frequency of a switching signal
f_{osc}	(Hz)	Frequency of the PWM oscillator
I_{batt}	(A)	Current provided by the battery
I_{B}	(A)	Bias current of the battery resistances $\mathrm{R}_{\mathrm{B}i}$
I_{CHG}	(A)	Nominal battery charging current
$I_{\mathrm{C}i}$	(A)	Current flowing through the capacitor C_i
I_{D}	(A)	Current flowing in the drain of a MOSFET

I_{EOC}	(A)	Battery end-of-charge threshold current
I_{in}	(A)	Input current of a DC-DC converter
$I_{\mathrm{L}i}$	(A)	Current flowing through the inductor L_i
I_{load}	(A)	Current consumed by the load
$I_{\mathrm{load(img)}}$	(A)	Image of the I_{load} current
I_{out}	(A)	Output current of a DC-DC converter
I_{PFM}	(A)	Current threshold for PFM operation mode
$I_{\mathrm{PFM(img)}}$	(A)	Image of the I_{PFM} current
I_{PRQ}	(A)	Battery charging current during prequalification mode
I_{PWM}	(A)	Current threshold for PWM operating mode
i	(-)	Positive integer designating a circuit device ($i \in \mathbb{N}$)
k	(J/K)	Boltzmann constant equal to $1.38 \cdot 10^{-23}$ J/K
L_i	(-)	Identification name of an inductor
L	(m)	Channel length of a MOSFET
l_{bw}	(m)	Length of a bond wire
M_i	(-)	Identification name of a MOSFET
M	(V/V)	Voltage conversion ratio in a DC-DC converter
M_{boost}	(V/V)	Voltage conversion ratio in a boost converter
M_{buck}	(V/V)	Voltage conversion ratio in a buck converter
$M_{\mathrm{buck\text{-}boost}}$	(V/V)	Voltage conversion ratio in a buck-boost converter
$M'_{\mathrm{buck\text{-}boost}}$	(V/V)	Voltage conversion ratio in the special buck-boost mode
M_{SEPIC}	(V/V)	Voltage conversion ratio in a SEPIC converter
M_{zeta}	(V/V)	Voltage conversion ratio in a zeta converter
m	(-)	Strictly positive integer ($m \in \mathbb{N}^*$)
N	(-)	Number of dies that can be get from a wafer
N_n	(-)	Number of fingers in an NMOS
N_p	(-)	Number of fingers in an PMOS
n	(-)	Indice designating the n-type silicon
P_{bw}	(W)	Conduction power losses in a bond wire
$P_{\mathrm{cond(tot)}}$	(W)	Sum of the conduction losses in a DC-DC converter
P_{DS}	(W)	Drain-source switching losses
$P_{\mathrm{DS(on)}}$	(W)	Drain-source conduction losses
P_{drv}	(W)	Power losses in the MOSFET gate drivers
P_{fixed}	(W)	Constant losses in the PWM regulation unit
P_{G}	(W)	Power losses in the MOSFET due to gate capacity
P_{load}	(W)	Power consumed by the load
P_{met}	(W)	Conduction power losses in the metallization
P_{oss}	(W)	MOSFET drain-source capacitance output power losses
$P_{\mathrm{pack(max)}}$	(W)	Maximum power that can be dissipated by the package
P_{rr}	(W)	Body diode reverse recovery power losses in MOSFETs

$P_{\mathrm{sw(tot)}}$	(W)	Sum of the switching losses in a DC-DC converter
p	(-)	Indice designating the p-type silicon
Q_{G}	(C)	Gate-charge capacitance of a MOSFET
Q_{oss}	(C)	Output charge of a MOSFET
q	(C)	Charge of an electron equal to $1.6 \cdot 10^{-19}\,\mathrm{C}$
R_i	(-)	Identification name of a resistor
$R_{\mathrm{B}i}$	(Ω)	Resistances controlling the battery specification voltages
R_{batt}	(Ω)	Internal series resistance of a battery
$R_{\mathrm{DS(on)}}$	(Ω)	Drain-Source resistance of a turned-on MOSFET
R_{dir}	(Ω)	Resistance defining the charger detection voltage
$R_{\mathrm{FB}i}$	(Ω)	Resistances controlling the gain of the feedback loop
R_{S}	(Ω)	Current-sense resistance
r	(m)	Radius of a silicon wafer
T_i	(-)	Identification name of a switch
S_{bw}	(m^2)	Section of a bond wire
T	(°C)	Temperature
T_{A}	(°C)	Ambient air temperature
T_{J}	(°C)	Junction temperature
$t_{\mathrm{c(off)}}$	(s)	Switch-off transient duration in a power MOSFET
$t_{\mathrm{c(on)}}$	(s)	Switch-on transient duration in a power MOSFET
t_{delay}	(s)	Delay time generated for anti-crossconduction
t_{off}	(s)	Time during which the energizing switch is turned off
t_{on}	(s)	Time during which the energizing switch is turned on
t_{sw}	(s)	Period of a switching signal
$t_{\mathrm{sw(on)}}$	(s)	Duration of the turn-on edge at the gate of a MOSFET
$t_{\mathrm{sw(off)}}$	(s)	Duration of the turn-off edge at the gate of a MOSFET
V_{ε}	(V)	Differential voltage seen at the input of an opamp
V_{A}	(V)	Buck and buck-boost crossover voltage in the IPC
V_{B1}	(V)	Buck-boost and boost crossover voltage in the IPC
V_{BS}	(V)	Bulk-source voltage of a MOSFET
V_{batt}	(V)	Voltage delivered by the battery
$V_{\mathrm{batt(CP)}}$	(V)	Threshold voltage for charge pump startup
$V_{\mathrm{batt(max)}}$	(V)	Maximum battery voltage when charged
$V_{\mathrm{batt(min)}}$	(V)	End-of-life battery voltage
$V_{\mathrm{batt(nom)}}$	(V)	Nominal battery voltage specified by the manufacturer
V_{CE}	(V)	Collector-emitter voltage across a BJT or an IGBT
V_{CI}	(V)	Regulation modes control voltage in the IPC
V_{CI1}	(V)	Shifted-up V_{CI} voltage
V_{CI2}	(V)	Shifted-down V_{CI} voltage
V_{CP}	(V)	Output voltage of the charge pump

$V_{\mathrm{C}i}$	(V)	Voltage across the capacitor C_i
V_{charger}	(V)	Voltage supplied by the battery charger
V_{clamp}	(V)	Control voltage for soft-start
V_{core}	(V)	Internal core voltage required by the CMOS technology
V_{DD}	(V)	Positive power voltage rail
V_{DDA}	(V)	Positive power voltage rail in the analog part
V_{DDD}	(V)	Positive power voltage rail in the digital part
V_{DS}	(V)	Drain-source voltage across a MOSFET
$V_{\mathrm{D(lim)}}$	(V)	Boost mode duty cycle clamping voltage for V_{CI}
V_{dir}	(V)	Voltage used for determining the energy's direction flow
$V_{\mathrm{EA(in)}}$	(V)	Error amplifier inverting input voltage in PWM unit
$V_{\mathrm{EA(out)}}$	(V)	Error amplifier output voltage in PWM unit
V_{FB}	(V)	Sensed feedback voltage in the feedback loop
V_{GS}	(V)	Gate-source drive voltage of a MOSFET
$V_{\mathrm{G(PDV)}}$	(V)	Peak-drive-voltage for driving the gate of the MOSFETs
$V_{\mathrm{G(M}i\mathrm{)}}$	(V)	Voltage applied to the gate of the MOSFET M_i
V_{in}	(V)	Voltage provided at the input of a DC-DC converter
$V_{\mathrm{L}i}$	(V)	Voltage across the inductor L_i
V_{load}	(V)	Voltage applied to the load
V_{osc}	(V)	Voltage waveform provided by the oscillator
V_{osc1}	(V)	Shifted-down V_{osc} voltage
V_{osc2}	(V)	Shifted-up V_{osc} voltage
V_{out}	(V)	Voltage provided at the output of a DC-DC converter
V_{ref}	(V)	Temperature and supply independent voltage reference
V_{S}	(V)	Voltage across the current-sense resistor R_{S}
V_{STDY}	(V)	Standby voltage supplied to the load for load detection
V_{shift1}	(V)	Positive shift voltage added to V_{CI} to get V_{CI1}
V_{shift2}	(V)	Positive shift voltage subtracted from V_{CI} to get V_{CI2}
V_{SSA}	(V)	Negative power voltage rail in the analog part
V_{SSD}	(V)	Negative power voltage rail in the digital part
V_{SSP}	(V)	Negative power voltage rail in the power part
V_{SW1}	(V)	Voltage at the inductor on the battery side
V_{SW2}	(V)	Voltage at the inductor on the load side
V_{T}	(V)	Thermal voltage equal to 25.86 mV at 300 K
V_{th}	(V)	Threshold voltage of a MOSFET
W	(m)	Channel width of a MOSFET
W_{f}	(m)	Channel width of a finger in a power MOSFET
y_{D}	(%)	Production die yield
y_{FT}	(%)	production final test yield
y_{W}	(%)	Production wafer yield

Z_{load}	(Ω)	Impedance of the load connected to the load side
Z_{out}	(Ω)	Impedance of the load connected to the output

Chapter 1

Introduction

1.1 Outline

The thesis is structured in seven chapters:

Chapter 1 introduces the organization and the conventions of this thesis. It describes the DC-DC conversion environment and exposes the importance of DC-DC conversion in today's mobile systems. It also presents the motivation of this research work. It gives an historical review of the DC-DC conversion topic and summarizes its current state-of-the-art. Finally, it shows the main goals and research objectives of this thesis.

Chapter 2 explains the principles used in DC-DC conversion. It begins with the presentation of the two most popular types of DC-DC converters, which are the linear voltage regulator and the switching voltage converter. Then it focuses on the controllers used in switching DC-DC converters and describes their different regulation principles.

Chapter 3 presents the specifications of the bidirectional DC-DC converter developed in this research work for low-power mobile systems. The choice of the CMOS technology and the choice of the power transistors type used for this design are explained. Floorplanning and packaging information for the prototypes are also detailed in this chapter.

Chapter 4 exposes the theory of operation of the bidirectional DC-DC converter designed in this thesis. There, the DC-DC controller algorithms, which control the whole DC-DC converter, are described and analyzed in detail. The operating principle of some special functions needed for autonomous bidirectional power conversion, like automatic battery charger detection and continuous voltage regulation feedback loop, is described. At the end of this chapter, a high abstraction level model of the DC-DC converter is presented.

Chapter 5 presents the CMOS design with the schematic and layout views of the bidirectional DC-DC converter prototype. The simulation results are also presented here. This chapter is divided into three parts: the analog part, the digital part, and the power part.

Chapter 6 shows the measurement results as well as the experimental environment that was used for obtaining them. These results are analyzed and discussed. Future technological improvements are also proposed in this chapter.

Chapter 7 concludes this thesis and summarizes the research contributions. Future research directions are also given in this final chapter.

1.2 Conventions

- The decimal separator used in this thesis is the dot (.).
  Example: 0.5 is the half of 1.
- The schematic components are designed by their names in normal fonts, while their values are written in italic fonts.
  Example: the capacitor C_{out} has a capacity of C_{out}.
- The [number] refers to the bibliography references.
  Example: [1] refers to the Ph.D. thesis written by A. Stratakos in 1998.
- The notation $[a, b]$ refers to the interval between value a and value b.
  Example: 2.57 is included in the interval $[2.0, 3.0]$.
- The digital signals are noted in small capitals. The active high signals are only referenced by their name. The active low signals are overlined.
  Example: the signal ENABLE is active high; the signal $\overline{\text{ENABLE}}$ is active low.
- A positive voltage is shown with the arrow from low potential to high potential.
- The abbreviation IPC stays for *Intelligent Power Converter*, which refers to the integrated bidirectional DC-DC converter presented in this thesis. The term *intelligent battery* refers to the battery with an integrated IPC. The term *charger* refers to the battery charger, which is the device used to recharge the battery. The verbs *charge* and *recharge* refer to the task of bringing energy to the battery. The term *load* refers to the load connected to the output of the IPC, which is supplied by the battery or the charger.

1.3 Motivation

There is an increasing demand for battery-powered mobile systems on the electronic consumer market, especially since cellular phones, personal digital assistants (PDA), digital cameras and wireless computer accessories have penetrated the market. All mobile systems have the same major issue: their batteries have a limited run-time, which has to be maximized.

Every newly developed mobile system powered by a battery implements a DC-DC converter. There are two different ways for improving the mobile system run-time. The first way consists in developing new battery chemistries with higher energy densities. The second way consists in improving the global efficiency of the mobile system powered by the battery. This is done by developing new energy management techniques, new DC-DC converter topologies [2], and new control schemes for them [3], as it is shown in this thesis.

To reduce the power consumption of these mobile systems, several solutions are used. One of these is clock gating, which is widely implemented in today's digital circuits (e.g., CPU), and coupled to a power management unit that powers down the unused units of the integrated circuits. More advanced design techniques like adaptive scaling of the supply voltage are also becoming important in modern processors, since the improvements of the battery run-time does not advance quickly enough to keep up with the increase in energy consumption of modern processors [4], [5], [6], [7], [8].

Another solution used to optimize the battery run-time consists in inserting a DC-DC converter between the battery and the supplied load. The voltage discharge characteristic of a battery is not a step function. For a lithium-ion battery, this voltage may vary by 20% around its nominal voltage value. The function of the DC-DC converter is to regulate the battery voltage and adapt it to the connected load. Therefore, the voltage supplied to the load becomes independent of the state-of-charge of the battery. Up to 50% increase in battery run-time have been reported by A. Stratakos [1] with digital CMOS loads when a DC-DC converter is used.

State-of-the-art in newly developed battery-powered mobile systems is the use of low voltage power supplies. According to the ITRS[1] summarized in Table 1.1, the supply voltage in battery-powered mobile systems (i.e., low power devices) will continue to decrease, and will be as low as 0.6 V in 2013. Simultaneously, the power dissipation in digital CMOS processors will continue to increase. As a direct consequence, the supply current will continue to increase. This shows that the new DC-DC converters must be designed for low voltages and high currents. However, these converters do not only have to be very power efficient at high currents. They must also perform efficiently at light loads, when the main processor of the mobile system is in standby. Therefore, today's needs in battery-powered DC-DC conversion technology are low voltage DC-DC converters with high output current and low quiescent current for high efficiency at both heavy and light loads.

Table 1.1: Supply voltage scaling and power dissipation in digital CMOS.

Year of Production	2007	2008	2010	2011	2012	2013	2015
V_{DD} (High Performance) (V)	1.10	1.00	1.00	0.95	0.90	0.90	0.80
Power Dissipation (W)	189	198	198	198	198	198	198
V_{DD} (Low Power) (V)	0.80	0.80	0.70	0.70	0.70	0.60	0.60
Battery Output Power (W)	3.0	3.0	3.0	3.0	3.0	3.0	3.0

1.3.1 Current Mobile Equipment Power Supply Topology

The battery-powered mobile devices currently available on the market use the power supply topology illustrated in Figure 1.1. In this topology, the battery supplies the system load through an unidirectional DC-DC converter, which regulates the voltage provided by the battery to a constant value, fixed by the design. In most of the cases, a power management unit is used and situated between the DC-DC converter and the battery. Its function is to monitor battery parameters, like the cell voltage, its temperature, and its remaining energy for estimating the remaining run-time.

When the battery is being recharged, the AC line provides the required electrical energy. A rectifier converts the AC voltage to a DC voltage, which is filtered, regulated, and held constant by a linear voltage regulator. This resulting supply voltage is used by the battery charger, which contains the charging algorithm adapted to the battery chemistry that is used. Its function is to control the entire charging cycle.

[1]ITRS: International Technology Roadmap for Semiconductors, 2007 Edition, Executive Summary, Table 6a, "Power Supply and Power Dissipation – Near-term Years", p. 82, 2007.

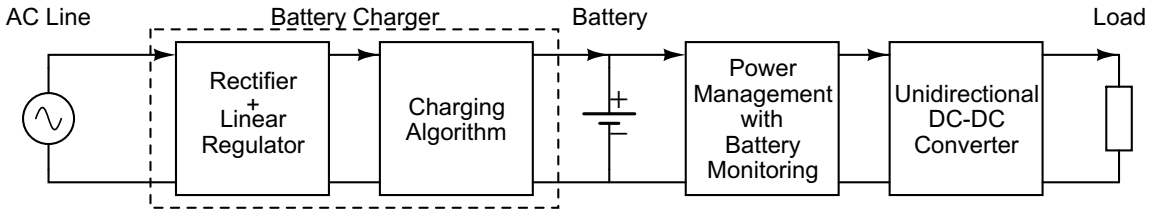

Figure 1.1: Power supply topology of state-of-the-art mobile systems.

Unidirectional DC-DC voltage converter ICs, battery management ICs, and battery charger ICs are provided on today's market by several manufacturers (e.g., Linear Technology, Maxim, Texas Instruments). But at the moment, there is no digitally controllable circuit on the market bringing together voltage conversion, battery charging, and power management. The state-of-the-art mobile equipment power supply topology has important drawbacks:

- If the battery has to be replaced, it cannot be replaced by using a battery with a different chemistry, since each chemistry has its own requirements concerning the recharging algorithm implemented in the battery charger. Typically, a lithium-ion battery has a lifetime of about three years, which is independent of the number of cycles it runs [9]. After these three years, the internal series resistance of the battery becomes so high that no more power can flow into or out of the battery.

- To offer optimal device performances, some parameters of the power management unit should be adjusted to the battery used. However, this cannot be done since these parameters are fixed at design time. The power supply unit is, therefore, often not optimized for the battery. For example, the measurement of the remaining energy — and therefore the remaining battery run-time — cannot be precisely performed when a battery with a different capacity in comparison to the original one is used.

- Low-cost batteries are not equipped with integrated protection electronics. This means, they are not protected against overcurrent, overvoltage, or overcharging when extracted from the mobile equipment. Even if some protections for the battery are provided in the battery charger and the power management units, they can only protect the battery as long as it is not removed from mobile equipment.

1.3.2 Novel Mobile Equipment Power Supply Topology

The newly proposed mobile equipment power supply topology presented in this work is shown in Figure 1.2. The main difference between the new and the state-of-the-art topology shown in Figure 1.1, is that the battery is now only connected to one unit. All units that are dependent on battery properties and parameters have been put together, resulting in one complex unit composed of a bidirectional DC-DC converter, a battery charger, and a part of the power management unit (the other part is located in the load itself). This complex unit is called *intelligent power converter* (IPC). This allows the adaptation and optimization of the IPC to the battery to which it is connected and

in which it is integrated. The system consisting of a battery and an IPC is hereafter called *intelligent battery*.

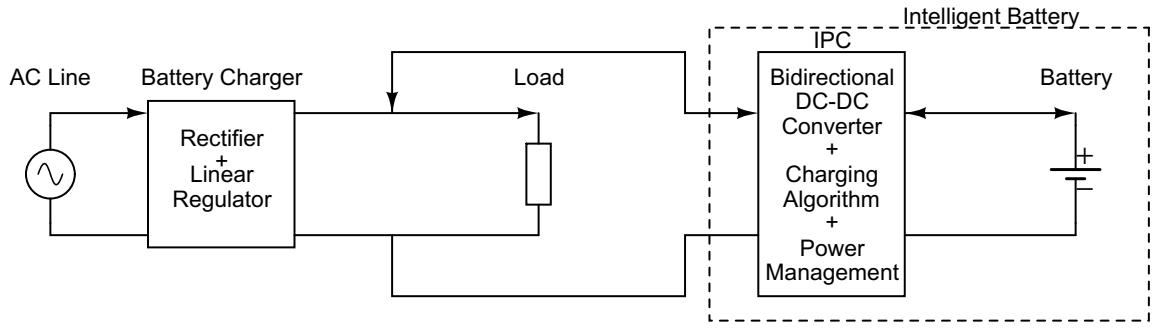

Figure 1.2: Power supply topology of novel mobile systems.

The DC-DC converter unit implemented in the IPC must be bidirectional. When a load is connected to the intelligent battery and no battery charger is connected (i.e., the AC line, the rectifier and the linear regulator are unplugged), the battery is supplying the load through the DC-DC converter. When a battery charger is connected additionally, the IPC recognizes this and starts to charge the battery. This is the reason why the DC-DC converter must be bidirectional. It must supply the load with the energy provided by the battery, or supply the battery with the energy provided by the charger, depending on what is connected to the intelligent battery (a load and/or a charger).

For the system to perform well without adding complexity to the battery charger, the battery charger must supply the load with a voltage slightly higher than the voltage provided at the output of the intelligent battery (i.e., the voltage provided by the IPC to the load). This allows the IPC to detect the battery charger. When the battery charger is removed again, the IPC rapidly detects a decrease in the voltage on the load side and starts to supply the load with the energy from the battery again. The detection mechanism is described in detail in Section 4.1.1. The new mobile equipment power supply topology combines the following advantages:

- The regulated voltage provided at the output of the intelligent battery can be adjusted. This allows the battery to be directly connected to electronic circuits, without an additional voltage regulator.
- When a replacement of the battery is due, the integrated battery management unit is also replaced, which means the new battery will contain again a fully optimized battery management. There will be no need to worry about the capacity or the chemistry of the battery. A battery upgrade will now also be possible.
- The integration of electronics in modern batteries will make it possible to integrate protection functions like overcurrent protection, overvoltage protection, or overtemperature protection into the battery. During transport and storage, the battery will then be fully protected. Additionally, counterfeit[2] can be fought by implementing an authentication procedure, as it is done on some printer cartridges.

[2]In 2004, the cellular phone manufacturer Nokia was the target of counterfeit batteries. Some of them exploded during normal use of the cellular phone and hurt some users severely. Battery counterfeit has become a major safety concern.

1.4 State of the Art

1.4.1 Historical Review

The invention of the *Bipolar Junction Transistor* (BJT) [10] in 1947 marked the beginning of semiconductor electronics. It permitted the increase of electrical equipment complexity and capability, and the reduction in size, costs, and power consumption. Semiconductor power diodes were available shortly after 1950. However, it was not until late 1957, when General Electric announced the *Silicon Controlled Rectifier* (SCR), a 4-layer thyristor (*pnpn*), that semiconductor power electronics really began.

The development of the modern forms of switched mode power supplies began in the 1960's. The realization of fast high voltage switching power BJTs [11] in 1967 made it possible to develop switched mode power supplies. Three basic topologies of nondissipative switching regulators based on a single energy storage device (i.e., an inductor) were designed for low voltage DC applications: the buck, boost and buck-boost regulators [12]. These three basic topologies are analyzed in Section 2.2.2.

The industry of switching mode power regulators began to grow in the early 1970's [13]. The theory and technology of switched mode power conversion became part of the academic discipline of power electronics. A major contributor to this discipline was R. Middlebrook and his team in the Power Electronics Group of Caltech in California, USA. The work of the Caltech Group in the switching power regulator application field has started in 1970. Its research objective was to develop models for the three basic DC-DC switching regulator topologies that were already developed in the 1960's [14], [15]. The result of this work was the modeling and analysis method called *state space averaging*, which allowed the theoretical prediction of the converter frequency response [16]. This allowed a better understanding of a switched mode regulator's feedback loop and stability criteria. Further work done at Caltech by S. Ćuk in his Ph.D. thesis [17] produced a new DC-DC converter topology. This new topology was called *Ćuk converter* and has been described as an optimum topology [18] since it has a special input-output symmetrical structure, which avoids pulsed currents on the input and the output. It uses three energy storage devices (i.e., two inductors and one capacitor), like the SEPIC and the zeta converters, which are both derived from the Ćuk topology. These three advanced topologies are analyzed in Section 2.2.3.

The power *Metal-Oxide-Semiconductor Field Effect Transistor* (power MOSFET) became available on the market at the end of the 1970's [11]. Unlike the BJT, the MOSFET has a high input impedance. This has greatly simplified the driving circuits and therefore reduced their size and costs. Additionally, when the MOSFET is turned on, the drain-source voltage drop V_{DS} can be as low as 50 mV when only low breakdown voltages are required. When high breakdown voltages are needed, the BJT offers a lower voltage drop V_{CE}, because of the resistive characteristic of the MOSFET's channel. However, the power MOSFET is more robust (e.g., no thermal runaway). It provides faster switching characteristics, thus opening the era of high frequency switching converters, where magnetics and capacitors can be dramatically reduced in values and therefore in sizes. Compared to the BJT, the MOSFET approaches more closely the ideal switch at low and medium power. As a consequence, it allows a higher converter efficiency. All these reasons explain why the BJT has been progressively replaced by the MOSFET in new low- and medium-power circuits that operate at higher switching frequencies.

Although different high voltage power MOSFET structures were developed (e.g., superjunction MOSFET, CoolMOS™ [19]), the requirement of MOSFETs with high breakdown voltages results in high drain-source resistance $R_{\mathrm{DS(on)}}$. In conventional high voltage MOSFETs, the voltage blocking capability in the drain drift region results in about 95% of the resistance in the current path. The intrinsic resistance of a conventional epitaxial drift region for a given breakdown voltage is the *silicon limit line*, which has been a barrier to improved performance in high voltage MOSFETs in the past [20]. Superjunction MOSFETs have broken this barrier, enabling the design of high voltage MOSFETs with a low area specific resistance. The limit in superjunction MOSFETs is no more a material limit (e.g., intrinsic resistance of silicon), but a manufacturing process limitation (e.g., small structures).

In the 1980's, a new addition to the family of power devices was made with the invention of the *Insulated Gate Bipolar Transistor* (IGBT). The IGBT combines the low power drive characteristics of the MOSFET with the low conduction losses and high blocking voltage characteristics of the BJT. Therefore, the IGBT is well suited for high power and high voltage applications. However, since its current transport principle is comparable to that of the BJT, its switching speed is much slower than that of the MOSFET.

Another power switch of interest is the *Static Induction Transistor* (SIT). The SIT was invented by J. Nishizawa [21] in the 1950's, but the power SIT was introduced on the market in its modern form [22] by the Tokin Corporation of Japan as late as 1987. The SIT is essentially a short channel *field effect transistor* (FET), well suited for high power, high frequency, and high temperature operation [23]. It could be taken as the solid-state version of a triode vacuum tube [24]. The SIT could become a promising power device for the future, if the problem of its too high channel resistance could be solved, although its conduction drop is lower than that of an equivalent MOSFET.

Another high power switch is the *MOS-Controlled Thyristor* (MCT). The MCT is a voltage controlled thyristor, which has two MOSFETs in its equivalent circuit: one for turn-on and another for turn-off. The first commercial MCT was introduced by Harris Semiconductors[3] in September 1992. However, it was a commercial flop, and the *Integrated Gate Commutated Thyristor* (IGCT) from ABB has replaced it. The IGCT combines high power conversion with high switching frequencies, high voltages, and low conduction losses. Figure 1.3 presents a summary of the analyzed power semiconductor devices classified by current, voltage and frequency ranges [25].

Research activities in the field of new materials like *silicon-carbide* (SiC), *gallium-arsenide* (AsGa), or diamond show tremendous potential for practically all power semiconductors in the mid-term future. A summary of the commercially available power devices is provided in Table 1.2. The given voltages and currents must be taken separately. They represent the maximum ratings that were found in the data sheets of different products currently available on the market. For example, the power device manufacturer Dynex Semiconductors provides an IGBT module referenced DIM400XSM65-K, which can support voltages up to 6500 V but only 400 A of continuous current. If high currents are required, the DIM3600ESM12-E is the device of choice, since it can handle continuous currents up to 3600 A, peak currents up to 7200 A, but voltages only up to 1200 V.

[3]Since August 1999, Harris sells its semiconductor devices under the name Intersil. Not all of Harris Semiconductors went with Intersil. Harris CMOS logic families are now part of Texas Instruments.

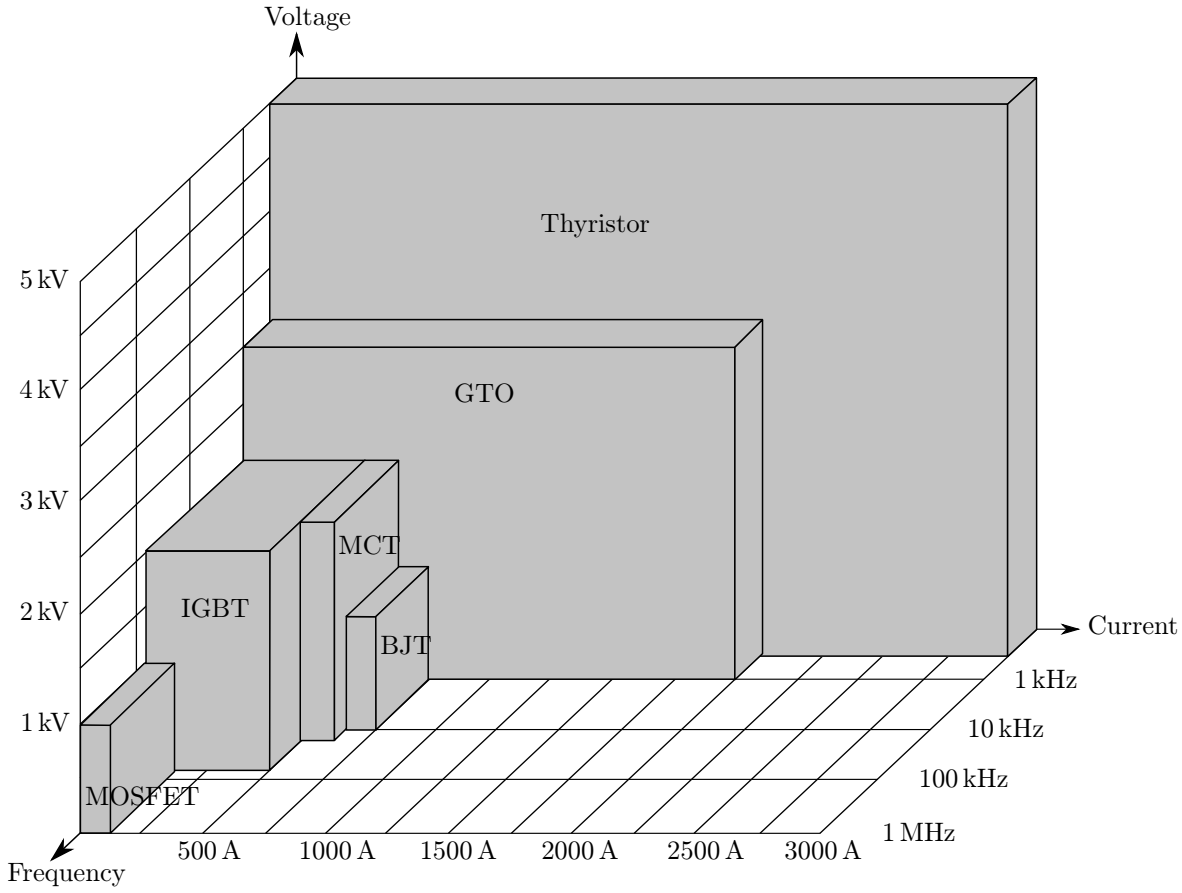

Figure 1.3: Summary of power semiconductor device capabilities [25].

Table 1.2: Ratings of commercial power semiconductor devices.

Device	Diode	SCR	BJT	MOSFET	IGBT
Voltage (V)	6000 V	8500 V	1700 V	1500 V	6500 V
Current (A)	10000 A	5000 A	160 A	430 A	3600 A
Manufacturer	Dynex	Dynex	ST	ST / IRF	Dynex

1.4.2 Research Directions in DC-DC Converters

Today, every integrated circuit needs a constant supply voltage for proper operation. However, the only way to store electrical energy in portable equipment is in DC energy reservoirs (e.g., batteries, accumulators and capacitors), which all suffer from the same drawback: their voltage decreases when they discharge [26]. The voltage delivered by such an energy tank must be regulated and adapted to the voltage requested by the electronics in the mobile device [27]. This makes the integration of DC-DC converters for mobile systems essential.

While the conversion of an AC voltage into another AC voltage can be done with high efficiency by a transformer, for DC-DC conversion no such simple device exists. The major concerns in DC-DC conversion are the efficiency of the conversion, the size of the converter and its costs.

The efficiency in power converters can mainly be improved by two factors: develop-

ments in power semiconductors (e.g., new materials, better control of manufacturing processes, improvements in packaging), and developments in control schemes (e.g., soft switching in resonant topologies). Some new converter topologies can also lead to an efficiency increase when combined with an adapted control scheme, but this is discussed more in detail in Section 2.2.

1.4.2.1 Research Directions in Power Semiconductors

Modern power semiconductors have permitted to achieve very high efficiencies [24], usually above 90% for state-of-the-art DC-DC converters. Development of new materials for capacitors and choke cores have contributed to the increase of efficiency. The development of modern high voltage devices is strongly dependent on the development of new materials, like SiC for high voltage power semiconductor devices. Although each power semiconductor device is used as a switch in power converters, the power semiconductor devices differ by their function and their commandability. It is of great interest to look at the current tendencies in the choice of power semiconductor devices, when power converters are designed.

For low- and medium-power applications, where voltages below 100 V are processed, the MOSFET remains the power switch of choice. It is especially well suited for compact designs, where high switching frequencies are needed. For this reason, it is largely used in modern power converters for mobile systems. This will remain the same in the future, since no emerging power semiconductor device can claim to outperform it in these applications.

For high power and high voltage converters, the BJT is reaching its limits. Most of these converters are replaced by better performing IGBT converters. The IGBT is definitely the switch of choice for medium voltage applications (400 V-2500 V). Its development has been accelerated in the last years, and IGBTs supporting voltages above 1200 V have become popular.

For specific applications requiring both high power and high frequencies, the IGCT will dominate, since it combines the advantages of both the GTO and the IGBT. However, the full potential of IGCT technology has not been reached yet. Some developments could dramatically improve the overall performance of the IGCT, which could become much more popular if some of its weaknesses could be improved (e.g., switching frequency).

Finally, a very important aspect concerning all the types of semiconductors mentioned previously is the assembly and the packaging method. A first challenge consists of carrying the high currents up to the active switches (e.g., up to the silicon die). If this is done by bond wires, the parasitic inductance provided by them can become a problem with high currents and/or high switching frequencies. Another challenge consists in ensuring the thermal power dissipation of the switching and conduction power losses. The type of assembly and packaging directly influences the reliability of the power device.

1.4.2.2 Research Directions in Control Schemes

In the past years, important progresses in conversion efficiency were accomplished in spite of the declining voltages and rising currents required by the modern integrated circuits. As explained in Section 1.4.2.1, the increase in efficiency is only partially due

to the improvement of the semiconductor devices and their materials in which they are manufactured. Instead, the most important gains were obtained through development of novel control schemes for driving the power semiconductor devices.

The *pulse-width modulation* (PWM) control scheme has been used since the beginning of switching regulators in the 1960's. It is still very usual today in hard switching and low power converters. Most of the power converters for mobile systems use an integrated circuit that offers a controller operating with a PWM control scheme.

The frequencies used by the integrated DC-DC converters are increasing, so that the converters can be combined with smaller passive devices. Therefore, smaller mobile systems can be developed. In 2003, D. Guckenberger *et al.* have presented an 88.7 MHz PWM-controlled integrated DC-DC converter [28]. However, PWM is not very efficient at light loads. This means that the converter becomes inefficient when the load is in standby, thus dramatically reducing the battery run-time in mobile systems. Therefore, practically all currently available integrated DC-DC converters implement a second control scheme like *pulse-skip modulation* (PSM) or *pulse-frequency modulation* (PFM). Both PSM and PFM have the same objective, which is to reduce the switching frequency of the power switches at light loads. This is done by skipping pulses (PSM) or by decreasing the PWM frequency (PFM).

For high power applications, the PWM control scheme used to drive the power switches leads to important switching losses, since it drives them when the current or the voltage across them is not zero. This is called *hard switching*. If the DC-DC converter circuit is modified and transformed into a DC-AC inverter followed by a high frequency AC-DC rectifier, a *resonant DC-DC converter* is obtained. However, the control scheme must be modified in such a way that the turn-on and/or turn-off of the power switches occurs at precisely defined instants, at those where the current or the voltage in the power switches of the DC-AC inverter is equal to zero. This control scheme is called *soft switching*. It permits to reduce drastically the switching losses in the power switches, at the costs of increased complexity in the control scheme. Resonant converters allow high conversion efficiency at high power and high switching frequencies [29].

Since the 1990's, *digitally controlled PWM* (DPWM) has become of interest [30], [31]. Digital control allows more flexibility in the development and also allows the integration of intelligence in the DC-DC converter itself. In 2004, J. Xiao *et al.* have presented a DPWM DC-DC converter for cellular phones [32]. Thanks to the digital technology, a simple power management unit has been integrated on the same die.

The DC-DC converter power density has been strongly increased when synchronous rectification was introduced. Synchronous rectification employs MOSFETs in place of the Schottky diodes in the output rectifier stage of the converter [33]. Therefore, less power is dissipated by the synchronous MOSFETs since their $R_{\mathrm{DS(on)}}$ resistance provides a lower voltage drop than the Schottky diodes. The driving of the synchronous rectifier MOSFETs needs some additional power and a specific driving circuit, which adds complexity to the design, but the gain in efficiency at full load is considerable.

By the introduction of multiphase conversion, the current density of DC-DC converters has been greatly increased. Multiphase conversion uses multiple drivers that operate out of phase and provide an apparent higher operating frequency, allowing the use of smaller capacitive and magnetic components [34].

By combining these different control schemes, today's power DC-DC converters usually exceed 88% of efficiency, at both heavy and light output loads [35].

1.5 Research Objectives

Excluding any new topology advance or new component technology, only fractional power density improvements are expected in the coming years. The number of different voltages required in mobile systems, like cellular phones, has been increasing continuously. An example of units using different voltages is shown in Figure 1.4. Simultaneously, the need to add management and control circuitry to manage the multitude of voltages on the circuit board has come. To control all these voltages, a battery management unit has been developed. This unit not only controls the different voltage sources, but also the charging and discharging cycles of the battery.

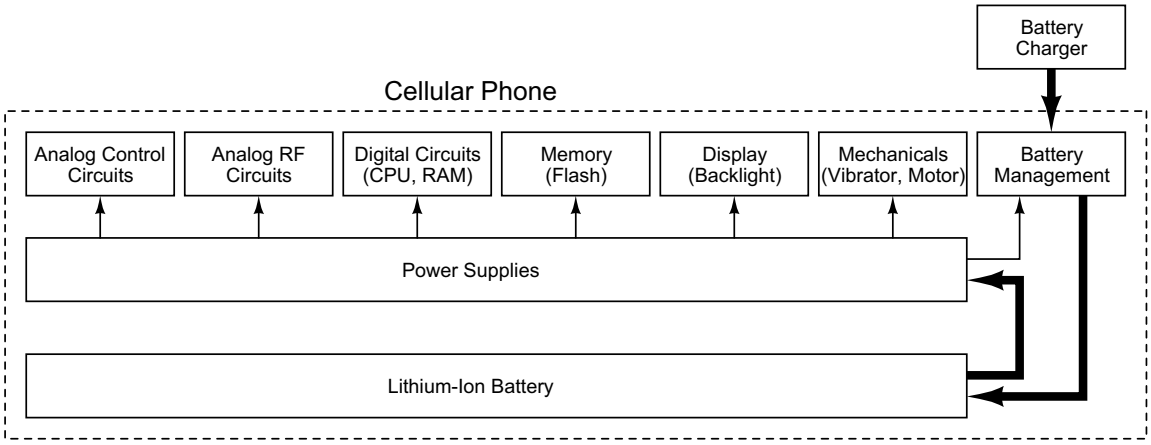

Figure 1.4: Power supplies in a cellular phone.

The future goal of the work presented in this thesis is to develop an intelligent battery. This intelligent battery will integrate a bidirectional DC-DC converter with its own battery management unit. This converter will be used during both charging and discharging operations. By designing a digitally reconfigurable battery management unit, it can be adapted easily to every mobile system's configuration. The goal of the present research work is to develop a concept enabling the realization of such a bidirectional DC-DC converter with embedded battery management functions (i.e., battery charging management), and to show the practical viability of this concept by building a demonstrator. The main research objectives followed during this thesis are summarized below:

- Design of a bidirectional DC-DC converter capable of detecting automatically the connection of a load and a battery charger on the same power side. The DC-DC converter must also detect the case in which no load and no charger are connected, thus it must enter a power saving standby mode. The goal is to demonstrate the concept exposed in Figure 1.2 by building a demonstrator.

- Integration of analog, digital and power electronics on the same silicon die. The goal is to build a monolithic bidirectional DC-DC converter, which integrates the power switches and the control and monitoring functions for the battery management. Since sensitive analog circuits are needed for the regulation loop, integrating these circuits onto the same silicon die as the power switches is a big challenge, especially concerning the thermal and noise concerns. A consequence of this integration is the increase in complexity of the converter design. As the

requirements of different control and monitoring functions increase, the circuitry becomes very complex and digital controls are therefore preferred.

- Investigation in using the dynamic MOSFET sizing concept at high switching frequencies. This principle was first mentioned by R. Williams *et al.* [36] with a discrete dual gate power MOSFET in 1997. A. Stratakos has made an integrated circuit demonstrator in his Ph.D. thesis [1] in 1998. More recently, in 2005, H.-C. Lee *et al.* have presented a monolithic current-mode CMOS DC-DC converter implementing the dynamic MOSFET sizing concept [37]. In the present thesis, the investigations in the field of dynamic MOSFET sizing began in early 2004. They focus on voltage-mode DC-DC converters designed in standard CMOS processes and requiring high switching frequencies (e.g., monolithic DC-DC converters with hybrid integrated power inductors).

- Development of a continuous regulation feedback loop for a DC-DC converter based on an H-bridge topology. This continuous regulation loop must enable smooth transitions between the voltage step-up and step-down modes when the supplied energy comes from a battery, which provides a decreasing voltage along its operating time. This regulation principle, novel in its manner, must enable bidirectional step-up and step-down conversions at high switching frequencies.

- Development of a lossless average current sensing method able to operate at high switching frequencies. This method must be adapted for low power switching converters, which need an estimation of the average inductor current, at switching frequencies up to 10 MHz and above. The average inductor current value is necessary to perform the constant current charging phase for a lithium-ion battery. Furthermore, this average inductor current value is needed for selecting the power transistor's width when the dynamic MOSFET sizing function is used.

Chapter 2

DC-DC Conversion Principles

In this chapter, the principles used in DC-DC conversion are explained. In the first part, the most popular type of voltage converters is presented: the linear regulator. In the second part, the switching converters are described and analyzed. Finally, in the third part, the controllers used in the switching converters are exposed and their different regulation principles are explained.

As shown in Figure 2.1, each electronic power converter consists in a power processor, a controller, and a voltage reference [25]. The input power coming from the supply is converted by the power processor and provided to the load. The power processor can be a current, a voltage, or a frequency converter (or any combination of these physical quantities). It consists of power electronic devices like those presented in Section 1.4.1. The feedback controller compares the output voltage of the power processor with a reference voltage value, and acts on the power processor so that the error between the two are minimized. Both linear regulators and switching regulators use this elementary regulation principle.

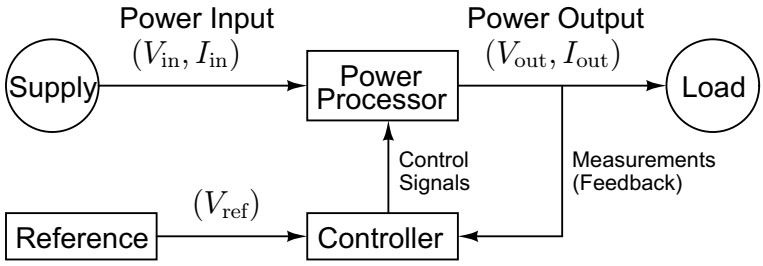

Figure 2.1: Block diagram of a typical electronic power conversion system.

2.1 Linear Voltage Regulators

A linear voltage regulator is a simple electronic device which supplies a load with a constant DC voltage. It comprises electronic circuits that hold the voltage provided to the load at the desired voltage value, regardless of changes in load current and input voltage. However, the regulation can only take place if the load voltage, the load current and the input voltage are within the acceptable operating range.

Linear regulators are cheap and easy to use. They offer very low output ripple to the load. Therefore, they are well suited to supply noise sensitive circuits, like radio-frequency integrated circuits in cellular phones. Linear regulators provide excellent line

and load regulation, and react very fast to transient load and line changes. Since they are nonswitching regulators, they do not emit *electromagnetic interferences* (EMI). Unfortunately, linear regulators also have some drawbacks. Their efficiency is poor, which means the power dissipated is generally high. This has a negative consequence on the circuit size, because huge heatsinks are mandatory.

2.1.1 Operating Principle

Figure 2.2 shows a typical linear voltage regulator. It is constituted of a pass-device (power transistor M_1), a voltage reference (V_{ref}) and an error amplifier with a resistive feedback loop composed of R_{FB1} and R_{FB2}. The capacitor C_{out} is used for adjusting the stability in the loop compensation.

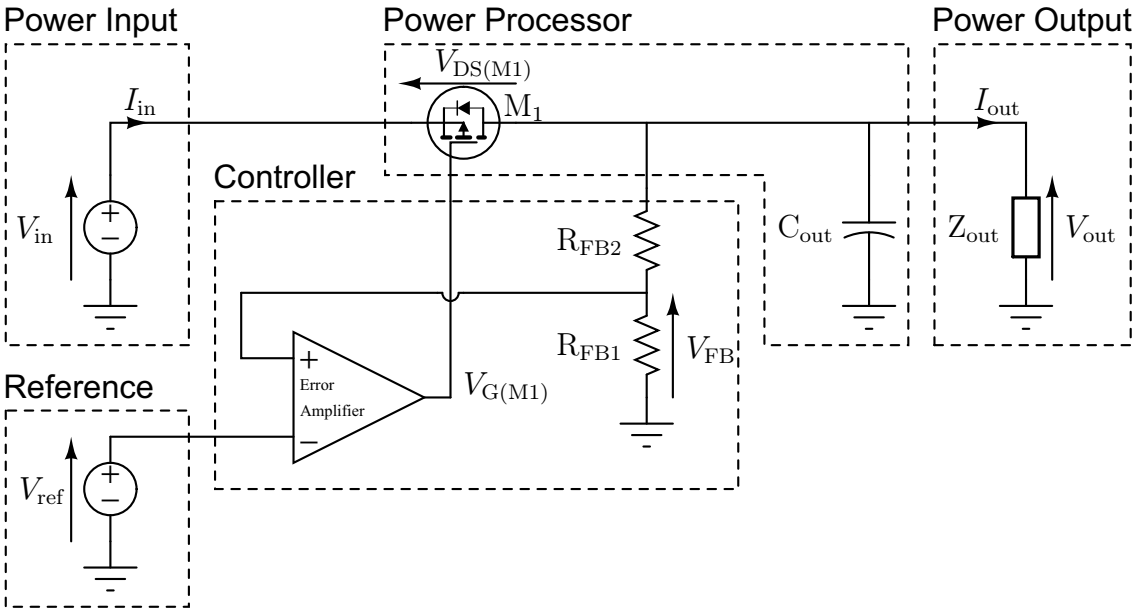

Figure 2.2: Block diagram of a typical low dropout linear voltage regulator using a PMOS transistor as pass-device.

The power PMOS M_1 acts as an adjustable resistor. The error amplifier adjusts the gate voltage $V_{G(M1)}$ so that the voltage drop $V_{DS(M1)}$ across the power transistor M_1 gives the desired output voltage value V_{out}. The regulated voltage value is controlled by the gain of the resistive feedback loop. The error amplifier tends to equalize the voltage at its inputs, and therefore, the load voltage V_{out} is given by:

$$V_{out} = V_{ref} \cdot \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \tag{2.1}$$

For the IPC, an integrated linear regulator was developed to generate its internal core voltage V_{core}. This circuit is analyzed in Section 5.1.1.4.

2.2 Switching Voltage Converters

Switching regulators generally use an oscillator for generating a clock signal, active elements as switches, and reactive passive elements (like capacitive and magnetic

devices) for storing the energy to convert. If the switching elements are considered without their parasitics, the efficiency of switching converters can theoretically reach 100%. Practically, unlike linear regulators in which the pass-device is used as an adjustable resistor, in switching converters only the parasitics lower the power conversion efficiency.

There are two main types of switching regulators. The simplest one is made only with capacitive components and switching devices: it is called *switched capacitor converter*. It is also often called *inductorless converter* or *charge pump*. This type of converter is mainly used in integrated circuits to multiply or divide the power supply voltage with a higher efficiency than a linear regulator. Charge pumps are generally low power converters using MOSFETs as active switching elements. They are analyzed more in detail in Section 2.2.1.

A more flexible and powerful type of switching regulator is the DC-DC converter using both capacitive and magnetic passive devices, in combination with active switching devices. The capacitive devices are integrated or discrete capacitors, while the magnetic devices are generally discrete power inductors or power transformers. Different active devices are used to design such converters, depending on the application's needs. These devices are mostly transistors, diodes and thyristors.

2.2.1 Switched Capacitor Converters

While the classic DC-DC converters use capacitors and inductors (see Section 2.2.2 and Section 2.2.3), the switched capacitor converters are only designed with capacitors. Switched capacitor DC-DC converters are low power converters that consist of power switches and energy transfer capacitors in the power stage. The switches are periodically turned on and off, so that the converter cycles through a number of switched networks. These topologies are not adapted to high power converters. Because they make no use of inductors, these converters can be completely integrated into a single silicon chip (power inductors are difficult to integrate on silicon [38]). There is no need to use off-chip capacitors nor inductors. The output power in the target applications is in the milliwatt range. The silicon area occupied by the converter and its on-chip capacitors can be very important. Most of the silicon area used by the switched capacitor converter is occupied by the MOS capacitors constituting the switched capacitor network. However, in deep sub-micron mixed-signal technologies, *metal-metal capacitors* (MMC) are the best choice. They provide a lower *equivalent series resistor* (ESR) and higher breakdown voltages, thus reaching a higher efficiency.

A major advantage of the switched capacitor converters is that they eliminate the magnetic fields and EMI that comes with an inductor or a transformer. A drawback is that they do no provide high conversion efficiency if the needed voltage conversion factor is not an integer.

The circuit shown in Figure 2.3 represents a basic switched capacitors noninverting voltage doubler [39]. During operation, two states of equal duration occur. During the first state, the capacitor C_1 is charged with the input voltage V_{in} through the switches T_1 and T_2 (T_3 and T_4 are open). During the second state, T_3 and T_4 are closed, while T_1 and T_2 are open. The voltage across C_1 (i.e., the voltage V_{in} at which C_1 has been charged during the first state) is added to the input voltage V_{in}, and provided to the output filter capacitor C_{out}. Therefore, the voltage V_{out} provided to the output is two times the input voltage V_{in}. Thus, the voltage conversion ratio M of this circuit is

given by:

$$M = \frac{V_{\text{out}}}{V_{\text{in}}} = 2 \tag{2.2}$$

A fully integrated 2-phase charge pump operating at a switching frequency of 200 MHz and using two metal-metal capacitors as charge transfer components [40] was developed for the IPC and is described in Section 5.1.1.3.

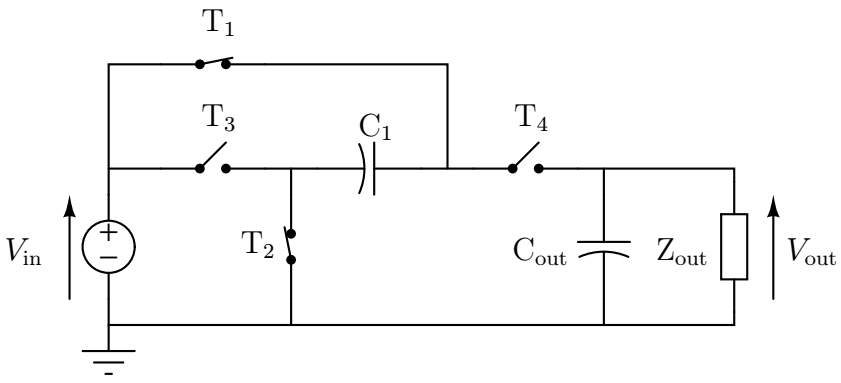

Figure 2.3: Schematic of a voltage doubler with switched capacitors.

2.2.2 Basic DC-DC Converter Topologies

In the following approaches, the converters are supposed to operate in steady-state with a constant input voltage V_{in} and a constant output voltage V_{out}. Further, the components used in the power paths are taken ideal and no parasitics are considered (e.g., the power transistors are assimilated to ideal switches having an infinite resistance when turned off, and no resistance when turned on). However, the parasitics in the power paths are analyzed and discussed in detail in Section 5.3, where precise component models are used in advanced circuit simulations.

The basic circuits used to design advanced DC-DC converters consist in three main topologies, which are the step-down topologies (like the buck converter shown in Figure 2.4), the step-up topologies, and the topologies able to perform both step-up and step-down conversion. Some circuits are also able to perform polarity inverting at output (e.g., converting an input voltage of 3.3 V into a negative output voltage of −5 V). The step-down topologies are only able to provide an output voltage lower than the input voltage, while the step-up topologies are only able to provide an output voltage higher than the input voltage. The combination of a step-up and a step-down topology enables both voltage reduction and voltage increase with a single switching converter.

The energy storage devices (i.e., capacitors, inductors or transformers) are the heart of any switching-mode power supply. Switching regulators use inductors which are usually wound on toroidal cores, often made of ferrite or powdered iron core with distributed air-gap to minimize core losses at high frequencies. Transformers are mostly used in isolated topologies. However, in this research work, only nonisolated topologies using capacitors and inductors are considered, because transformers are not easily integrable in mobile systems.

A capacitor stores its energy in an electrical field. This field builds up when a voltage V_{C1} is applied to the capacitor's terminals. The ability of a capacitor to store

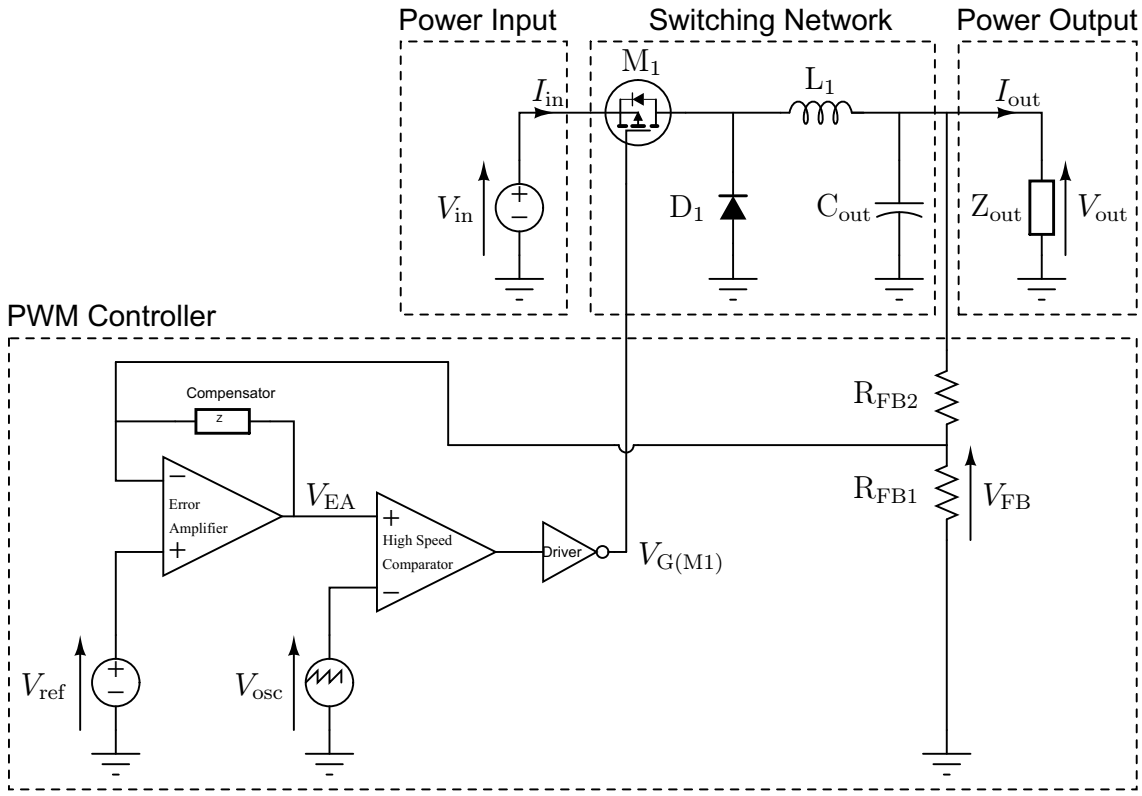

Figure 2.4: Typical voltage mode PWM buck converter with its feedback loop.

energy in the form of an electric field, and consequently to oppose changes in voltage, is called capacitance. The capacitor equation states that the current I_{C1} flowing through the capacitor C_1 is proportional to the rate of change in voltage V_{C1} at the capacitor's terminals. The constant of proportionality is the capacitance C_1.

$$I_{\mathrm{C1}}(t) = C_1 \cdot \frac{d}{dt} V_{\mathrm{C1}}(t) \tag{2.3}$$

An inductor stores its energy in a magnetic field. This field builds up when a current I_{L1} flows through the inductor. The ability of an inductor to store energy in the form of a magnetic field, and consequently to oppose changes in current, is called inductance. The inductor equation states that the voltage V_{L1} at the inductor's terminals is proportional to the rate of change in current through the inductor L_1. The constant of proportionality is the inductance L_1.

$$V_{\mathrm{L1}}(t) = L_1 \cdot \frac{d}{dt} I_{\mathrm{L1}}(t) \tag{2.4}$$

Before analyzing the basic DC-DC converter topologies, some definitions used in this thesis must be presented. Figure 2.4 shows a buck converter with its environment (the buck converter is presented in detail in Section 2.2.2.1). In mobile applications, the voltage at the power input is provided by a battery, but any other DC voltage source is also usable. The switching network consists in switches like power diodes and transistors (NMOS or PMOS), and in reactive elements like inductors and capacitors. It is the power part of the power converter. The power output consists in a load $\mathrm{Z}_{\mathrm{out}}$

which is an impedance. The PWM controller contains the pulse-width modulation unit (oscillator, error amplifier, PWM comparator), the regulation feedback loop (feedback voltage, reference voltage, loop compensator), and the buffer for driving the power transistor's gate (driver).

Figure 2.5 shows the analog signal waveform V_{osc} of the sawtooth oscillator switching between the voltages V_1 and V_2. It also shows the error amplifier output voltage V_{EA}, and the digital PWM signal waveform $V_{G(M1)}$ of the power transistor gate driver, which commands the PMOS transistor M_1 in Figure 2.4. The time variable t_{sw} represents the period of the sawtooth oscillator, t_{on} is the period during which the energizing power transistor is turned on, and t_{off} is the period during which it is turned off. The duty cycle D is defined as the ratio of t_{on} to t_{sw} (see Equation (2.5)). The energizing transistor is defined as the transistor which increases the current flowing through the inductor L_1 when it is turned on (see Figure 2.5).

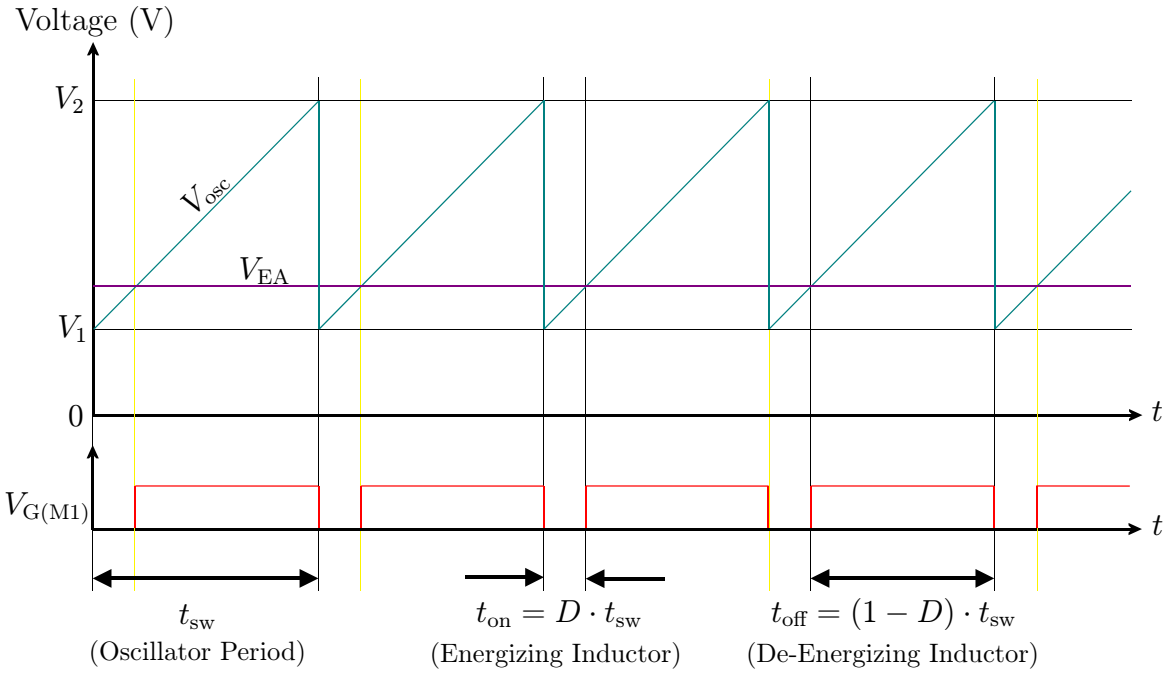

Figure 2.5: Steady-state PWM timing diagram of the buck converter shown in Figure 2.4. $V_{G(M1)}$ is the gate drive voltage applied to the PMOS M_1.

2.2.2.1 Buck Converter

The buck converter shown in Figure 2.6 is the simplest step-down switching topology. It is made of a PMOS power transistor M_1 acting as the energizing switch for the inductor L_1, a power diode D_1 assuring the continuity of the current in L_1, and a filtering capacitor C_{out} reducing the output voltage ripple on V_{out}. The power input is represented by the DC voltage source delivering V_{in}. The output load is represented by the impedance Z_{out}, which value can vary in time (e.g., a heavily loaded CPU entering the idle state).

The regulation of the output voltage V_{out} can be done by the voltage mode controller previously illustrated in Figure 2.4. It consists in generating a PWM signal based on the feedback voltage V_{FB}. When the energizing power transistor M_1 is turned

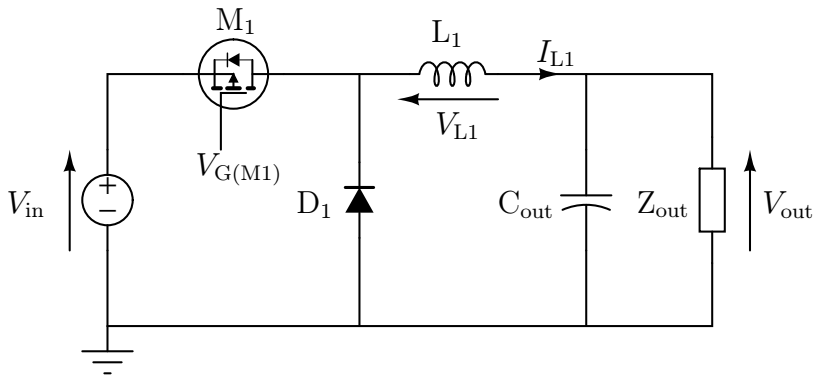

Figure 2.6: Buck converter schematic.

on, the inductor current I_{L1} increases and the free-wheeling diode D_1 is reverse biased. When M_1 is turned off, D_1 becomes forward biased and I_{L1} decreases. Depending on the load impedance Z_{out}, if the current I_{L1} does not reach zero during t_{off}, the converter operates in the *continuous conduction mode* (CCM). If I_{L1} reaches zero during t_{off}, it tries to reverse but it is blocked by the diode D_1 and the converter operates in the *discontinuous conduction mode* (DCM). This is illustrated in Figure 2.7.

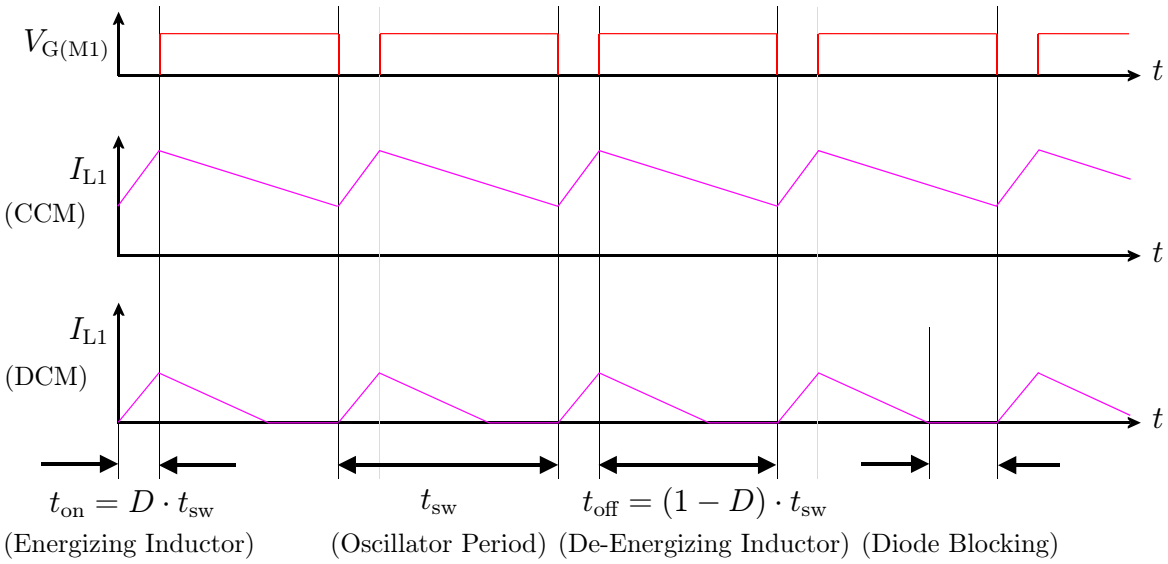

Figure 2.7: Steady-state inductor current I_{L1} timing diagram of the buck converter shown in Figure 2.4 and Figure 2.6.

The body diode of the power transistor M_1 shown in Figure 2.6 is not used in the buck converter. However, in topologies like the H-bridge converter presented in Section 2.2.3.5, the body diode of the energizing transistor plays an essential role. To calculate the transfer functions in the converter topologies presented hereafter, the converter is considered to operate in steady-state and continuous conduction mode. Some definitions are made in Equation (2.5) and illustrated in Figure 2.7. They are

used in all this thesis.

$$\begin{cases} f_{sw} = \dfrac{1}{t_{sw}} \\ t_{sw} = t_{on} + t_{off} \\ D = \dfrac{t_{on}}{t_{sw}} \end{cases} \tag{2.5}$$

To determine the relation between V_{in} and V_{out}, two states must be distinguished:

- State 1: M_1 is turned on, D_1 is reverse biased ($0 < t < t_{on}$):

$$V_{L1} = V_{in} - V_{out} \tag{2.6}$$

- State 2: M_1 is turned off, D_1 is forward biased ($t_{on} < t < t_{sw}$):

$$V_{L1} = -V_{out} \tag{2.7}$$

The current I_{L1} in the inductor L_1 is continuous and periodic in time. Integrating Equation (2.4) over one complete switching period t_{sw} yields:

$$I_{L1}(t_{sw}) - I_{L1}(0) = \frac{1}{L_1} \cdot \int_0^{t_{sw}} V_{L1}(t) \cdot dt \tag{2.8}$$

In steady-state, the initial value $I_{L1}(0)$ and the final value $I_{L1}(t_{sw})$ of the inductor current are equal. Therefore, the integral of the applied inductor voltage must be equal to zero:

$$0 = \int_0^{t_{sw}} V_{L1}(t) \cdot dt = \int_0^{t_{on}} V_{L1}(t) \cdot dt + \int_{t_{on}}^{t_{sw}} V_{L1}(t) \cdot dt \tag{2.9}$$

Equation (2.9) is called the principle of *inductor volt-second balance* [41]. It is used over this thesis to determine the conversion ratio M of each topology presented. By neglecting the voltage ripple on V_{in} and V_{out}, the voltage V_{L1} over the inductor L_1 can be considered constant between $[0, t_{on}[$ and between $]t_{on}, t_{sw}]$ with a discontinuity step at $t = t_{on}$. Substituting Equation (2.6) and Equation (2.7) into Equation (2.9) gives:

$$\int_0^{t_{on}} (V_{in} - V_{out}) \cdot dt + \int_{t_{on}}^{t_{sw}} (-V_{out}) \cdot dt = 0 \tag{2.10}$$

Since V_{in} and V_{out} are considered constant when the output filter is designed properly (i.e., C_{out} must be chosen large enough to provide an output voltage ripple that can be neglected), the integration of Equation (2.10) gives:

$$(V_{in} - V_{out}) \cdot (t_{on} - 0) - V_{out} \cdot (t_{sw} - t_{on}) = 0 \tag{2.11}$$

which simplifies to:

$$V_{in} \cdot t_{on} - V_{out} \cdot t_{sw} = 0 \tag{2.12}$$

Using Equation (2.12), the voltage conversion ratio M_{buck} of the buck converter can be calculated:

$$M_{buck} = \frac{V_{out}}{V_{in}} = \frac{t_{on}}{t_{sw}} = D \tag{2.13}$$

The average output voltage value V_{out} depends on the ratio of t_{on} to t_{sw}. In other words, the output voltage V_{out} depends exclusively on the duty cycle D of the PWM signal $V_{G(M1)}$ generated by the controller when it is operating in CCM. M_{buck} can vary between 0 and 1 (i.e., $M_{buck} \in [0, 1]$).

2.2.2.2 Boost Converter

The boost converter topology shown in Figure 2.8 is used when an output voltage V_{out} higher than the input voltage V_{in} is required. When the energizing power transistor M_1 (NMOS) is turned on, the current I_{L1} flowing through the inductor L_1 increases, while the diode D_1 is reverse biased. When M_1 turns off, the diode D_1 becomes forward biased and the inductor current I_{L1} is delivered to the load Z_{out}. As for the analysis of the buck converter, it is assumed for the following analysis that the inductor current never reaches zero during one complete period t_{sw} (i.e., the boost converter operates in the continuous conduction mode). The calculation is made when the steady-state has been reached.

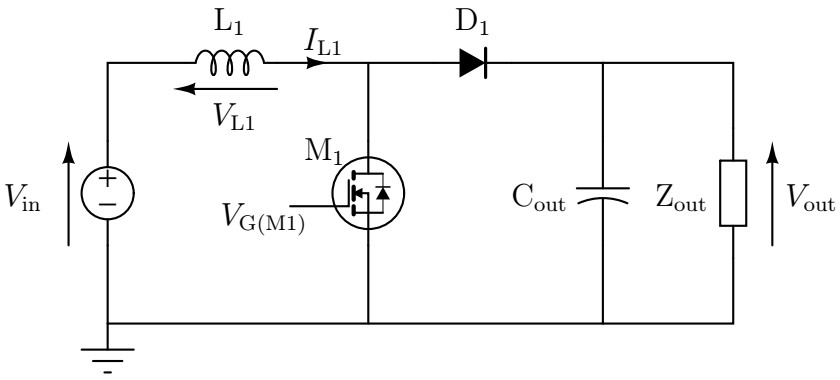

Figure 2.8: Boost converter schematic.

By using the same methodology as for the buck converter in Section 2.2.2.1, the voltage conversion ratio M_{boost} of the boost converter can be calculated:

$$M_{\text{boost}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{t_{\text{sw}}}{t_{\text{sw}} - t_{\text{on}}} = \frac{1}{1 - D} \tag{2.14}$$

Theoretically, the conversion ratio M_{boost} can vary between 1 and infinity (i.e., $M_{\text{boost}} \in [1, +\infty[$). This converter has a low input current ripple due to the inductor placed at the input, but it has a high output current ripple.

2.2.2.3 Inverting Buck-Boost Converter

The buck-boost converter circuit is used when a higher and/or lower output voltage V_{out} than the input voltage V_{in} is required (e.g., in case a 3.7 V lithium-ion battery supplies a 3.3 V circuit, the battery delivers only 3.0 V at the end of discharge). Its schematic is illustrated in Figure 2.9. When the energizing transistor M_1 is on, the current flowing through the inductor L_1 increases, and the diode D_1 is reverse biased. When M_1 is turned off, the inductor L_1 drains the current through the diode D_1 which becomes forward biased. This generates a negative voltage V_{out} at the output. For this analysis, the same hypothesis as for the previous ones are considered (i.e., the converter operates in continuous conduction mode and has reached the steady-state).

By using the same methodology as for the buck converter in Section 2.2.2.1, the voltage conversion ratio $M_{\text{buck-boost(inv)}}$ of the inverting buck-boost converter can be calculated:

$$M_{\text{buck-boost(inv)}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{-t_{\text{on}}}{t_{\text{sw}} - t_{\text{on}}} = \frac{-D}{1 - D} \tag{2.15}$$

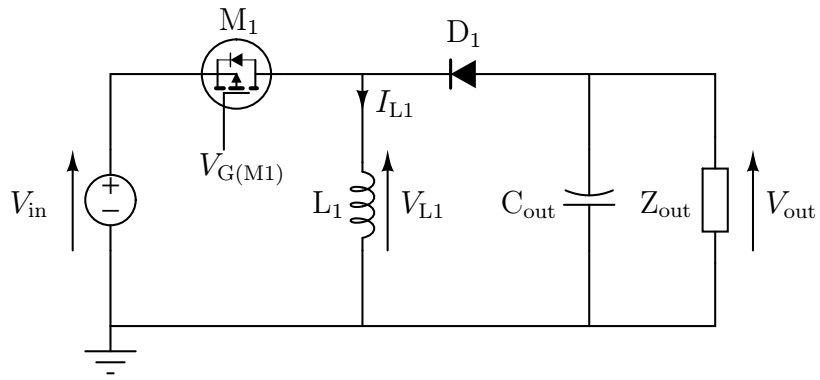

Figure 2.9: Inverting buck-boost converter schematic.

The conversion ratio $M_{\text{buck-boost(inv)}}$ can vary between minus infinity and 0 (i.e., $M_{\text{buck-boost(inv)}} \in]-\infty, 0[$). This means that the buck-boost converter provides a negative voltage at its output. This converter has a high input and a high output current ripple due to the inductor alternatively placed on the input and the output. Figure 2.10 shows the absolute value of the transfer functions of the buck, buck-boost, and boost converters.

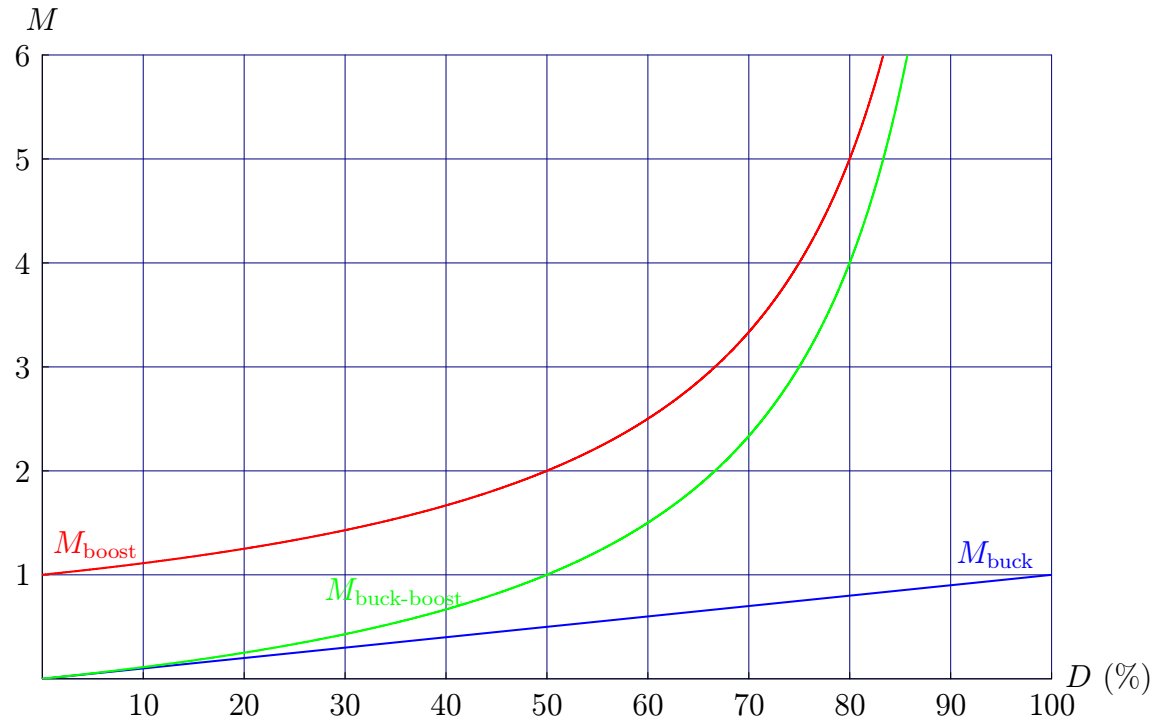

Figure 2.10: Buck, noninverting buck-boost, and boost transfer functions in CCM.

2.2.3 Advanced DC-DC Converter Topologies

Most of the today's mobile systems are powered by lithium-ion batteries providing a voltage between 3.0 V and 4.2 V and having to supply 3.3 V electronic circuits. Therefore, only topologies able to perform either step-up and step-down conversion

are of interest. Topologies with several switches and/or several energy storage devices are considered hereafter.

2.2.3.1 Noninverting Buck-Boost Converter

This converter is the noninverting version of the buck-boost converter presented in Section 2.2.2.3. It is the result obtained by connecting a buck and a boost converter together. It provides a positive output voltage V_{out} but requires two active switches M_1 and M_2, as shown in Figure 2.11. When the energizing transistors M_1 and M_2 are turned on, the current flowing through the inductor L_1 increases, and the diodes D_1 and D_2 are reverse biased. When M_1 and M_2 are turned off, D_1 and D_2 become forward biased and the inductor current generates V_{out}. In the basic noninverting buck-boost converter, the transistors M_1 and M_2 are driven simultaneously, but other control schemes are possible. Since M_1 is of type PMOS and M_2 of type NMOS, the driver circuitry is more complex than for the topologies analyzed previously.

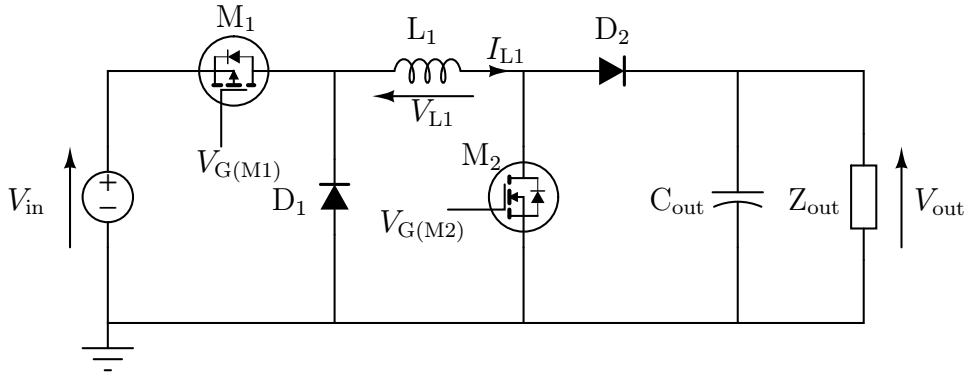

Figure 2.11: Noninverting buck-boost converter schematic.

By using the same methodology as for the buck converter in Section 2.2.2.1, the voltage conversion ratio $M_{\text{buck-boost}}$ of the noninverting buck-boost converter can be calculated:

$$M_{\text{buck-boost}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{t_{\text{on}}}{t_{\text{sw}} - t_{\text{on}}} = \frac{D}{1 - D} \tag{2.16}$$

The conversion ratio $M_{\text{buck-boost}}$ can vary between 0 and infinity (i.e., $M_{\text{buck-boost}} \in]0, +\infty[$).

2.2.3.2 Ćuk Converter

The Ćuk converter shown in Figure 2.12 can either increase or decrease the input voltage V_{in}. It also inverts the polarity, like the inverting buck-boost converter presented in Section 2.2.2.3. The Ćuk converter operates via capacitive energy transfer [41]. When M_1 is turned on, the diode D_1 is reverse biased, the current in both L_1 and L_2 increases, and the power is delivered to the load. When M_1 is turned off, D_1 becomes forward biased and the capacitor C_1 is recharged.

To determine the relation between V_{in} and V_{out}, two states must be considered:

- State 1: M_1 is turned on, D_1 is reverse biased ($0 < t < t_{\text{on}}$):

$$\begin{cases} V_{\text{L1}} = V_{\text{in}} \\ V_{\text{L2}} = V_{\text{out}} + V_{\text{C1}} \end{cases} \tag{2.17}$$

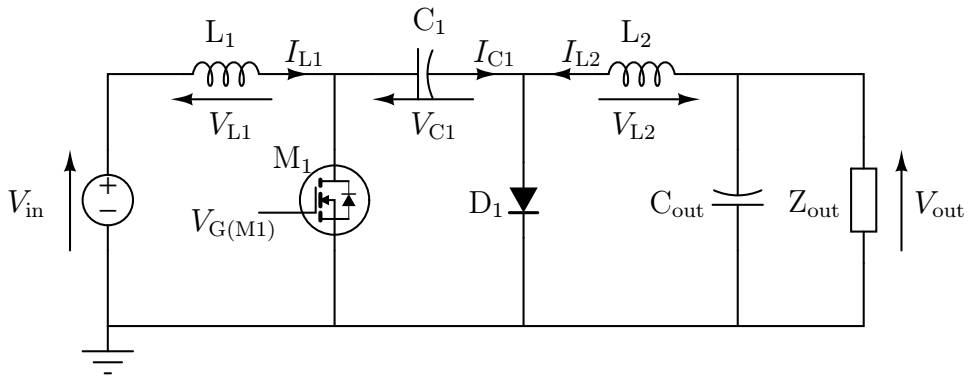

Figure 2.12: Ćuk converter schematic.

- State 2: M_1 is turned off, D_1 is forward biased ($t_{on} < t < t_{sw}$):

$$\begin{cases} V_{L1} = V_{in} - V_{C1} \\ V_{L2} = V_{out} \end{cases} \tag{2.18}$$

When the converter performs in the steady-state, the capacity C_1 is supposed to be large enough so that the voltage ripple across C_1 can be neglected. Thus, V_{L1} and V_{L2} are also constant between $[0, t_{on}[$ and $]t_{on}, t_{sw}]$ with a discontinuity step at $t = t_{on}$. The inductor current change through L_2 during steady-state operation expressed in Equation (2.9) is therefore written:

$$\int_0^{t_{on}} V_{L2} \cdot dt + \int_{t_{on}}^{t_{sw}} V_{L2} \cdot dt = 0 \tag{2.19}$$

By replacing V_{L2} in Equation (2.19) with the expressions from Equation (2.17) and Equation (2.18), it is obtained:

$$\int_0^{t_{on}} (V_{out} + V_{C1}) \cdot dt + \int_{t_{on}}^{t_{sw}} V_{out} \cdot dt = 0 \tag{2.20}$$

Integrating Equation (2.20) yields:

$$(V_{out} + V_{C1}) \cdot (t_{on} - 0) + V_{out} \cdot (t_{sw} - t_{on}) = 0 \tag{2.21}$$

$$\Longrightarrow V_{C1} = -V_{out} \cdot \frac{t_{sw}}{t_{on}} \tag{2.22}$$

The steady-state current change through L_1 is expressed by:

$$\int_0^{t_{on}} V_{L1} \cdot dt + \int_{t_{on}}^{t_{sw}} V_{L1} \cdot dt = 0 \tag{2.23}$$

By replacing V_{L1} in Equation (2.23) with the expressions from Equation (2.17) and Equation (2.18), it is obtained:

$$\int_0^{t_{on}} V_{in} \cdot dt + \int_{t_{on}}^{t_{sw}} (V_{in} - V_{C1}) \cdot dt = 0 \tag{2.24}$$

Integrating Equation (2.24) yields:

$$V_{\text{in}} \cdot (t_{\text{on}} - 0) + (V_{\text{in}} - V_{\text{C1}}) \cdot (t_{\text{sw}} - t_{\text{on}}) = 0 \tag{2.25}$$

$$V_{\text{in}} \cdot (t_{\text{on}} - 0) + \left(V_{\text{in}} + V_{\text{out}} \cdot \frac{t_{\text{sw}}}{t_{\text{on}}}\right) \cdot (t_{\text{sw}} - t_{\text{on}}) = 0 \tag{2.26}$$

$$V_{\text{in}} \cdot t_{\text{sw}} + V_{\text{out}} \cdot \frac{t_{\text{sw}}}{t_{\text{on}}} \cdot (t_{\text{sw}} - t_{\text{on}}) = 0 \tag{2.27}$$

Finally, the voltage conversion ratio $M_{\text{Ćuk}}$ of the Ćuk converter is given by:

$$M_{\text{Ćuk}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{-t_{\text{on}}}{t_{\text{sw}} - t_{\text{on}}} = \frac{-D}{1 - D} \tag{2.28}$$

The conversion ratio $M_{\text{Ćuk}}$ can vary between minus infinity and 0 (i.e., $M_{\text{Ćuk}} \in]-\infty, 0[$). The Ćuk topology has the inductor L_1 always connected to the input and the inductor L_2 always connected to the output, thus providing low input and output current ripples. The Ćuk converter can be made a bidirectional converter by replacing the diode D_1 through a power MOSFET. The drawback of the Ćuk converter is the need of two power inductors (i.e., L_1 and L_2) and an additional capacitor for the energy transfer (i.e., C_1), like the SEPIC and the zeta topologies presented in Section 2.2.3.3 and in Section 2.2.3.4, respectively.

2.2.3.3 SEPIC Converter

The *Single-Ended Primary Inductance Converter* (SEPIC) shown in Figure 2.13 is build using the boost converter topology (see Figure 2.8) and by inserting a capacitor C_1 between the inductor L_1 and the diode D_1. This capacitor obviously blocks any DC current path between the input and the output. However, the anode of the diode D_1 must be connected to a defined potential. This is accomplished by connecting D_1 to ground through a second inductor, L_2. This inductor L_2 can be separate from L_1 or wound on the same core. The SEPIC topology can generate an output voltage V_{out} above, below or equal to the input voltage V_{in}.

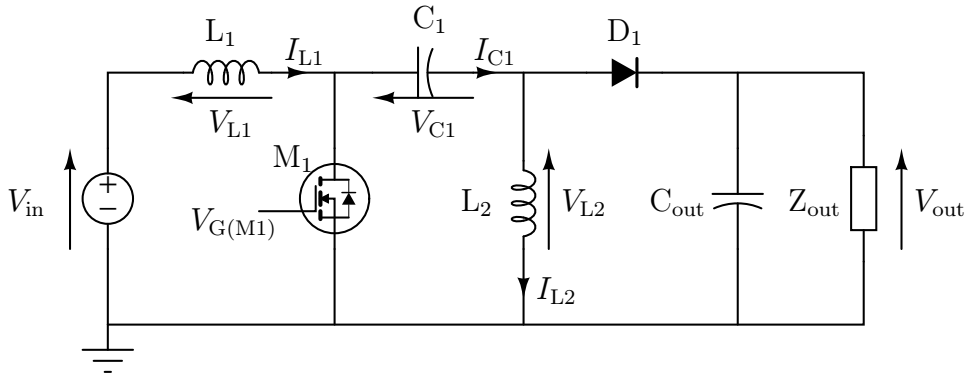

Figure 2.13: SEPIC converter schematic.

As shown in Figure 2.13, when the energizing transistor M_1 is turned on, the input voltage V_{in} appears across the inductor L_1 and the current I_{L1} increases. Energy is also stored in the inductor L_2 as soon as the voltage across the capacitor C_1 appears across L_2. The diode D_1 is reverse biased during this period. But when M_1 turns

off, D_1 conducts. The energy stored in L_1 and L_2 is delivered to the output, and C_1 is recharged by L_1 for the next period. By using the same methodology as for the Ćuk converter in Section 2.2.3.2, the voltage conversion ratio M_{SEPIC} of the SEPIC converter is given by:

$$M_{\text{SEPIC}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{t_{\text{on}}}{t_{\text{sw}} - t_{\text{on}}} = \frac{D}{1 - D} \tag{2.29}$$

The conversion ratio M_{SEPIC} can vary between 0 and infinity (i.e., $M_{\text{SEPIC}} \in]0, +\infty[$). The SEPIC topology has the inductor L_1 always connected to the input, thus providing a low input current ripple. Since there is no inductor always connected to the output, this topology provides a high output current ripple.

2.2.3.4 Zeta Converter

The zeta converter shown in Figure 2.14 is build by interchanging the transistor M_1 and the diode D_1 from the SEPIC topology, and by also interchanging the I/O power terminals. Thus, it is also known as the inverse of SEPIC converter. The operating principle of the zeta converter is comparable to the SEPIC converter. At the beginning of each switching period, the energizing transistor M_1 is turned on and the current through the inductor L_1 increases. During this phase, the diode D_1 is reverse biased and the energy stored in the capacitor C_1 makes the current through the inductor L_2 to increase (i.e., energy is transferred to the output). When M_1 is turned off, the current in the inductor L_1 forces D_1 to turn on. The energy stored in the inductor L_1 is transferred to the capacitor C_1 and the current through the inductor L_2 decreases.

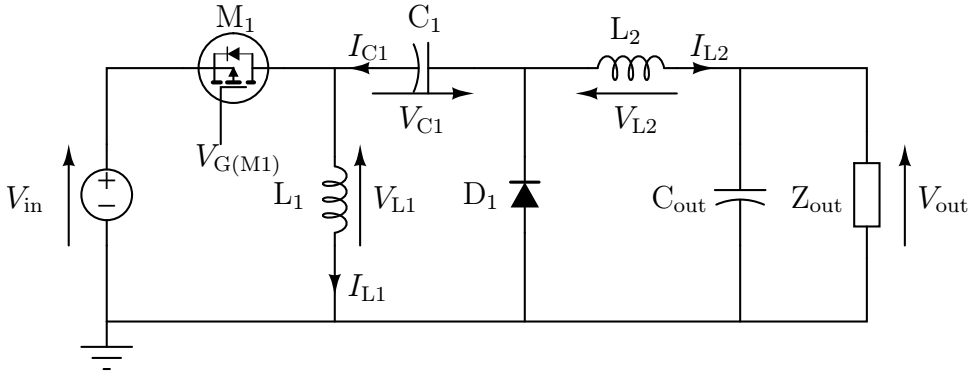

Figure 2.14: Zeta converter schematic.

By using the same methodology as for the Ćuk converter in Section 2.2.3.2, the voltage conversion ratio M_{zeta} of the zeta converter is given by:

$$M_{\text{zeta}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{t_{\text{on}}}{t_{\text{sw}} - t_{\text{on}}} = \frac{D}{1 - D} \tag{2.30}$$

The conversion ratio M_{zeta} can vary between 0 and infinity (i.e., $M_{\text{zeta}} \in]0, +\infty[$). The zeta topology has the inductor L_2 always connected to the output, thus providing low output current ripple. Since there is no inductor always connected to the input, this topology provides high input current ripple.

The zeta converter is very similar to the SEPIC converter which would be powered from its output side. If the diode D_1 of the SEPIC converter shown in Figure 2.13 is

replaced by a transistor, the topology presented in Figure 2.15 is obtained. If M_2 is always turned off (M_1 is the switching transistor), its body diode makes this topology exactly equivalent to the SEPIC converter shown in Figure 2.13. Now, if the I/O terminals from Figure 2.15 are interchanged (i.e., V_{in} becomes V_{out}, and V_{out} becomes V_{in}), and if the transistor M_1 is always turned off (M_2 is the switching transistor), this topology becomes exactly equivalent to the zeta converter shown in Figure 2.14.

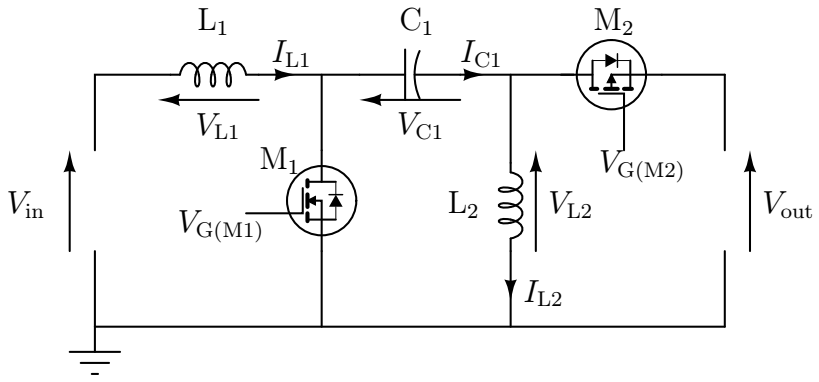

Figure 2.15: SEPIC converter forward - Zeta converter backward.

The topology shown in Figure 2.15 provides bidirectional conversion, with step-up and step-down capability and with the same transfer function in both directions. However, some drawbacks exists. First, two inductors are required, which is unwanted in mobile applications, since inductors are difficult to integrate. Second, it is an unsymmetrical topology due to the positions of the inductors, therefore providing different input and output performances (e.g., current ripple).

2.2.3.5 H-Bridge Converter

The H-bridge topology (also called *full-bridge*) shown in Figure 2.16 is derived from the noninverting buck-boost topology shown in Figure 2.11. It is a completely symmetrical topology, which allows the energy to flow in both directions (i.e., from input to output, and from output to input). Because of its switches configuration, the buck, buck-boost, and boost topologies can be obtained by turning on and off the transistors, as illustrated in Figure 2.17.

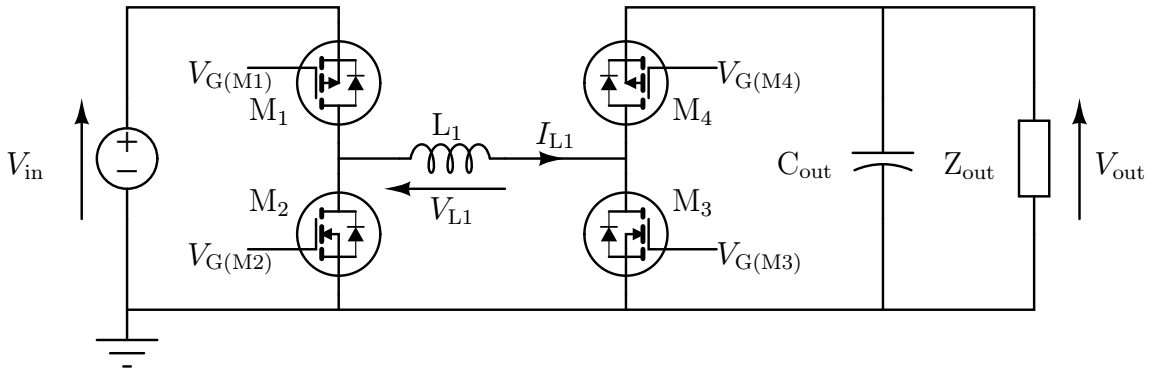

Figure 2.16: H-bridge converter schematic (full-bridge).

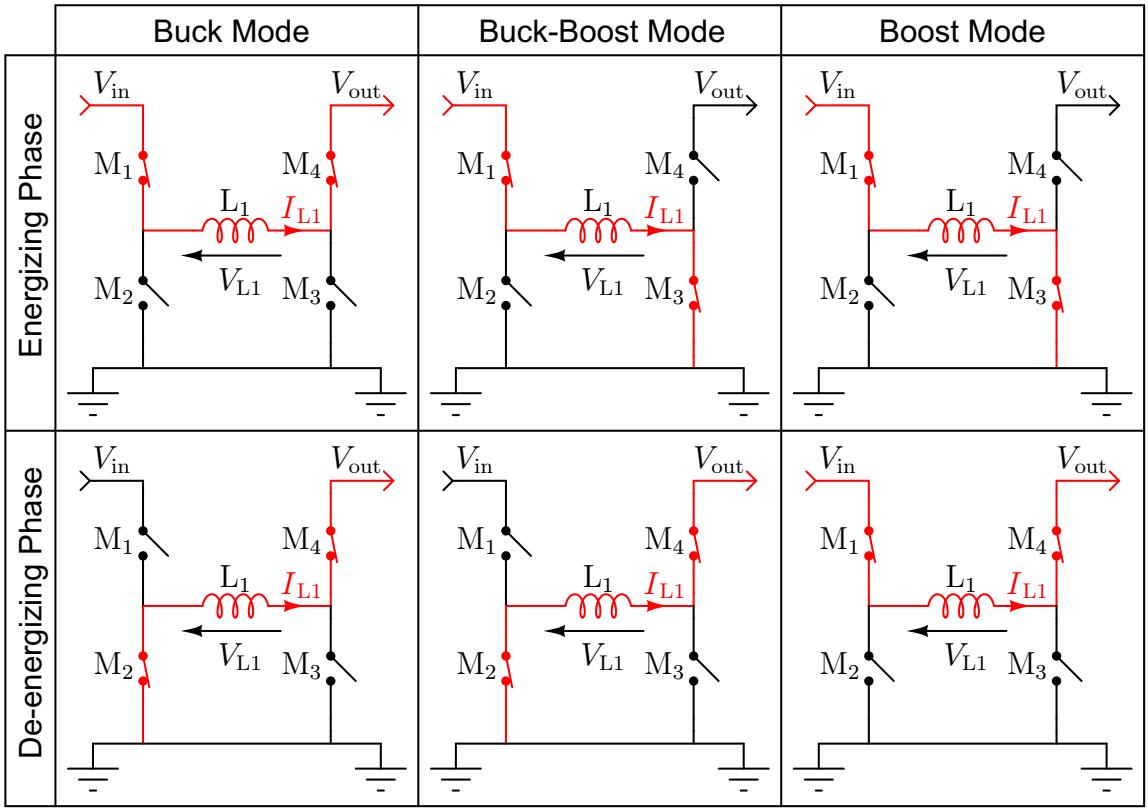

Figure 2.17: Switching modes in an H-bridge converter.

The H-bridge topology requires only one inductor (L_1), thus making it well suited for integrated DC-DC converters. Because of its advantages (e.g., low passive devices count, high flexibility, high efficiency in high and low power conversion), the H-bridge topology was chosen for designing the IPC.

However, the H-bridge topology has also some drawbacks. If NMOS transistors are used as high-side switches, a charge pump is needed to provide a sufficient gate-drive voltage. If PMOS transistors are used as high-side switches (see M_1 and M_4 in Figure 2.16), a minimum voltage at the input V_{in} and output V_{out} is required. A negative driving voltage to turn on M_1 and M_4 would be a solution to this problem, but only very few commercially available CMOS technologies support both positive as well as negative voltages. Another option for reducing the effects of this problem is to use low-threshold voltage transistors. More investigations concerning the integration in a CMOS technology of an H-bridge are done in Section 3.2.

2.3 Switching Controllers Considerations

In a switching converter (e.g., in the buck converter shown in Figure 2.4), the controller pilots the power devices, and therefore acts directly on the power conversion efficiency. Several tasks are accomplished by the controller. One of them consists of protecting the power devices against destructive effects (e.g., overcurrent, temperature overstress) by monitoring the currents, the voltages, and the temperature. However, its principal role is to regulate the output voltage V_{out} to the requested voltage value, as it was

illustrated in Figure 2.4. To do this, the controller can be designed to use different operation control methods, each of them adapted to a specific case. These operation control methods are discussed in Section 2.3.1. The two most popular regulation principles (i.e., voltage mode, current mode) are analyzed in Section 2.3.2.

2.3.1 Operation Control

Mainly two different modulations are used in today's DC-DC converters, each optimized for a specific load condition (i.e., a different output power range). The first is the pulse-width modulation (PWM) operation control method, which is well suited for high power conversions. The second is the pulse-frequency modulation (PFM) operation control method, which is better suited for low power conversions. By combining both of these operation control methods into one controller, the converter can be made very efficient over a wide range of output power [42].

2.3.1.1 Pulse-Width Modulation

With the pulse-width modulation control illustrated previously in Figure 2.5, the regulation of output voltage is achieved by varying the duty cycle D of the switching devices, keeping the frequency of operation constant. Usually, the operation control by pulse-width modulation is the preferred method, since constant frequency operation greatly simplifies the design of the regulation feedback loop and the output ripple filter, thus avoiding stability issues. However, since the switching frequency is constant in the PWM control scheme, the switching losses (e.g., the losses due to the charging/discharging of the gate and output capacitances of the power transistors) are independent of the load current. The direct consequence is that PWM becomes inefficient when a light load is supplied, because the switching losses dominate the conduction losses, which are load dependent.

2.3.1.2 Pulse-Frequency Modulation

To overcome the dramatic efficiency reduction in lightly loaded PWM converters, an additional operation control scheme called pulse-frequency modulation (PFM) has been developed. PFM is a nonlinear operation scheme in which pulse trains are applied to the energizing switch to maintain the output voltage within the preset voltage range. This mode lowers the frequency of the switching-cycle events, therefore lowering the switching losses, which are dominant to the conduction losses at light output loads (i.e., when the requested output current is low). Although PFM control has become prevalent in battery-operated mobile equipment because its light-load efficiency exceeds that of PWM, PFM is more difficult to design because this operation control scheme has some important issues concerning the stability in the frequency domain, since it is a variable-frequency control scheme. PFM allows to extend battery life of the mobile equipment in the suspend and standby modes of operation. However, the low frequencies can cause switching noise to enter the audio band. This can be avoided by sizing the passives so that the PFM converter is forced to operate above the audio band at the minimum load condition.

There are several PFM operation schemes, such as single-pulse PFM, multi-pulse PFM, and burst-mode PFM. However, all operate according to the basic principle of initiating switching cycles only as needed to maintain the output voltage. Figure 2.18

shows the waveforms produced by a burst-mode PFM controller. The pulse trains represent the PFM operation control. The ripple on the output voltage V_{out} has been increased for readability reason. In practice, this voltage ripple does not exceed 150 mV peak-to-peak voltage.

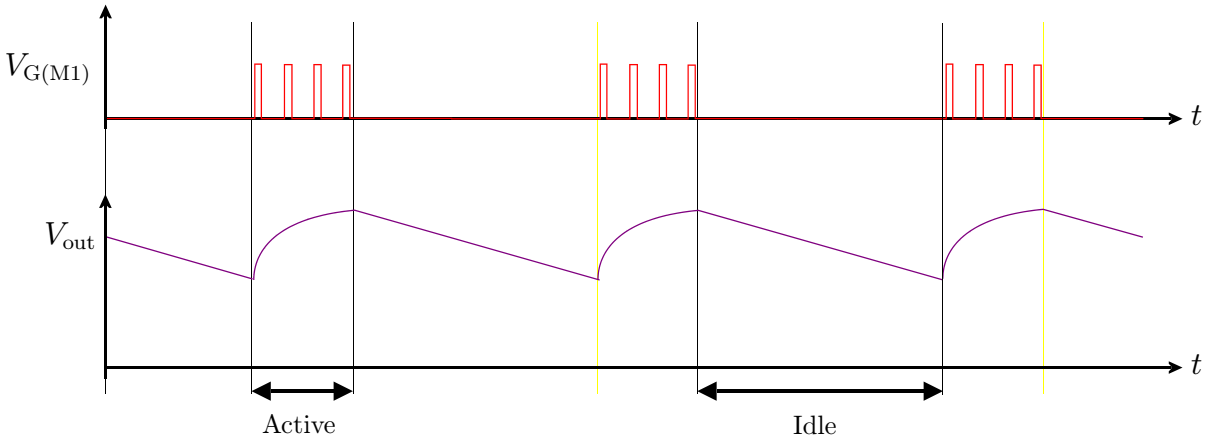

Figure 2.18: Signal waveforms of the PFM operation control in steady-state. When the current requested by the load decreases, the idle time increases, and therefore the frequency also decreases.

In DC-DC converters for mobile equipment, the PFM operation control is never used standalone. It is always coupled to a PWM controller. The current trend in todays DC-DC converters is to increase the switching frequency of the controllers, so that the passive device sizes (i.e., inductors and capacitors) can be reduced. To enable future on-chip hybrid integration of power inductors [38], the switching frequencies are approaching 10 MHz and they will continue to increase [28]. Therefore, the most efficient way to reach high efficiency in both heavy and light load conditions is to combine both PWM and PFM operation control schemes [42].

2.3.2 Regulation Mode

Three main regulation strategies exist in DC-DC converters. The first and most intuitive one, called the *voltage mode regulation* and presented in Section 2.3.2.1, consists of sensing a voltage proportional to the output voltage for regulating it (i.e., like it is done in a linear voltage regulator). The second one, called the *current mode regulation* and presented in Section 2.3.2.2, consists of sensing a voltage proportional to the output voltage and using it as a set value for an inner current control loop to regulate the output voltage. The third one, called the *hysteretic mode regulation* and presented in Section 2.3.2.3, does use a comparator instead of an error amplifier for regulating the output voltage.

All of these methods have their own advantages and drawbacks [43]. There is no single regulation mode which is optimum for all applications. In 1978, the introduction of the current mode regulation seemed to be the answer for solving the problems in voltage mode regulation [44]. Moreover, if voltage mode regulation is updated with modern circuit and process developments, it is a viable contender to the current mode regulation.

2.3.2.1 Voltage Mode Regulation

The voltage mode regulation was the approach used for the first switching regulator designs. Figure 2.19 shows an example of a basic voltage mode regulation based on a boost converter [43]. In the voltage mode regulation, there is only a single voltage feedback loop. This loop is generally constituted of a resistive network acting as a voltage divider, and a compensator network made with resistors and capacitors for ensuring loop stability. The pulse-width modulation is performed by comparing the the error amplifier output voltage V_{EA} with the ramp waveform V_{osc}.

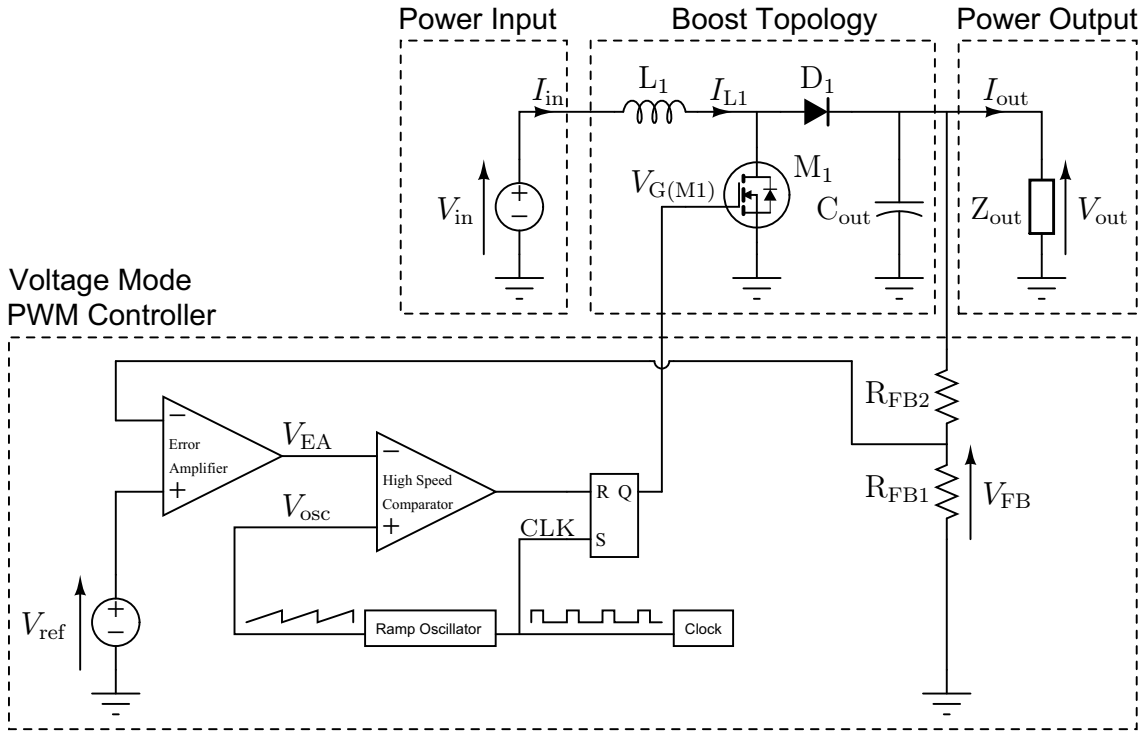

Figure 2.19: Schematic of the voltage mode regulation principle.

Figure 2.20 shows the waveforms of the signals in a voltage mode PWM controller. The ramp carrier V_{osc} (i.e., sawtooth signal) is generated by using the clock pulses (i.e., CLK) as the command for the charging of a capacitor at constant current.
The advantages of the voltage mode regulation are [43]:

- A single feedback loop is easier to design and analyze.
- A large amplitude sawtooth waveform provides good noise margin for a stable modulation process.
- An accurate CMOS voltage sensor is easy to design and nearly lossless.

The drawbacks of the voltage mode regulation are [43]:

- Any change in input voltage V_{in} or in the output voltage V_{out} must first be sensed as an output change and then corrected by the feedback loop. This provides slower transient response.

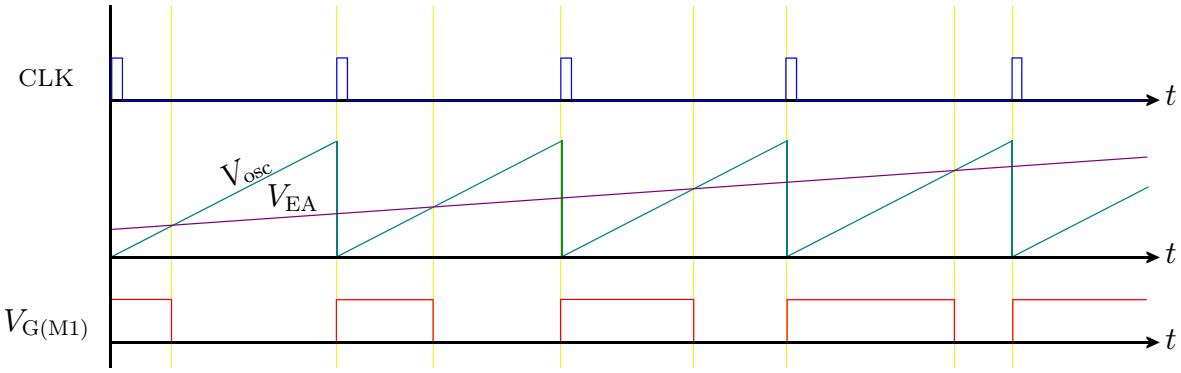

Figure 2.20: Signal waveforms of the voltage mode regulation principle shown in Figure 2.19.

- The compensation is further complicated by the fact that the loop gain depends on the input voltage V_{in}.

2.3.2.2 Current Mode Regulation

As analyzed previously, the disadvantages of the voltage mode regulation are relatively significant. Therefore, as the current mode regulation was introduced in 1978 [44], the designers were highly motivated to consider the different regulation possibilities offered by the current mode (e.g., peak, valley, average current mode), because it seemed to be able to overcome all the drawbacks of the voltage mode regulation. As shown in Figure 2.21 [43], the peak-current mode regulation uses the oscillator only as a fixed frequency pulse generator. The ramp waveform is no more generated by the oscillator.

Figure 2.22 shows the waveforms of the signals in a peak-current mode PWM controller. The ramp carrier is replaced by a voltage image of the current flowing through the inductor. It is generated by using the clock pulses as the command for the charging of a capacitor at constant current.
The advantages of the peak-current mode regulation are [43]:

- Since the inductor current I_{L1} rises with a slope determined by the difference between V_{in} and V_{out}, this waveform responds immediately to input voltage changes, eliminating both the delayed response as well as the gain variation with changes in the input voltage.

- Since the error amplifier is now used to command an output current rather than an output voltage, the effect of the output inductor is minimized and the filter now offers only a single pole to the feedback loop. This allows both simpler compensation and a higher gain bandwidth product over a comparable voltage mode circuit.

- An additional benefit of current mode regulation includes an inherent pulse-by-pulse current limiting by merely clamping the command from the error amplifier.

While the improvements offered by current mode regulation are impressive, this method also comes with its own unique set of problems, which must be solved in the design process. The drawbacks of the peak-current mode regulation are [43]:

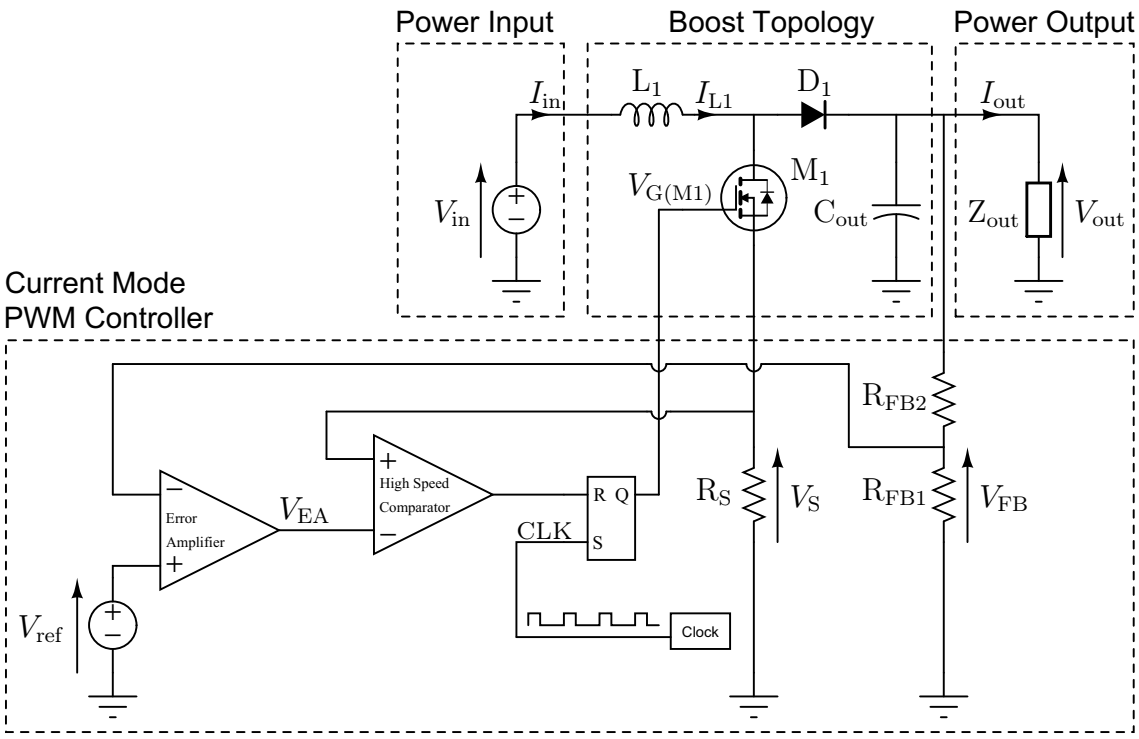

Figure 2.21: Schematic of the peak-current mode regulation principle.

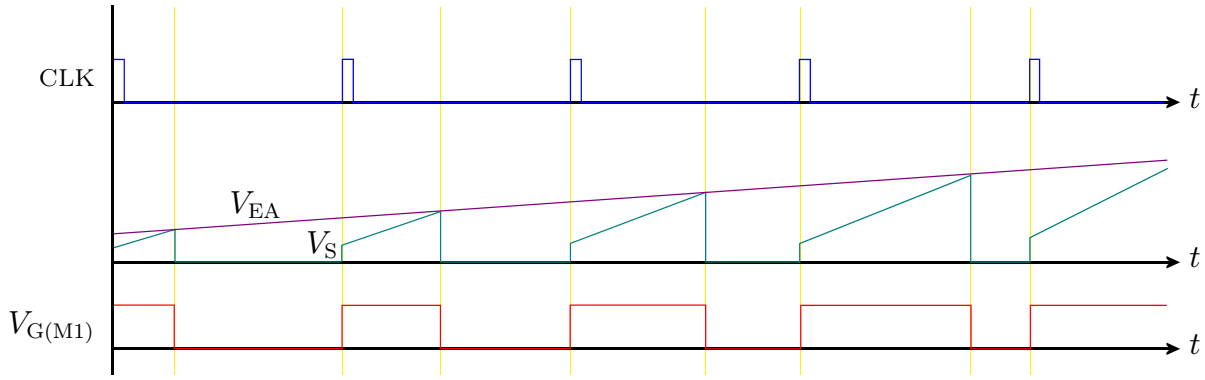

Figure 2.22: Signal waveforms of the peak-current mode regulation principle shown in Figure 2.21.

- There are two feedback loops, making the circuit analysis more difficult.
- The control loop becomes unstable at duty cycles above 50%, unless slope compensation to the voltage image of the inductor current is added.
- Since the control modulation is based on a signal derived from the output current, oscillations in the power stage can insert noise into the control loop.

While current mode regulation corrects many of the limitations of voltage mode regulation, it also creates new challenges for the design engineers. However, with the knowledge gained from the most recent developments in power control technology [45], [46], [47], a re-evaluation of voltage mode regulation indicated that there are efficient

ways to correct its major weaknesses [48]. This is why the voltage mode regulation was preferred to the current mode regulation for the design of the IPC.

2.3.2.3 Hysteretic Mode Regulation

The hysteretic regulation mode is the only mode that does not employ an error amplifier, but uses a comparator instead [49]. Both hysteretic voltage mode and hysteretic current mode control exist. The provided output voltage is controlled within an interval. In a buck converter like the one shown in Figure 2.6, an hysteretic voltage mode control of the output voltage V_{out} would consist in turning on the energizing power transistor M_1 when V_{out} is too low, and turning M_1 off when V_{out} is large enough again. An example of an hysteretic mode buck converter is shown in Figure 2.23.

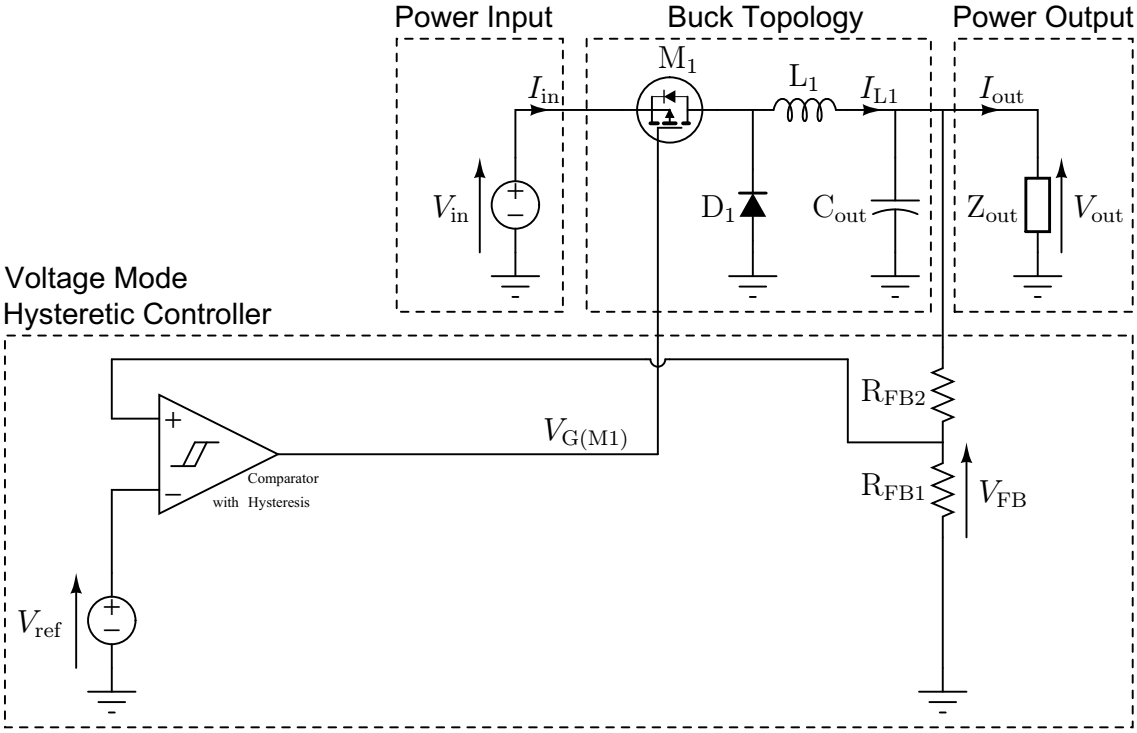

Figure 2.23: Schematic of the hysteretic voltage mode regulation principle by using a comparator with an hysteresis. A typical value for the hysteresis is 10 mV.

The hysteretic voltage mode control is very simple to build since no oscillator is needed. The regulation loop reacts very rapidly to changes in the voltages and currents of the line and the load, since they depend only on the propagation delays and not also on waiting for an oscillator to start a new cycle. This regulation mode does not need a loop compensation. The designs are simplified and the instability issues are avoided. However, the regulation behaves a little bit unpredictably when the range of the switching frequency needs to be defined. Since no oscillator is present, many parameters influence the switching frequency. Not all converter topologies are adapted to be easily controlled by an hysteretic regulation. Table 2.1 summarizes the characteristics of the three main regulation modes presented in Section 2.3.2.

Table 2.1: Summary of the characteristics of the different regulation modes.

Characteristic	Voltage Mode	Current Mode	Hysteretic Mode
Output Voltage Ripple	Low	Low	High
Loop Bandwidth	Medium	Low	High
Loop Compensation	Difficult	Easy	Not Needed
Fixed Frequency Compliant	Yes	Yes	No
Large V_{in} to V_{out} Differences	Possible	Difficult	Possible

Chapter 3

Technological Design Considerations

In this chapter, the specifications of the bidirectional DC-DC converter developed in this research work for low power mobile systems are presented [50]. The choice of the CMOS technology and the choice of the power transistors type used for the design are explained here. The floorplanning and packaging information used for the prototypes are also reported.

3.1 Bidirectional DC-DC Converter Specifications

As introduced in Chapter 1, the goal of this research work is to present the proof of concept of an integrated bidirectional DC-DC converter for mobile systems, which will be the basis for energy harvesting mobile systems in the mid-term future.

3.1.1 Electrical and Mechanical Specifications

The initial demand for a bidirectional DC-DC converter came from the german batteries manufacturer Bullith Batteries AG. Two different battery chemistries of customized lithium-polymer batteries are provided by this company.

The most usual lithium-ion battery chemistry type is the lithium-graphite type (Graphite-$LiCoO_2$ for 3.7 V systems), which provides performances comparable to the standard lithium-polymer batteries available on the market. The high-end battery type is the lithium-titanate (LiTi-$LiCoO_2$ for 2.3 V systems), which provides a much longer battery lifetime. Indeed, the remaining battery capacity still resides above 80% after 3000 charging/discharging cycles.

Customized batteries are specifically manufactured for different applications. The size and the capacity of the battery is adjusted for medical, robotic, mobile, and security products. Two product categories must be distinguished: the 2000 mA and below powered products and the 2000 mA and above products. The first category makes full use of the power transistors integrated into the bidirectional DC-DC converter, while the second category needs external power transistors to achieve the high current requirements. Due to the wide applications range, the bidirectional DC-DC converter must be adaptable and configurable to achieve high currents and high efficiency in each application.

The bidirectional DC-DC converter must be a high efficiency buck-boost DC-DC converter that operates from input voltages above, below, or equal to the output voltage. Since today almost all state-of-the-art mobile equipment uses a 3.3 V (or below)

supply voltage, it has been decided not to support voltages above 3.6 V. The topology incorporated in the converter must provide a continuous transfer function through all operating modes so that the supplied output voltage is independent of the battery voltage. The switching frequency must be programmable. Low quiescent current is necessary to maximize the battery lifetime in mobile applications. Other features include shutdown, soft-start control, and automatic current limit for the internal power transistors. A thermally enhanced package is mandatory for the bidirectional DC-DC converter (further details about packaging and bonding are provided in Section 3.3).

The high-level block diagram shown in Figure 3.1 gives an overview of the different parts contained in the bidirectional DC-DC converter. As defined in Section 1.3.2, an intelligent battery regroups a rechargeable lithium-polymer battery and a DC-DC converter ASIC. The load represents the mobile system that must be supplied by the intelligent battery. The battery charger, when connected to the mobile system, supplies the load and the battery simultaneously. A microcontroller located in the mobile system can be used for monitoring some physical quantities, like voltages, currents, and the temperature of the silicon die. The bidirectional DC-DC converter ASIC also requires some external passive components. For example, the power inductor is not implemented on the silicon substrate; a resistor is used for adjusting the switching frequency of the PWM controller; the compensation of the regulation loop is done externally by adjustable passive elements for more design flexibility.

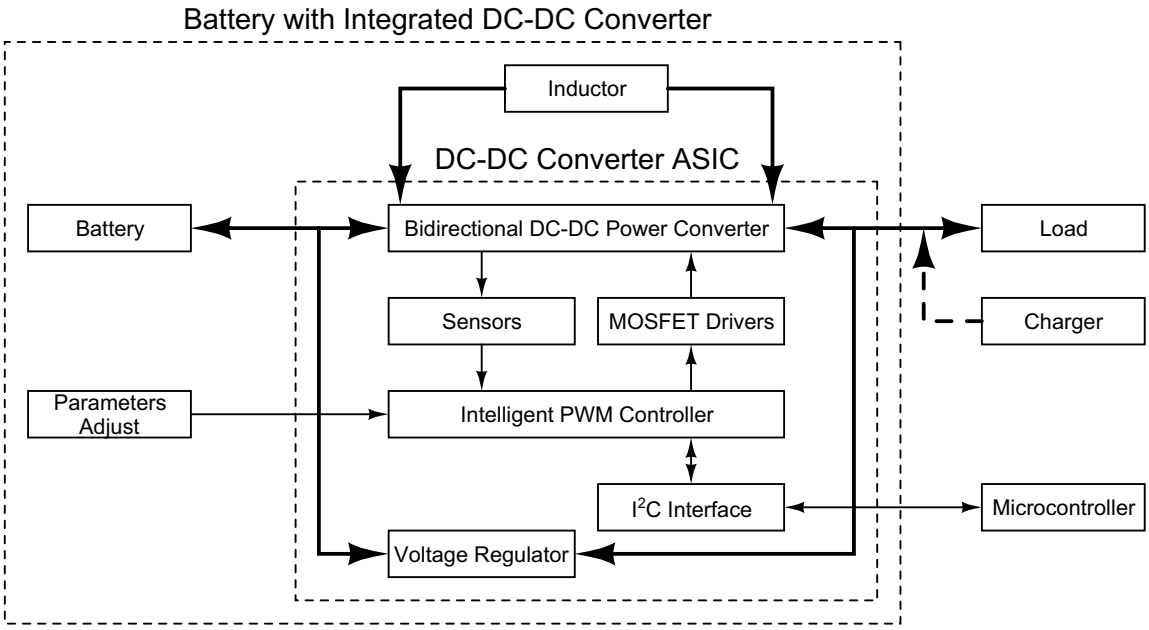

Figure 3.1: Block diagram of the IPC and its environment.

The DC-DC converter ASIC shown in Figure 3.1 is constituted of six main units. The bidirectional DC-DC power converter unit contains the power transistors used for the power converter, the role of which is to perform the voltage conversion. These power transistors are in an H-bridge configuration, since this topology allows the best performance in systems with a bidirectional energy flow (see Section 2.2.3.5 for more details about the H-bridge topology). The MOSFET drivers unit comprises the gate drivers of the power transistors from the H-bridge, the level shifters, and the anti-crossconduction logic of the H-bridge. The sensors unit contains the voltage and

current sensing circuits that are necessary for protecting the bidirectional DC-DC power converter unit against overcurrents. The intelligent PWM controller unit contains various complex analog units needed for the voltage regulation (e.g., triangular oscillator, PWM modulator, error amplifier, discontinuous conduction mode control, overcurrent detection). The I^2C Interface unit provides a digital interface to an external microcontroller. This 2-wire digital interface can be used for monitoring of converter states, operating modes, internal voltages, internal currents, and monitoring the temperature of the silicon die. It is the only full digital unit contained in the DC-DC converter ASIC. The voltage regulator unit provides the internal core supply voltage V_{core} for all the previously described units. The generated core voltage is independent of the battery voltage (i.e., independent of the battery charge state). The detailed CMOS designs (i.e., down to the transistor level) of the units presented here are given in Chapter 5. The main features of the designed bidirectional DC-DC converter are:

- single inductor, bidirectional H-bridge topology
- 1.8 V to 3.6 V input voltage range (V_{batt}, battery side)
- 1.8 V to 3.6 V output voltage range (V_{load}, load and charger side)
- externally adjustable output voltage (V_{load})
- integrated power transistors up to 2000 mA continuous output current
- operation with V_{batt} above, below or equal to V_{load}
- synchronous rectification for high efficiency at high currents
- adjustable oscillator frequency through external resistor
- soft-start function to limit inrush startup current
- microcontroller I^2C interface for controlling, monitoring and testing
- small thermally enhanced package

3.1.2 Economical Considerations

When an ASIC has to be designed, the costs always occupy a central position. For this research work, the cost of a silicon die processed in mass production was analyzed. The cost estimations are based on the specifications of the bidirectional DC-DC converter given in Section 3.1.1.

The first step for calculating a cost estimation consists in evaluating the die yield, which represents the number of working dies divided by the total number of dies produced. J. Hennessy and D. Patterson use a modified Bose-Einstein parametric yield model [51], which is nowadays usually used for estimating the yield of modern silicon processes. The Hennessy and Patterson die yield estimation y_{D} is given by:

$$y_{\text{D}} \approx y_{\text{W}} \cdot \left(1 + \frac{\gamma \cdot A}{\alpha}\right)^{-\alpha} \tag{3.1}$$

where y_W is the wafer yield, γ the defect density in defects per cm^2, A the die area in cm^2, and α the process complexity factor.

Through the wafer yield y_W, this cost model takes into account that a certain fraction of wafers are defective, due to mis-processing. The wafer yield y_W approaches 100% when the process is mature and the processing line is running mass production.

The defects density γ was about 0.6 to 1.2 defects per cm^2 in 1996, down from approximately 2 in 1990. In 2000, γ was down further to 0.4 to 0.8. The defect density γ is dependent of the process complexity (i.e., the number of process steps), the type of processed run (e.g., multi-project wafer run, pilot run, mass production run), and the quality of the silicon used for manufacturing the silicon ingots (e.g., the sand employed should contain only a few radioactive isotopes of silicon once the ingot was manufactured, because if a radioactive atom of silicon decays after it has been built into a CMOS circuit, the ejected decay product can produce enough mass and energy to damage the transistor structures of the circuit) [51].

The die area A is the area occupied by the designed layout, which can be square or rectangular. The coefficient α corresponds to the process complexity factor and therefore does not represent a physical quantity. A typical value of α for a 2-metal 0.8 µm CMOS process from 1992 is taken to be equal to 2. For a 4-metal 0.35 µm CMOS process from 1996, α is taken equal to 3. For a 6-metal 0.18 µm CMOS process from 2000, α is taken equal to 4. For more complex processes such as BiCMOS or GaAs processes, the value of α is higher [51].

To calculate the exact number of dies N that can be placed on a silicon wafer of a radius r, each of them occupying an area A, a complex computer algorithm has to be used [52]. However, such numerical iterative algorithms are not convenient for giving rapid estimations of the die counts per wafer. A simple expression for estimating an approached value of N is given by O. Trapp [53]:

$$N \approx \frac{\pi \cdot \left(r - \sqrt{A}\right)^2}{A} \tag{3.2}$$

This expression does not consider different aspect ratios of a design (i.e., square design or rectangular design) but it is accurate enough for giving a first estimation in the targeted application, which consists in a small die size (between 2.3 mm^2 and 5 mm^2 die area) compared to the huge wafer size (200 mm or 300 mm diameter). The calculated value of N corresponds to the worst case approximation (i.e., an under-estimated value). More accurate expressions that take into account the aspect ratio of the design are proposed by A. Ferris-Prabhu [54].

The wafer costs c_W are constant in a given process and are mainly dependent of the process complexity (i.e., c_W is independent of the design size). The die costs c_D are calculated with the following expression:

$$c_D = \frac{c_W}{N \cdot y_D} \tag{3.3}$$

Finally, the packaged chip costs c_C are given by:

$$c_C = \frac{c_D + c_T + c_P}{y_{FT}} \tag{3.4}$$

where c_D are the die costs, c_T the testing costs (which are proportional to the needed testing time), c_P the packaging costs (i.e., costs of the leadframe and the die attach) and y_{FT} the final test yield.

Table 3.1 shows estimations of the costs for two different die areas produced in a 6-metal layers 0.18 µm CMOS technology. The mask's costs and the testing costs are not included in the calculation of these estimations. The costs of a full mask set in a 0.18 µm mixed-signal CMOS technology consisting in 36 masks were as high as 350000 € in the year 2004.

Table 3.1: Estimations of die costs in 2004 with a 0.18 µm 6-metal CMOS process.

A	γ	α	y_W	y_D	r	N	c_W	c_D
$1525\times1525\,\mu m^2$	$0.6\,cm^{-2}$	4	90%	88.7%	100 mm	13099	4000 €	0.305 €
$1525\times3240\,\mu m^2$	$0.6\,cm^{-2}$	4	90%	87.3%	100 mm	6078	4000 €	0.658 €

3.2 CMOS Technology Considerations

To demonstrate the novel solutions developed for this thesis and exposed in Chapter 4, two prototypes of DC-DC converters were manufactured. The choice of the most suited foundry technology plays a very important role in the bidirectional DC-DC converter performances (e.g., die temperature, current densities, conduction losses). The european research institutes have access to several commercial CMOS and BiCMOS technologies of different foundry houses through the Europractice program managed by the belgian IMEC and the german Fraunhofer IIS research institutes. Therefore, a technology provided through the Europractice program was chosen.

3.2.1 Selection of the CMOS Technology

Only mixed-signal technologies are suitable for this research project, since digital, analog and power electronics have to cohabit on a single silicon die. The controller of the bidirectional DC-DC converter requires digital electronics. Therefore, only deep sub-micron technologies below 0.5 µm are considered in this analysis. Since the DC-DC converter includes many different analog sensors, high quality analog cells (e.g., resistors, capacitors) in a fully qualified CMOS process with very well modeled devices are necessary. In November 2003, the time at which the development of the bidirectional DC-DC converter was started, only two CMOS technologies achieved these exigencies within the Europractice program. It was the AMS H35 process of Austria Microsystems (Austria) and the UMC L180 process of United Microelectronics Corporation (Taiwan).

3.2.1.1 Description of the AMS H35 Technology

The AMS H35 is a 0.35 µm CMOS technology with a *high voltage* (HV) option. It is a so called 2P4M process, which means that two polysilicon layers and four metal layers are provided for the layout designer. This arrangement is illustrated in Figure 3.2.

The fourth metal layer is an optional thick power metal layer, which is a necessity in integrated circuits that must handle high currents. The core technology is based on 3.3 V transistors with a minimum channel length L of 350 nm. For the input/output interfacing (I/O circuitry), 5 V transistors are provided. Only regular threshold voltage

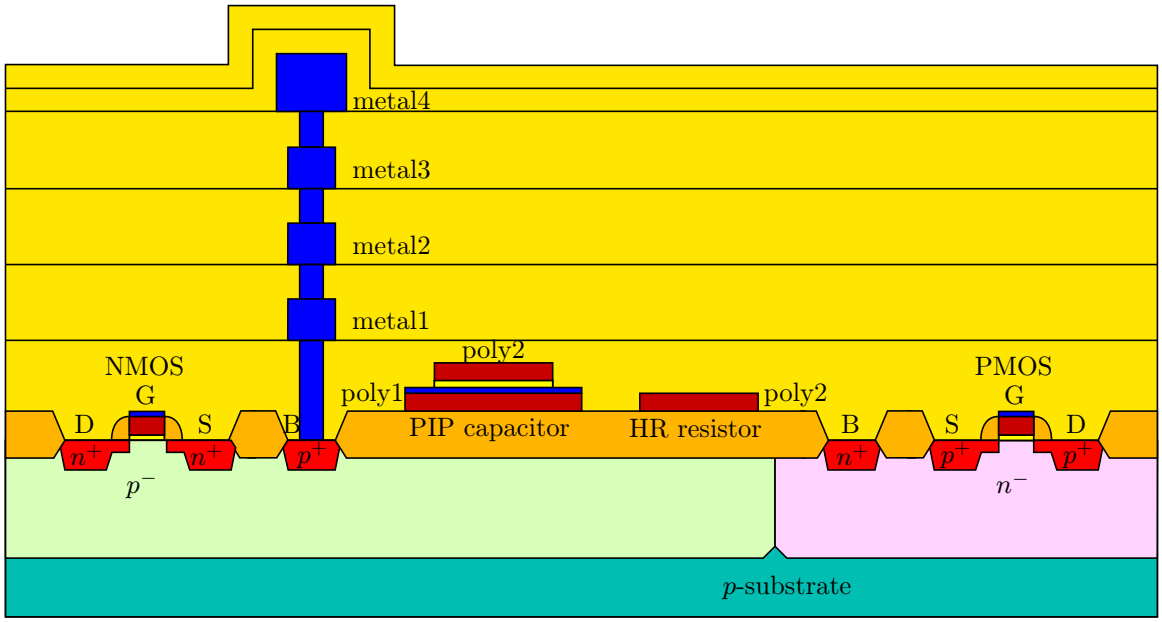

Figure 3.2: AMS H35B4 process (NMOS, PMOS, PIP capacitor, HR resistor).

(regular-V_{th}) transistors are available (i.e., no low threshold voltage transistors are provided).

The two available polysilicon layers are used to lay out polysilicon-insulator-polysilicon (PIP) capacitors. Since the resistivity of polysilicon is approximately 100 times higher than the resistivity of metal, the equivalent series resistance (ESR) of these PIP capacitors is also high. Their characteristics are therefore far away from ideal capacitors. This results in reduced performances in switched capacitors circuits.

As shown in Figure 3.3, the NMOS and PMOS transistors are available in isolated wells. These isolated transistors provide reduced substrate coupling [55]. When they are switching, the substrate voltage swing is lower compared to nonisolated transistors and therefore they provide better electromagnetical interferences (EMI) shielding and better noise performances when used in sensitive analog sensor circuits.

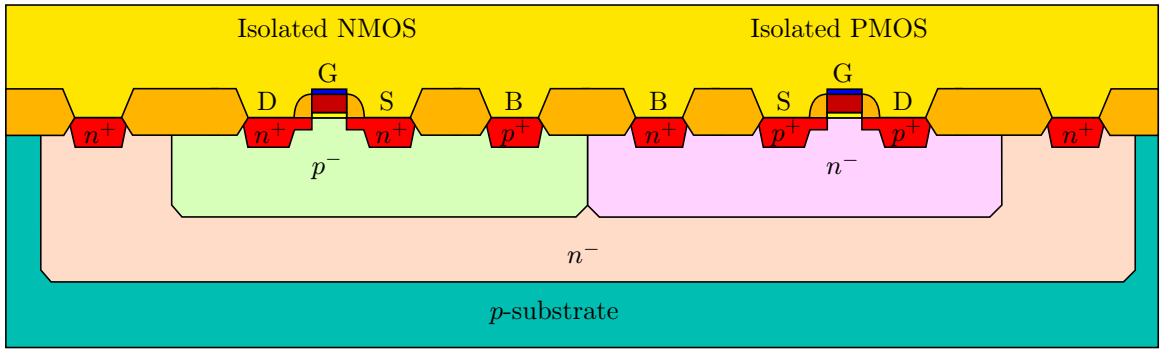

Figure 3.3: AMS H35B4 process (isolated NMOS and PMOS transistors).

The high voltage option provides additional transistors which are shown in Figure 3.4 and which were developed for performing at voltages up to 50 V. However, these high voltage transistors need a long channel length L to achieve the high break-

down voltage, which results in higher turn on channel resistance $R_{\mathrm{DS(on)}}$ and higher gate charge Q_{G}. The consequence is a higher power dissipation through significantly more conduction and switching losses, in the case these high voltage transistors are used in the power H-bridge of the DC-DC converter.

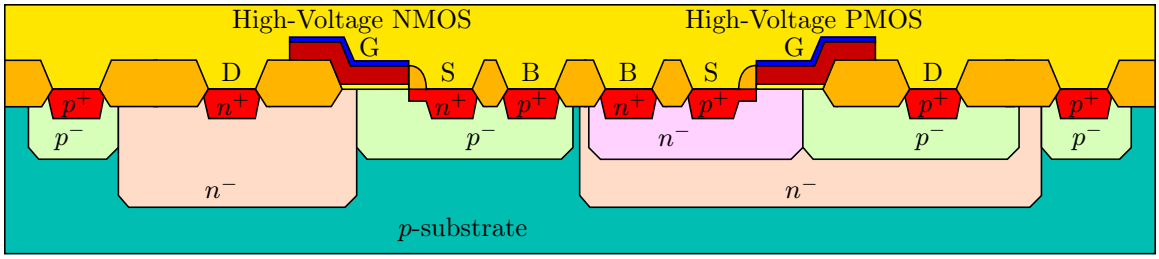

Figure 3.4: AMS H35B4 process (HV NMOS50 and PMOS50 transistors).

Additionally, high voltage transistors occupy much more silicon area. However, to test the concept of the novel bidirectional DC-DC converter, high breakdown voltages are not mandatory. The efficiency is the most important point. Due to all these reasons and according to the specifications of the bidirectional DC-DC converter defined in Section 3.1, the provided high voltage transistors were not of interest for designing the DC-DC converter's prototypes.

As the H35 technology was released in early 2004, it was a newly available CMOS process by AMS. Some data sets like the voltage and temperature dependencies of the available devices were incomplete in the process documents, which made it difficult to design a well defined CMOS temperature compensated voltage reference. The technology was not mature yet and the models were inaccurate. Some simulations were performed in the Cadence Spectre simulator environment with the 3.3 V transistors from AMS to estimate their conduction losses in a power H-bridge capable of supplying roughly 2000 mA of continuous current. The simulations were actualized in early 2006 by using the Hit-Kit (HK) 3.71 and the results are shown in Figure 3.9.

3.2.1.2 Description of the UMC L180 Technology

The UMC L180 is a 0.18 µm mixed-signal/RF[4] CMOS technology. It is a so-called 1P6M process, which provides one polysilicon layer and six metal layers to the layout designer. A thick top metal layer is available by using the sixth metal layer. Additionally, to offer high current densities, this thick top metal layer permits the realization of inductors with a high quality factor (high-Q) for RF applications. The core technology is based on 1.8 V transistors with a minimum channel length L of 180 nm. Several 3.3 V transistors with a minimum channel length of 340 nm are also available, for example for the I/O circuits. By using the Europractice design libraries, no high voltage option is available in this technology. However, a high voltage module is provided by UMC, but it is only available for industrial customers requesting high volume production of wafers.

[4]RF stands for Radio Frequency: UMC provides very well characterized RF transistors, which have a fixed channel length and a fixed channel width, for use in high frequency applications (e.g., wireless data transmissions) up to several GHz.

The UMC process proposes several threshold voltages V_{th} for the 1.8 V and 3.3 V transistors. Additionally to the regular-V_{th} (REG) transistors, low-V_{th} (LV) transistors and zero-V_{th} (ZV) transistors in both 1.8 V and 3.3 V are provided. The low-V_{th} transistors are especially well suited for low power applications and high speed digital circuits. They are also very useful in analog applications which are supplied by low voltage sources (e.g., one cell batteries). The zero-V_{th} transistors are exclusively NMOS transistors. They are used in very specific applications (e.g., design of a current source which consists of one transistor only).

In the UMC technology, *metal-insulator-metal* (MIM) capacitors are available. They provide very low capacitance dependence to voltage and temperature variations. Unlike the PIP capacitors which use polysilicon electrodes, MIM capacitors use metal electrodes and therefore they provide an ESR that is 10 to 100 times lower than that of PIP capacitors. The MIM capacitors are therefore well suited for switched capacitors circuits. An highly power efficient charge pump build up with MIM capacitors is described in Section 5.1.1.3.

With the so-called *triple-well* (T-Well) option illustrated in Figure 3.5, isolated NMOS (1.8 V and 3.3 V) with regular-V_{th} are provided. Unlike the AMS technology, this isolation well is only available for the NMOS transistors. This option is useful for isolating parts of circuitry which generate noise from noise sensitive parts [55]. Additionally, the body effect occurring in NMOS transistors when the source is not connected to ground is eliminated by connecting the bulk of the NMOS directly to its source.

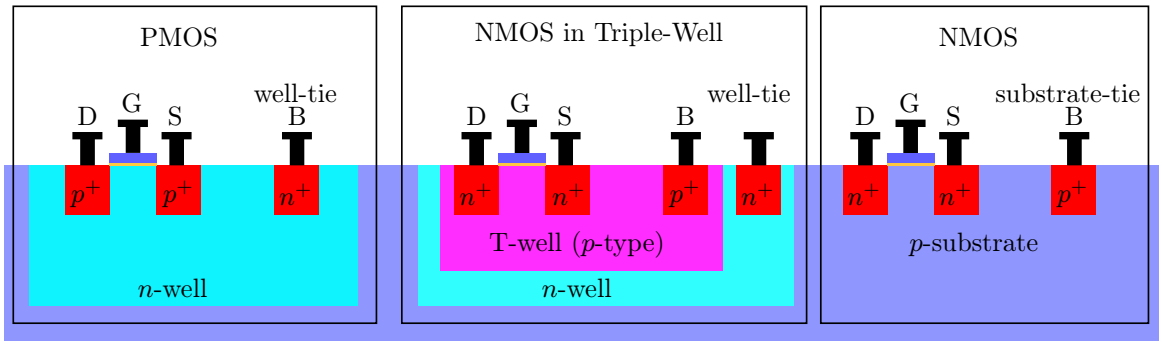

Figure 3.5: Illustration of the triple-well option by UMC.

As the L180 technology was investigated for this work in early 2004, it was already a mature CMOS process commercially available by UMC. The models of all types of transistors were well defined and the process documentation was complete. Some simulations were also performed in the Cadence Spectre simulator environment with the 3.3 V transistors from UMC to show their conduction losses in a power H-bridge capable of supplying roughly 2000 mA of continuous current. The simulations were actualized in early 2006 by using the *foundry design kit* (FDK) version 2.6_P1. These results are presented in Figure 3.9.

3.2.1.3 Performances of the H35 and L180 Technologies

To compare both AMS and UMC technologies, efficiency simulations were performed with the power H-bridge shown in Figure 3.6. The goal of these simulations was

to determine which technology provides the best performance for integrated power electronics.

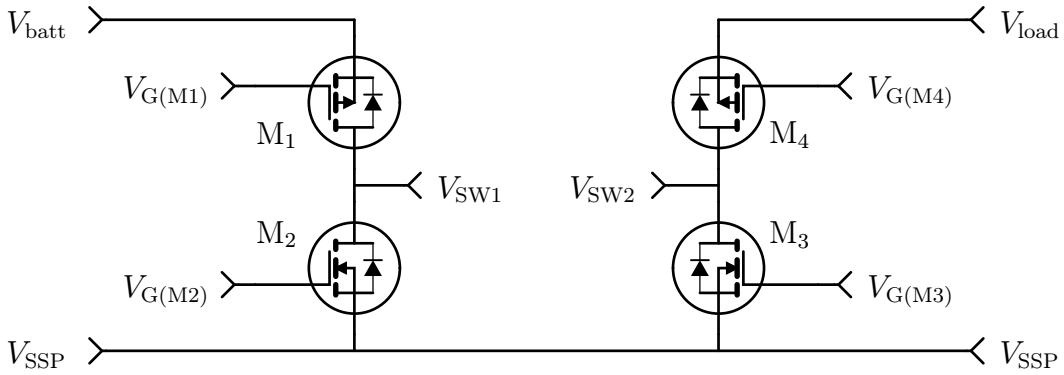

Figure 3.6: H-bridge schematic designed in the Cadence Spectre environment.

The high voltage transistors provided in the AMS H35 technology need a high gate-source V_{GS} voltage to operate in the deep triode region (i.e., like a turned on switch). Battery voltages around 3.6 V are not sufficient for driving them. Therefore, the high voltage transistors would dramatically reduce the efficiency of the H-bridge. As explained in Section 3.1, all state-of-the-art mobile equipment uses a supply voltage around or below 3.3 V. Therefore, it has been decided not to support voltages over 3.6 V. Thus, only the 3.3 V transistors of both manufacturers were compared here. The main characteristic values of both AMS and UMC technologies are synthesized in Table 3.2.

Table 3.2: Characteristics comparison of the AMS and UMC technologies.

Characteristics Name		AMS	UMC
Technology Node		0.35 µm	0.18 µm
Number of Masks		27	36
Polysilicon Layers		2	1
High Resistivity Poly		1200 Ω/□	1000 Ω/□
Number of Metal Layers		4	6
Metal Type		Aluminum	Aluminum
Thick Top Metal Current Density		3.35 mA/µm	4.225 mA/µm
Capacitor Types		MOS, PIP	MOS, MIM
Gate Oxide Capacitance		4.54 fF/µm^2	4.933 fF/µm^2
Threshold Voltages of 3.3 V Transistors	NMOS (REG ; LV)	+0.59 V ; —	+0.65 V ;+0.31 V
	PMOS (REG ; LV)	−0.72 V ; —	−0.70 V ;−0.42 V
Saturation Current of 3.3 V Transistors	NMOS (REG)	+540 µA/µm	+590 µA/µm
	PMOS (REG)	−240 µA/µm	−260 µA/µm

The H-bridge was simulated with the Cadence Spectre software combined with the corresponding design kit of the foundry houses. Figure 3.6 shows the schematic of the H-bridge in the Cadence Spectre environment. Two NMOS transistors were

used for the low-side switches and two PMOS transistors were used for the high-side switches. The transistors M_1, M_3 and M_2, M_4 are turned on and off alternating. The DC-DC converter is therefore operating in the noninverting buck-boost mode (see Section 2.2.3.1 for more details about the operating principle of the noninverting buck-boost converter). The battery is connected to the input side while the load is connected to the output side. The complete schematic used to simulate the H-bridge is shown in Figure 3.7. The values of the parameters used for the simulation of the H-bridge are listed in Table 3.3. The same values were used for both AMS and UMC simulations, allowing direct performance comparison between both technologies.

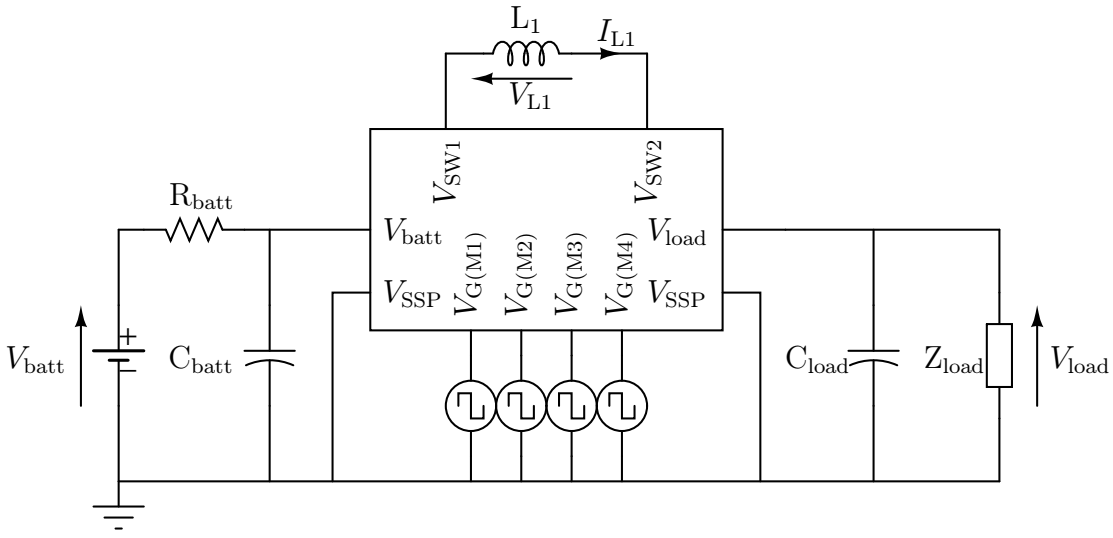

Figure 3.7: Complete H-bridge simulation configuration in Cadence Spectre.

Table 3.3: Parameter values used in the H-bridge simulations.

Parameter Description	Name	Value
Duty Cycle	D	90%
Transfer Function (Buck-Boost)	M	$D/(1-D)$
Cycle Period	T	1 µs
Transistor Fingers Width	W_f	100 µm
Number of Fingers in NMOS	N_n	1100
Number of Fingers in PMOS	N_p	3500
Load Resistor Resistance	R_1	1 Ω
Filter Capacitor Capacity	C_1	220 µF
Power Inductor Inductance	L_sw	10 µH
Input Battery Voltage (worst case)	V_batt	1.8 V

The Cadence Spectre schematic used to compare the drain current I_D versus the applied gate-source voltage V_GS of both the AMS and the UMC transistors, is shown in Figure 3.8. Only the DC behavior was simulated with this schematic. The total width of the simulated NMOS is 110000 µm (i.e., 1100 fingers, each with a width W_f of

100 µm) while the total width of the PMOS is 350000 µm (i.e., 3500 fingers, each with a width W_f of 100 µm). Both AMS and UMC transistors have been simulated with the same width. The UMC transistors were sized so that they can provide 2000 mA of continuous current at a chip temperature of 80°C with a drain-source voltage drop V_{DS} of 50 mV.

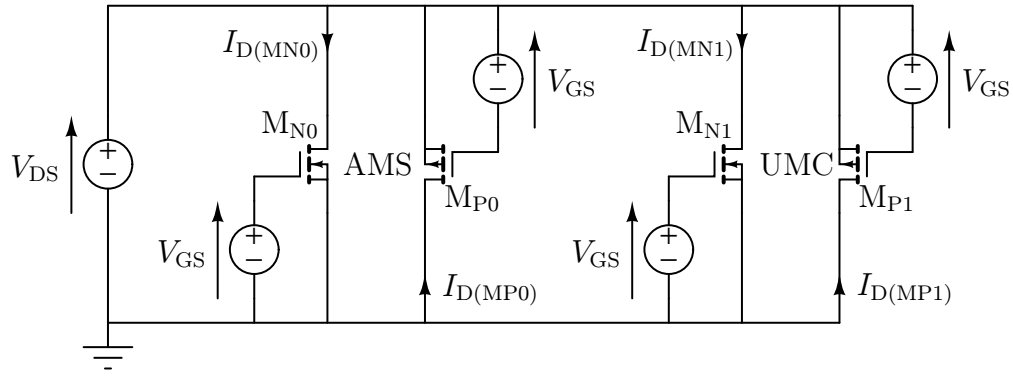

Figure 3.8: Cadence schematic for comparing the drain current I_D of both AMS and UMC 3.3 V transistors driven by the same gate-source voltage V_{GS}.

Figure 3.9 shows both AMS and UMC transistor drain currents I_D (NMOS and PMOS) versus the gate-source voltage V_{GS} at a fixed V_{DS} of 50 mV. The V_{th} values given in the design documents from AMS are slightly lower than those given in the design documents from UMC. However, the simulation results show that both AMS and UMC 3.3 V transistors have nearly the same threshold voltage V_{th}. However, the UMC transistors carry more current than the AMS ones. They also show a lower channel resistance $R_{DS(on)}$ than the AMS transistors. The difference in the minimum gate length L (AMS: $L = 350$ nm; UMC: $L = 340$ nm) contributes to this phenomenon.

Table 3.4 lists the electrical characteristics of the transistors from both foundries at two different V_{GS} levels when the transistors are switching in the H-bridge (see Figure 3.7).

Table 3.4: Transistor characteristics comparison.

Foundry	MOSFET	W	L	V_{GS}	I_D	$R_{DS(on)}$	$I_{G(rms)}$ [a]
AMS	NMOS	110000 µm	350 nm	1.8 V	1.7 A	29 mΩ	1.4 mA
UMC	NMOS	110000 µm	340 nm	1.8 V	2.5 A	20 mΩ	1.7 mA
AMS	PMOS	350000 µm	350 nm	1.8 V	1.5 A	34 mΩ	3.9 mA
UMC	PMOS	350000 µm	340 nm	1.8 V	2.4 A	21 mΩ	4.9 mA
AMS	NMOS	110000 µm	350 nm	3.3 V	2.4 A	20 mΩ	2.7 mA
UMC	NMOS	110000 µm	340 nm	3.3 V	3.8 A	13 mΩ	3.4 mA
AMS	PMOS	350000 µm	350 nm	3.3 V	2.3 A	22 mΩ	7.9 mA
UMC	PMOS	350000 µm	340 nm	3.3 V	4.3 A	12 mΩ	9.8 mA

[a] RMS gate current when switching at 1 MHz

When comparing the drain current I_D to the RMS gate current, the UMC transistors provide a higher efficiency. They have a slightly smaller channel length L and

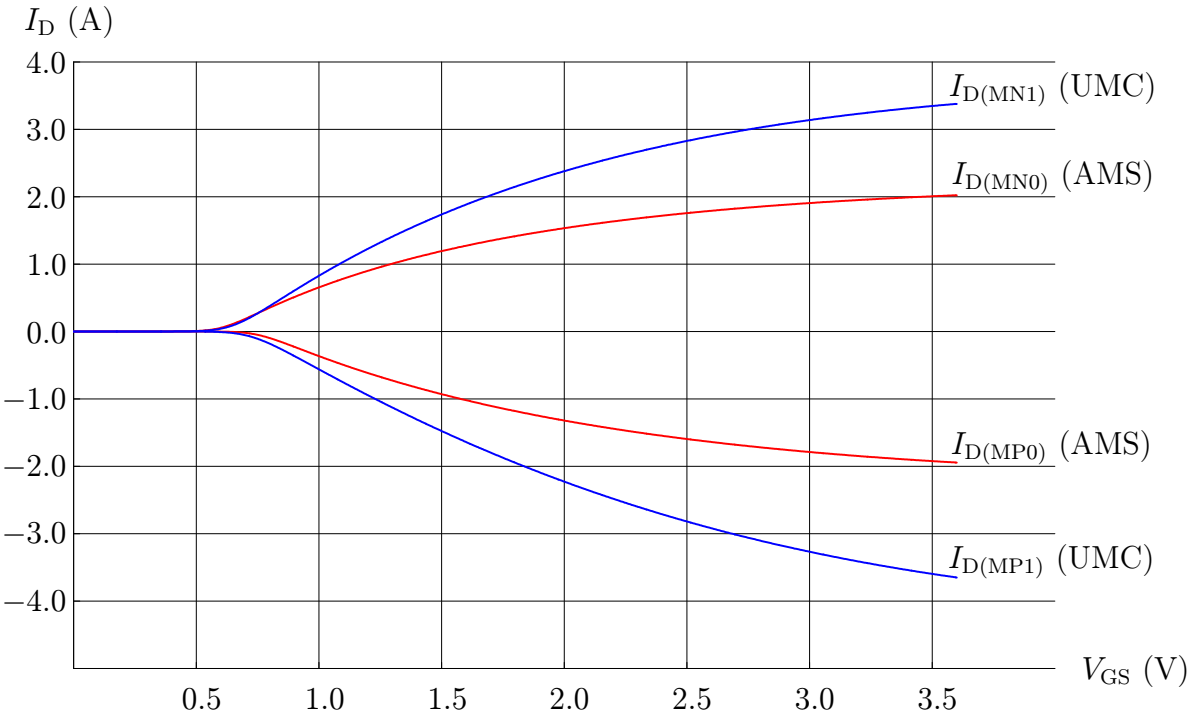

Figure 3.9: AMS and UMC 3.3 V transistor comparison (I_D versus V_{GS}) with a drain-source voltage V_{DS} fixed to 50 mV.

therefore a lower $R_{DS(on)}$. Thus, they can conduct higher currents. Finally, they have, proportionally to their drain current I_D, a lower gate capacitance. Because of these facts, the UMC technology was chosen for designing the power H-bridge. Furthermore, the continuity of the 0.18 µm technology is ensured, as illustrated in Figure 3.10. Especially the mixed-signal 0.18 µm processes will be further available in the future, because some analog designs cannot be scaled, even if the process scales down (e.g., due to punch-through, the gate length L cannot be significantly scaled down if the breakdown voltage for V_{DS} have to remain the same).

3.2.2 Selection of the Type of Power Transistors

The different types of transistors available in the UMC L180 CMOS technology are listed in Table 3.5. To design the H-bridge, two different transistor types were analyzed. One was the 3.3 V regular-V_{th} transistor type (REG33), which is a transistor with a regular threshold voltage V_{th} of typically 0.65 V and a minimum channel length L of 340 nm. The other was the 3.3 V low-V_{th} transistor type (LV33), which has a low threshold voltage V_{th} of typically 0.35 V and a minimum channel length L of 500 nm.

3.2.2.1 Drain Current versus Drain-Source Voltage

Since the transistors are used as switches in the H-bridge, when they are turned on, they operate in the linear region. To determine which transistor type provides the best overall efficiency, the drain current I_D was analyzed in forward conduction mode and plotted versus the drain-source voltage drop V_{DS} with a gate-source voltage V_{GS} of 1.8 V. To get the curves shown in Figure 3.11, three NMOS transistors (i.e., an

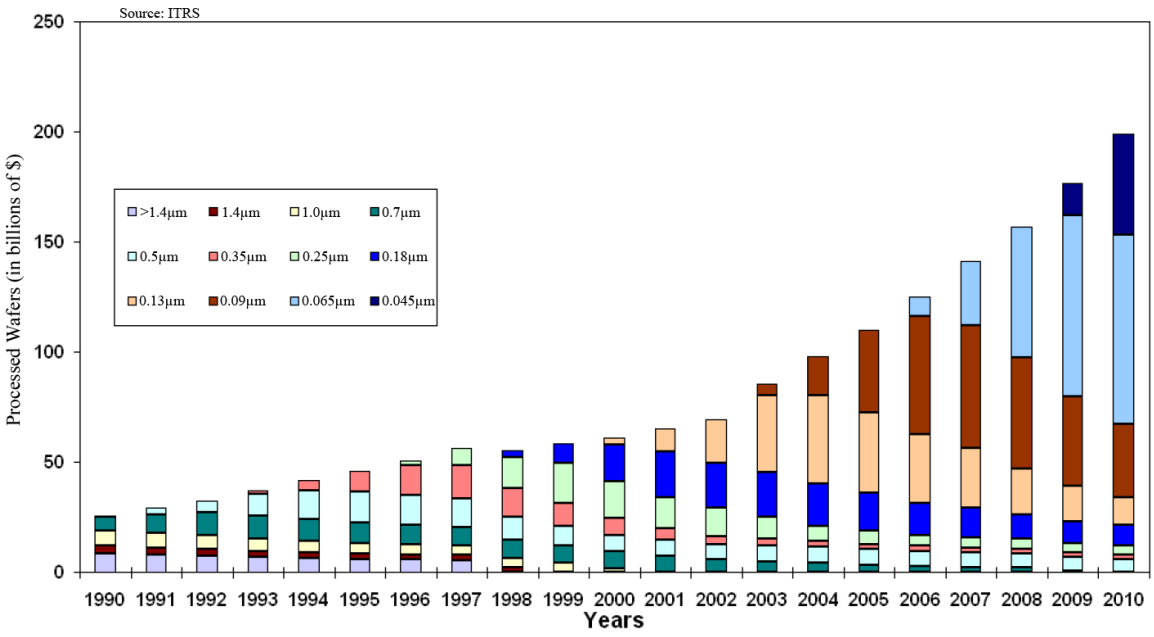

Figure 3.10: Continuity of the CMOS technologies.

Table 3.5: Threshold voltage of the UMC L180 mixed-signal transistors.

Transistors	Type	$V_{\mathrm{th(min)}}$	$V_{\mathrm{th(typ)}}$	$V_{\mathrm{th(max)}}$	Triple-Well Option
1.8 V NMOS	reg-V_{th}	+0.44 V	+0.51 V	+0.58 V	Yes
1.8 V NMOS	low-V_{th}	+0.10 V	+0.22 V	+0.34 V	No
1.8 V NMOS	zero-V_{th}	−0.14 V	−0.02 V	+0.10 V	No
1.8 V PMOS	reg-V_{th}	−0.43 V	−0.50 V	−0.57 V	No
1.8 V PMOS	low-V_{th}	−0.10 V	−0.22 V	−0.34 V	No
3.3 V NMOS	reg-V_{th}	+0.55 V	+0.65 V	+0.75 V	Yes
3.3 V NMOS	low-V_{th}	+0.21 V	+0.31 V	+0.41 V	No
3.3 V NMOS	zero-V_{th}	−0.10 V	+0.02 V	+0.14 V	No
3.3 V PMOS	reg-V_{th}	−0.60 V	−0.70 V	−0.80 V	No
3.3 V PMOS	low-V_{th}	−0.32 V	−0.42 V	−0.52 V	No

LV33 with a channel length of 500 nm, a REG33 with a channel length of 340 nm, and a REG33 with a channel length of 500 nm) with the same width W of 110000 µm were connected in parallel to an ideal voltage source generating the drain-source voltage V_{DS}, as it was illustrated previously in Figure 3.8.

In Figure 3.11, it is shown that the REG33 transistor with a channel length L of 500 nm has a lower drain current I_{D} than the LV33 transistor, when both are driven in the deep triode region at a gate-source voltage V_{GS} of 1.8 V. Since the LV33 transistor has a lower threshold voltage V_{th}, this was expected when the channel length L of both LV33 and REG33 transistors are equal. However, the minimum channel length L of the REG33 transistor is 340 nm where the minimum channel length L of the LV33 transistor is 500 nm. At a gate-source voltage V_{GS} of 1.8 V, the REG33 transistor with the minimum channel length conducts more current than the LV33 transistor. This fact is analyzed hereafter.

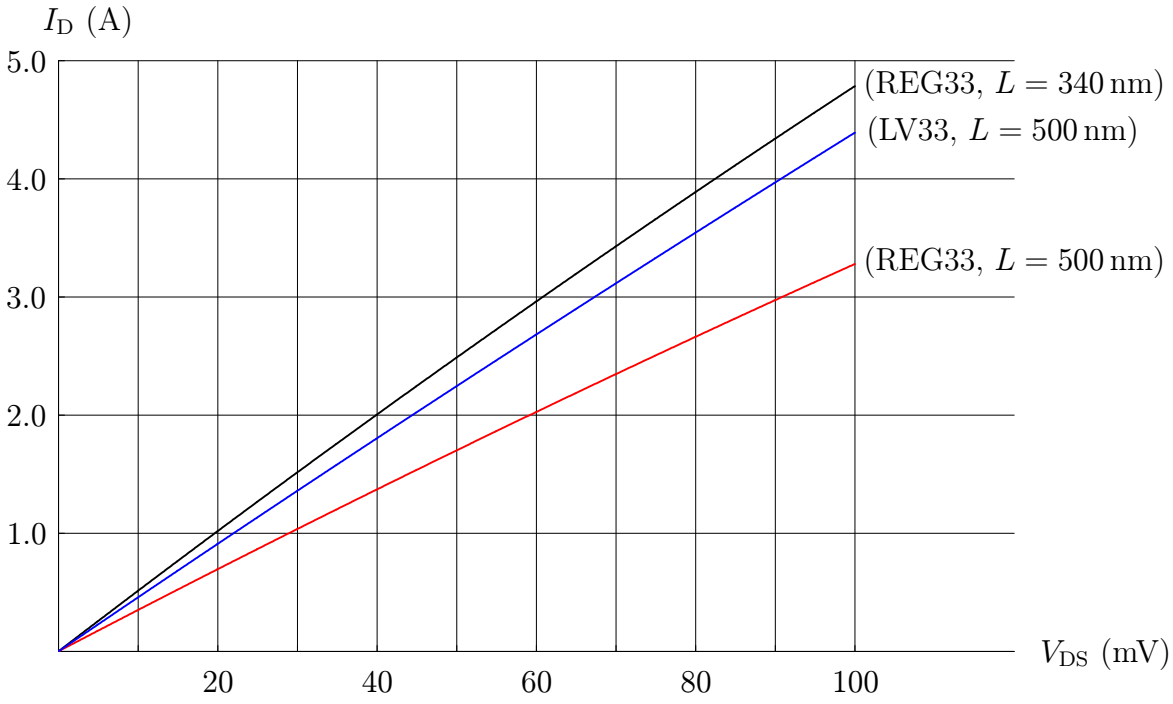

Figure 3.11: Drain current I_D versus drain-source voltage V_{DS} for the UMC 3.3 V NMOS low threshold and regular threshold voltage transistors driven by a gate-source voltage V_{GS} of 1.8 V.

3.2.2.2 Drain Current versus Gate-Source Voltage

The drain current I_D of a MOSFET operating in the linear region depends on the carrier mobility μ in the MOSFET channel, the gate oxide capacitance per unit area C_{ox}, the channel width W, the channel length L, the gate-source voltage V_{GS}, the threshold voltage V_{th}, and the drain-source voltage V_{DS}. It is given by:

$$I_D = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot \left((V_{GS} - V_{th}) \cdot V_{DS} - \frac{1}{2} \cdot V_{DS}^2 \right) \tag{3.5}$$

In this application, the power transistors of the H-bridge are sized the way that, when they are turned on, they have a drain-source voltage V_{DS} around 50 mV at a gate-source voltage V_{GS} of 1.8 V. These values were chosen for optimizing the conduction losses occurring in the power transistors of the H-bridge at the nominal battery voltage of 2.3 V. The worst case occurs when the battery delivers its end-of-life voltage (i.e., discharged battery). Then, the gate-source voltage V_{GS} used for driving the power transistors in the H-bridge is as low as 1.8 V. When the transistor operates in the deep triode region, the following condition becomes true:

$$\frac{1}{2} \cdot V_{DS} \ll (V_{GS} - V_{th}) \tag{3.6}$$

In the deep triode region, the expression in Equation (3.5) can be approximated by:

$$I_D \approx \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{th}) \cdot V_{DS} \tag{3.7}$$

The channel resistance $R_{\mathrm{DS(on)}}$ of a MOSFET operating in the deep triode region is:

$$R_{\mathrm{DS(on)}} = \frac{V_{\mathrm{DS}}}{I_{\mathrm{D}}} = \frac{1}{\mu \cdot C_{\mathrm{ox}} \cdot \frac{W}{L} \cdot (V_{\mathrm{GS}} - V_{\mathrm{th}})} \tag{3.8}$$

To decrease the value of the threshold voltage V_{th}, the channel doping concentration was decreased in the LV33 transistors, compared to the REG33 transistors. If the threshold voltage V_{th} decreases, and if all other terms remain the same, the $R_{\mathrm{DS(on)}}$ decreases, too (see Equation (3.8)). However, it has to be considered that the minimum channel width of both LV33 and REG33 transistors differs. The value of the carriers mobility μ provided by UMC is affected by the doping difference. The channel resistance $R_{\mathrm{DS(on)}}$ is calculated by using the values of the model parameters shown in Table 3.6.

Table 3.6: UMC NMOS model parameters.

NMOS Type	V_{th} (V)	μ ($\mathrm{m^2/V \cdot s}$)	C_{ox} ($\mathrm{pF/\mu m^2}$)	W (µm)	L (µm)
LV33	0.314	$4.07 \cdot 10^{-2}$	$500 \cdot 10^{-5}$	110000	0.500
REG33	0.592	$3.41 \cdot 10^{-2}$	$500 \cdot 10^{-5}$	110000	0.340

When using the values given in Table 3.6, and solving Equation (3.8) to get the gate-source voltage V_{GS} at which both LV33 (with a channel length of 500 nm) and REG33 (with a channel length of 340 nm) channel resistances $R_{\mathrm{DS(on)}}$ are equal, the value 1.79 V is obtained for V_{GS}. The short channel effects and other deep sub-micron influences are not taken into consideration for this simple estimation. However, these complex effects are accurately modeled and used in the Cadence Spectre simulator. Figure 3.12, shows the drain current I_{D} versus the gate-source voltage V_{GS}. An intersection point exists at which both the LV33 (with a channel length of 500 nm) and the REG33 (with a channel length of 340 nm) transistor types have the same channel resistance $R_{\mathrm{DS(on)}}$ when a drain-source voltage V_{DS} of 50 mV is applied to them. The simulation results indicate that below a gate-source voltage V_{GS} of 1.39 V, the LV33 transistor provides the lowest $R_{\mathrm{DS(on)}}$, while above this voltage value, the REG33 transistor provides the lowest $R_{\mathrm{DS(on)}}$. The same considerations apply for PMOS transistors. Since the lowest drive voltage applied to the gate will be 1.8 V in the targeted mobile application (end-of-life voltage of the battery), the REG33 transistor provides the lowest $R_{\mathrm{DS(on)}}$.

To take the final decision for choosing between the LV33 and the REG33 transistor types, their gate charge losses were analyzed. Since the minimum gate length L is 500 nm for the LV33 transistor, it uses a larger gate polysilicon area, and therefore it has a fairly higher gate capacity, compared to the REG33 transistor which has a 340 nm minimal gate length. The short channel effect decreases the gate-source voltage V_{GS} that equals the $R_{\mathrm{DS(on)}}$ value of both types of transistors (see simulation results in Figure 3.12). Thus, to get the same $R_{\mathrm{DS(on)}}$ than the REG33 transistors at a gate-source voltage V_{GS} of 1.8 V, the LV33 transistors must be designed roughly 30% wider. This is shown in Table 3.7. The consequence is more wasted dynamic power through the charging and discharging of the gate capacity in the LV33 transistors compared to the REG33 transistors, as reported in Table 3.7.

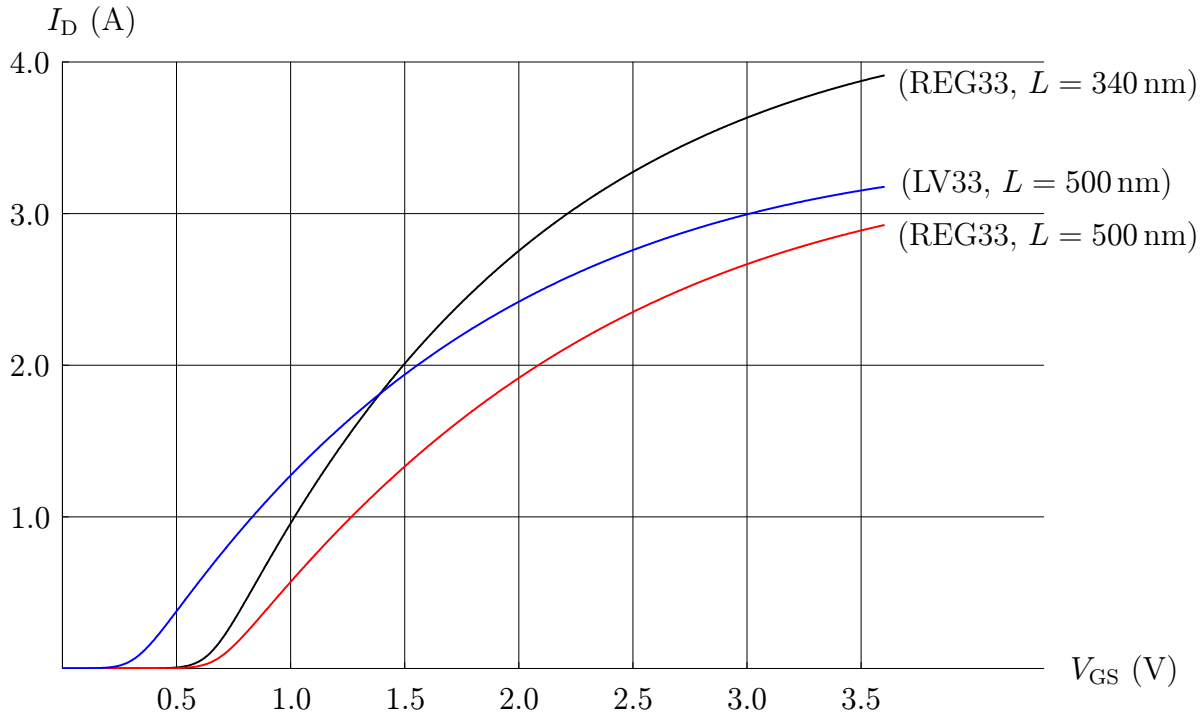

Figure 3.12: Drain current I_D versus gate-source voltage V_{GS} for the UMC 3.3 V NMOS LV33 and REG33 transistors at a drain-source voltage V_{DS} of 50 mV.

Table 3.7: Regular and low threshold transistors comparison.

MOSFET	L	W [a]	Silicon Area	Gate Losses [b]	Leakage [c]
N_REG33	340 nm	110000 µm	0.15 mm^2	2.2 mW	13.08 nA
N_LV33	500 nm	125000 µm	0.19 mm^2	3.2 mW	61.1 µA [d]
P_REG33	340 nm	350000 µm	0.46 mm^2	5.9 mW	13.54 nA
P_LV33	500 nm	410000 µm	0.61 mm^2	8.8 mW	386.1 nA

[a] The transistors were sized in such a way that I_D=2 A at V_{GS}=1.8 V, V_{DS}=50 mV, $T = 100$°C
[b] RMS gate current when V_{GS} is switched between 0 and 1.8 V at $f_{sw} = 1$ MHz and $T = 100$°C
[c] Simulated at $T = 27$°C with V_{DS}=1.8 V
[d] Extremely high leakage current value obtained through simulations (reason undetermined)

Because the $R_{DS(on)}$ at full V_{GS}, the area consumption and the gate capacity are lower with the REG33 transistors, it has been decided to use the REG33 NMOS and PMOS to design the power H-bridge of the bidirectional DC-DC converter. The REG33 transistors provide the best overall performances in the targeted applications.

3.3 Packaging and Bonding Considerations

For testing purposes (e.g., easy die access), the prototypes have been packaged in a ceramic package. The packaging choice was a very important point in realizing the bidirectional DC-DC converter prototypes, because of the high continuous currents carried by the power pins (i.e., up to 2000 mA) [56]. The ideal choice would have been a flip-chip package type, which is well suited for currents up to 20 A in compact silicon

designs. However, this packaging technology is only proposed at wafer level. This means that the complete wafer must be provided for flip-chip assembling. However, the prototypes were realized through multi-project-wafer runs (Europractice), which provides only sawn silicon dies (i.e., no complete wafers). Therefore, an assembly solution for the prototypes with the more usual wire-bonding had to be chosen.

3.3.1 Ceramic Packages for Prototyping

There are several criteria which must be considered when choosing the package for prototyping. Since the silicon die of the bidirectional DC-DC converter is rectangular, with its pads disposed along the four sides, the most adapted package is a so-called *quad* package, which offers pins on its four sides. For bonding and testing flexibility, a ceramic package is a better choice for prototyping than a plastic package, because it offers access to the silicon die (in a plastic package, the die is sealed in the plastic and it cannot be accessed without breaking the plastic package). Additionally, the thermal resistance of ceramic material is lower than that of plastic. This results in better thermal dissipation, which is very important for a power converter. The minimum pin number is defined by the number of pads placed on the four sides of the layout of the prototype. A quad package of 60 pins is a minimum for the IPC.

The thermal performance of the package is important since the targeted application is power conversion. The thermal resistance is a characteristic value for the thermal performance of a package. It is a measure of the package's heat dissipation capability from the silicon die's active surface (i.e., junction) to a given reference point (e.g., ambient air, printed circuit board). In the manufacturers IC package datasheets, the most usually documented thermal resistance is the junction-to-air thermal resistance Θ_{JA} (in K/W). Often, the junction-to-case thermal resistance Θ_{JC} is also given. It is useful for calculating the size of the heatsink when more power than the maximum admissible power $P_{\mathrm{pack(max)}}$ must be dissipated by the considered package.

The junction-to-air thermal resistance Θ_{JA} expresses the ability of the package to dissipate the heat from the surface of the silicon die to the ambient air. It is used when the packaged IC performs without a heat sink and is determined by:

$$\Theta_{\mathrm{JA}} = \frac{T_{\mathrm{J}} - T_{\mathrm{A}}}{P_{\mathrm{pack(max)}}} \tag{3.9}$$

where T_{J} is the junction temperature in °C (generally 150°C for standard CMOS processes), T_{A} is the ambient air temperature in °C, and $P_{\mathrm{pack(max)}}$ is the maximum power that can be dissipated by the package without a heatsink. Table 3.8 shows the thermal characteristics of the *ceramic leadless chip carrier* (CLCC) and the *ceramic J-leaded chip carrier* (JLCC) packages that were considered for manufacturing the prototypes of the IPC. The very popular *plastic leaded chip carrier* (PLCC) is shown as reference. Note that the presented data can vary, because of the spread values given by the different package manufacturers.

The CLCC package is shown in Figure 3.13. It is compatible with the standard PLCC sockets in through holes and surface mounted versions, which are simple to acquire. This allows easy testing and rapid characterization of the prototypes. The standard cavity opening of 300 mils in the package is much bigger than the minimum needed cavity opening of 160 mils (4000 µm) required by the design size of the prototypes. This has a negative consequence on the length of the bond wires. The minimum

Table 3.8: Packages thermal characteristics.

Package	Cavity (square)	Θ_{JA}	Θ_{JC}[a]	$P_{pack(max)}$
PLCC-68 (plastic)	0.300 in	46.1 K/W	14.6 K/W	2.71 W
CLCC-68 (ceramic)	0.320 in	15.0 K/W	2.6 K/W	8.33 W
JLCC-68 (ceramic)	0.265 in	17.0 K/W	3.0 K/W	7.35 W

[a]The related chip area was not specified by the manufacturer

measured bonding wire length (i.e., flight line) is 3.5 mm, if a cavity of 300 mils is used. The maximum length attained in the corners is then around 4.5 mm. The bonding wires are analyzed in detail in Section 3.3.3.

Figure 3.13: Ceramic Leadless Chip Carrier (CLCC) with 28 pins.

The JLCC package is identical to the CLCC package, but with additional J-leads. The thermal and electrical specifications are nearly the same. Figure 3.14 shows how the JLCC package looks like. There are mainly two advantages by using a JLCC package in place of a CLCC package. The first advantage is that the JLCC package is available with a smaller cavity size than the CLCC package, which results in shorter bonding wires and therefore lower conduction losses in high current paths. The second advantage is that thanks to the J-leads, more mechanical flexibility is left between the package and the printed circuit board for the thermal cycles. The J-leads are more easily deformable compared to no-leads packages, which results in higher reliability.

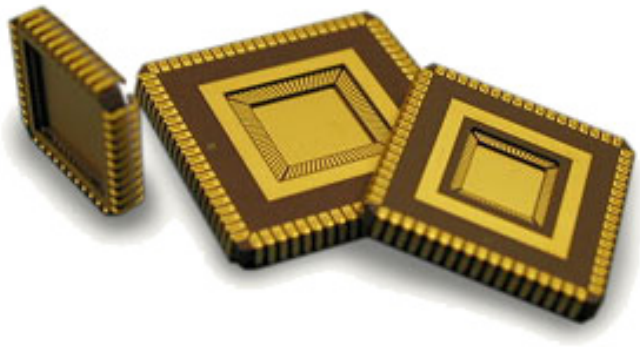

Figure 3.14: Ceramic J-Leaded Chip Carrier (JLCC).

Like the CLCC package, the JLCC package is compatible with the standard PLCC sockets. Therefore, both prototypes of the IPC were assembled in a JLCC package. The printed circuit test board used for characterizing the prototypes was equipped with a PLCC socket, thus providing rapid exchange of the device under test.

3.3.2 Plastic Packages for Mass Production

A mass production packaging solution was investigated for the IPC. One of the most cutting-edge packaging technologies to recently emerge in the electronics marketplace is the *quad flat no-leads* (QFN) package [57] depicted in Figure 3.15.

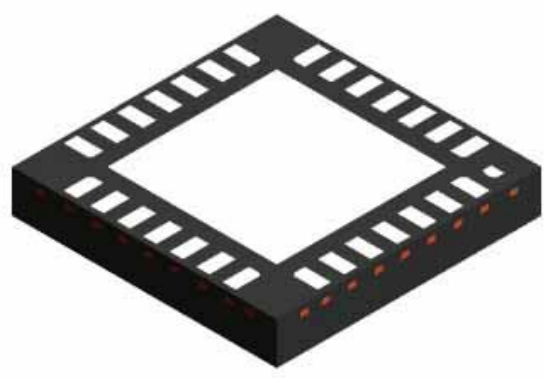

Figure 3.15: Quad Flat No-leads package with 28 pins.

The QFN package provides small size, cost effectiveness and good production yields. Additionally, it provides as good electrical performances as array packages, but it does not require *ball grid array* (BGA) substrates nor expensive ball tooling. It is best suited for low lead count integrated circuits.

The QFN package possesses several mechanical advantages for high speed and high power circuits, including improved heat dissipation [58]. Because it does not have gull wing leads acting as antennas and therefore creating noise in high frequency applications, the QFN package has superior electrical performance when it is compared to the traditional leaded packages like the PLCC. In addition, it provides excellent thermal performances through the exposed leadframe pad, which enables a direct thermal path for dissipating the heat from the package. This thermal enhancing feature performs best when the package leadframe pad is soldered to the printed circuit board. Then, the exposed die flag offers a heat conduit for thermal relief that enables very high power dissipation. In 2004, a high power version of the QFN package (HQFN) was presented in the literature [58].

Power converters in QFN packages are planned to be used in cell phones, and take advantage of the QFN soldered die flag to dissipate considerable thermal energy with a minimal inductive coupling to the surrounding circuitry. This thermal pad enhances the performances of further coming monolithic integrated DC-DC converters, like the LTM4600 micro-module shown in Figure 3.16, which was brought on the market in the year 2006 by Linear Technology [59].

Both wire-bond and flip-chip versions of the QFN packages exist [57]. The electrical properties of the flip-chip version considerably surpasses those of the wire-bonded version. It provides the needed electrical performances to the new ICs demanding high currents, low voltages and high operating frequencies. The QFN package in its

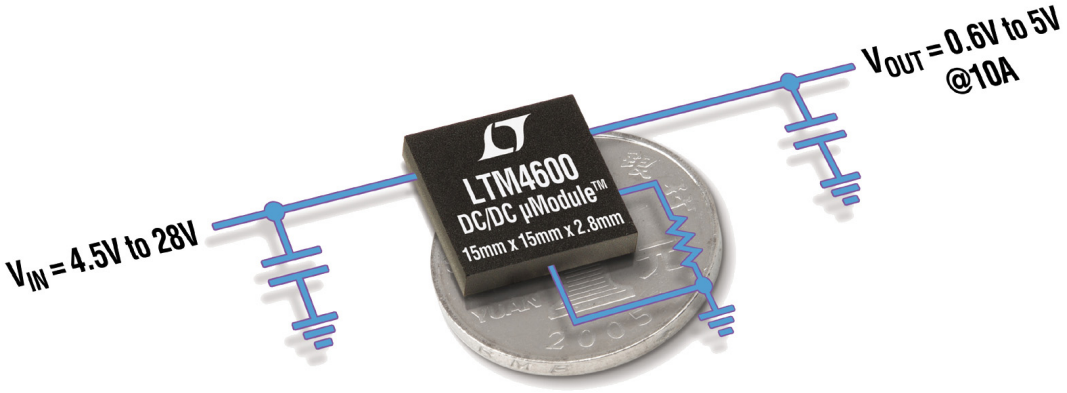

Figure 3.16: DC-DC converter micro-module from Linear Technology [59].

flip-chip version is the ideal choice for a mass production of an integrated bidirectional power DC-DC converter, since it combines low costs and high reliability with high electrical and thermal performances.

3.3.3 Bonding Wires and Bonding Pads

The length of the bond wires in high current or high speed designs is always a critical point. Long bond wires have a higher inductance and a higher resistance compared to short bond wires. The inductance of the bonding wires is directly proportional to their length. This can lead to issues when high speed digital signals are used, or when the high currents in the power paths are switched (see Section 6.2.4). Concerning the resistance of the bond wires, some issues had to be solved. A high bond wire resistance leads to high conduction losses when high currents are carried. Thus, a significant IR-drop occurs across the bond wire. This reduces the efficiency of the DC-DC converter. If the current flowing through the bond wire approaches the fusing current, the metal reaches its melting point and the bond wire fuses. An additional destructive effect for bond wires in high current applications is the electromigration, which occurs principally at the contact ends. However, the dependence of the bond wire length of the electromigration process is negligible. Electromigration is accentuated by unidirectional pulsed high currents (i.e., high electron flow in the metal).

To maximize the current carried by the bond wires, their length must be kept to minimum, so that the IR-drop is also minimum. Like the electrical characteristics of ceramic packages, the electrical characteristics of bond wires (e.g., fusing current) are extremely difficult to get, since they depend on the environment of the bond wire (e.g., air, resin, plastic, solvent). Table 3.9 shows the electrical characteristics of gold bond wires, while Table 3.10 shows those of aluminum bond wires.

The determination of the bond wire thickness is done by analyzing the maximum current that flows through it. The size of the bond pads on the silicon die must also be considered. The most usual bonding method is the ball-wedge bonding. This means that ball bonding is done at the die side and wedge bonding at the leadframe side. Ball bonding is often used with gold wires in low current applications, where high pin counts are needed. Table 3.11 summarizes the needed bond pad sizes when ball bonding is used. In some cases (e.g., for the power supply connections), double or triple bonds are used in parallel to one big bond pad to carry more current.

Table 3.9: Characteristics of gold bond wires (99.99% purity, 10 mm long, 20°C).

Wire Diameter	Wire Cross-Section	Wire Resistivity	Fusing Current[a]
18 µm	254 µm^2	88 mΩ/mm	0.4 A to 0.5 A
20 µm	314 µm^2	71 mΩ/mm	0.5 A to 0.6 A
23 µm	415 µm^2	54 mΩ/mm	0.6 A to 0.7 A
25 µm	491 µm^2	46 mΩ/mm	0.7 A to 0.8 A
28 µm	616 µm^2	36 mΩ/mm	0.8 A to 0.9 A
30 µm	707 µm^2	32 mΩ/mm	0.9 A to 1.0 A
33 µm	855 µm^2	27 mΩ/mm	1.1 A to 1.2 A
38 µm	1134 µm^2	21 mΩ/mm	1.3 A to 1.4 A
50 µm	1963 µm^2	12 mΩ/mm	2.0 A to 2.1 A

[a]Source: Advanced Semiconductor Engineering (ASE), Taiwan, `http://www.aseglobal.com`

Table 3.10: Characteristics of aluminum bond wires (99.99% purity, 10 mm long, 20°C).

Wire Diameter	Wire Cross-Section	Wire Resistivity	Fusing Current[a]
25 µm	490 µm^2	52 mΩ/mm	0.2 A to 0.3 A
33 µm	855 µm^2	34 mΩ/mm	0.4 A to 0.5 A
38 µm	1134 µm^2	23 mΩ/mm	0.6 A to 0.7 A
50 µm	1963 µm^2	13 mΩ/mm	1.0 A to 1.2 A
75 µm	4418 µm^2	5.9 mΩ/mm	2.0 A to 2.5 A
100 µm	7854 µm^2	3.3 mΩ/mm	3.5 A to 4.0 A
125 µm	12272 µm^2	2.1 mΩ/mm	5.0 A to 6.0 A
200 µm	31416 µm^2	0.83 mΩ/mm	11.0 A to 12.0 A
250 µm	49087 µm^2	0.53 mΩ/mm	16.0 A to 18.0 A
300 µm	70686 µm^2	0.37 mΩ/mm	21.0 A to 23.0 A
375 µm	110447 µm^2	0.23 mΩ/mm	30.0 A to 35.0 A
500 µm	196350 µm^2	0.13 mΩ/mm	50.0 A to 60.0 A

[a]Source: Signal Processing Group Inc. (SPG), USA, `http://www.signalpro.com`

Table 3.11: Typical bond pad sizes for ball-wedge bonding.

Bond Wire Diameter	Single Pitch	Single Bond	Double Bond	Triple Bond
20-25 µm	094 µm	076 µm×076 µm	076 µm×170 µm	076 µm×264 µm
26-32 µm	114 µm	094 µm×094 µm	094 µm×208 µm	094 µm×322 µm
33 µm	140 µm	102 µm×102 µm	102 µm×241 µm	102 µm×381 µm
38 µm	190 µm	114 µm×114 µm	114 µm×305 µm	114 µm×495 µm
50 µm	254 µm	165 µm×165 µm	165 µm×419 µm	165 µm×673 µm

An alternative bonding type is the wedge-wedge bonding shown in Figure 3.17. Thanks to information from Fraunhofer IZM (Institute for Reliability and Microintegration, Germany), the bond pad sizes have been determined for each bond wire thickness and completed in Table 3.12.

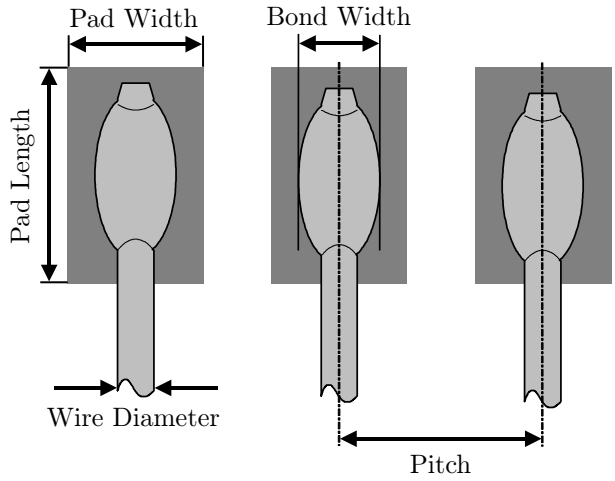

Figure 3.17: Example sketch of wedge-wedge bonding.

For the high current paths in the bidirectional DC-DC converter, two possibilities were considered to optimize the bond wire thickness and the bond pad size on the silicon die. The first bonding solution considered consists of a 75 µm thick aluminum bond wire that is used with the standard wedge bonding. Table 3.12 lists the required bond pad size to have a minimum of 180 µm×200 µm. The second bonding solution considered consists of a 100 µm thick aluminum bond wire that is used with the cutting edge wedge bonding. In this second case, according to Table 3.13, the minimum bond pad size has to be 150 µm×220 µm. Finally, the design size of the power bond pads was defined to be 180 µm×220 µm, so that both bonding solutions can be used at packaging time, depending on the available bonding equipment. However, the bond wire thickness (75 µm versus 100 µm) directly impacts the maximum current that can be carried and therefore the electrical performances of the IPC.

Table 3.12: Bond pad sizes for standard wedge-wedge bonding.

Bond Wire Diameter	Standard Wedge Bonding[a]			
	Pad Width	Pad Length	Pad Pitch	Bond Width
25 µm	100 µm	125 µm	125 µm	45 µm
50 µm	125 µm	150 µm	200 µm	75 µm
75 µm	180 µm	200 µm	250 µm	125 µm
100 µm	200 µm	280 µm	280 µm	130 µm
125 µm	250 µm	300 µm	350 µm	150 µm
150 µm	250 µm	500 µm	400 µm	200 µm
250 µm	400 µm	800 µm	600 µm	320 µm
500 µm	800 µm	1300 µm	1150 µm	650 µm

[a]Source: Fraunhofer IZM (Institute for Reliability and Microintegration), Germany

Table 3.13: Bond pad sizes for cutting-edge wedge-wedge bonding.

Bond Wire Diameter	Cutting-Edge Wedge Bonding[a]			
	Pad Width	Pad Length	Pad Pitch	Bond Width
25 µm	50 µm	75 µm	75 µm	38 µm
50 µm	90 µm	125 µm	140 µm	70 µm
75 µm	120 µm	170 µm	150 µm	112 µm
100 µm	150 µm	220 µm	190 µm	130 µm
125 µm	175 µm	250 µm	250 µm	150 µm
150 µm	230 µm	320 µm	250 µm	180 µm
250 µm	350 µm	500 µm	350 µm	300 µm
500 µm	660 µm	950 µm	700 µm	600 µm

[a]Source: Fraunhofer IZM (Institute for Reliability and Microintegration), Germany

Chapter 4

Bidirectional DC-DC Converter Operation Theory

In this chapter, the operation theory of the bidirectional DC-DC converter designed in this thesis is explained. The DC-DC controller algorithms, which control the whole DC-DC converter, are described and analyzed in detail. The operating principle of novel functions needed for autonomous bidirectional power conversion, like automatic battery charger detection and continuous voltage regulation feedback loop, is described.

4.1 Controller Operating Direction

The bidirectional DC-DC converter has been developed for enabling energy to flow in and out of the mobile system's batteries. Therefore, the controller of the IPC provides two operating directions, selected automatically, depending on whether a battery charger is connected or not. The automatic detection of the presence of a charger is analyzed in Section 4.1.1. When a battery charger is connected to the load side, the energy flows from the charger to the battery, so the controller executes the charging algorithm. This is presented in Section 4.1.2. When the battery charger is removed, the energy flow reverses and the discharging algorithm is executed by the controller. This is presented in Section 4.1.3. The detection circuit of the presence of a load is presented in Section 4.1.4.

4.1.1 Automatic Battery Charger Detection

To manage bidirectional energy flows, the IPC must be able to recognize the presence of a battery charger automatically. Without such an ability, the battery would never be recharged. Figure 4.1 shows a simplified schematic of the connections needed by the IPC. The IPC is always powered by the battery voltage V_{batt}. On the battery side, four resistors are used to set up the three voltage thresholds: $V_{\text{batt(min)}}$, $V_{\text{batt(CP)}}$, and $V_{\text{batt(max)}}$. The voltage $V_{\text{batt(min)}}$ is used to set up the end-of-discharge battery voltage, which corresponds to the minimum allowed battery voltage at which the IPC will supply the load. If the battery voltage goes below $V_{\text{batt(min)}}$, the IPC shuts down to protect the battery from deep discharging damage. The $V_{\text{batt(CP)}}$ threshold sets up the value of the battery voltage V_{batt} below which the integrated charge pump must double the V_{batt} voltage to ensure that the internal core supply voltage V_{core} is

always constant and equal to 1.8 V. The sensed $V_{\text{batt(max)}}$ voltage is used to set up the maximum allowed battery voltage during the charging process. All these three sensed voltages are internally compared to a reference voltage V_{ref}. Therefore, the following equation system is used to calculate the corresponding resistor values:

$$\begin{cases} R_{\text{B4}} = \dfrac{V_{\text{ref}}}{V_{\text{batt(max)}}} \cdot \left(\displaystyle\sum_{i=1}^{4} R_{\text{B}i} \right) \\ R_{\text{B3}} = \dfrac{V_{\text{ref}}}{V_{\text{batt(CP)}}} \cdot \left(\displaystyle\sum_{i=1}^{4} R_{\text{B}i} \right) - R_{\text{B4}} \\ R_{\text{B2}} = \dfrac{V_{\text{ref}}}{V_{\text{batt(min)}}} \cdot \left(\displaystyle\sum_{i=1}^{4} R_{\text{B}i} \right) - R_{\text{B3}} - R_{\text{B4}} \\ \displaystyle\sum_{i=1}^{4} R_{\text{B}i} = \dfrac{V_{\text{batt(nom)}}}{I_{\text{B}}} \end{cases} \tag{4.1}$$

where $V_{\text{batt(nom)}}$ is the nominal battery voltage (2.7 V), I_{B} is the desired nominal bias current, V_{ref} is the internal reference voltage (520 mV), $V_{\text{batt(min)}}$ is the end-of-discharge battery voltage, $V_{\text{batt(max)}}$ is the maximum allowable battery voltage, and $V_{\text{batt(CP)}}$ is the battery voltage under which the internal charge pump must start to ensure the 1.8 V internal core voltage V_{core} (a recommended value for $V_{\text{batt(CP)}}$ is around 1.85 V).

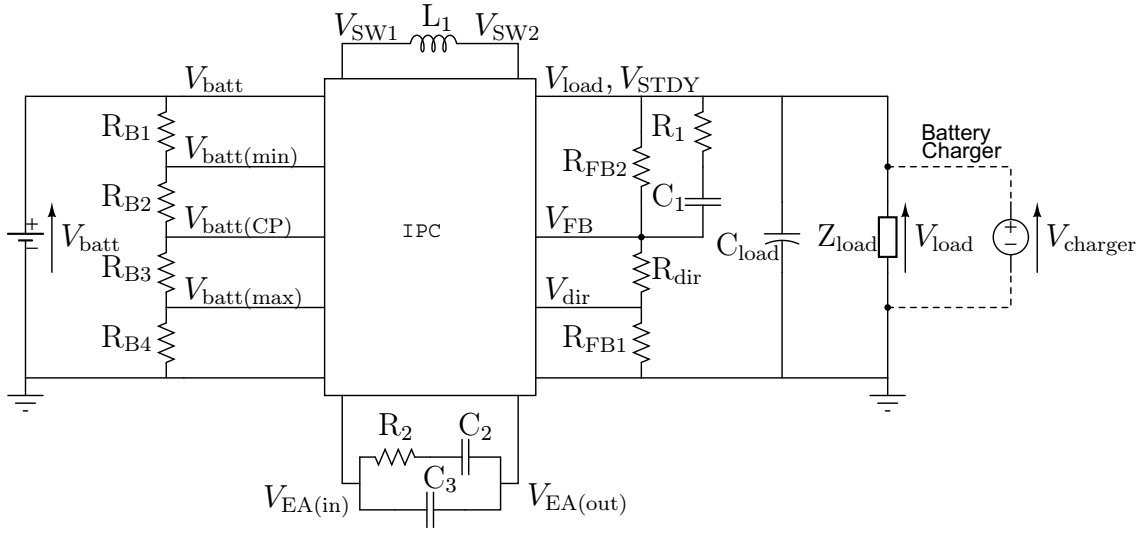

Figure 4.1: Connections of the bidirectional DC-DC converter to its environment.

The automatic detection of the battery charger occurs on the load side. When the IPC supplies the load, the load voltage is sensed through the feedback voltage V_{FB}. The resistors R_{FB1}, R_{FB2} and R_{dir} are used to set up the value of the load voltage V_{load} by adjusting the DC gain of the feedback loop. This is expressed by:

$$V_{\text{load}} = V_{\text{ref}} \cdot \frac{R_{\text{FB1}} + R_{\text{dir}} + R_{\text{FB2}}}{R_{\text{FB1}} + R_{\text{dir}}} \tag{4.2}$$

To allow the automatic detection of a battery charger, the sensed V_{dir} voltage must satisfy:

$$V_{\text{dir}} = V_{\text{charger}} \cdot \frac{R_{\text{FB1}}}{R_{\text{FB1}} + R_{\text{dir}} + R_{\text{FB2}}} > V_{\text{ref}} \tag{4.3}$$

The voltage threshold that is needed for a battery charger to be detected is set up by the resistor R_{dir}. Typically, if the IPC is set up for delivering a regulated voltage V_{load}, the battery charger must deliver a constant voltage V_{charger} that is typically 2-5% higher. Typically, the resistance R_{dir} is chosen to be 0.02 to 0.05 times R_{FB1}.

The schematic of the charger detection unit is shown in Figure 4.2. Because of the electrical connections shown in Figure 4.1, the V_{dir} voltage is always lower than the V_{FB} voltage. The digital CLK signal is the clock output from the triangular waveform oscillator unit, which is described in Section 5.1.3.3. The digital charging signal is high (i.e., equal to a logic **1**) when a battery charger was detected. It remains low (i.e., equal to a logic **0**) when no battery charger is present.

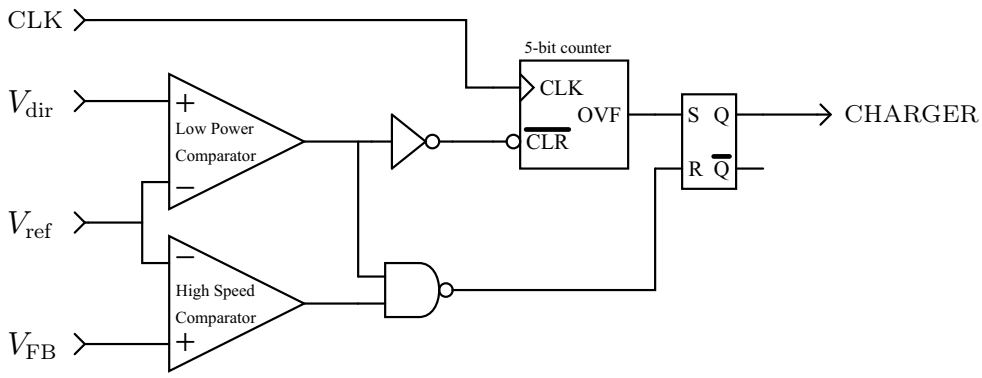

Figure 4.2: Automatic battery charger detection principle.

When the IPC supplies the load, the power supply of the fast comparator is turned off (i.e., its output is a logic **0**), therefore resetting the RS flip-flop shown in Figure 4.2. The value of the digital charger output is a logic **0**, meaning that no battery charger has been detected. If no charger is connected, V_{FB} is approximately maintained equal to V_{ref} by the external feedback regulation loop. This means that V_{dir} is below V_{ref}, thus the overflow output OVF of the counter is cleared (i.e., the CLR input gets a logic **1**, and the OVF provides a logic **0**). The power supply of the slow comparator is always turned on, because its role is to detect the presence of the battery charger. Since there is no timing constraint on the speed of the detection of the battery charger, this comparator is a very low power circuit.

Now, if a battery charger is connected to the load side, the V_{dir} voltage becomes higher than the reference voltage V_{ref} (see Figure 4.1 and Equation (4.3)). This removes the clear signal CLR, and the counter begins to count (at this moment, CHARGER is still equal to **0**). During this time, the power supply of the fast comparator is powered up. Since the V_{FB} voltage is above the reference voltage V_{ref}, the fast comparator outputs a logic **1**, thus tieing the R input of the RS flip-flop to a logic **0**. After a specific amount of time, which is set up by design so that the voltage ripple in V_{load} is filtered out and the fast comparator has enough time to turn on, the counter overflows and its OVF output goes high, thus setting the CHARGER signal to a logic **1**.

The role of the fast comparator is to immediately detect a fall in the V_{load} or V_{charger} voltage and reset the digital CHARGER signal, so that the V_{load} voltage remains in the specified voltage variation tolerance (typically $\pm 10\%$ of the nominal V_{load} value). If the battery charger is removed, the V_{load} voltage falls, as V_{FB} does. When V_{FB} falls below V_{ref}, the fast comparator immediately resets the CHARGER signal, and the IPC reverts the energy flow by using the battery to supply the load. The inversion of

the energy flow has been tested with the second IPC prototype. The corresponding measurements are presented in Section 6.2.4.

4.1.2 Charging Algorithm

A typical lithium-ion battery charging process is presented in Figure 4.3 [60].

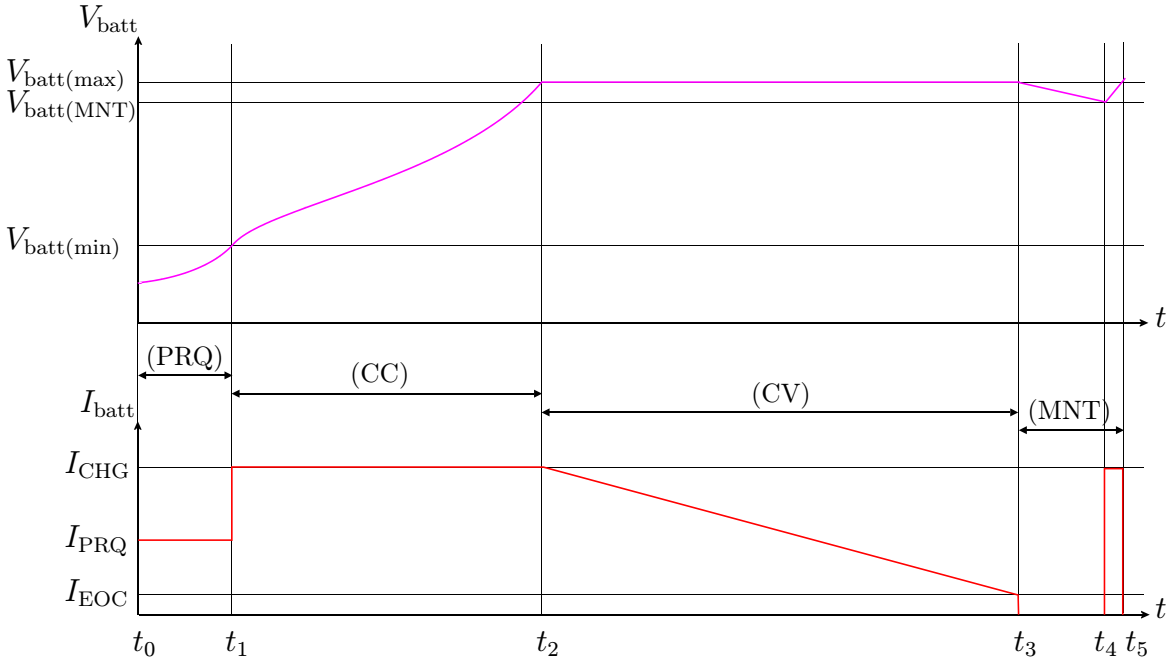

Figure 4.3: Battery voltage and current waveforms during charging process.

An important parameter of a battery is its energy capacity, also called C-rate, and given in Ah (Amperes · hours). For example, a 2 Ah battery can source a 2 A current during 1 hour before it is discharged. As listed below, the charging algorithm consists in four steps which are graphically illustrated in Figure 4.3.

- Prequalification mode (PRQ): this mode is entered only if the battery is deeply discharged (i.e., V_{batt} has fallen below $V_{batt(min)}$). During this phase (i.e., between t_0 and t_1 in Figure 4.3), the battery is charged with a constant low current I_{PRQ}, approximately 0.2 times its nominal current. After a deep discharge, this mode must be entered to prevent battery destruction, or simply to test if the battery is not damaged. If the battery voltage is not above $V_{batt(min)}$ after typically 2 hours, the battery is considered damaged and must be replaced.

- Constant Current mode (CC): during this mode, from t_1 to t_2, the battery is charged with the constant current I_{CHG}, while the battery voltage increases from $V_{batt(min)}$ to $V_{batt(max)}$. When $V_{batt(max)}$ is reached, the constant current mode ends up and the constant voltage mode is entered.

- Constant Voltage mode (CV): this is the last charging mode, during which the battery voltage is regulated to a constant voltage value equal to $V_{batt(max)}$. The current decreases and the charging stops when the end-of-charge current I_{EOC} is reached. At t_3, the battery can be considered as fully recharged.

- Maintenance mode (MNT): this mode is important and must be considered when a battery charger is connected for a long time to the mobile system, after the battery has been charged. A maintenance charge must be applied to the battery when its voltage falls below the given $V_{\text{batt(MNT)}}$ threshold, so that it is ensured that the battery is always fully charged when it is taken off from the charger.

The charging algorithm can then be deduced and plotted, as shown in Figure 4.4.

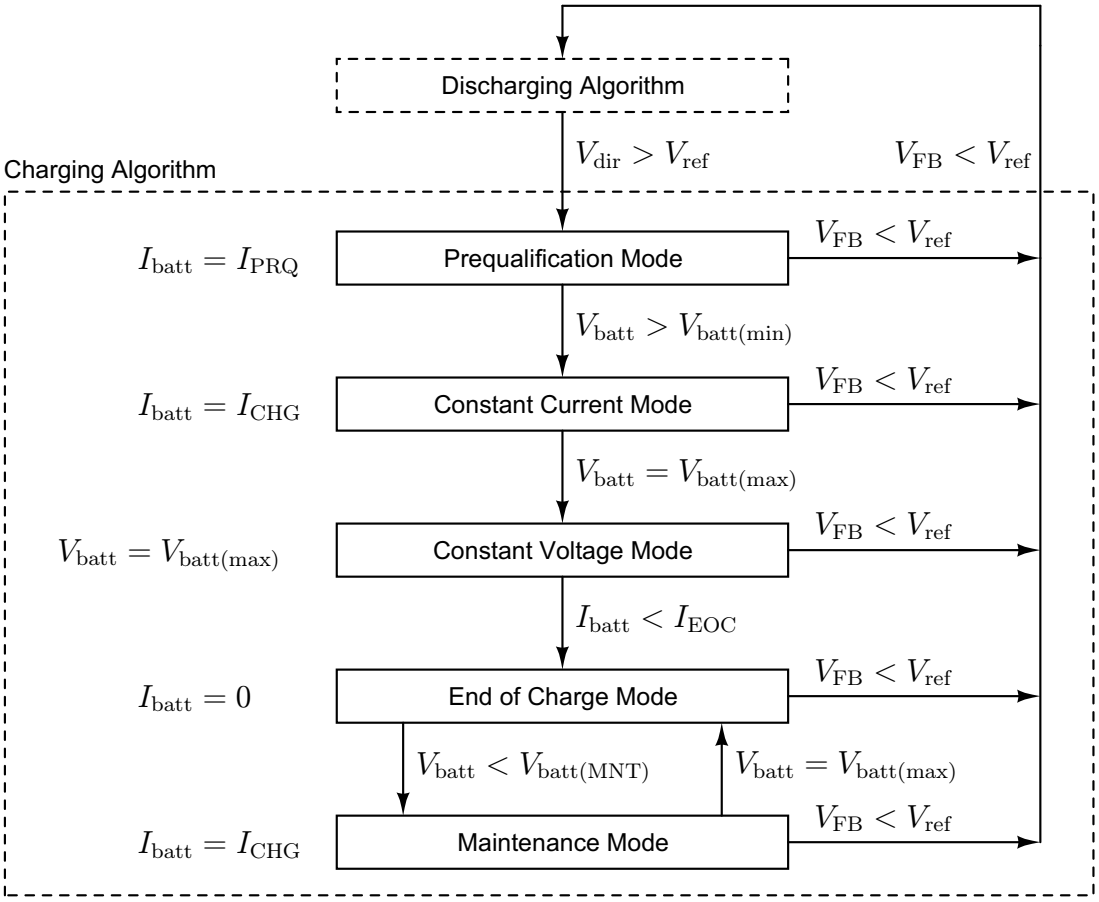

Figure 4.4: Charging algorithm of the IPC's controller.

4.1.3 Discharging Algorithm

The discharging algorithm must be especially well optimized because it contributes directly to the efficiency of the DC-DC converter. Several voltages and currents must be monitored to ensure that the IPC is operating in the best suited mode for the present situation. As illustrated in Figure 4.5, there are mainly four operating modes, when the IPC supplies the load with the energy of the battery:

- PWM mode: this is the default active mode, when a heavy load is connected to the load side of the IPC (i.e., when the load sinks more than I_{PWM}, which is typically equal to 100 mA). This mode uses an oscillator operating at fixed frequency, which can be adjusted by an external resistor.

- PFM mode: if the load sinks less than 100 mA of current, the IPC enters the PFM mode. In this mode, the oscillator is shut-down during the idle phases (see Figure 2.18) making it very power efficient at light loads, but also generating more voltage ripple on V_{load}. This mode is not suited for heavy loads sinking high currents, because it would require larger output capacitors to filter the high voltage ripple. The efficiency decreases at high currents, because of the current saturation phenomenon observed in the power inductor, which is a consequence of the higher current variations due to the lowered frequency.

- Standby mode: this mode is entered if the current sourced by the battery becomes very low (i.e., below I_{PFM}, which is typically less than 1 mA), two possibilities exist. The first possibility is that the load was removed and no load is currently connected to the output. The second possibility is that a charger was connected and no more current is sourced by the battery since it is sourced by the charger. Therefore, if the current sourced by the battery becomes too low, the standby mode is entered. A high impedance voltage source provides the voltage V_{STDY} and applies it to the output pin V_{load} (see Figure 4.1, Figure 4.6 and Section 4.1.4 for more details about the automatic load detection). The generated V_{STDY} voltage is greater than the internal voltage reference V_{ref} when no load is connected. If the monitored V_{STDY} voltage is sensed greater than the internal voltage reference V_{ref}, the IPC supposes that no charger is present and that the load was removed. If V_{STDY} becomes lower than V_{ref}, the connection of a new load occurred and the IPC immediately wakes up and enters the PWM mode to supply the load. Another possibility when waiting in the standby mode, is that V_{dir} becomes higher than V_{ref}. In this case, the IPC considers that a charger has been connected to the load side. In the standby mode, the only units that are supplied are the low power voltage reference, some comparators and some nonclocked digital gates.

- Shutdown mode: this mode is entered if the battery voltage V_{batt} falls below $V_{\text{batt(min)}}$. Only some nonclocked logic gates are supplied in this mode. Memory elements such as latches and flip-flops are needed to lock the IPC in this mode as long as no charger has been detected to recharge the fully discharged battery. No voltage reference nor amplifiers/comparators are running, so that the maximum amount of energy is saved. This is necessary for attaining the extremely low current consumption needed to prevent the battery from deep discharging during storage. Because of this, the only way to wake up the IPC from the shutdown mode is to perform a reset when a charger is connected to the load side.

The discharging algorithm is shown in Figure 4.5. It is entered when the battery charger is removed. It always starts with the PWM mode. If the current sunk by the load is not high enough (i.e., $I_{\text{load}} < I_{\text{PWM}}$), the IPC switches to the PFM mode to optimize the power conversion efficiency. If the load is removed, the IPC enters the standby mode. If the battery undergoes the end-of-discharge voltage, the IPC shuts down itself until a battery charger is connected and the IPC reset.

The PFM and the shutdown modes have not been implemented in the prototypes of the IPC, because they are not mandatory for proving the operation of the bidirectional DC-DC converter concept.

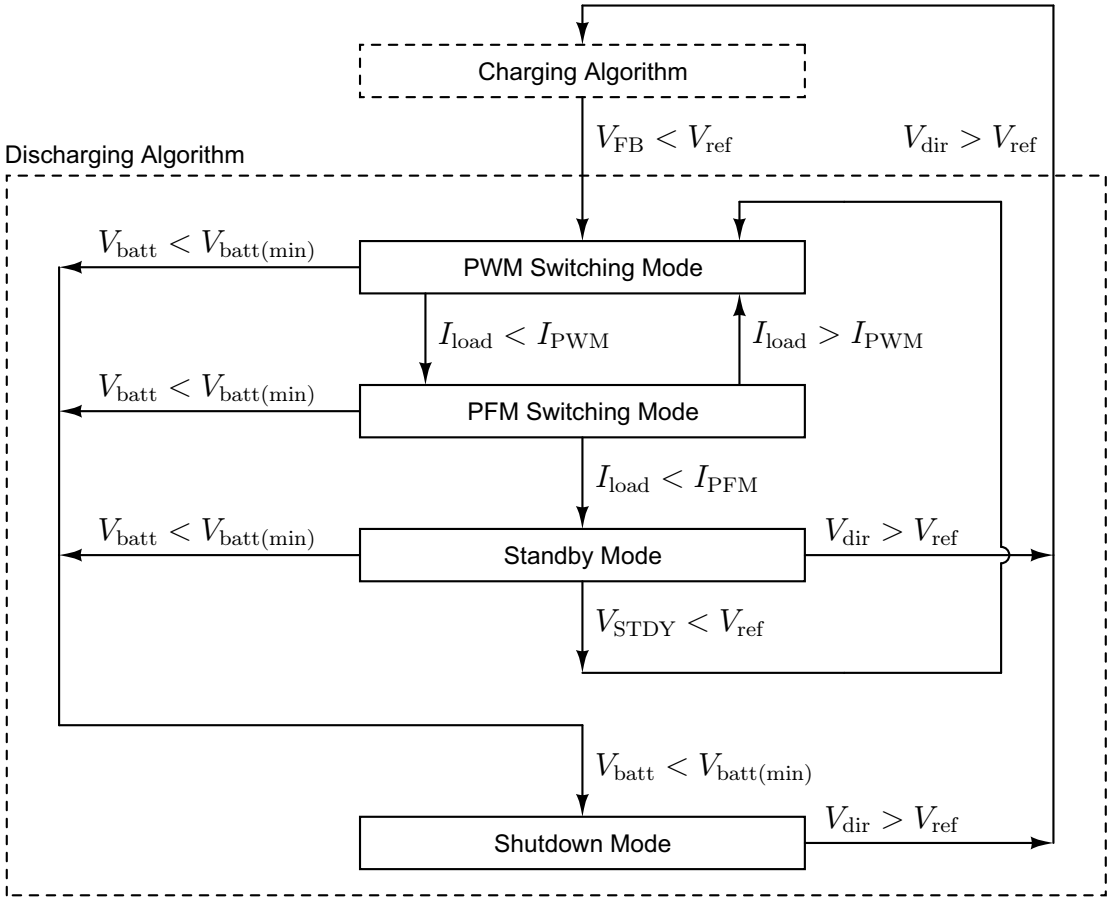

Figure 4.5: Discharging algorithm of the IPC's controller.

4.1.4 Automatic Load Detection

To manage the automatic shutdown and the wake-up of the bidirectional DC-DC converter, an automatic load detection unit has been developed. This unit is shown in Figure 4.6.

The STANDBY signal is equal to a logic **1** when the IPC is in standby mode, and the two switches shown in Figure 4.6 are then closed. The standby mode is entered only when the three following conditions are simultaneously valid: the battery is not discharged (i.e., V_{batt} is not below $V_{batt(min)}$), no load is connected, and no charger is connected. Therefore, the boolean expression of the STANDBY signal is given by:

$$\text{STANDBY} = \overline{\text{DISCHARGED}} \cdot \overline{\text{LOAD}} \cdot \overline{\text{CHARGER}} \tag{4.4}$$

The resistor R_{STDY} must be designed so that the voltage V_{STDY} generated through the current source I_{STDY} is higher than the reference voltage V_{ref} when the STANDBY switches are open, but lower than the nominal output voltage V_{load} requested by the load. This is mandatory to ensure that during standby, the load (if connected) will never be supplied by a V_{STDY} voltage higher than the nominal voltage of the load.

When the IPC is supplying the load, LOAD is equal to **1** and STANDBY is equal to **0**. The two STANDBY switches are therefore open, and V_{STDY} is higher than V_{ref}. The LOADDETECTED signal is equal to **0**, LOADTOOLIGHT is equal to **0**, and POWERGOOD

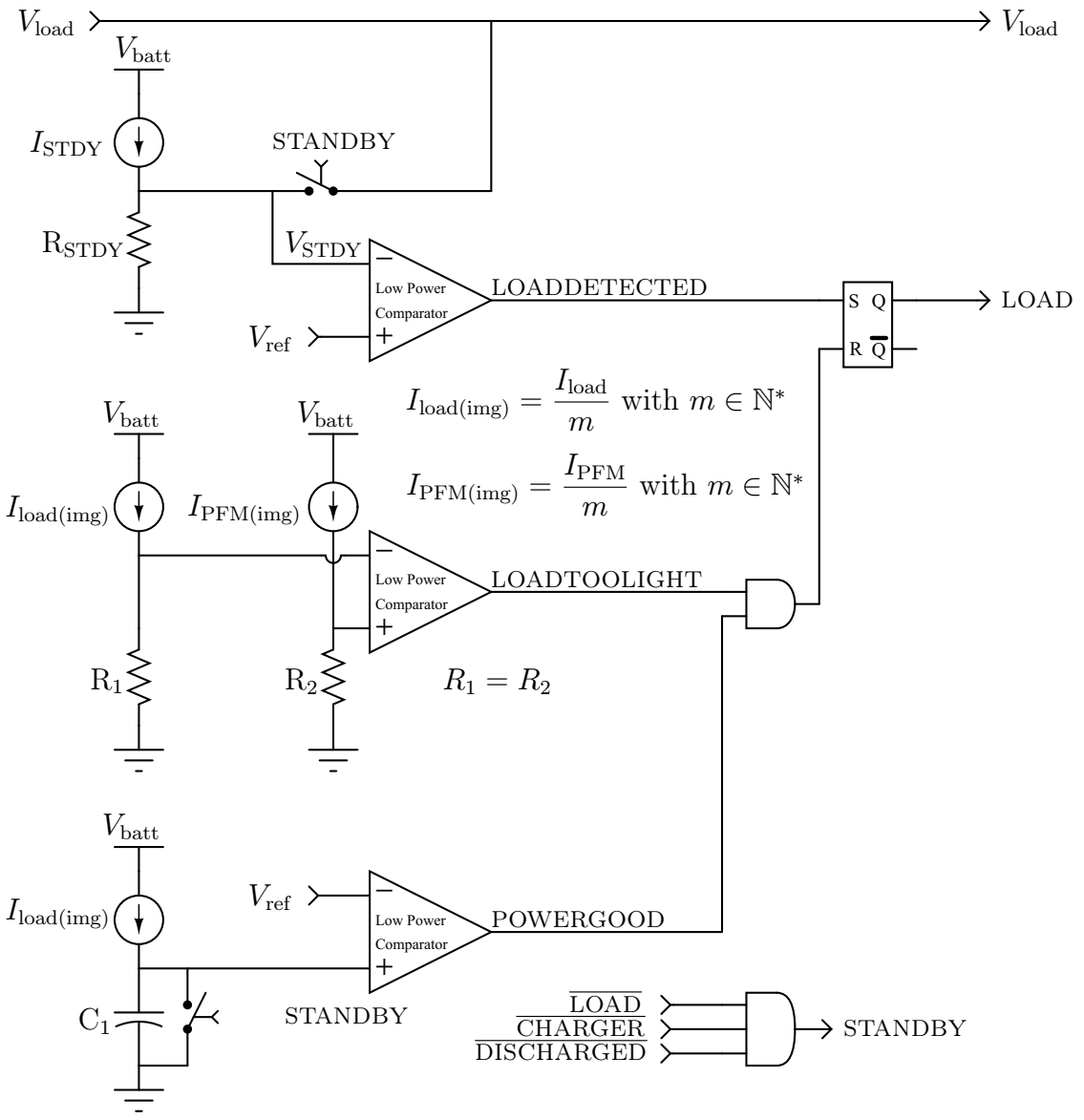

Figure 4.6: Automatic load detection principle. $I_{\text{load(img)}}$ and $I_{\text{PFM(img)}}$ are small current images of the currents I_{load} and I_{PFM}, respectively.

is equal to **1**. If now the load is removed, LOADTOOLIGHT becomes **1**, and the RS flip-flop is reset (i.e., LOAD becomes equal to **0**), thus closing the two STANDBY switches. As long as no load is detected, LOADDETECTED and POWERGOOD will stay equal to **0**. If now a load is connected, V_{STDY} drops below V_{ref}, and LOADDETECTED becomes equal to **1**, thus setting the RS flip-flop (i.e., LOAD becomes equal to **1**). The STANDBY switches open again, LOADDETECTED and LOADTOOLIGHT become equal to **0**, and after a short delay during which the capacitor C_1 is being charged, POWERGOOD becomes equal to **1**. The load detection unit is then ready to detect the next remove of the load.

The automatic load detection unit has not been implemented in the CMOS design of the IPC's prototypes, but its principle has been successfully tested in simulation.

4.2 Dynamic Power MOSFET Sizing

The efficiency and the size of the switching-mode power supplies are two essential points for the autonomy and the portability of mobile systems. State-of-the-art for driving the DC-DC converters in these power supplies is to use pulse-width modulation (PWM) with increasing switching frequencies [34]. This is done to reduce the size of the passive elements [28] or to integrate them on-chip [38]. However, above 1 MHz switching frequency, the switching losses in the power transistors become a limiting factor for the efficiency [36]. At high switching frequencies, the sizing of the power MOSFETs for achieving the highest efficiency in DC-DC converters is a trade-off between conduction losses and switching losses. Especially, the light-load efficiency in mobile systems suffers from high switching frequencies since the switching losses become predominant on the conduction losses.

Further, state-of-the-art is to add pulse-frequency modulation (PFM) to the DC-DC converters for achieving high efficiency also at low output currents. However, this variable frequency regulation control is difficult to stabilize [43]. Additionally, it provides a higher output voltage ripple which generates noise and sub-harmonic waves. These can dip in the audio spectrum or interfere with radio frequency design parts, such as power amplifiers for wireless communications.

An alternative to PFM is called *dynamic MOSFET sizing* (DMS) and consists in reducing dynamically the driven width W of the power MOSFETs. This consequently reduces the switched gate capacity and therefore the gate-charge losses, when the DC-DC converter supplies the load with only a fraction of the nominal output current (e.g., when the mobile system is in standby mode). This concept was first proposed as a discrete dual-gate MOSFET by R. Williams *et al.* in 1997 [36]. In 1998 A. Stratakos has implemented DMS in an integrated DC-DC converter [1]. Other methods for improving the light-load efficiency in constant switching frequency converters have been investigated in the literature, but the superiority of DMS in conversion efficiency improvement was demonstrated by H.-C. Lee *et al.* in 2005 [37].

In the following analysis, the light-load efficiency improvements provided by DMS in the synchronous buck converter shown in Figure 4.7 operating in continuous conduction mode (CCM) are analyzed at switching frequencies in the range of 1-100 MHz.

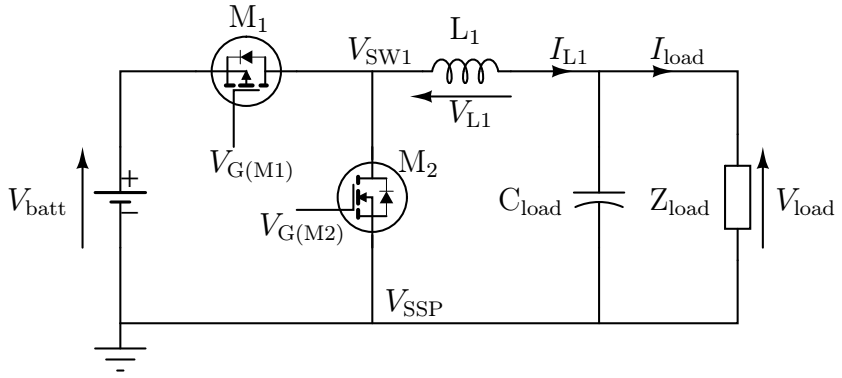

Figure 4.7: Synchronous buck converter schematic.

Dynamic MOSFET sizing results in switching of only a fraction W of the full width W_{tot} of the power MOSFET. This can be expressed by:

$$W = \beta \cdot W_{tot} \tag{4.5}$$

where β is a factor comprised in the interval $]0, 1]$. The ideal value of β is calculated in order to achieve the highest power conversion efficiency η when the DC-DC converter is operating at a constant PWM switching frequency f_{sw}.

4.2.1 Loss Mechanisms in Power MOSFETs

The models presented in this analysis are based on the synchronous buck converter shown in Figure 4.7 operating in CCM. The expression of the efficiency η is given by:

$$\eta = \frac{P_{\text{load}}}{P_{\text{load}} + P_{\text{cond(tot)}} + P_{\text{sw(tot)}} + P_{\text{fixed}}} \tag{4.6}$$

where P_{load} is the output power consumed by the load, $P_{\text{cond(tot)}}$ is the power lost through conduction in the power MOSFETs, and $P_{\text{sw(tot)}}$ is the power lost through the switching of the power MOSFETs and their gate drivers. P_{fixed} represents the constant power consumed by the PWM regulation unit (e.g., bias currents, voltage reference, error amplifier, sawtooth oscillator, PWM modulator). P_{fixed} is therefore partially dependent on the switching frequency f_{sw} but it does not scale with DMS.

Since synchronous rectification is used, the conduction losses $P_{\text{cond(tot)}}$ in the power transistors shown in Figure 4.8 are given by the expression:

$$P_{\text{cond(tot)}} = D \cdot P_{\text{cond}(p)} + (1 - D) \cdot P_{\text{cond}(n)} \tag{4.7}$$

$$P_{\text{cond}(p,n)} = \frac{R_{\text{DS(on)}(p,n)}}{\beta} \cdot I_{\text{L1}}^2 \tag{4.8}$$

where the indices p and n designate the PMOS and NMOS power transistors. D is the duty cycle, $R_{\text{DS(on)}}$ is the channel resistance of the MOSFETs at full width when the peak-drive voltage $V_{\text{G(PDV)}}$ is applied between gate and source, and I_{L1} is the current through the inductor L_1. The expression of the switching losses $P_{\text{sw(tot)}}$ in the power transistors are shown in Figure 4.8 and given by:

$$P_{\text{sw(tot)}} = P_{\text{sw}(p+n)} + P_{\text{oss}(p+n)} + P_{\text{rr}(p+n)} \tag{4.9}$$

$$P_{\text{sw}(p,n)} = P_{\text{DS}(p,n)} + P_{\text{G}(p,n)} + P_{\text{drv}(p,n)} \tag{4.10}$$

$$P_{\text{oss}(p,n)} = Q_{\text{oss}(p,n)} \cdot V_{\text{batt}} \cdot f_{\text{sw}} \tag{4.11}$$

where P_{oss} is the power dissipated by the charge Q_{oss} lost in drain-source and drain-gate capacitances of the power MOSFETs [61]. P_{rr} is the reverse recovery power lost in the body diodes. It is neglected here by considering that the converter operates without any dead-time. This is difficult to reach in practice, but not impossible when the dead-time can be adjusted during the operation. V_{batt} is the battery voltage appearing alternatively across the drain-source of M_1 and M_2 shown in Figure 4.7.

The switching losses $P_{\text{sw}(p,n)}$ are the sum of the drain-source losses P_{DS}, the gate-charge losses P_{G}, and the power losses in the gate-drive logic P_{drv}:

$$P_{\text{DS}} = \frac{1}{2} \cdot V_{\text{batt}} \cdot I_{L1} \cdot \left(t_{\text{c(on)}} + t_{\text{c(off)}}\right) \cdot f_{\text{sw}} \tag{4.12}$$

$$P_{\text{G}} = \beta \cdot Q_{\text{G}} \cdot V_{\text{G(PDV)}} \cdot f_{\text{sw}} \tag{4.13}$$

$$P_{\text{drv}} = \beta \cdot E_{\text{drv}} \cdot f_{\text{sw}} \tag{4.14}$$

where $t_{\text{c(on)}}$ and $t_{\text{c(off)}}$ are the turn-on and turn-off times of the MOSFET, and Q_{G} is the total gate charge when $V_{\text{G(PDV)}}$ is the gate-drive voltage. E_{drv} is the energy dissipated during one cycle in the gate-drive logic shown in Figure 4.9 and Figure 4.10.

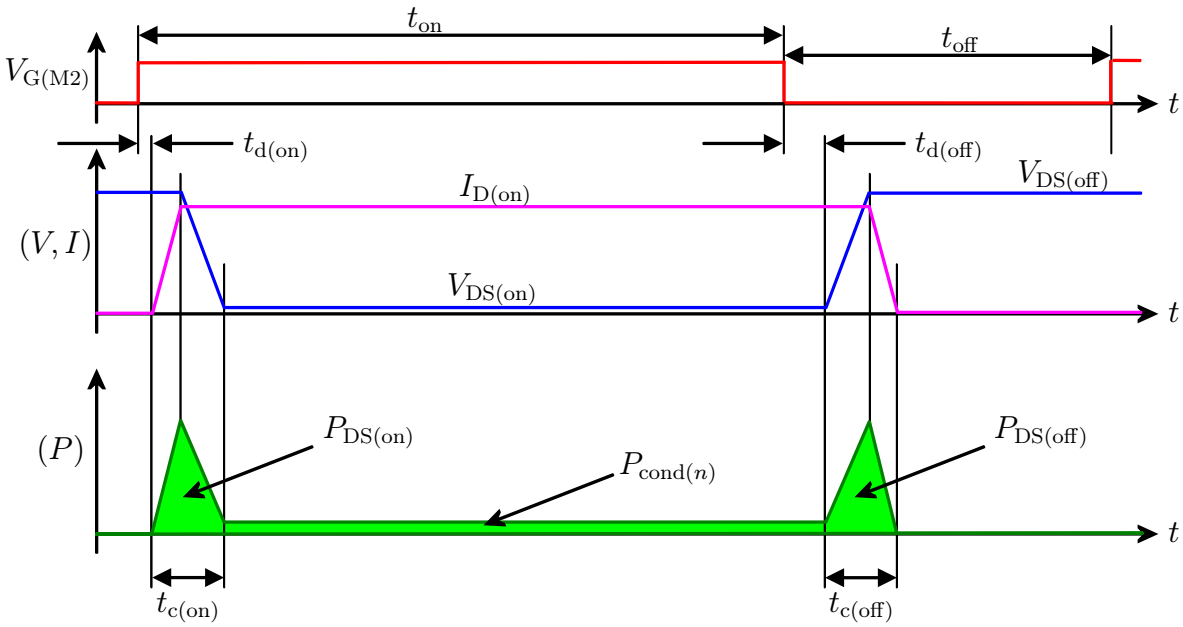

Figure 4.8: Conduction and switching losses in the NMOS M_2 in Figure 4.7.

4.2.2 Schematic Implementation of Dynamic MOSFET Sizing

Two schematic implementations of DMS in a gate-drive logic are illustrated in Figure 4.9 and Figure 4.10. Both alternatives are analyzed and compared. The gate-drive logic is built by the gate drivers (i.e., cascaded inverters with increasing transistor widths, to increase the drive strength), the logic level shifters, and the size decoder. The power NMOS M_2 is divided into parallel connected MOSFETs (M_{2a}, M_{2b}, M_{2c}, M_{2d}) with different widths. The same is done for the PMOS M_1. The PWM switching signal is only transmitted to the MOSFETs when the corresponding select signals are active (S_1, S_2, S_3, S_4).

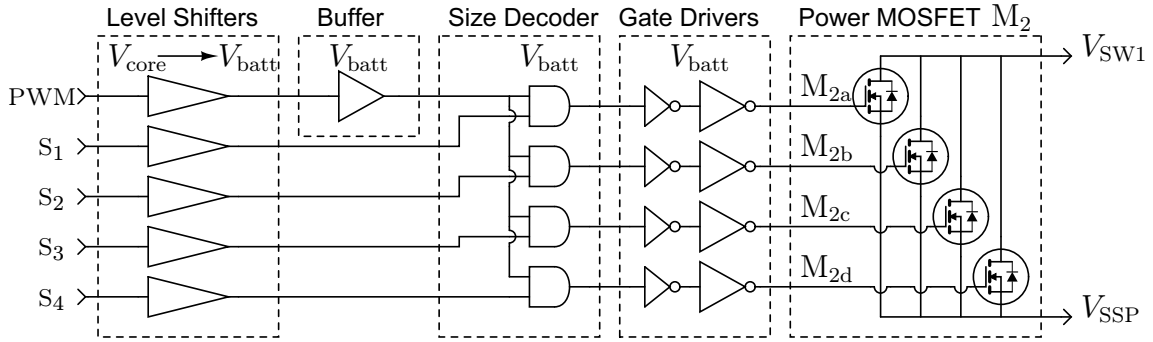

Figure 4.9: Schematic of the implementation of dynamic MOSFET sizing for the synchronous rectifier switch M_2 shown in Figure 4.7 when the logic level shifters are placed *before* the size decoder.

The DMS implementation shown in Figure 4.9 requires five logic level shifters: one for the PWM signal and one for each of the select signals (S_1, S_2, S_3, S_4). A drawback of this implementation is that the size decoder operates at high logic voltage levels (i.e., V_{batt}), thus dissipating more power than necessary. Because of the weak fan-out of

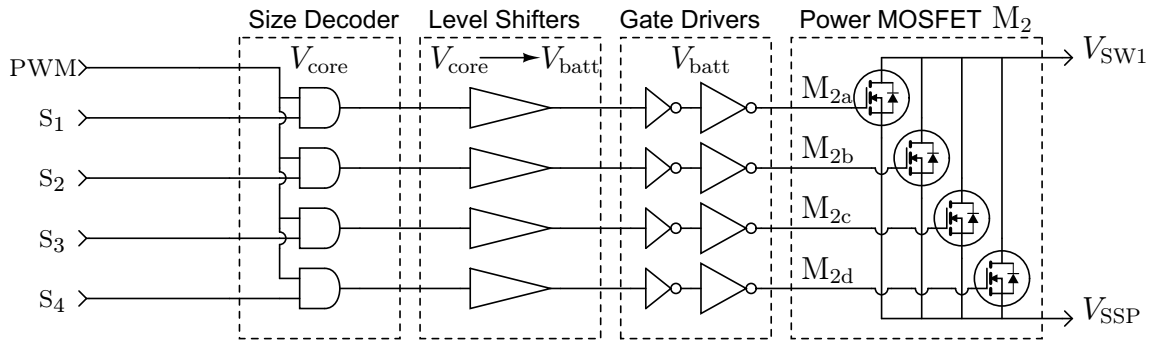

Figure 4.10: Schematic of the implementation of dynamic MOSFET sizing for the synchronous rectifier switch M_2 shown in Figure 4.7 when the logic level shifters are placed *after* the size decoder.

static logic level shifters, designs using this implementation generally need additional output buffers in the PWM signal path, thus increasing the power losses at high switching frequencies.

The DMS implementation shown in Figure 4.10 has the advantage of operating on the logic signals at the core voltage V_{core}, which is lower than V_{batt} (V_{core} is equal to 1.8 V for high-speed 0.18 µm CMOS technologies), thus dissipating less energy than the implementation of Figure 4.9. The size decoding is done before the logic level shifting, which guarantees a better defined propagation delay. Only the gate drivers connected after the logic level shifters are supplied with the battery voltage, which is higher than the core voltage.

This second implementation (Figure 4.10) was chosen for designing the IPC. The numerical values (e.g., E_{drv}) used for the efficiency simulations were also obtained from this implementation. The energy dissipated in the input of the size decoder is frequency dependent but it cannot be scaled by DMS. In the loss model equations, it is included in the constant power losses P_{fixed}.

4.2.3 Simulated Light-Load Efficiency Improvement

The synchronous buck converter shown in Figure 4.7 is considered to operate with ideal synchronous rectification (i.e., no dead-time) at a duty cycle D of 0.5. The two power transistors M_1 and M_2 are designed in the 0.18 µm mixed-signal CMOS technology from UMC and are sized in such a way that they can provide 2000 mA of continuous current at 80°C with a drain-source voltage drop V_{DS} of less than 50 mV when they are driven with a gate-source peak-drive voltage $V_{\text{G(PDV)}}$ of 1.8 V. A consequence is that the PMOS transistor M_1 must be sized approximately three times as wide as the NMOS transistor M_2. The minimum channel length of 340 nm was used for these 3.3 V power transistors. The losses in the passive devices (e.g., power inductor L_1, output filter capacitor C_{load}) were not considered in the models exposed here. For the NMOS, the total gate charge Q_{G} and the output charge Q_{oss} were determined to be 458 pC and 186 pC, respectively. These values are approximately tripled for the PMOS.

Figure 4.11 shows the converter's efficiency versus the effectively switched width W of the power transistors at several switching frequencies when a light load is supplied (e.g., I_{load} around 20 mA). It can be observed that the maximum of efficiency

is reached for a decreasing value of β when the frequency increases. This result is explained through the switching losses which become dominant over conduction losses at light loads for high switching frequencies. The factor β depends not only on the load current, but also on the switching frequency. Therefore, the best suited value for β at a given load current is a tradeoff between conduction losses and switching losses at the considered frequency, so that the maximum of efficiency is reached.

At PWM switching frequencies below 100 kHz, the conduction losses are predominant over the switching losses, and DMS does not provide a significant improvement in efficiency at light loads (i.e., at load currents below 1/10 of the nominal load). This is illustrated in Figure 4.11. Beginning with 1 MHz switching frequencies, the variation of the transistor's width provides improvement in efficiency.

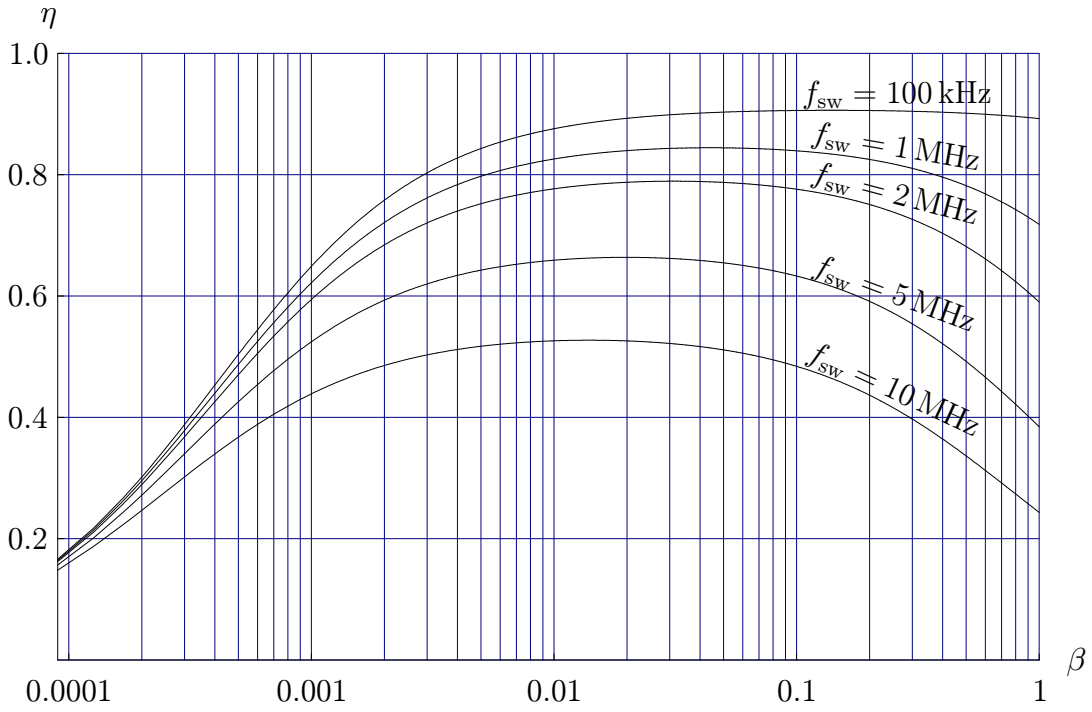

Figure 4.11: Efficiency η versus the transistor's width factor β at a light-load current I_{load} of 20 mA, which corresponds to $1/100^{th}$ of the nominal converter current.

At PWM switching frequencies above 10 MHz, the light-load conversion efficiency becomes significantly limited by the P_{oss} losses (due to drain-source and drain-gate capacitors), which are not scaled by DMS. This means that power MOSFETs with a channel length around 0.35 µm can only perform efficiently over less than two decades of load current at frequencies above 10 MHz.

Figure 4.12 and Figure 4.13 show the distribution of the efficiency depending on β as a function of the load current I_{load} at a PWM switching frequency of 1 MHz and 10 MHz, respectively. The asymptotic attainable efficiency obtained with the best suited value of β as a function of the load current is also plotted. To provide a high efficiency over the largest load current range, two values of β are sufficient at 1 MHz: 0.03, and 1. However, at 10 MHz, three values of β are suited: 0.03, 0.1, and 1. Below 0.03, further reduction of β means no more improvement in light-load efficiency, because of the P_{oss} losses, which are not scaled by DMS.

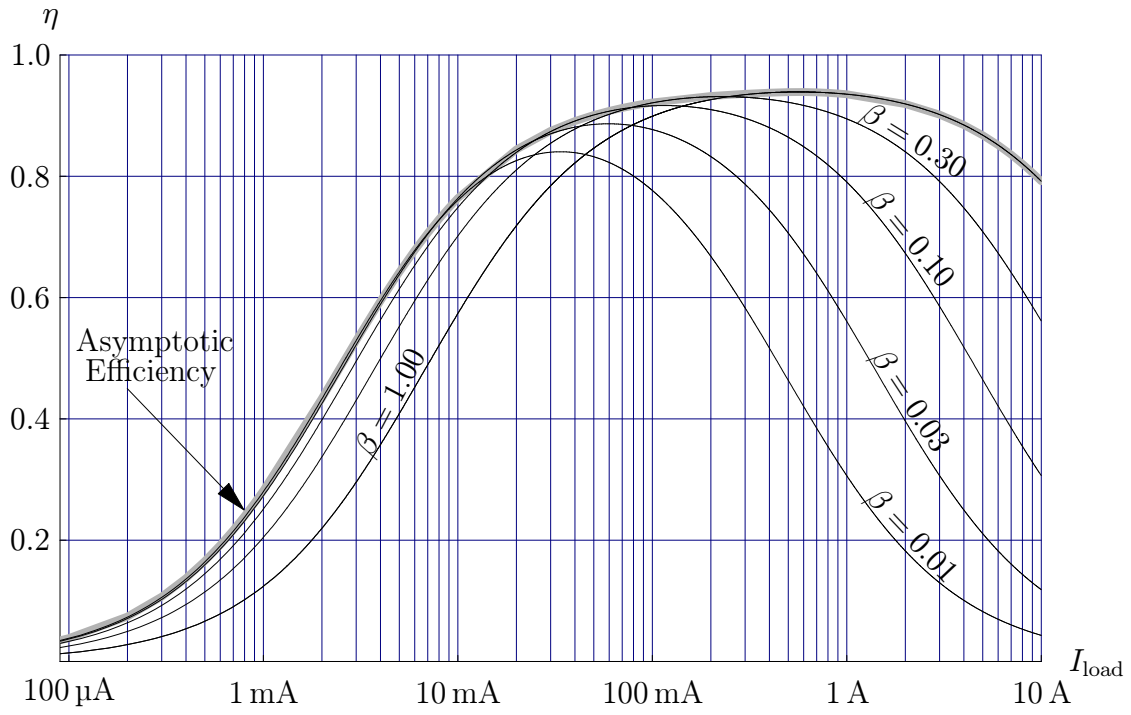

Figure 4.12: Efficiency η versus load current I_{load} at a switching frequency f_{sw} of 1 MHz.

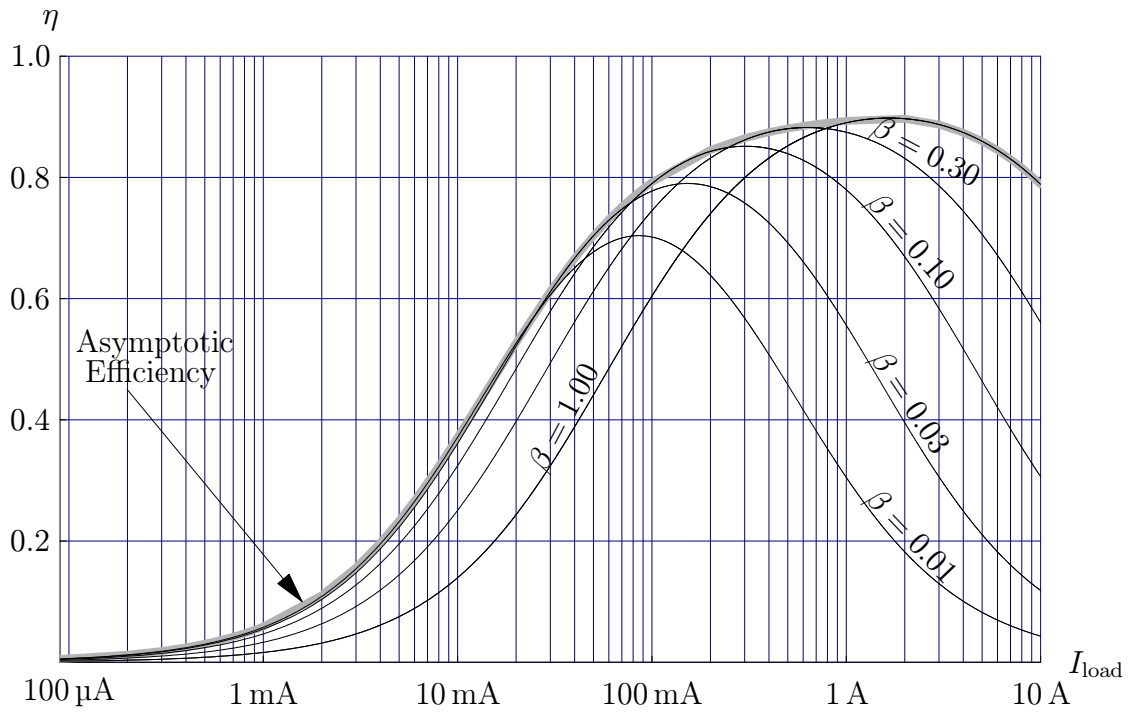

Figure 4.13: Efficiency η versus load current I_{load} at a switching frequency f_{sw} of 10 MHz.

Investigations of efficiency at light loads have shown that there is no significant advantage of deactivating synchronous rectification when DMS is used. An improvements of less than 2% was obtained with f_{sw} above 10 MHz and I_{load} below 20 mA.

The maximum efficiency attainable at a given PWM frequency with the synchronous buck converter in Figure 4.7 is shown in Figure 4.14. The best tradeoff between the size of the passive devices and the efficiency of the DC-DC converter is reached for a switching frequency in the 1-3 MHz range. When the size of the passive devices must be further reduced, DMS allows an efficiency higher than 80% over nearly two decades of output current up to a switching frequency of 10 MHz. Table 4.1 lists the maximum efficiency $\eta_{\max}$ and the maximum improvement in efficiency $\Delta_{\max}(\eta)$ obtained with DMS at different switching frequencies.

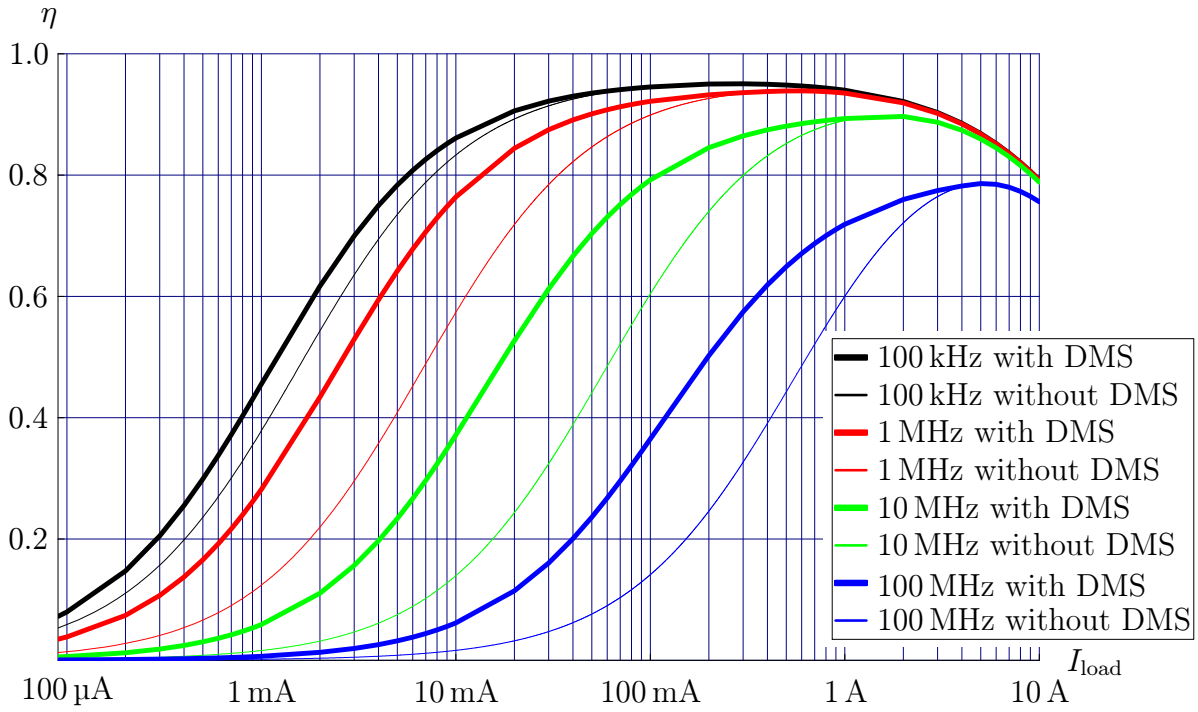

Figure 4.14: Comparison of the efficiency achieved with and without DMS.

Table 4.1: Maximum efficiency improvement provided by dynamic MOSFET sizing.

f_{sw}	100 kHz	300 kHz	1 MHz	3 MHz	10 MHz	30 MHz	100 MHz
$\eta_{\max}$	95.1%	94.7%	93.9%	92.5%	89.7%	85.7%	78.6%
@I_{load}	0.3 A	0.4 A	0.6 A	0.9 A	2.0 A	3.0 A	5.0 A
$\Delta_{\max}(\eta)$	7.73%	15.5%	23.7%	27.9%	28.9%	28.1%	25.7%
@I_{load}	1 mA	2 mA	4 mA	9 mA	30 mA	70 mA	200 mA

As illustrated in Figure 4.14 and Table 4.1, DMS provides more than 25% absolute improvement in efficiency for switching frequencies in the range of 3-30 MHz. By using DMS at a constant 10 MHz PWM switching frequency, the efficiency can be kept above 80% over roughly two decades of load current, without decreasing the switching frequency (Figure 4.14). In contrast to PFM modulation, the combination of PWM and DMS adds no voltage ripple to the output in case of a light-load condition. For low-ripple high-frequency switching DC-DC converters, DMS is clearly a control method of choice for improving the light-load efficiency.

4.3 Continuous Voltage Regulation Feedback Loop

The designed DC-DC converter must provide an adjustable voltage on the load side. As analyzed in Section 2.2.3.5, the H-bridge shown in Figure 4.15 provides the buck, buck-boost, and boost topologies. The role of the continuous voltage regulation feedback loop is to provide smooth transitions between these regulation modes.

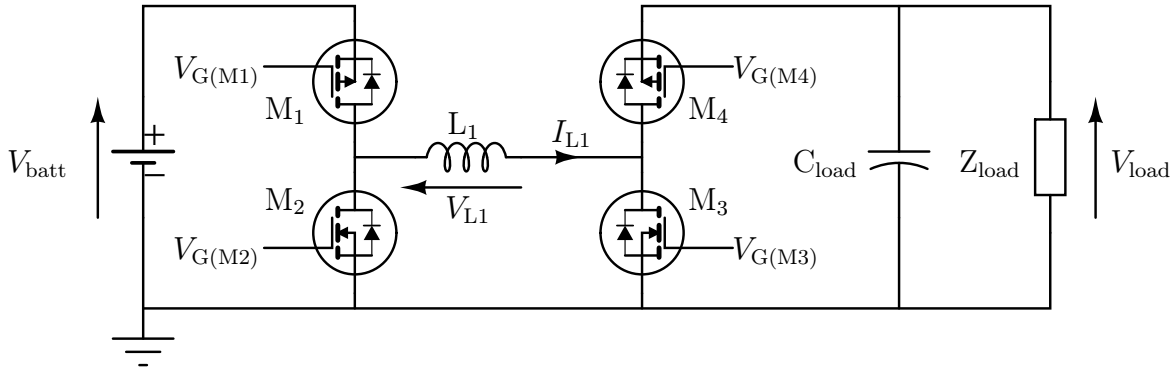

Figure 4.15: Representation of the power switches M_1, M_2, M_3, M_4 in the H-bridge.

A typical voltage discharge characteristic of a battery is illustrated in Figure 4.16. If the battery voltage V_{batt} is higher than the desired regulated voltage V_{load} on the load side, the IPC operates in the buck mode (i.e., step-down conversion). If the battery voltage V_{batt} is lower than the regulated voltage V_{load} on the load side, the IPC operates in the boost mode (i.e., step-up conversion). In some configurations, because the battery voltage decreases during the discharge, the regulation loop has to switch from buck mode to boost mode (this case is illustrated in Figure 4.16).

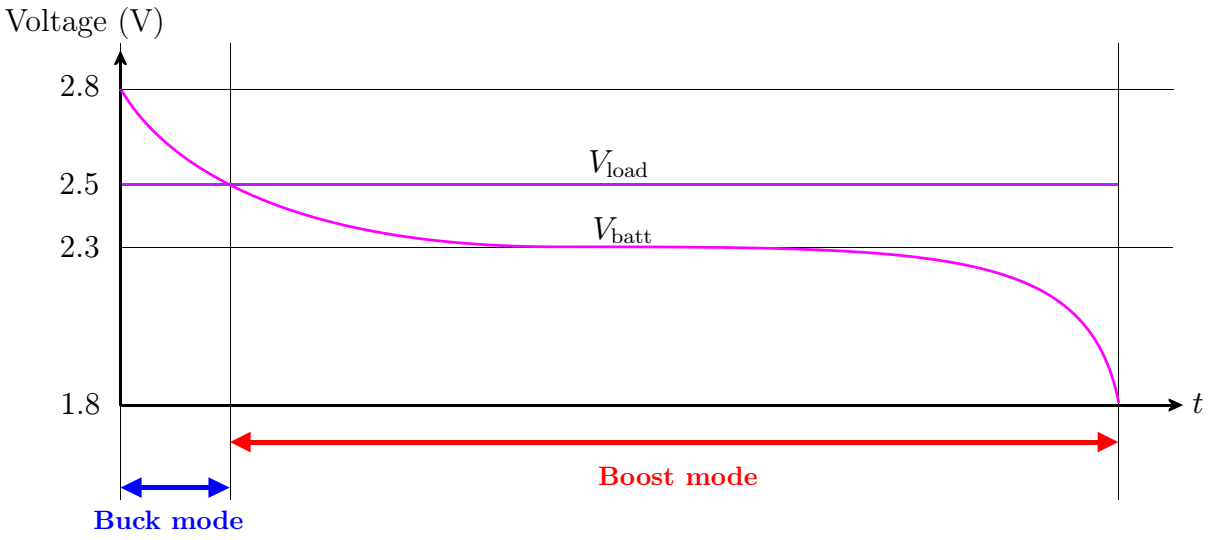

Figure 4.16: Voltage characteristic of a discharging battery.

4.3.1 Operating Principle of the Continuous Regulation Loop

Several methods for controlling the buck and boost modes in a DC-DC converter based on an H-bridge topology are described in the literature [62], [63], [64], [65]. The design of the control method for the IPC began in early 2004. In 2005, B. Sahu *et al.* have presented a control method which was based on smooth transitions between buck and boost mode comparable to the one that was developed in this work in parallel. However, B. Sahu *et al.* have not presented their concept via mathematical analysis of their control method [66], they have just simulated it in an unidirectional DC-DC converter, and no experimental results were provided. For the IPC, the control method is presented in Section 4.3.1.2 and the experimental results are presented in Section 6.2.3. Further, B. Sahu *et al.* have implemented a PFM mode additionally to the PWM mode [66], [67], [68], for increasing the light-load conversion efficiency. Indeed, the PWM/PFM mode selection is done manually, because no load-current sensing circuit was developed. For the IPC, a current sensing circuit has been designed and is presented in Section 5.1.4.2. In the bidirectional DC-DC converter, the same regulation principle is used in both conversion directions, thus keeping the design size to the minimum. Therefore, to simplify the description of the operating principle of the continuous regulation loop, only the direction when the battery is supplying the load is considered hereafter.

The basic idea behind the method of providing buck and boost mode regulation in an H-bridge converter topology consists in combining two PWM converters (i.e., a buck and a boost converter), as shown in Figure 4.17. With this assembly, the duty cycle D of both buck and boost converters can be controlled by a single internal control voltage V_{CI}, limited to $V_{\mathrm{D(lim)}}$ so that unlimited energizing of the inductor L_1 is avoided in boost mode. Theoretically, both converters can be juxtaposed, so that V_2 is equal to V_3. However, in practice, it is mandatory to have an overlap between buck and boost regions, which means that V_2 is lower than V_3, so that a third operating mode called *special buck-boost mode* is obtained. The reason for the necessity of this overlap is due to the implementation of the CMOS design (i.e., comparator's offset). This is investigated deeper in Section 5.1.3.

The combination with overlapping of a buck and a boost converter, both driven by a common control voltage V_{CI}, provides buck, buck-boost, and boost regulation, depending on the input voltage V_{batt} on the battery side and the requested output voltage V_{load} on the load side. When the battery voltage is approximately the same as the desired load voltage, the converter operates in the special buck-boost mode. This mode has the same basic function as the buck-boost converter presented in Section 2.2.3.1, but does not have the same transfer function (this is analyzed in Section 4.3.2). The special buck-boost mode covers the whole output voltage range, but all the four power transistors of the H-bridge must be switched during each cycle in this operating mode. Since the buck and boost modes only switch two of the four power transistors, these modes provide less switching losses and therefore a higher efficiency. This is the reason why these modes are associated to the special buck-boost mode.

The V_{CI} voltage is a control voltage generated internally by the DC-DC converter on the base of the output voltage provided by the error amplifier shown on the complete PWM regulator schematic depicted in Figure 5.19, and analyzed in detail at the transistor's level in Section 5.1.3. The V_{CI} voltage is an integrated value of the

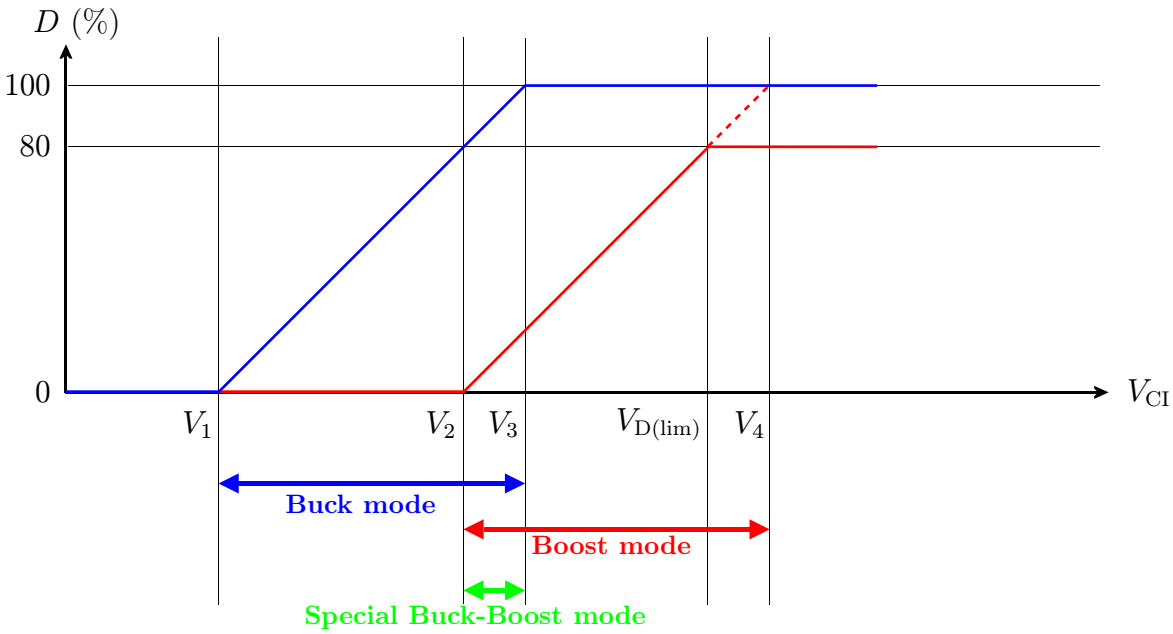

Figure 4.17: Overlapping assembly of buck and boost converter, with duty cycle limitation.

feedback voltage V_{FB} (see Section 5.1.3 for the detailed explanation of how the V_{CI} voltage is generated). The V_{CI} voltage increases when the V_{load} voltage on the load side is lower than the requested load voltage value. On the contrary, the V_{CI} voltage decreases when the V_{load} voltage on the load side is higher than the requested load voltage value. Two methods for implementing the combination of buck, buck-boost, and boost regulation are described hereafter.

4.3.1.1 State-of-the-Art Continuous Regulation Loop

The first known implementation of a continuous regulation loop over buck, buck-boost, and boost modes comes from the american ICs manufacturer Linear Technology [62], [63] in 2001 with its LTC3440, a commercial DC-DC converter [69]. It consists in the combination of a buck and a boost converter, as shown in Figure 4.18. However, this unidirectional converter topology has important drawbacks. Since it uses two different sawtooth signals V_{osc1} and V_{osc2}, it requires an output phasing circuit, which makes the circuit complex, thus consuming more die area and reducing the converter efficiency by wasting additional power through switching signals.

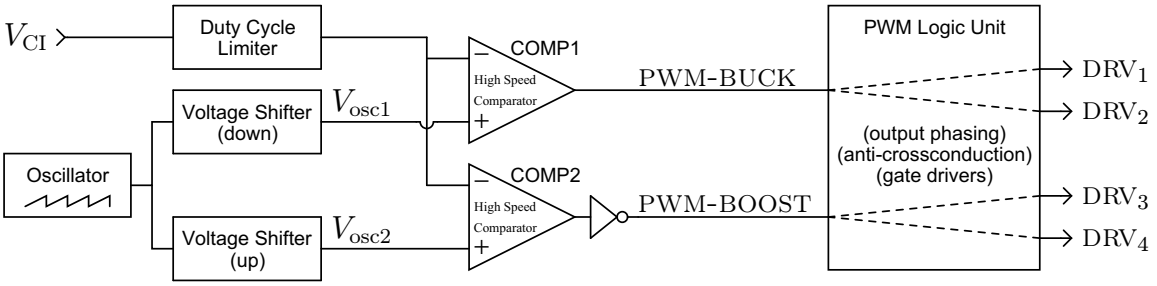

Figure 4.18: Implementation of the continuous regulation loop in the LTC3440.

The operating principle of the LTC3440 consists in a sawtooth oscillator, that generates the carrier for the two PWM comparators COMP1 and COMP2. The voltage shifter on the buck side is connected to the noninverting input of COMP1. It adds a negative voltage shift to the sawtooth waveform generated by the oscillator, thus providing the V_{osc1} signal which is switching between V_1 and V_3 (see Figure 4.17 and Figure 4.18). The voltage shifter on the boost side is connected to the noninverting input of COMP2. It adds a positive voltage shift to the sawtooth waveform generated by the oscillator, thus providing the V_{osc2} signal which is switching between V_2 and V_4. The control voltage V_{CI} is clamped to $V_{D(lim)}$ to limit the maximum duty cycle of the boost PWM comparator COMP2, as illustrated previously in Figure 4.17. The PWM-BUCK and PWM-BOOST signals are digital outputs, which are used to command the power transistors M_1, M_2, M_3, M_4 shown in Figure 4.15. These digital signals are processed by the PWM logic unit by adding dead-times to avoid crossconduction between M_1, M_2, and between M_3, M_4 (see Section 5.2.1 for more details about the anti-crossconduction logic). All these signals are shown in the timing diagram plotted in Figure 4.19. Gate drivers must be inserted between the PWM logic unit and the power transistors M_1, M_2, M_3, M_4. For complexity reasons, the PWM-BUCK and PWM-BOOST digital signals shown in Figure 4.18 are considered to drive directly the gates of the power transistors M_1, M_2 and M_3, M_4, respectively (see Figure 4.15).

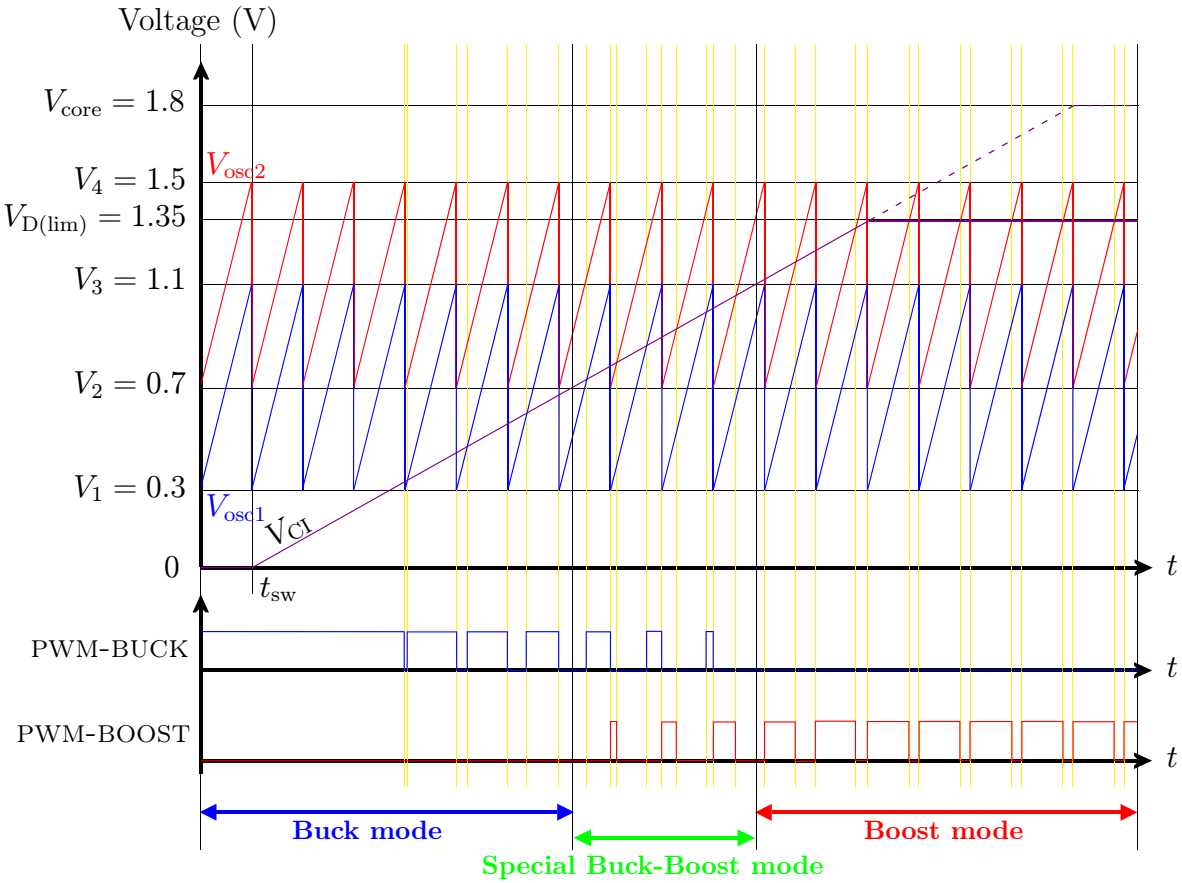

Figure 4.19: Buck and boost modes timing diagram in the LTC3440.

When the PWM-BUCK signal provides a logic **0**, the transistor M_1 (PMOS) is switched on and the transistor M_2 (NMOS) is switched off. When the PWM-BUCK

signal provides a logic **1**, the transistors M_1 and M_2 behave the other way around. When the PWM-BOOST signal provides a logic **0**, the transistor M_4 (PMOS) is switched on and the transistor M_3 (NMOS) is switched off. When the PWM-BOOST signal provides a logic **1**, the transistors M_4 and M_3 behave the other way around. The control voltage V_{CI} is clamped to $V_{D(lim)}$, which is typically 75-95% of the maximum V_{osc2} voltage value. This limits the maximum duty cycle of the boost mode to 75-95% and avoids the unlimited energizing of the inductor L_1 through the turned on power transistors M_1 and M_3, which would result in a failure by overcurrent (see Figure 4.15).

The control method used in the LTC3440 for getting smooth transitions between the operating modes was further used in the LTC3441, LTC3442, LTC3443 converters. However, for high frequency DC-DC converters with on-chip inductor and synchronous rectification, this method is not suitable, because of the difficulty to control the dead-times during the buck-boost operation mode.

4.3.1.2 Novel Continuous Regulation Loop

For designing a DC-DC converter supporting bidirectional energy flows, a fully novel control method had to be developed. The IPC implements a PWM buck and a PWM boost converter, which are driven by a single oscillator. Figure 4.20 shows the electrical block diagram of the combined buck and boost converters in the IPC.

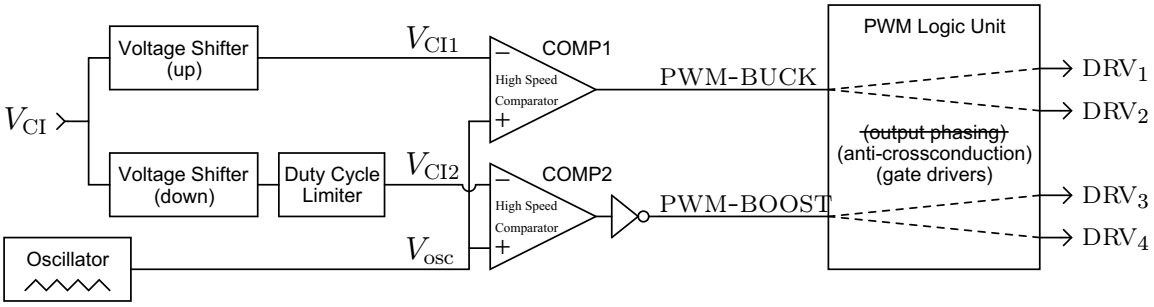

Figure 4.20: Implementation of the continuous regulation loop in the IPC.

Unlike Linear Technology which uses two sawtooth carriers, a single symmetrical triangular carrier is generated by the oscillator of the IPC. This provides slower edges and therefore lower EMI at high switching frequencies [3]. A single high frequency symmetrical triangular carrier generates less noise than two shifted sawtooth carriers. When an on-chip power inductor is used, the bidirectional DC-DC converter must be able to operate at frequencies up to 10 MHz.

The symmetrical triangular carrier is directly used by the two PWM comparators, COMP1 and COMP2, as shown in Figure 4.20. Unlike Linear Technology, no voltage shifting is done on this high frequency switching signal. Therefore, no high speed voltage shifters are needed and less power is consumed. In the IPC, it is the low frequency control voltage V_{CI} that is shifted up for the buck converter, and shifted down for the boost converter. The shifted up control voltage becomes V_{CI1}. The shifted down control voltage is additionally clamped, before becoming V_{CI2}. This provides the boost mode duty cycle limitation. The advantage of this clamping method is that it is accurately done by the addition of only one transistor in the schematic design (see Section 5.1.3.2). The PWM-BUCK and PWM-BOOST digital output signals drive the

same circuit as these of the LTC3440 block diagram in Figure 4.18. No gate drivers for the power transistors are considered here.

The reason of the presence of the inverter (INV) in Figure 4.20 is explained by the properties of the high speed comparators COMP1 and COMP2. Due to their topology, these comparators have a noisy and a quiet input. The noisy input is noninverting, while the quiet input is inverting. Both comparators get the same symmetrical triangular carrier on their noisy input. The quiet inputs are connected to the shifted control signals V_{CI1} and V_{CI2}, which are therefore not perturbed by the switching of the comparators outputs. The reason why it has been decided to shift both V_{CI1} and V_{CI2} remains from the CMOS implementation. Both control voltages are isolated from each other, and a perturbation on one has no effect on the other one (more details are found in Section 5.1.3). Due to the amount of voltage difference between V_{CI1} and V_{CI2} (typically 700 mV), when the triangular carrier gets a glitch due to the switching of one of the high speed comparators output, the other comparator is not perturbed by the generated noise on the triangular carrier it sees (see Section 5.1.3.4).

Figure 4.21 shows the timing diagram of the novel continuous regulation method developed for the IPC. As explained, the control voltage V_{CI} is not used directly by the comparators. Only the shifted control voltages V_{CI1} and V_{CI2} are used by the comparators. Since V_{CI} is shifted upwards to become V_{CI1} and downwards to become V_{CI2}, V_{CI1} is always above V_{CI2}. When V_{CI2} is lower than V_1, the converter runs in buck mode. When simultaneously V_{CI1} is above V_1 and V_{CI2} below V_2, the converter runs in the special buck-boost mode. When V_{CI1} is above V_2, the converter runs in boost mode. The timing diagram shown in Figure 4.21 also illustrates the V_{CI2} clamping to $V_{\mathrm{D(lim)}}$, limiting the maximum duty cycle of the PWM-BOOST signal.

When comparing the timing diagram of the novel control method developed for the IPC (see Figure 4.21), and the timing diagram of the state-of-the-art control method used by the LTC3440 (see Figure 4.19), a significant functional difference appears in the special buck-boost mode region. With sawtooth carriers (like in the LTC3440), there is simultaneously a falling edge on PWM-BUCK and a rising edge on PWM-BOOST, as illustrated in the timing diagram in Figure 4.19. This introduces a timing violation, because two edges never occur simultaneously in practice. In worst case, PWM-BUCK still provides a logic **1** when PWM-BOOST has provided the rising edge. This turns on both NMOS M_2 and M_3 simultaneously in Figure 4.15 (M_1 and M_4 are turned off). The consequence is lost power, because the inductor is de-energized in a ground loop (i.e., the inductor current flows through M_2, L_1, M_3). By using a symmetrical triangular carrier like it is done in the IPC and illustrated in Figure 4.21, this timing violation phenomenon is avoided, because the one pulses (i.e., the pulses at which the NMOS M_2 and M_3 are turned on) of both PWM-BUCK and PWM-BOOST signals are centered and cannot overlap themselves, providing the longest possible blanking time between a PWM-BUCK pulse and a PWM-BOOST pulse. For this reason, no output phasing circuit is needed in this novel control method.

Further, by the control method used in the LTC3440 (see Figure 4.18 and Figure 4.19), when a sawtooth carrier is used in place of a triangular carrier, and especially when it is additionally shifted up and down, both shifted carriers are not absolutely identical (i.e., in phase and in distortion). A skew is inevitably introduced between the V_{osc1} and the V_{osc2} signals in the LTC3440. Therefore, an additional delay control circuit must be added to the PWM logic unit to control the phasing between the PWM-BUCK and the PWM-BOOST signals. This makes the PWM logic unit more com-

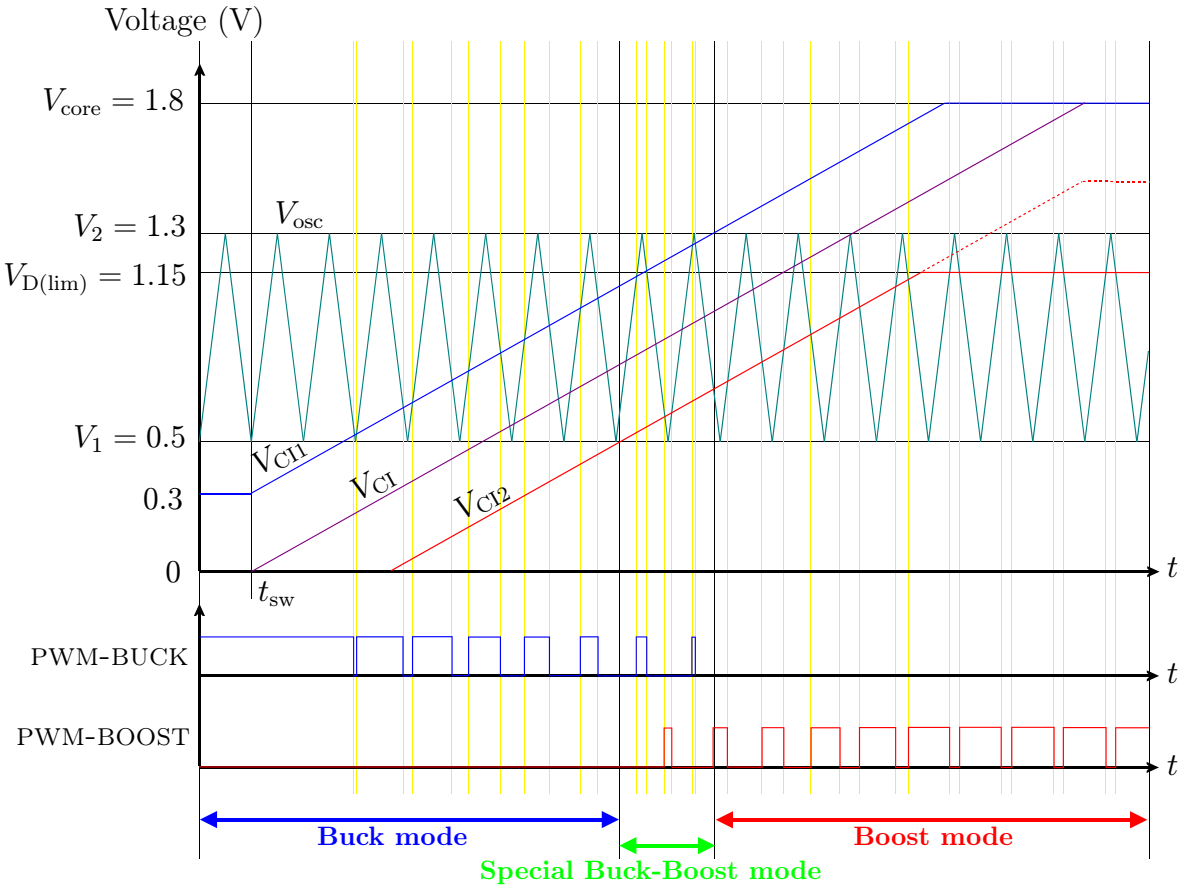

Figure 4.21: Buck and boost modes timing diagram in the IPC.

plex in the LTC3440. This phasing is automatically controlled when the method implemented in the IPC is used, since the one pulses on PWM-BUCK and on PWM-BOOST are automatically centered by using an unique triangular carrier (see Figure 4.20 and Figure 4.21). No skew is introduced on the carrier, since the same carrier signal is used with both comparators COMP1 and COMP2. The pulses are automatically centered when using a symmetrical triangular carrier. Additionally, by separating and centering the pulses on the PWM-BUCK and PWM-BOOST signals, the current peaks created by the gate drivers (due to gate capacitance charging/discharging and shortcut current in the inverters used in the gate drivers) are spaced and their amplitudes are reduced since the internal decoupling capacitors connected between the supply rails have more time to recharge themselves (the time separating two falling edges on PWM-BUCK and PWM-BOOST signals is the longest possible in Figure 4.21). The mathematical analysis of the novel method used in the IPC is exposed in Section 4.3.2.

4.3.2 Transfer Function of the IPC

The voltage conversion factor M is the ratio of the output load voltage V_{out} divided by the input battery voltage V_{in}. It is only a function of the duty cycle D of the PWM signal when the converter is operating in the continuous conduction mode (CCM) (i.e., the inductor current can reverse at light loads due to synchronous rectification). When the IPC performs step-down conversion, it runs in the buck mode. As shown

in Section 2.2.2.1, the relation between V_{in} and V_{out} in a buck converter is given by:

$$M_{\text{buck}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{t_{\text{on}}}{t_{\text{sw}}} = D \tag{4.15}$$

When the IPC performs step-up conversion, it runs in the boost mode. As shown in Section 2.2.2.2, the relation between the input battery voltage V_{in} and the output load voltage V_{out} in a boost converter is given by:

$$M_{\text{boost}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{t_{\text{sw}}}{t_{\text{sw}} - t_{\text{on}}} = \frac{1}{1-D} \tag{4.16}$$

When the IPC has to supply a load voltage V_{out} that is close to the battery voltage V_{in}, the special buck-boost mode is entered. As presented in Section 2.2.3.1, a standard noninverting buck-boost converter provides a transfer function given by:

$$M_{\text{buck-boost}} = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{t_{\text{on}}}{t_{\text{sw}} - t_{\text{on}}} = \frac{D}{1-D} \tag{4.17}$$

However, the special buck-boost mode resulting from the combination of the buck and the boost converters in the IPC does not satisfy Equation (4.17), because the overlapping range between the buck and the boost converters is not total. Therefore, when the DC-DC converter is performing in the special buck-boost mode, the duty cycles D_{buck} and D_{boost} of the buck and boost converters, respectively, are not complementary. In other words, the logic **1** pulses generated by the comparators COMP1 and COMP2 are not complementary over one period t_{sw}. For example, when both M_1 and M_3 are turned off, M_2 and M_4 are not necessarily both turned on, as it would be the case in a typical buck-boost converter. This phenomenon is shown in Figure 4.22 and is analyzed from the mathematical point of view hereafter.

To calculate the transfer function of the special buck-boost mode, the following hypotheses are considered (refer to Figure 4.22):

- The input voltage (V_{in}) is supposed to be constant over one period t_{sw}.
- The converter is operating in steady-state. The control voltages (V_{CI}, V_{CI1}, and V_{CI2}) are constant over one period t_{sw}.
- The output capacitor C_{load} filters out the voltage ripple. The small ripple approximation [41] allows to consider the output voltage (V_{out}) as constant over one oscillator period t_{sw}.
- The inductor current $I_{\text{L1}}(t)$ is continuous and periodic. It satisfies the equation:

$$I_{\text{L1}}(t) = I_{\text{L1}}(t_{\text{sw}} + t) \tag{4.18}$$

- The converter operates in the special buck-boost mode. This implies that:

$$0 < V_1 < V_{\text{CI2}} < V_{\text{CI}} < V_{\text{CI1}} < V_2 < V_{\text{core}} \tag{4.19}$$

- The shift voltage V_{shift1} is added to the control voltage V_{CI} to become V_{CI1}, while the shift voltage V_{shift2} is subtracted from V_{CI} to become V_{CI2}. These shift voltages are not necessarily equal, but they are both supposed to be positive.

$$V_{\text{CI1}} = V_{\text{CI}} + V_{\text{shift1}} \tag{4.20}$$

$$V_{\text{CI2}} = V_{\text{CI}} - V_{\text{shift2}} \tag{4.21}$$

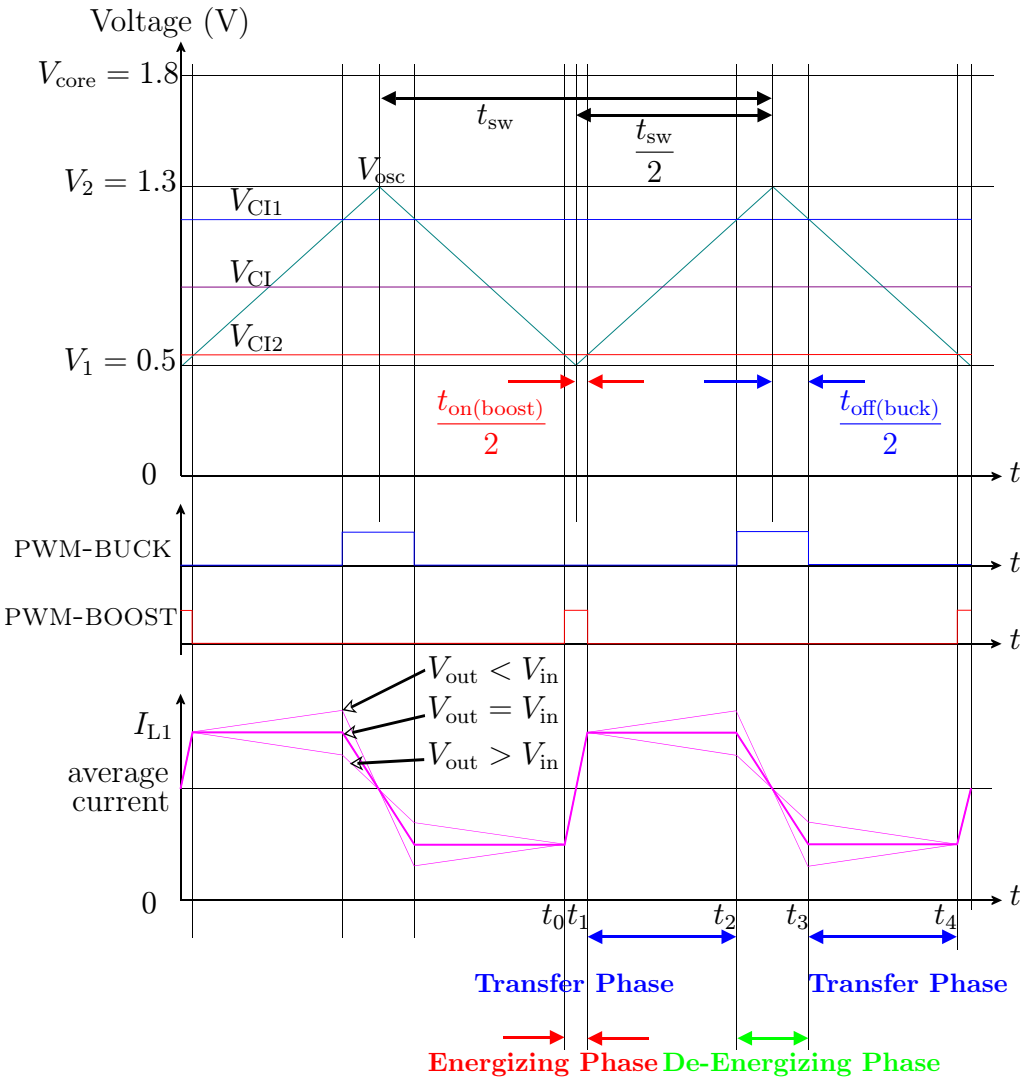

Figure 4.22: Special buck-boost mode running in steady-state. The three different inductor current waveforms I_{L1} are only given as overview. They are not scaled on each other.

- The timings t_1, t_2, t_3, t_4 in Figure 4.22 are defined as follow:

$$\begin{cases} t_1 - t_0 = t_{on(boost)} \\ t_2 - t_1 = \frac{t_{sw}}{2} - \frac{t_{on(boost)}}{2} - \frac{t_{off(buck)}}{2} \\ t_3 - t_2 = t_{off(buck)} \\ t_4 - t_3 = \frac{t_{sw}}{2} - \frac{t_{on(boost)}}{2} - \frac{t_{off(buck)}}{2} \end{cases} \tag{4.22}$$

The signal waveforms used to calculate the transfer function of the special buck-boost mode are shown in Figure 4.22. By considering the time interval t_0 to t_4 (i.e., one complete oscillator period t_{sw}), three schematic configurations occur. These configurations are shown in Figure 4.23. The time interval t_0 to t_1 corresponds to the *energizing phase* in a basic boost converter. The inductor is connected between the input voltage V_{in} and the ground, therefore its current I_{L1} increases. The time interval

t_1 to t_2 corresponds to the energizing phase in a basic buck converter if the output voltage V_{out} is lower than the input voltage V_{in}. It corresponds to the de-energizing phase of a basic boost converter if the output voltage V_{out} is higher than the input voltage V_{in}. This period subinterval is hereafter simply called *transfer phase*. The switches configuration of an energizing buck and a de-energizing boost is the same. The difference is that if V_{out} is lower than V_{in}, the inductor current I_{L1} increases, and if V_{out} is higher than V_{in}, the inductor current I_{L1} decreases. The time interval t_2 to t_3 corresponds to the *de-energizing phase* of a buck converter. During this phase, the inductor current I_{L1} decreases. The time interval t_3 to t_4 corresponds to the same configuration as the time interval t_1 to t_2.

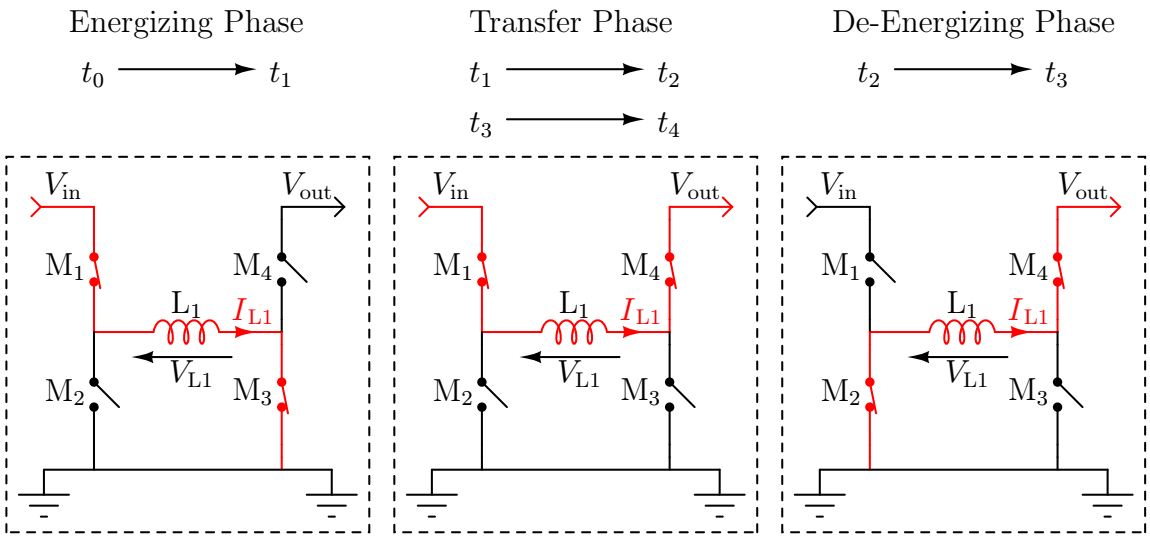

Figure 4.23: Successive switches configuration in the special buck-boost mode.

Since the inductor current I_{L1} is continuous, the following equations are obtained:

- from t_0 to t_1 the current variation in the inductor is expressed by:

$$\Delta I_{L1}(t_0, t_1) = \frac{1}{L_1} \cdot \int_{t_0}^{t_1} (V_{L1} \cdot dt) = \frac{1}{L_1} \cdot V_{in} \cdot (t_1 - t_0) \tag{4.23}$$

- from t_1 to t_2 the current variation in the inductor is expressed by:

$$\Delta I_{L1}(t_1, t_2) = \frac{1}{L_1} \cdot \int_{t_1}^{t_2} (V_{L1} \cdot dt) = \frac{1}{L_1} \cdot (V_{in} - V_{out}) \cdot (t_2 - t_1) \tag{4.24}$$

- from t_2 to t_3 the current variation in the inductor is expressed by:

$$\Delta I_{L1}(t_2, t_3) = \frac{1}{L_1} \cdot \int_{t_2}^{t_3} (V_{L1} \cdot dt) = \frac{1}{L_1} \cdot (-V_{out}) \cdot (t_3 - t_2) \tag{4.25}$$

- from t_3 to t_4 the current variation in the inductor is expressed by:

$$\Delta I_{L1}(t_3, t_4) = \frac{1}{L_1} \cdot \int_{t_3}^{t_4} (V_{L1} \cdot dt) = \frac{1}{L_1} \cdot (V_{in} - V_{out}) \cdot (t_4 - t_3) \tag{4.26}$$

In steady-state operation, the inductor current $I_{\mathrm{L1}}(t)$ is equal to $I_{\mathrm{L1}}(t_{\mathrm{sw}}+t)$, where t_{sw} is the period of the oscillator. Therefore, the following equation is satisfied:

$$\Delta I_{\mathrm{L1}}(t_0,t_1)+\Delta I_{\mathrm{L1}}(t_1,t_2)+\Delta I_{\mathrm{L1}}(t_2,t_3)+\Delta I_{\mathrm{L1}}(t_3,t_4)=0 \tag{4.27}$$

By developing Equation (4.27), it is obtained:

$$V_{\mathrm{in}}\cdot\Big((t_1-t_0)+(t_2-t_1)+(t_4-t_3)\Big)-V_{\mathrm{out}}\cdot\Big((t_2-t_1)+(t_3-t_2)+(t_4-t_3)\Big)=0 \tag{4.28}$$

Applying the definitions given in Equation (4.22) to Equation (4.28) gives:

$$V_{\mathrm{in}}\cdot\Big(t_{\mathrm{on(boost)}}+t_{\mathrm{sw}}-t_{\mathrm{off(buck)}})\Big)-V_{\mathrm{out}}\cdot(t_{\mathrm{sw}})=0 \tag{4.29}$$

By arranging Equation (4.29), the transfer function of the special buck-boost mode is:

$$M'_{\text{buck-boost}}=\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}=1+\frac{t_{\mathrm{on(boost)}}-t_{\mathrm{off(buck)}}}{t_{\mathrm{sw}}} \tag{4.30}$$

The time ranges $[t_1,t_2]$ and $[t_3,t_4]$ shown in Figure 4.22 when the special buck-boost mode is running can be expressed as:

$$(t_2-t_1)=(t_4-t_3)=\frac{t_{\mathrm{sw}}}{2}-\frac{t_{\mathrm{on(boost)}}}{2}-\frac{t_{\mathrm{off(buck)}}}{2} \tag{4.31}$$

The times (t_2-t_1) and (t_4-t_3) expressed in Equation (4.31) are linked to the voltages V_1, V_2, V_{shift1}, V_{shift2} in the following manner:

$$\left(\frac{t_{\mathrm{sw}}}{2}-\frac{t_{\mathrm{on(boost)}}}{2}-\frac{t_{\mathrm{off(buck)}}}{2}\right)\cdot\frac{V_2-V_1}{\frac{t_{\mathrm{sw}}}{2}}=V_{\mathrm{shift1}}+V_{\mathrm{shift2}} \tag{4.32}$$

By reordering Equation (4.32), it is obtained:

$$\frac{t_{\mathrm{sw}}-t_{\mathrm{on(boost)}}-t_{\mathrm{off(buck)}}}{t_{\mathrm{sw}}}=\frac{V_{\mathrm{shift1}}+V_{\mathrm{shift2}}}{V_2-V_1} \tag{4.33}$$

Concretely, Equation (4.33) shows that, if the pulses (i.e., logic **1**) on the digital PWM-BUCK output become wider, the pulses (i.e., logic **1**) on the digital PWM-BOOST output become narrower from the same amount of time (i.e., only $t_{\mathrm{on(boost)}}$ and $t_{\mathrm{off(buck)}}$ are not fixed by design). Therefore, the time during which both PWM-BUCK and PWM-BOOST signals are low remains constant. This means that the time intervals $[t_1,t_2]$ and $[t_3,t_4]$ shown in Figure 4.22 are independent of the control voltage V_{CI} when the special buck-boost mode is running. Additionally, like the method used for obtaining Equation (4.33), $t_{\mathrm{on(boost)}}$ and $t_{\mathrm{off(buck)}}$ can be written as:

$$\frac{V_2-V_1}{\frac{t_{\mathrm{sw}}}{2}}\cdot\frac{t_{\mathrm{on(boost)}}}{2}=V_{\mathrm{CI2}}-V_1\quad\Longrightarrow\quad\frac{t_{\mathrm{on(boost)}}}{t_{\mathrm{sw}}}=\frac{V_{\mathrm{CI2}}-V_1}{V_2-V_1} \tag{4.34}$$

$$\frac{V_2-V_1}{\frac{t_{\mathrm{sw}}}{2}}\cdot\frac{t_{\mathrm{off(buck)}}}{2}=V_2-V_{\mathrm{CI1}}\quad\Longrightarrow\quad\frac{t_{\mathrm{off(buck)}}}{t_{\mathrm{sw}}}=\frac{V_2-V_{\mathrm{CI1}}}{V_2-V_1} \tag{4.35}$$

The special buck-boost mode transfer function from Equation (4.30) can then also be written as a function of the internal control voltage V_{CI}:

$$M'_{\text{buck-boost}} = \frac{1}{V_2 - V_1} \cdot \Big(2 \cdot V_{\mathrm{CI}} + (V_{\text{shift1}} - V_{\text{shift2}}) - 2 \cdot V_1\Big) \tag{4.36}$$

By using Equation (4.15), the transfer function of the buck mode can also be written as a function of the control voltage V_{CI}:

$$M_{\text{buck}} = \frac{t_{\text{sw}} - t_{\text{off(buck)}}}{t_{\text{sw}}} = \frac{1}{V_2 - V_1} \cdot (V_{\mathrm{CI}} + V_{\text{shift1}} - V_1) \tag{4.37}$$

By using Equation (4.16), the transfer function of the boost mode can also be written as a function of the control voltage V_{CI}:

$$M_{\text{boost}} = \frac{t_{\text{sw}}}{t_{\text{sw}} - t_{\text{off(boost)}}} = \frac{V_2 - V_1}{V_2 + V_{\text{shift2}} - V_{\mathrm{CI}}} \tag{4.38}$$

Equation (4.36), Equation (4.37), and Equation (4.38) are only valid when the control voltage V_{CI} is in the corresponding interval, as listed in Table 4.2. The buck, buck-boost, and boost mode transfer functions M are plotted over the control voltage V_{CI} in Figure 4.24.

Table 4.2: Operating modes with their corresponding V_{CI} control voltage ranges.

Operating Mode	V_{CI1}	V_{CI2}	V_{CI}
Buck	$V_{\mathrm{CI1}} \geq V_1$	$V_{\mathrm{CI2}} < V_1$	$V_{\mathrm{CI}} \in [V_1 - V_{\text{shift1}}\ , V_1 + V_{\text{shift2}}]$
Buck-Boost	$V_{\mathrm{CI1}} \leq V_2$	$V_{\mathrm{CI2}} \geq V_1$	$V_{\mathrm{CI}} \in [V_1 + V_{\text{shift2}}\ , V_2 - V_{\text{shift1}}]$
Boost	$V_{\mathrm{CI1}} > V_2$	$V_{\mathrm{CI2}} < V_2$	$V_{\mathrm{CI}} \in [V_2 - V_{\text{shift1}}\ , V_2 + V_{\text{shift2}}]$

The transfer function M of the bidirectional DC-DC converter is made continuous over the three operating modes by defining the transition points A, B_1, and B_2 as shown in Figure 4.24. The location of these points is set up by V_{shift1} and V_{shift2}. Their coordinates are obtained by solving Equation (4.39) for V_{CI} at the point A (i.e., intersection between the buck and the buck-boost curve) and Equation (4.40) at the points B_1 and B_2 (i.e., intersections between the boost and the buck-boost curve):

$$\exists V_{\mathrm{CI}} = V_{\mathrm{A}} \in \mathbb{R}\ ,\ M'_{\text{buck-boost}}(V_{\mathrm{CI}}) = M_{\text{buck}}(V_{\mathrm{CI}}) \tag{4.39}$$

$$\exists V_{\mathrm{CI}} = V_{\mathrm{B1}} \in \mathbb{R} \text{ and } \exists V_{\mathrm{CI}} = V_{\mathrm{B2}} \in \mathbb{R}\ ,\ M'_{\text{buck-boost}}(V_{\mathrm{CI}}) = M_{\text{boost}}(V_{\mathrm{CI}}) \tag{4.40}$$

By solving Equation (4.39), the abscise V_{A} of the intersection point A (refer to Figure 4.24) between the buck and the buck-boost curves is given by:

$$V_{\mathrm{CI}} = V_{\mathrm{A}} = V_1 + V_{\text{shift2}} \tag{4.41}$$

By solving Equation (4.40), the abscises V_{B1} and V_{B2} of the intersection points B_1 and B_2 between the buck-boost and the boost curves are given by:

$$V_{\mathrm{B1}} = \frac{1}{4} \cdot \Big(2 \cdot (V_1 + V_2) - V_{\text{shift1}} + 3 \cdot V_{\text{shift2}} - \sqrt{\Delta}\Big) \tag{4.42}$$

$$V_{\mathrm{B2}} = \frac{1}{4} \cdot \Big(2 \cdot (V_1 + V_2) - V_{\text{shift1}} + 3 \cdot V_{\text{shift2}} + \sqrt{\Delta}\Big) \tag{4.43}$$

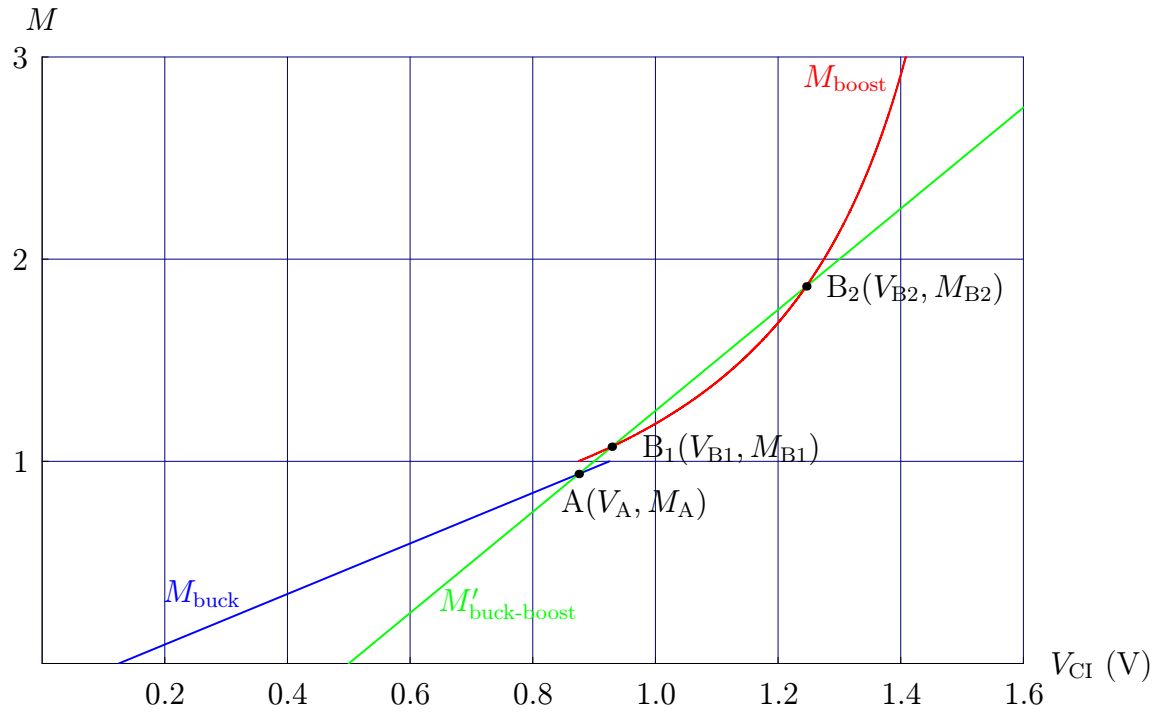

Figure 4.24: Buck, boost and special buck-boost transfer functions. To plot these curves, V_{shift1} and V_{shift2} were both taken equal to 350 mV.

where Δ is the discriminant expressed by:

$$\Delta = (V_{shift1} + V_{shift2})^2 + 4 \cdot (V_2 - V_1) \cdot (V_{shift1} + V_{shift2}) - 4 \cdot (V_2 - V_1)^2 \tag{4.44}$$

Actually, the point B_2 is a mathematical but not a physical solution for the transfer function of the IPC. The IPC operates in the buck mode when the control voltage V_{CI} is below V_A. It operates in the buck-boost mode when V_{CI} is comprised between V_A and V_{B1}. It operates in the boost mode when V_{CI} is above V_{B1}. This can be graphically observed in Figure 4.22.

Mathematically, it is interesting to notice that it exists a relation between V_{shift1} and V_{shift2} so that the points B_1 and B_2 are superposed. This point, noted B, has the abscise V_B and is the unique intersection between the buck-boost and boost curves in Figure 4.24:

$$\exists V_B \in \mathbb{R} \ , \ V_B = V_{B1} = V_{B2} \iff \Delta = 0 \tag{4.45}$$

By solving the Equation (4.45) for Δ, two real solutions are obtained for V_{shift1} in Equation (4.46) and Equation (4.47):

$$V_{shift1} = 2 \cdot (V_1 - V_2) - V_{shift2} - \sqrt{\Delta_{shift}} \tag{4.46}$$

$$V_{shift1} = 2 \cdot (V_1 - V_2) - V_{shift2} + \sqrt{\Delta_{shift}} \tag{4.47}$$

where Δ_{shift} is the discriminant expressed by:

$$\sqrt{\Delta_{shift}} = 2 \cdot \sqrt{2} \cdot (V_2 - V_1) \tag{4.48}$$

The solution proposed in Equation (4.46) is always negative, since the shift voltages are taken positive as supposed previously in the hypotheses, and because V_2 is higher

than V_1. Finally, the only possible solution is given in Equation (4.47). However, there is no practical advantage of choosing V_{shift1} and V_{shift2} so that the points B_1 and B_2 superpose to a single point B. On the contrary, choosing V_{shift1} and V_{shift2} so that the point B is unique could lead to no intersection in practice between the buck-boost and the boost curves (for example, because of comparator's offset). In this case, the transfer function M would show a discontinuity, which would avoid the regulation loop to operate properly at the crossover control voltage between buck-boost and boost mode given in Table 4.2 as:

$$V_{\text{CI}} = V_2 - V_{\text{shift1}} \tag{4.49}$$

It is therefore useful to determine the minimum values for V_{shift1} and V_{shift2} so that an intersection between the buck-boost and the boost mode curves is ensured. When V_{shift1} is taken equal to V_{shift2} for solving Equation (4.47), the shift voltage value for V_{shift} below which the buck-boost and the boost curves have no intersection point is given by:

$$V_{\text{shift}} = V_{\text{shift1}} = V_{\text{shift2}} = (V_2 - V_1) \cdot (\sqrt{2} - 1) \tag{4.50}$$

The shift voltages V_{shift1} and V_{shift2} are realized practically by voltage shifters (see Section 5.1.3.2 for more details). Using equal values for V_{shift1} and V_{shift2} is not mandatory. However, matched shift voltages are easier to provide than absolute voltage values which are inaccurately controlled in integrated circuit design. In other words, the exact value of V_{shift1} is hard to control in integrated circuit, but it is easy to reproduce V_{shift1} for generating V_{shift2} when both V_{shift1} and V_{shift2} have the same voltage value V_{shift}. In the chosen UMC technology, the low-V_{th} transistors have a threshold voltage around 300 mV. Since the amplitude of the oscillator voltage is 800 mV ($V_2 - V_1 = 1.3 - 0.5 = 0.8$ V), the voltage shift done by each voltage shifter must be strictly lower than 400 mV, so that an overlap between the buck and boost region is ensured. By evaluating numerically Equation (4.50), the minimum shift voltage ensuring an intersection point between the buck-boost and the boost transfer function is obtained for a V_{shift} voltage of 332 mV. Finally, V_{shift} must satisfy:

$$332\,\text{mV} < V_{\text{shift}} < 400\,\text{mV} \tag{4.51}$$

The values of the parameters used for designing the bidirectional DC-DC converter are listed in Table 4.3. The complete transfer function M of the bidirectional DC-DC converter is shown in Figure 4.25. The junction points A and B_1 between the buck, buck-boost, and boost curves were determined by the method exposed previously.

Table 4.3: Continuous transfer function parameter values.

Parameter	V_1	V_2	V_{shift}	V_{A}	M_{A}	V_{B1}	M_{B1}
Value	0.5 V	1.3 V	0.350 V	0.850 V	0.875 V/V	0.972 V	1.180 V/V

Thanks to the symmetrical triangular waveform oscillator, this newly developed regulation method provides the advantage of avoiding the simultaneous turn on of the NMOS M_2 and M_3 in Figure 4.15 when the special buck-boost mode is used. The logic **1** pulses provided by the PWM-BUCK and PWM-BOOST signals are automatically centered, as shown in Figure 4.21. The timing separating these logic pulses are very well controlled by the design voltage parameters V_1, V_2 and V_{shift}. No additional logic is needed in the PWM logic unit shown in Figure 4.20, which simplifies the circuit design and improves the power efficiency of the bidirectional DC-DC converter.

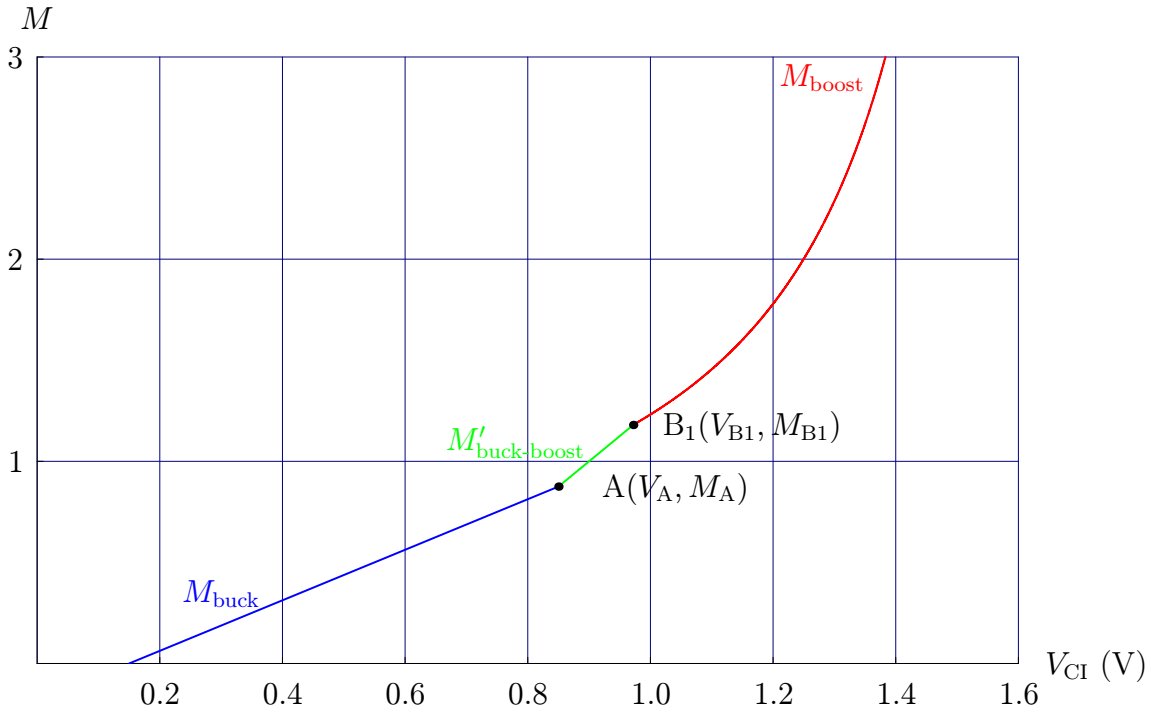

Figure 4.25: Continuous transfer function of the IPC. In the IPC, V_{shift1} and V_{shift2} were both taken equal to V_{shift} (i.e., 350 mV).

Chapter 5

Bidirectional DC-DC Converter Design

In this chapter, the CMOS design of the bidirectional DC-DC converter is presented. The schematics, the simulations, and the layouts are analyzed in detail. The design is based on the block diagram of the IPC shown in Figure 5.1. This chapter is divided into three parts, corresponding to the three electronic parts developed for the IPC: the analog part (see Section 5.1), the digital part (see Section 5.2), and the power electronic part (see Section 5.3). The combination of all these three electronic parts on a single silicon die was an asking challenge in terms of design and layout, because of electrical isolation, decoupling, and noise issues.

Two prototypes of the IPC were manufactured. The first prototype contains the H-bridge with the power MOSFET gate drivers adapted for performing dynamic MOSFET sizing. It integrates a simplified version of the internal core voltage power supply unit. No PWM regulation was integrated in this first prototype, which occupies a silicon die area of $1525 \times 1525\,\mu m$.

The design of the second prototype of the IPC, which is described in detail hereafter, uses twice the silicon area of the first prototype ($1525 \times 3240\,\mu m$) because it integrates an enhanced version of the core voltage power unit (see Section 5.1.1), an intelligent energy flow direction management unit (see Section 5.1.2), a PWM regulation unit (see Section 5.1.3), a current measurement unit (see Section 5.1.4), and a digital I^2C interface (see Section 5.2.4). Further, the layout of the power part was modified to allow switching frequencies up to 10 MHz (see Section 5.3.2 and Section 5.3.1) so that it becomes possible to use hybrid integrated power inductors processed on a silicon substrate. The dynamic MOSFET sizing function was not implemented in the second prototype, because of a lack in silicon die area. The bonding pad layout was redesigned to use wedge bonds for the power pads to avoid bond wire fusing during high current operation.

The schematics were all designed with the Cadence Virtuoso tool. The simulations were performed with the Cadence Spectre tool. Both tools are contained in the IC5141 package available through Europractice. Only simulation results are presented hereafter. The experimental results are presented in Chapter 6. The layout verification steps (DRC: Design Rules Check ; LVS: Layout Versus Schematic ; LPE: Layout Parasitics Extraction) were performed with the Cadence Assura tool contained in the ASSURA316 package.

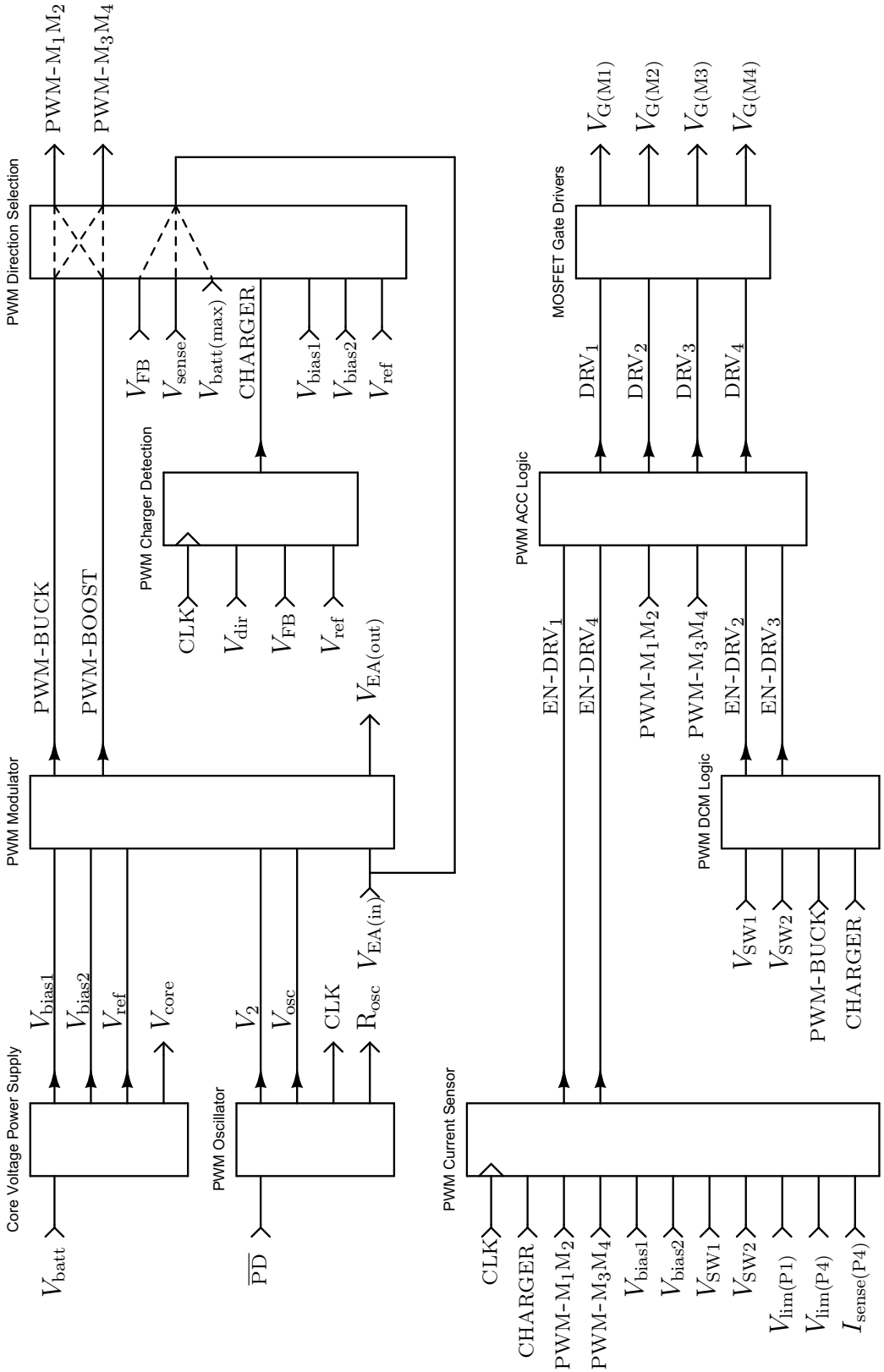

Figure 5.1: Detailed block diagram of the IPC. The digital I^2C test interface and the power H-bridge are not shown in this diagram.

5.1 Analog Part Design

In this section, the technical characteristics of each elementary analog unit constituting the IPC are presented. All these units are low power units, like comparators, operational amplifiers, voltage shifters, voltage references, or biasing circuits. The Cadence Spectre simulator was used to do the electrical simulations. Each unit is detailed in its own paragraph: unit description, global functions overview, electrical parameters, electrical schematics, simulation results and layout considerations. The block diagram of the analog part of the IPC is given in Figure 5.1. Most of the units can be powered down by the active low $\overline{\text{PD}}$ digital signal, even if this is not shown for each unit.

5.1.1 Core Voltage Power Supply Unit

The block diagram of the core voltage power supply unit is given in Figure 5.2. The role of this unit is to provide the regulated V_{core} voltage of 1.8 V to all the units operating at the core voltage (i.e., all the units which do not need to operate at the battery voltage V_{batt} nor the load voltage V_{load}). For most of the analog units contained in the IPC (e.g., comparators, operational amplifiers), such a regulated core voltage is needed to ensure constant and well defined performances.

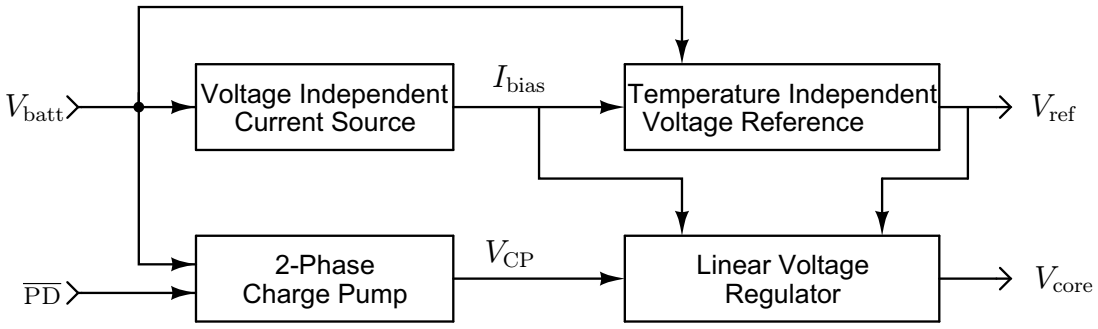

Figure 5.2: Block diagram of the core voltage power supply.

The voltage independent current source is powered by the battery voltage and provides a constant bias current I_{bias}. It is presented in Section 5.1.1.1. This constant current source is used to bias the temperature independent voltage reference described in Section 5.1.1.2 and which provides the reference voltage V_{ref} used by the linear voltage regulator and several other units of the IPC's block diagram shown in Figure 5.1. A 2-phase high-frequency fully integrated charge pump presented in Section 5.1.1.3 is activated through the power down $\overline{\text{PD}}$ digital signal when the battery voltage falls below 1.8 V. It provides a voltage V_{CP} that is the double of the input battery voltage V_{batt}. If the charge pump is powered down, its output voltage V_{CP} is equal to the battery voltage V_{batt}. The regulation of the core voltage V_{core} is performed by a linear voltage regulator, which is presented in Section 5.1.1.4.

5.1.1.1 Voltage Independent Current Source

In integrated analog circuit design, nearly each elementary cell (e.g., amplifier) needs current sinks or current sources. These are provided by a voltage independent biasing

circuit. In the IPC, this is done by the voltage independent current source shown in Figure 5.3. This current source is a modified high swing cascode version of the self-biased threshold voltage V_{th} referenced current source [70], [71]. Thanks to the self-biasing technique, the bias current dependence over the supply voltage is greatly reduced.

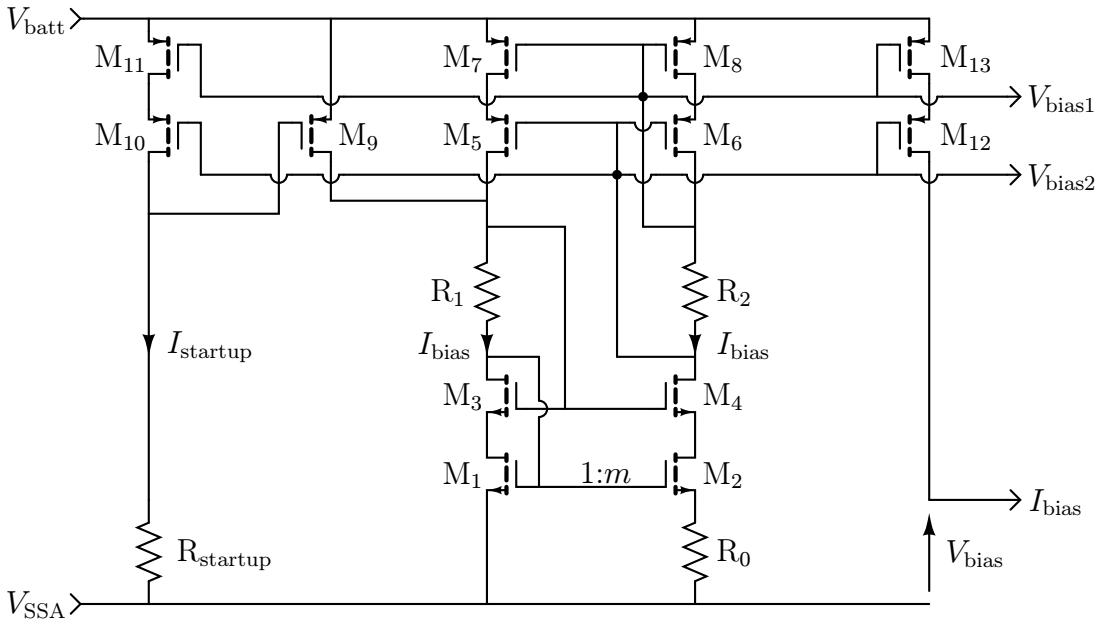

Figure 5.3: Schematic of the supply voltage independent high swing cascode current source used for the biasing of the analog units.

The principle of the self-biased current source consists in connecting a current source together with a current mirror. The drain currents of M_1 and M_2 are equaled by the cascode current mirror M_5, M_6, M_7 and M_8, so that:

$$I_{\text{D(M1)}} = I_{\text{D(M2)}} = I_{\text{bias}} \tag{5.1}$$

The transistors M_1 to M_8 are used in the saturation region. This means that the drain current $I_{\text{D(M}i\text{)}}$ through the transistor M_i is given by:

$$I_{\text{D(M}i\text{)}} = \frac{1}{2} \cdot \mu_n \cdot C_{\text{ox}} \cdot \left(\frac{W}{L}\right)_{\text{M}i} \cdot (V_{\text{GS(M}i\text{)}} - V_{\text{th}})^2 \tag{5.2}$$

where μ_n is the carrier mobility in the channel of the NMOS and C_{ox} the gate oxide capacitance per unit area. Equation (5.2) can be rewritten to:

$$V_{\text{GS(M}i\text{)}} = \sqrt{\frac{2 \cdot I_{\text{D(M}i\text{)}}}{\mu_n \cdot C_{\text{ox}}} \cdot \left(\frac{L}{W}\right)_{\text{M}i}} + V_{\text{th}} \tag{5.3}$$

The value of the current I_{bias} in Figure 5.3 is calculated as following:

$$V_{\text{GS(M1)}} = V_{\text{GS(M2)}} + R_0 \cdot I_{\text{D(M2)}} \tag{5.4}$$

$$\sqrt{\frac{2 \cdot I_{\text{D(M1)}}}{\mu_n \cdot C_{\text{ox}}} \cdot \left(\frac{L}{W}\right)_{\text{M1}}} + V_{\text{th}} = \sqrt{\frac{2 \cdot I_{\text{D(M2)}}}{\mu_n \cdot C_{\text{ox}}} \cdot \left(\frac{L}{W}\right)_{\text{M2}}} + V_{\text{th}} + R_0 \cdot I_{\text{D(M2)}} \tag{5.5}$$

The transistors M_1 and M_2 are designed so that:

$$\left(\frac{W}{L}\right)_{M2} = m \cdot \left(\frac{W}{L}\right)_{M1} \quad \text{with } m \in \mathbb{N} \text{ and } m \geq 2 \tag{5.6}$$

By combining Equations 5.1, 5.5 and 5.6, the bias current I_{bias} is given by:

$$I_{bias} = \frac{2}{\mu_n \cdot C_{ox}} \cdot \left(\frac{L}{W}\right)_{M1} \cdot \left[\frac{1}{R_0} \cdot \left(1 - \frac{1}{\sqrt{m}}\right)\right]^2 \tag{5.7}$$

In this bias current source topology, huge resistance values for R_0 are not mandatory for generating low bias currents. In the IPC, R_0 was taken equal to 8 kΩ to generate a bias current I_{bias} of approximately 3 µA. The resistance values of the resistors R_1 and R_2 are not critical, since they are only used to ensure that the transistors M_1–M_8 are biased into their saturation region. In the IPC, R_1 and R_2 are taken equal to 80 kΩ, and the gain factor m is taken equal to 2.

A drawback of self-biased current sources is the presence of two stable operating points [70], [71]. One is located at the desired bias current, and the other at the origin (i.e., at $I_{bias} = 0$). Since the gain at the origin is very low, it is generally too low to ensure a proper startup of the current source. Therefore, the startup circuit (i.e., $R_{startup}$, M_9, M_{10}, M_{11}) shown in Figure 5.3 is mandatory. It consumes 3 µA of current.

Simulations were performed with the circuit presented in Figure 5.3. The dependence of the bias current I_{bias} versus the supply voltage V_{batt} is shown in Figure 5.4. The current source starts with a supply voltage below 1.0 V, and the bias current is maintained constant up to the maximum safe supply voltage of this technology (i.e., 3.6 V). The horizontality of the current curve is obtained by the cascode stage.

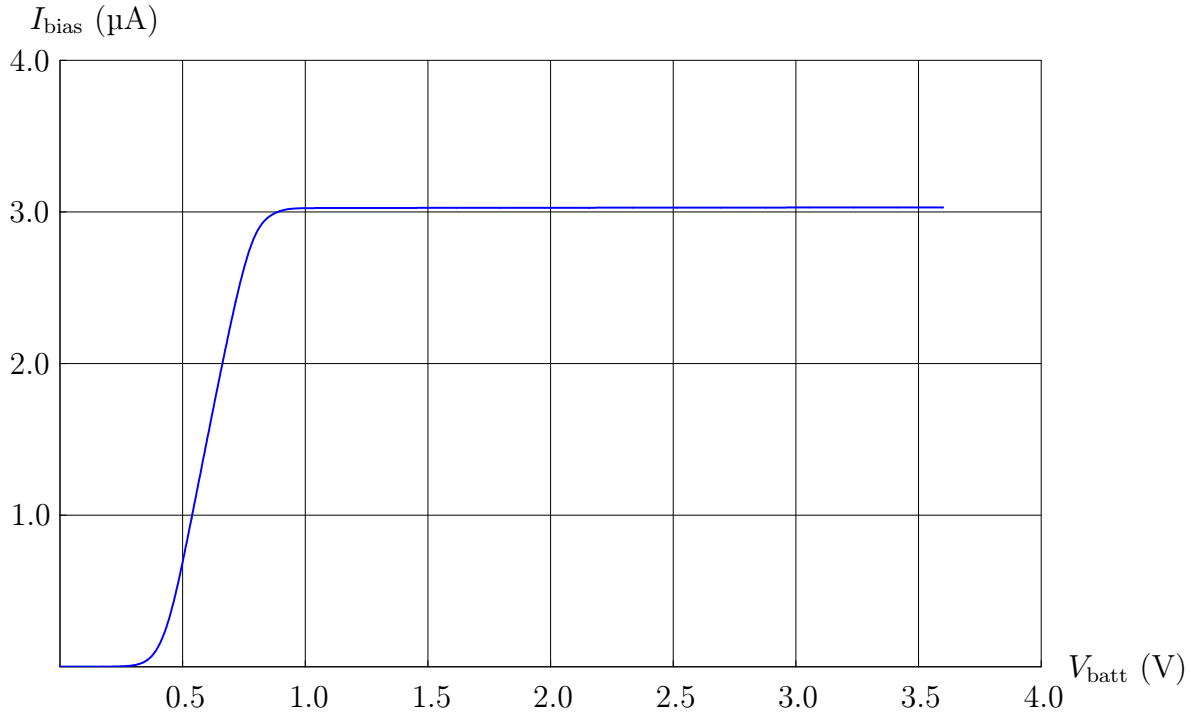

Figure 5.4: Bias current I_{bias} plotted versus the supply voltage V_{batt}.

In the simulation results plotted in Figure 5.5, the current source was supplied by a constant 2.3 V battery voltage. It is shown that the current source performs like an ideal current source up to a bias voltage V_{bias} that is only 200 mV below the battery voltage. This high swing performance is enabled by the two bias resistors R_1 and R_2.

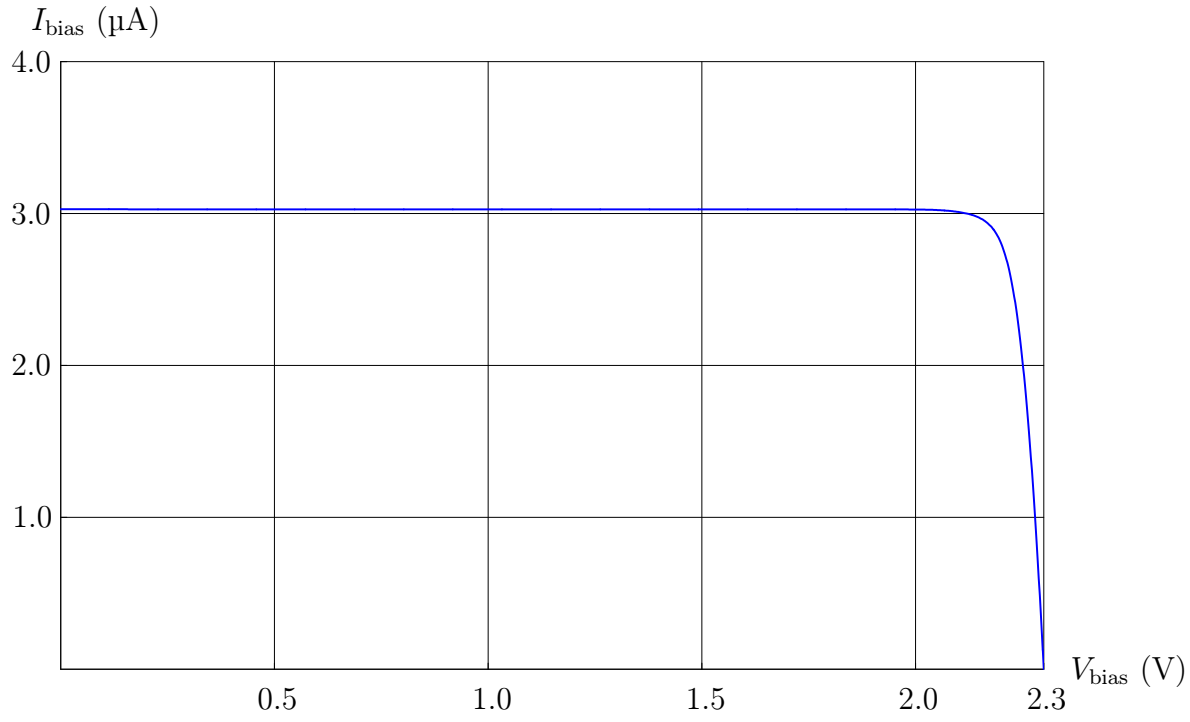

Figure 5.5: Bias current I_{bias} plotted versus the bias voltage V_{bias} at a V_{batt} of 2.3 V.

5.1.1.2 Temperature Independent Voltage Reference

The temperature and supply-voltage independent voltage reference circuit shown in Figure 5.6 is a base block for the IPC. It is used in the linear core voltage regulator (see Section 5.1.1.4), and in the PWM unit for the regulation loop (see Section 5.1.3). It provides a nominal reference voltage V_{ref} of 520 mV as illustrated by the simulation results shown in Figure 5.7 and in Figure 5.8.

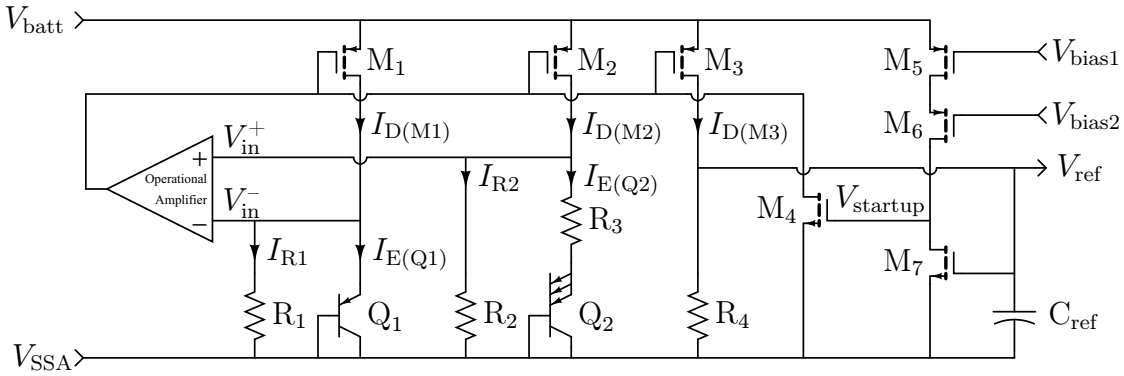

Figure 5.6: Schematic of the 520 mV voltage reference.

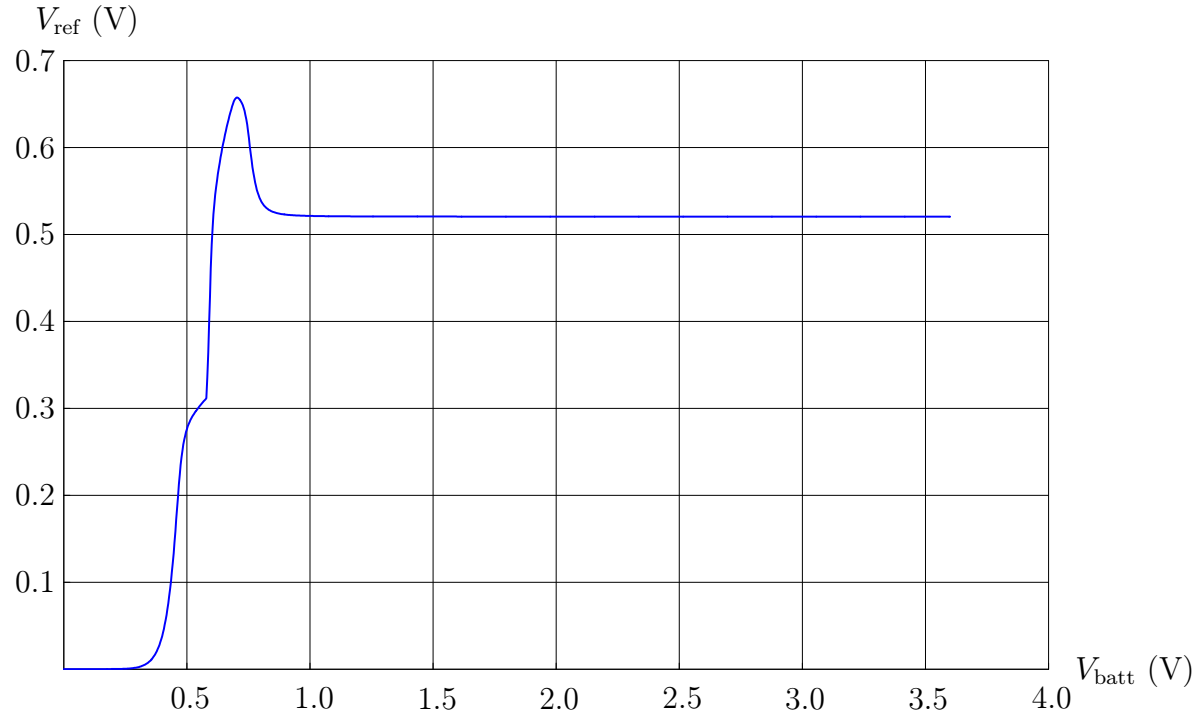

Figure 5.7: Reference voltage versus supply voltage at a temperature of 27°C.

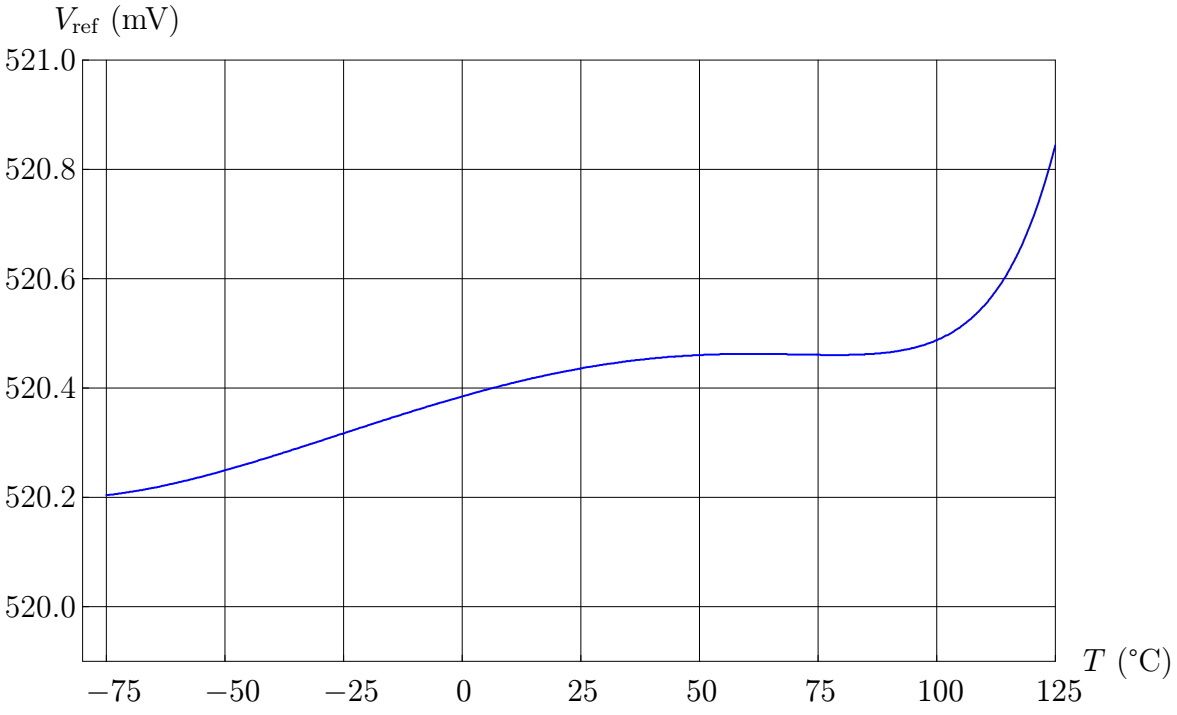

Figure 5.8: Reference voltage versus temperature when supplied by a 2.3 V voltage.

In the first prototype of the IPC (IPC1), the voltage reference was designed on the principle developed by K. Leung based on the weighted difference of gate-source voltages between PMOS and NMOS transistors [72]. However, the measurements on

this first prototype have shown an important process variations dependency. The reference voltages measured experimentally were spread between 350 mV and 600 mV. Therefore, it has been decided to change the topology used for the voltage reference and to switch to a less process dependent one. In the second prototype of the IPC, the implemented voltage reference is based on a current-mode bandgap voltage reference topology [73], [74], [75], [76]. The developed circuit, which is shown in Figure 5.6, is based on the principle described by H. Banba [73]. To quantify the effect of the process variations to the value of the reference voltage, Monte-Carlo simulation models of the process variations have been developed. Simulation results taking into account the process variations are illustrated in Figure 5.9. The theoretical reference voltage V_{ref} is now spread between 517 mV and 524 mV with the circuit shown in Figure 5.6.

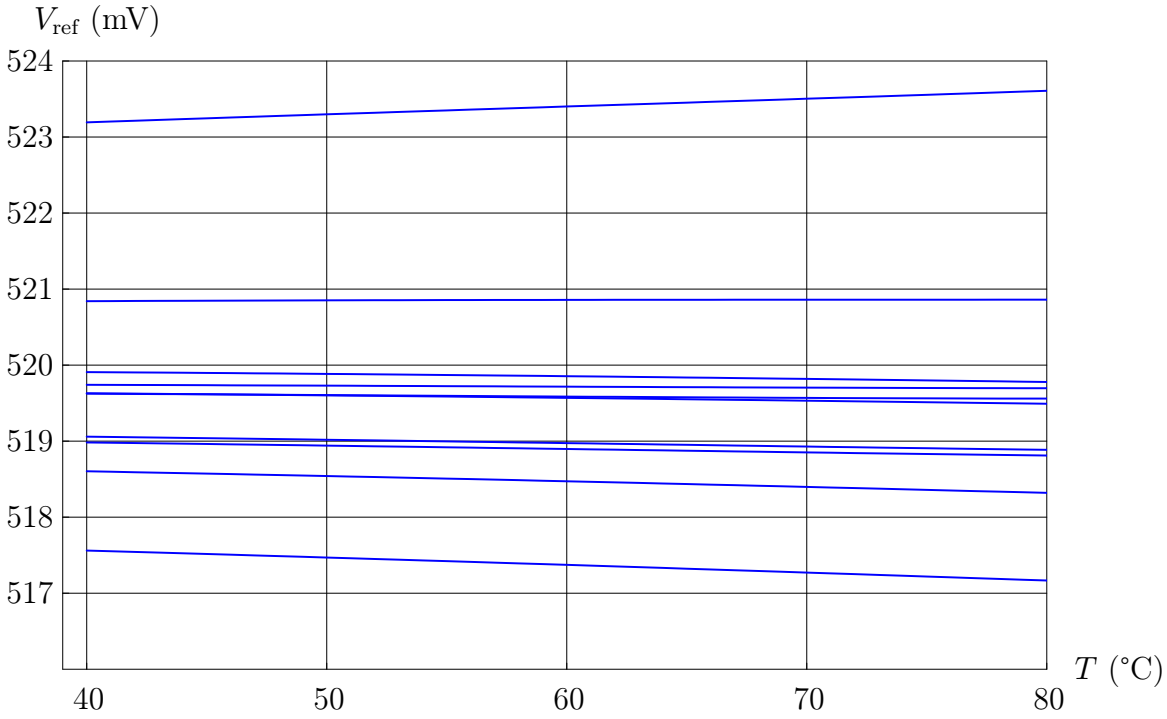

Figure 5.9: Monte-Carlo simulations of the voltage reference (V_{ref} vs. T).

In the designed voltage reference circuit shown in Figure 5.6, it is ensured by design that M_1, M_2, M_3 have equal sizes and that they are well matched transistors in the layout [77]. Since their gates are driven by the same gate-source voltage V_{GS}, the drain currents across them are equal:

$$I_{\text{D(M1)}} = I_{\text{D(M2)}} = I_{\text{D(M3)}} = I_{\text{D}} \tag{5.8}$$

The *pnp* transistor Q_2 is build by using m transistors Q_1 connected in parallel ($m \in \mathbb{N}$ and $m \geq 2$). The resistors R_1 and R_2 have the same resistance. The resistors R_1, R_2 and R_4 are laid out so that their ratio to R_3 permits to ensure good matching:

$$\begin{cases} R_1 = R_2 = m' \cdot R_3 \\ R_4 = m'' \cdot R_3 \end{cases} \quad \text{with } \{m', m''\} \in \mathbb{N}^* \tag{5.9}$$

Further, the operational amplifier in Figure 5.6 is considered to operate in the linear region and therefore tends to equalize the voltages provided at its inputs V_{in}^-

and V_{in}^{+}. In consequence of these hypotheses, the following relations are verified:

$$V_{\text{in}}^{+} = V_{\text{in}}^{-} \Longrightarrow I_{\text{R1}} = I_{\text{R2}} \tag{5.10}$$

$$I_{\text{E(Q1)}} = I_{\text{E(Q2)}} \tag{5.11}$$

The Ebers-Moll expression of the emitter current in a bipolar transistor Q_i is [78]:

$$I_{\text{E(Q}i\text{)}} = \frac{I_{\text{S(Q}i\text{)}}}{\alpha_{\text{F(Q}i\text{)}}} \cdot \left(e^{\frac{V_{\text{BE(Q}i\text{)}}}{V_{\text{T}}}} - 1 \right) - I_{\text{S(Q}i\text{)}} \cdot \left(e^{\frac{V_{\text{BC(Q}i\text{)}}}{V_{\text{T}}}} - 1 \right) \tag{5.12}$$

where $I_{\text{E(Q}i\text{)}}$ is the emitter current in the bipolar transistor transistor Q_i, $I_{\text{S(Q}i\text{)}}$ is the transport saturation current, $\alpha_{\text{F(Q}i\text{)}}$ is the large-signal forward current gain of the common base configuration, $V_{\text{BE(Q}i\text{)}}$ is the base-emitter voltage, $V_{\text{BC(Q}i\text{)}}$ is the base-collector voltage, and V_{T} is the thermal voltage given by:

$$V_{\text{T}} = \frac{k \cdot T}{q} \tag{5.13}$$

where k is the Boltzman constant ($1.38 \cdot 10^{-23}\,\text{J/K}$), T is the temperature in Kelvin, and q is the absolute value of the charge of an electron ($1.60 \cdot 10^{-19}\,\text{C}$). By the way, in the designed voltage reference circuit, the bipolar transistors Q_1 and Q_2 are operated in the forward active region, which is roughly characterized by $0.98 < \alpha_{\text{F(Q}i\text{)}} < 0.998$, $V_{\text{BE(Q}i\text{)}} \geq 0.5\,\text{V}$ and $V_{\text{BC(Q}i\text{)}} = 0\,\text{V}$. Under these assumptions, the Ebers-Moll model given in Equation (5.12) can be simplified to:

$$I_{\text{E(Q}i\text{)}} \approx I_{\text{S(Q}i\text{)}} \cdot e^{\frac{V_{\text{BE(Q}i\text{)}}}{V_{\text{T}}}} \tag{5.14}$$

Since the transport saturation current I_{S} of a bipolar transistor is proportional to its emitter-base junction area [70], and since the emitter-base junction area of Q_2 is equal to m times the emitter-base junction area of Q_1, Equation (5.14) injected in Equation (5.11) leads to:

$$I_{\text{S(Q1)}} \cdot e^{\frac{V_{\text{BE(Q1)}}}{V_{\text{T}}}} = m \cdot I_{\text{S(Q1)}} \cdot e^{\frac{V_{\text{BE(Q2)}}}{V_{\text{T}}}} \tag{5.15}$$

By taking the logarithm of Equation (5.15), it can be written:

$$V_{\text{BE(Q1)}} - V_{\text{BE(Q2)}} = \ln(m) \cdot V_{\text{T}} \tag{5.16}$$

Additionally:

$$V_{\text{BE(Q1)}} = V_{\text{BE(Q2)}} + R_3 \cdot I_{\text{E(Q2)}} \Longrightarrow I_{\text{E(Q2)}} = \frac{\ln(m) \cdot V_{\text{T}}}{R_3} \tag{5.17}$$

Finally, the expression of the current I_{D} is:

$$I_{\text{D(M2)}} = I_{\text{E(Q2)}} + I_{\text{R2}} \Longrightarrow I_{\text{D}} = \frac{\ln(m) \cdot V_{\text{T}}}{R_3} + \frac{V_{\text{BE(Q1)}}}{R_1} \tag{5.18}$$

For the reference voltage to be temperature independent, the current $I_{\text{D(M3)}}$ (which is also equal to I_{D}) must be temperature independent, and the resistors must provide a low temperature dependency. In other words, I_{D} must satisfy:

$$\frac{d}{dT} I_{\text{D}} = \frac{d}{dT} \left(\underbrace{\frac{\ln(m)}{R_3} \cdot V_{\text{T}}(T)}_{\text{PTAT}} + \underbrace{\frac{1}{R_1} \cdot V_{\text{BE(Q1)}}(T)}_{\text{CTAT}} \right) = 0 \tag{5.19}$$

Equation (5.19) is the sum of a term *proportional to the absolute temperature* (PTAT) ($V_{\mathrm{T}}(T)$) and a term *conversely proportional to the absolute temperature* (CTAT) ($V_{\mathrm{BE(Q1)}}(T)$). In the literature, at 300 K, a usual value for the temperature coefficient of the thermal voltage V_{T} is +0.087 mV/K, whereas a usual value for the first order temperature coefficient of the base-emitter voltage $V_{\mathrm{BE}}(T)$ is −1.5 mV/K [79]. In the voltage reference presented in Figure 5.6 [73], only the first order variations in the base-emitter voltage is compensated. R_1, R_2, R_3 and m must be chosen in such a way that the temperature dependency of the current I_{D} is cancelled. R_4 is used only to define the value of the reference voltage V_{ref}.

In the simulation results in Figure 5.8, the voltage reference shows a temperature dependence of less than 3.5 ppm/°C between –75°C and +125°C when it is supplied with a battery voltage of 2.3 V. Further, in the simulation results shown in Figure 5.7, a supply voltage dependence (i.e., the reference voltage dependence over the battery voltage) of less than 285 ppm/V is shown. The resistance value used for R_1 is 700 kΩ, and the values used for $\{m', m''\}$ in the layout are $\{19, 8\}$ (see Equation (5.9)). The current consumed by the voltage reference circuit shown in Figure 5.6 is about 15 µA.

5.1.1.3 Integrated Charge Pump

The voltage doubler developed for the IPC is a 2-phase charge pump topology, which is driven by a 200 MHz clock [40]. This clock signal (i.e., CLOCK) is a square wave signal generated by a 3-stage ring oscillator composed of CMOS inverters. The schematic of the 3-stage ring oscillator with its output buffer is shown in Figure 5.10. The ring oscillator is only activated when the charge pump has to operate, which is the case when the battery voltage V_{batt} falls below 1.8 V. The amplitude of the clock voltage is equal to V_{core} (i.e., 1.8 V). The starting time of the ring oscillator is less than 5 ns and it consumes 45 µW of power at 200 MHz (i.e., 25 µA RMS current).

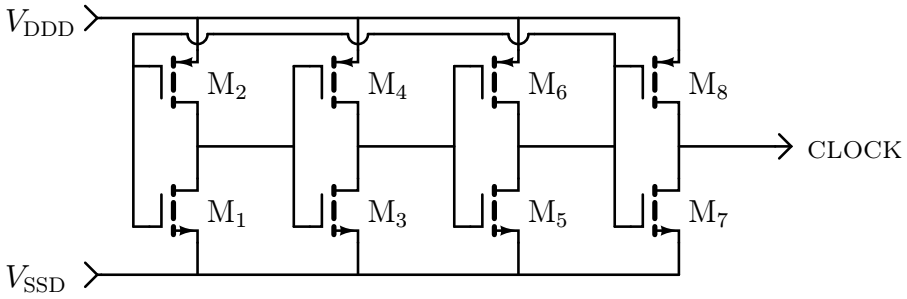

Figure 5.10: Schematic of the ring oscillator.

The schematic of the charge pump is given in Figure 5.11. The capacitors C_1 and C_2 are 2.5 pF metal-insulator-metal (MIM) capacitors with a 15 V breakdown voltage, which is much more than the 4.2 V oxide breakdown voltage of the 1.8 V regular-V_{th} MOSFETs used for the four switches M_1, M_2, M_3 and M_4. The topology described here was developed by R. Pelliconi *et al.* [40]. This topology requires the availability of isolated NMOS transistors for the switches M_1 and M_2. This is available in the UMC technology by using the NMOS transistors in triple-well.

When the charge pump is operating, the internal 1.8 V core voltage V_{core} can still be supplied to all the units of the IPC until the battery voltage falls below 1.3 V. Even at 1.3 V, the charge pump can provide a V_{CP} output voltage of more than 1.9 V when

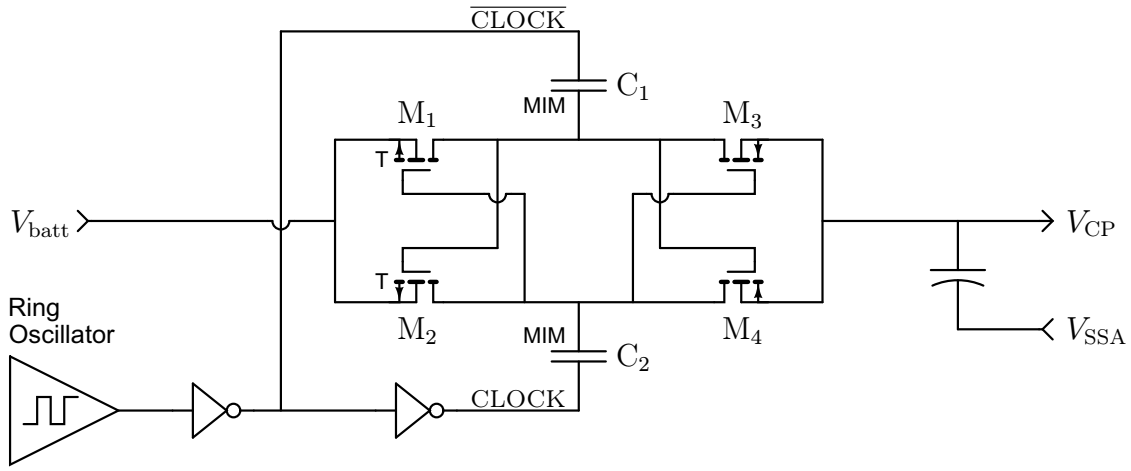

Figure 5.11: Schematic of the 2-phase charge pump.

supplying a load consuming 0.5 mA. In this worst case configuration, the efficiency of the charge pump still exceeds 68%. The simulation results obtained in such a situation are shown in Figure 5.12. These simulation results also show that after a startup condition given by the power down digital signal $\overline{\text{PD}}$, the charge pump is fully turned on after less than 100 ns.

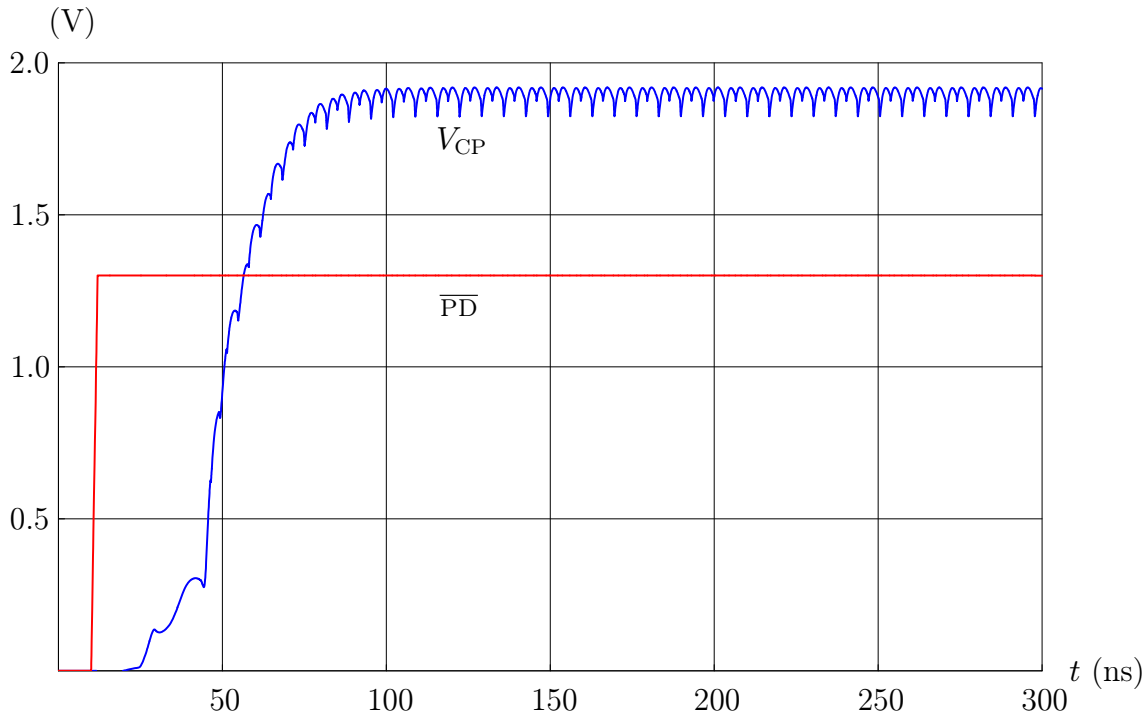

Figure 5.12: Simulation of the 2-phase charge pump supplied by a battery voltage V_{batt} of 1.3 V.

5.1.1.4 Linear Core Voltage Regulator

The analog units of the IPC need to be supplied by a regulated core voltage V_{core} because their performances are dependent of their supply voltage (i.e., V_{core}). In the used UMC technology, the nominal V_{core} voltage is 1.8 V. To ensure well defined and constant performances, the design of the analog units is optimized for operating at this core voltage, so that the circuits perform as they were designed and simulated.

To regulate the internal core voltage, several solutions were considered. One of them consisted in a switched capacitor regulator, but this solution was abandoned, because it generates too much noise. Another solution was a linear regulator with a high power supply rejection ratio (PSRR) [80]. A high PSRR is important, because when the power converter is switching, noise is superposed to the battery voltage V_{batt} supplying the linear regulator and transmitted to the sensitive analog units. Finally, the retained solution is a low dropout linear voltage regulator. The schematic of the circuit is shown in Figure 5.13 and the DC simulation results are shown in Figure 5.14.

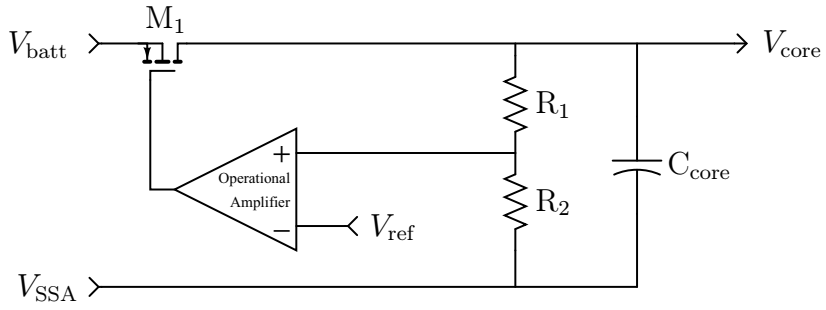

Figure 5.13: Schematic of the linear core voltage regulator.

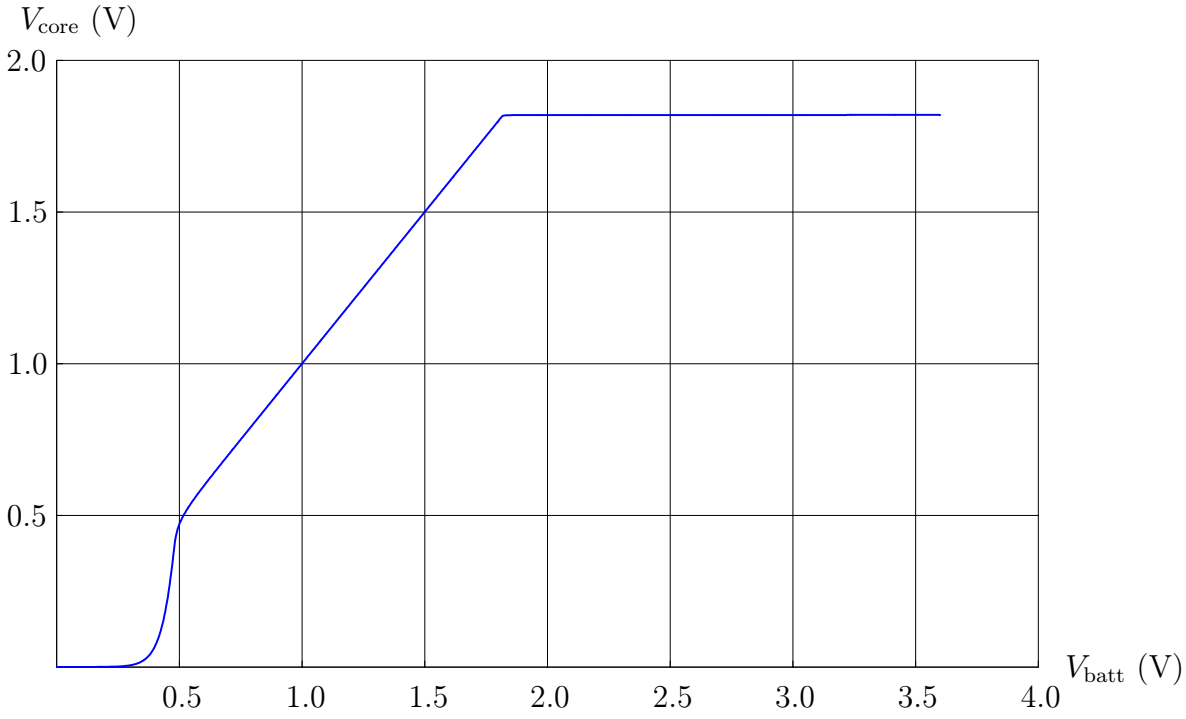

Figure 5.14: Voltage regulator output voltage (V_{core}) versus input voltage (V_{batt}).

The total current consumption of the IPC on the core voltage line is designed to be less than 1 mA. The simulated output voltage is approximately 1.827 V, as shown in Figure 5.14 and Figure 5.15. At this current, the pass device (PMOS transistor M_1 in Figure 5.13) provides a dropout around 30 mV. This pass device has been oversized to provide this low dropout and to be able to source up to 10 mA of continuous current, which is useful in case the IPC is switched at high PWM frequencies (e.g., 10 MHz). To simulate the transient response provided by the developed linear regulator, the load current was switched between 5 µA (i.e., current consumed on the V_{core} line when the IPC is in standby) and 500 µA (i.e., when the IPC is operating at a 1 MHz PWM frequency). The results of this simulation are shown in Figure 5.15. The MOS filter capacitor C_{core} shown in Figure 5.13 is constituted of multiple capacitors spread all over the IPC's analog units. The total C_{core} capacity is around 5 pF.

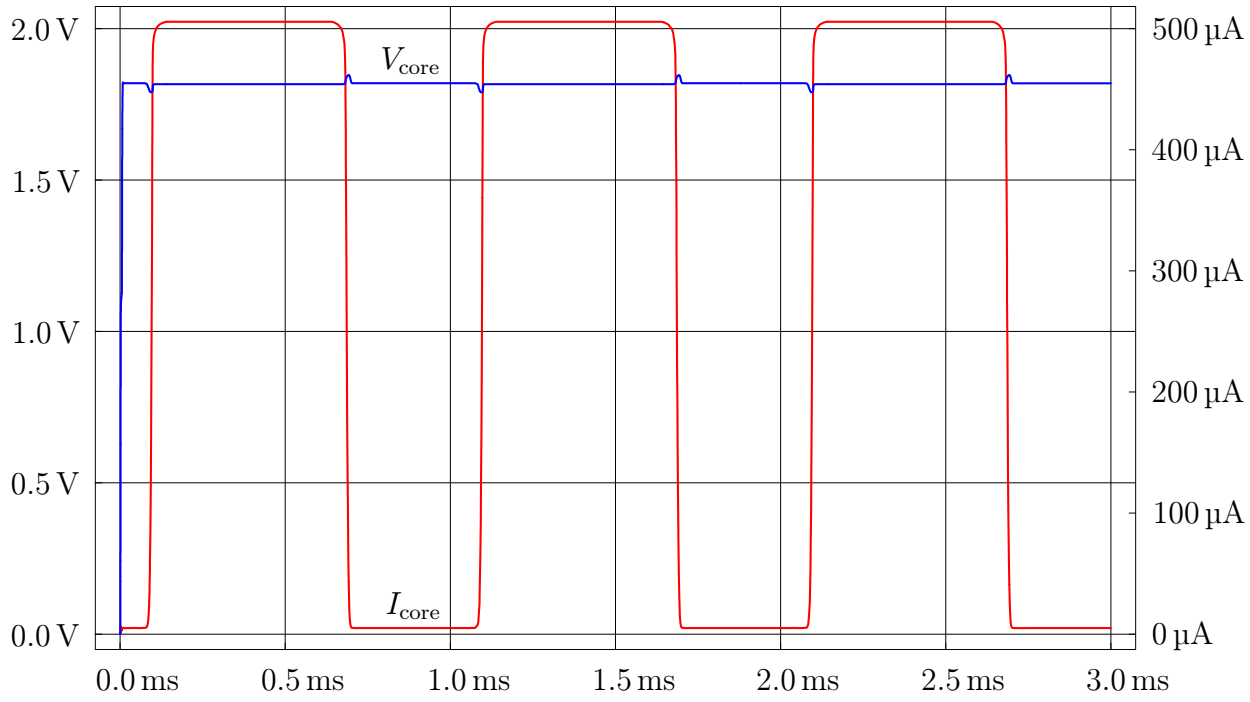

Figure 5.15: Transient simulation showing the variation in output core voltage V_{core} versus full range core current I_{core} steps (5 µA to 500 µA).

5.1.2 Energy Flow Direction Management Unit

The energy flow direction management unit performs the automatic detection of a battery charger and configures the internal control signals in such a way that they are usable by the pulse-width modulation unit described in Section 5.1.3.

5.1.2.1 Energy Flow Direction Detection

The automatic battery charger detection is performed by the circuit shown in Figure 5.16. The electrical connections to the IPC's environment were shown previously in Figure 4.1. The simulation results are shown in Figure 5.17.

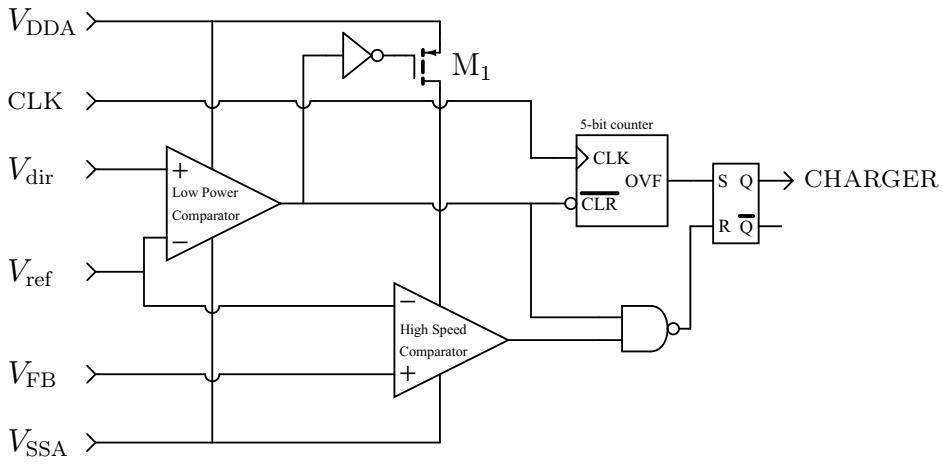

Figure 5.16: Schematic of the automatic charger detection unit used in the IPC.

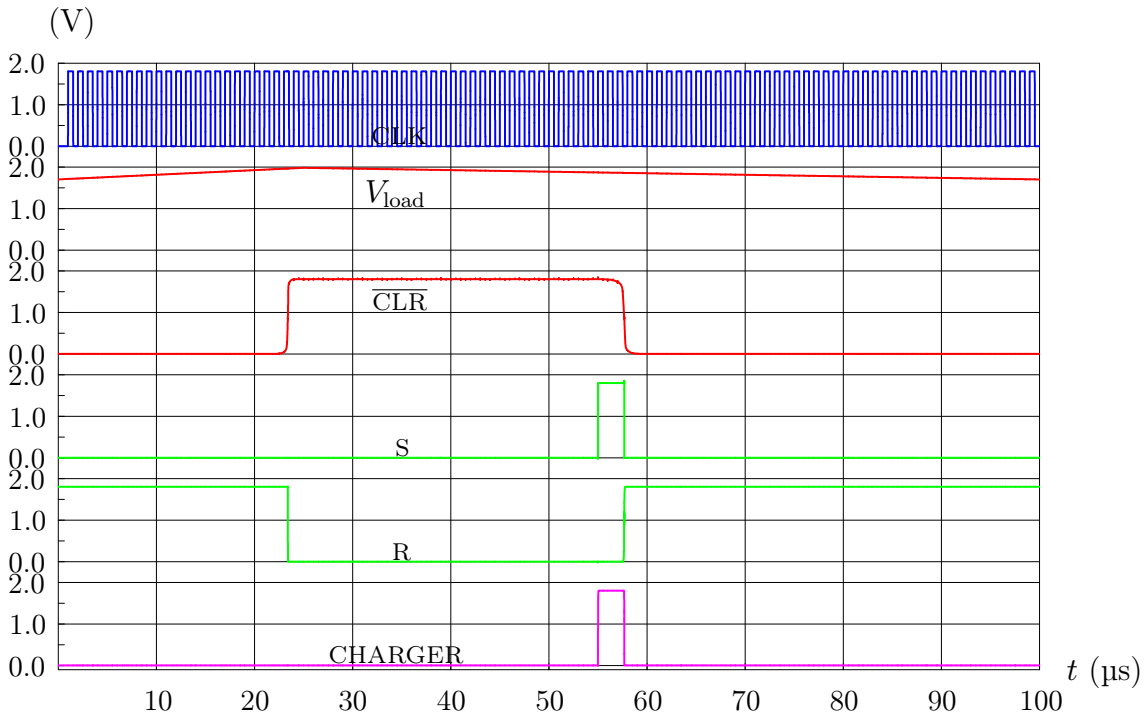

Figure 5.17: Simulation of the automatic charger detection circuit shown in Figure 5.16 and used in the IPC (see also Figure 4.1 for the external connections).

The operation principle of the circuit shown in Figure 5.16 is based on the monitoring of the V_{load} voltage (see Figure 4.1). When the V_{load} voltage is provided by the IPC, the direction detection voltage V_{dir} is below the reference voltage V_{ref}, thus the low power comparator clears the 5-bit counter shown in Figure 5.16 ($\overline{CLR}$ is an active low asynchronous clear signal) and the high speed comparator is powered down by the PMOS M_1. The RS flip-flop is therefore reseted and the digital CHARGER signal provides a logic **0**, thus indicating that no battery charger was detected.

When a battery charger is connected to the V_{load} side, it must provide a voltage that is high enough for V_{dir} to be above V_{ref}, thus the digital clear signal $\overline{CLR}$ goes high and the 5-bit counter begins to count at each rising clock edge. Simultaneously,

the high speed comparator is powered on though the PMOS M_1 shown in Figure 5.16. Since in this case the feedback voltage V_{FB} of the regulation loop is higher than the reference voltage V_{ref} (see Figure 4.1), the digital reset signal R is released from the RS flip-flop. After 32 clock pulses, the 5-bit counter overflows and the OVF signal goes high, setting the CHARGER signal to a logic **1**, thus indicating that a battery charger was detected. In case the charger is removed, the V_{dir} voltage falls below V_{ref} (see Figure 4.1), and the high speed comparator detects it in less than 10 ns. The high speed comparator consumes 16 µA, while the low power comparator consumes only 1.5 µA. This is the reason why the high speed comparator is powered down when no charger is connected. The low power comparator requires 1.5 µs to detect that the charger was removed, thus ensuring that the high speed comparator has switched before it is powered down. A complete sequence of a battery charger connection, detection and disconnection was simulated and the simulation results are shown in Figure 5.17.

5.1.2.2 Regulation Direction Setup

The regulation direction setup unit is the base for the bidirectional operation. The schematic of this unit is shown in in Figure 5.18. Its function is to route the right regulation signals (V_{FB}, V_{sense}, $V_{batt(max)}$) to the input of the error amplifier ($V_{EA(in)}$), and to route the right PWM switching signals (PWM-BUCK, PWM-BOOST) to the right power MOSFET gate drivers (PWM-M_1M_2, PWM-M_3M_4). The circuit has been designed in such a way that at any time, a single select signal is applied to each multiplexer (S1, S2, S3), thus the three output signals of the circuit are always defined.

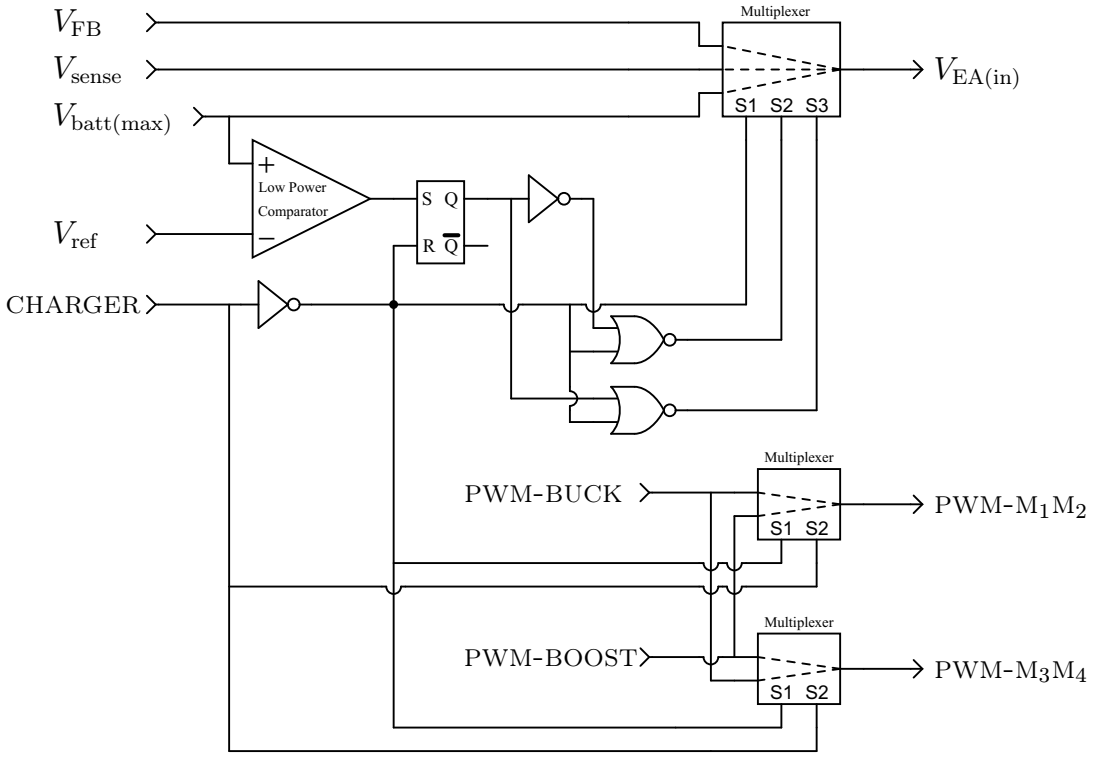

Figure 5.18: Schematic of the regulation direction setup unit used in the IPC to configure the PWM regulation unit depending on the energy flow direction.

The V_{FB} voltage is connected to $V_{EA(in)}$ when no charger has been detected (i.e., when the IPC is supplying the load). The V_{sense} voltage is connected to $V_{EA(in)}$ when a charger has been detected and the battery is being charged in constant current mode. Finally, the $V_{batt(max)}$ is connected to $V_{EA(in)}$ when a charger has been detected and the battery is being charged in constant voltage mode. All this is expressed by the three following relations:

$$V_{EA(in)} = \begin{cases} V_{FB} & \text{if CHARGER} = 0 \\ V_{sense} & \text{if CHARGER} = 1 \text{ and } V_{batt(max)} \text{ has not exceeded } V_{ref} \\ V_{batt(max)} & \text{if CHARGER} = 1 \text{ and } V_{batt(max)} \text{ has exceeded } V_{ref} \end{cases} \quad (5.20)$$

$$\text{PWM-M}_1\text{M}_2 = \text{PWM-BUCK} \cdot \overline{\text{CHARGER}} + \text{PWM-BOOST} \cdot \text{CHARGER} \quad (5.21)$$

$$\text{PWM-M}_3\text{M}_4 = \text{PWM-BUCK} \cdot \text{CHARGER} + \text{PWM-BOOST} \cdot \overline{\text{CHARGER}} \quad (5.22)$$

5.1.3 Pulse-Width Modulation Unit

The pulse-width modulation unit presented in the schematic in Figure 5.19 is the heart of the voltage regulation control of the IPC. It is constituted by an error amplifier with the corresponding compensated feedback loop providing the control signal V_{CI} for the voltage regulation (see Section 5.1.3.1), a dual voltage shifter limiting also the duty cycle in the boost conversion mode (see Section 5.1.3.2), a triangular waveform oscillator (not shown in Figure 5.19) providing the carrier V_{osc} (see Section 5.1.3.3), and finally two high speed comparators generating the PWM signals PWM-BUCK and PWM-BOOST (see Section 5.1.3.4).

The overlapping of the buck and boost regions (refer to Section 4.3 and Figure 4.17) is mandatory because of the fabrication process, which introduces mismatches between transistors in the layout. These mismatches produce offset voltages in the input stages of the high speed comparators, thus adding inaccurateness to the veritable area value of the crossover buck-boost region. In consequence, a precisely defined buck-boost region with an area reduced to zero cannot be ensured practically (i.e., this would lead practically to either a buck, boost and a small buck-boost region, or to two disjoined buck and boost regions). This means that it must be guaranteed by design that the overlapping of the buck and the boost region still exists after the manufacturing process. Further, since the duty cycle in this crossover buck-boost region is high for the buck comparator and low for the boost comparator (see Figure 4.20, Figure 4.21 and Figure 5.19), the width of the generated PWM-BUCK and PWM-BOOST pulses is a problem. Actually, it is practically possible to operate a buck converter with a duty cycle D equal to 100% (i.e., with the power transistor M_1 in the buck converter in Figure 2.6 always turned on). However, it is practically impossible to operate this same buck converter with a PWM frequency of 1 MHz at a duty cycle D of 99,999%, since the duration of the turn-off pulses delivered to the gate of the power transistor M_1 would be 0.1 ns. This signifies that, when defining the area of the overlapping buck-boost region shown in Figure 4.17, the width of the simultaneous buck and boost pulses delivered in this region must be carefully investigated, so that they can be practically generated by the power MOSFET gate drivers, and be executed by the

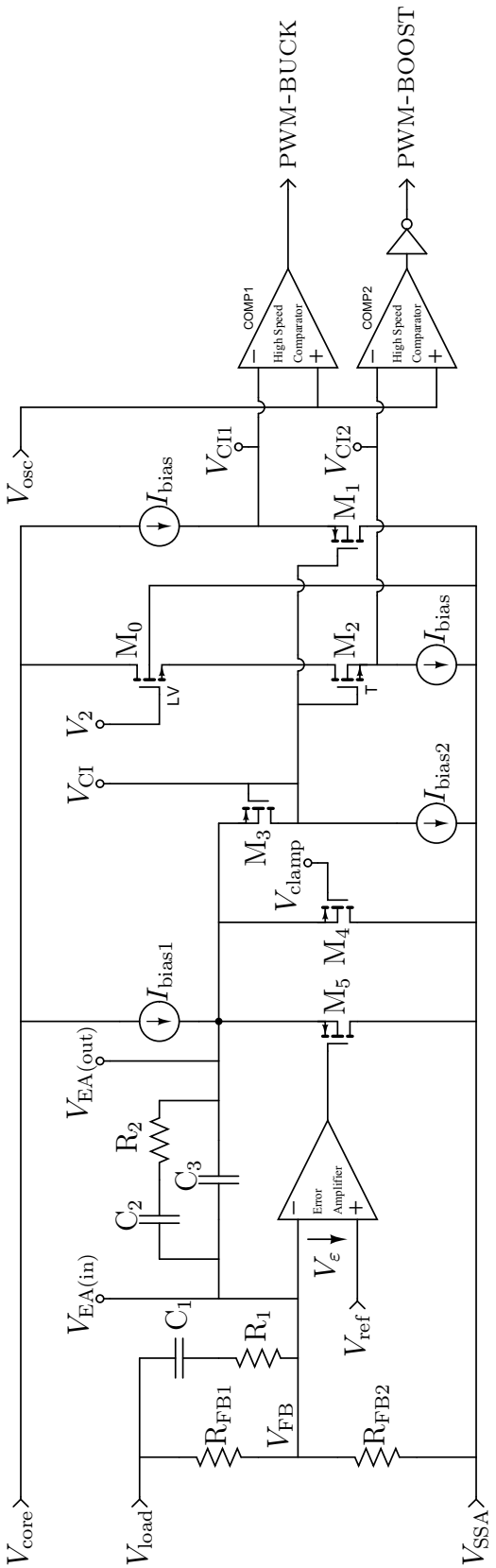

Figure 5.19: Schematic of the complete PWM regulator unit showing the continuous regulation loop. Note that the components in the feedback and compensation loop (R_{FB1}, R_{FB2}, R_1, R_2, C_1, C_2, C_3) are not integrated in the IPC, thus making it convenient for setting up the IPC for different target applications.

power transistor itself. If this is not done, the designed circuit may practically provide a buck-boost region, but its area will be too small and the width of the PWM-BUCK and PWM-BOOST pulses too narrow to make the power transistors switching.

In the PWM control scheme presented by B. Sahu *et al.* [66] and shown in Figure 5.20, only one of the two control signals V_{CI1} and V_{CI2} shown in Figure 5.19 is shifted. In other words, the signal $V_{\mathrm{EA(out)}}$ is directly connected to the noninverting input of the boost comparator (COMP2), while $V_{\mathrm{EA(out)}}$ is shifted up and connected to the inverting input of the buck comparator (COMP1). The triangular waveform oscillator is therefore connected to the noninverting input of the buck comparator (COMP1) and to the inverting input of the boost comparator (COMP2). However, these high speed comparators have parasitic capacitive retroaction. Depending of their architecture, they couple the noise generated by their output to their inputs (the output noise of the VCDA architecture used as high speed comparator in the IPC is mainly coupled to the noninverting input [81], [82]). This means that when the output is switching, the inputs see a part of the generated switching noise (see Section 5.1.3.4 for more details about the high speed comparators used in the IPC). Thus, two major weaknesses appear in the design proposed by B. Sahu *et al.* [66]:

- The first weakness is due to the fact that the control voltage $V_{\mathrm{EA(out)}}$ is directly provided to COMP2. When the output of COMP2 switches, it injects noise back into $V_{\mathrm{EA(out)}}$. In the worst case, this noise is shifted up and transmitted to COMP1 through V_{CI1}. At high switching frequencies (i.e., at high dV/dt), the injected noise amplitude can exceed 100 mV (observed in simulations, because of the gate-drain Miller capacity C_{GD} of the MOSFETs), which leads to operation failure since the oscillator waveform V_{osc} has an amplitude of only 800 mV (the digital signals PWM-BUCK and PWM-BOOST have an amplitude of 1.8 V).

- The second weakness is that the control signals (i.e., issued from $V_{\mathrm{EA(out)}}$) are connected to the inverting input of COMP1 and noninverting input of COMP2. Since the high speed comparators based on the VCDA architecture couple the generated output noise to the noninverting input, the design proposed by B. Sahu *et al.* [66] superposes noise to the control signal $V_{\mathrm{EA(out)}}$ and to the oscillator waveform V_{osc}, thus increasing the inaccurateness by unmatched noise balancing.

Due to both of these reasons, the control scheme proposed by B. Sahu *et al.* [66] is not a noise-robust design, thus it cannot be used for high frequency PWM DC-DC converters (i.e., operating at PWM frequencies above 1 MHz).

In the design of the IPC, these weaknesses were avoided from the very first. Therefore, in the control scheme that was developed in parallel to that of B. Sahu *et al.* [66], both high speed comparators have their noisy input (i.e., noninverting input) connected to the oscillator signal V_{osc} (see Figure 5.19). Hence, when one of the comparators is switching, the other comparator sees the same amount of noise at the V_{osc} side. The inverting side of the high speed comparators (VCDA topology, see Section 5.1.3.4) is nearly insensitive to the noise generated by the switching output. However, this configuration requires an additional inverter to be connected to the output of COMP2 (see Figure 5.19).

Additionally, in the IPC, two control signals V_{CI1} and V_{CI2} are generated by two voltage shifters (see Figure 4.20 and Figure 5.19). The principle of this voltage shifting

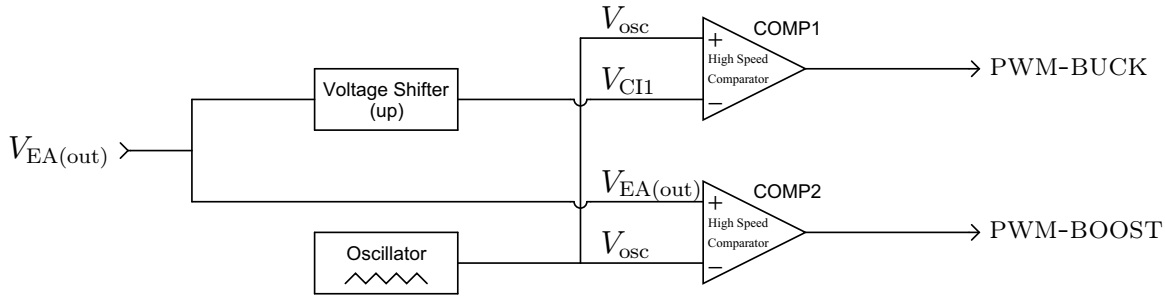

Figure 5.20: Implementation of the continuous regulation loop by B. Sahu *et al.* [66].

is presented in Section 5.1.3.2. There are mainly three advantages of this dual shifting method. The first advantage is that the same distortion is applied to both of the shifted control signals V_{CI1} and V_{CI2}, thus avoiding signal waveform mismatches (i.e., both signals have same bandwidth and same drive strength). The second advantage is that, due to the voltage shifting, the control signals V_{CI1} and V_{CI2} are essentially decoupled, thus avoiding noise to flow between V_{CI1} and V_{CI2}. In other words, no retroaction exists from V_{CI1} or V_{CI12} to V_{CI}, thus V_{CI1} is independent of V_{CI2}, and V_{CI2} is independent of V_{CI1}. Finally, the third advantage of this method is that the duty cycle D of the boost converter can be easily and precisely limited by using only one more transistor (see Section 5.1.3.2 for more details).

5.1.3.1 Error Amplifier

As stated in Section 2.3.2.1, the voltage mode regulation principle was chosen for designing the IPC. As shown in Figure 5.19, the load voltage V_{load} is sensed and fed back through the V_{FB} voltage to the inverting input of the error amplifier. This feedback voltage V_{FB} is then compared to the internal reference voltage V_{ref}, which is connected to the noninverting input of the error amplifier. The voltage difference (i.e., the error voltage V_{ε}) is then amplified and integrated by the error amplifier, since its feedback loop — constituted of R_2, C_2, C_3 — is capacitive (i.e., there is no DC path). The transistors M_3, M_4, M_5 and the current sources I_{bias1}, I_{bias2} have been implemented to allow the use of a soft-start circuit, which controls the V_{clamp} voltage. This soft-start circuit is not shown in Figure 5.19, but it has been implemented in the IPC. The startup speed (i.e., the amount of inrush current during startup) is adjustable externally by connecting a capacitor to the C_{SS} pin shown in Figure 5.46.

The transient response of a DC-DC converter is a function of both small signal and large signal responses. The small signal response is determined by the compensation network of the error amplifier (i.e., R_2, C_2, C_3). The large signal response is a function of the gain, bandwidth and slew rate of the error amplifier, as well as the inductance L_1 of the power inductor and the capacity C_{load} of the output filter capacitor. The circuit of the error amplifier designed for the IPC is shown in Figure 5.21. It is a self-compensating topology [84], [85] based on the low-voltage complementary folded cascode operational amplifier proposed by R. Roewer *et al.* [83]. The DC simulation results are shown in Figure 5.22. The open loop Bode plot of the transfer function of the error amplifier is illustrated in Figure 5.23. At a supply voltage of 1.8 V and with a 1 pF output load capacitor, the error amplifier provides a 50° phase margin at 6.7 MHz and consumes 45 µW of power (i.e., 25 µA of current).

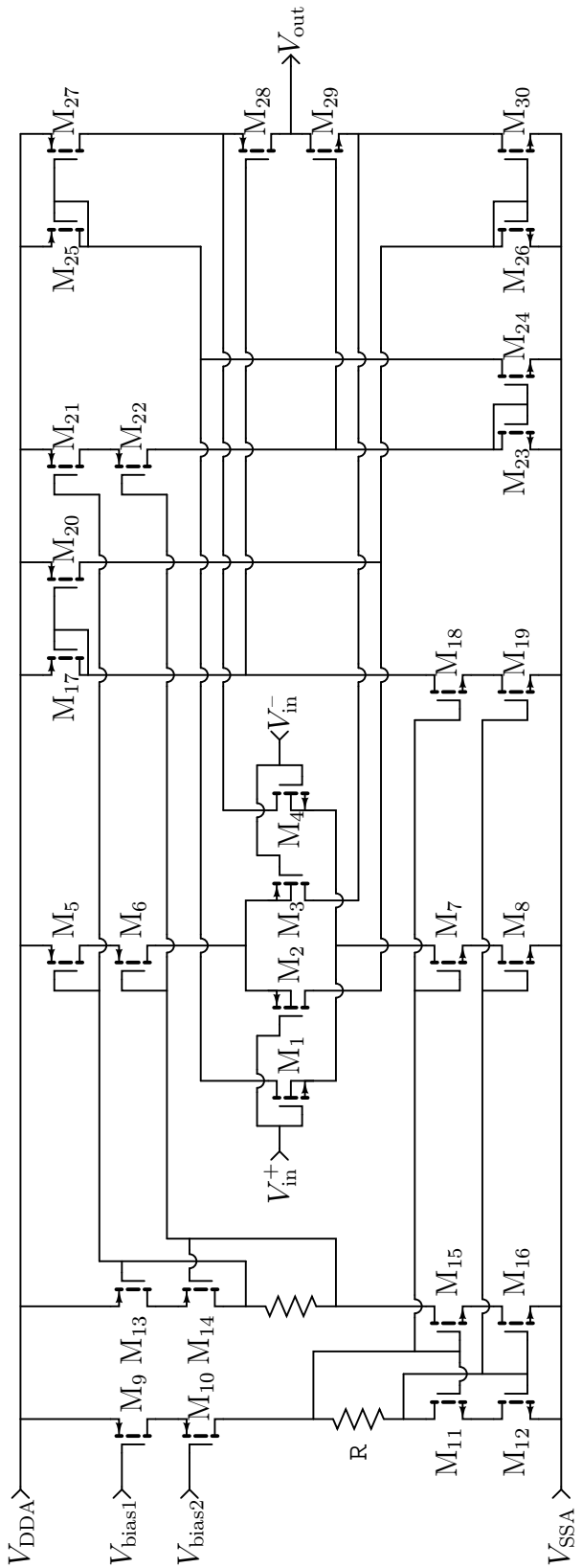

Figure 5.21: Schematic of the error amplifier implemented in the IPC. The architecture is based on the complementary folded cascode operational amplifiers for low supply voltage proposed by R. Roewer *et al.* [83].

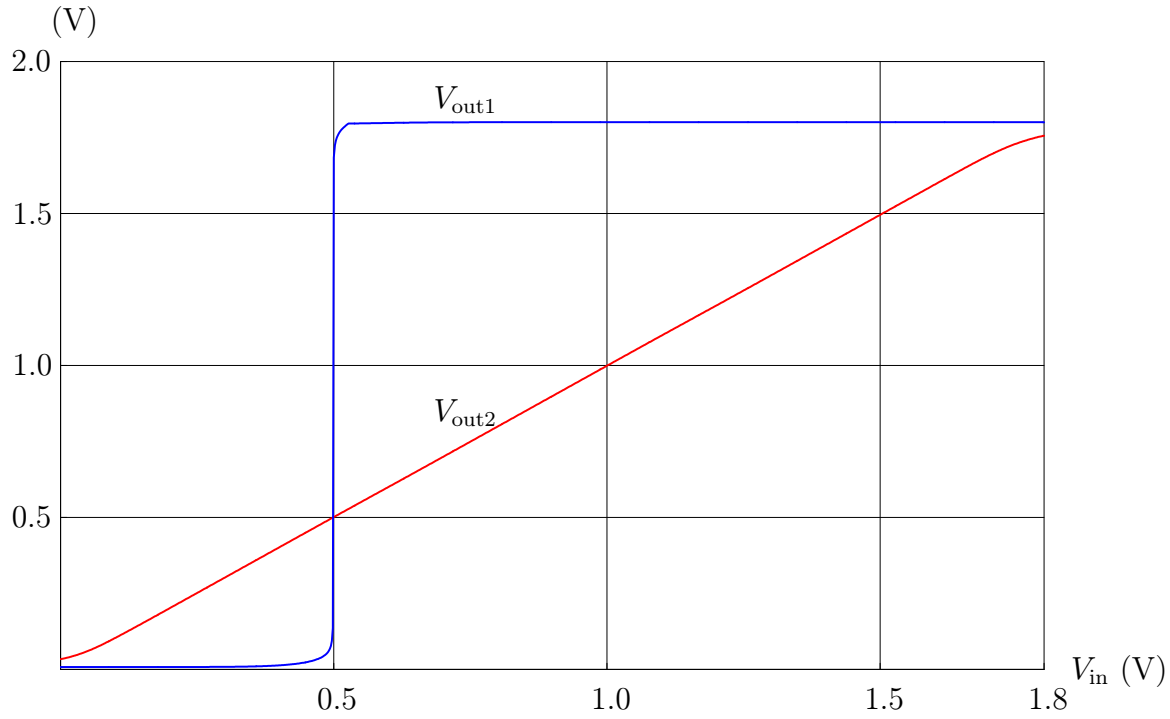

Figure 5.22: Simulation results obtained when the error amplifier is connected as a voltage comparator (V_{out1}) and as a voltage follower (V_{out2}). In both cases, the error amplifier supplied by the V_{core} voltage (i.e., 1.8 V).

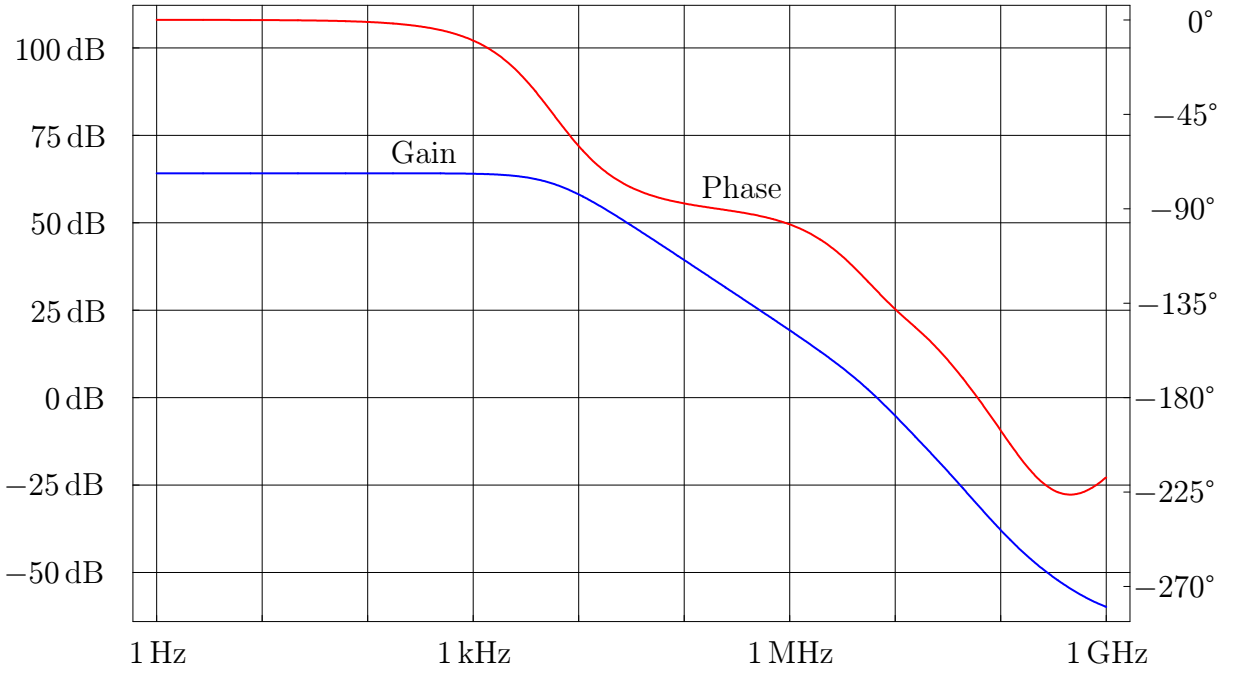

Figure 5.23: Open loop Bode plot of the error amplifier, when supplied by the V_{core} voltage of 1.8 V. With a 1 pF load capacitor, the phase margin is 50° at 6.7 MHz.

The voltage feedback loop — constituted of R_{FB1}, R_{FB2} in Figure 5.19 — must be compensated to provide stability margin, and to minimize the output voltage overshoot and undershoot response to line and load transients [86]. For the IPC, a *Type III* error amplifier compensation network is used. It is constituted of the devices R_1, R_2, C_1, C_2, C_3 (see Figure 5.19). This configuration has a pole at the origin and two zero-pole pairs, thus it can provide up to 180° of phase boost (in the literature [87], the used values for the phase margin ensuring the closed loop system is stable are in the interval [45°,60°]). The method for calculating the values of the components in the compensation loop is not provided in this thesis, but it can be easily found in the literature, since it is a popular compensation scheme [41], [88].

5.1.3.2 Voltage Shifter and Duty Cycle Limiter

The voltage shifting of the control voltage V_{CI} is performed by a source follower (common drain) transistor configuration [89], [90]. Figure 5.24 shows the schematic of the double voltage shifter implemented in the IPC. The PMOS M_1 is biased by a constant current source I_{bias}. The input voltage V_{CI} is directly connected to the gate of M_1 (i.e., high impedance input). The output is the voltage V_{CI1} provided at the source of M_1. The principle of a source follower circuit consists in an output voltage provided at the source that follows the gate voltage at the input. The body effect of the transistor M_1 has been cancelled, since its bulk is directly connected to its source. This is possible when an *n*-well CMOS process is used (see Section 3.2). The transistor M_1 is driven in the saturation region. Therefore, when the channel-length modulation is neglected, the relation between the constant bias current I_{bias} and the input and output voltages is given by [79]:

$$I_{bias} = \frac{1}{2} \cdot \mu_p \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_{M1} \cdot (V_{GS(M1)} - V_{th})^2 \tag{5.23}$$

where μ_p is the carrier mobility in *p*-type silicon, C_{ox} is the gate oxide capacitance per unit area, W is the transistor's channel width, L is the transistor's channel length, $V_{GS(M1)}$ is the gate-source voltage of the PMOS M_1, and V_{th} is its threshold voltage. Since the bias current I_{bias} is constant, to satisfy Equation (5.23), the voltage $V_{GS(M1)}$ must also remain constant because all other parameters are fixed by the technology (i.e., μ_p, C_{ox}, V_{th}) and by the design (i.e., W, L). $V_{GS(M1)}$ is defined as:

$$V_{GS(M1)} = V_{G(M1)} - V_{S(M1)} = V_{CI} - V_{CI1} \tag{5.24}$$

Thus, the voltage difference between V_{CI} and V_{CI1} is a constant and adjusted by the design through the $(W/L)_{M1}$ ratio. Therefore, the circuit shown in Figure 5.24 provides a constant positive voltage shift for V_{CI1} (approximately +350 mV in the IPC).

The principle used to generate V_{CI2} is the same as the one used to generate V_{CI1}:

$$I_{bias} = \frac{1}{2} \cdot \mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_{M2} \cdot (V_{GS(M2)} - V_{th})^2 \tag{5.25}$$

$$V_{GS(M2)} = V_{G(M2)} - V_{S(M2)} = V_{CI} - V_{CI2} \tag{5.26}$$

However, the voltage shift provided by the NMOS M_2 is negative. The body effect of M_2 is cancelled by connecting its bulk directly to its source. This is possible because M_2 is an NMOS transistor in triple-well, which is available in the UMC technology

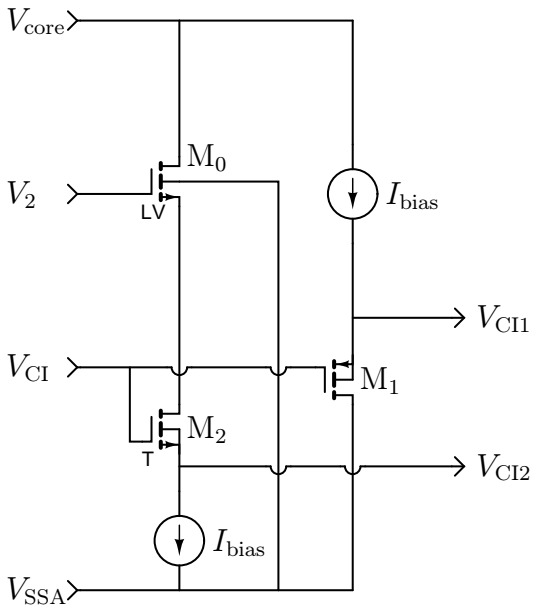

Figure 5.24: Schematic of the voltage shifter and the duty cycle limiter. The transistor M_0 is a low-V_{th} NMOS, and the transistor M_2 is an NMOS in a triple-well.

(see Section 3.2). The $(W/L)_{\text{M2}}$ ratio is also used to adjust by design the difference between V_{CI} and V_{CI2} (approximately $-350\,\text{mV}$ in the IPC).

As explained in Section 4.3.1, the duty cycle of the boost converter must be limited to 75%–95% to avoid unlimited energizing of the power inductor L_1 (see Figure 4.15). This represents a voltage limit between 40 mV and 200 mV below the maximum triangular oscillator voltage V_2, since in the IPC, the amplitude of the waveform generated by the triangular oscillator is 800 mV (see Section 4.3.1.2 and Section 5.1.3.3 for more details). In the circuit shown in Figure 5.24, the down shifting of V_2 is accomplished by the NMOS M_0. Since this down shift is around 100 mV, the use of a low-V_{th} transistor is mandatory for M_0 (see Table 3.5). The value of the down shift voltage is adjusted by the $(W/L)_{\text{M0}}$ ratio.

Unfortunately, the low-V_{th} transistors do no exist with the triple-well option in the chosen UMC L180 technology. Therefore, the body effect occurring in M_0 is unavoidable. However, this is not an issue, since the voltage V_2 is fixed and constant, thus the drain-source voltage drop $V_{\text{DS(M0)}}$ across M_0 is also constant, because M_0 is biased by a constant current source I_{bias}. Therefore, the bulk-source voltage V_{BS} is also constant. Finally, the maximum value of V_{CI2} is given by:

$$V_{\text{CI2}} \leq V_2 - V_{\text{th(M0)}} - V_{\text{DS(M2)}} \tag{5.27}$$

The combination of the two voltage shifters and the duty cycle limiter shown in Figure 5.24 makes the IPC advantageous compared to the state-of-the-art DC-DC converter (e.g., the LTC344x family from Linear Technology) in the domains of design complexity and design size. Namely, only two transistors are needed for doing the voltage shifting (M_1, M_2), one more for performing the duty cycle limitation (M_0), and two more for the current sources providing I_{bias}. Further, the weaknesses contained in the method developed by B. Sahu *et al.* [66] and presented at the beginning of Section 5.1.3 are avoided. This novel method is easy to design and to implement, and also very robust against noise.

5.1.3.3 Symmetrical Triangular Waveform Oscillator

In the PWM block diagram in Figure 5.1, the PWM oscillator consists in a symmetrical triangular waveform oscillator. The schematic of the triangular oscillator developed for the IPC is shown in Figure 5.25, and the corresponding simulation results are presented in Figure 5.26.

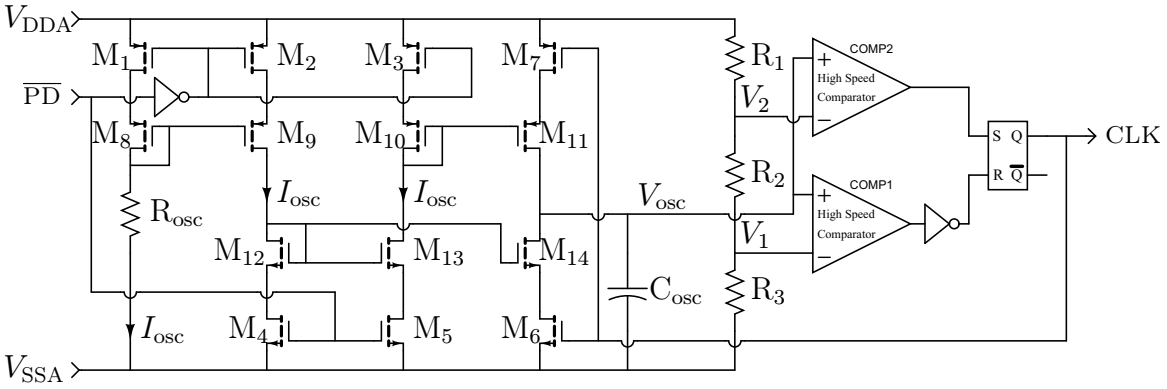

Figure 5.25: Schematic of the triangular waveform oscillator with adjustable frequency. The resistor R_{osc} used to adjust the switching frequency of the oscillator is an external resistor, which is not included in the CMOS layout of the IPC.

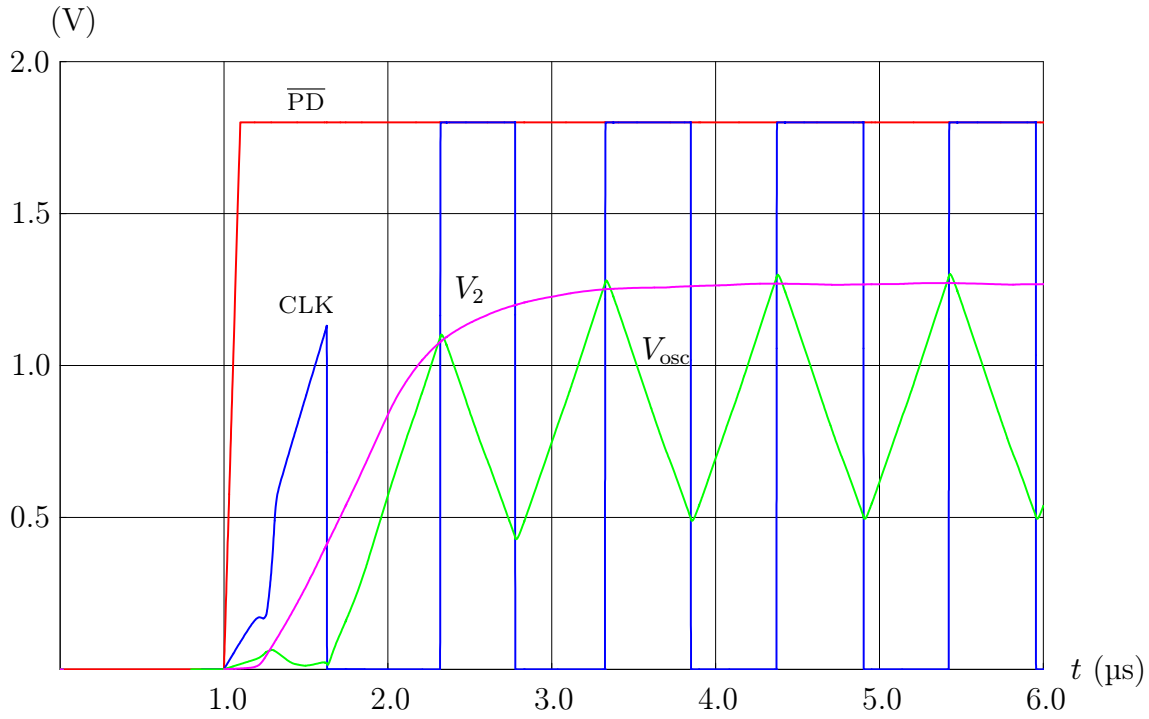

Figure 5.26: Simulation results of the triangular waveform oscillator.

The switching frequency of the DC-DC converter is defined by the switching frequency of the oscillator that generates the triangular carrier. The reasons for which a triangular carrier was chosen for the IPC has been exposed in Section 4.3.1.2. As

shown in the schematic in Figure 5.25, the principle used for generating the triangular voltage waveform carrier V_{osc} consists in charging and discharging the capacitor C_{osc} with the same constant current I_{osc}, thus generating a waveform with a constant slope:

$$V_{osc} = \frac{1}{C_{osc}} \cdot \int I_{osc} \cdot dt \tag{5.28}$$

In the schematic presented in Figure 5.25, the transistors M_1, M_2, M_3, M_4, M_5 are used as switches. In the IPC, these transistors are used to power down the triangular oscillator through the $\overline{PD}$ signal, and also to compensate for the drain-source voltage drop across the switching transistors M_6 and M_7. The resistor R_{osc}, which is an external resistor not included in the CMOS layout of the IPC, is used to setup the current flowing though the transistor M_8, which is connected in a diode configuration. The transistor pairs (M_8, M_9), (M_{10}, M_{11}), (M_{12}, M_{13}), (M_{12}, M_{14}) are connected in a current mirror configuration. The drain currents in M_{12}, M_{13}, M_{10} are therefore identical. When M_6 is turned on (i.e., M_7 is turned off), the drain current in M_{14} is equal to the drain current in M_{12}. On the contrary, when M_7 is turned on (i.e., M_6 is turned off), the drain current in M_{11} is equal to the drain current in M_{12}. The turn-on and turn-off of M_6 and M_7 is done by the clock signal CLK, which is itself constructed in the following way: when M_6 is turned off, M_7 is turned on, the constant current I_{osc} is sourced by M_{11}, thus charging C_{osc}. V_{osc} increases, and when it reaches V_2, COMP2 outputs a logic **1** and sets the RS flip-flop output Q to 1. This turns off M_7 and turns on M_6, so M_{14} is sinking the constant current I_{osc}, thus discharging C_{osc}. As a result, V_{osc} decreases, until it reaches V_1. Then COMP1 resets the RS flip-flop and the next cycle begins. The configuration of the comparators COMP1 and COMP2 avoid the possibility of having both R and S signals high simultaneously.

The reference voltages V_1 and V_2 are noise sensitive. Since the high speed comparators designed for the IPC (see Section 5.1.3.4 for more details) generate noise on their noninverting inputs when their output switches, the quiet inverting inputs have been connected to the reference voltages V_1 and V_2. In the IPC, V_1 is set to 0.5 V and V_2 to 1.3 V (See Figure 4.21). The noisy noninverting inputs have been connected to the V_{osc} triangular waveform. The reason for this is that the V_{osc} voltage is less noise sensitive because of the presence of the C_{osc} capacitor. In this configuration, the triangular oscillator in Figure 5.25, which is supplied by the 1.8 V V_{core} voltage, is able to generate a triangular waveform with low distortion at frequencies up to 10 MHz. When R_{osc} is adjusted so that the oscillator frequency is 1 MHz, the triangular waveform oscillator consumes a total power of 80 µW (i.e., 45 µA at a supply voltage of 1.8 V). The startup time is less than 2 µs, as shown in Figure 5.26.

5.1.3.4 High Speed Comparator

For the PWM regulator shown in Figure 5.19 and for the triangular waveform oscillator shown in Figure 5.25, the comparators COMP1 and COMP2 are two high speed comparators. These high speed comparators are based on the *very-wide common-mode-range differential amplifier* (VCDA) developed by M. Bazes [81], [82]. The schematic of such a comparator is shown in Figure 5.27 and the corresponding simulation results are provided in Figure 5.28. The VCDA provides a rail-to-rail voltage input range since it uses complementary MOSFETs in the input stage (M_1, M_2, M_3, M_4). The NMOS M_1 and M_2 are isolated in triple-well so that the bulk can be shorted

with the source to cancel the body effect. The output of the VCDA has been buffered to provide a rail-to-rail output swing with improved driving strength (M_{14}, M_{15}). The transistor M_{16} is used as decoupling capacitor on the power rails, to absorb the important current peaks generated in the supply rails by the fast switching transients occurring in fast comparators.

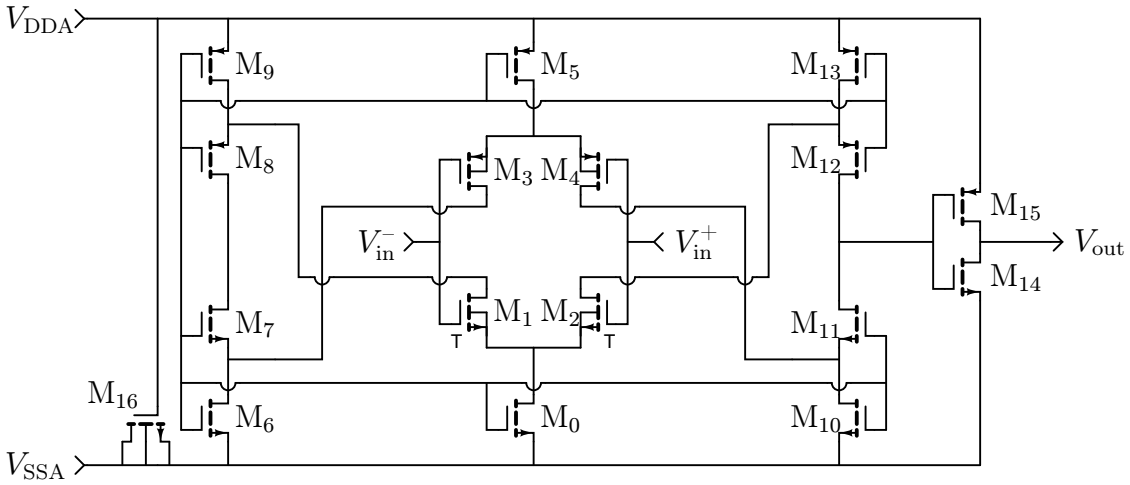

Figure 5.27: Schematic of the high speed VCDA comparator [81], [82].

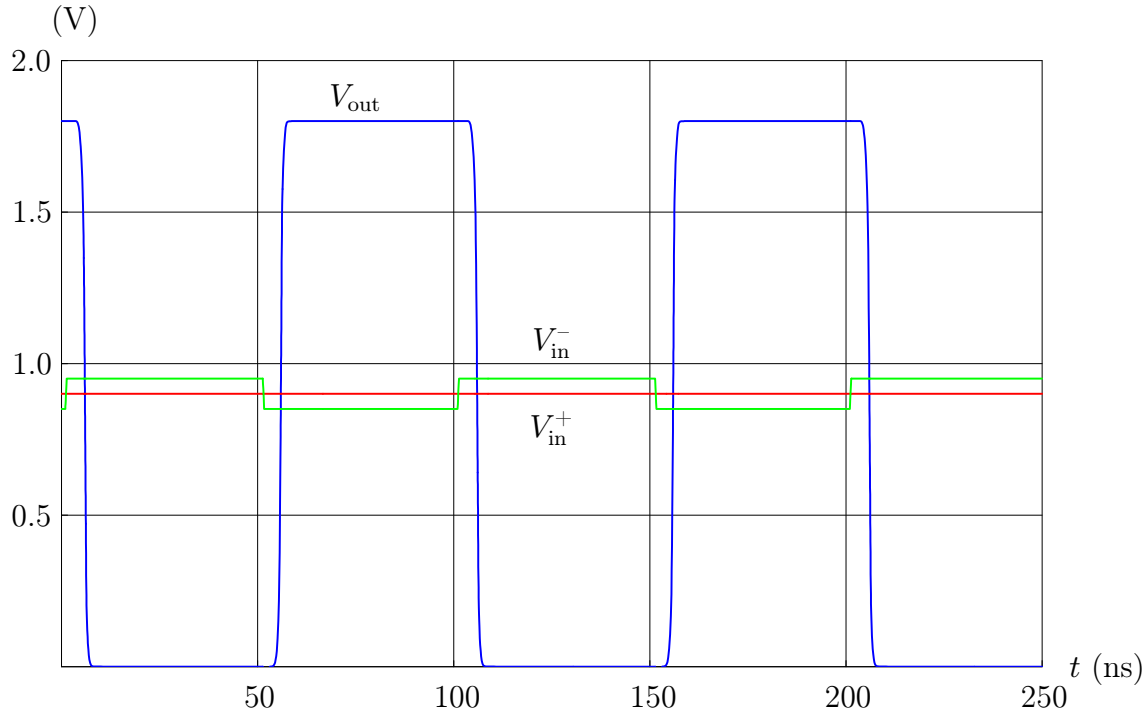

Figure 5.28: Extracted layout simulation results (i.e., with parasitics) of the high speed VCDA comparator when it is supplied by a 1.8 V voltage. In this case, the comparison time is less than 10 ns.

Figure 5.28 shows the simulation results obtained in the Cadence Spectre environment when the VCDA is supplied by a 1.8 V voltage. Because of their influence on the

signal delay (approximately a factor 2), the layout parasitics were considered for the simulations. Therefore, the extracted layout of the VCDA was used to get these simulation results. A fixed 1.0 V voltage has been provided to the noninverting input, and a square wave has been applied to the inverting input. The overdrive voltage of the square wave applied to V_{in}^{-} is about 50 mV, and its frequency is 10 MHz. The output is switching from rail-to-rail with a delay of approximately 8 ns. If the parasitics are not taken into account, the observed delay is only about 5 ns. The low power VCDA developed for the IPC consumes less than 30 µW (16 µA at 1.8 V). It is faster and consumes less power than the comparators reported in the most recent literature. For example, in the latest paper found about high-speed and low-power continuous-time comparators, W. Chu [91] reports a measured average delay of about 63 ns at a supply voltage of 3.0 V and a supply current of 1.3 mA. The VCDA designed for the IPC is therefore 8 times faster and consumes more than 72 times less power. Further, when the designed VCDA is supplied with 3.3 V, the comparison time becomes less than 4 ns, but 330 µW of power are then consumed (i.e., the quiescent current is 100 µA).

5.1.4 Current Measuring Unit

The current measuring unit is the most complex unit from a design point of view that was developed for the IPC. It was the most time consuming, because of the difficulty to combine an acceptable measurement accuracy with the high switching frequencies reached by the IPC (i.e., up to 10 MHz). Further, it was decided in the specifications of the IPC not to allow the current measuring unit to restrict the choice of the external device types, nor to request additional external components (e.g., a current sense shunt resistor). The current measuring unit regroups mainly three functions: the protection of the IPC against overcurrent (see Section 5.1.4.1), the measurement of the average inductor current for performing the constant current battery charging phase (see Section 5.1.4.2), and the zero-current crossing detection for avoiding the inductor current to reverse when performing in the discontinuous conduction mode (see Section 5.1.4.3).

5.1.4.1 Overcurrent Protection

The overcurrent protection principle in the IPC is ensured by the circuit shown in Figure 5.29. Actually, two of these circuits are implemented in the IPC, because both of the energizing transistors in the H-bridge needs to be protected (i.e., PMOS M_1 and M_4 in Figure 2.17). The function of this circuit is to protect the power transistors, the bonding wires, and the metal paths from sustained overcurrents.

The principle used by the overcurrent protection circuit shown in Figure 5.29 for detecting an overcurrent condition through the PMOS M_4 consists in measuring its drain-source voltage $V_{\text{DS(M4)}}$. The resistor R_{lim} is sized so that the voltage drop across it is equal to $V_{\text{DS(M4)}}$ when its drain current $I_{\text{D(M4)}}$ is approximately equal to 3 A. The digital signal OCP is used to enable and disable the overcurrent protection function (used in prototype for overcurrent failure tests).

During a normal battery charging phase (i.e., no overcurrent situation), when the power PMOS M_4 in the H-bridge (see Figure 4.15) is turned on, the voltage drop across it is less than the voltage drop across R_{lim} (see Figure 5.29) (i.e., $V_{\text{SW2}} > V_{\text{lim(M4)}}$). In the case an overcurrent situation occurs (i.e., V_{SW2} is below $V_{\text{lim(M4)}}$ when PMOS M_4

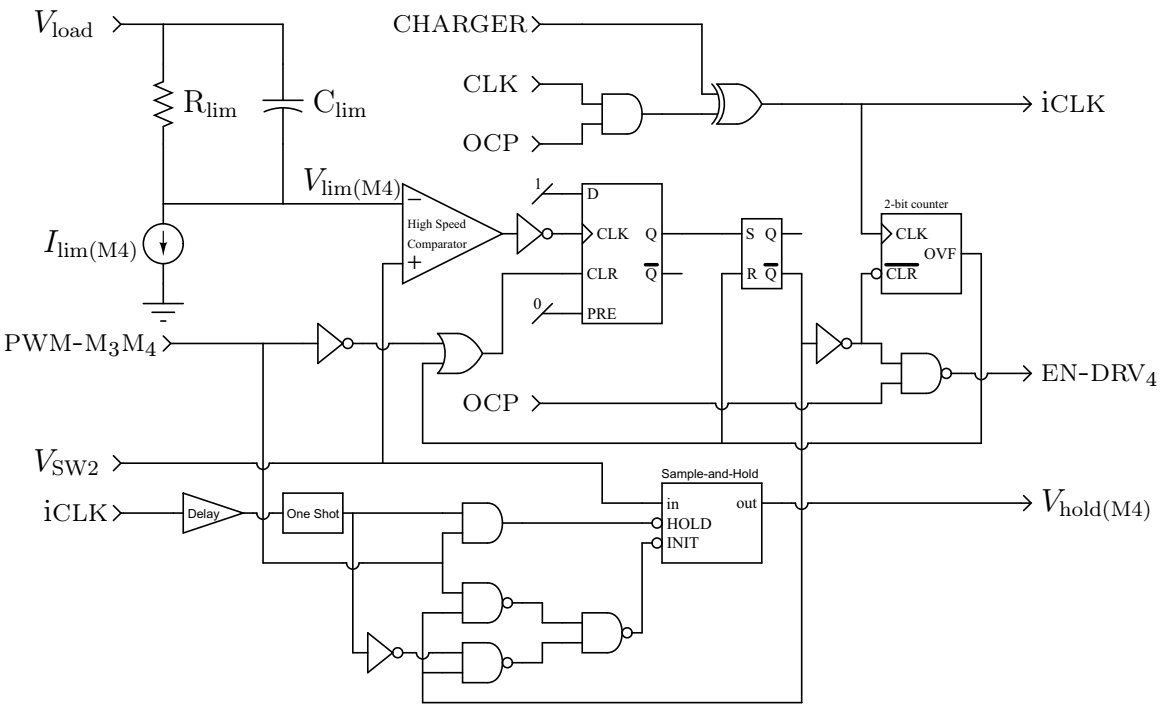

Figure 5.29: Schematic of the overcurrent protection circuit for the power PMOS M_4 in the H-bridge. The same type of protection is used for the power PMOS M_1. The sample-and-hold circuit is detailed in Figure 5.31.

is turned on), the clear input CLR of the D flip-flop goes low, and the output of the high speed comparator provides a falling edge. Therefore, the logic **1** present on the input D of the D flip-flop is copied to the S input of the RS flip-flop. The clear signal $\overline{\text{CLR}}$ of the 2-bit counter is then removed. The counter begins to count internally on each rising clock edge CLK, and during this time, M_4 is turned off because EN-DRV_4 is low. After 4 clock pulses, the 2-bit counter overflows (i.e., OVF goes high) and the RS flip-flop is reset, thus the EN-DRV_4 signal goes high. The power MOSFET M_4 is therefore enabled again, until another overcurrent condition is detected.

Some additional circuitry is shown in Figure 5.29 for generating an analog signal named $V_{hold(M4)}$, which is used in the average current sensing unit and described in Section 5.1.4.2.

5.1.4.2 Average Current Sensing

The average current sensing unit shown in Figure 5.30 estimates the average current flowing through the power inductor L_1 (see Figure 4.15). At the time this thesis was written, no H-bridge converter with an internal average current sensing unit, independent of the external components, has been found in the literature. In a DC-DC converter, the condition for choosing between PFM and PWM mode is related to the current I_{load} consumed by the load (see Figure 4.5). In the DC-DC converter presented by B. Sahu *et al.* in 2005 [66], the transition between PFM and PWM is not automatic, because no current sensing circuit was integrated. This is certainly due to the important design effort needed for developing such a circuit.

For the IPC, a novel average current sensing method was developed. However, it

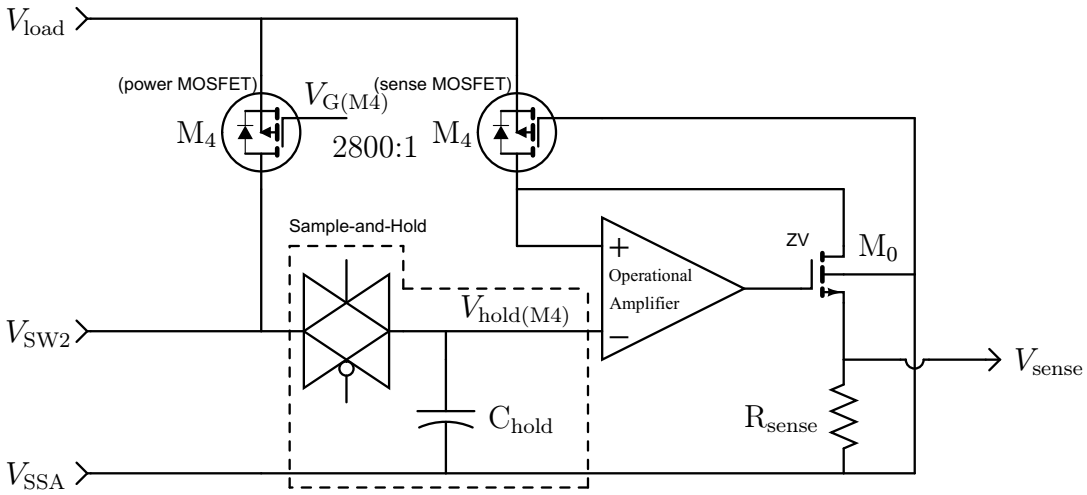

Figure 5.30: Schematic of the average current sensing circuit used when charging the battery in the constant current mode. Note that the command signals of the sample-and-hold circuit are shown in Figure 5.31.

was decided not to implement the PFM mode, since it has become very popular in the literature and also in commercial DC-DC converters [69], [88], thus saving design time and silicon area for the prototypes. In the IPC, the average current sensing unit is needed for performing the constant current charging phase when the lithium-ion battery is being recharged, as exposed in Section 4.1.2. The development of this unit was very challenging, because of the high PWM switching frequencies and the number of operating modes available in the IPC (i.e., buck, buck-boost, boost).

As illustrated previously in Figure 2.17, the voltage across the power inductor in the buck-boost mode is inverted during each phase (i.e., energizing phase and de-energizing phase). This makes current sensing over a low-pass filter reproducing the image of the inductor current very difficult [92], [93], [94], [95], because of the generated switching noise. After having investigated and simulated this method, it was abandoned because of the poor accuracy and because of the important noise issues in the buck-boost operation mode.

Another method that was investigated consists in measuring the inductor current through the $V_{DS(on)}$ of the power MOSFETs. This method is more accurate than the previous one, but requires a well known $R_{DS(on)}$ of the power transistors. Unfortunately, in the IPC, the high side PMOS power transistors M_1 and M_4 (see Figure 4.15) are driven with a gate-source voltage V_{GS} that is dependent of the input battery voltage V_{batt} and the output load voltage V_{load}, respectively. This means that the $R_{DS(on)}$ of M_1 and M_4 is strongly dependent of the operating conditions, thus making the current measurement so inaccurate that it cannot be used for controlling the charging current precisely enough. Another idea consists in measuring the current across the low side NMOS power transistors M_2 and M_3 (see Figure 4.15) and drive them with a defined gate-source voltage V_{GS}, for example with the internal constant core voltage V_{core} of 1.8 V. This provides an accurate current measurement, however, in the simulation, an important drawback was discovered. The anti-crossconduction logic presented in Section 5.2.1 provides a well controlled blanking time between turn-off of the high side power transistor and turn-on of the low side power transistor only

if the gate of both NMOS power transistors are switched with the same gate drive voltage value. In other words, if the high side switch is driven with the battery voltage ($1.2\,\mathrm{V} \leq V_{\mathrm{batt}} \leq 4.2\,\mathrm{V}$) and the low side switch with the core voltage ($V_{\mathrm{core}} = 1.8\,\mathrm{V}$), the propagation delay in the low side drivers is much longer than in the high side drivers. It is therefore possible that, even if a delay is inserted for the turn-on of the high side switch, the turn-off of the low side switch can occur earlier. This means that the input battery voltage V_{batt} is shorted to the ground, thus generating very high shoot-through currents, which will destroy the IPC (e.g., bond wires fusing, electromigration). In simulation, shoot-through currents up to 18 A have been observed, even if the blanking time is set to 15 ns. An important blanking time reduces significantly the power conversion efficiency and the maximum PWM switching frequency. Therefore, to ensure a blanking time is provided for every gate drive voltage, the same gate drive voltage V_{GS} must be used for each pair of high and low side switches. This means that $(\mathrm{M}_1, \mathrm{M}_2)$ must be driven with V_{batt}, and that $(\mathrm{M}_3, \mathrm{M}_4)$ must be driven with V_{load}. This constraint makes the current sensing over the $V_{\mathrm{DS(on)}}$ of the low side switches impossible, since V_{batt} and V_{load} are not fixed (i.e., V_{batt} varies when the battery discharges, and V_{load} depends on the target application).

Finally, the method retained for measuring the inductor current in the IPC is the so-called SenseFET principle [94] illustrated in Figure 5.30. It consists in a current mirror that makes a copy of the current flowing in the energizing transistors of the H-bridge (i.e., M_1 and M_4) and injects it into a resistor (i.e., $\mathrm{R}_{\mathrm{sense}}$) to provide a voltage (i.e., V_{sense}) that is proportional to the sensed current. Since the layout of the sense MOSFET is part of the power MOSFET, good accuracy can be obtained by matched layouts (for example, when the sense MOSFET is a finger of the whole power MOSFET constituted of a lot of identical fingers). In the IPC, a reduction gain of 2800 : 1 is applied to the inductor current, which means that when a current of 2800 mA flows through the power MOSFET, the sense MOSFET sources only 1 mA. This gain between the power MOSFET and the sense MOSFET is only precisely defined if their $V_{\mathrm{DS(on)}}$ are equalized. This is the role of the operational amplifier.

The implementation of this sensing method has required important design effort, since the power MOSFET M_4 can switch at a frequency up to 10 MHz. At this frequency, and with a duty cycle D of 80% in boost mode, M_4 is turned on only 20 ns during each PWM cycle. No low power operational amplifier (i.e., consuming less than 50 µW of power) provides a bandwidth that is large enough to sense voltages or currents varying at these frequencies. To overcome this problem, the sample-and-hold circuit shown in Figure 5.31 has been implemented.

The drain-source voltage of the sense MOSFET in Figure 5.30 is adjusted by the operational amplifier to the value of the drain-source voltage of the power MOSFET, when the later is turned on. To have enough time to do this with a low power operational amplifier, the V_{SW2} voltage is copied to $V_{\mathrm{hold(M4)}}$ each time the power MOSFET M_4 is turned on by the sample-and-hold circuit shown in Figure 5.31. The accuracy of this average current sensing method is increased when a power inductor with a high inductance value L_1 is used, because the current variation through the inductor during one PWM cycle is reduced. This reduces the variations in the drain-source voltage $V_{\mathrm{DS(on)}}$ sensed by the sample-and-hold circuit, and also the speed of the current variation. As a consequence, the moment at which the sample is taken is therefore less important. For example, when showing the inductor current I_{L1} in Figure 4.22, it is easier to get an accurate value of the average inductor current when I_{L1} varies more

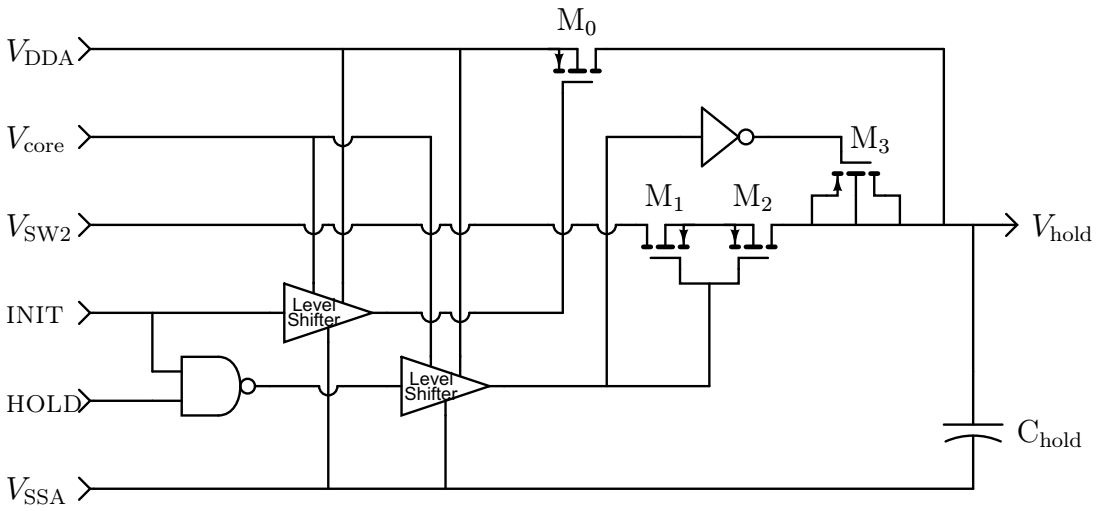

Figure 5.31: Schematic of the sample-and-hold circuit used in the IPC to sample the drain voltage of the PMOS M_4 in the H-bridge to measure and regulate the current flowing to the battery during the constant current charging mode. The transistor M_3 is used for performing clock feedthrough cancellation.

slowly and is closer to the average inductor current value. The sampling moment occurs at each rising and falling edge of the clock signal CLK provided by the triangular waveform oscillator presented in Section 5.1.3.3.

5.1.4.3 Zero-Crossing Current Detection

In Section 2.2.2 and especially in Figure 2.7, the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM) of the inductor current were presented.

A diode can conduct current only in the forward direction. However, a symmetrical lateral MOSFET that is turned-on can conduct current with low conduction losses in both directions. Therefore, DC-DC converters using synchronous rectification (i.e., controlled MOSFETs in the place of diodes) require an additional DCM circuit to drive the synchronous rectifier MOSFETs. The DCM circuit developed for the IPC is able to manage the discontinuous conduction mode in both charging and discharging directions. The schematic of this circuit is shown in Figure 5.32.

The function of the DCM circuit consists in detecting the moment at which the inductor current I_{L1} reaches zero and begins to reverse. At this moment, the DCM circuit must react rapidly and deactivate the rectifying switch to avoid the load voltage V_{load} to energize the inductor in the reverse direction (e.g., see the de-energizing phase of the buck mode in Figure 2.17). The circuit shown in Figure 5.32 was simulated and the corresponding simulation results are shown in Figure 5.33.

These simulations do not represent a real case (i.e., when the IPC is running): the V_{SW1} signal was chosen arbitrarily and it is equal to the drain-source voltage $V_{DS(M2)}$ across the power NMOS M_2 (see Figure 4.15). The inductor current I_{L1} is linked to $V_{DS(M2)}$ by the $R_{DS(on)}$ of M_2:

$$V_{DS(M2)} = R_{DS(on)(M2)} \cdot I_{L1} \tag{5.29}$$

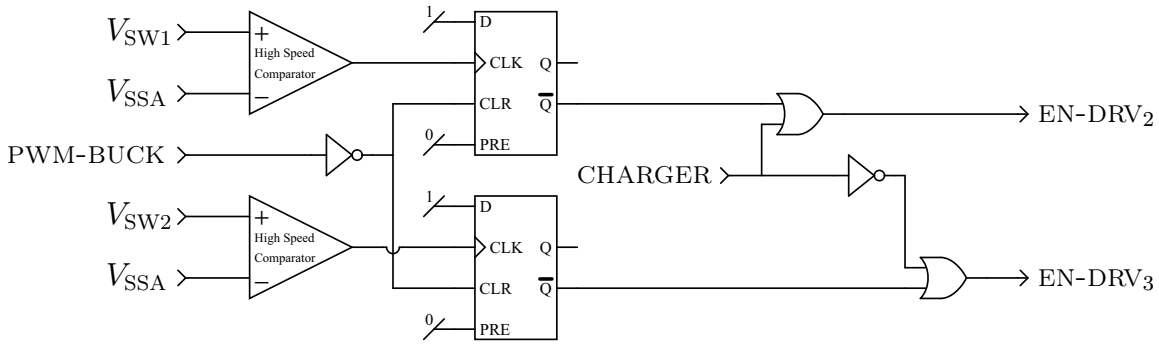

Figure 5.32: Schematic of the inductor current zero-crossing detection for discontinuous conduction mode operation in the IPC.

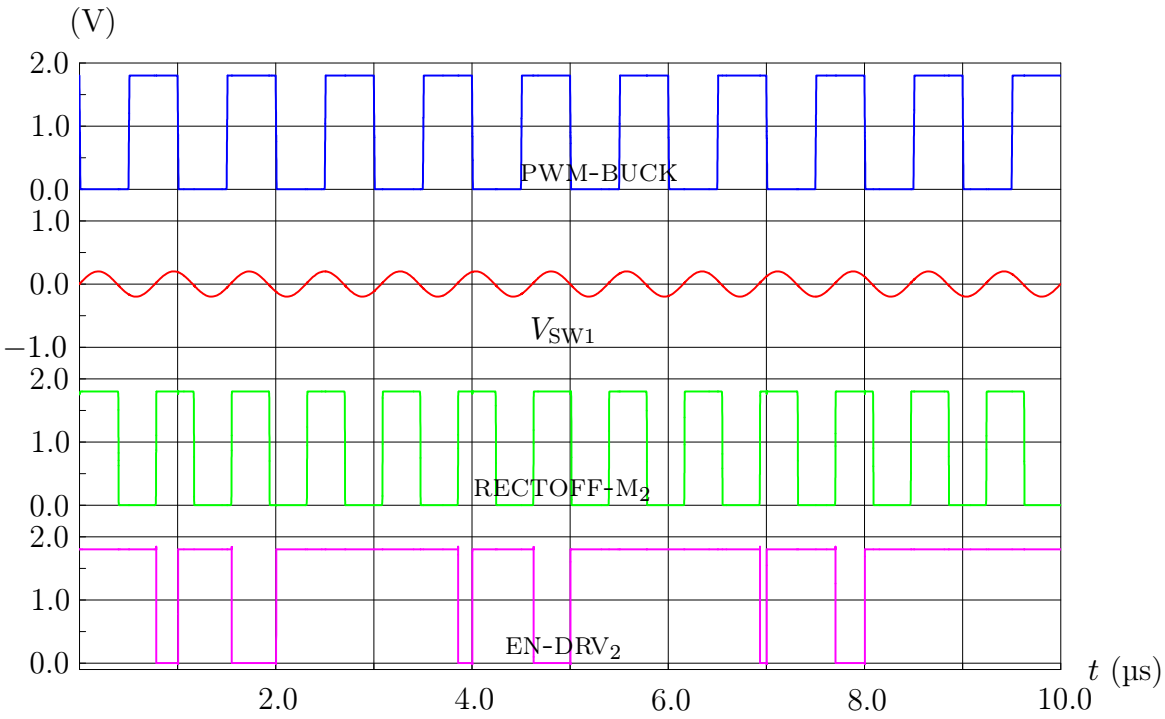

Figure 5.33: Simulation of the zero inductor current crossing detection for discontinuous conduction mode operation in the IPC. The voltage V_{SW1} has been chosen for the simulation and therefore does not represent the real signal waveform occurring in the IPC (e.g., V_{SW1} cannot be positive directly after a rising edge on PWM-BUCK, because I_{L1} is flowing to the output at this instant).

It is wanted from I_{L1} to flow from the input to the output when the battery is discharging. This means that when M_2 is turned on, $V_{DS(M2)}$ is negative. In other words, the DCM circuit must detect when $V_{DS(M2)}$ goes positive (i.e., when $V_{DS(M2)}$ reaches the zero potential defined by V_{SSA}).

The real signal transmitted by the gate drivers to the power PMOS M_1 is the PWM-BUCK signal, while the real signal transmitted by the MOSFET gate drivers to the power NMOS M_2 is the boolean "or" function of the signals PWM-BUCK and EN-DRV$_2$.

5.2 Digital Part Design

In this section, the technical characteristics from each elementary digital unit constituting the IPC is presented. All these units are low power units, like combinatory and sequential logical units. Each unit is detailed in its own paragraph: unit description, functional overview, electrical schematics, simulation results and layout considerations.

5.2.1 Anti-Crossconduction Logic

The function of the anti-crossconduction circuit shown in Figure 5.34 consists in avoiding the shoot-through current that could be initiated in the power transistor pairs (M_1, M_2) and (M_3, M_4) in Figure 4.15. The transistor pairs cannot be connected in a simple inverter configuration (i.e., with their gates tied together), since the generated shoot-through currents would reach hazardous values (e.g., shoot-through currents of more than 18 A have been simulated with the designed H-bridge when crossconduction is not avoided). Therefore, these shoot-through currents must absolutely be avoided, since they are destructive for the IPC (e.g., bond wires fusing, excessive load voltage ripple, important noise and heat generation, dramatic reduction of the power conversion efficiency, premature failure of the power transistors).

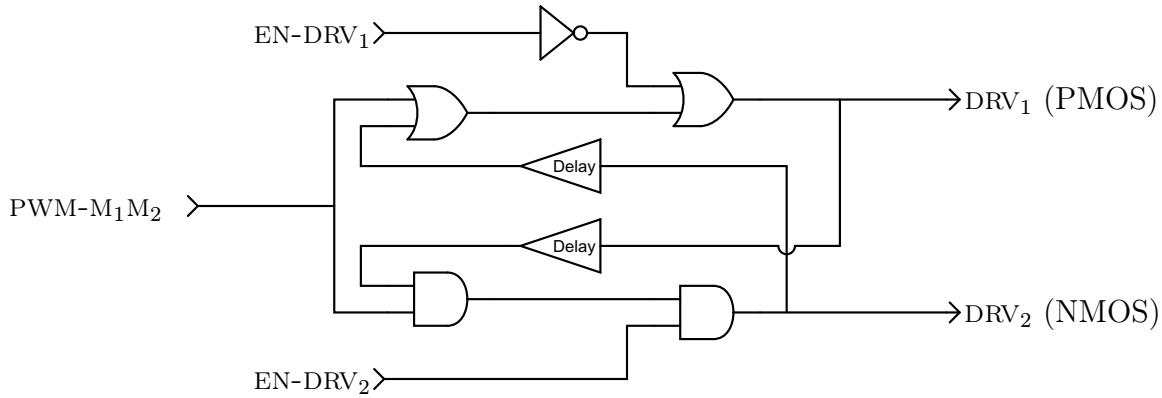

Figure 5.34: Schematic of the anti-crossconduction logic unit used for avoiding crossconduction between the complementary power transistor pairs M_1 and M_2 in the H-bridge. The same circuit is also used for the power transistor pairs M_4 and M_3, respectively.

The idea behind preventing crossconduction consists in adding a delay t_{delay} to the driver signal of the transistor that must be turned on. A typical sequence when the power transistor pair (M_1, M_2) is switching is: (M_1 off, M_2 on) during t_{off} ; (M_1 off, M_2 off) during t_{delay} ; (M_1 on, M_2 off) during t_{on} ; (M_1 off, M_2 off) during t_{delay} ; (M_1 off, M_2 on) during t_{off}.

The delay component used in the circuit shown in Figure 5.34 is made of an inverter chain with low drive strength and loaded with MOS capacitors, thus providing a delay of approximately 4 ns when supplied with the 1.8 V V_{core} voltage. The provided delay time t_{delay} is therefore constant and independent of the V_{batt} and V_{load} voltages. The anti-crossconduction circuit shown in Figure 5.34 was simulated, and the corresponding simulation results are shown in Figure 5.35.

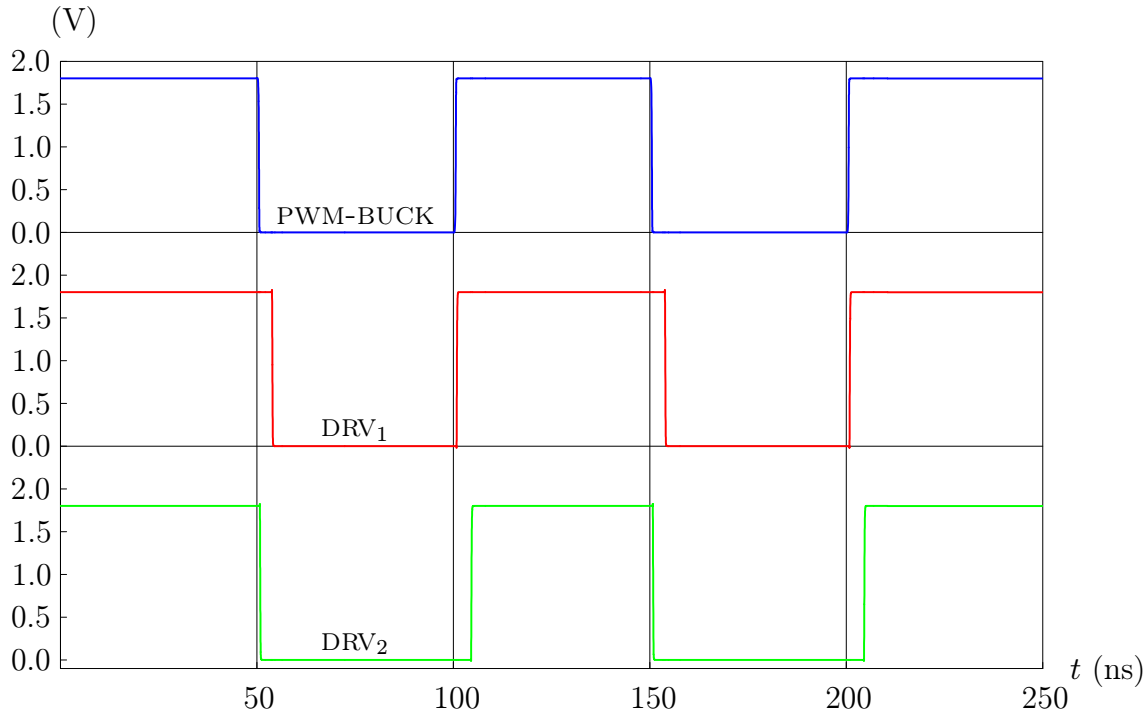

Figure 5.35: Simulation results of the anti-crossconduction logic unit.

5.2.2 High Speed Logic Level Shifter

The schematic of the high speed logic level shifters used in the IPC is shown in Figure 5.36. This level shifter is used to shift the logical levels (i.e., V_{core}) up or down, to adapt them to the voltage levels required by the gate drivers of the power MOSFETs (i.e., V_{batt} and V_{load}). The transistors of the logic level shifter were sized in such a way that they provide a switching time of less than 1 ns at both low and high output voltages. This is shown in the simulation results presented in Figure 5.37. Actually, this design is simpler and also faster than the fastest delay time reported in the literature by W.-T. Wang *et al.* in a 0.13 µm technology [96].

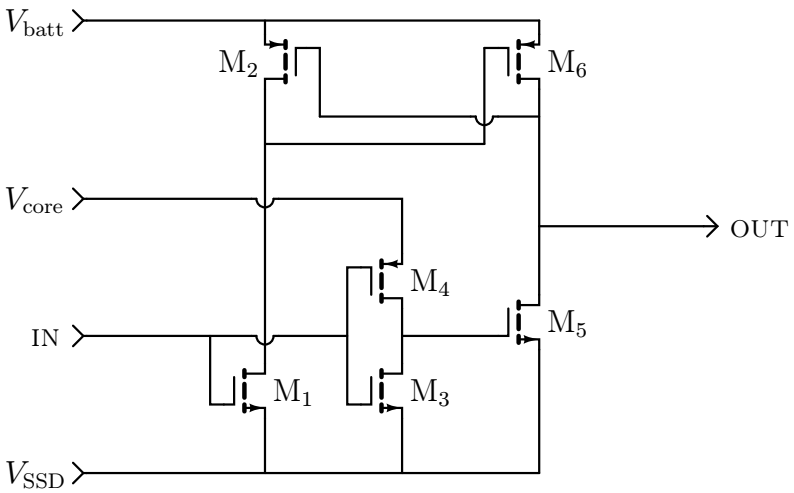

Figure 5.36: Schematic of the high speed logic level shifter. The architecture shown here is fully static and consumes current only during the transients.

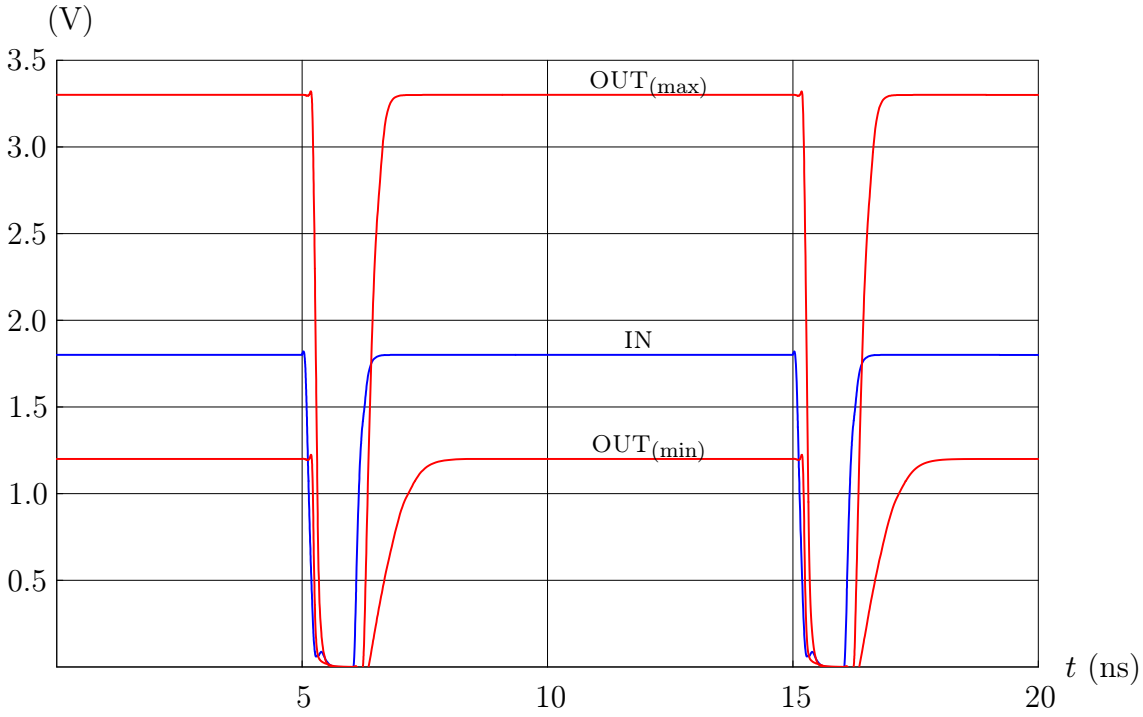

Figure 5.37: Simulation results of the high speed digital level shifter shown in Figure 5.36 when a 100 MHz PWM signal with a duty cycle D of 10% is applied to the input (IN). Two simulations were performed, one with a 1.2 V output level ($\text{OUT}_{(\text{min})}$) and one with a 3.3 V output level ($\text{OUT}_{(\text{max})}$).

5.2.3 One Shot Pulse Generator

For driving the sample-and-hold circuit shown in Section 5.1.4.2, in Figure 5.29 and in Figure 5.30, a one shot pulse generator has been developed. Its circuit is shown in Figure 5.38 and the corresponding simulation results are provided in Figure 5.39. The principle used for generating the single pulses on clock edges consists in superposing the real clock signal over a delayed one. Three digital outputs are provided by the one shot pulse generator. The PULSE-R output generates a 2 ns width pulse on every rising clock edge, while the PULSE-F output generates a 2 ns pulse on every falling clock edge. The PULSE-RF output generates 2 ns width pulses on both rising and falling clock edges.

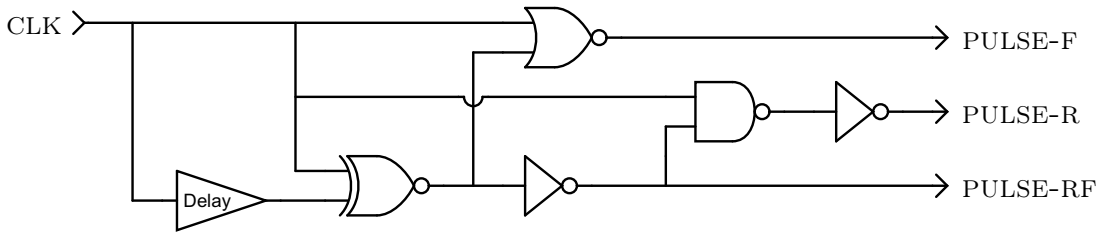

Figure 5.38: Schematic of the one shot pulse generator able to generate 2 ns pulses on rising, falling, or both rising and falling edges of an input clock.

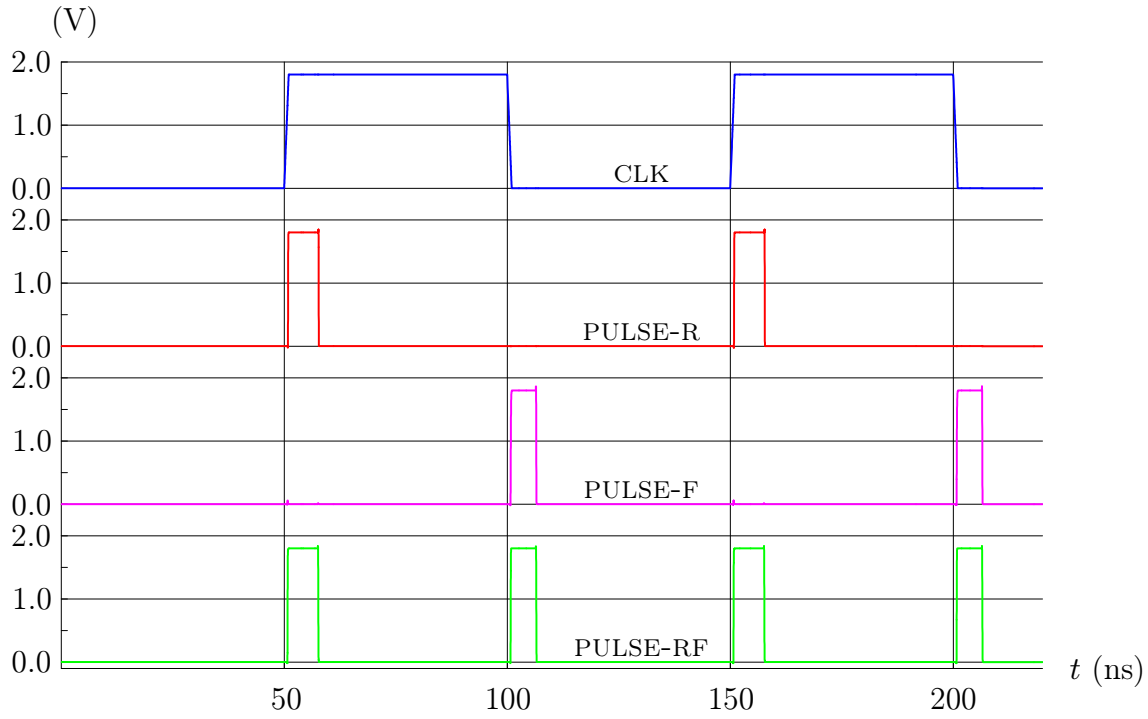

Figure 5.39: Simulation results of the one shot pulse generator.

5.2.4 I²C Test Interface

For testing the manufactured prototypes, a digital *inter-integrated circuit* (I^2C) interface has been developed by M. Al-Rabbat within the scope of his master thesis [97]. The role of this interface is to enable the probing of internal analog and digital signals, and to output them to a pin (V_{test}), so that they can be observed with an oscilloscope. This interface is commanded by an external microcontroller using a bidirectional clock (SCL) and data (SDA) line. The principle is illustrated in Figure 5.40. Before the I^2C interface could be implemented in the IPC, its layout had to be redesigned, since the digital core-fillers containing the supply rail decoupling capacitors were not integrated properly. A layout view of the I^2C interface is provided in Figure 5.41.

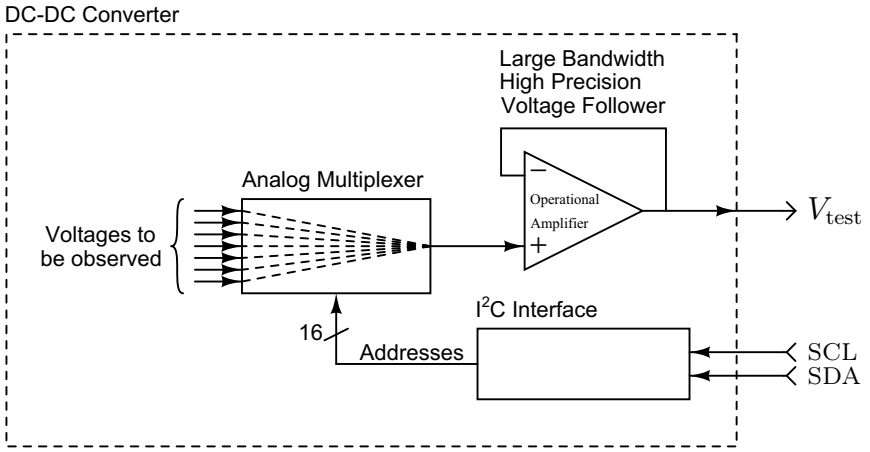

Figure 5.40: Block diagram of the digital I^2C test interface.

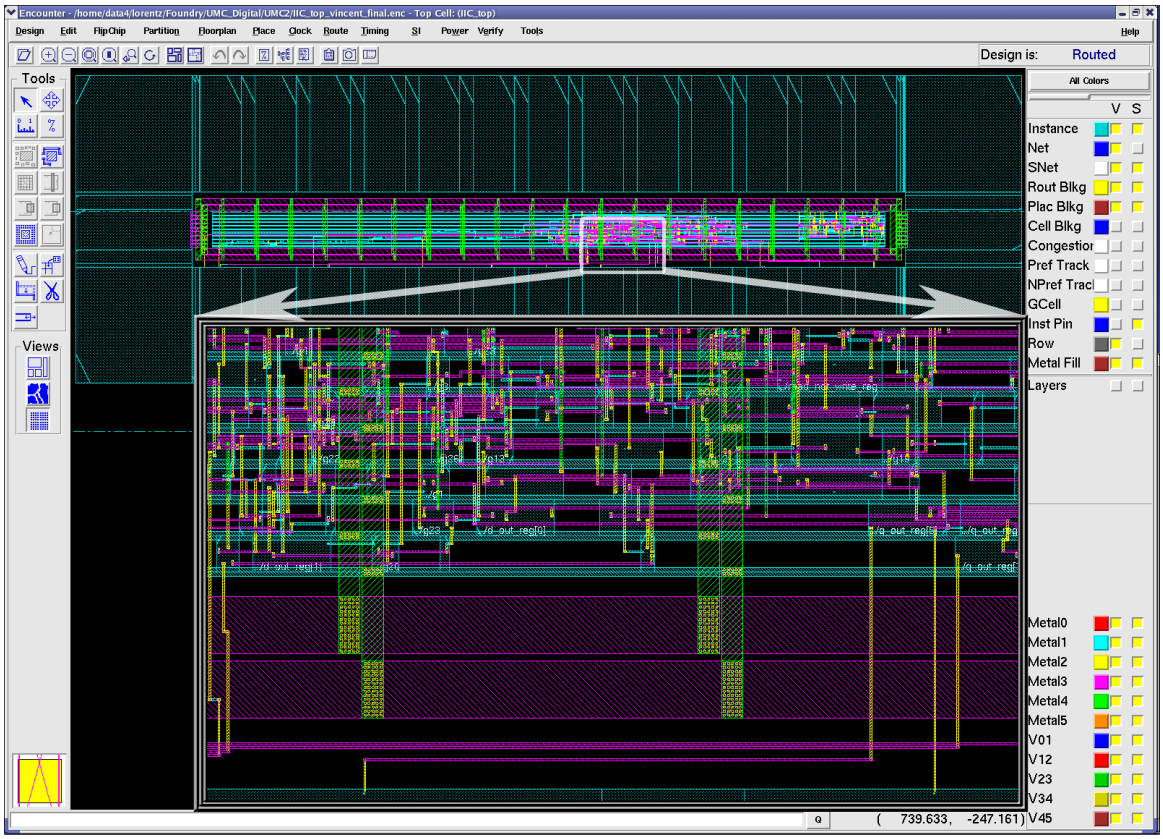

Figure 5.41: Layout of the digital I^{2}C interface.

5.3 Power Part Design

The challenges of power CMOS design are located in the layout [79], [98], [99], [100]. The power part of the bidirectional DC-DC converter consists in the four power transistors (H-bridge) and their corresponding gate drivers. The layout of the power transistors is presented in detail in Section 5.3.1. The design and the layout configuration of the gate drivers is presented in Section 5.3.2.

5.3.1 Power Transistors Layout

The four power transistors in the H-bridge (and also their drain and source metal connections) are sized in such a way that they can provide 2000 mA of continuous current at a die temperature of 80°C with a drain-source voltage drop V_{DS} around 50 mV when they are driven with a gate-source voltage V_{GS} of 1.8 V.

Since in silicon, the mobility of holes μ_p is around one-third of the mobility of electrons μ_n, p-channel transistors (i.e., PMOS) provide a higher channel resistance $R_{DS(on)}$ than n-channel transistors (i.e., NMOS) [79]. In the UMC technology, when turned on with the same gate drive voltage, and for the same channel length L, a PMOS transistor must be sized three times wider than the complementary NMOS transistor to provide the same drain-source voltage drop $V_{DS(on)}$ when turned on. Therefore, in the H-bridge of the IPC, the channel width W_p of the high side PMOS transistors (i.e., M_1, M_4) has been chosen three times wider than the channel width

W_n of the low side NMOS transistors (i.e., M_2, M_3):

$$W_p = 3 \cdot W_n \tag{5.30}$$

This design constraint (i.e., three PMOS for one NMOS) has forced the development of a specific layout topology, allowing the highest possible power density to be reached. The schematic arrangement that satisfies this constraint for the power transistors in the H-bridge is shown in Figure 5.42. The connections on the right side are the battery connections ($V_{\text{batt\_a}}$, $V_{\text{batt\_b}}$) for V_{batt}, the load and charger connections ($V_{\text{load\_a}}$, $V_{\text{load\_b}}$) for V_{load}, the inductor connections ($V_{\text{SW1\_a}}$, $V_{\text{SW1\_b}}$, $V_{\text{SW2\_a}}$, $V_{\text{SW2\_b}}$) for V_{SW1} and V_{SW2} and the power ground connection V_{SSP}.

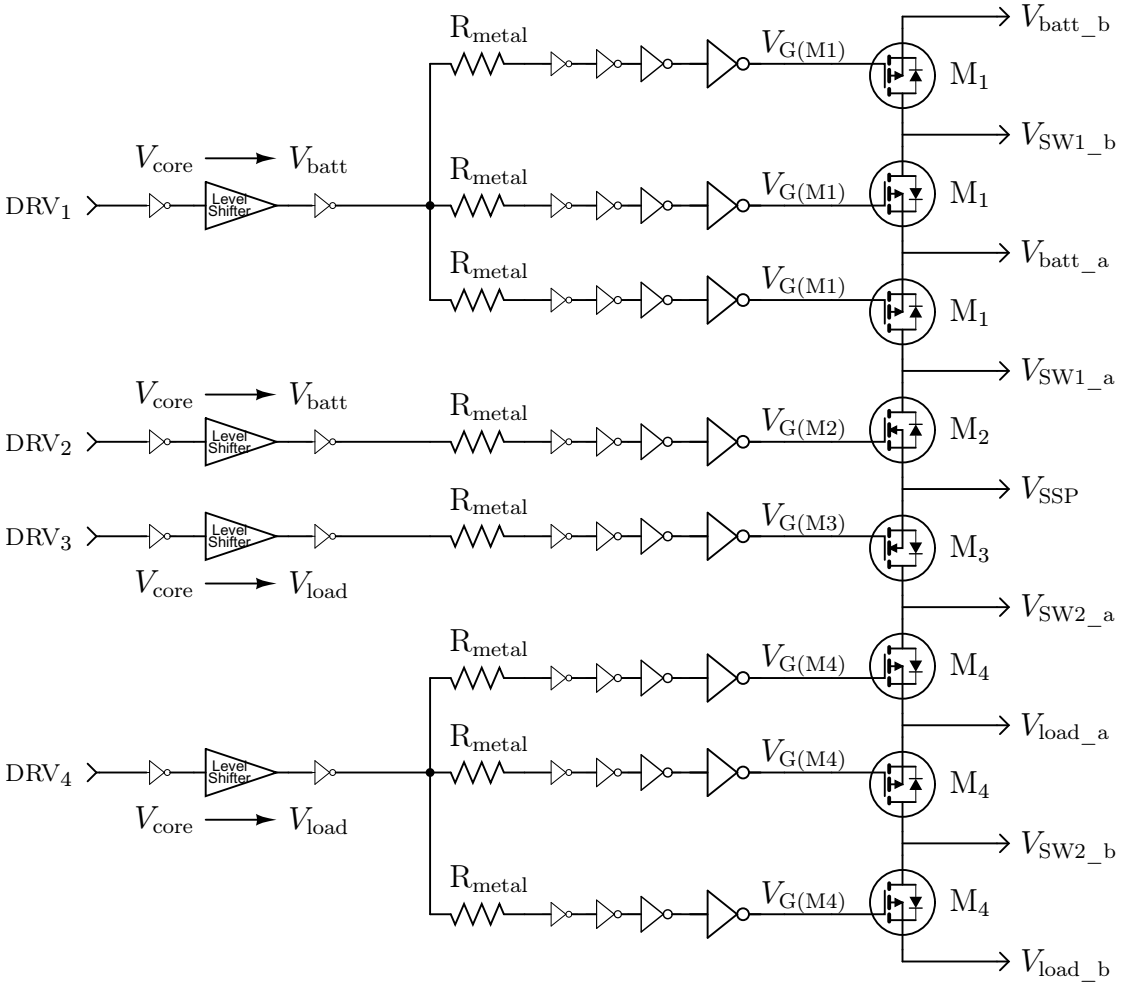

Figure 5.42: Schematic of the power part showing the high speed logic level shifters, the MOSFET gate drivers, and the power MOSFETs.

The best way to get the lowest silicon area occupation when transposing the circuit shown in Figure 5.42 into the layout, is to design NMOS and PMOS power transistors that can be easily assembled together in a huge matrix. A layout view of an elementary power NMOS in triple-well is shown in Figure 5.43. The reasons of the choice of the triple-well option for the NMOS in the H-bridge were exposed in Section 3.2.1.2. The function of the triple-well isolation in the power NMOS is to decouple them from the substrate, thus reducing significantly the injected switching noise [55]. A layout

view of an elementary power PMOS in an n-well is shown in Figure 5.44. An example of assembly of these power transistors in a matrix field establishing the H-bridge is shown in Figure 5.45.

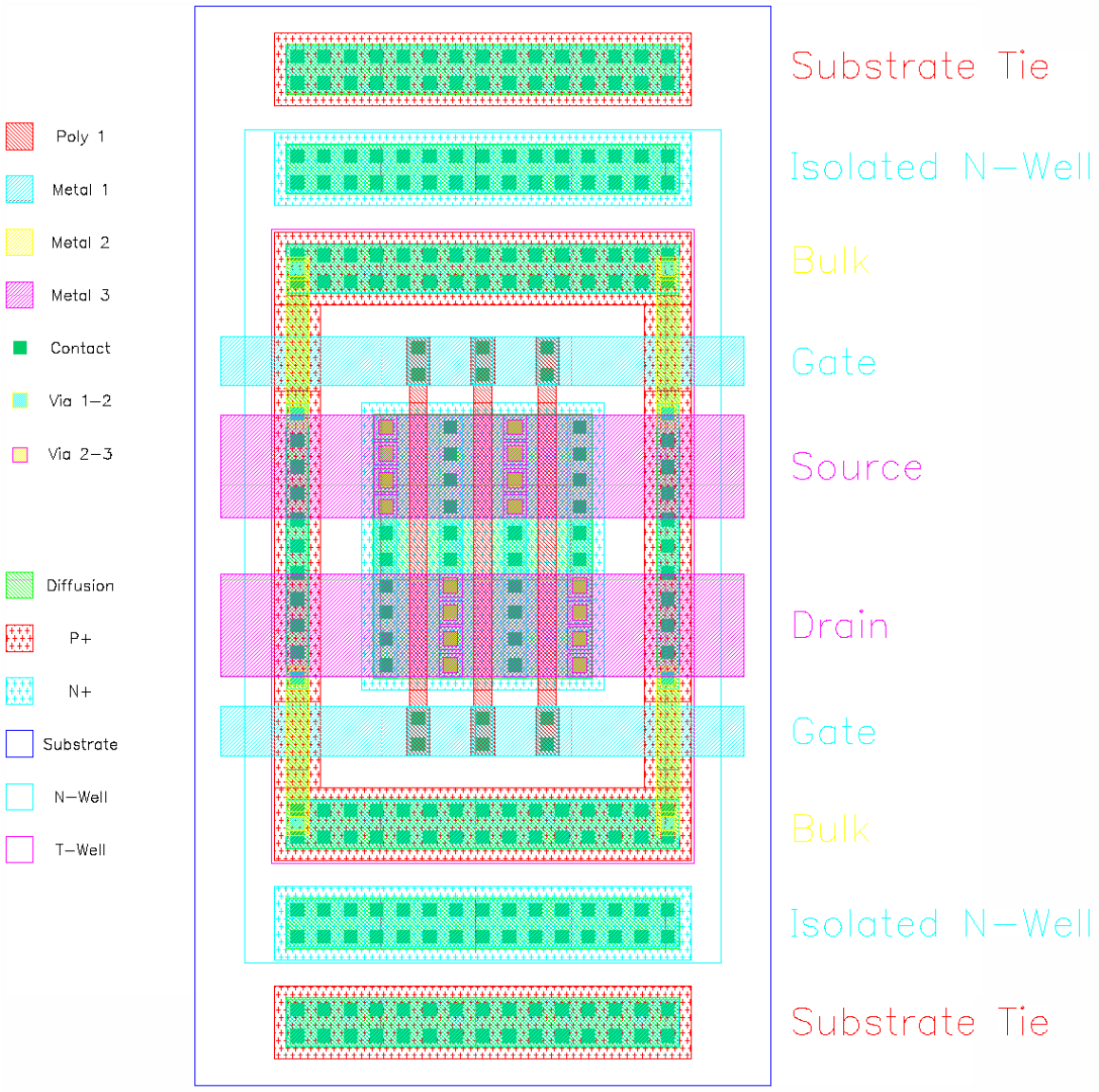

Figure 5.43: Simplified layout of a part of a triple-well power NMOS in the H-bridge. Refer to the Figure 3.5 for a vertical view of an NMOS transistor.

In the simplified layout views of the NMOS and PMOS power transistors shown in Figure 5.43 and Figure 5.44, the elementary power transistors are represented with only 3 fingers (i.e., 3 gates). In the layout of the H-bridge in the IPC, each elementary power transistor is designed with 25 fingers of 25 µm width each, thus providing a short gate length and therefore a low gate resistance. Additionally, the polysilicon gates are contacted on both sides with metal 1, thus halving the gate resistance. This enables high switching frequencies when charging and discharging the parasitic gate capacity.

When laying out power transistors in a CMOS technology, three main aspects must be considered. First, the power transistors are powerful noise generators. Therefore, they must be well isolated from the sensitive analog circuits present on the same silicon

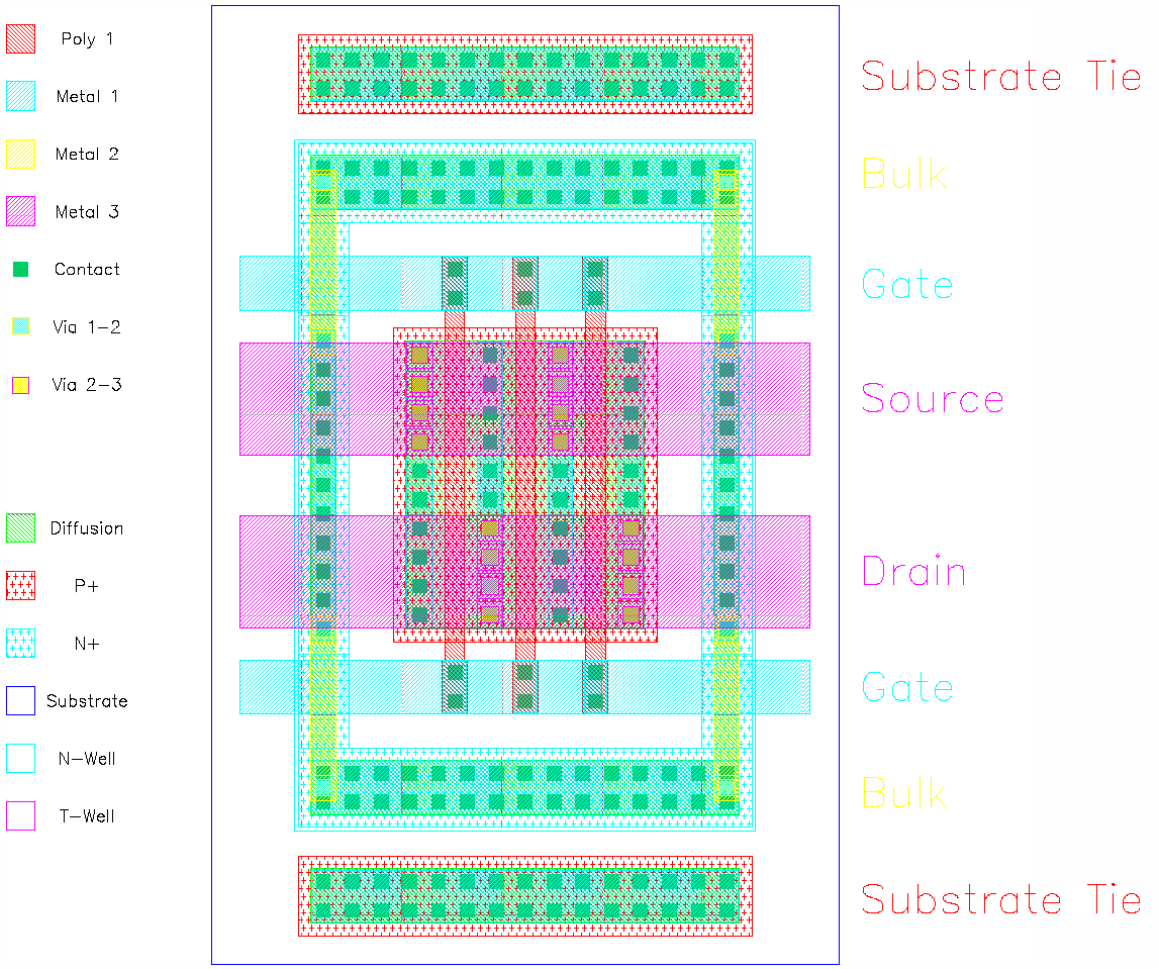

Figure 5.44: Simplified layout of a part of a power PMOS in the H-bridge. Refer to the Figure 3.5 for a vertical view of a PMOS transistor.

die. To do this, wide guard rings must be laid out all around the power transistors. For the NMOS power transistor shown in Figure 5.43, this is the function of the substrate tie and the contacts located in the isolated *n*-well area. For the PMOS power transistor shown in Figure 5.44, this is the function of the substrate ties only. Second, the implementation of both NMOS and PMOS closely together increases the danger of initiating the parasitic thyristor they constitute [79]. If this occurs, the current carried by the power transistors is able to damage the IPC (e.g., fusing of bond wires or metal interconnections). This effect is called *latch-up* and is due to a weakly connected bulk (e.g., not enough bulk contacts). In the H-bridge of the IPC, the bulk contacts are strongly connected to the supply rails (i.e., wide diffusions and wide metal paths) and they are routed all around each elementary power transistor (see Figure 5.43 and Figure 5.44). Therefore, each point inside an active area in the H-bridge is never separated from more than 16 µm of a bulk connection (real value measured in the final layout of the second prototype of the IPC also taking into account the additional space needed by the gate connections, as shown in Figure 5.43, Figure 5.44, and Figure 5.45). Third, the power transistors must provide body diodes that are sized large enough to support the full inductor current during the dead time of the switching transients. These body diodes are considered in the BSIM3v3 MOSFET models provided by UMC. However, the area of the bulk connections of these body

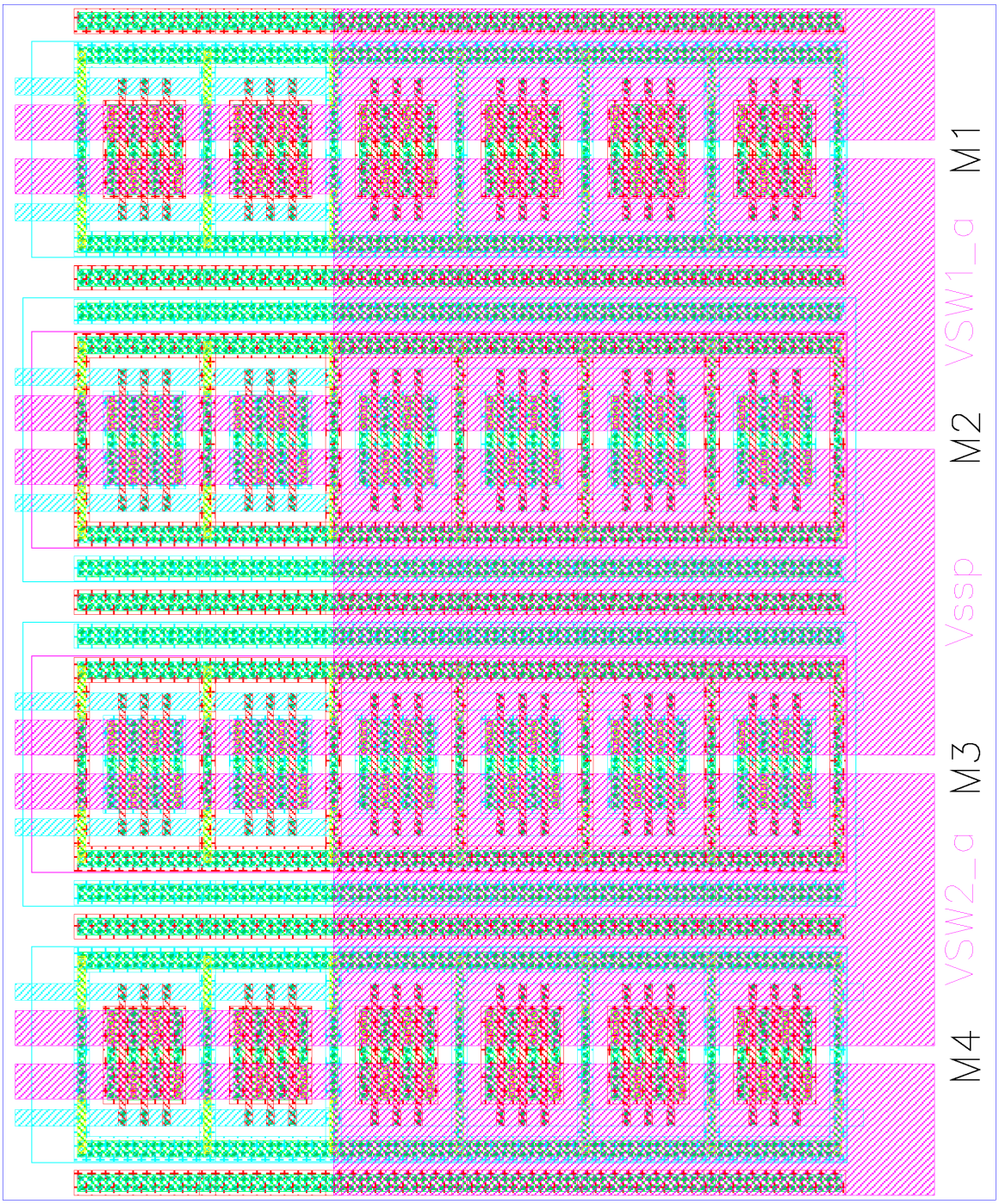

Figure 5.45: Simplified layout of parallel and serial connected power MOSFETs as it is done for the H-bridge. The power NMOS and PMOS are laid out in such a way that they can be connected together in a compact matrix arrangement. On the left side, a part of metal 3 has been removed to make the underneath layers better visible. For the legend, refer to Figure 5.43.

diodes cannot be adjusted in the simulation environment (i.e., Cadence Spectre). This area is internally defined and calculated as linearly dependant on the total width W of the power MOSFET. However, the real electrical behavior of a body diode (e.g., current capability, forward voltage drop) with a small bulk connection area is not the same as with a large bulk connection area. In the H-bridge of the IPC, the bulk

connection area has been sized in such a way that it occupies the same area as the drain connection of the corresponding power MOSFET. This design choice allows the IPC to be used without external Schottky diodes in parallel with the body diodes provided by the power MOSFETs in the H-bridge. However, to reach the highest efficiency, the use of external fast recovery Schottky diodes is recommended.

The simplified layout of an H-bridge shown in Figure 5.45 is not complete. As shown in Equation (5.30), the width W_p of the power PMOS transistors must be three times larger than the width W_n of the power NMOS transistors. Therefore, in the real layout of the IPC, the power PMOS M_1 and M_4 each consist in three rows laid out and connected electrically as shown in Figure 5.42. In other words, this means that there are not only four rows of power transistors constituting the H-bridge of the IPC as shown in Figure 5.45, but actually a total of eight rows (3 rows for PMOS M_1, 1 row for NMOS M_2, 1 row for NMOS M_3, 3 rows for PMOS M_4).

Two prototypes of the IPC have been designed. In the first one, the H-bridge was optimized for low conduction losses (i.e., high current capabilities), while in the second one, it was optimized for high switching frequencies (i.e., up to 10 MHz, for use with power inductors manufactured on silicon). The width W_n of an NMOS in the first prototype is equal to 95 mm (i.e., 38 cells $\times$ 50 fingers $\times$ 50 µm), while in the second prototype, it is equal to 70 mm (i.e., 112 cells $\times$ 25 fingers $\times$ 25 µm). The characteristics of the H-bridge of both prototypes were compared to these of the commercially available LTC3440 from Linear Technology, and the results are summarized in Table 5.1.

Table 5.1: Electrical characteristics comparison of H-bridges.

IC	$R_{\mathrm{DS(on)}(n)}$	$R_{\mathrm{DS(on)}(p)}$	$V_{\mathrm{DS(on)}}$	$I_{\mathrm{D(max)}}$	H-Bridge Area
LTC3440	0.190 Ω	0.220 Ω	120 mV	600 mA	2.79 mm^2
IPC1	0.021 Ω	0.023 Ω	50 mV	2000 mA	1.56 mm^2
IPC2	0.032 Ω	0.035 Ω	70 mV	2000 mA	2.08 mm^2

The complete layout of the second prototype is shown in Figure 5.46. Only the metal layers are shown. The power part, situated in the middle of the design, is laid out in such a way that each power path provides a bonding pad at each side end (i.e., left and right side end). This divides by two the current stress applied to the bond wires and to the internal metal interconnections in the power path. The metal slotting rules, which must be respected to avoid thermal issues during wafer processing and electromigration failures during normal operation of the IPC, are also shown in this layout view.

5.3.2 Power Transistors Gate Drivers

In the first prototype of the IPC, the power transistors in the H-bridge were sized in such a way that the conduction losses are minimized. Therefore, most of the power part area was consumed by the power transistors themselves. Only a reduced area was available for their gate drivers, thus providing a low drive strength. Indeed, the highest possible switching frequency was limited to 1 MHz.

In the second prototype of the IPC, the power transistors in the H-bridge were laid out differently. The goal was to develop a H-bridge layout (i.e., power transistors

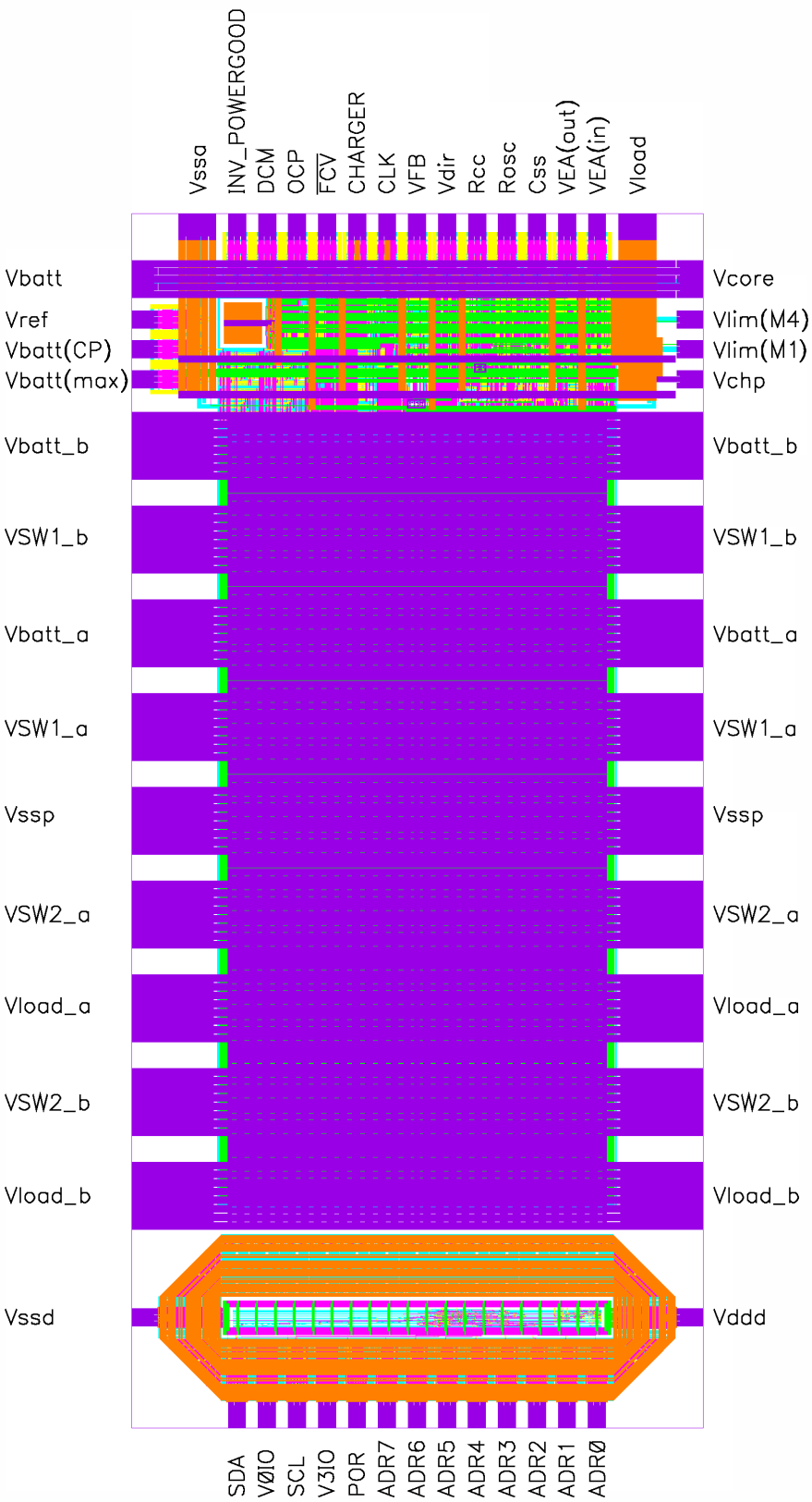

Figure 5.46: Complete layout overview of the second IPC prototype. Only the metal layers are shown. Three zones can be distinguished. The analog electronic part is located at the top. The digital electronic part is located at the bottom. The power electronic part is located between the analog and digital parts.

with their gate drivers) in which the gate drivers can switch the power transistors at frequencies up to 10 MHz. To reach this objective, the gate resistance of the power MOSFETs has been reduced and the drive strength of the gate drivers increased. The first was reached by reducing the length of the gate fingers (i.e., 50 µm in the IPC1, 25 µm in the IPC2), by using gate contacts at both ends, and by placing a gate driver directly aside each power transistor cells. The second was reached by increasing the number of cascaded inverters in the driver chain (i.e., 2 inverters in the IPC1, 4 inverters in the IPC2) to improve the drive strength. The schematic of the drivers developed for the second prototype of the IPC is shown in Figure 5.42.

At switching frequencies above 1 MHz, high dV/dt and dI/dt are achieved during the transients, especially at the potential point V_{SW1} and V_{SW2} shown in Figure 4.15 and in Figure 5.42. In the simulations, issues due to the Miller effect have been observed. It is caused by the parasitic gate-drain capacity C_{GD} of the power transistors. This effect consists in a retroaction between the drain voltage and the applied gate voltage. For example, when considering that M_1 is turned off and M_2 turned on: if M_2 is then switched off and if M_2 is switched on very rapidly, the potential V_{SW1} is pulled high very strongly, thus also pulling the gate of M_2 ($V_{G(M2)}$) high, because C_{GD} does not have enough time to charge. During the time needed by C_{GD} to charge, M_2 sinks current because $V_{GS(M2)}$ is higher than the threshold voltage V_{th} (e.g., up to 12 A have been reached in simulation). To solve this issue appearing with strong gate drivers, it was decided to design them asymmetrically. In other words, this means that the gate drivers switch off the power transistors very rapidly, but they switch it back on more slowly, so that the capacitor C_{GD} has enough time to load itself without pulling the gate voltage of the complementary power transistor above the threshold voltage V_{th} (i.e., $V_{GS(M2)}$ is lower than the threshold voltage V_{th} at every moment of the switching transient, when M_2 is wanted to be turned off).

In the design of the IPC — especially in the design of the second prototype — the layout of the power part was very challenging, but all the encountered issues were solved per design and the simulation results have confirmed the validity of the implemented solutions. The area specific resistance (ASR) of the power MOSFETs used in the H-bridge is $4.76\,\mathrm{m\Omega \cdot mm^2}$ for the NMOS, and $15.6\,\mathrm{m\Omega \cdot mm^2}$ for the PMOS. The bulk contacts, which have been sized in such a way that they can carry the full drain current of the considered MOSFET, were taken into account for the computation of these ASR values. The experimental results to the simulated design are presented in the Chapter 6.

Chapter 6

Bidirectional DC-DC Converter Prototyping

In this chapter, the theoretical concepts introduced in Chapter 4 and the design techniques described in Chapter 5 are demonstrated experimentally in two separate DC-DC converter prototypes (i.e., the IPC1, containing only the power part ; and the IPC2, containing all the parts presented in Chapter 5). The measurement results, as well as the experimental environment used for the experiments, are presented.

6.1 First Prototype (IPC1)

The first prototype of the IPC (i.e., IPC1) was manufactured in summer 2005. The design included the power supply for the core voltage, the power H-bridge, and the gate drivers with dynamic MOSFET sizing ability. No PWM regulation unit was implemented in the IPC1. The objectives of this first run were to validate the ESD protection structures implemented in the I/O pads, to get experience in process variations and layout mismatches for the development of Monte-Carlo simulation models, and to demonstrate the improvement in efficiency provided by dynamic MOSFET sizing. A photography of the manufactured IPC1 is shown in Figure 6.1.

The ESD protection structures are necessary to protect the sensing inputs (e.g., V_{FB}, V_{dir}, $V_{\mathrm{EA(in)}}$, $V_{\mathrm{EA(out)}}$; see Figure 5.46) against electrostatic discharges, which can be destructive for the gate oxide of the MOSFETs. Monte-Carlo simulation models were developed for analyzing the influences of the process variations and the layout mismatches on the performances of the analog units (e.g., voltage reference, current mirror). The dynamic MOSFET sizing function has been implemented only in the IPC1, because of a poor absolute gain in efficiency of less than 4% that was measured, compared to the absolute gain in efficiency of more than 20% obtained from the simulation results presented in Section 4.2.3. However, this poor gain in efficiency was due to a malfunction in the logic level shifters driving the power MOSFET gate drivers. At voltages below 1.8 V, the logic level shifters (see Figure 5.36) developed for the IPC1 switch slowly. Therefore, the transition time during which both transistors M_5 and M_6 are turned on is longer, thus dissipating more power, because of the shoot-through current flowing through them. The design of the logic level shifters was corrected for the IPC2 by using low-V_{th} transistors for M_1, M_2, M_5, and M_6, to avoid this speed limitation at low voltages (see Figure 5.37).

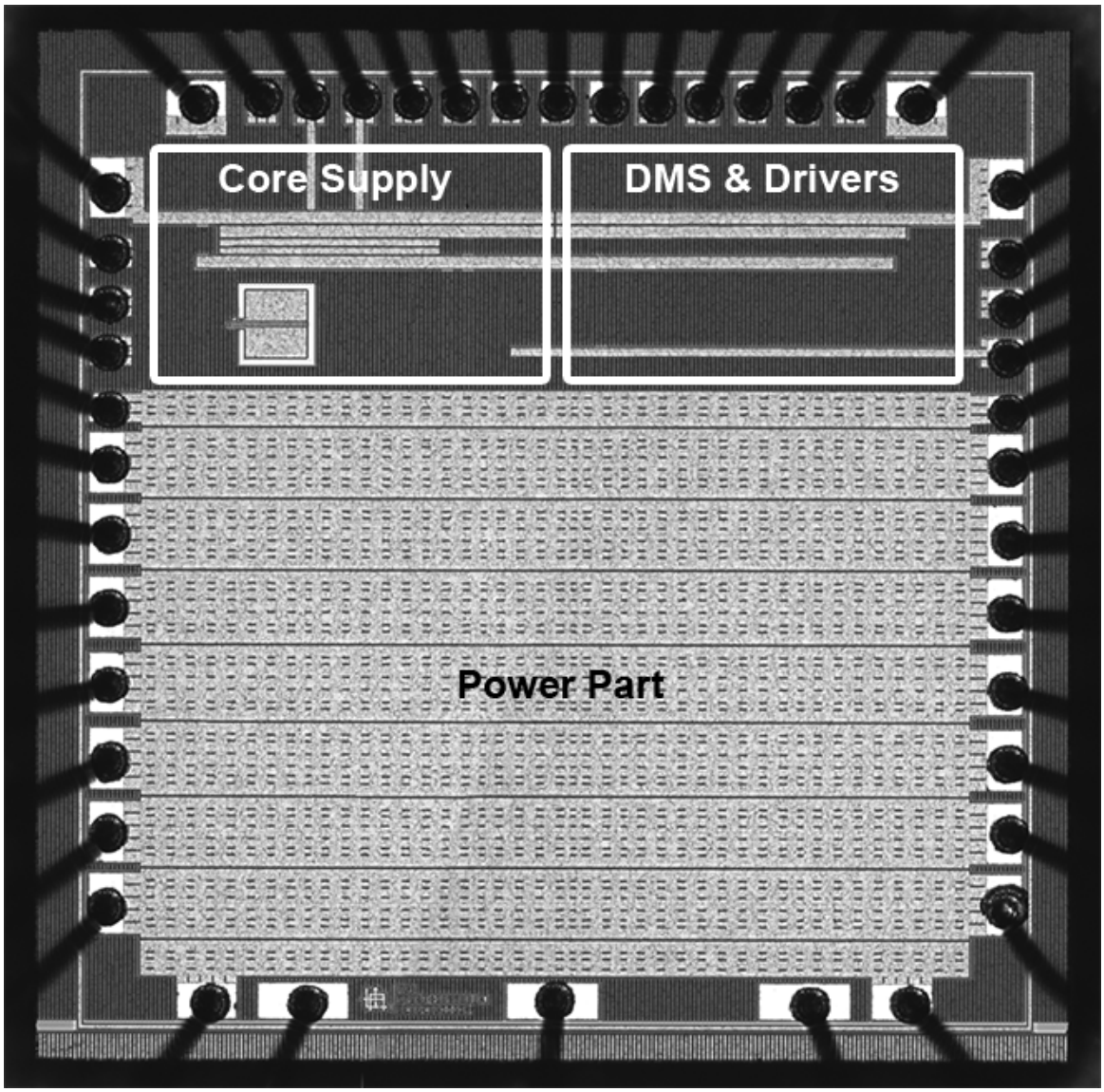

Figure 6.1: Photography of the die of the IPC1.

6.1.1 Test Board for the First Prototype

The block diagram of the test board used to characterize the IPC1 is shown in Figure 6.2. The IPC1 was supplied with the battery voltage V_{batt}. The driver inputs of the H-bridge (i.e., DRV_1, DRV_2, DRV_3, DRV_4) were switched by a 2 MHz PWM signal generated by the TPS43000 [88], a DC-DC controller from Texas Instrument providing buck or boost regulation, with synchronous rectification. However, the TPS43000 provides only two complementary PWM signals (i.e., one for the power PMOS, and one for the power NMOS). Therefore, the complete H-bridge transistors could not be driven simultaneously (i.e., no buck-boost operation was possible with this PWM controller). For the tests, switches were implemented on the test board, so that it was possible to chose manually between buck operation (i.e., when DRV_1 and DRV_2 are driven) and boost operation (i.e., when DRV_3 and DRV_4 are driven).

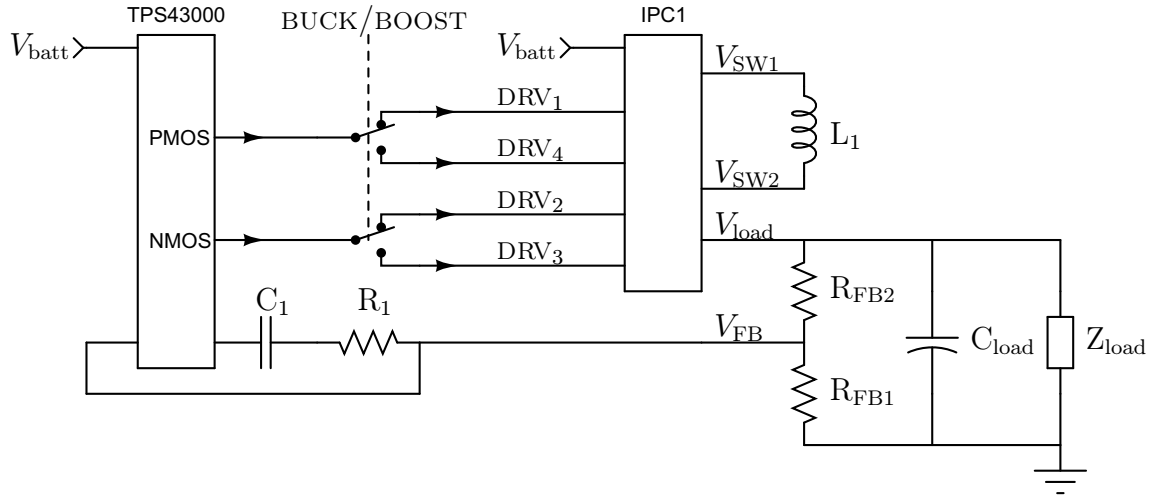

Figure 6.2: Block diagram of the test board developed for the IPC1 in buck mode configuration (i.e., when DRV_1 and DRV_2 are driven by the TPS43000). Pull-down resistors on the DRV_1, DRV_2, DRV_3, and DRV_4 lines are needed to ensure the proper power switch configuration when these lines are not connected to the TPS43000 PWM controller.

6.1.2 Experimental Results of Dynamic MOSFET Sizing

The theory of the dynamic MOSFET sizing principle was presented in Section 4.2. It was only implemented in the IPC1. The experimental results were obtained with the circuit depicted in Figure 6.2 and configured as a synchronous buck converter (the topology of a typical synchronous buck converter was shown in Figure 4.7). The TPS43000 was used in the buck mode at its highest switching frequency of 2 MHz [88]. The output voltage V_{load} was 0.9 V and the input voltage V_{batt} was 1.8 V. The light-load output current I_{load} was 1% the nominal current of 2000 mA (i.e., 20 mA).

In this synchronous buck mode configuration, the switching speed of the level shifters does not limit the conversion efficiency η. The level shifters connected to the V_{load} side were driven by a constant logic signal and therefore did not switch (i.e., DRV_3 and DRV_4 were pulled down, so that the NMOS M_3 was turned off and the PMOS M_4 was turned on). Only the level shifters connected to DRV_1 and DRV_2 were switching at 2 MHz, but since these level shifters were supplied by the 1.8 V V_{batt} voltage, the voltage level was sufficient to ensure that the speed limitation does not occur. The power losses in all four level shifters could therefore be neglected in this configuration.

Table 6.1 shows the measurement results, which confirm a 15% of absolute improvement in conversion efficiency when the transistor's width sizing factor β is decreased to 0.053 at a light-load operating condition. In other words, this signifies that in mobile systems, a gain of 15% in operating time can be achieved. At low β values, the measured efficiency is lower than the simulated efficiency because of the losses in the ESD protection structures connected to the driver inputs (i.e., DRV_1, DRV_2, DRV_3, DRV_4). These ESD structures have parasitic capacities in the range of 2 pF to 8 pF per input pad. With a fully monolithic integration (i.e., with the PWM controller and the power H-bridge on the same silicon die), the losses due to the ESD protection structures located at the driver inputs can be avoided, and the simulated efficiency can be approached.

Table 6.1: Efficiency measurements obtained with DMS at a 2 MHz PWM frequency.

β	0.053	0.105	0.421	0.842	1.000
Simulated η	81.4%	80.2%	72.8%	64.7%	62.1%
Measured η	77.2%	74.5%	67.8%	63.8%	61.9%

The experimental results show good accordance to the simulation results (see Table 6.1). In contrary to PFM modulation, the combination of PWM and dynamic MOSFET sizing adds no voltage ripple to the output voltage V_{load} in case of a light-load condition. Dynamic power MOSFET sizing will have an important impact on enabling monolithic integrated high-frequency DC-DC converters with hybrid integrated on-chip power inductors.

6.2 Second Prototype (IPC2)

The second prototype of the IPC (i.e., IPC2) was manufactured in winter 2006/2007. The design included all the units represented in the block diagram in Figure 3.1: the power supply for the core voltage (with a process independent voltage reference), the power converter (with redesigned layout of the power H-bridge for an operating frequency up to 10 MHz), the MOSFET gate drivers (with high speed level shifters operating at voltages down to 1.2 V), the sensors (e.g., current sensors for overcurrent protection), the PWM controller (with the continuous regulation loop), and the digital I^2C interface (tested successfully with a microcontroller, but currently not used in the IPC2 for setting up the DC/DC converter itself).

An overview of the pinout used for the IPC2 in a JLCC-68 package is shown in Figure 6.3. The description of the function of each pin is given in Table 6.2. Some pins are dedicated to testing purposes, and are therefore followed by the mention *tests only*. A photography of the die of the IPC2 is shown in Figure 6.4.

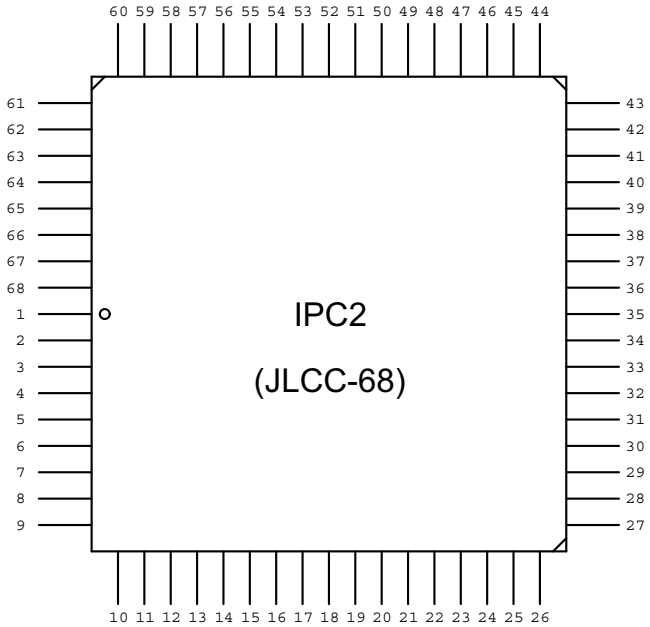

Figure 6.3: Pinout of the IPC2 in JLCC-68 package.

Table 6.2: Pinout of the IPC2 in JLCC-68 package shown in Figure 6.3.

Pin No.	Pin Name	Pin Function
1	V_{SSP}	Ground connection of the power part
2	$V_{\mathrm{SW2\_a}}$	Inductor connection of the power part (V_{SW2})
3	$V_{\mathrm{load\_a}}$	Load and charger connection of the power part (V_{load})
4	$V_{\mathrm{SW2\_b}}$	Inductor connection of the power part (V_{SW2})
5	$V_{\mathrm{load\_b}}$	Load and charger connection of the power part (V_{load})
6	V_{SSD}	Ground supply connection of the digital part
7	V_{SSD}	Ground supply connection of the digital part
8	V_{SSD}	Ground supply connection of the digital part
9	GND	Ground connection of the cavity of the package
10	GND	Ground connection of the cavity of the package
11	NC	Internally not connected
12	SDA	Serial data line of the I^2C interface
13	V_{0IO}	Ground connection of the digital I/O of the I^2C interface
14	SCL	Serial clock line of the I^2C interface
15	V_{3IO}	Positive supply connection of the digital I/O of the I^2C interface
16	POR	Power-on reset of the I^2C interface
17	ADR_7	Address line 7 of the I^2C interface
18	ADR_6	Address line 6 of the I^2C interface
19	ADR_5	Address line 5 of the I^2C interface
20	ADR_4	Address line 4 of the I^2C interface
21	ADR_3	Address line 3 of the I^2C interface
22	ADR_2	Address line 2 of the I^2C interface
23	ADR_1	Address line 1 of the I^2C interface
24	ADR_0	Address line 0 of the I^2C interface
25	NC	Internally not connected
26	GND	Ground connection of the cavity of the package
27	GND	Ground connection of the cavity of the package
28	V_{DDD}	Positive supply connection of the I^2C interface
29	V_{DDD}	Positive supply connection of the I^2C interface
30	V_{DDD}	Positive supply connection of the I^2C interface
31	$V_{\mathrm{load\_b}}$	Load and charger connection of the power part (V_{load})
32	$V_{\mathrm{SW2\_b}}$	Inductor connection of the power part (V_{SW2})

Table 6.2: Pinout of the IPC2 in JLCC-68 package shown in Figure 6.3. (continued)

Pin No.	Pin Name	Pin Function
33	$V_{\text{load\_a}}$	Load and charger connection of the power part (V_{load})
34	$V_{\text{SW2\_a}}$	Inductor connection of the power part (V_{SW2})
35	V_{SSP}	Ground connection of the power part
36	$V_{\text{SW1\_a}}$	Inductor connection of the power part (V_{SW1})
37	$V_{\text{batt\_a}}$	Battery connection of the power part (V_{batt})
38	$V_{\text{SW1\_b}}$	Inductor connection of the power part (V_{SW1})
39	$V_{\text{batt\_b}}$	Battery connection of the power part (V_{batt})
40	V_{CP}	Output voltage of the charge pump
41	$V_{\text{lim(M1)}}$	Current sink used to define the maximum allowed $V_{\text{DS(on)}}$ over M_1 to protect it against overcurrent (tests only)
42	$V_{\text{lim(M4)}}$	Current sink used to define the maximum allowed $V_{\text{DS(on)}}$ over M_4 to protect it against overcurrent (tests only)
43	V_{core}	Output of the core supply voltage (tests only)
44	V_{load}	Load and charger connection (supply for the level shifters)
45	V_{load}	Load and charger connection (supply for the level shifters)
46	$V_{\text{EA(in)}}$	Pin connected to the input of the error amplifier
47	$V_{\text{EA(out)}}$	Pin connected to the output of the error amplifier
48	C_{SS}	Connection of the capacitor defining the soft-start startup time
49	R_{osc}	Connection of the resistor for adjusting the switching frequency of the PWM oscillator
50	R_{CC}	Connection of the resistor defining the current value used for charging the battery during the constant current charging phase
51	V_{dir}	Sensing input used to detect the presence of a battery charger on the load side
52	V_{FB}	Sensing input used to regulate the load voltage during the discharging phase
53	CLK	Digital clock output of the PWM oscillator (tests only)
54	CHARGER	Digital output that indicates if a charger has been detected (tests only)
55	$\overline{\text{FCV}}$	Digital input to force constant voltage charging (tests only)

Table 6.2: Pinout of the IPC2 in JLCC-68 package shown in Figure 6.3. (continued)

Pin No.	Pin Name	Pin Function
56	OCP	Digital input to disable the overcurrent protection (tests only)
57	DCM	Digital input to disable discontinuous conduction mode operation (tests only)
58	INV-POWERGOOD	Digital input to invert the internal POWERGOOD signal (tests only)
59	V_{SSA}	Ground connection of the analog part
60	V_{SSA}	Ground connection of the analog part
61	V_{batt}	Positive power supply connection for the analog part
62	V_{ref}	Output of the reference voltage (tests only)
63	$V_{\mathrm{batt(CP)}}$	The internal charge pump starts if the voltage sensed by this pin is below the reference voltage V_{ref}
64	$V_{\mathrm{batt(max)}}$	The voltage sensed by this pin is used to regulate the battery voltage during the charging process
65	$V_{\mathrm{batt\_b}}$	Battery connection of the power part (V_{batt})
66	$V_{\mathrm{SW1\_b}}$	Inductor connection of the power part (V_{SW1})
67	$V_{\mathrm{batt\_a}}$	Battery connection of the power part (V_{batt})
68	$V_{\mathrm{SW1\_a}}$	Inductor connection of the power part (V_{SW1})

The objectives of this second run were to validate the continuous voltage regulation loop (see Section 4.3) and the automatic charger plug/unplug detection, which is essential for the bidirectional operation of the IPC (see Section 4.1).

6.2.1 Test Board for the Second Prototype

The printed circuit board developed for testing and characterizing the IPC2 is shown in Figure 6.5. The schematic of this printed circuit board is given in Figure 6.6.

For the tests, a battery and a DC power supply can be connected to the two orange plugs shown in the bottom left in Figure 6.5. The load and the battery charger must be connected to the orange plug situated in the bottom right of the test board. The linear regulator in the TO-3 package with heat sink is used to provide the V_{batt} voltage for the tests. This is done to replace the battery and to overcome the constraint of recharging it when performing endurance tests at high currents. The Schottky diodes were implemented for the first tests only, to protect the power transistors in the H-bridge against overcurrent in case of a malfunction in the anti-crossconduction logic unit. Since the anti-crosscondution logic was performing as predicted in the simulations, the Schottky diodes were removed. They were not used for the test performed hereafter.

A Microchip PIC 16F628A microcontroller was used to test the digital I^2C interface. The role of the microcontroller is to transmit an address to an analog multiplexer

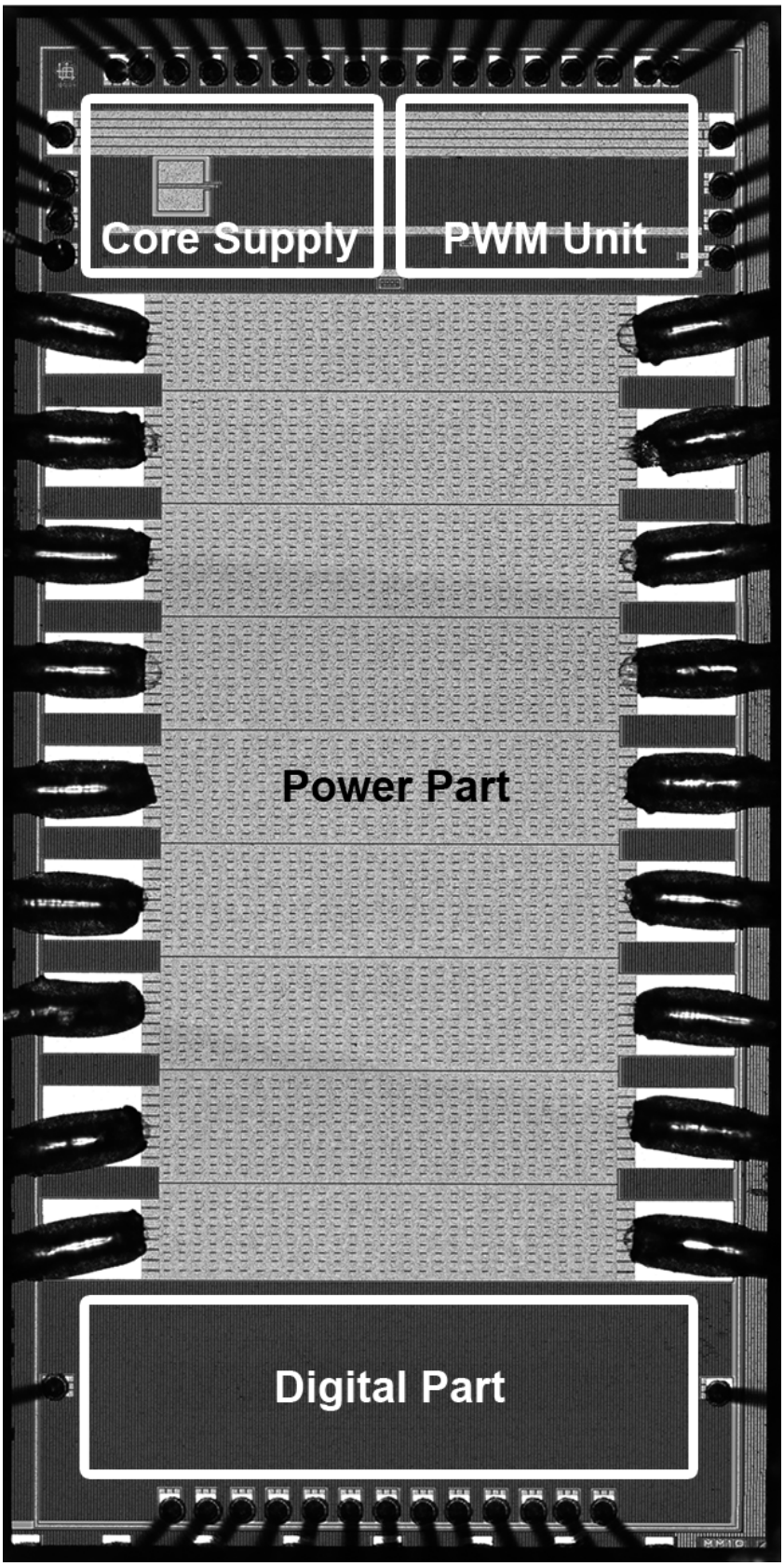

Figure 6.4: Photography of the die of the IPC2. The power pads with the 75 µm aluminum bond wires (wedge bonds) can be clearly distinguished from the signal pads with the 25 µm gold bond wires (ball bonds).

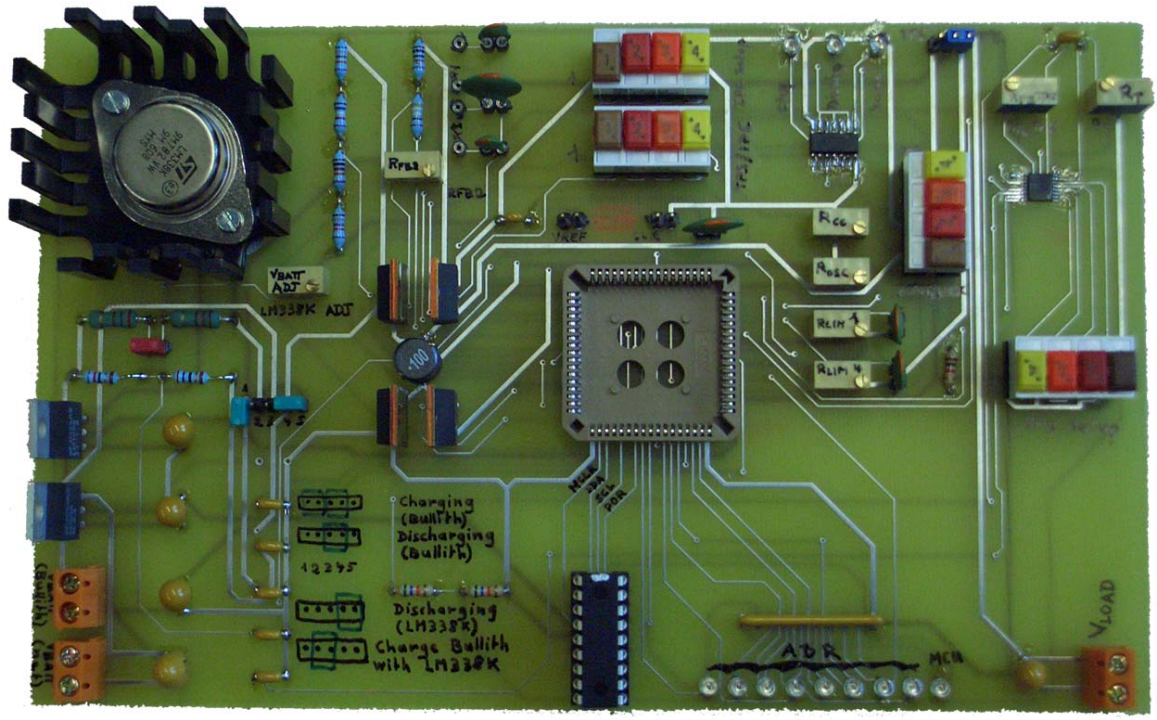

Figure 6.5: Test board developed for the IPC2.

implemented in the IPC2, thus selecting the analog signal to be output on a special test pin called V_{test} (not implemented in the manufactured IPC2, but shown previously in Figure 5.40). To control whether the digital I^2C interface is performing as expected and whether the multiplexer is getting the right address from the microcontroller, each bit of the 8-bit address value transmitted to the multiplexer is connected to an output driver pad. These driver pads are all connected to LEDs (see Figure 6.6), thus allowing a rapid visual validation of the transmitted address. The digital I^2C interface was successfully tested and has performed as expected from the simulations.

Finally, the commercial DC-DC controller TPS43000 from Texas Instruments was implemented on the test board to drive at least parts of the H-bridge of the IPC2 in case of a malfunction in the PWM regulation unit. The TPS43000 was not used in the measurement results presented hereafter, since the PWM unit of the IPC2 is performing as expected from the simulations.

6.2.2 Experimental Results of the Core Voltage Regulator

The core voltage regulator providing the V_{core} voltage of 1.8 V is essential for ensuring that the performances are independent of the V_{batt} voltage. If V_{batt} falls below 1.8 V, the 200 MHz 2-phase charge pump boosts internally V_{batt}, thus ensuring that V_{core} stays at 1.8 V as long as V_{batt} does not fall below 1.2 V. Tests accomplished on the IPC2 have shown that the core voltage regulator performs as predicted in the simulations. This is illustrated in the oscilloscope plots shown in Figure 6.7, where V_{batt} was decreased with the potentiometer `R_LIN_REG` shown in Figure 6.6. The V_{core} voltage remained constant during the transient response, when the charge pump started.

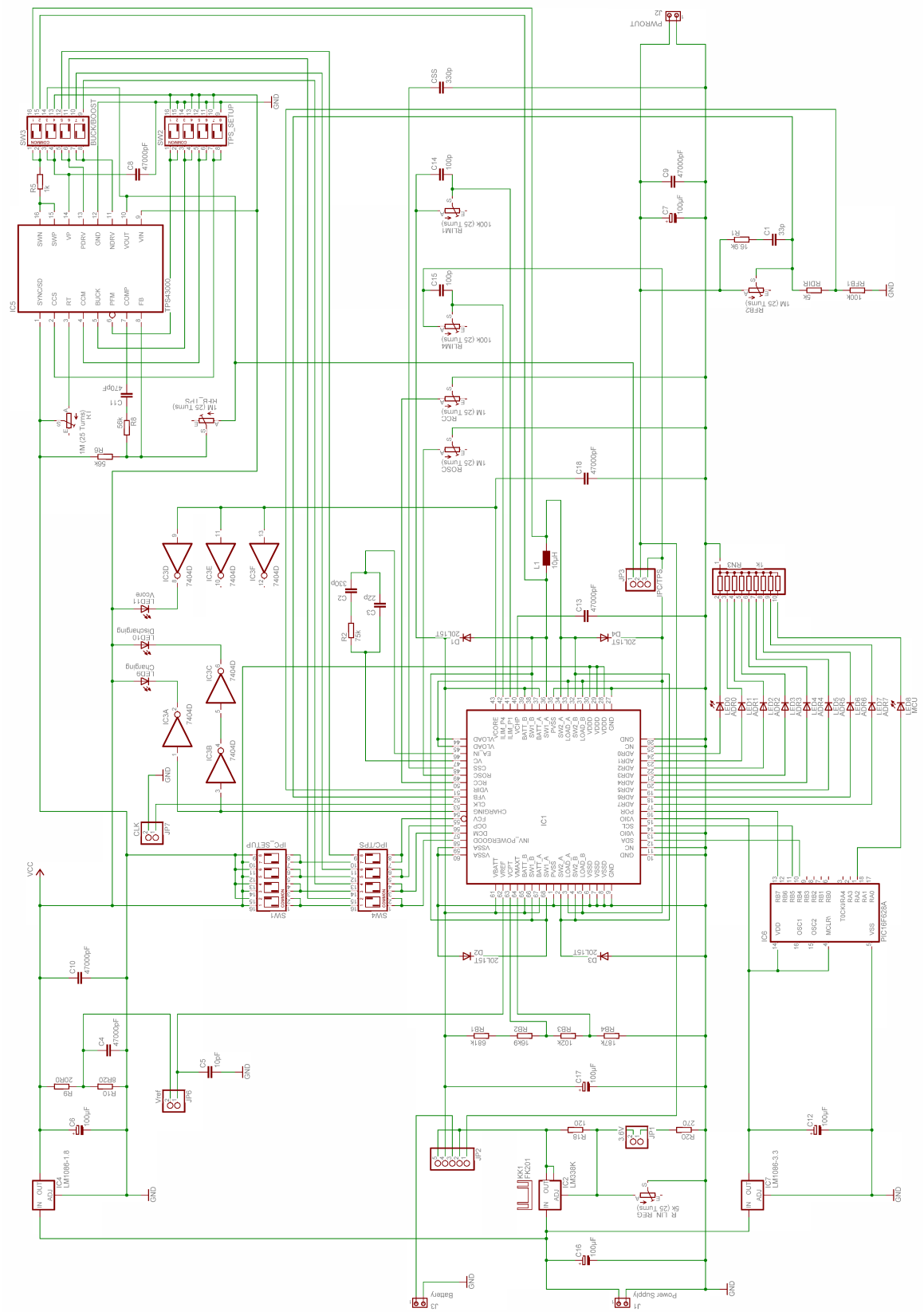

Figure 6.6: Schematic of the printed circuit board designed for testing the IPC2. The TPS43000 and the Schottky diodes were foreseen to test the H-bridge as a standalone unit, but they were not used in the measurements shown hereafter.

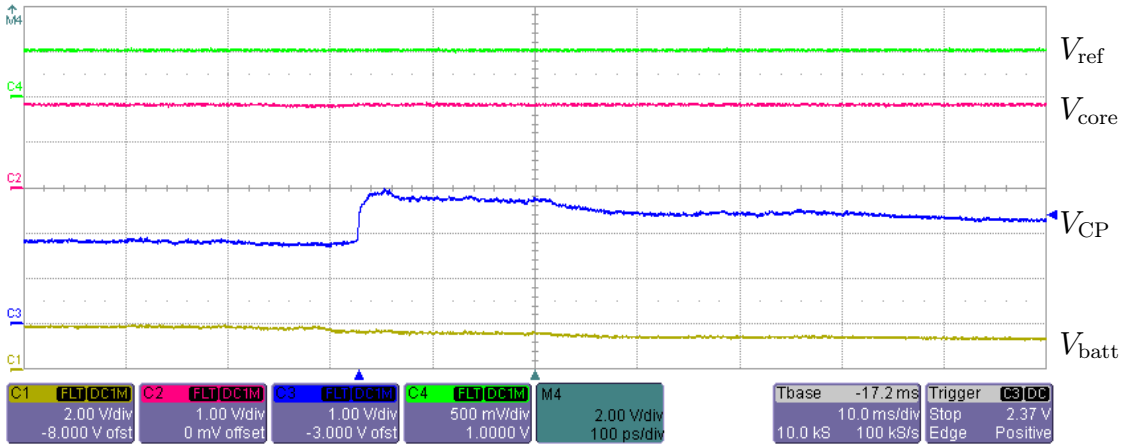

Figure 6.7: Transient response of V_{core} when V_{batt} falls and the charge pump starts.

6.2.3 Experimental Results of the PWM Regulation

The PWM regulation unit was implemented in the IPC2 as described in Section 5.1.3. The oscillograms in Figure 6.8, Figure 6.9, and Figure 6.10 present the measurements for a 56 Ω load, a V_{load} of 1.8 V, and a decrease in V_{batt} from 2.1 V to 1.6 V. The experimental results presented hereafter agree well with the theory presented in Section 4.3. They were obtained during the discharging of the battery. Similar results can be obtained during charging of the battery, since the same PWM regulation unit is used in both modes.

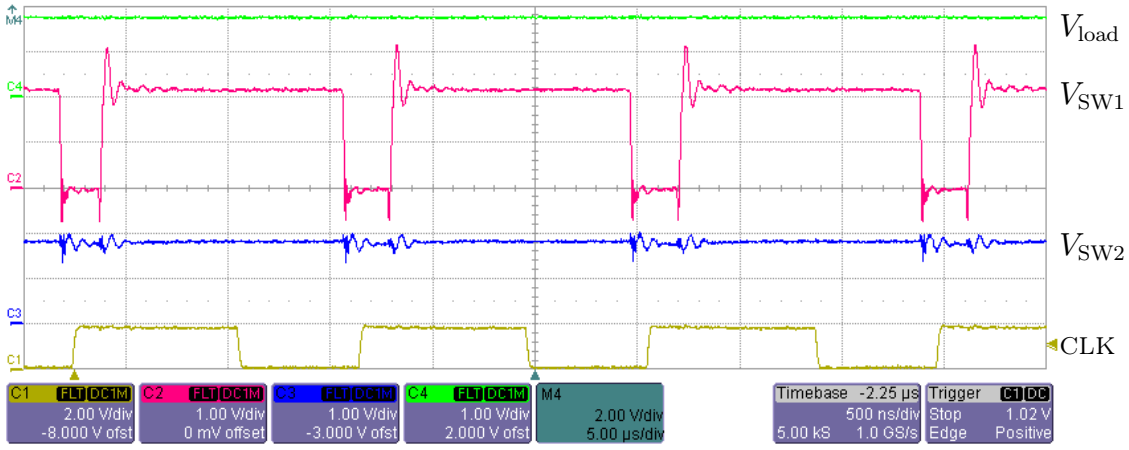

Figure 6.8: Oscillogram of the IPC2 in buck mode ($V_{batt} = 2.1$ V, $V_{load} = 1.8$ V).

To achieve a high power conversion efficiency, the IPC2 uses synchronous rectification. An anti-crossconduction logic adds a dead-time t_{delay} between the turn-off of the rectifying transistor (M_2) and the turn-on of the energizing transistor (M_1) (see Section 5.2.1). The delay was set per design to 4 ns, without considering the interconnection parasitics. It is applied to the PWM signal and depends only on the V_{core} voltage. In other words, t_{delay} is independent of V_{batt} and V_{load}, thus ensuring a minimum dead-time in any operating condition. Experimentally, the total dead-time measured in Figure 6.11 is 6 ns, because of the interconnection parasitics.

The IPC2 is designed for a nominal operating frequency of 1 MHz, but the design is able to operate at frequencies up to 10 MHz. However, the double layer printed circuit board shown in Figure 6.5 is designed for testing the IPC2 by adjusting discrete

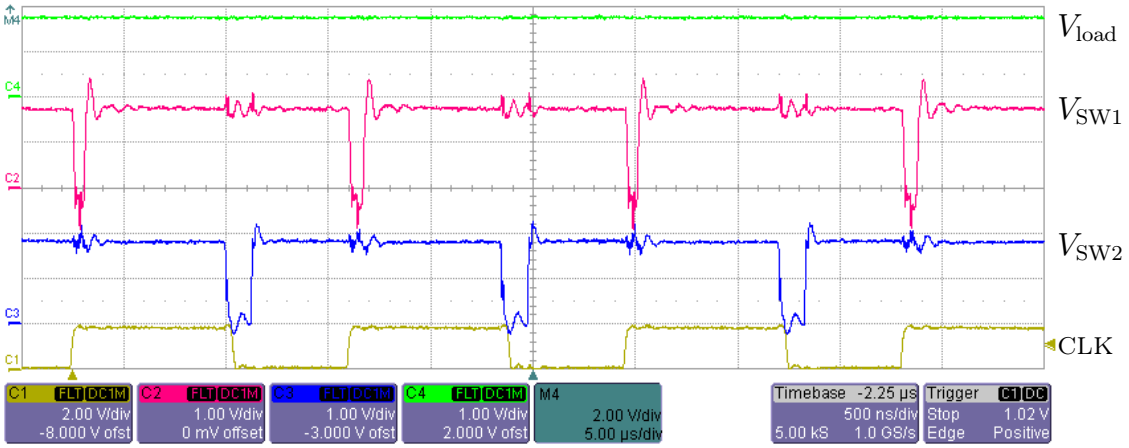

Figure 6.9: Oscillogram of the IPC2 in buck-boost mode ($V_{batt} = 1.8\,V$, $V_{load} = 1.8\,V$).

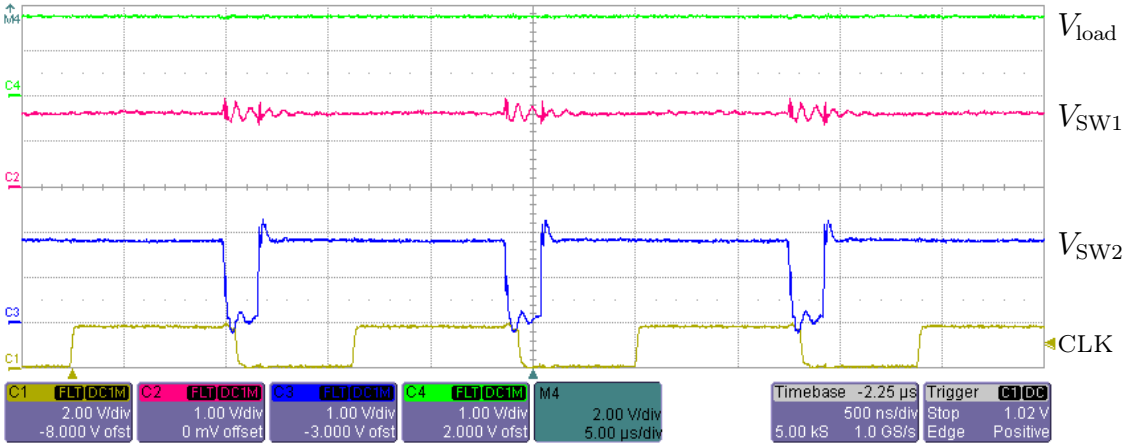

Figure 6.10: Oscillogram of the IPC2 in boost mode ($V_{batt} = 1.6\,V$, $V_{load} = 1.8\,V$).

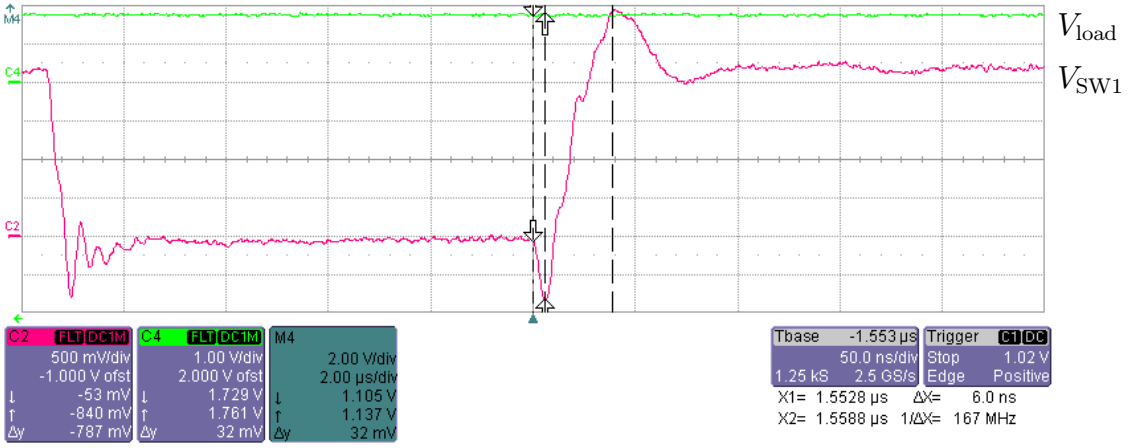

Figure 6.11: Oscillogram of the IPC2 in buck mode showing the use of synchronous rectification ($V_{batt} = 2.1\,V$, $V_{load} = 1.8\,V$).

mounted switches and potentiometers. For this, longer PCB tracks are needed which, however, generate more electromagnetic interferences (EMI). Due to the additional track lengths, the parasitics (i.e., resistance, inductance, capacitance) are increased, and important harmonics are therefore generated in the power and signal paths, thus limiting the maximum switching frequency. The oscillogram in Figure 6.12 shows the IPC2 operating in synchronous buck mode at a PWM switching frequency of 5 MHz.

Figure 6.12: Oscillogram of the IPC2 in buck mode ($V_{batt} = 1.7\,V$, $V_{load} = 1.0\,V$, $f_{osc} = 5\,MHz$). The interferences are due to the long signal tracks on the test PCB.

The oscillogram in Figure 6.13 shows the startup of the IPC2 with a $56\,\Omega$ load and with a V_{load} voltage of 1.8 V. The battery voltage V_{batt} is 2.3 V, thus forcing the IPC2 to operate in buck mode once the steady-state operation mode is reached. The startup begins with a short buck phase (i.e., M_1 and M_2 are switched on the V_{SW1} side), because the internal control voltage V_{CI} is still low. Since the sensed feedback voltage V_{FB} is much too low yet, V_{CI} is rising (see Figure 4.21). After this buck phase, a boost phase is entered (i.e., M_3 and M_4 are switched on the V_{SW2} side). Once V_{load} reaches 1.8 V, V_{CI} drops, the converter enters again the buck mode, and it reaches steady-state operation. The overall startup time is less than 4 ms with an output filter capacity C_{load} of 100 µF. The overshoot on the V_{load} voltage due to the startup of the regulation is around 6% of the nominal voltage (i.e, it is not higher than the 1.98 V specified in the accepted tolerance of ±10% by 1.8 V circuits).

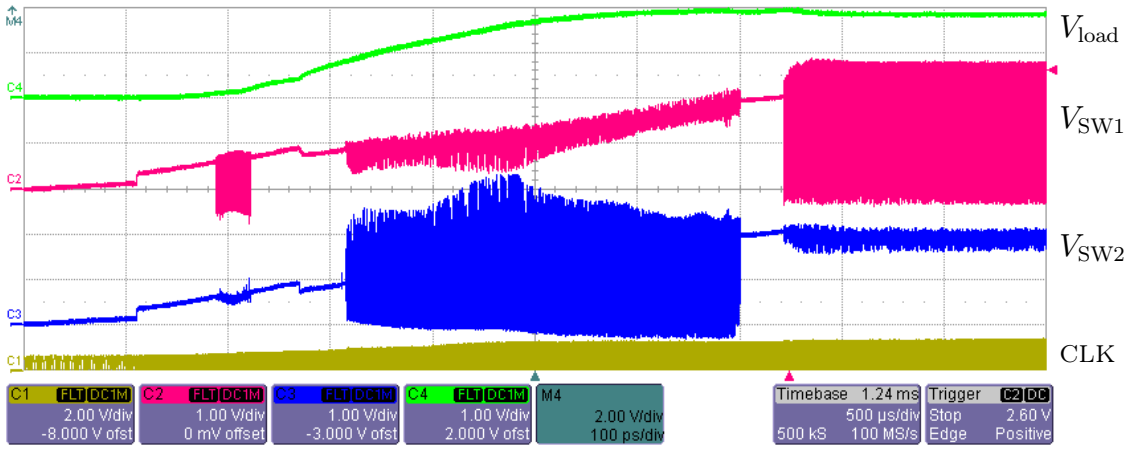

Figure 6.13: Oscillogram showing the soft-start of the IPC2 ($V_{batt} = 2.3\,V$, $V_{load} = 1.8\,V$). Due to the soft-start provided by the IPC2, the overshoot on the V_{load} voltage during the startup is strongly damped.

The conversion efficiency of the IPC2 was measured in each conversion mode (i.e., buck, buck-boost, boost). Power tests were performed with different resistive loads to vary the load current I_{load}. The regulated output voltage V_{load} was adjusted to 1.8 V. The input battery voltage V_{batt} was 3.0 V in the buck mode, 1.8 V in the buck-boost mode, and 1.4 V in the boost mode. The efficiency curves shown in Figure 6.14 were computed from the measured input/output currents and voltages.

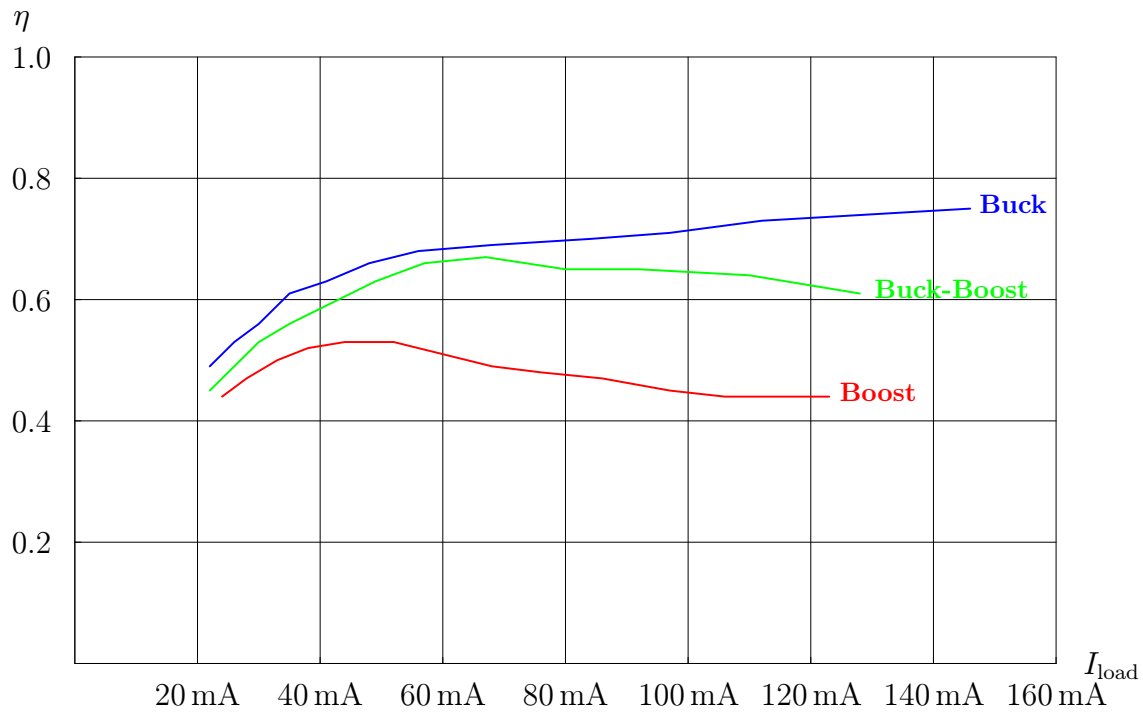

Figure 6.14: Experimental efficiency of the IPC2 in buck mode (3.0 V→1.8 V), buck-boost mode (1.8 V→1.8 V), and boost mode (1.4 V→1.8 V) at a PWM frequency f_{osc} of 1 MHz.

The maximum efficiency reached by the IPC2 during the power tests performed on the printed circuit test board was around 77%. The maximum output power delivered by the IPC2 to a connected load was around 550 mW. The maximum output current at a given output voltage was around 150 mA. This is much lower than the maximum current of 2000 mA for which the IPC2 was designed. This is not due to a nonideal design of the IPC2 itself, but it is due to a nonadapted packaging method[5] (i.e., wire bonding instead of flip-chip bumping) and due to the low quality of the test board (i.e., thin copper 2-layer printed circuit test board without power planes). The printed circuit test board presented in Figure 6.5 was oversized to allow easy access to the different signals having to be sensed on it. However, conducting high currents over long resistive metal interconnections results in important power losses, and therefore in a reduced efficiency.

Further, during the packaging of the IPC2, the wedge bonds done on the power pads have shorted them to the die seal ring, as shown in the photography presented in Figure 6.15. Therefore, the bonding solution exposed in Section 3.3.3 could not be used for the prototype of the IPC2. Instead of the wedge bonded 100 µm aluminum bond wires, 4 parallel ball bonded 18 µm gold bond wires were used. Referring to Table 3.9 and Table 3.10, the 4 parallel 18 µm gold bond wires provide a resistivity of 22 mΩ/mm, where the 100 µm aluminum bond wire would have provided a resistivity of only 3.3 mΩ/mm.

[5]When using multi-project wafer (MPW) runs, only dies are provided. However, for flip-chip bumping, complete wafers are generally needed. Therefore, for prototyping, flip-chip bumping could not be used, since no packaging house was able to do flip-chip bumping in low volumes at die level for prototyping.

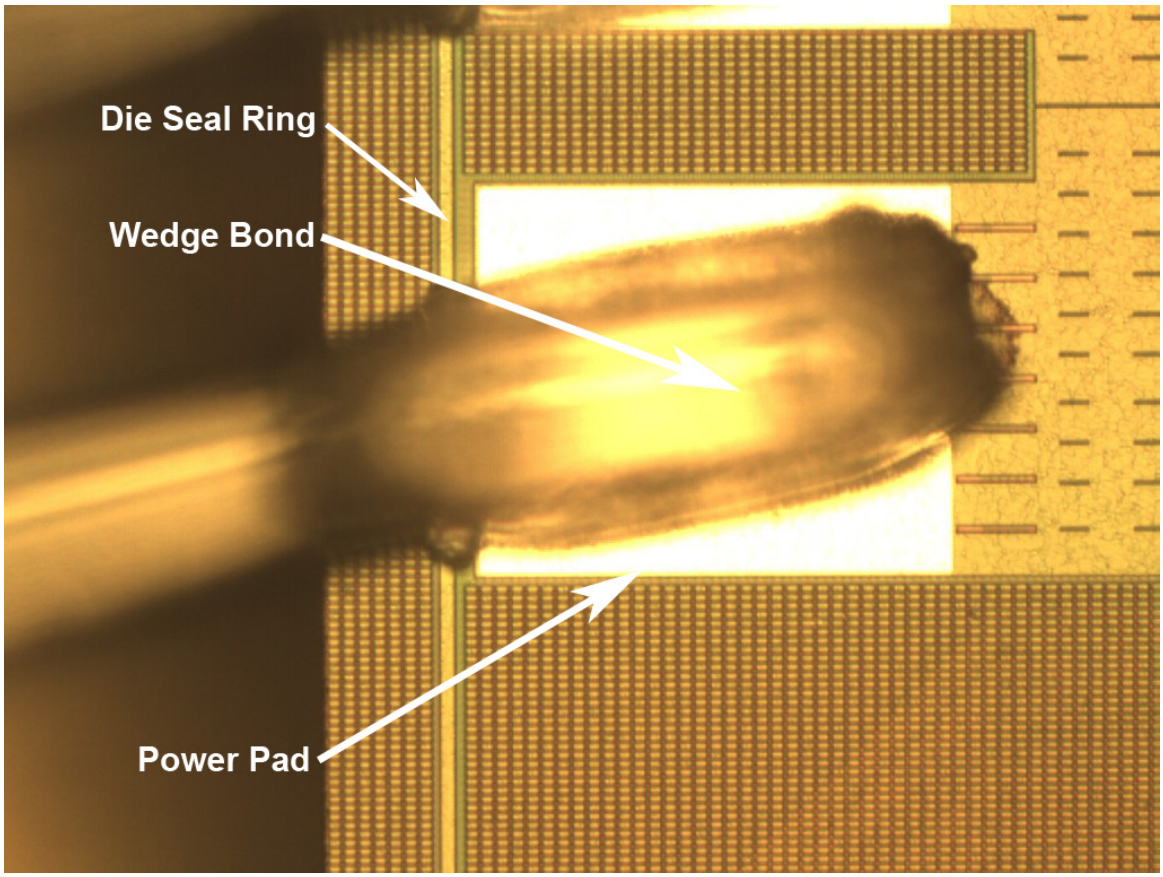

Figure 6.15: Die seal ring shorted to the power pads by the wedge bonds.

To understand the efficiency and the current limitations observed in Figure 6.14, the conduction power losses occurring in the power paths carrying high currents were investigated. Figure 6.16 illustrates the location of the conduction losses in the IPC2 when the inductor current I_{L1} flows through the NMOS M_3 in the power H-bridge. The conduction losses are due to the bond wires (P_{bw}), the metallization of the IC (P_{met}), and the $R_{DS(on)}$ of the power transistors ($P_{RDS(on)}$). The model of the conduction losses is based on the layout of the H-bridge shown in Figure 5.45.

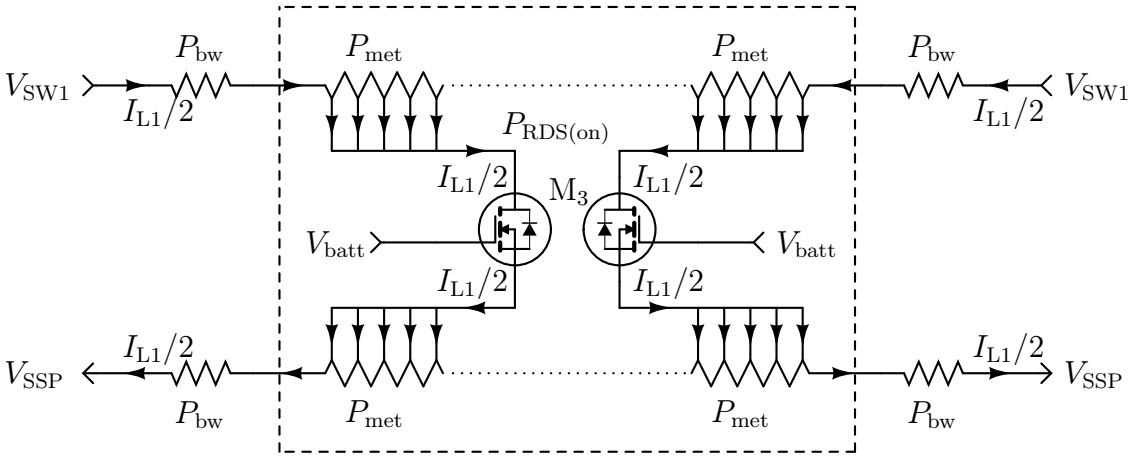

Figure 6.16: Model used to estimate the conduction losses in the IPC2.

The first source for conduction power losses in the IPC2 is the resistance R_{met} of the metallization of the IC. These conduction power losses are noted P_{met}. They can be computed by using the representation shown in Figure 6.17. The power transistor M_3 is composed of a total of m fingers. An approximation consists in considering that the input current $I_{L1}/2$ is equally distributed over all these m fingers.

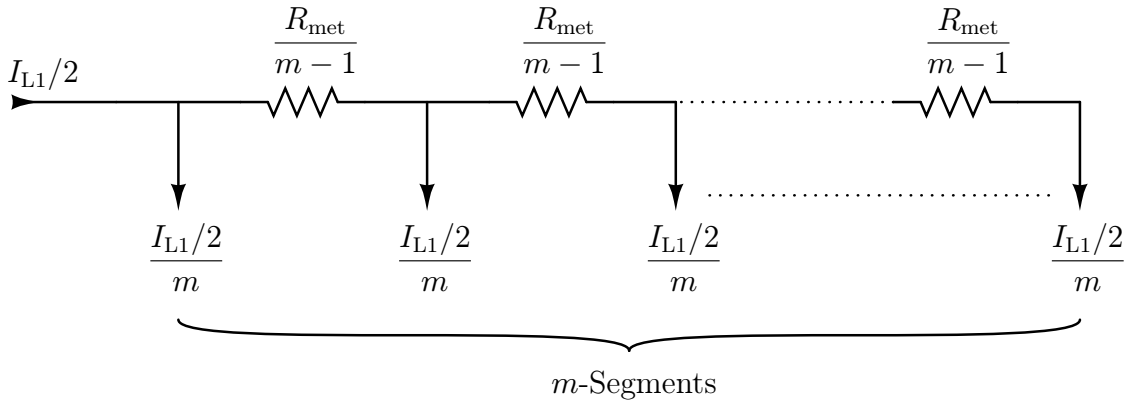

Figure 6.17: Model used to estimate the conduction losses in the metallization of the IPC2.

The conduction power losses P_{met} can therefore be written as the sum of decreasing currents each flowing through an additional elementary resistor:

$$\begin{aligned} P_{\text{met}} &= \frac{R_{\text{met}}}{m-1} \cdot \left(I_{L1}/2 - 1 \cdot \frac{I_{L1}/2}{m} \right)^2 \\ &\quad + \frac{R_{\text{met}}}{m-1} \cdot \left(I_{L1}/2 - 2 \cdot \frac{I_{L1}/2}{m} \right)^2 \\ &\quad + ... \\ &\quad + \frac{R_{\text{met}}}{m-1} \cdot \left(I_{L1}/2 - (m-1) \cdot \frac{I_{L1}/2}{m} \right)^2 \\ &= \frac{R_{\text{met}}}{m-1} \cdot \left(\frac{I_{L1}}{2} \right)^2 \cdot \sum_{i=1}^{m-1} \left(1 - \frac{i}{m} \right)^2 \end{aligned} \tag{6.1}$$

When the number of segments m is large, Equation (6.1) can be approximated by:

$$\lim_{m \to +\infty} (P_{\text{met}}) = \frac{1}{3} \cdot R_{\text{met}} \cdot \left(\frac{I_{L1}}{2} \right)^2 \tag{6.2}$$

In the case of the IPC2, R_{met} was measured to be 75 mΩ. Since there are four metallization paths to be considered (see Figure 6.16), the total conduction losses $\sum P_{\text{met}}$ occurring when the nominal current I_{L1} of 2 A flows is equal to:

$$\sum P_{\text{met}} = 4 \times \frac{1}{3} \cdot R_{\text{met}} \cdot \left(\frac{I_{L1}}{2} \right)^2 = 100\,\text{mW} \tag{6.3}$$

The second source of conduction power losses in the IPC2 is due to the on-resistance $R_{DS(on)}$ of the power transistors constituting the H-bridge. Table 6.3 shows the conduction power losses $P_{RDS(on)}$ occurring in the power NMOS M_3 at different

die temperatures when an inductor current I_{L1} of 2 A is flowing through the NMOS M_3 turned on by a gate-source voltage V_{GS} equal to V_{batt} (i.e., 1.8 V). Since only M_3 is considered in this analysis, the sum of the power losses ($\sum P_{RDS(on)}$) due to the conduction losses in the $R_{DS(on)}$ of M_3 are equal to the previously calculated $P_{RDS(on)}$.

Table 6.3: Conduction power losses simulated when 2 A flow in the NMOS M_3.

Silicon Die Temperature	$V_{DS(on)}$	$P_{RDS(on)}$
27°C	65 mV	130 mW
80°C	75 mV	150 mW
100°C	78 mV	156 mW
125°C	83 mV	166 mW
150°C	88 mV	176 mW

The third source of conduction power losses in the IPC2 is due to the resistance R_{bw} of the bond wires. The conduction power losses P_{bw} occurring in the bond wires are expressed by:

$$P_{bw} = \frac{\rho_{bw} \cdot l_{bw}}{S_{bw}} \cdot \left(\frac{I_{L1}}{2}\right)^2 \tag{6.4}$$

where l_{bw} is the length of the bond wire (in m), S_{bw} its section (in m^2), and ρ_{bw} its resistivity (in $\Omega \cdot m$). For 4 parallel connected 18 µm gold bond wires conducting a total current of 1 A at a temperature of 80°C, 225 mW of power are dissipated by conduction losses. For a 100 µm aluminum bond wire conducting 1 A at a temperature of 80°C, the conduction power dissipated by the bond wire would be only 35 mW.

Table 6.4 provides the calculated results of the conduction power losses occurring in the 18 µm gold bond wires used for carrying the current I_{L1} into and out of the IPC2 (i.e., P_{bw}), the conduction power losses occurring in the NMOS M_3 of the H-bridge (i.e., $P_{RDS(on)}$), and the conduction power losses occurring in the metallization of the integrated circuit itself (i.e., P_{met}). Based on these results, the conduction power losses with the 100 µm aluminum bond wires were computed and are shown for comparison. It is illustrated that with the bonding method used for the prototypes of the IPC2 (i.e., 4×18 µm gold bond wires), 78% of the conduction losses occur in the bond wires. Since larger pads are not considered because of higher manufacturing costs, an adequate solution will be the usage of flip-chip bumping which allows to carry the high current into and out of the IPC2. Unfortunately, all the contacted packaging houses able to perform flip-chip die attach at wafer level were unable to perform flip-chip die attach at die level for prototyping, since conventional equipment cannot be used for this.

Table 6.4: Conduction losses occurring at 2 A and 80°C in the power NMOS M_3.

Bonding Method	$\sum P_{bw}$	$\sum P_{RDS(on)}$	$\sum P_{met}$	Total
4×18 µm	900 mW	150 mW	100 mW	1150 mW
Gold Wire	78%	13%	9%	100%
1×100 µm	140 mW	150 mW	100 mW	390 mW
Aluminum Wire	36%	38%	26%	100%

6.2.4 Experimental Results of the Charger Detection

The IPC2 is a bidirectionnal DC-DC converter, able to supply the load, and able to recharge the battery when a battery charger is connected in parallel with the load (see Figure 4.1). The principle developed for detecting a battery charger was presented in details in Section 4.1. To show if the detection unit performs as predicted by the simulations, two kind of tests were done.

The first test was performed with no battery charger connected. The resulting oscillogram is shown in Figure 6.18. The IPC2 was supplying the load with a given V_{load} voltage. In contrary to the schematic shown in Figure 4.1, the V_{dir} pin was first grounded, and after several seconds, tied to the V_{core} voltage (i.e., 1.8 V). After 32 clock pulses on the CLK signal, the 5-bit counter shown in Figure 4.2 has overflowed, and the digital CHARGER signal has gone high. By this signal value, the IPC2 considers that a charger has been detected, and it tries to reverse the energy flow by charging the battery. However, the V_{load} voltage began to fall immediately, because no charger was actually connected. When the IPC2 senses a feedback voltage V_{FB} that is lower than the internal reference voltage V_{ref}, it immediately cancels the charging process and reverts the energy flow to supply the load again with the energy provided by the battery. The amount of voltage fall at V_{load} depends upon the speed of the VCDA comparator, the capacity C_{load} of the load capacitor, and the amount of current I_{load} consumed by the load. By this first test, it was demonstrated that the IPC2 detects reliably and rapidly enough a removed battery charger, so that the voltage seen by the load never falls more than 10% below the nominal voltage.

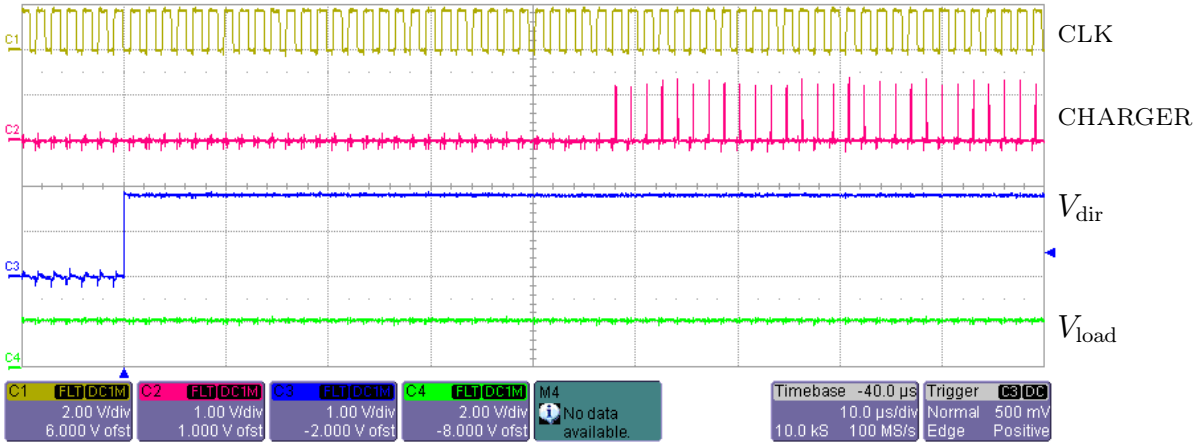

Figure 6.18: Oscillogram of the IPC2 when forcing the detection of a battery charger.

The second test consists in detecting the battery charger while supplying the load. The schematic presented in Figure 4.1 was used for this test. The IPC2 was first supplying the load with the adjusted load voltage, after what a battery charger was connected in parallel to the load. The IPC2 first performs in the buck mode (i.e., voltage step-down conversion when supplying the load with the energy from the battery). When the battery charger has been connected and detected, the digital CHARGER signal goes high (i.e., logic **1**). The energy flow reverses, and the battery is being charged. The IPC2 is then performing in boost mode. The experimental results are presented in Figure 6.19. The IPC2 was successful in reversing the energy flow to charge the battery, as it was in reverting it back to supply the load again. The bidirectionnality has therefore been successfully demonstrated.

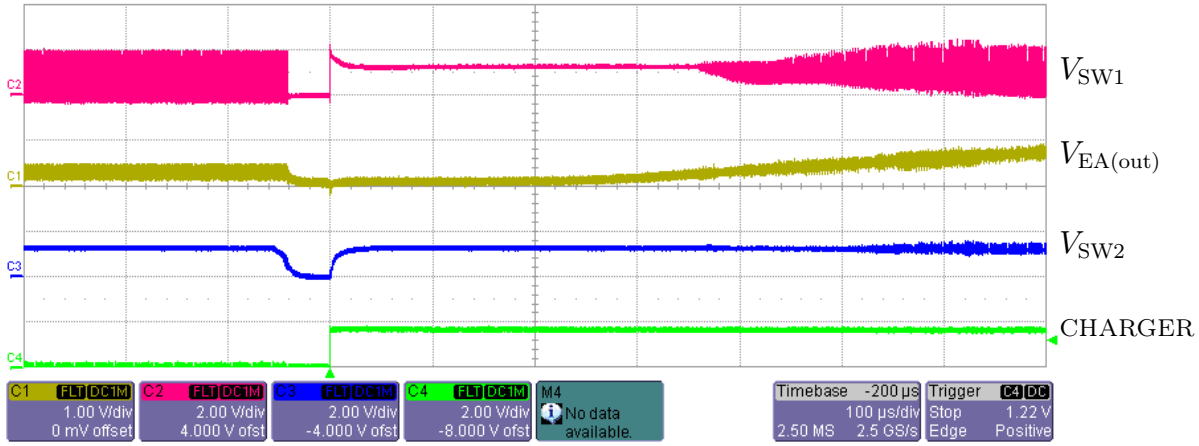

Figure 6.19: Oscillogram of the IPC2 when detecting a battery charger. First, the IPC2 performs in the buck mode and supplies the load. After the detection of the battery charger, the IPC2 runs in boost mode in reverse direction.

The circuit developed for detecting the battery charger performed as predicted by the simulations. However, the use of bond wires instead of bumps had some reliability issues in the IPC2. The bond wires provide for each power path an inductance of approximately 10 nH. Further, the printed circuit board layout was designed for testing purposes, and the power paths are long (i.e., several centimeters) and not symmetrical (i.e., discharging and charging modes of the IPC2 does not see the same parasitics at the same schematic points).

The reliability issues consist in destructive overvoltage spikes appearing when the power transistors in the H-bridge are switching high currents with very fast switching times, thus generating high current and voltage transients (i.e., high dI/dt and high dV/dt) in the power paths. An oscillogram of destructive voltage spikes is shown in Figure 6.20. Such spikes only appear when the IPC2 is charging the battery (i.e., when a battery charger is connected), as shown in Figure 6.21 (this oscillogram was taken with an IPC2 that was damaged by these voltage spikes, during an automatic charger detection test). The origin of the generation of these spikes is analyzed hereafter.

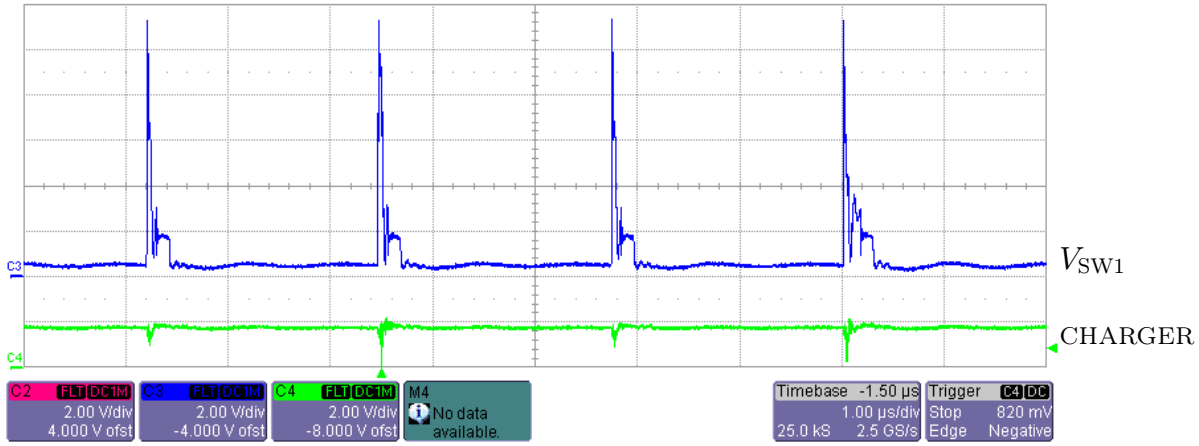

Figure 6.20: Destructive voltage spikes due to the parasitics of the test board and the bond wires. The screenshot was taken before the IPC2 was damaged by them. The voltage spikes reach more than 11 V, because of the gate drivers fast switching times defined during the design of the IPC2 for operating at 10 MHz. Therefore, these switching times cannot be increased by external components.

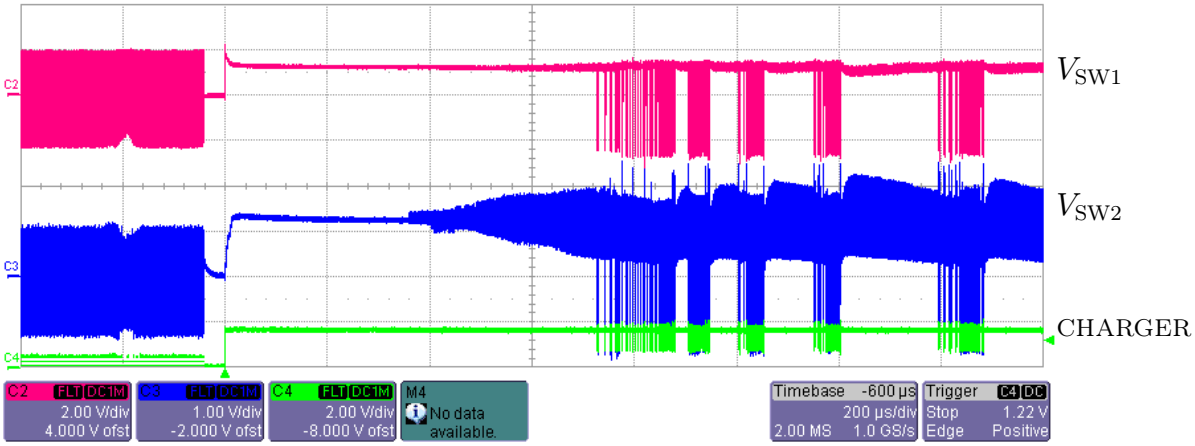

Figure 6.21: Oscillogram of a damaged IPC2 detecting a battery charger. The fault is illustrated by the negative voltage spikes in the discharging mode region (i.e., when the CHARGER signal is low). The voltage spikes in the charging mode (i.e., when the CHARGER signal is high) appear when the current flowing from the battery charger to the battery outreaches several tenths of milliamperes.

The parasitics being the cause of the overvoltage spikes were modelled and represented in Figure 6.22. They mainly originate from the resistance and inductance of the tracks of the printed circuit board, from the resistance and inductance of the bond wires in the power path of the IPC2, and from the parasitic capacities of the power transistors in the H-bridge (i.e., C_{DG}, C_{DS}, C_{DB}). The modelled circuit was simulated in Cadence Spectre. The switch-on ($t_{sw(on)}$) and switch-off ($t_{sw(off)}$) times of the pulses applied to the gate of the NMOS M_2 power transistor were taken approximately equal to the switching times defined in the design of the IPC2 (i.e., 3 ns). The parasitic component values used for the simulation are summarized in Table 6.5.

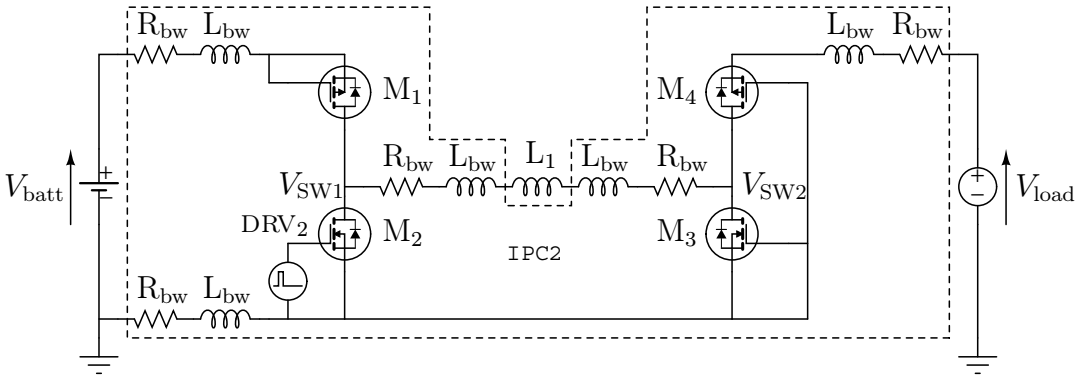

Figure 6.22: Model of the parasitics in the power path of the IPC2.

Table 6.5: Parasitic component values used for the simulation.

Parameter	V_{batt}	V_{load}	L_1	L_{bw}	R_{bw}	$t_{sw(on)}$	$t_{sw(off)}$
Value	2.0 V	1.2 V	10 µH	10 nH	225 mΩ	3 ns	3 ns

The simulation results presented in Figure 6.23 and in Figure 6.24 illustrate the overvoltage spikes phenomenon occurring in the IPC2. The obtained simulation results are very close to the experimental results shown in Figure 6.20.

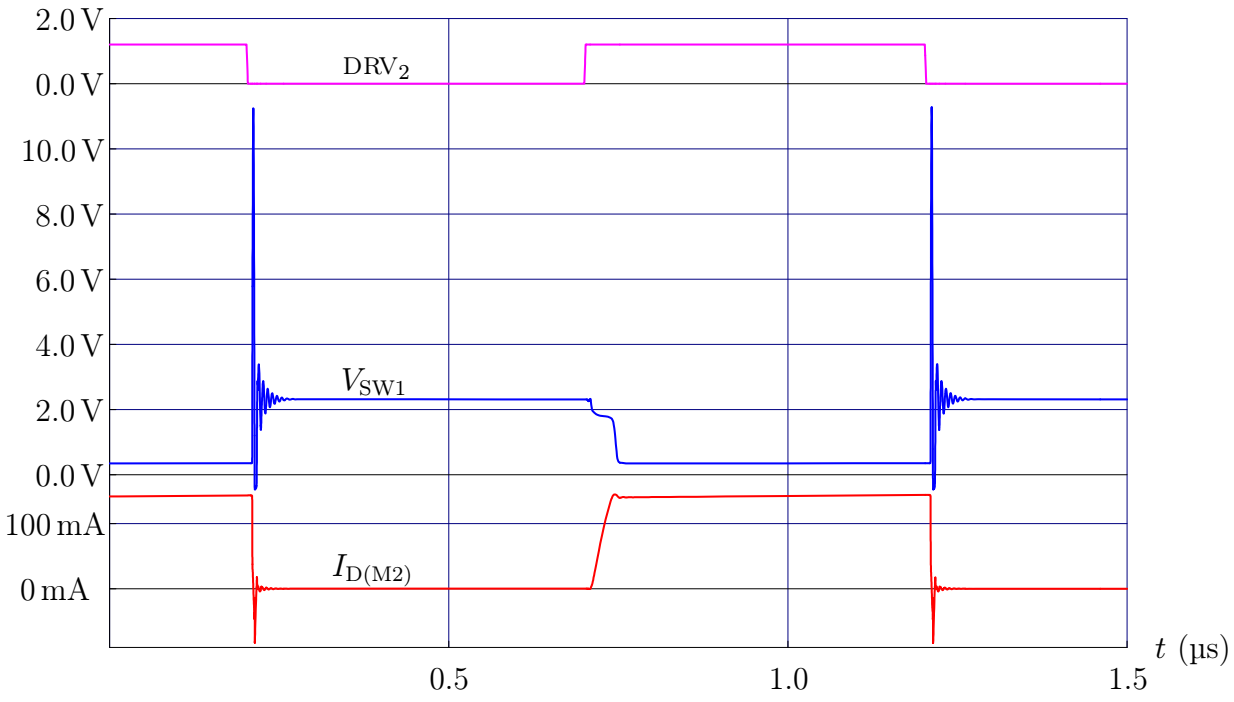

Figure 6.23: Simulated destructive voltage spikes occurring with the IPC2 when a battery charger is connected, and the charging mode is running. The schematic used to get these simulation results is shown in Figure 6.22. The values of the parasitics used for the simulation are summarized in Table 6.5.

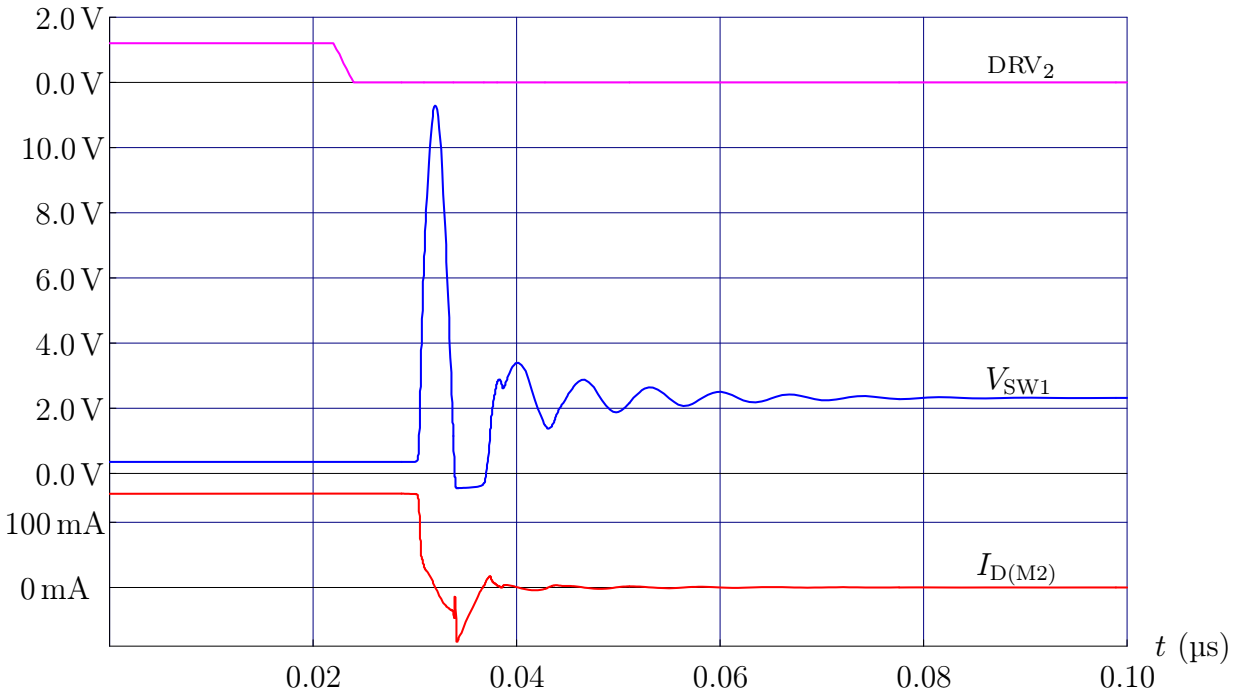

Figure 6.24: Simulated destructive voltage spike occurring with the IPC2. Magnification of a voltage spike shown in Figure 6.23.

The origin of the voltage spikes is explained and illustrated in Figure 6.25. For the analysis, the battery charger is considered to be charging the battery:

a. In a first phase, M_2 is turned on, and the current I_{L1} increases.

b. In a second phase, M_2 was turned off quickly. The current I_{L1} through the inductor L_1 stays continuous. However, the current through the parasitic bond wire inductor L_{bw} connected to the positive pole of the battery cannot rise instantly to I_{L1}. The current provided by L_1 flows into the parasitic capacities of M_2 (i.e., C_{DG}, C_{DS}, C_{DB}). Since these capacities are small compared to the current I_{L1}, the voltage V_{SW1} across M_2 rises rapidly (i.e., the voltage V_{SW1} increases, the current $I_{D(M2)}$ entering the drain of M_2 is positive). This voltage can easily reach values far above the breakdown voltage of the considered CMOS technology.

c. In a third phase, all the I_{L1} current flows through the body diode of the PMOS M_1. The parasitic capacities of M_2 are now discharging through the body diode of M_1, until V_{SW1} reaches the voltage value defined by V_{batt} and the voltage drop across the body diode of M_1 (i.e., the voltage V_{SW1} decreases, the current $I_{D(M2)}$ entering the drain of M_2 is negative). Because of the parasitic bond wire inductor connected to the ground, several cycles of the second and third phases can be observed, thus generating the oscillations shown in Figure 6.24 in the time interval $[0.04, 0.08]$ µs.

d. In a fourth phase, all the I_{L1} current flows through the body diode of the PMOS M_1, and the voltage V_{SW1} is constant.

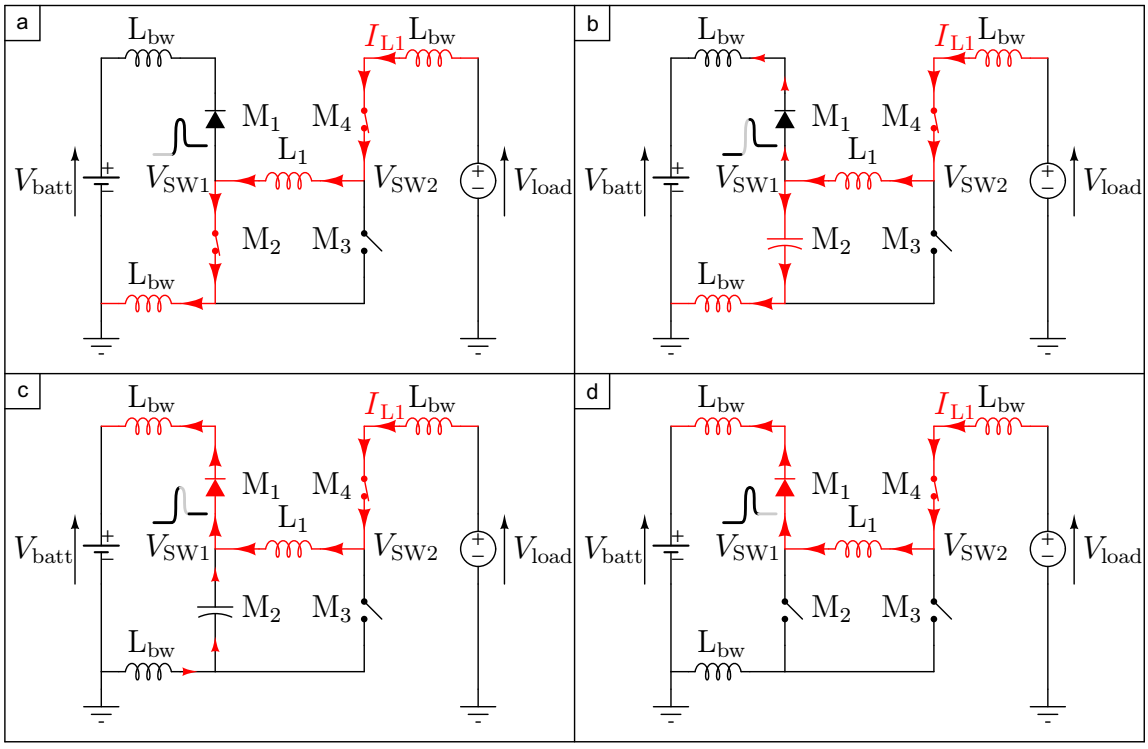

Figure 6.25: Determination of the origin of the voltage spikes. The model was simplified and only the elements needed for the comprehension of the generation of the voltage spikes measured at V_{SW1} are shown.

To reduce these destructive voltage spikes, the bond wires of the IPC2 should be replaced by solder bumps (bump mapping assembly) to suppress the parasitic inductance, thus allowing the IPC2 to operate with much lower voltage spikes at fast switch-on and switch-off times. Further, the length of the tracks on the printed circuit board must be reduced, thus decreasing the parasitic inductance of the power tracks. Ideally, each supply rail should have its own power plane on a multi-layer PCB. Placing very low ESR decoupling capacitors just beneath the die of the IPC would help to reduce the voltage spikes. Reducing the switch-off speed of the power transistors would also lead to lower voltage spikes, but this would limit the maximum switching frequency. A more advanced solution for avoiding these overvoltage spikes at fast switch-on and switch-off times would consist in implementing soft switching. However, soft switching would require additional external passive components and additional complexity in the DC-DC controller unit.

The current measurement unit used to perform the constant current charging could unfortunately not be tested because of these destructive voltage spikes (i.e., $> 11\,\mathrm{V}$) generated when the energy flow is reversed (i.e., when the battery is being recharged by the battery charger).

Chapter 7

Conclusion and Outlook

7.1 Conclusion

The purpose of this thesis was to develop an intelligent power converter (IPC). This IPC consists in a bidirectional monolithic integrated DC-DC converter and a battery management unit, both integrated in a single silicon die. The IPC is dedicated to be integrated into lithium-ion batteries, to build a so-called *intelligent battery*. It has to manage the charging and the discharging of the battery, and must therefore provide several flexible adjustment functions (e.g., load voltage, charging current).

In a first step, the specifications of the IPC were defined. In a second step, a full custom circuit library was designed with the 0.18 µm mixed-signal CMOS technology from UMC and simulated in the Cadence environment. Input and output signal pads with ESD protection were also developed. In a third step, the IPC was simulated at the transistor level and its circuits were redesigned until the specified performances were reached. Monte-Carlo simulation models were written to simulate the influence of manufacturing process variations, thus making it possible to design circuits with low process variation dependence. In a fourth step, the layout of the designed analog and power parts was drawn. More than 4800 MOSFETs are shown in the circuit view, while more than 36000 MOSFETs are shown in the layout view (because some transistors have several gate fingers, like the power transistors). In parallel, a digital I^2C interface was developed in layout level. Two different prototype versions of the IPC (i.e., IPC1 and IPC2) were manufactured through multi-project-wafer runs by UMC. Finally, in a fifth step, the manufactured prototypes were tested and characterized with help of a specifically developed printed circuit test board.

The key research contributions made during the development of the IPC are summarized below:

- The first monolithic integrated bidirectional DC-DC converter capable of reverting the direction of the energy flow was designed and tested experimentally.
- The first DC-DC converter integrating a power management unit was designed and tested experimentally. This power management controls the charging of the connected lithium-ion battery. It can be configured through external passive devices (e.g., resistors, capacitors).
- The first DC-DC converter with automatic detection of the connection of a battery charger on the load side was designed and tested experimentally.

- The advantage of using the dynamic MOSFET sizing concept at high switching frequencies (i.e., in the 1-100 MHz range) was proven theoretically, and tested experimentally at switching frequencies up to 2 MHz.

- A continuous regulation feedback loop for DC-DC converters based on the H-bridge topology was developed and tested experimentally. The corresponding theory was also investigated mathematically. This continuous regulation loop enables smooth transitions between the voltage step-up and step-down modes in both conversion directions (i.e., charging and discharging) and can operate at high switching frequencies (i.e., up to 10 MHz and above).

- A novel lossless average current sensing method based on the sample-and-hold principle was developed and tested in the simulation. This method is especially well suited for low power switching converters, which need an approximation of the average inductor current at switching frequencies up to 10 MHz and above. In the IPC, the average inductor current value is used to perform an approximately constant current charging phase for the lithium-ion battery.

The experimental results obtained from the second prototype (i.e., IPC2) have shown a fully functional DC-DC converter. The digital part containing the I^2C interface was successfully tested with an external microcontroller. The power part of the IPC2 has shown experimentally an efficiency of 77%, and has reached switching frequencies of 5 MHz. Due to the chip assembly, the maximum inductor current was limited to only 200 mA, instead of 2000 mA as defined in the design specifications. This issue can be solved by reducing the conduction losses by using flip-chip bump mapping at die level instead of bond wires. The analog part worked well in all of the 45 prototypes of the IPC2, which confirms that the design of the layout permits to achieve a very high yield. The basic analog units all worked as expected in the simulation environment (e.g., bias current source, voltage reference, triangular oscillator, linear regulator, soft-start circuit, overcurrent protection, 2-phase charge-pump). Also the more complex units have shown their full functionality: the continuous regulation loop implemented in the PWM unit has shown experimental results fully compliant with the theoretical analysis. The automatic detection of a battery charger connected to the load side was successfully simulated, and demonstrated experimentally. Voltage spikes were observed when recharging the battery. They are due to the parasitics of the long bond wires in the IPC2 combined with the low quality printed circuit test board used for the experiments. A model of these parasitics was build and simulated, so that the solution for suppressing these destructive voltage spikes is known for future work. The solution is to use flip-chip bump mapping to suppress the bond wires, and solder the IPC2 on a 4-layer PCB using a ground plane and a supply plane.

7.2 Outlook

This research work has provided the basis for enabling the development of intelligent batteries with integrated electronics. Future research directions will focus on higher level integration. The power inductor and the filter capacitors will be integrated into a single packaged IC, or further, onto a single silicon die.

The battery management developed during this thesis controls the charging of the battery. The battery monitoring systems developed commercially until now and available on the market have some important drawbacks. They are not accurate, because they are developed for a specific battery type. They are neither parameterized nor adjustable. Therefore, they cannot be adapted to different battery capacities or to different battery chemistries. Additionally, if they are intelligent, they consume a significant part of the battery energy to do their monitoring tasks. Future developments will include a standardized digital and fully parameterized battery management system, capable of being adapted to any battery type (e.g., battery capacity, battery chemistry) and any portable system (e.g., cellular phone, MP3 player, pocket PC) by adjustment of the internal variables, as done for example in MOSFET models. The battery management will offer the intelligence to recognize and calculate automatically the remaining battery energy. The real value of the remaining energy depends on several physical quantities (e.g., battery age, ambient temperature) and is therefore difficult to estimate accurately. However, the remaining operating time is an important information for the user of mobile systems.

In mid-term future, the intelligent battery concept proposed in this research work will be the basis for enabling automatic energy harvesting. This means that the mobile system will be able to get the necessary energy from its environment (i.e., from electrical, mechanical, electromagnetical, chemical or thermal sources). The bidirectional energy flow allowed by the IPC enables it to perform like an uninterruptible power supply. In other words, when the external energy sources in the environment provide enough energy to the load, the IPC will use the energy in excess to recharge the battery. Later, when the external energy sources in the environment are too weak (e.g., not enough solar rays are received by the solar cells), the IPC will compensate the lack of energy by using the energy previously stored in the battery.

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Glossary

A

AC	Alternating Current.
ADC	Analog to Digital Converter.
AMS	Austria Microsystems (foundry house, Austria).
ASE	Advanced Semiconductor Engineering (packaging house, Taiwan).
ASIC	Application Specific Integrated Circuit.
ASR	Area Specific Resistance.

B

BGA	Ball Grid Array.
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor.
BJT	Bipolar Junction Transistor.

C

CC	Constant Current.
CCM	Continuous Conduction Mode.
CLCC	Ceramic Leadless Chip Carrier.
CMOS	Complementary Metal Oxide Semiconductor.
CNRS	Centre National de la Recherche Scientifique (France).
CPU	Central Processing Unit.
CTAT	Conversely proportional To Absolute Temperature.
CV	Constant Voltage.

D

DAC Digital to Analog Converter.

DC Direct Current.

DCM Discontinuous Conduction Mode.

DPWM Digitally controlled PWM.

DRC Design Rule Check.

DUT Device Under Test.

E

EMI Electromagnetical Interferences.

ESD Electrostatic Discharge.

ESR Equivalent Series Resistor.

Q

HQFN High power Quad Flat No-leads package.

H

HV High Voltage.

I

I^2C Inter-Integrated Circuit.

IC Integrated Circuit.

IGBT Insulated-Gate Bipolar Transistor.

IIS Fraunhofer Institut Integrierte Schaltungen (Germany).

IISB Fraunhofer Institut Integrierte Systeme und Bauelementetechnologie (Germany).

IMEC Interuniversity Microelectronics Center (Belgium).

InESS Institut d'Électronique du Solide et des Systèmes (France).

IPC Intelligent Power Converter.

ITRS International Technology Roadmap for Semiconductors.

IZM Fraunhofer Institut Zuverlässigkeit und Mikrointegration (Germany).

J

JLCC Ceramic J-Leaded Chip Carrier.

L

LPE Layout Parasitics Extraction.

LVS Layout Versus Schematic.

M

MCT MOS-Controlled Thyristor.

MIM Metal-Insulator-Metal.

MMC Metal-Metal Capacitor.

L

MOSFET Metal Oxide Semiconductor Field Effect Transistor.

P

PDA Personal Digital Assistant.

PFM Pulse-Frequency Modulation.

PIP Polysilicon-Insulator-Polysilicon.

PLCC Plastic Leaded Chip Carrier.

PSM Pulse-Skip Modulation.

PSRR Power Supply Rejection Ratio.

PTAT Proportional To Absolute Temperature.

PWM Pulse-Width Modulation.

Q

QFN Quad Flat No-leads package.

R

RAM Random Access Memory.

RF Radio Frequency.

RMS Root Mean Square.

S

SEPIC Single-Ended Primary Inductance Converter.

SIT Static Induction Transistor.

U

UMC United Microelectronics Corporation (foundry house, Taiwan).

V

VCDA Very-wide-Common-mode-range Differential Amplifier.

Index

Curriculum Vitæ

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