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Thèse

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Développement des capteurs à pixels avec microcircuits intégrés pour le détecteur vertex de l'expérience STAR au collisionneur RHIC

Development of pixel detectors with integrated microcircuits for the Vertex Detector in the STAR experiment at the RHIC collider

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Abstract

This work is part of the Monolithic Active Pixel Sensor (MAPS) R&D program that is directed towards constructing a new, 135 Mega pixel vertex detector for the STAR experiment at the RHIC collider. The new detector is planned to be installed in 2011 and it will extend the current physics capabilities of the system due to its planned high pointing resolution of 30 μm. This will allow direct reconstruction of charmed mesons using their decay vertices. The STAR collaboration is actively pursuing detector development in the emerging MAPS technology that offers monolithic detectors fabricated in standard CMOS processes, potentially low power dissipation, and thin (50 μm) devices. The work presented addresses development of MAPS from basic architectures to the basic integrated on-chip signal processing. A common element for most of the presented readout schemes is a low-noise, low power consumption, compact in-pixel amplifier. A review of possible solutions for this element is presented together with experimental results.

MAPS operating in current mode have also been investigated in this thesis as an alternative to the classical voltage operating mode.

The final part of the research and development presented is dedicated to the integration of MAPS sensors in a complete detector system. A prototype readout system for the STAR vertex detector was built in a scaled-down version and coupled to a detector telescope composed from three MAPS prototypes. Optimization of readout of a multi-million pixel detector has been addressed in this work with a study of an "on-the-fly" cluster finding algorithm reducing data rates.

The operation of RHIC with increased luminosity will require more advanced pixel architectures than the simple design implemented in the first prototypes dedicated to STAR. In this work the solutions presented indicate a development path for the final sensor with in-pixel signal amplification and on-chip data digitization and rudimentary sparsification.

Résumé

Introduction

Ce travail contribue au programme de recherche et de développement des détecteurs monolithiques à pixels actifs (Monolithic Active Pixels Sensors - MAPS) pour la physique des particules au sein des accélérateurs. Ces capteurs ont été réalisés dans une technologie standard CMOS. La thèse se concentre sur l'optimisation des architectures de pixels. L'accent est mis sur les capteurs pour la construction du prochain détecteur de vertex dans l'expérience STAR du collisionneur RHIC prévue pour 2011.

La motivation pour cette thèse est fondée sur de nouvelles recherches dans la physique des particules, particulièrement au RHIC, comme par exemple les mesures du flux des mésons charmes et l'atténuation des jets dans les collisions des ions lourds ultra relativistes. Ces nouvelles études nécessitent des détecteurs vertex avec une très bonne résolution spatiale, inférieure à 10 μm. L'environnement de l'expérience avec un grand flux de hadrons près de la région des interactions, exige de nouvelles caractéristiques sur l'architecture et sur la technologie des capteurs. Sont particulièrement importantes la vitesse de lecture rapide pour éviter la superposition des événements (pile-up) ainsi que la conception et réalisation du circuit électronique qui doit être tolérante aux radiations.

La collaboration STAR a choisi comme solution la plus attrayante pour le nouveau détecteur vertex la technologie nouvelle des MAPS qui fournit beaucoup d'avantages et un bon compromis au niveau des performances, par rapport aux autres technologies disponibles. Les avantages principaux des MAPS incluent : l'intégration d'une matrice de capteurs et de l'électronique de lecture dans le même substrat de silicium, une consommation en puissance faible et un temps de lecture rapide. Il existe également des techniques industrielles afin d'amincir l'épaisseur des capteurs. Les capteurs minces sont une nécessité du système, car ils permettent de minimaliser le matériel près du point de collision et de réduire au minimum la diffusion multiple des particules chargées traversant les détecteurs. Le détecteur proposé et développé par les laboratoires de l'IPHC et du LBL de la collaboration STAR, appelé le "Heavy Flavor Tracker" (HFT), se composera de 33 capteurs organisés en deux barils. Chaque capteur aminci à 50 microns contiendra 640×640 pixels, au total 135 millions de pixels sur une surface de 1320 cm^2.

Travail réalisé

L'application au RHIC du détecteur de vertex, exige un grand débit des données (supérieur à plusieurs GB/s), par conséquence le traitement électronique des signaux au détecteur lui-même est crucial. Le travail présenté dans cette thèse, décrit la progression du développement de la technologie MAPS d'une simple architecture (deux ou trois transistors par pixel) jusqu'à des conceptions plus complexes qui intègrent le traitement des signaux sur le circuit du MAPS.

Le traitement de base des signaux, étudié dans ce travail, inclut l'amplification des signaux

intégrés dans les pixels et le double échantillonnage corrélé (CDS), intégré in situ. Le CDS libère le signal produit par le passage d'une particule du bruit fixe dû à la non uniformité du circuit (FPN) et dû à des composants corrélés du bruit temporel à basse fréquence. Quelques prototypes de ces capteurs qui fournissent cette fonctionnalité ont été analysés avec les outils d'un logiciel CAO (Conception assisté par Ordinateur). Ils ont été également étudiés intensivement en laboratoire.

Plusieurs possibilités de développements pour adapter et optimiser les MAPS pour des applications dans un contexte spécifique sont présentées dans ce travail. L'une d'entre elles est la construction du détecteur de vertex de STAR qui s'appuie sur des circuits simples de pixels à deux transistors. Cette structure est appropriée à l'environnement de l'expérience STAR : fonctionnement en temps d'intégration importante (4 ms pour la première étape) et fonctionnement à température ambiante avec une dissipation de puissance minimale (inférieure de 100 mW/cm^2). Pour réaliser les temps de lecture les plus rapides, environ 200 μs, le traitement de base des signaux sur les circuits est essentiel. On propose un circuit avec lecture des colonnes de pixels en parallèle et l'amplification des signaux intégrés dans les pixels ainsi qu'un double échantillonnage corrélé (CDS) intégré sur le capteur. Le CDS libère le signal produit par le passage d'une particule du bruit fixe dû à la non uniformité du circuit (FPN) et dû à des composants corrélés du bruit temporel à basse fréquence. Les résultats de ce prototype démontrent que FPN est réduite au-dessous d'un niveau de quinze électrons, permettant l'utilisation d'un comparateur simple ou d'un ADC à basse résolution par colonne de pixels.

Une étude des possibilités pour un amplificateur d'entrée en mode tension intégré au niveau d'un pixel avec une consommation de puissance faible et à faible bruit, est présentée avec les résultats expérimentaux associés. Les structures d'amplifications simples avec un gain d'environ cinq, suffisent pour un bruit inférieur à 15 électrons. Ceci pourra assurer un rapport du signal sur bruit (S/B) supérieur de 15-20 pour la valeur la plus probable d'ionisation dans un capteur avec une épaisseur de couche épitaxiale d'environ 14 μm, donnant une efficacité de détection de particules supérieur a 99%.

Le fonctionnement des MAPS en mode courant a été également étudié dans cette thèse. L'élément de détection de chaque pixel est une diode de n-well/p-sub avec un transistor PMOS intégré dans le n-well du silicium. La baisse du potentiel du n-well due à la collecte des charges régule le courant du transistor. Une partie de l'étude est consacrée aux structures alternatives de l'amplificateur de transconductance effectuant le traitement de CDS. Les problèmes du bruit élevé de 50 électrons et la dispersion pendant la lecture de la chaîne complète rencontrés avec ce circuit, ont été analysés et ils ont préparé le terrain pour les futures améliorations. L'analyse a permis d'identifier un transistor du pixel comme source du bruit et a indiqué les possibilités de corrections du prototype prochain par optimisation de bande passante de ce transistor. En dépit des problèmes d'exécution, le fonctionnement de tous les blocs constitutifs a pu être vérifié. Bien qu'actuellement cette structure ne soit pas une priorité du développement dédié à STAR, elle pourrait, à l'avenir, offrir une alternative intéressante par rapport aux pixels en mode tension.

Le premier prototype de MAPS consacré au détecteur de vertex de STAR a été fabriqué en mi-2005. Une partie du travail exécuté dans cette thèse a été dédié aux études étendues de ce dispositif. Une série de mesures de caractérisations incluent typiquement : la calibration en laboratoire, avec une source de rayons X, afin d'évaluer le facteur de conversion de charge et le S/B; des tests avec une dose intégrée de rayonnements ionisants jusqu'à 50 krad pour étudier la résistance aux irradiations ; et également des tests avec un faisceau d'électrons pour étudier

l'efficacité de détection des particules au minimum d'ionisation. Une performance satisfaisante du détecteur HFT (un bruit de 17 électrons ENC, S/B de 15, et une efficacité de détection supérieure de 99.8% à 30 °C) pourrait être réalisée avec cette conception pour une dose intégrée correspondant à une année du fonctionnement au niveau de 30 krad par an et à une température de fonctionnement d'environ 30 °C. Un refroidissement efficace du HFT est indispensable : une série de tests a indiqué une dégradation de l'efficacité avec l'augmentation de la température ainsi qu'avec la dose intégrée.

La dernière partie de la thèse est consacrée à l'intégration des capteurs MAPS au détecteur du vertex de l'expérience STAR. L'intégration est une tâche importante: la conception d'un capteur dépend fortement des conditions dans lesquelles un système complet de plusieurs matrices de pixels fonctionne. Ce travail consiste à établir un prototype du système de lecture à taille réduite et à le coupler à un télescope de détecteurs composé de 3 prototypes MAPS. Le système a été étudié en détails au laboratoire, avec un faisceau d'électrons et dans l'expérience STAR lui-même. La principale difficulté de l'intégration est due à l'exigence de l'utilisation des structures légères afin de minimiser le budget en longueurs de radiation. Dans le système du prototype le nombre des capacitances de découplage a été limité donnant la dégradation de bruit des capteurs. En dépit du bruit élevé, le système a bien marché et a été intégré avec succès dans les systèmes de STAR. Les particules ont bien été observées et les traces reconstruites.

L'optimisation de la lecture d'un système portant sur plusieurs millions de pixels a été étudiée dans ce travail avec un algorithme trouvant dynamiquement les pixels touchés par le faisceau afin de réduire le débit des données. Cet algorithme a été implémenté dans un FPGA mais sa simplicité est aussi intéressante pour l'intégrer directement dans un capteur. Pour le détecteur HFT construit avec des capteurs possédant des sorties analogiques, l'algorithme étudié réduit le débit des données, initialement à 50 GB/s au niveau du capteur, jusqu'à 115 MB/s au niveau du système d'acquisition et du stockage. Pour le capteur final, avec une lecture binaire on attend une réduction du débit des données de 3.4 GB/s à 23 MB/s.

Conclusions

Les résultats obtenus à partir de ces études ont validé le choix technologique et de l'architecture du capteur dédié au détecteur du vertex de STAR. La tenue aux rayonnements accrue a été réalisée en éliminant l'oxyde de champ de la proximité de la diode rassemblant les charges. Un refroidissement efficace du HFT est indispensable: une série de tests a indiqué une dégradation de l'efficacité avec l'augmentation de la température ainsi qu'avec la dose intégrée.

L'opération du RHIC à une luminosité plus grande exige des architectures plus avancées que la simple conception mise en application dans ce premier prototype consacré à STAR. Dans ce travail les solutions présentées indiquent le chemin de développement pour les capteurs finaux avec une amplification du signal intégré dans les pixels, les colonnes traitées en parallèle, et une numérisation des données sur le détecteur ainsi qu'une réduction des données rudimentaires. Un simple amplificateur d'entrée en mode tension réalisé comme une source commune ou cascode doit être suffisant pour assurer la performance du capteur avec un rapport signal sur bruit supérieur à 15-20 et une efficacité supérieure à 99.8%.

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Chapter 1

Introduction

Particle physics, or High Energy Physics (HEP), studies elementary constituents of matter and radiation and the interactions between them. It is known that the smallest fundamental particles have sizes below 10^{-18} m. Studying them requires probes with wavelengths of similar size or smaller. These probes are particles accelerated to very high energies (on the order of a TeV) witch deliver the de Broglie wavelength $\lambda = h/p$, where the wavelength of a particle, λ, is inversely proportional to its momentum, p, and h is the Planck constant.

Colliding particles at very high center of mass energies provides energy that can be converted into very massive particles in agreement with Einstein's equation $E = mc^2$, where E is energy, m is the particle mass, and c is the speed of light in vacuum.

Current experiments in particle physics collide accelerated particles with each other or with a fixed target. The products of the collision are studied with sophisticated detector systems built around the interaction point. For colliding beam experiments, the detector has typically a cylindrical shape as the particles are radiated in all directions.

Modern multi-component detectors test different aspects of each collision (called an event) by tracking particles and their decay products in a strong magnetic field. Massive, unstable particles containing heavy quarks (charm, bottom), for example the D meson, decay into less-massive particles on a picosecond timescale. These short lived particles never reach detectors and their presence can only be established by identifying and tracking their decay products.

1.1 STAR at RHIC

The Relativistic Heavy Ion Collider (RHIC), located at Brookhaven National Laboratory (BNL), Upton, NY, USA, was constructed to study Quantum ChromoDynamics (QCD) at high densities and temperatures. QCD is the theory of strong interactions of quarks and gluons and it is a part of the Standard Model of particle physics. An important property of QCD is quark confinement. Color-charged particles (such as quarks) can not be found individually. The force between these particles does not decrease with distance and an infinite amount of energy would be required to separate them. Quarks are therefore confined in color neutral groups - hadrons (mesons and baryons composed of two and three quarks, respectively). The quark-gluon plasma (QGP) is a phase of nuclear matter that is predicted by QCD to exist at extremely high temperature and/or particle density [1]. In this phase, mesons (made of quark-antiquark pairs) and baryons

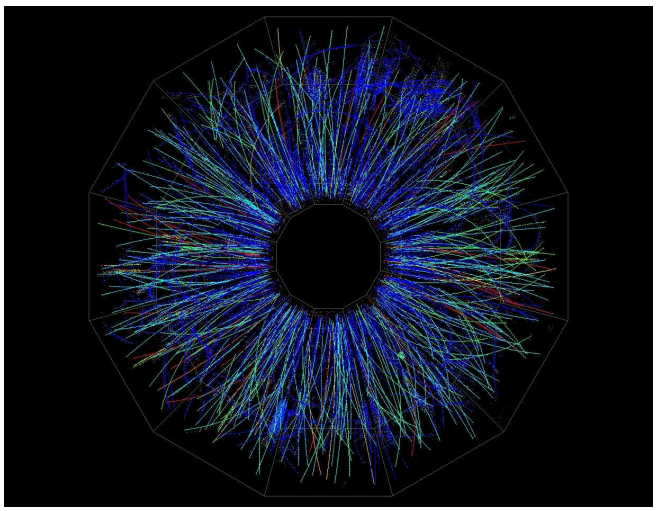


Figure 1.1: Beam axis view of tracks from particles created in a heavy-ion collision registered by the STAR TPC.

(three-quark particles), are no longer bound together in hadrons but form a plasma of quarks and gluons. In this state quarks and gluons are deconfined. This hot and dense state of nuclear matter must have existed a few microseconds after the Big Bang, when hadronic matter started to form. It is also believed to exist in very dense stars. At RHIC one searches for the formation of the QGP in ultra-relativistic heavy-ion collisions.

RHIC started operation in 1999 [2]. It is a colliding beam accelerator with center of mass energies of up to 200 GeV per nucleon (500 GeV in proton-proton collisions). The RHIC can collide heavy ions (e.g. Au-Au, Cu-Cu) as well as light nuclei. Data from collisions of deuterium nuclei with gold nuclei, as well as proton-proton collisions, were collected as a reference to which the heavy-ion collisions can be compared. The highest luminosity Au-Au collisions at RHIC produce approximately 1000 particles per unit of pseudo-rapidity,[1] creating a very high density tracking environment. Each collision also produces a high flux of secondary particles that are produced by the interaction of the primary particles with the material in the detector, and by the decay of short-lived particles produced in the initial interaction. Figure 1.1 illustrates high density of particle tracks resulting from a central Au-Au collision observed by the STAR experiment.

The Solenoidal Tracker At RHIC (STAR) is one of four dedicated experiments at RHIC. The main feature of the STAR experiment are detector systems with complete azimuthal angular coverage and with large pseudo-rapidity range ($|\eta| \leqslant 1$) for tracking, momentum analysis, and particle identification at central rapidity [3].

Other experiments at RHIC are: PHENIX (Pioneering High Energy Nuclear Interaction eXperiment) designed specifically to measure direct probes of the collisions such as electrons, muons, and photons; PHOBOS (named after one of the moons of Mars) has the largest pseudo-rapidity coverage of all detectors, and was tailored for bulk particle multiplicity measurement –

[1] Pseudo-rapidity, η, is a commonly used quantity in experimental particle physics that describes the angle of a particle relative to the beam axis. It is defined as $\eta = -\ln[\tan(\theta/2)]$, where θ is the angle relative to the beam axis.

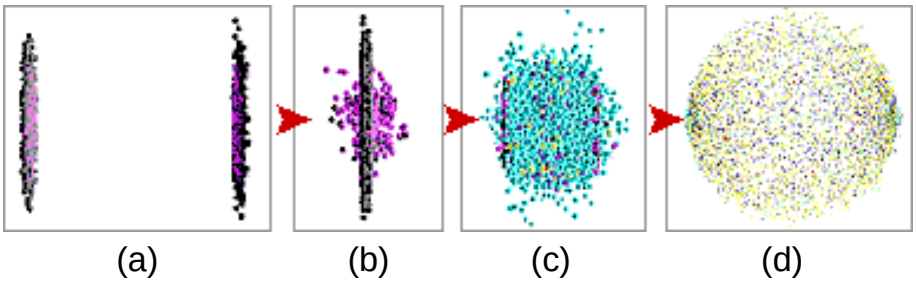


Figure 1.2: Stages of a Heavy Ion collision. Lorentz contracted ions before the collision (a). As the nuclei pass through one another their nucleons interact, (b), and hot and dense matter is formed (c). The matter cools down, quarks and gluons form hadrons, and thousands of particles emerge and reach detectors (d). (from `http://www.bnl.gov/rhic/heavy_ion.htm`)

it is inactive since 2005; BRAHMS (Broad RAnge Hadron Magnetic Spectrometers experiment) designed to measure charged hadrons over a wide range of rapidity and transverse momentum.

1.1.1 Selected Aspects of Heavy Ion Collisions at RHIC

High energy nuclear collisions can be characterized by three distinct phases as illustrated in Figure 1.2:

- initial: dominated by hard interactions between partons of the incoming nuclei,
- intermediate: when interactions between the matter constituents result in collectivity,
- final: when hadronization and chemical and thermal freeze-out take place.

Properties of the hot and dense matter created in high-energy nuclear collisions, also called fireball, can be studied from dynamics of the collective expansion of the bulk of the produced particles and from interactions between penetrating probes and the medium.

Penetrating probes include particles with very high transverse momentum (pT) and heavy particles containing charm or bottom quarks. These heavy particles can only be formed in early stages of the interaction when either the center of mass energy of the individual parton-parton collisions or the initial collective energy density is sufficient. Early creation of these particles makes them sensitive to the evolution of the medium and, therefore, gives them a paramount importance as probes of the nature of the fireball.

Experimental data collected by RHIC experiments, in particular the measured particle multiplicities and energies, allowed for the determination of the energy density in the heavy-ion collisions. This value is well above 1 GeV/fm^3 [4], the theoretically predicted threshold for the formation of a QGP.

Other crucial measurements include:

- The measurement of large elliptic flow; (At the beginning of a non-central collision the spatial distribution of the colliding matter resembles an ellipsoid due to the incomplete overlap of the two colliding nuclei. Strong scattering in this early stage converts the spatial anisotropy to a momentum anisotropy which is observable as an elliptic flow of the emitted hadrons. If strong scattering is sufficient to establish local thermal equilibrium, then the

pressure gradient is largest in the shortest direction of the ellipsoid. This produces higher momenta in that direction, quickly reducing the spatial asymmetry.)

- The observation of strong suppression of high pT particle production expressed by the nuclear modification factor $R_{AA} \approx 5$ for the momentum range of $5 < pT < 10$ GeV/c in Au-Au collisions; (R_{AA} is the ratio of particle production in heavy-ion collisions relative to the yield in p-p or d-Au collisions.)

- The nearly complete suppression of the away side jet in central Au-Au collisions; (A jet is a narrow cone of hadrons and other particles produced by the hadronization of a quark or gluon. Momentum conservation in the parton scattering results in a jet on the away-side with opposite momentum.)

These results have provided evidence for the formation of a high density and strongly interacting state of nuclear matter at RHIC [4].

The available theoretical studies indicate that for the high density system created at RHIC a description on the base of hadrons alone is not sufficient and partonic degrees of freedom have to be included. However, so far there is no direct evidence that the created state of matter is characterized by quark deconfinement that would directly indicate quark-gluon plasma formation [4].

In the coming years, STAR will focus on further refinement of the observed properties of the created medium as well as investigation of new properties through measurements that include: charm collectivity and flow to test thermalization[2] of the fireball created and charm energy loss to test perturbative QCD[3] in the hot and dense medium at RHIC.

If the elliptic flow of heavy quarks is comparable to the elliptic flow of lighter quarks (u, d, s) it would indicate frequent interactions between all quarks and gluons, and therefore, thermalization of light quarks. Presence of the local equilibrium will allow using hydrodynamic models to study the produced matter and to understand the related degrees of freedom.

Thermal production of charm quarks in the fireball is suppressed due to their large masses. When they are produced, they can interact with thermalized light quarks to form mesons. Therefore, the relative yield of various charmed mesons (including D^+, D^-, D^0) is sensitive to the properties of the light quark medium. Measuring these yields will improve the understanding of the medium. It is important to note that these heavy particles have short lifetimes and quickly decay into less massive daughter particles.

An example of a decay of a charmed hadron D^0 is presented in Figure 1.3. D^0 originates at the interaction point (primary vertex) and, after traveling a distance of about 100 μm, decays into a kaon and a pion creating the displaced secondary vertex. Until now, the STAR experiment has successfully reconstructed small numbers of D^0's in d-Au and peripheral Au-Au collisions by pairing charged hadrons with opposite charge. But in central collisions, the large numbers

[2]Thermalization is a process in which particles reach thermodynamical equilibrium through mutual interactions.

[3]pQCD is a procedure to calculate the magnitude of physical observables by neglecting the effect of long range interactions. Under this assumption, the expression of the physical observables can be expanded in terms of powers of the strong coupling constant. Since the strong coupling constant in this case is significantly smaller than one, the expansion converges, rendering the physical observables precisely calculable. Thus the calculation results can be compared with experimental measurements.

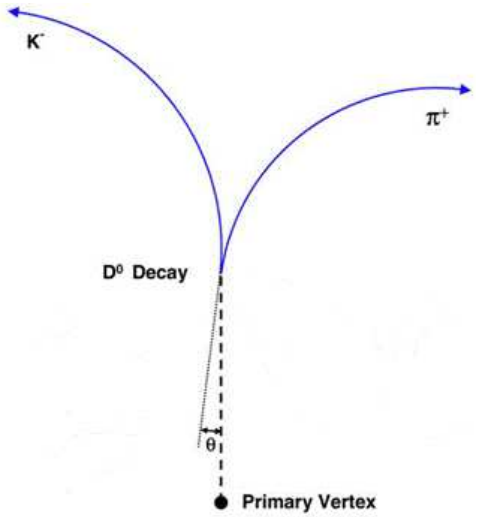


Figure 1.3: The decay topology for a D^0 particle decaying into a kaon and a pion. The distance from the primary vertex to the decay point is on the order of 100 μm.

of K and π produced provide high combinatorial background that is few orders of magnitude larger than the signal and makes the study intractable.

To obtain information on the heavy flavor production in central heavy-ion collisions it is necessary to measure charm and bottom hadrons by direct topological reconstruction. Reconstruction of short-lived D mesons requires measurements of displaced vertices with a precision of approximately 50 μm.

It is important to note that the STAR physics program is not limited to the study of the QGP but encompasses also the analysis of the proton spin. This area of research will be addressed with polarized proton collisions at 200 and 500 GeV center-of-mass energies and will allow studying the contribution of the spin of gluons to the overall spin of the proton [5].

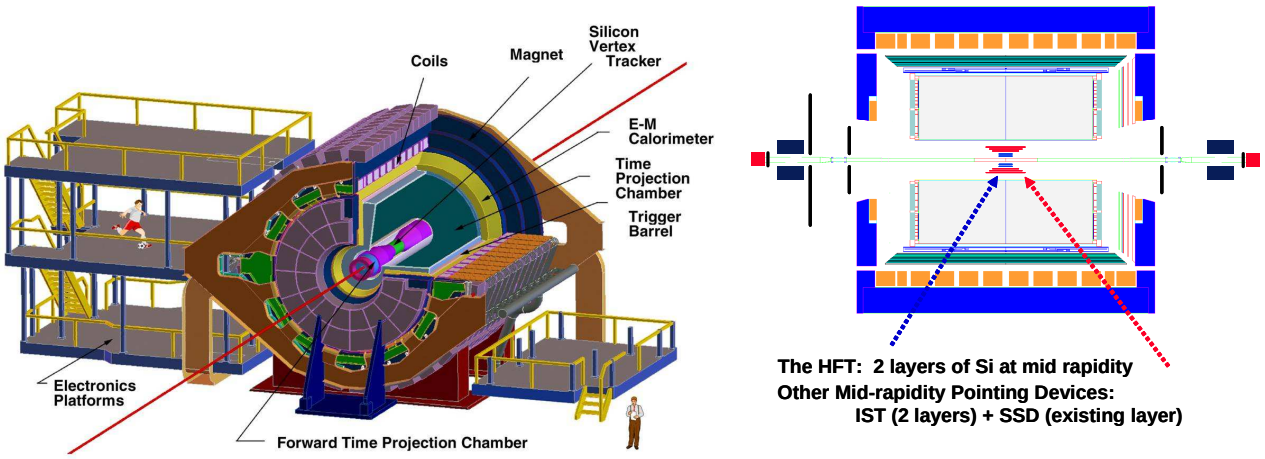
1.2 STAR detector

The layout of the STAR experiment is shown in Figure 1.4. The STAR detector utilizes a cylindrical geometry with a large cylindrical Time-Projection Chamber (TPC) (4 m in diameter and 4.2 m long) being the main tracking detector. It is installed inside a large solenoid magnet with a typical operating field of 0.5 T. The TPC can provide three dimensional tracking capability for thousands of tracks (except for large η). Projections on the end sectors give the $x-y$ coordinates[4], and the drift time of ionization electrons gives the z-coordinates of track segments. This detector can collect close to 70 millions of signal samples per event[5]. The dE/dx measurements of track segments allow for identification of particles over a significant momentum range of interest from 100 MeV/c to greater than 1 GeV/c.

The Barrel Electromagnetic Calorimeter and the End-cap Electromagnetic Calorimeter mea-

[4]The coordinate system in STAR is a Cartesian system with the z-axis defined along the beam line and y and x axes defined vertically and horizontally, respectively.

[5]136608 pads $\times$ 512 time samples (typically 380)



(a) (b)

Figure 1.4: Cross section views of the STAR detector. The proposed upgrade of the vertex detector is shown in the middle of the detector near the beam pipe. Blue layers represent the Heavy Flavor Tracker. Red layers correspond to the new Intermediate Silicon Tracker and the existing Silicon Strip Detector.

sure photons and electrons.

The physics capabilities of the TPC are improved by the Silicon Strip Detector (SSD) that surrounds the beam pipe and facilitates detection of decay vertices of short-lived particles. The SSD has been built in double-sided silicon strip technology and has a total radiation length of approximately 1% and achieves resolution of 20 μm in the transverse plane and 740 μm along the z-axis.

In addition, a Silicon Vertex Detector (SVT) was installed closest to the interaction point. The SVT was a three-barrel microvertex detector implemented in the silicon drift detector (SDD) technology. The total averaged radiation length of the SVT was below 6% for all three layers. This detector has recently been decommissioned.

The present STAR detector (TPC and SSD) allows for measurements of the primary vertex position with a precision of approximately 100 μm and secondary decay vertices with precision of about 500 μm. This is insufficient to accomplish the heavy flavor program described in Chapter 1.1.1. An upgrade of the detector is necessary.

1.2.1 Detector upgrades

After several years of operation the RHIC and its experiments are going through a series of upgrades that will allow to measure more observables and to study new physics. To extend physics capabilities of the RHIC experiments, the accelerator will be upgraded to allow for higher beam luminosities. This is followed by detector upgrades that will allow the experiment to take advantage of the increased luminosity.

The STAR experiment major upgrades include new sub-detectors:

- Time-Of-Flight (TOF) barrel to extend the momentum range of STAR's particle identification capabilities.
- A high rate data acquisition system and new front-end TPC electronics to efficiently use the RHIC's luminosity.
- Forward GEM Tracker (FGT) to improve tracking at $|\eta| > 1$.
- Heavy Flavor Tracker (HFT) to improve tracking capabilities and to allow identification of short-lived charm and bottom containing mesons.

The addition of the HFT, the new high-precision vertex detector, to STAR will enable measurements of displaced decay vertices at distances of approximately 100 μm from the primary vertex. Studies of parent particles with very short lifetimes, such as the D^0 meson, will be possible through direct topological identification of their decays [6].

A vertex detector is the innermost part of the detector system in HEP collider experiments. It is positioned as close to the collision point as possible, i.e., a few centimeters from the beam pipe. The vertex detector is typically arranged in several concentric cylindrical layers that measure with a high precision the space point coordinates for track reconstruction. In most of the HEP experiments, and especially those that collide heavy ions, there is an abundance of particles associated with each event. The innermost layers of a vertex detector need to be highly granular to minimize the track extrapolation ambiguities. The high particle density results also in a radiation environment in which a vertex detector must be able to operate.

A figure of merit that characterizes a vertex detector performance is the pointing accuracy. High pointing accuracy allows precise identification of secondary vertices.

A simple 2-dimensional model for the pointing accuracy of a two layer detector is derived in appendix A.1 and expressed by:

$$\sigma^2 = \frac{\sigma_1^2 r_2^2 + \sigma_2^2 r_1^2}{(r_2 - r_1)^2} + \frac{\theta_{mcs}^2 r_1^2}{\sin^2\theta} \tag{1.1}$$

where r_1 and r_2 are the radii of the detector layers with spatial resolution of σ_1 and σ_2, respectively; θ is the track polar angle; θ_{mcs} is the deflection angle from multiple Coulomb scattering in the first layer of the detector (at r_1). The multiple Coulomb scattering is given by

$$\theta_{mcs} \approx \frac{13.6\ MeV}{\beta cp} z\sqrt{x/X_0}\,[1 + 0.038\ln(x/X_0)] \tag{1.2}$$

where p, βc and z are the momentum, velocity, and charge number of the incident particle, and x/X_0 is the thickness of the scattering medium in radiation lengths[6]. Study of the formulas 1.1 and 1.2 reveals that an optimized vertex detector would have a very high single point resolution and would be very thin to minimize the multiple Coulomb scattering. It would also have the first layer located as close as possible to the interaction point and a distant second layer. Building a precise vertex detector requires finding an optimum for these and other, e.g. mechanical, constraints.

[6]Radiation length, X_0, is the mean distance over which a high-energy electron loses all but $1/e$ of its energy (predominantly by bremsstrahlung). For high-energy photons, which lose energy predominantly by electron-positron pair production, radiation length is 7/9 of the mean free path for pair production. Typically, X_0 is measured in $\mathrm{g \cdot cm^{-2}}$

The HFT that the STAR collaboration is proposing to build will consist of three detector systems with graded resolution [5]: the outermost layers will consist of the upgraded, existing Silicon Strip Detector [7, 5]. The two central layers will be organized into the new Inner Silicon Tracker [8, 5] that will use silicon strip detectors. The inner-most and highest precision sub-detector will feature the new highly granular pixel arrays (referred to as PIXEL), described below. TPC will point at SSD with a resolution of approximately 1 mm, SSD will point at IST with a resolution of about 300 μm, IST will point at PIXEL with a resolution of about 150 μm, and the PIXEL detector will allow for determination of a collision vertex with a precision better than 50 μm.

To achieve these goals, the PIXEL detector is characterized by small radiation length that limits the effect of multiple Coulomb scattering. The detector must also have a very good spatial resolution, on the order of several micrometers. To achieve such resolution, a precise positioning of the detector is required to allow localization of each pixel in the assembly to within about 20 micrometers. Therefore the detector structure must be light, have a low Z value, and be very stiff.

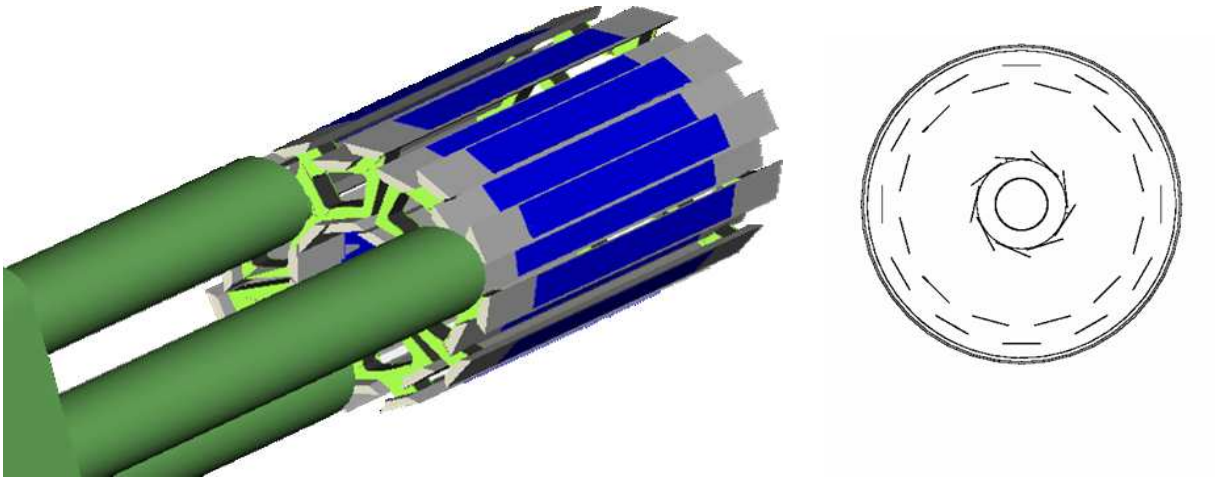
The work presented in this thesis focuses on the PIXEL detector and its components (including silicon sensors and a readout system). A complete description of the HFT detector is beyond the scope of this thesis and can be found in [5].

1.3 MAPS at STAR

There are number of technologies available for a silicon vertex detector and all of them have advantages and disadvantages, as briefly presented in Chapter 2.

The technology chosen for the PIXEL detector of the STAR upgrade is Active Pixel Sensors (APS) fabricated in standard CMOS processes. This technology evolved from visible light applications. In the early 1990s the APS became a viable alternative to Charge Coupled Devices (CCD) in visible imaging [9]. Initially these detectors suffered from low fill factor (30%) limited by in-pixel electronics absorbing the visible light. Later, by using the epitaxial layer to collect charges generated by photons, the fill factor was increased to nearly 100%, limited only by the metal lines present in pixels [10]. Use of this technique allowed, in 1999, the introduction of APS as a technology applicable to charged particle tracking [11].

Currently, Monolithic Active Pixel Sensors can offer resolution and speed performances that are competitive to other technologies in a variety of fields, including high-energy physics, medicine, biology, material and space sciences. The emergence of these devices in the field of high energy physics offers new possibilities. MAPS allow integration of the detector and the signal processing circuitry in the same substrate, which provides exciting possibilities for System-On-Chip (SoC) development. MAPS have a lot of potential and are carefully studied for the use in future experiments (including the International Linear Collider) or upgrades of the existing ones (e.g. STAR, BELLE). MAPS were chosen for their performance characteristics that best meet the STAR HFT requirements. They offer excellent spatial resolution, short readout time, satisfactory radiation tolerance, high detection efficiency, and can be thinned to a few tens of micrometers.



(a) Perspective view of PIXEL (b) Cross section

Figure 1.5: Architecture of the PIXEL detector. Left - 3-D view of two concentric barrels divided into three sections. The supporting structure on one side of the detector is also presented in the form of three cylindrical fixtures. Right - detector ladder arrangement with the inner layer composed of 9 ladders and the outer layer composed of 24 ladders.

1.3.1 PIXEL vertex detector

The architecture of the PIXEL detector is shown in Figure 1.5(a) with its cross section presented schematically in Figure 1.5(b). The main parameters of the detector are listed in Table 1.1

The PIXEL detector is composed of effectively two barrels located at radii of 2.5 and staggered at 6.5/7.0 cm from the center of the beam pipe. The barrels are composed of 9 and 24 detector ladders for the inner and outer radii, respectively. Each ladder contains a row of 10 MAPS chips with a total active area of 19.2 cm $\times$ 1.92 cm. Each sensor chip is a 640$\times$640 array of pixels with a 30 μm pitch. The sensors will be thinned to a thickness of 50 μm and the ladder support needs to be made of low mass carbon fiber structure to minimize tracking errors generated by multiple Coulomb scattering.

A two phase upgrade of the STAR vertex detector has been proposed. The first phase will provide a full-scale prototype suitable for evaluating the performance of the MAPS sensors in the collider environment. The current RHIC luminosity (Au-Au) of $1 \times 10^{27} cm^{-2} s^{-1}$ requires a modest read-out speed of the sensor in approximately 4 ms. This design is discussed in Chapter 6. An increase in luminosity by a factor of $\sim$ 8 is expected in the era of RHIC II [12]. A next generation of CMOS sensors is needed to handle the resulting high track density environment. The sensor integration time will have to be shorter to minimize the pile up effect. In addition, the PIXEL detector readout time will have to match the 1 ms readout time of the TPC. The design consideration for the MAPS complying with the requirements of the ultimate PIXEL detector will be presented in Section 8.1.2.

Table 1.1: PIXEL requirements for the first upgrade phase and for the final detector

	Step I **PIXEL 4–ms prototype**	Step II **ultimate PIXEL**
RHIC luminosity for Au-Au	1×10^{27}	8×10^{27}
ladder active area	approximately 2 cm × 20 cm	
pixel size	30 μm × 30 μm	
pixels/ladder	4,096,000	
number of barrels	2	
inner barrel	9 ladders @ 2.5 cm radius	
outer barrel	24 ladders @ 6.5 cm / 7.5 cm radius (staggered)	
sensor alignment accuracy	< 10 μm	
sensor single point resolution	$\lesssim 10$ μm	
power dissipation	< 100 mW/cm^2	
operating temperature	$\geq 30\,^\circ$C	$< 20\,^\circ$C[a]
integration time	4 ms	200 μs
readout time	4 ms	1 ms
mean silicon thickness	~ 50 μm	
total ladder thickness	$< 0.4\% X_0$	
detection efficiency	$\gtrsim 98\%$	
predicted hit density [hits/cm^2] (inner layer)	∼53	∼61
sensor readout	analog (12b ADC)	binary (1 bit/pixel)
expected data rates (sensors;detector)[b]	∼50 GB/s; ∼113 MB/s	∼50 MB/s
ionizing radiation tolerance/1 year operation (inner layer)	31 krad	150 (300) krad
non-ionizing radiation tolerance/1 year operation (inner layer)	$\sim 10^{12} \mathrm{n_{eq}cm^{-2}}$	$\sim 10^{13} \mathrm{n_{eq}cm^{-2}}$

[a] Operation of the detector at as low temperature as possible will probably be forced by high radiation doses expected in the STAR as a result of the increased beam luminosity.

[b] On-line cluster finding and zero suppression algorithms that will reduce data flow are foreseen for the 4-ms prototype.

1.4 Layout of thesis

MAPS are relatively new in the field of HEP and they are a very attractive solution for vertex detectors in present and future experiments. In the past few years, the use of MAPS for ionizing particle imaging has been proven [13]. MAPS continue to be extensively studied for vertex detector applications and their resistance to radiation damage [14]. MAPS have evolved from basic architectures to more complex designs that include on-chip signal processing (e.g. ADC) [15].These sensors find also use in many applications outside of HEP (see [16]).

The work presented in this thesis is focused on two aspects of MAPS development. The first is the general optimization of pixel architectures required for designing application specific devices, including sensors for STAR (Chapter 3). The second focuses on the use of MAPS sensors for the vertex detector upgrade at the STAR experiment.

Chapter 2 presents basic physics principles governing charge generation and collection in semiconductor materials after a passage of an ionizing particle, with an emphasis on silicon devices. A short description of radiation induced effects that deteriorate detector performance is presented. Part of the chapter covers pixel detector technologies, including short descriptions of the HPS, CCD, and DEPFET, followed by an introduction of MAPS. The numerous advantages of MAPS are defined and the weak points are identified.

Development of MAPS at Institut Pluridisciplinaire Hubert Curien (IPHC), Strasbourg, France, in the past few years is summarized in the beginning of Chapter 3. It is followed by a summary of procedures and tools used in this thesis for testing sensor prototypes. The main part of the chapter discusses optimization of pixel architecture, including charge sensing element, in-pixel amplification, and in-pixel correlated double sampling. A large part of this thesis is focused on studies and tests of different aspects of pixel optimization and the results are presented in the corresponding sections in Chapter 4. In addition to the classical approach to sensors operated in voltage mode, Chapter 5 covers advantages and problems of sensors with pixels operated in current mode.

Chapter 6 presents sensors developed at IPHC and dedicated to the STAR vertex detector upgrade. Their performance and compliance with requirements is studied through different tests, including laboratory tests with an ^{55}Fe source, tests with electron beams, and latch-up tests. Part of the work for this thesis was performed at the Lawrence Berkeley National Laboratory, Berkeley, USA, where the effort was focused on building a prototype telescope system and placing MAPS in the STAR environment. Chapter 7 covers a number of detector design issues closely related to sensors and optimization of the readout of a multi-million pixel detector. A prototype of the readout system for the PIXEL detector was built and tested. Performance of MAPS in the system that was built driven by vertex detector requirements is presented. At the end, the architecture and features of the ultimate MAPS sensor for STAR are discussed.

This work concludes in Chapter 8, where the perspectives for using MAPS in vertex detectors, especially in STAR, are addressed. Further MAPS optimization paths that will better satisfy vertex detector requirements are discussed. Since MAPS offer an appealing detection solutions beyond HEP, a brief description of selected spin-off applications is presented.

Chapter 2

Position sensitive silicon detectors

A charged particle passing through a detecting medium ionizes atoms along its track producing a cloud of electron-hole (e-h) pairs. The signal induced in a detector volume can be collected on detector electrodes and, in detectors with segmented electrodes, provide information on the path of the traversing particle. Silicon detectors are widely used for tracking of ionizing particles, including vertex detectors applications. In this chapter, interaction of radiation with matter, the principle of operation of silicon detectors, and different types of silicon pixel detectors are described. The discussion is focused on monolithic devices, especially the principle of operation and characteristic properties of MAPS.

2.1 Energy loss of charged particles

Charged particles lose energy in matter primarily by ionization and atomic excitation. The mean rate of energy loss (or stopping power) is given by the Bethe-Bloch equation (2.1). The region of validity is limited and, at very high energies, radiative effects begin to be important, while at very low energies, various corrections must be introduced [17]. For example, for pions the validity range extends from a few MeV to a few GeV.

$$-\frac{dE}{dx} = Kz^2\frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\left(\frac{2m_ec^2\beta^2\gamma^2T_{max}}{I^2}\right) - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right] \tag{2.1}$$

where

$K/A = 4\pi N_A r_e^2 m_e c^2/A = 0.307$ MeVg^{-1}cm^2 for $A = 1$ g mol^{-1};
$m_e \times c^2 = 0.510$ MeV, electron mass times squared speed of light;
$r_e = \frac{e^2}{4\pi m_e c^2} = 2.817 \times 10^{-13}$ cm is the classical electron radius;
$N_A = 6.022 \times 10^{23}$mol^{-1} is Avogadro's number;
Z and A are the atomic number and mass of the absorber;
I is the mean excitation energy [eV];
z is the charge of the incident particle in terms of electron charge;
$\beta = v/c$ is the velocity of the particle in units of speed of light;
$\gamma = \frac{1}{\sqrt{1-\beta^2}}$ is the Lorentz factor;
$\delta(\beta\gamma)$ is the density effect correction to ionization energy loss;

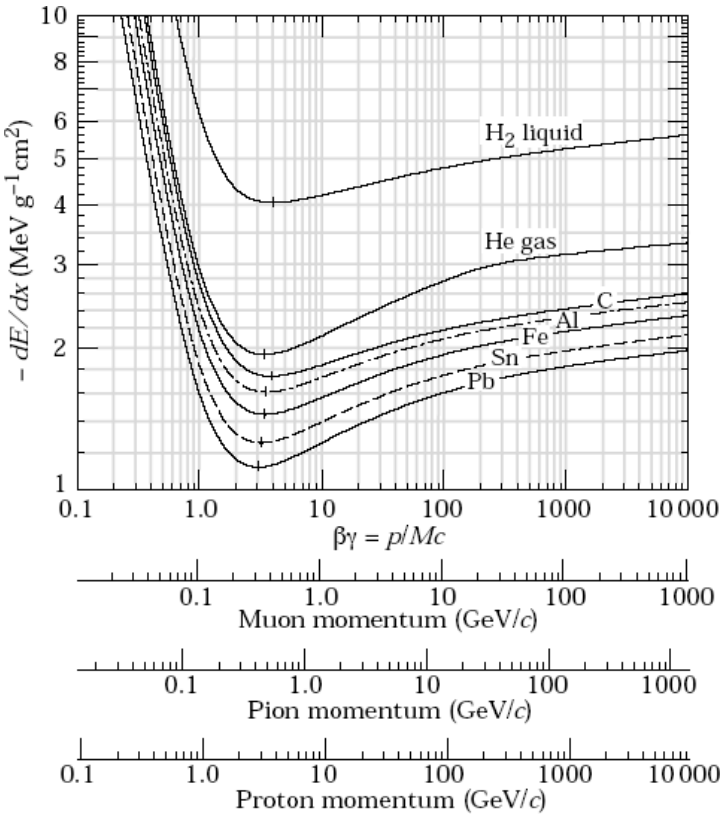


Figure 2.1: Mean energy loss rate in different absorber materials plotted as a function of the relativistic factor $\beta\gamma$ and as momentum of different particles. (Source: [17])

Tmax is the maximum kinetic energy which can be transferred to a free electron in a single collision:

$$T_{max} = \frac{2m_e c^2 \beta^2 \gamma^2}{1 + 2\gamma\frac{m_e}{M} + \left(\frac{m_e}{M}\right)^2} \tag{2.2}$$

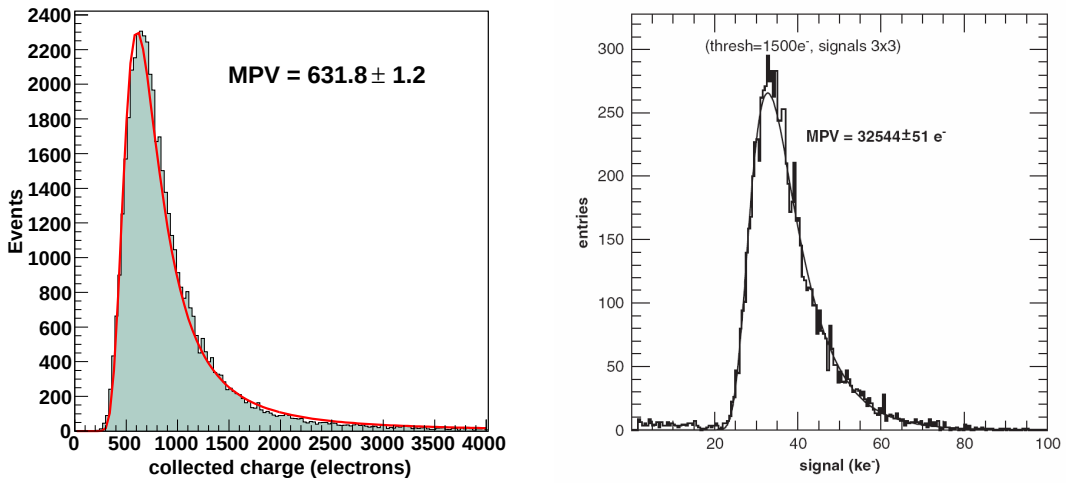
where M is the mass of the incident particle.

The parameter δ corrects for the density effect related to the polarization of the medium. This limits the electric field of very fast charged particles, effectively truncating the logarithmic rise of the energy loss function at very high energies at $\gamma\beta \gtrsim 10$.

For all practical purposes in high-energy physics dE/dx in a given material is a function only of β and does not depend on the mass of the particle. The mean energy loss for different absorbers is presented in Figure 2.1. A particle with an energy corresponding to the minimum of the energy loss rate is called a Minimum Ionizing Particle (MIP).

Part of the relativistic rise at high energies originates from the enhancement of the electric field in the transverse direction that allows the particle to interact with larger number of electrons. Another effect responsible for the relativistic rise develops due to the $\beta^2\gamma^2$ growth of Tmax, which is due to rare large energy transfers to a few electrons. When these cases are excluded, i.e. energy transfers are restricted to $T \leq Tmax$, the energy deposit in an absorbing layer approaches a constant value [17].

The amount of charge liberated in the active volume of the detector, which contributes to



(a) (b)

Figure 2.2: Energy loss distribution measured for ~ 5 GeV electrons with a CMOS sensor prototype MIMOSTAR2 (Chapter 6) for cluster size of 9 pixels, (a). Data was collected with an electron beam at the DESY testing facility. The shape of the distribution is compared with the signal in a fully depleted detector (DEPFET with thickness of 450 μm, tested with a $\sim$ 6 GeV electron beam at DESY [19]), (b).

the sensed signal, depends on the energy deposited along the particle track rather than directly on the energy lost by the traversing particle. A part of the energy lost by a traversing particle can escape from the track vicinity through high-energy knock-on electrons (δ-rays) produced. Practical tracking detectors measure the energy deposited close to the particle track and not the total energy lost.

Fluctuation in energy loss

The most probable energy loss in a detector is considerably below the mean given by the Bethe-Bloch equation. The energy loss is a discrete stochastic process. The quantity $(dE/dx)\delta x$ is the mean energy loss via interaction with electrons in a layer of thickness δx. For finite δx, there are fluctuations in the actual energy loss. The distribution is skewed toward high values (the Landau tail) [18]. The peak in the distribution defines the most probable energy loss. The mean energy loss is shifted towards higher values. An example of the Landau distribution is presented in Figure 2.2(a).

When the mean energy required for charge carrier generation in a given material is known, the most probable energy loss allows defining the most probable number of charge carriers generated along the particle track per unit length. In the case of semiconductor material, this quantity is expressed with the number of e-h pairs generated. A single MIP particle, traversing a silicon detector, yields about 80 e-h pairs per micrometer of the particle track as the most probable number. The Landau distribution is not an accurate description of energy loss in thin absorbers, such as CMOS sensors. For thin, absorbing layers, the most probable energy loss can

be calculated adequately [17] but its distribution becomes significantly wider than the Landau width. Thinner absorbing layers exhibit larger deviation from the Landau distribution.

The energy loss distribution has implications on the ideal detector thickness. Thin detectors are preferred due to lower Coulomb scattering and due to smaller probability that a δ-electron that is capable of traveling large distances modifies the shape of the electron cloud. Such spread of the charge will result in lower tracking accuracy. On the other hand, the energy distribution in thin detectors is much wider than the Landau curve. The low energy tail is closer to the noise of the detector, decreasing therefore the signal-to-noise ratio (SNR or S/N). Good separation of signal and noise is crucial for detector performance (high S/N). Practical detector systems accept signals above certain threshold. If the threshold is too low, false hits can be generated by temporal noise fluctuations. On the other hand, if the threshold is too high, part of signal from the low-energy tail of the distribution can be rejected, lowering the detection efficiency.

Energy loss by photons

A photon interacting with matter loses its energy and/or is scattered through several different physics processes. The contribution of different processes depends on the photon energy. Bellow is a short summary of the aspects of these interactions that are relevant to this thesis.

At low energies, the photoelectric effect dominates. A photon is absorbed and its energy is transferred to an electron. If the energy is sufficient to extract an electron from the atom, the electron, called photoelectron, is excited from the valence band to the conduction band and an electron-hole pair is generated. The remaining energy is transferred to the photoelectron as kinetic energy. If the later is sufficient, the photoelectron can produce secondary ionization along its trajectory.

Other interactions that contribute to energy loss and become more important for higher energies include Rayleigh scattering (also known as coherent or elastic scattering) and Compton scattering (known as incoherent or inelastic scattering). The Rayleigh scattering is the scattering of electromagnetic radiation by particles that are small in relation to the wavelength of the light. The photon changes its direction but preserves its initial energy and atoms are neither ionized nor excited. The Compton scattering (effect) is the interaction between photons and electrons free or loosely bound in atoms. The electron is given part of the energy and recoils while the photon carrying the remaining energy is emitted in a different direction from the initial one, so that the overall momentum of the system is conserved[1].

For high energy photons, the pair production process becomes dominant. Formation of an electron/positron pair is possible when a photon, which has a total energy of at least twice the rest mass of an electron (1.022 MeV), interacts with an atomic nucleus. A direct conversion of radiant energy into matter is possible in the vicinity of an atomic nucleus that allows for momentum conservation. The positrons quickly disappear by being reconverted into photons in the process of annihilation with other electrons.

Soft X-rays (photons with energies below 10 keV) interact with silicon predominantly through the photoelectric effect. The average energy required for an electron-hole pair generation in silicon is about 3.6 eV. In pixel detectors discussed in this work, soft X-rays will produce many electron-hole pairs in a small, point-like spatial region.

[1]The effect, discovered in 1922, demonstrates the nature of the photon as a true particle with both energy and momentum (the wave-particle duality of electromagnetic radiation).

A method used at IPHC for MAPS calibration, also exploited in this work, utilizes an ^{55}Fe source. The source emits photons in two γ emission modes with energies of 5.9 keV and 6.5 keV. The yield of the latter mode is only about 11% of the first mode [20]. The attenuation lengths for these photons in silicon are 29 μm and 37 μm, respectively [21]. The energy of these photons is sufficient to allow them to penetrate the whole active volume of the MAPS sensors discussed in this work. This active volume is the epitaxial layer with the thickness on the order of ten micrometers. A 5.9 keV photon will generate approximately 1639 electron-hole pairs in a silicon detector.

2.2 Silicon detector physics

Silicon is a semiconductor material[2] that is very widely used for radiation detectors based on solid-state medium. It offers good energy and excellent position resolution. Currently, it is the preferred material for high precision tracking detectors. The energy band gap of 1.12 eV at room temperature is low enough to allow abundant production of charge carriers by an ionizing particle (about 80 e-h pairs per micron track length for a MIP), but high enough to avoid high leakage current from electron-hole pair generation at room temperature. In addition, the high stopping power[3] of silicon (3.8 MeV/cm for a MIP) allows for large signals spawned in thin detectors. Silicon, as a relatively low Z material, is well suited for tracking detectors where multiple Coulomb scattering is of concern. Physical properties of silicon are summarized in Appendix A.2

Typically, it is preferred that the silicon detector volume be fully depleted. The presence of an electric field in the active volume allows fast charge collection on sensing electrodes. This speeds up the detector response and improves charge collection efficiency. Carriers moving faster in an electric field are less probable to become trapped in the lattice defects and the recombination rate becomes lower as electrons and holes move in opposite directions. However, this is not the case in MAPS devices discussed in this thesis. MAPS are fabricated using standard CMOS processes and are not compatible with high electric fields. The electric field is present only in the vicinity of the electrode and the charge from the undepleted active volume is collected through thermal diffusion.

The other major advantage of using silicon in tracking detectors is the existing and very advanced integrated circuit technology based on this material. IC technology, driven by the mass consumer market, allows reliable mass production of circuits with continuously decreasing feature size thanks to the advanced photolithography used in modern VLSI processes. Detector fabrication can take full benefit from the well developed planar processing technology used for ICs. Detectors with very high granularity can be constructed. Fabrication steps in a typical planar process are explained in details in [22]. In addition, integrating readout electronics and the detector volume in the same substrate is possible. MAPS discussed in this work are an example of monolithic detectors that are being developed for tracking detectors in HEP.

[2]Semiconductors have electrical conductivity (reciprocal of the resistivity) that can be controlled over a wide range. At room temperature, it is between that of a conductor and of an insulator. At high temperatures, the conductivity approaches that of a metal, and at low temperatures the material acts as an insulator.

[3]Stopping power is the property of a material that is numerically equal to the average energy loss of the particle per unit path length.

As it has been presented, silicon detectors are of particular interest to physicists working in the HEP domain. They are also used in other scientific applications, including medical imaging and space sciences. However, their main and the widest use is for detecting visible light in the mass consumer market for digital cameras and camcorders.

2.2.1 Silicon detector

In general, silicon detectors work as ionization chambers with detector electrodes inducing electric field in the medium. Absorbed radiation liberates charge carrier pairs, electrons and holes, which are separated in the electric field and induce currents in the external circuit. A high electric field in the detecting volume allows fast detector response and minimizes charge trapping that can affect charge collection efficiency. Some fabrication technologies, including widely available CMOS processes, restrict the maximum voltage allowed in the detector volume. In this case, the charge collection process results from drift in the electric field in the limited volume near the electrodes and from thermal diffusion elsewhere. The signal current is generally small (the peak value of this current is on the order of 10 nA), therefore, the dark current in the medium has to be limited. This necessitates the use of high resistivity materials[4].

In semiconductors, the conduction band is empty only at 0 K. At higher temperatures, the thermal excitation can elevate electrons form the valence band to the conduction band, leaving holes behind. A semiconductor that contains approximately the same number of holes in the valence band and electrons in the conduction band is called intrinsic[5]. The density of free electrons, n, and holes, p, is given by

$$n = N_C \exp\left(-\frac{E_C - E_F}{kT}\right) \quad \text{and} \quad p = N_V \exp\left(-\frac{E_F - E_V}{kT}\right) \tag{2.3}$$

where k is the Boltzmann constant, T is the absolute temperature, E_C and E_V are conduction and valence energy levels, E_F is the Fermi level - the energy at which the probability of occupation by an electron is exactly one half.[6], and N_C, N_V are the effective densities of energy states in the conduction and valence bands, correspondingly, given by

$$N_{C,V} = 2\left(\frac{2\pi m_{e,h} kT}{h^2}\right)^{3/2} \tag{2.4}$$

with $m_{e,h}$ representing the effective mass of electrons and holes respectively, and h is the Planck's constant. The intrinsic carrier density is expressed by n_i:

$$np = n_i^2 \tag{2.5}$$

. Equation 2.5 is called the *mass action law* and is valid in thermal equilibrium. At room temperature, n_i for silicon is on the order of 10^{10} cm^{-3}.

[4]The resistivity is a function of the number of free carriers.

[5]In practice, intrinsic semiconductors contain a small amount of impurities that introduce additional electrons or holes.

[6]The probability that an electronic state with energy E is occupied by an electron is given by the Fermi-Dirac distribution function: $F(E) = 1/\left(1 + e^{(E-E_F)/kT}\right)$

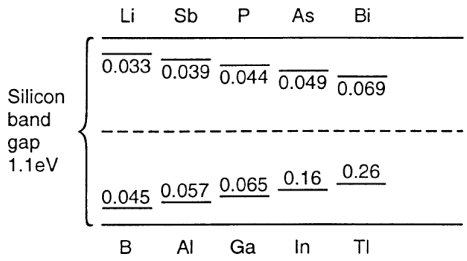


Figure 2.3: Energy levels in the silicon band gap introduced by various donor and acceptor dopants.

The resistivity of the semiconductor is given by

$$\rho = \frac{1}{q(n\mu_e + p\mu_h)} \tag{2.6}$$

where $q = 1.602 \times 10^{-19}$C is the elementary charge, μ_e, μ_h are the mobilities of electrons and holes, respectively.

The resistivity of pure silicon is approximately 400 kΩ·cm at 300 K. In practice, the resistivity is reduced by more than one order of magnitude due to the imperfections of the crystal lattice and minute impurity concentration. However, it is still possible to achieve a high-field region with a low DC current by using a reverse-biased p-n junction (diode).

The conductivity of semiconductor can be adjusted by adding, in a controlled manner, small amounts of impurities. This process is called doping. Required concentrations range from $10^{11} - 10^{20}$ cm^{-3}, compared to the number of Si atoms in a lattice, about 5×10^{22} atoms/cm^3. Impurities replace silicon atoms in the crystal structure and create additional energy levels in the band gap. Such semiconductors are called extrinsic. In a crystal structure, four electrons in the valence band are needed to create a covalent bonding[7]. Dopants that have five (e.g. phosphorus, P) or three (e.g. boron, B) valence electrons are called donors and acceptors, respectively. They introduce additional electrons (holes) into the conduction (valence) band leaving the atom charged positively (negatively). For shallow levels of doping, almost all dopants become ionized at room temperature ($kT = 26$ meV). For example, phosphorus and boron introduce in silicon donor and acceptor levels at $E_d = E_C - 0.044$ eV and $E_a = E_V + 0.046$ eV, respectively. Figure 2.3 shows energy levels introduced into silicon by various dopant atoms.

As a result, the electron density is equal to the donor concentration ($n = N_D$) and the hole density is equal to the acceptor concentration ($p = N_A$). The mass action law, $np = n_i^2$, is also valid here. The increase in the number of one type of carriers results in the reduction of the number of the other type of carriers through recombination and the product of the two remains constant at a given temperature. If the concentration of donors exceeds the concentration of acceptors, the material is called n-type. It is called p-type if the opposite is true. For intrinsic material, the Fermi level is in the middle of the band gap. In material with donor impurities, the Fermi level is near the valence or conduction band edge for p- and n-type material, respectively.

P-type and n-type regions joined in a single crystal semiconductor material form a p-n junction. Holes from the p-side diffuse into the n-side and electrons from the n-side diffuse into the

[7]Covalent bonding is a description of chemical bonding that is characterized by the sharing of pairs of electrons between atoms; each electron pair constitutes a covalent bond.

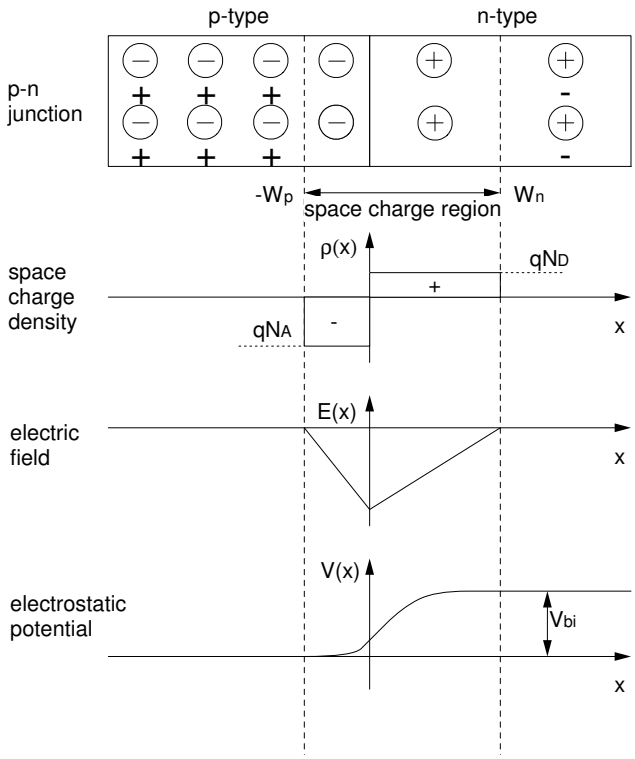


Figure 2.4: Approximation of an abrupt p-n junction: space charge density, electric field distribution, and electrostatic potential distribution are shown in and outside of the space charge region.

p-side. Ionized dopant ions in the vicinity of the junction become uncompensated and cause a negative space charge in the p-side and positive space charge in the n-side. An electric field builds up that impedes the further diffusion of charge. This creates a region free of mobile carriers called *depletion region* or *space-charge region*. The electrostatic potential difference across the depletion region at thermal equilibrium is called *built-in potential*:

$$V_{bi} = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} \tag{2.7}$$

where N_A and N_D are concentrations of acceptors and donors, respectively.

Assuming an abrupt transition of doping concentration between the n- and p-type regions (abrupt junction)[8] and solving the Poisson's electric potential equation[9], the width of the depletion region is found to be:

$$W = \sqrt{\frac{2\epsilon_{Si}\epsilon_0}{q} \left(\frac{N_A + N_D}{N_A N_D} \right) V_{bi}} \tag{2.8}$$

[8]This approximation is appropriate for a p-n junction created by shallow diffusion or low-energy ion implantation. The impurity profile in a junction created by deep diffusion or high-energy implantation is more accurately described by the linear variation of the impurity distribution across the junction (linearly graded junction).

[9] $\frac{d^2\Psi}{dx^2} = \frac{\varrho_s}{\epsilon_{Si}\epsilon_0}$, where ϵ_{Si} and ϵ_0 are the dielectric constants of silicon and the permittivity of vacuum, respectively.

A typical model of a p-n junction is presented in Figure 2.4. The depth of the depletion region in each side of the junction is inversely proportional to the doping concentration[10]. In detector diodes, the doping in one side of the junction is typically a few orders of magnitude higher and the depletion region extends essentially only into the less doped region, bulk. Equation 2.8 can be written as

$$W = \sqrt{\frac{2\epsilon_{Si}\epsilon_0 V_{bi}}{qN_B}} \tag{2.9}$$

where N_B is the lightly doped bulk concentration. The width of the depletion region can be increased by applying external reverse bias voltage, i.e., with the same polarity as the built-in potential. The width of the depletion region increases only as a square root of the applied voltage. Typically 60 to 100 volts are required to significantly deplete a lightly doped bulk of a silicon detector that is generally made on a wafer with a 300 μm thickness. The detector full depletion voltage can be extracted from Equation 2.9. The maximum voltage applied to the junction can not exceed its breakdown voltage[11].

The depletion region is bounded by conductive n- and p-type regions. It can be regarded as a parallel plate capacitor with a capacitance expressed as:

$$C_j = \frac{\epsilon_{Si}\epsilon_0 A}{W} = A\sqrt{\frac{q\epsilon_{Si}\epsilon_0 N_B}{2(V_{bi} - V_B)}} \tag{2.10}$$

where V_b is the reverse bias voltage and A is the plate area.

In the case of particle detectors, a larger depleted volume translates to a larger sensitive volume and decreased node capacitance. This translates to increase in the signal charge and increase of the S/N.

Charge collection

Transport of free carriers in a semiconductor bulk occurs through diffusion and drift. Thermal energy causes the random movement of carriers and their scattering on the lattice and impurity atoms. The random motion leads to a zero net displacement. A typical average distance between collisions (mean free path) is about 10 μm with the average time between collisions (mean free time) of about 1 ps. In silicon at room temperature, the mean velocity of electrons is about 10^7 cm/s. In the presence of inhomogeneous distribution of free carriers, the statistical outcome of the random motion will yield net movement of free carriers from high to low concentration. The process results in the diffusion current with direction opposite to the concentration gradient.

The presence of the electric field causes carriers to move parallel to the field. All the momentum gained by carriers in the electric field is lost in the frequent collisions with the lattice,

[10]This follows from the neutrality of the overall space charge in the semiconductor: $N_A x_p = N_D x_n$, where x_n and x_p are the depletion widths in the n-type and p-type region, respectively.

[11]For a high reverse voltage, a junction can break down and conduct a very large current. An upper limit on the reverse bias for most diodes is imposed by the avalanche multiplication mechanism. A thermally generated electron gains kinetic energy from the electric field. If the field is sufficiently high, the electron can create additional e-h pairs via impact on lattice atoms (impact ionization). This process can be cascaded resulting in an avalanche multiplication.

therefore, equilibrium is obtained and the drift velocity is proportional to the electric field:

$$\vec{v} = \mu\vec{E} \tag{2.11}$$

where μ is the mobility[12] in units of $\mathrm{cm}^2/\mathrm{Vs}$.

The carrier flow due to drift and diffusion gives rise to current densities for electrons and holes that are expressed as:

$$J_n = q\mu_e nE + qD_e\frac{dn}{dx}n \quad \text{and} \quad J_p = q\mu_h pE - qD_h\frac{dp}{dx}p \tag{2.12}$$

where $J_{n,p}$ is the net current density of electrons, holes. The first component is the drift current and E is the electric field in the x direction. The second component is diffusion current and $D_{n,p}$ is the diffusion constant (diffusivity). The diffusion constant and mobility are related through the Einstein relation $D = \frac{kT}{q}\mu$. In a p-n junction in thermal equilibrium, the net currents of holes and electrons are equal zero.

Electrons and holes in silicon have mobilities of 1400 and 480 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$, respectively. The mobility is constant for fields up to about 10^4 V/cm and the drift velocity is a linear function of the electric field. In high fields, $> 10^5$ V/cm, the mobility is proportional to $1/E$ and the drift velocity is saturated at about 10^7. In a fully depleted detector, the charge collection time depends on the electric field and typical values for silicon with the resistivity of 10 kΩ are on the order of 10 and 30 ns for electrons and holes, respectively. However for a partially depleted detector, the collection time is independent of the bias voltage, and depends only on the carrier mobility and doping concentration in the bulk material, yielding, for the same material, three times longer collection times [13].

Signal current

Charge generated in the sensitive volume does not have to be collected to induce signal current. Signal current is generated by charge moving in the sensitive volume of the sensor through charge induced on the collecting electrodes. Quantitative description of this problem is described by Ramo's theorem [23]. The validity of the Ramo's theorem is very wide as it applies to all structures that register the effect of charges moving in an ensemble of electrodes. It is not affected by dielectric properties of the material between electrodes and neither by the presence of space charge.

The theorem states that the amount of induced charge, Q, is given by the product of the charge placed in a given point between electrodes and the signal weighting potential at this point. Charge q moving along any path from position 1 to position 2 induces charge on electrode k according to:

$$\Delta Q_k = q(\Phi_k(2) - \Phi_k(1)) \tag{2.13}$$

where Φ is the *weighting potential* that describes the coupling of a charge at any position to the electrode k. The instantaneous current through the electrode k can be expressed in terms of the weighting field determined for this electrode

$$i_k = -q\vec{v}\vec{E}_w \tag{2.14}$$

[12] $\mu = q\tau_c/m_{eff}$, where τ_c is mean free time and m_{eff} is the effective mass of the carrier, either electron or hole.

where $\vec{E}_w = -\nabla\Phi$ is the weighting field, and $\vec{v}$ velocity of motion of the generated charge carrier.

The weighting field is determined by applying unit potential to the measurement electrode and zero to all others. This field depends only on geometry of the electrodes. Therefore, generally, the electric field is different from the weighting field, and they are the same only for two electrode configurations. The actual field defines the trajectory and velocity of the charge. The weighting field determines the coupling between the moving charge and the electrode. In general, if a moving charge does not terminate on the measurement electrode, the induced signal current changes sign and integrates to zero. The current cancelation on non-collecting electrodes relies on the motion of both electrons and holes. In multi-electrode systems the instantaneous current from one electrode must balance the sum of currents from other electrodes. In case of strip or pixel detectors, the weighting potential is highest near the signal electrode; therefore, most of the charge is induced when the moving charge is near or terminates on the signal electrode.

2.2.2 Electronic noise

The figure of merit for a tracking detector system is the tracking resolution and detection efficiency. Simplifying, one can say that the first parameter depends on the geometry and material properties of the detector. The second parameter depends on the effectiveness of distinguishing between signals generated by ionizing particles (real hits) and noise fluctuations (fake hits). Therefore, the detection efficiency depends on the signal-to-noise ratio in the detector. Typically the amplitude of the signal is limited due to physics or detector limitations. Therefore, noise performance can become a critical issue. Noise in a detector system can result from many sources of internal and external origin. The external sources, such as electromagnetic interference or power supply fluctuations, can often be minimized to a negligible level by proper circuit design techniques or shielding and grounding. The internal, electronic noise sets the limits on the ability to distinguish and precisely measure signals.

The electronic noise in a detector system can be assigned to two mechanisms related to current flow. When N charge carriers move with a velocity v through a sample of length l bounded by two electrodes, they induce a current I:

$$I = \frac{qNv}{l} \tag{2.15}$$

The fluctuation of the current is given by

$$\overline{dI^2} = \left(\frac{qN}{l}\overline{dv}\right)^2 + \left(\frac{qv}{l}\overline{dN}\right)^2 \tag{2.16}$$

where the two terms are added in quadrature as statistically uncorrelated.

These are fluctuations of the carrier velocity due to thermal excitations, *thermal noise*, and fluctuations in the number of charge carriers when carriers are injected into a sample independently of each other. The latter can be assigned to a carrier flow over a potential barrier (e.g. current flow in a semiconductor diode), where the probability of an individual carrier crossing the barrier is independent from others and results in a random process, *shot noise*. This can be also due to random generation and recombination processes in a reverse biased diode. Another source of fluctuations in the number of carriers is carrier trapping on impurities and imperfections in a

crystal lattice. The traps acquire carriers and release them with a characteristic time constant resulting in a non-random fluctuation. This leads to a frequency dependent power spectrum $1/f^{\alpha}$, where α is typically in the range of 0.5-2. Therefore, the noise with such spectral distribution is called *1/f* or *flicker noise*. Thermal noise and shot noise both have spectral densities that are independent of frequency. They are classified as white noise for which the power per unit bandwidth is constant. Spectral density of low frequency noise (flicker or 1/f noise) is inversely proportional to the frequency. All the noise sources mentioned here are characterized by zero mean value.

Thermal noise depends on temperature but not on current flow. The most common example of noise due to velocity fluctuations is the thermal noise of resistors. The spectral noise power density is expressed as $dP_n/df = 4kT$. Therefore, the voltage and current spectral noise densities for a resistor are, accordingly, expressed by

$$\frac{dV_n^2}{df} = v_n^2 = 4kTR \quad \text{and} \quad \frac{dI_n^2}{df} = i_n^2 = \frac{4kT}{R} \tag{2.17}$$

where k is the Boltzmann constant and R is resistance.

Another common device that exhibits thermal noise is a MOS transistor, in which the noise is generated by the drain-source resistance[13]. The spectral noise current density can be described for the linear and saturation region as

$$i_n^2 = \frac{8kT}{3} g_m \tag{2.18}$$

where g_m is the transconductance of the transistor.

The generated noise can be compared with input signal by division of i_n^2 by g_m^2. The input referred noise is given by:

$$v_{nin}^2 = \frac{8kT}{3} \frac{1}{g_m} \tag{2.19}$$

This noise occurs in series with the gate.

Shot noise depends only on the current flow and is independent on the temperature. The example is current flow through a p-n junction as in a detector diode or a bipolar transistor. The spectral noise current density is expressed by

$$i_n^2 = 2qI \tag{2.20}$$

where I is the average current flowing through the junction. Shot noise is related to an independent injection of carriers. It is not the case in an ohmic resistor, where $I = V/R$, and any fluctuations are compensated by additional carriers.

Flicker noise is associated with both resistive regions and potential barriers and is proportional to the current flowing through an electronic device. For a detector diode, the flicker noise adds to the shot noise (Equation 2.20) and is expressed as

$$i_n^2 = \frac{K_F I_D}{A_D} \frac{1}{f} \tag{2.21}$$

[13]The drain-source resistance in the linear region approximately equals the inverse transconductance $1/g_m$ in the saturation region. Due to field effects in the channel the noise is reduced by a factor of about 2/3 [24].

where K_F is a technological noise constant, A_D is the size of the diode, and I_D is the constant current. A MOS transistor also suffers from flicker noise, which results mainly from the traps in the gate oxide - silicon interface. The current spectral density and input referred noise for a transistor in saturation are modeled with

$$i_{nf}^2 = \frac{K_{Ff} g_m^2}{WLC_{ox}^2} \frac{1}{f} \quad \text{and} \quad v_{inf}^2 = \frac{K_{Ff}}{WLC_{ox}^2} \frac{1}{f} \tag{2.22}$$

where K_{Ff} is a technological constant, W and L are gate dimensions and C_{ox} is gate capacitance.

Total noise of the detector system depends on the frequency range or bandwidth of the complete signal processing chain. Typically, signal in the system has a spectrum that is much narrower than the noise spectra. Therefore, optimizing the frequency response of the system can improve signal-to-noise ratio. The total noise is obtained by integrating the noise power over the bandwidth. The output noise of a voltage or current amplifier with a frequency dependant gain $H(f)$ is expressed by:

$$v_{no}^2 = \int_0^{\text{inf}} v_n^2 H^2(f) df \quad \text{or} \quad i_{no}^2 = \int_0^{\text{inf}} i_n^2 H^2(f) df \tag{2.23}$$

Customarily, detector readout systems that measure signal charge are characterized in terms of equivalent noise charge or ENC. This is the charge that would equalize the output signal to the noise level. In other words, it is a charge that yields signal-to-noise ratio equal to one. The value is derived based on the output noise of the system, which is a combination of all noise contributions within the system's bandwidth.

2.2.3 Radiation damages

Electromagnetic radiation passing through silicon detectors can cause transient and permanent effects. Some effects can affect the detector performance and their negative impact is refereed to as radiation damage. As the energy of electromagnetic radiation increases the effects become more severe. At energies above 10 eV, electron-hole pairs in silicon dioxide start to be generated. Although most of them will recombine, as the energy increases hot carriers are more likely to cause surface damage at the silicon-silicon dioxide interface. Energies exceeding 250 keV can force silicon atoms from their lattice sites resulting in *displacement damage*.

Atom displacement in the bulk degrades minority carrier lifetime. Typical effect is the degradation of gain and leakage current in bipolar transistor. Since the operation of MOS transistors does not depend on minority carriers, the bulk damage does not have much impact on these devices. In case of silicon detectors, the bulk damage is mostly damaging to the charge collection rather than to the readout electronics. This is opposed to the surface damage that results from ionizing radiation. Ionizing radiation introduces interface defects and trapped charges, which lead to shifts in threshold voltages and affect the operating point of transistors. Therefore, it mostly degrades the performance of the readout electronics.

The radiation damage degrades the S/N performance of a detector. Signal is limited due to lower charge collection resulting from charge trapping, and lower mobility and lifetime of charge carriers. At the same time, noise is augmented mainly due to the leakage current increase. Radiation tolerant detectors and readout electronics are required for scientific applications where

harsh radiation environment is present (particle physics experiments, space and military applications). This is especially important for tracking devices in particle physics experiments, where the detector is close to the interaction point and is subject to a very high particle flux.

Displacement damage

High energetic particles can interact with the silicon crystal and displace its atoms from normal lattice locations[14] causing displacement damage. When a particle displaces the primary knock-on atom, it creates an interstitial and a vacancy in the lattice. If the recoil atom has sufficient kinetic energy it may knock out additional atoms and lead to cascades. The recoil atoms lose their energy due to ionization and further displacements, however, at the end of their range, non-ionizing interactions prevail leading to clusters of defects. The interstitials and vacancies can migrate in the lattice. They can recombine and repair the defects or combine with impurities (oxygen, carbon, dopant atoms) and form permanent defects.

An isolated atom displacement, classified as point damage, is characteristic to high energy electromagnetic radiation (photons, electrons). Large assemblage of defects, referred to as a cluster, results from interaction of massive particles such as protons and neutrons. The threshold energy for displacement of the primary recoil atom in silicon is 25 eV. A recoil Si atom needs about 5 keV of energy to displace other Si atoms in the crystal. A 50 keV recoil silicon nucleus can create clusters of damage, typically, over a volume of several hundred ångströms. An electron needs about 260 keV of energy to displace a Si atom and more than 5 MeV to generate clusters. The energy of a neutron causing the same damage is 190 eV and 15 keV for point defects and clusters, respectively [25, 26, 27].

To a good approximation, displacement damage effects produced by different particles over a wide range of energies are proportional to the non-ionizing energy losses (NIEL) of the incident particle. The NIEL expresses energy lost to non-ionizing events per unit length (MeV/cm or MeV cm^2/g). Frequently, for different particles, NIEL is normalized to 1 MeV neutron.

The defects in the crystal structure introduce additional energy levels within the silicon bandgap, affecting properties of the device. The additional donor-like and acceptor-like energy levels can trap charge carriers, seriously degrading the minority carrier lifetime that is inversely proportional to the number of the point defects and their capture cross section. These additional generation-recombination centers reduce the carrier mobility and introduce additional leakage current in a depleted material.

The radiation induced bulk damage has an important impact on macroscopic properties of the device, especially fabricated from a detector grade material (high quality, high resistivity, low doped ($\sim 10^{12}$ cm^{-3}), long minority carrier lifetime):

- modified effective dopant concentration (donors and acceptors compensate material) affects the full depletion voltage. It can also lead to inversion of the conduction type (n-type to p-type) for high irradiation doses.

- increased bulk dark current, related to cluster damages, may result in large spatial non-uniformities of dark current in the detector. In the case of pixel sensors, cells with dark current significantly above its average value are referred to as *hot pixels*. Generally, dark current can be significantly reduced by operating the detector at low temperature.

[14] This can happen through high energy transfer in atomic collisions or nuclear interactions

- degradation of the charge collection efficiency that results from trapping of drifting or diffusing charge carriers. Charge traps are characterized by different time constants and, in addition, capture and emission processes are temperature dependent [26]. Electrons trapped and not released in time to be collected with the rest of the signal charge packet account for charge losses. The charge collection inefficiency can be minimized for detectors operated at high temperatures, where the quick release will allow electron to join its charge packet, and at low temperatures, where the trap will remain occupied for a long time and not interfere with later packets.

Ionization damage

Direct ionization of medium can lead to radiation damage located at the interface of silicon and silicon dioxide. The band gap in silicon dioxide is 8.8 eV and the average energy of about 18 eV is needed to generate an electron-hole pair. Most of the charge recombines without inducing any negative effects; however, a small fraction of the original charge will migrate and become trapped, creating zones of space charge.

Traps at the Si-$Si0_2$ interface result from the presence of strained or dangling silicon bonds and their amount depends on the processing parameters, for example oxidation temperature. Ionizing radiation will further increase the amount of interface traps. Trapping centers will affect charge collection in the detector. Traps acting as generation-recombination centers will increase recombination rate at the interface, leading to increased leakage current.

Charge trapping mechanism in the oxide is related mostly to positive charge carriers. The holes have mobility orders of magnitude lower compared to electrons, while their capture cross section near the interface is higher. Therefore, holes become blocked in the oxide while electrons are removed shortly after they are generated. The holes are grouped near the Si-$Si0_2$ or polysilicon gate - $Si0_2$ interface for the positive and negative gate biasing voltage, respectively. The effect is stronger in regions of a device where the thick oxide (field oxide) is present. The charge buildup induces a flat-band voltage shift. In the case of p-type substrates, commonly used in CMOS processes, it can result in an inversion layer which can short n-implants in the substrate. In addition, the charge accumulated at the ends of an NMOS transistor gate with a classical rectangular shape may prevent the device from switching off completely. Careful design practices can eliminate both problems. Widely used techniques include p+-type guard-rings separating n-type regions and the enclosed gate NMOS transistor layout [28]. An example of the enclosed gate transistor layout in a MAPS pixel cell is shown in Figure 2.5.

Apart from the design techniques that increase radiation tolerance of readout electronics, detector properties depend on the fabrication process. Since the amount of the trapped charge carriers is proportional to the number of defects, it is crucial to control the gate oxide quality in radiation hard technologies. In modern, sub-micrometer processes used for integrated circuit fabrication, the gate oxide thickness is significantly reduced compared to older technologies. As the result, the radiation induced threshold voltage shift and increase in the surface states density are very small. Modern chips can withstand doses of tens of megarads[15].

[15] 1 rad=0.01 Gy

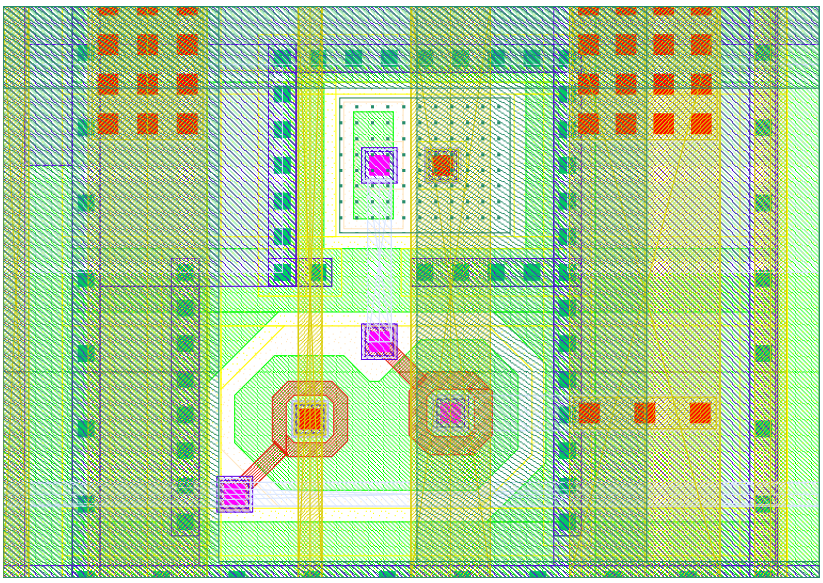


Figure 2.5: A section of the MIMOSTAR2 pixel layout. The charge collecting diode, visible in the upper center part of the picture, is read out through two enclosed layout transistors, which are visible in the bottom center part of the image.

Single Event Effect

In addition to the described effects of ionizing radiation on detector performance, incident high-energy ionizing particles may interfere with readout electronics. This is referred to as a *single event effect* (SEE) and often is classified as a *single event upset* (SEU) or a *single event latch-up* (SEL) condition. The first effect can cause soft errors that are not destructive to the circuit by definition, but the latter one may result in permanent damage. This is particularly a concern for space application, but it can also be dangerous to tracking detectors that have readout electronics exposed to the high-particle flux environment. Both effects can be recovered from by power cycling the circuit.

SEU happens when the traversing particle that loses energy through ionization leaves behind a wake of electron-hole pairs. Typically SEU appear as transient pluses in analog circuitry (glitches), or as bit flips in memory cells or registers.

Latch-up is the inadvertent creation of a low-impedance path, typically, but not only, between the power supply rails of an electronic component that triggers a thyristor-like parasitic structure, which acts as a short circuit. Increasing density and circuit complexity in modern VLSI CMOS devices makes them more susceptible to this effect. Latch-up can be triggered by ionizing particles as well as by electrical over stress event (transient over-voltage, circuit switching noise).

Parasitic bipolar PNP and NPN transistors present in CMOS processes form the PNPN structure of a thyristor. Location of the components of a parasitic thyristor in a CMOS device is shown in Figure 2.6. If either of the transistors is forced into conducting current, the second one will follow and both of them will be biasing each other in the loop of positive current feedback. If either of the emitter/base junctions is forward biased, emitter currents will be sourced to base/collector regions and, if the current is high enough, the junctions will be forward biased and

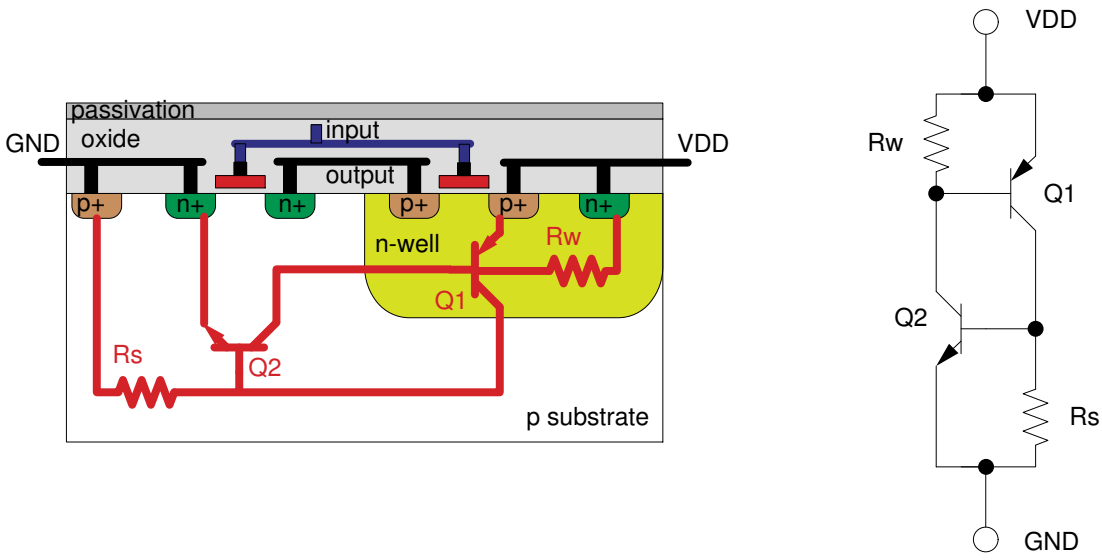


Figure 2.6: A cross section through a typical CMOS device with highlighted elements of a parasitic thyristor.

the condition can be sustained - thyristor enters the conducting mode. The latch-up condition is stable for as long as the holding current required by the PNPN path can be delivered. The shunting resistors across the base-emitter junctions divert base drive from the bipolar transistors and, consequently, increase both the trigger current and holding current levels required for the structures to participate in latch-up. Minimizing this resistance will increase the trigger current and holding current levels required for latch-up. A sustainable latch-up action can result in a high operating current that can destroy the device due to excessive heating and metallization or bond wire failure. The latch-up action is removed by powering down the circuit.

Susceptibility of circuits to latch-up can be decreased to some extent with layout techniques (guard rings, spacing, well geometry and contact placement). However the biggest impact comes from the fabrication technology. Commercial processes may feature retrograde wells[16] and LOCOS[17](bird's beak), which are replaced with STI[18] in more recent processes, used for separation of components. Commonly used epitaxial layer allows the use of a separate layer of substrate silicon, with a resistivity about three orders of magnitude lower than the epitaxial layer. This increases the holding current for latch-up as the base-emitter shunting resistor is decreased (small resistance from the bulk connected in parallel to high resistance within the epitaxial layer). A comparison of bulk and epitaxial CMOS technologies is presented in Appendix A.3. Devices fabricated in the SOI technology, described in section 2.4.1, are inherently latch-up resistant.

[16]The highest concentration of dopants implanted in the well is located at a certain distance from the surface

[17]Local Oxidation of Silicon - isolation scheme commonly used in MOS/CMOS silicon technology. A thick (in the range of 500 nm) pad of thermally grown SiO_2 separates adjacent devices, e.g. PMOS and NMOS transistor in CMOS structure.

[18]Shallow Trench Isolation - the process involves etching a pattern of trenches in the silicon, depositing one or more dielectric materials (such as silicon dioxide) to fill the trenches, and removing the excess dielectric using a technique such as chemical-mechanical planarization.

2.3 Pixel detectors

The purpose of a tracking detector is to provide spatial information about the path of a traversing ionizing particle. A silicon detector used for tracking requires that the sensitive volume be segmented to provide spatial resolution. This solution has been long used in microstrip detectors.

Strip detectors are composed of many strip segments, fully depleted p-n diodes, and each is associated with a metal electrode. The strips have fine pitch ($\sim$ 10 μm) but are typically very long (several centimeters). Therefore, they provide only one-dimensional tracking information. However, modifications of this basic structure exist to increase tracking capabilities. This includes double-sided microstrip detectors (strips are implemented on both sides of the silicon wafer) where two layers are shifted by an angle with respect to each other. Even this structure does not provide unique two-dimensional information about positions of traversing particles and cannot resolve correctly high density event topologies. Much higher segmentation (higher granularity) and unambiguous particle track reconstruction is required for areas where large track density is expected. In this environment, pixel detectors that deliver true two-dimensional pictures become necessary.

Planar processes used for fabrication of silicon detectors allow for segmentation of a detector into an array of pixels. The pixels are generally squared with a pitch as small as a few tens of micrometers. The pixel size depends on the technology and complexity of the pixel. A comparison of information obtained with pixel and strip detectors for an event topology of a jet with 3 particles is presented in Figure 2.7. In a double-sided strip detector, N particles produce $N!$ possible crossing positions. Solving ambiguities for more than just a few tracks would require complex detector structure arrangement (with strips differently oriented in all layers) and/or rely on external detectors. Pixel detectors provide unique two-dimensional information and tracks can be correctly and unambiguously reconstructed for very large fluxes. A pixel vertex detector that can be used as a stand-alone device for track recognition is a very powerful tool for physicists.

Pixel devices are of great interdisciplinary importance and are used both in consumer electronic products and scientific applications, including high-energy particle physics. The granularity provided by pixel detectors significantly improves the precision of event reconstruction due to better resolution and less ambiguous hit position compared to other detectors.

In tracking in HEP, it is important to note that the precision of the position measurement does not simply scale with the detector resolution. The measurement precision for particles with relatively low momentum might by limited by multiple scattering in the material between the interaction point and the detector layer.

Detector technologies that are most attractive for vertex and general purpose tracking detectors are Hybrid Pixel detectors (Chapter 2.3.1), CCD (Chapter 2.3.2), DEPFET (Chapter 2.3.3), and MAPS (Chapter 2.4.2). It should be noted, that other detectors that can provide two-dimensional resolution exist. This includes drift[19] [29] and pad detectors[20] [30, 31].

[19]Special biasing scheme of implants on both sides of the detector creates a channel where carriers (typically electrons) drift towards the collection electrode (n+-type pads at the edge of the device). One coordinate is given by pad electrodes. The second one is given by the time between the particle crossing and the arrival of electrons at the collecting electrode.

[20]An array of p-n diodes connected to individual readout channels (at the edge of the chip) by metal lines on top of the detector.

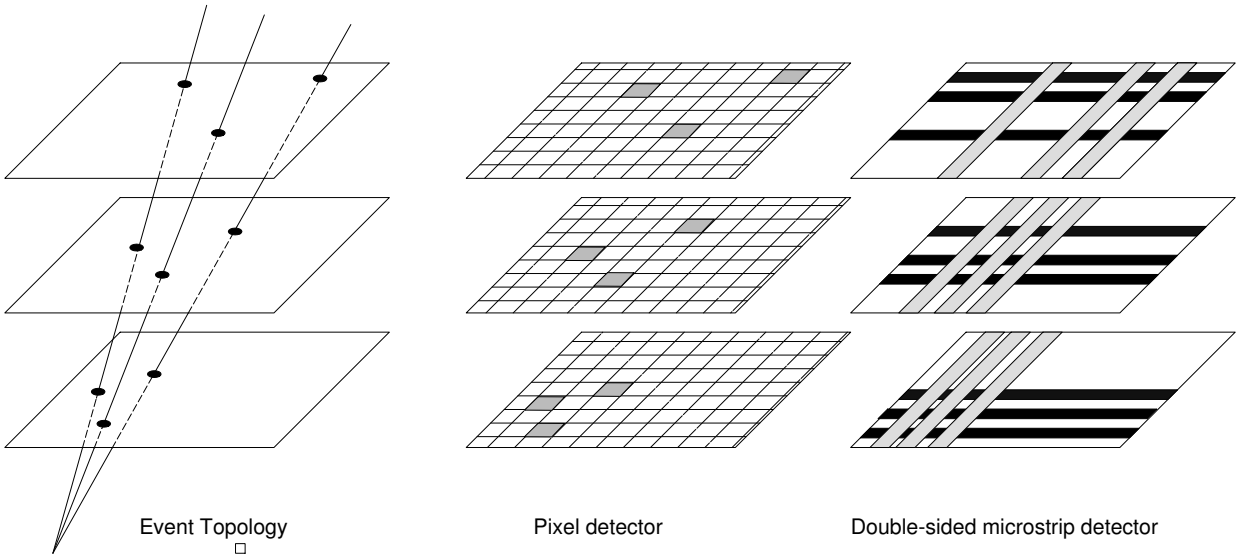


Figure 2.7: Three tracks passing three detector layers and the resulting information obtained with pixel and strip detectors. For clarity of the picture, the complete segmentation of the double-sided strip detector is not shown - only strips that collected charge are highlighted.

Microstrip detectors are still in common use especially for covering large surfaces where the track density is much smaller compared to the region close to the interaction. Microstrip detectors can be preferred due to the maturity of this technology and smaller silicon and readout electronics costs per surface area.

Position resolution delivered by a detector depends mostly on the geometry of the detector segments. Therefore, the most critical parameter is the pitch of pixels or strips. The simplest hit reconstruction resolution, where the hit position information is revealed by segments that fired (the signal passed a certain threshold), is referred to as a binary resolution. Each segment has a box-like response (uniform distribution) function. For tracks that are randomly spread, differences between the true positions and the measured ones have a Gaussian distribution with the standard deviation σ given by

$$\sigma^2 = \int_{-p/2}^{p/2} \frac{x^2}{p} dx = \frac{p^2}{12} \tag{2.24}$$

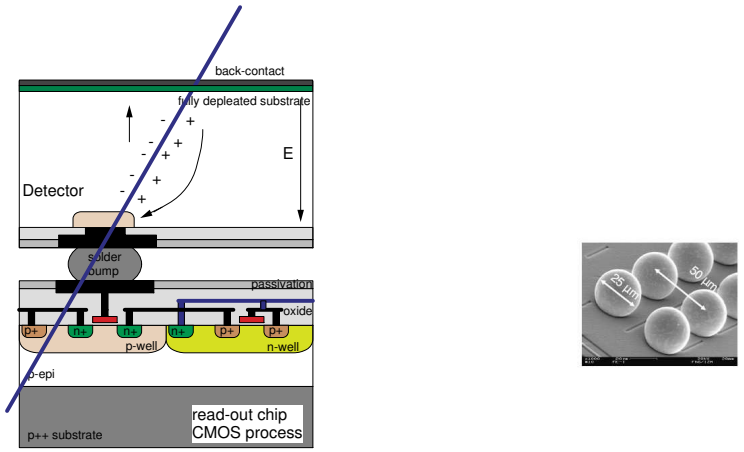
where p is the segment pitch in a given direction. This results in the position resolution defined by the segment pitch divided by $\sqrt{12}$. Very often pixel detectors have squared pixels, providing the same resolution in two dimensions. A detector with a pixel size of 30 μm $\times$ 30 μm allows, theoretically, reaching the binary resolution of about 8.5 μm.

The resolution can be further increased by taking the advantage of charge sharing between neighboring segments that form clusters. Charge clouds drifting towards detector electrodes experience also thermal diffusion. This might lead to charge spread over more than one detector segment. The information about fractional charge can greatly improve the position determination. The use of center-of-gravity or η algorithms is very common. A detailed description of these algorithms can be found in [32]. A detector with 30 μm pixels can provide spatial resolution of a few micrometers when these algorithms are used.

2.3.1 Hybrid pixels

Hybrid pixel detectors are built from two independently processed layers of silicon. One layer, based on high-resistivity silicon substrate or other semiconductor material, is the sensitive volume of the detector. The second layer contains the readout electronics, typically developed in a standard CMOS process. Both layers are interconnected in the final production stage. This approach gives the advantage of optimizing each layer according to its function: electronics for fast readout and signal processing with data sparsification, and the sensitive volume for radiation hardness. Typically the active volume is fully depleted to allow fast charge collection that also translates to a higher immunity to radiation.

The detector and readout electronics are, conventionally, connected together using the flip-chip and bump-bonding techniques [33]. An array of small balls of solder, indium or gold, is used to provide an electrical and mechanical connection between the two wafers. Essentially, the sizes of pixels on both chips need to be the same. The minimum size of the pixel is limited by the size of the pixel with readout electronics and by the size of the solder bond. The principle of a hybrid pixel detector is presented in Figure 2.8. The architecture, known from microstrip detectors, with interleaved pixels that are capacitively coupled to those that are readout, can be used to increase the spatial resolution capabilities.



(a) Detector structure

(b) Solder bumps

Figure 2.8: Cross-section view of a hybrid pixel detector (a): two separate silicon devices - detector chip and electronics chip - are connected together by solder bumps, (b), using bump bonding techniques.

Pixel detectors based on hybrid technology were successfully used in heavy-ion experiments, for example WA97, at SPS, CERN [34]. In the near future they will be used in the ATLAS [35], ALICE [36], and CMS [37] experiments at the LHC, CERN. The pixel size in present-day experiments utilizing hybrid pixels detectors are 150 μm by 150 μm (CMS) and 50 μm by 400 μm (ATLAS).

To summarize, hybrid pixels detectors offer highly optimized readout electronics coupled to a detecting part that can work in the most radiation harsh environments that are found near the collision point of relativistic particles. However, they have a series of disadvantages that limit

their practical use: limited granularity, very high complexity of interconnections, large amount of material they introduce, and relatively high power dissipation (a few hundred of mW/cm^2).

2.3.2 CCD

The charge coupled devices were first introduced in the early 1970's [38, 39]. CCDs are extensively used as imaging devices, especially in consumer electronics as visible light sensors, but also in space science [40] and as tracking detectors. They were successfully used as vertex detectors of NA32, a fixed target experiment at CERN SPS [41], and SLD [42]. CCDs provide thin detectors with very high granularity. The pixels size in the SLD vertex detector was 20 μm by 20 μm.

A CCD device is an array of MOS photocapacitors tightly covering the substrate. An appropriate voltage applied to the polysilicon gate changes the electrostatic potential in the silicon and forms a potential well that collects electrons created by incident radiation. The charge is confined in a single well by potential barriers created under neighboring gates in one dimension and channel stopper implants in the second dimension. When a proper biasing sequence is applied to the MOS gates, the stored charge packets can be transferred in parallel along each column in a shift-register way (Figure 2.9). A serial shift register is located at the bottom of the column that allows shifting samples to an output node for charge to voltage conversion. This process has to be completed for each raw of samples arriving from the pixel array. Different approaches can be used for making practical CCD devices: buried channel[21] can be used for transferring charge packets and different gate/electrode configurations and clocking schemes can be employed.

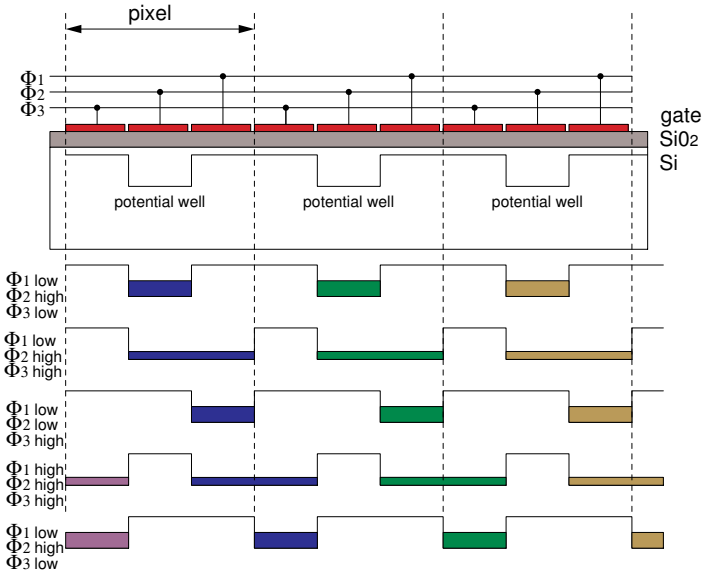


Figure 2.9: Typical CCD detectors have three gates over each pixel. High voltage over one of the gates creates a potential well just below the MOS gate, where electrons generated after a passage of an impinging particle are collected. An appropriate voltage sequence applied to the MOS gates shifts the charge to the edge of the detector where the signal is read out.

[21]The charge stored in the bulk of the silicon is approximately 1 μm below the surface. Buried channel replaced the early CCD technology, surface channel CCD, where charge was collected and transferred at the Si-SiO_2 interface.

The very high granularity complemented by a large area of the detector (millions of pixels) make CCDs a very attractive solution for tracking devices. However, the charge transfer is a relatively slow process and it takes a significant amount of time to read out a large sensor. An improvement can be expected from in-situ image storage and column parallel readout architecture [43]. Another limitation of CCDs used as tracking devices is their inherent sensitivity to radiation damage. Decrease in the carrier life time and increase in charge trapping resulting from radiation effects, translate to degradation of the charge transfer efficiency. Even a small decrease of efficiency in as single cell can lead to several percent of losses after passing through a long chain of pixels [44].

2.3.3 DEPFET

Another approach to pixel sensors is based on a DEpleted P-channel FET or DEPFET device [45, 46]. A JFET transistor is implanted in the detector high-resistivity substrate and an additional buried n-type implant under the transistor is created. The implant acts as a second gate of the transistor and is referred to as the *internal gate*. In the fully depleted bulk, the internal gate forms the potential minimum for electrons that is located underneath the transistor channel. Electrons generated by an impinging ionizing particle are collected and stored on the internal gate. The resulting change of the potential on the internal gate modulates the current in the transistor channel and the signal can be measured. The readout is non-destructive and, after each readout cycle, the charge on the internal gate has to be removed by proper biasing of the clearing electrode that is present in the structure (*clear* electrode in Figure 2.10).

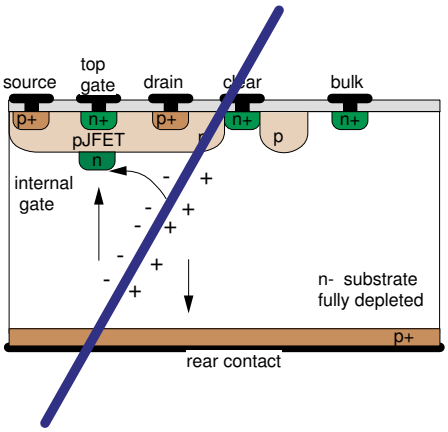


Figure 2.10: A cross section view of a DEPFET pixel. The internal gate under the JFET transistor provides the potential minimum for electrons deposited in the active volume by an impinging ionizing particle. Charge collected on the internal gate modulates the transistor current allowing the signal to be read out.

The DEPFET device provides low noise performance at room temperature, large signals originating in the fully depleted bulk, and low power consumption [47]. DEPFET devices are readout using specialized external VLSI circuits that increase the complexity of the system design. A large size detector with a fast readout and low noise performance still needs to be demonstrated before DEPFET becomes a viable vertex detector technology.

2.4 Monolithic pixel sensors

Monolithic sensors take their name from the architecture where the readout electronics is fully integrated with the detector in a single piece of silicon. Each pixel in such a sensor contains a charge collecting electrode accompanied by electronics needed for reading out the signal. This is a very attractive structure for general imaging and tracking applications, as it simplifies the system structure and enables System-on-Chip architecture.

First monolithic pixel detectors were built in early '90s [48] with a non-standard CMOS process on high resistivity p-type bulk. The design was based on a pin-diode, created by an n-type diffusion on the bottom side of the detector, and, on the top side, on an array of ohmic contacts to the substrate that served as collection electrodes. Detectors were operated in a particle beam and a 100% detection efficiency was measured ([49]), however, no further development followed.

Currently, two technologies can provide monolithic detector solutions: SOI and CMOS sensors. In the first case, the signal processing circuits are built in a thin silicon layer separated from the active volume by an insulating layer of $Si0_2$. In the second case, the electronics are located in wells next to the charge collecting electrodes.

2.4.1 Silicon-On-Insulator

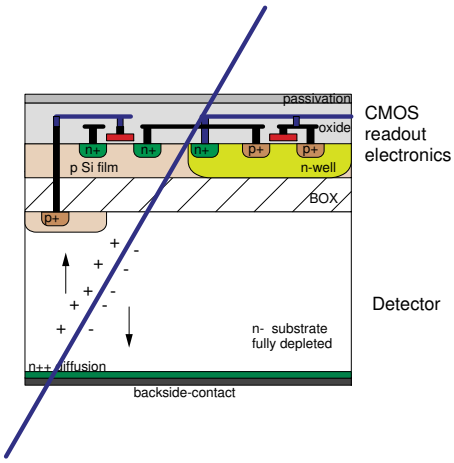


Figure 2.11: Cross section of a monolithic pixel detector in SOI technology. The device layer and the support layer are separated with a thin insulating layer of buried oxide (BOX). A high-resistivity support layer can be used as a detector volume. It is possible to bias the detector with a relatively high voltage to obtain a large depleted volume.

Silicon on Insulator (SOI) is a semiconductor wafer technology that features a thin insulating layer, such as silicon oxide, between a thin layer/film of silicon, called a device layer, and the silicon substrate, called a support layer or handle wafer. This provides smaller junction capacitance and higher drive currents, resulting in faster devices than traditional bulk CMOS techniques. In addition, the isolation of all transistors implemented in the thin silicon film provides immunity to latch-up [50].

Monolithic active pixel detectors implemented in the SOI technology utilize the silicon support/substrate layer as the radiation sensitive volume, while readout electronics are implemented

in the device layer (see Figure 2.11). This detector technology has been investigated for several years (CERN, RD19 [51]). Recent studies ([52]) and advancement in the SOI technology in the microelectronics commercial market, including wafer bonding techniques, make this detector technology very promising for the future. SOI pixel detectors allow efficient detection of ionizing radiation in a fully depleted substrate similarly to hybrid detectors but free from the complexity of the bump bonding technique. At the same time, they provide more flexibility in the design of on-chip electronics, compared to CMOS MAPS discussed in this work, by allowing NMOS and PMOS transistors in each pixel. The presence of the buried oxide layer (BOX) in SOI devices might affect the radiation hardness of this technology, which still needs to be validated in radiation harsh environments. In addition, possible coupling between the detector volume and readout electronics is a currently investigated issue.

2.4.2 Monolithic Active Pixel Sensors

Active Pixel Sensors (APS) or Monolithic Active Pixel Sensors (MAPS) are a relatively new approach to charged particle detection compared to the well-established technologies such as CCD and hybrid detectors. APS feature an amplifier integrated in each pixel[22] to buffer the signal from the photosensitive element. This is opposed to earlier Passive Pixel Sensors, where only a switch was used to connect the sensitive element to the output line for readout. APS has been the dominating architecture due to its superior performance.

Starting in the early '90s, rapid development of CMOS detectors has been driven by the visible light sensors for consumer electronics, including digital photography and video applications. These detectors are fabricated using modern CMOS VLSI technologies commonly used in the microelectronics industry. CMOS detectors, competing with CCD devices, have found applications in a variety of fields, ranging from consumer electronics to medical imaging and high-energy physics. The development of CMOS sensors for tracking applications was initiated by the IReS/LEPSI[23] research group in 1999.

MAPS approach allows for easy integration of the sensor part and the readout electronics in the same substrate. A cross section of a typical MAPS device is presented in Figure 2.12. The active volume of the sensor is a lightly doped and undepleted epitaxial layer. This layer is common in many modern CMOS processes featuring twin tubs (twin wells), where it is grown on a highly doped substrate. The fact that it is underneath the readout electronics allows MAPS having 100% fill factor that is necessary in tracking applications.

Sub-micron technologies support biasing voltages limited to a few volts. Therefore, in MAPS, the active layer cannot be fully depleted. The collection mechanism is not enhanced by a strong electric field and results mainly from thermal diffusion. The charge generated in the active volume after passage of an ionizing particle is collected by an n-well/p-substrate diode that presents the minimum-potential well for electrons. At the same time, the large difference in doping levels between the lightly doped p-type epi-layer and the p+ wells and p++ substrate results in potential barriers at the layer boundaries that act like mirrors and limit the diffusion of the electrons. Device simulations at the physical level showed the diffusion time, for a typical

[22]The amplifier can be as simple as a single transistor in a source follower configuration (gain lower than one).

[23]Institut de Recherches Subatomiques and Laboratoire d'Electronique et Physique de Systèmes Instrumentaux, Strasbourg, France. In 2006 these units became a part of Département Recherches Subatomiques at Institut Pluridisciplinaire Hubert Curien (IPHC), Strasbourg.

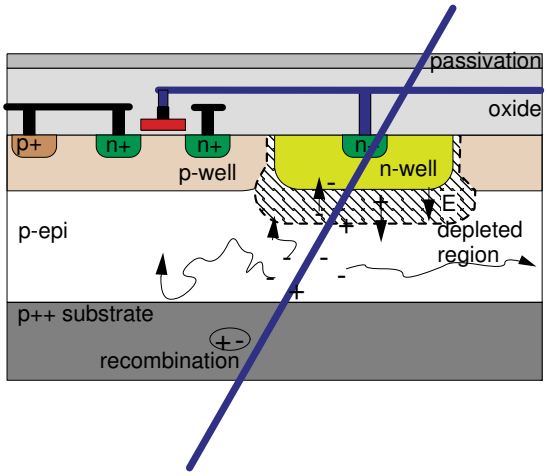


Figure 2.12: Cross section view of a MAPS pixel. The undepleted epitaxial layer, common in modern CMOS processes, forms the active volume of the detector. Charge deposited in this volume by an impinging ionizing particle diffuses thermally and is collected by an n-well/p-epi diode that presents the minimum-potential for electrons. Typically, the thickness of the epitaxial layer is limited to approximately 15 μm.

pixel pitch of 30 μm, to be less than 100 ns [13]. The majority of charge carriers generated in the highly doped, low-quality substrate will quickly recombine and only a small fraction will reach the active layer.

The current induced by electrons is integrated on the n-well/p-epi junction capacitance, resulting in a voltage signal typically of several mV per MIP. The diffusing charge is generally shared between several neighboring pixels that form clusters.

A typical MAPS device is designed as an array of pixels with the readout and processing electronics located at the periphery of a chip. A series of prototypes called MIMOSA (standing for Minimum Ionizing particle MOS Active pixel sensor) has been designed and tested by the IReS group, proving the working principle.

The measured performance parameters included excellent spatial resolution (as high as 1.5 μm) and detection efficiency, close to 100% ($> 99.8\%$). Several small-scale prototypes, with pixel arrays of several thousands cells, and one large scale device, composed of one million of pixels, fabricated in different sub-micron technologies justified the concept of this approach. The operation of sensors fabricated with epitaxial and high-resistivity substrates has been proven. The basic pixel structure, based on a 3-transistor (3T) cell, allows for a small pitch (< 20 μm) and high granularity of the sensor. Optimization of noise performance can lead to ENC as low as 10 e^- at room temperatures.

MAPS devices accomplish low power operation through a sequential access to pixels, which reduces the activity of the array to the currently readout pixel or groups of pixels. In addition, the device can be thinned, in a commercially available post-processing, to a few tens of μm, aiming at reduction of the multiple scattering in the tracking detector layer. Thinning of MAPS to 50 μm has already been tested with satisfactory results (see Chapter 3.4).

Another very important issue for MAPS as possible vertex detectors is their resistivity to radiation damages. MAPS approach takes the advantage of the intrinsic radiation hardness of

modern deep sub-micron technologies against ionizing radiation, since very thin layers of gate oxide protect from the buildup of trapped charge. At the same time, due to the lack of a strong electric field enhancing charge collection, MAPS can be sensitive to bulk damages induced by massive or very high energy particles.

MAPS suffer from a few apparent shortcomings. The first one is the fact that the circuitry in the pixel is limited to NMOS transistors. In a twin-tub process, a PMOS transistor has to be placed in a n-well that is positively biased. Any additional n-well in a pixel cell would collect signal electrons, limiting the charge collection on the sensitive electrode. Triple well processes, that provide nested wells, are investigated as a possible solution to this problem. Two options are possible. The deep n-well, available in some commercial CMOS processes for better isolation of NMOS transistors from the substrate, can be used as a large charge collecting electrode. The PMOS devices can be located in n-wells at the border of the pixel layout with relatively modest impact on the circuit behavior, especially the fill-factor [53]. Processes with deep p-wells can be considered even more interesting as they allow for placement of PMOS transistors in a pixel area without compromising the charge collection efficiency. First prototypes have been recently designed in a novel image-sensor technology [54]. Another novel approach to MAPS design uses an electric field of desirable shape that is created inside the active volume of the pixel. The electric field introduces the drift component in the movement of the signal electrons towards charge collecting electrodes. The electric field, resulting form the hole current within an individual pixel, contributes to the transport mechanism and reduces the charge collection time and charge sharing between adjacent pixels. It also allows both types of MOS transistors to be used in a pixel [29].

The second limitation originates from the same feature that gives MAPS so much strength, i.e., the use of commercial CMOS processes. Although the processes are easily available through multi-project[24] and engineering runs that allow cost-effective and relatively fast design-to-verification cycle in detector design, they evolve according to mass market requirements that very often are contrary to physicist's needs. This includes the general tendency to limit the thickness of the epitaxial layer up to its total elimination and transition to bulk processes. This is, however, a limited problem, because there are processes, developed for CMOS cameras, that feature thick 14-20 μm epitaxial layers. It has been already shown that charge collection from a high-resistivity ($\sim$ 10 Ωcm) bulk can be accomplished. The time that the process is available on the market is never guaranteed and makes fixing detector technology impossible on a longer time scale. Additionally, foundries tend not to reveal all the process parameters, including thickness of the epitaxial layer and doping profiles. This hinders detailed studies of a detector performance, especially the charge collection process.

Basic pixel architecture of MAPS is presented in a simplified schematic in the inset of Figure 2.13. The classical three transistor cell constitutes of the transistor M1 that resets the diode to reverse bias, transistor M3 that is a row selection switch, and transistor M2 that operates as a source follower. The current source for the source follower and the column selection switch are located outside the pixel. The sensor is a charge integrating device with the integration time

[24]Many small area IC designs from different institutions are processed on the same wafer effectively reducing a single user costs. The limitations come from a minimum and maximum area available for a single project and the number of fabricated devices. On the contrary, in the engineering run, a requested number of wafers are dedicated to a single project. Examples of companies that support multi-project submission include Circuits Multi-Projets (CMP), based in Grenoble, France, and MOSIS in California, USA.

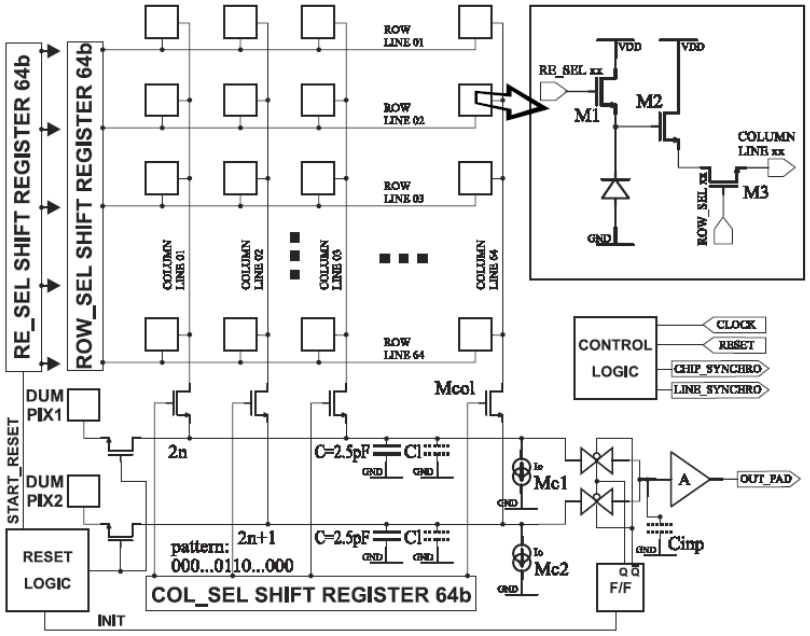


Figure 2.13: A simplified diagram of the readout scheme in MAPS prototypes. The column and row addressing shift registers sequentially select pixels for readout. The schematic of the simplest pixel cell, consisting of three transistors (3T) and the charge collecting diode, is shown in the inset.

separating two consecutive reset operations.

The readout of the pixel array is achieved with addressing logic. Any pixel in the array can be accessed and connected to the readout chain by selecting the corresponding row and column. An example of a simple detector architecture is schematically presented in Figure 2.13.

High granularity and good S/N of MAPS devices provide a very good spatial resolution and high detection efficiency. When these features are combined with a limited power consumption and the possibility of fabricating thin devices, MAPS appear as a very attractive solution for vertex detectors, with an exception of extremely harsh radiation environments.

Currently, CMOS detectors for tracking in high-energy physics experiments are investigated world-wide. The main developments are focused on upgrades of existing detectors (STAR at RHIC, BELLE at KEKb) as well as future projects (International Linear Collider, ILC, Compressed Baryonic Matter, CBM). The environments in the vertex detectors become harsher as the goal luminosities climb to very large numbers (e.g. at BELLE it amounts to $10^{34} cm^{-2} s^{-1}$). The use of strongly radiation tolerant and very fast-operated devices is thus unavoidable. Different sensor structures are proposed to deal with short integration times, such as fast multi-sample sensors (at RAL [55], Hawaii Univ. [56], and IReS) or on-chip data sparsification (at IReS, Dapnia, [see Chapter 3]). An example of a pixel structure that allows for on-chip subtraction of two signal samples, the first step in the on-chip data sparsification, is presented in Figure 2.14. The complexity of the pixel architecture is significantly increased with respect to the basic pixel presented in Figure 2.13.

Due to all the aforementioned advantages of the MAPS devices, CMOS detectors have been chosen as the technology most appropriate to meet all the requirements of the STAR experiment environment. Dedicated simulations show that a large boost of physics capabilities is expected

after installation of the PIXEL detector composed of CMOS sensors [6].

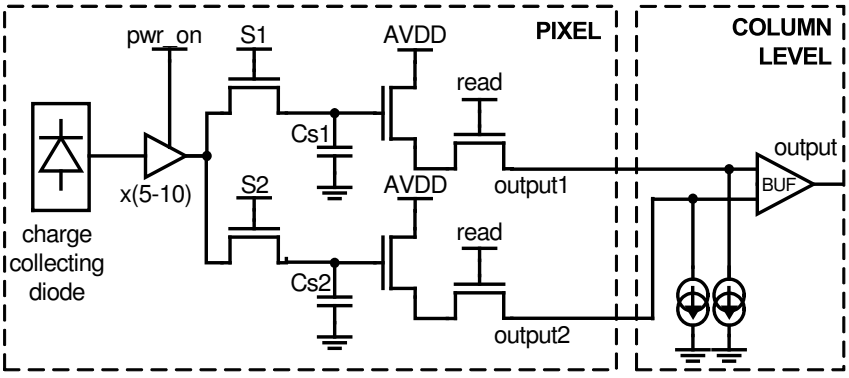


Figure 2.14: MAPS pixel structure that includes an amplifier and a sampling circuit with two analog memories. The subtraction of two voltage samples can be performed outside of the pixel, at the column level.

Chapter 3

MAPS development

The concept of MAPS detectors that has been introduced in the previous sections has been significantly developed over the past few years. The framework for this thesis was set by the state-of-the-art MAPS development performed by the CMOS research group at IPHC. The following sections describe the MAPS development status and testing environment that are fundamental for this work and the development geared towards the PIXEL vertex detector for STAR.

3.1 A short history of MAPS

In 1999, the IReS-LEPSI group proposed, based on developments of CMOS pixel sensors for visible light applications, the idea of using MAPS devices for high-energy charged particle tracking [57, 58]. The ability of the monolithic CMOS sensors to provide charged particle tracking has been since demonstrated in a series of MIMOSA (Minimum Ionizing particle MOS Active pixel sensor) prototypes. Since that time, technological processes from different silicon foundries were tested and their impact on the sensor properties was studied.

MAPS developments follow the evolution of CMOS processes and a transition from one process to another is sometimes a choice and sometimes a necessity when processes are withdrawn from the market. As modern CMOS processes evolved in the past several years, also MAPS sensors with different feature sizes and different substrate types were tested. A detailed analysis of charge collection efficiency and radiation tolerance inherent to each technology was conducted to choose the most suitable process for MAPS fabrication [14]. It has been proven that both epitaxial and high resistivity substrates may be used for device fabrication [59]. The reduction of device dimensions in modern CMOS processes is accompanied by the tendency to minimize the thickness of the epitaxial layer in order to prevent latch-up effects. The exception from this rule are processes optimized for CMOS sensors for visible light applications (e.g., AMS OPTO), where thicker epitaxial layers are used to improve light sensitivity. This shows that the production of CMOS processes with relatively thick epitaxial layers will probably continue for the benefit of ionizing particle tracking applications.

Microelectronics needed for proper operation of the sensor matured along with the fabrication process selection. The development started with very simple three-transistor cells that had a buffered serial readout. New chips have relatively advanced microelectronic circuits that enable

Table 3.1: MAPS development history at IReS-LEPSI. The table summarizes different MAPS prototypes, their most significant features, and technologies used for their fabrication.

Chip	Year	Process (μm)	Epi.(μm)	Pitch (μm)	Metal	Pixels	Peculiar
M1	1999	AMS 0.6	14	20	3M	16k	thick epitaxy
M2	2000	MIETEC 0.35	4.2	20	5M	16k	thin epitaxy
M3	2001	IBM 0.25	2	8	3M	32k	deep sub- μm
M4	2001	AMS 0.35	no	20	3M	16k	low dop. Substrate
M5	2001	AMS 0.6	14	17	3M	1M	real scale 1M pixels
M6	2002	AMIS 0.35	4.2	28	5M	4k	fast col. // r.o. and integrated spars.
M7	2003	AMS 0.35	no	25	4M	1k	fast col. // r.o. + integ. spars. (PhotoFET)
M8	2003	TSMC 0.25	$\sim$8	25	5M	4k	fast col. // r.o. and integrated spars.
M9	2004	AMS 0.35 OPTO	$\sim$14	20/30/40	4M	7k	tests diodes/pitch/leakage current
M9 no epi	2004	AMS 0.35 OPTO	no	20/30/40	4M	7k	tests diodes/pitch/leakage current
M10 Star 1	2004	TSMC 0.25	$\sim$8	30	3M	16k	1st proto. for STAR vtx det. upgrade
M11	2005	AMS 0.35 OPTO	$\sim$14	30	3M	7k	rad.tol. struct.
M12 Mosaic 1	2005	AMS 0.35 hires	no	35	4M	0.6k	multi-memory pixels (FAPS)
M13 Mosaic 2	2005	AMS 0.35 hires	no	20	4M	1.4k	fast col. // r.o.
M14 Star 2	2005	AMS 0.35 OPTO	$\sim$14	30	4M	16k	final proto. STAR vtx det. upgrade
M15	2005	AMS 0.35 OPTO	$\sim$14	20/30	4M	7k	multi-purpose tracker-imager
M16	2006	AMS 0.35 OPTO	$\sim$14	25	4M	4k	M8 translation in AMS OPTO
M17 Mtel	2006	AMS 0.35 OPTO	$\sim$14	30	4M	65k	Eudet telescope demonstrator
M18 Mimager.1	2006	AMS 0.35 OPTO	$\sim$14	$\sim$10	4M	262k	imager, high resolution
M19 Mimager.2	2006	AMS 0.35 OPTO	$\sim$14	$\sim$12	4M	80k	imager, charge spreading suppression
M20 Star 3	2006	AMS 0.35 OPTO	$\sim$14	30	4M	204k	STAR vtx det. upgrade
M21	2006	ST BiCMOS 0.25	no	20/10	4M	30k	deep p++ implants for pixel separation
SUC 1	2003	AMIS 0.35	4.2	25-35	5M	4k	rad.tol. struct. (SUCIMA project)
SUC 2	2003	AMS 0.35	no	40	3M	4k	low dop. Substrate (SUCIMA project)
SUC 3	2003	AMIS 0.35	4.2	20	5M	8k	rad.tol. struct. (SUCIMA project)
SUC 4 Mtera	2004	AMS 0.35	14	150	3M	12.5k	hadrontherapy/beam monitor. (SUCIMA)
SUC 5	2004	AMIS 0.35	4.2	30	5M	65k	proto. Dosimetry (SUCIMA project)

(http://wwwires.in2p3.fr/ires/web2/article.php3?id_article=115)

on-chip signal processing such as CDS or analog signal discrimination.

A summary of the first chips designed and tested by the IReS-LEPSI group is presented in Table 3.1 where different design and technology aspects are summarized. Tests of different technologies and their properties for charged particle tracking were the main driving force in the first two years. Different approaches to the charge collection optimization were tested, including pixels with multiple charge collecting diodes (up to four diodes per pixel). The study has lead to the conclusion that better charge collection obtained with multiple diodes is not able to compensate for disadvantages of the increased input node capacitance [60]. Currently, the commonly applied solution is based on a single charge collecting diode in each pixel. The continuous reverse bias, also called self-biased structure (SB), was introduced as an alternative to the classical reset diode [61]. The new approach, presented in details in section 3.3, simplified the pixel architecture and eliminated pedestals inherent to pixel operation.

Different diode sizes were tested along with the preferable squared layout minimizing diode capacitance through the reduction of the periphery capacitance. Diode sizes were tested from very small, 1 μm$\times$1 μm, up to 6 μm$\times$6 μm. For a typical pixel size of 30 μm$\times$30 μm, the optimum diode size was found to be approximately 15 μm^2. Table 3.2 summarizes noise performance of different prototypes. It is necessary to underline the fact that for efficient detection ($> 99.8\%$), the equivalent noise charge (ENC) should be limited to less than 20 electrons. As a consequence, the prototypes with very high noise in the laboratory tests did not undergo tests with MIPs. Currently, most of the design effort focuses on the chip architecture and fast column-parallel readout.

Table 3.2: Summary of the performance of selected MAPS prototypes in terms of noise and MIP detection efficiency. The error on the measured noise performance is typically on the order of 5-10%.

Chip	Diode size (μm)	ENC(e^-)	Detection Efficiency (%)
M1	3.1×3.1	12 (1-diode) 25 (4-diode)	99.5 ± 0.2 99.2 ± 0.2
M2	1.7×1.7	9 (1-diode) 13 (4-diode	98.5 ± 0.2 96.0 ± 0.2
M3	1.0×1.0	8 (1-diode)	not tested with MIPs
M4	$2.0 \times 2.0,\ 4.3 \times 4.3$	9 (SB diode) 5(PhotoFET)	99.7 ± 0.2 NA
M5	$3.1 \times 3.1,\ 5.0 \times 5.0$	21 (small diode)	99.3 ± 0.2
M6	$4.0 \times 3.7,\ 5.0 \times 4.7$	20 (after CDS)	not tested with MIPs
M7	4.0×3.7	50 (after CDS)	not tested with MIPs
M8	$4.1 \times 2.5,\ 1.2 \times 1.2,\ 1.7 \times 1.7,\ 2.4 \times 2.4$	16, 13, 15, 18	up to 99
M9	$3.4 \times 4.3,\ 5.0 \times 5.0,\ 6.0 \times 6.0$	10, 11, 14	> 99.9

The optimization of the radiation tolerance of MAPS has been important from the beginning. Many different diode layouts were tested to optimize the dark current and to minimize its increase due to radiation. This has lead to significant improvements over the past years [62].

In present days, the main driving force in MAPS development comes from the physics domain. The requirements in the possible future applications in particle physics are very stringent. The process of MAPS development is continuous and may last as long as new CMOS technologies are introduced to the market.

One of the milestones in the development of MAPS was a large scale device. The prototype, named MIMOSA V, featured the sensitive region divided into one million of pixels [63]. It proved the feasibility of scaling a small prototype to the reticule-size sensor.

The observed excellent tracking performance makes CMOS MAPS an interesting candidate for vertex detectors of future particle physics experiments and for various ionizing radiation imaging applications. The possibility of using MAPS in low energy electron imaging (typically with energies of a few keV) has recently been demonstrated with a thinned, back side illuminated sensor MIMOSA V. This opens the door to applications in medicine (e.g. beam monitoring for hadron-therapy [64]), biology (beta marking with tritium) and material science (electron microscopy) [65, 66].

The scientific community behind the future HEP experiments, together with the existing ones that need to be upgraded, is interested in the use of MAPS to provide wide range of physics capabilities. STAR is one of the experiments that need to be upgraded in the near-term future to extend its physics capabilities beyond what is currently achievable. The construction of the PIXEL detector focused on CMOS sensors because of their advantages over other available pixel detector technologies. Hybrid pixel sensors were rejected as being too thick and not sufficiently granular. CCDs would not provide sufficient radiation resistance and would require liquid cooling system that would boost the material budget. At the time of selecting the optimal technology for STAR, DEPFET was not sufficiently advanced to promise a realistic, large, and thin device and monolithic SOI detectors were not available.

The most challenging design aspect for MAPS operated in the STAR environment is the relatively high operating temperature. The construction of the existing detector and constraints on the material budget in the experiment prohibit the use of an active cooling system. Therefore, the vertex detector will operate at ambient temperature with a forced air flow that will introduce

very limited mechanical distortions. The performance of the first MAPS prototypes was strongly dependent on the leakage current in the charge collecting diodes. The challenges for MAPS design dedicated to the STAR upgrade were focused on minimization of the power dissipation and sensitivity to the leakage current increase due to the operating temperature and to radiation damage. In the past few years, two of the developed prototypes were strictly dedicated to the STAR upgrade. These devices will be described in more details in Chapter 6.

The work performed within this thesis derives from the results obtained in the early years of development. In particular, it contributes to the pixel optimization issues in MAPS. This is becoming of crucial importance as MAPS mature and practical sensors need to be tailored to their applications. Results from extensive tests of different pixel architectures provide guidance for the future development.

Various tests performed within the scope of this work on prototypes dedicated to the STAR vertex detector range from laboratory calibrations to operation inside the STAR detector. Measured performance is discussed with respect to the upgrade requirements. Part of this work extends into a vertex detector system and covers selected issues related to building and operating of the detector system. As part of the work presented in this thesis, a prototype of the PIXEL detector readout system was built and integrated into the STAR framework.

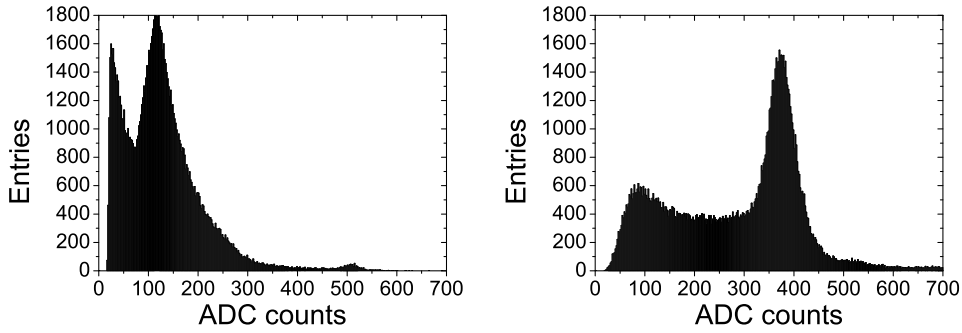
3.2 Test environment for MAPS

3.2.1 Calibration procedure

Calibration is one of the most basic procedures for MAPS characterization. The aim of the calibration is to estimate the charge-to-voltage or charge-to-current conversion factors and, consequently, the noise performance in terms of ENC of the device under test. The measurement requires injecting a signal with a precisely known magnitude into the charge collecting region. Putting any test connections inside a pixel will strongly modify the behavior of a cell, especially by changing the input capacitance of the charge sensing node. Tests with a laser source with precisely controlled power will allow for only relative calibrations. These tests can provide a measurement of the dynamic range of the device but will not extract the absolute gain/conversion factor.

An absolute calibration is performed using spectroscopy with 5.9 keV X-rays from an ^{55}Fe source. The charge liberated in silicon by a 5.9 keV photon amounts to about 1640 e^- (3.6 eV per electron-hole pair generation). The magnitude of the charge generated after photon conversion is comparable with the amount of charge expected from a minimum ionizing particle, assuming the epitaxial layer thickness to be approximately 15 μm. In most cases, the charge is naturally spread among several pixels due to thermal diffusion. However, the assumption of fully efficient charge collection is justified for a small sample of photons converted inside the depleted volume of the n-well/p-epi junction. The distribution of all extracted signals should exhibit a small peak corresponding to 1640 e^- collected in a single pixel. This peak in the distribution, if it is visible, is used as the absolute reference for the estimation of the pixel gain [67].

An example of such a distribution of signals from single pixels is shown in Figure 3.1(a). The spectrum was obtained selecting S/N larger than five. Three peaks are visible in the spectrum. The first, partial peak is dominated by noise. The second peak, at approximately 140 ADC



(a) (b)

Figure 3.1: Spectrum of signals from an iron source ^{55}Fe registered with a MAPS prototype. Signal spectrum from seed pixels, (a), shows three peaks: a noise peak at low values, a large peak from partial charge collection, and a small peak from complete charge collection, the calibration peak, at approximately 500 ADC counts. The corresponding spectrum for signals summed in 5×5 pixel clusters, (b), shows a large signal peak at approximately 400 ADC counts.

counts, represents the charge collected by a single pixel due to thermal diffusion. The third peak, located at about 510 ADC counts, is due to the complete collection of the 1640 e^- generated by 5.9 keV X-ray photons. In this particular case, one ADC unit corresponds to 0.5 mV. The charge-to-voltage conversion gain can easily be calculated from $CVF = \frac{peak \times 0.5\ mV}{(G_{analog} \times 1640\ e^-)}$ and ENC is derived from $ENC = \frac{noise[ADC] \times 1640\ e^-}{peak[ADC]}$. Figure 3.1(b) shows the distribution of signals collected in 5×5 pixel clusters. In this example, the ratio of the location of the large peak to the calibration peak indicates that the overall charge collection efficiency is at the level of 80%.

3.2.2 Analysis software

To quantify the performance of a sensor during the calibration tests, dedicated data treatment is required. All analysis results presented in this work are based on the analysis program developed at IPHC in the LabView environment[1] prior to the presented work. This section discusses the algorithms used and the efficiency and accuracy of the presented approach.

The analysis software was initially developed to test the MIMOSA V prototype, which is a large size device, and storing of all data transferred from the chip to a hard disk was highly inefficient (4 MB for one complete frame). The implemented functionality provided basic on-line data analysis and the possibility of storing only selected results. The software was optimized to operate with the USB2 acquisition card developed for MAPS within the SUCIMA collaboration [69]. The readout system was controlled by software implemented in the LabView environment and it was natural to integrate analysis software in the same environment. This analysis software proved to be very useful and reliable. The analysis was adopted for processing data from other prototypes that featured different size pixel arrays and different readout types, including serial and parallel readout).

[1]LabView is a graphical programming environment dedicated to development of test, measurement, and control applications [68]

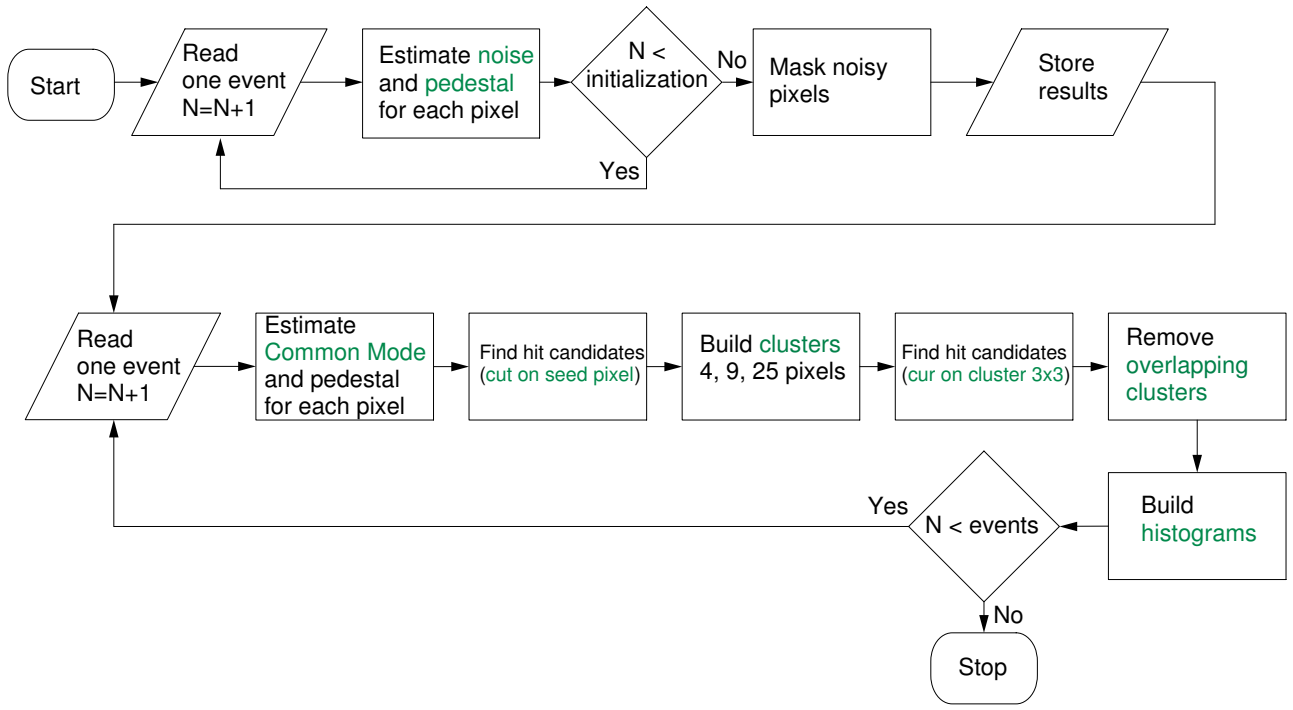


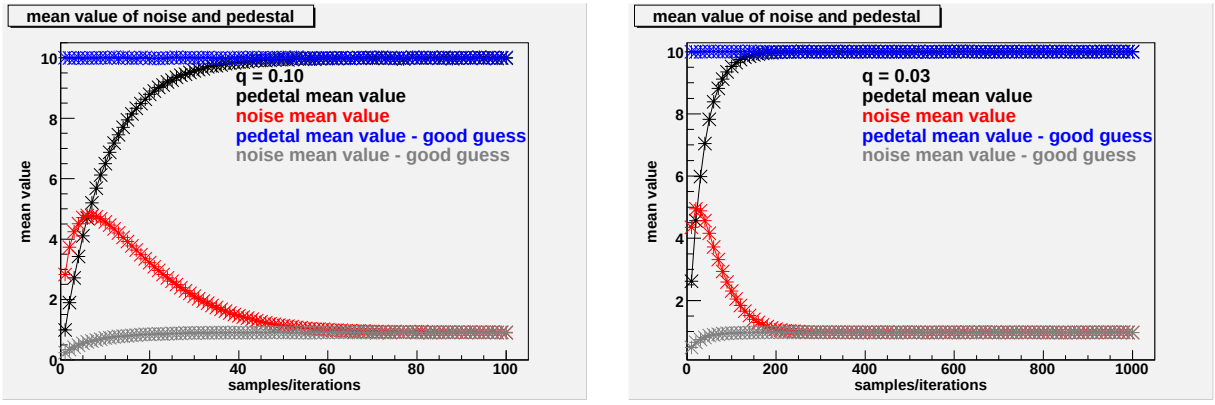
Figure 3.2: Flow chart of the data analysis algorithm used in this work for MAPS characterization. Pedestal and noise values are calculated for each pixel independently before the signal registered in the pixel array can be analyzed. Hit candidates are selected when registered signals pass thresholds set on the signal level or the signal-to-noise ratio for a seed pixel and a 3×3 pixel cluster. In the case of significantly overlapping clusters, the cluster with the largest signal/signal-to-noise ratio in the seed pixel is accepted and the others are eliminated.

The analysis algorithm used throughout this work is described in a flow chart in Figure 3.2. This analysis algorithm was adopted for on-line data treatment and all operations are performed in loops, processing one frame at a time. The algorithm can be divided into two main parts:

1. pedestal and noise estimation,
2. hit-search procedure.

The first part allows initial calculations to be performed for data collected without exposing the chip to an ^{55}Fe source. This allows for precise estimations of noise and pedestals that are not biased by large signals generated by photons. The analysis estimates noise and pedestals for each pixel as well as their distribution for the whole analyzed array.

The second part of the procedure corrects data for common mode and searches for photon generated signals. Pixels are classified as hit candidates if they pass a selected threshold on the amplitude of the collected signal or on a signal-to-noise ratio. Next, clusters of pixels are selected around these pixels that are hit candidates. The central pixel of a cluster is typically referred to as seed pixel. Seed pixel is expected to have collected most of the charge in a cluster. If two or more neighboring pixels collected enough charge to pass the threshold criteria, clusters built around these pixels have a significant overlap. It is necessary to correctly select the true cluster (with most of the charge) and to discard the false ones. Details of the implementation of this general process flow are described next.



(a) (b)

Figure 3.3: Mean value of noise and pedestal for the weighted average as a function of the number of samples for the weighting factors $q = 0.10$, (a), and $q = 0.03$, (b).

Pedestal and noise estimations

In a classical approach, pedestal is calculated as a mean signal value from a specified number of entries and noise is defined as standard deviation:

$$\overline{x} = \frac{1}{N}\sum_{i=1}^{N} x_i = \frac{x_1 + x_2 + \ldots + x_N}{N} \tag{3.1}$$

$$\sigma = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(x_i - \overline{x})^2} \tag{3.2}$$

Performing these calculations requires the knowledge of N samples. For the purpose of MAPS analysis, with the particular focus on fast, on-line processing, an alternative approach was chosen. An adaptative algorithm that suppressed the need for a deep memory buffer and sped up calculations was implemented. This algorithm, based on weighted sums, calculates pedestal and noise values for each pixel from the current data sample, D_n, according to:

$$P_n = p \times P_{n-1} + q \times D_n \tag{3.3}$$

$$N_n = \sqrt{p \times N_{n-1}^2 + q \times (D_n - P_n)^2} \tag{3.4}$$

where P_n, N_n, and P_{n-1}, N_{n-1} represent pedestal and noise values in the current (n) and previous (n-1) frame, respectively, $p = \frac{W-1}{W}$, $q = \frac{1}{W}$, and W is an arbitrarily chosen weighting constant.

The plots in Figure 3.3 illustrate the speed of convergence of the algorithm, depending on the initial settings and the q factor. The input data was chosen to have a Gaussian distribution with a mean value of 10 and standard deviation of 1. Black and red curves show convergence speed when the initial guesses for pedestal and noise values are equal zero. Plots in blue and gray are for the initial noise value equal 0 and the initial pedestal value equal 10. As expected,

the number of steps that are required for the convergence of the algorithm is larger when the initial guess is farther from the real value.

The accuracy of the adaptative algorithm can be compared with the classical mean and standard deviation calculations. In case of the standard average, the error on the pedestal estimation due to noise fluctuations of the signal sample D_n is given by $\varepsilon^2 = \frac{\sigma^2_{Noise}}{N}$. For a large number of samples (N), the estimation does not depend on the value of the standard deviation. For the weighted average, the error can be calculated as follows:

$$P_N = p^N P_0 + q \sum_{n=1}^{N} p^{n-1} D_{N-n} \tag{3.5}$$

$$\varepsilon^2 = \sum_{n=1}^{N} \left(\frac{\partial P_N}{\partial D_{N-n}} \, \sigma_{Noise} \right)^2 = q^2 \sum_{n=1}^{N} p^{2(n-1)} \sigma^2_{Noise} \tag{3.6}$$

The sum of geometric series is given by relationship 3.7. For $p < 1$, it has a limit at infinity given by Equation 3.8

$$S_k = \sum_{k=1}^{K} p^k = \frac{1 - p^K}{1 - p} \tag{3.7}$$

$$\lim_{K \to \infty} S_k = \frac{1}{1 - p} \tag{3.8}$$

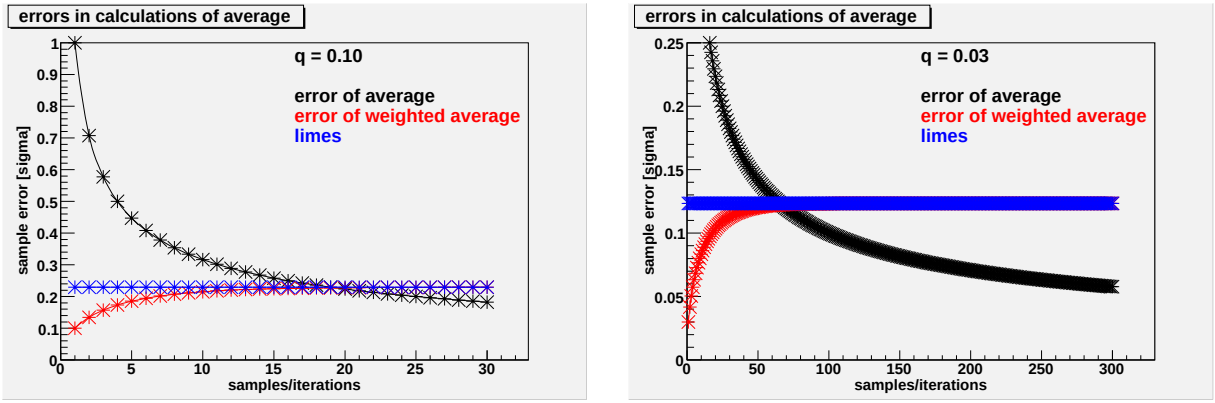
The error on the estimate can be rewritten according to:

$$\varepsilon^2 = \frac{q^2}{p^2} \times p^2 \times \frac{1 - p^{2N}}{1 - p^2} \sigma^2_{Noise} \tag{3.9}$$

which for $N \to \infty$ gives

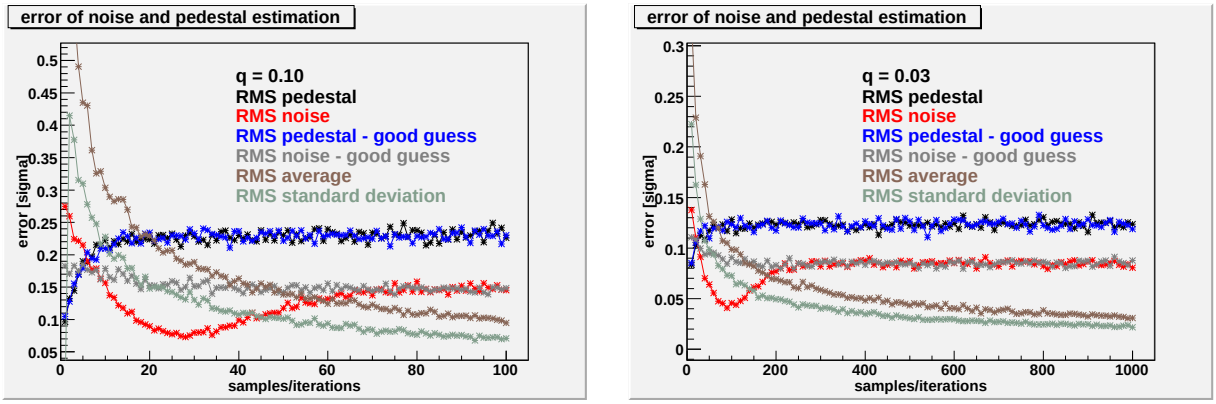
$$\varepsilon^2 = \frac{q^2}{1 - p^2} \sigma^2_{Noise} = \frac{q}{1 + p} \sigma^2_{Noise} \tag{3.10}$$

The above analysis shows that the accuracy of the adaptative algorithm is characterized by a constant error proportional to the noise variation, even for a large number of iterations. However, the error value is small and, to a first approximation, can be neglected. The plots in Figure 3.4 illustrate how the number of samples used for calculations affects the error on the pedestal estimation. Errors for the average and for the weighted average are compared for different q values of 0.1 and 0.03. The limit of the error for the weighted average is also plotted in Figure 3.4. The classical mean calculation can be applied to large data sets without requiring knowledge of all samples by implementing a sliding window that calculates the mean value on a subset of data. Depending on the size of the window the approach can give larger or smaller errors than the adaptative algorithm. The crossing of the error asymptote and the error curve in Figure 3.4 indicates the window size that provides the same accuracy as the adaptative algorithm (for the given q). For a large number of samples and $q = 0.03$, the error on the pedestal estimate is about 0.12 of the standard deviation and the same accuracy can be achieved with a sliding window algorithm using the window size of approximately 60. Most of the data analysis presented later in this work used the q value of 0.03.



(a) (b)

Figure 3.4: Comparison of errors in calculation of average using the classical mean and the weighted average algorithm. Errors are presented as functions of the number of samples and for the weighting factors $q = 0.10$, (a), and $q = 0.03$, (b).



(a) (b)

Figure 3.5: Comparison of errors in calculation of errors for noise and pedestals values using the mean and the weighted average algorithm. Errors are presented as functions of the number of samples and with the weighting factors $q = 0.10$, (a), and $q = 0.03$, (b).

The main advantage of this adaptative algorithm is that it operates on the current sample and the previously calculated value and does not require any additional memory for storing other samples. In addition, the algorithm can follow pedestal changes more closely as the most recent sample is assigned the largest weight. It might be important in the case of a significant change of pedestals during data analysis. However, under stable operating conditions, the pedestal value should stay constant during the whole measurement and no adjustment on its estimate should be necessary.

When the accuracy of the pedestal estimation is known, the question of the accuracy on noise estimate arises. The standard error of the standard deviation is expressed by $\varepsilon_{std} = \frac{\sigma_{Noise}}{\sqrt{2N}}$ [70]. A series of simulations were performed to compare this error with the error of the adaptative algorithm. Data samples with the specified Gaussian distribution were generated and the noise was derived from the number of samples used. This operation was repeated 500 times to extract the rms value of the distribution. The comparison between the rms of the standard deviation and the noise calculated with the adaptative algorithm is presented in Figure 3.5. In the case of the adaptative algorithm and large number of samples, all errors converge to constant values. In the case of sufficiently small q, the error is small enough to be neglected. These results prove that the presented adaptative algorithm is sufficiently accurate for estimating noise and pedestal values when using $q = 0.03$.

Hit searching procedure

Charge generated by a traversing particle or a photon can spread into more than one pixel and create clusters. Typically, analyzed clusters are geometrical regions of 3×3 and 5×5 pixels. The central pixel, often referred to as seed pixel, is the one that collected more charge than its neighbors. The hit searching procedure described below identifies clusters of pixels that collected the deposited charge.

The hit selection procedure begins with an optional correction for common mode, CM. The common mode is defined here as a variation of all signals in one frame as a function of the frame number. It is calculated as an average signal from the selected number of pixels. To avoid biasing the CM value, pixels with possible hits should be discarded from the calculation or the amplitude of their signals should be limited. These pixels can be selected by comparing their signal with an arbitrary threshold. The algorithm limiting the amplitude of signals used for the estimation of the CM value is defined as:

$$CM = \begin{cases} \frac{1}{n}\sum_{i=0}^{n-1}(D_i - P_i) & if D_i - P_i \leq 3 \times N_i \times Threshold_{CM} \\ \frac{1}{n}\sum_{i=0}^{n-1}(3 \times N_i \times Threshold_{CM}) & if D_i - P_i > 3 \times N_i \times Threshold_{CM} \end{cases} \tag{3.11}$$

where $Threshold$ has an arbitrarily chosen value. To speed up the analysis, the common mode correction can be calculated on a subset of pixels, but it still applies to all pixels in the given frame. Before searching for hits, signal values for all pixels can be corrected by subtracting pedestals and the calculated CM value.

In the next step, all signals from the pixel array are sorted in descending order. The pixel with the highest signal is most probably the one that collected charge generated by a traversing particle or a photon. Pixels with signal above a certain threshold are qualified for cluster reconstruction. Typically the threshold, or cut, is defined as a signal-to-noise ratio of approximately 5. After forming 3×3-pixel clusters, a second cut is applied on the sum of signals in the cluster. It is

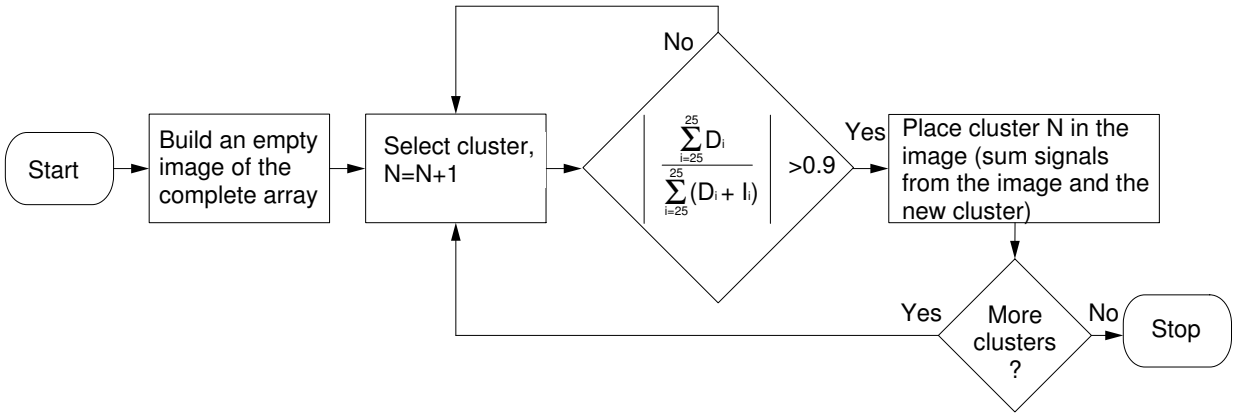


Figure 3.6: Algorithm for finding and eliminating overlapping clusters.

usually the ratio of the summed signals to the sum of noise in all 9 pixels ($\sqrt{\sum \sigma^2}$). This step is intended to eliminate seed pixels generated by high values of temporal noise.

A traversing particle can generate signals that pass the first threshold in more than one pixel, resulting in more than one seed pixel associated with such an event. Merging signals from several pixels to build one cluster is performed by the procedure that checks for overlapping clusters. The simplest approach is to compare the geometrical distance between all seed pixels chosen. The comparison starts with the highest S/N in the seed pixel as the most probable hit, and then continues with lower signals. If the distance between two pixels is smaller than an arbitrarily chosen value ($\sqrt{x_{dist}^2 + y_{dist}^2}$), the two pixels are associated with the same hit. This means that these two clusters overlap and the one with less signal in the seed pixel should be rejected, since its signal is already taken into account in the first cluster. This method requires comparing distances between all possible pairs of seed pixels, resulting in $C_N^2 = \binom{N}{2} = \frac{N \times (N-1)}{2}$ comparisons. For large matrices, where many hits can be registered in one frame, this algorithm is not time efficient.

As an alternative, a faster algorithm, presented in Figure 3.6, was used for data analysis. The clusters are arranged according to the descending S/N or S in seed pixels. The procedure begins by placing the first cluster in an empty image corresponding to the pixel array. Then, the next cluster is compared with the newly created image. The signals from the tested cluster are added to the image if the sum of signals in this cluster is larger by a defined factor than the sum of signals in the region of the existing image that corresponds to the location of the tested cluster. If the condition is not fulfilled, the cluster being tested is considered overlapping and, consequently, rejected. The advantage of this method is its speed. It requires N comparisons for N defined clusters. After the elimination of overlapping clusters, all clusters that are left are treated as separate hits.

Part of the analysis algorithm is to study charge sharing among neighboring pixels. The presented software analysis used in this work compares signals collected in seed pixels, 4-pixel, 9-pixel and 25-pixel clusters. The clusters are not selected geometrically but are built from N=$\{4, 9, 25\}$ pixels with the highest signal in the 5×5-pixel cluster. This approach reveals the number of pixels in a cluster that contain the relevant part of the signal generated by a traversing particle. For a typical sensor with a 30 μm pixel pitch, approximately 15 μm^2 diode, and the

epitaxial layer thickness of ∼15 μm, more than 90% of the charge is collected in 12 pixels for 90° incident angles.

3.2.3 Testing equipment

For testing different prototypes, a reliable and flexible system is needed. The system used for testing MAPS is typically modular and, for different chips, a part or all modules can be used. These modules are recognized as: a) a proximity board, PB, containing the tested device and the necessary control and readout electronics; b) an intermediate board, IB, with all additional power supplies, which for space limitation reasons can not be placed on the PB; c) the acquisition card that is the main part of the data acquisition system (DAQ). Each prototype requires a customized PB, but the IB and the DAQ system are designed as general purpose cards.

The modular structure of the system is compulsory for the intended tests of sensors with minimum ionizing particles. For these tests, the PB has to be small and power dissipation on the board has to be limited to avoid self-heating in a closed volume. In addition, the acquisition system is located at a remote distance from the device under tests, requiring long connection cables. Typically, the flow of analog and digital signals to the distant acquisition card is set up with shielded twisted pair, Ethernet type, cables.

An example of such a test bench is presented in Figure 3.7. This particular system uses all three of the mentioned components and was developed for testing the MIMOSA VII prototype described in Chapter 5. The clock signal, sequencing the chip operation, was generated locally on the PB to avoid sending fast digital signal over long cables. The chip played the role of a master with respect to DAQ. It generated internally, and provided outside, all digital signals necessary for the synchronization of the data acquisition process. A flag showing the validity of the analog data was generated because the rate of the analog data was much slower than the main clock and a different duty cycle was used. The flag signal was used in DAQ directly as its analog-to-digital conversion clock. The PB was directly coupled to the IB using flat ribbon cables for digital and analog signals. This latter board contained functions such as: generation of the reference voltages for the chip, LVDS conversion and buffering of digital signals for sending them to the DAQ, and loading control digital patterns from a PC computer to the chip under test.

Intermediate board

The intermediate board can be used as a power supply and reference voltage generator, and as a transceiver for digital signals, including from and to the parallel port of a PC. The connection with a PC is important for prototypes that need to be driven or programmed externally (e.g. MIMOSA VII, MIMOSA VIII, MIMOSTAR). An example of digital signals passing through an IB are the analog to digital conversion clock and frame synchronization markers, sent by the MIMOSA VII chip to DAQ. The card provides necessary buffering and conversion to the LVDS standard for digital connection to DAQ.

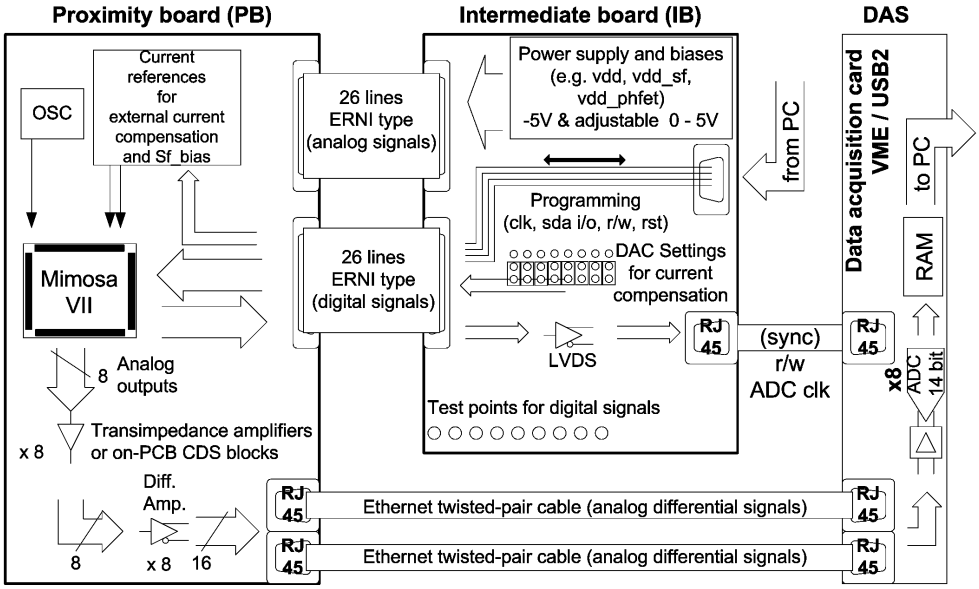


Figure 3.7: Block diagram of a typical MAPS test bench. The system is composed of three basic building blocks: a proximity board that contains a MAPS prototype, an intermediate board that provides interfaces between the proximity board and readout system, and a data readout/acquisition system.

Data acquisition system

The DAQ used in this work for sensor testing was based on the analog-to-digital conversion boards interfaced to a PC for storing data. Each board was equipped with four differential analog channels connected to fast 12-bit ADCs achieving an LSB resolution of 500 μV. The board contained banks of SRAM memory, used for temporary data storage. The on-board FPGA logic controlled the data flow from ADCs to the RAM and then to the PC for storage [71]. When a simultaneous acquisition of up to four analog channels is required, e.g. MIMOSA IX, the tests can be performed with one acquisition card. When a larger number of parallel outputs are to be registered, e.g. MIMOSA VII direct current outputs, two acquisition cards working in parallel are necessary.

3.3 Optimization of charge sensing in MAPS

Among the most important parameters for sensors used in a vertex detector are detection efficiency and spatial resolution. The STAR upgrade for 2007 requires resolution better than 10 μm and detection efficiency above 95%. The history of MAPS development at IReS shows that the analogue readout and post-acquisition data processing lead to a spatial resolution of approximately two micrometers for a pixel pitch of 30 μm.

To achieve high detection efficiency, it is necessary to distinguish real hits from accidental hits caused by excessive noise. This is accomplished by selecting signals above a certain threshold. If the threshold is set too high, some of the real events can be cut out. On the other hand, when the level is too low, signals not caused by detected particles will interfere. To deal with

this problem, a clear separation of signals from noise is required. This is where, in addition to the noise characteristics, the uniformity of the pixel array performance becomes an issue. For small and slow systems, the uniformity of pixel output levels and pixel gains is required, but is not critical. Differences between pixels can be corrected later, off-chip, by special procedures implemented in hardware (FPGA) or in software (analysis procedures), by mapping and reading from tables the offsets and gain correction factors for each pixel. This is not true for fast sensors that require on-chip data sparsification to reduce data rates. In this case, the matrix uniformity becomes a very strong concern. The large number of pixels from one matrix or sub-matrix should be treated with the same analogue readout and conditioning circuits. The uniformity of the DC output level, as well as the uniformity of the pixel gain, is necessary, especially for large arrays. Therefore, a significant design effort is dedicated to minimization and elimination of pixel-to-pixel dispersions. These issues will be addressed in the following sections.

The possibility of using MAPS for different applications (different HEP experiments, medicine and material science domains) is the driving force for continuous development. Each of the applications has its specific requirements (e.g. speed, radiation immunity), according to which the sensors should be tailored. The optimization of the performance and the architecture is essential in many design aspects. It is also true that certain solutions which are optimal for one application can be successfully implemented in other domains. For example, an efficient charge collection with low noise signal processing will be beneficial in all possible applications. The designing process of MAPS can be conceptually divided into smaller parts treated as building-blocks for the sensor. These modules provide the possibility of building a pathway for information flow in the device. It starts with the detection of an impinging particle, passes through different parts of the analogue and possible digital readout channel, and ends with the information sent to a data acquisition system. The following sections describe the charge sensing elements implemented in MAPS. The study of other upstream building blocks will be presented in Chapter 4.

3.3.1 Voltage and current operating modes

The very first approach to the sensing element in the MAPS development was a charge collecting diode with periodically restored bias level by a reset transistor connecting the diode with the reference/reset voltage [11]. The structure is schematically presented in Figure 3.8, with the time diagram showing the principle of operation. The signal generated by a particle is observed as a change of the voltage level on the floating n-well/p-substrate diode. The leakage current introduces a signal offset which depends strongly on the integration time. This offset is referred to as pedestal. It will vary from pixel to pixel due to the dispersion of process parameters. In general, all time invariant dispersions between pixel outputs are classified as fixed pattern noise (FPN). To correctly extract particle's footprint, this offset must be subtracted. This subtraction can be easily achieved in software, for example, using a table of offsets measured for all pixels. Hardware implementation becomes problematic. It would require a large memory capable of storing a reference level for each pixel of the array. Such a memory, built as analog or digital, would be complex and occupy a significant area of the chip, decreasing space available for pixels. In addition, it could significantly contribute to power consumption.

The noise performance of the three-transistor structure from Figure 3.8 is dominated by reset noise. This noise is generated whenever a voltage on the capacitance C is reset to a reference level through a resistance R. In a switched circuit, such as a pixel, this resistance is the switch

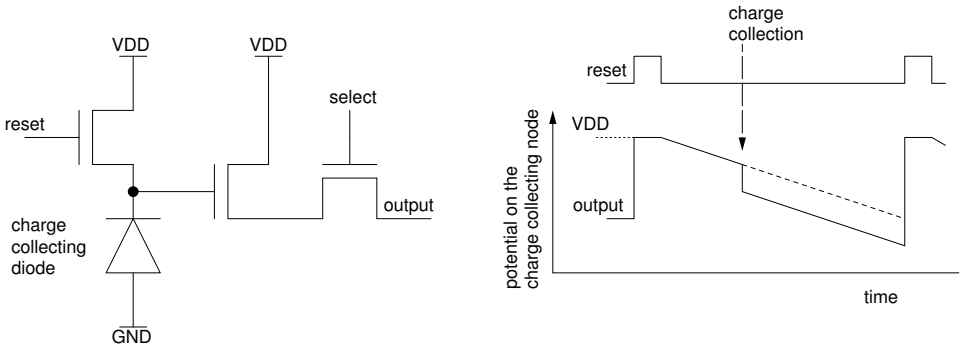


Figure 3.8: Three transistor cell, (a), and a timing diagram illustrating the signal shape after passage of an ionizing particle in between two reset operations, (b).

resistance. The thermal noise of a resistor with the power density of $4kTRdf$ is filtered by the RC network with the transfer function of

$$H(f) = \frac{1}{(1 + j\frac{f}{f_c})} \tag{3.12}$$

where $f_c = 1/(2\pi RC)$ leading to the total noise:

$$\overline{V_{out}} = \sqrt{\int_0^\infty dv_R^2 \times |H(f)|^2 df} \tag{3.13}$$

Conducting the integration and noting that $\int \frac{dx}{1+x^2} = \arctan x$ and $\int_0^\infty \frac{dx}{1+x^2} = \frac{\pi}{2}$ yields:

$$\overline{V_{out}} = \sqrt{f_c \frac{\pi}{2} \overline{dv_R^2}} \tag{3.14}$$

in which $f_c\frac{\pi}{2}$ is called the noise bandwidth. This bandwidth can be used to calculate the total white noise. This holds true for first-order filters with a finite slope of 20 dB/dec. For higher order filters, the noise bandwidth is equal to f_c. Simplifying Equation 3.14 yields:

$$\overline{V_{out}} = \sqrt{\frac{kT}{C}} \tag{3.15}$$

The voltage-to-charge relation through the capacitance C results in the equivalent noise charge generated by the reset and is equal to $ENC_{reset}^2 = kTC$. At room temperature, this is $12.7\sqrt{C(fF)}$. Typically, in MAPS with an input capacitance of several fF, the reset noise contributions are on the order of 40-50 e^-.

The above estimations hold true when the reset time is long enough for the structure to reach steady state conditions, meaning the transistor subthreshold current equals the value of the diode leakage current. However, in real systems, the steady state might not be reached. In that case, the average reset noise power is expressed by Equation 3.16, as proven in [72]

$$\overline{V_{out}} = \sqrt{\frac{1}{2}\frac{kT}{C}} \tag{3.16}$$

There is a possibility of reducing the kTC noise by using *Correlated Double Sampling* (CDS). This technique will be described in more details in section 4.1.3.

During the integration phase, the dominant source of noise is the shot noise. The voltage noise at the charge collecting diode is expressed as a function of the charge integration time, t_{int}, and the input capacitance, C_d.

$$\overline{V_{n,int}^2 t_{int}} = \frac{q i_{leak}}{C_d^2} t_{int} \tag{3.17}$$

Typically in MAPS, the leakage current is on the order of a few to several femto amperes at temperatures around 0 °C. Shot noise will not become dominant unless the leakage current increases due to radiation damages, high operating temperatures, or when the integration time becomes long. All these factors become very important in the STAR environment. Therefore, the leakage current considerations become crucial for this application.

Self-biased diode structure

For applications with a relatively low or moderate hit occupancy[2], a structure based on two diodes connected together with cathode and anode nodes was proposed by the IReS/LEPSI group. The charge collecting diode is reverse biased, while the other diode is biased in the forward direction. The very high resistance of the forward biased diode allows for treating the n-well as a floating node. When the reverse biased diode collects charge deposited by an impinging particle, the voltage on the diode drops and a slow recovery (discharge time) begins. The structure operates at a constant reverse bias and is often referred to as a self-biased diode. The structure is schematically presented in Figure 3.9, with a time diagram illustrating the principle of operation.

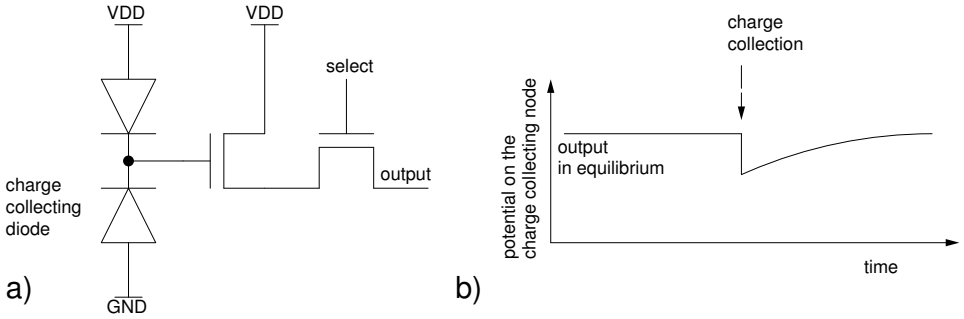


Figure 3.9: Self-biased structure, (a), and a timing diagram illustrating the signal shape after passage of an ionizing particle, (b).

The self-biased structure is effectively a logarithmic pixel [74]. The response of the system is, by default, not linear, but for small input signals, it can be approximated with a linear behavior. Device simulations show the linearity of response up to approximately 3 ke^-. Simulations have to be tuned according to the measured detector behavior, due to the limitations of available

[2]e.g., STAR 2009 - in the 4 ms integration time there would be 53 hits/cm^2 in the inner layer (2.5 cm) and about 10 hits/cm^2 in the outer layer (at 7 cm on average) [73]). This can be compared to ILC, where at the 1.5 cm radius, it is expected to have more than 3 hits/cm^2/bunch (8 from the latest calculations at IPHC). The beam structure consists of 2820 bunches in 950 μs with a 200 ms period.

device models. This dynamic range is satisfactory for most tracking applications. Typically, the most probable value, MPV, of charge collected in a single pixel after a MIP passage is at the level of 250 e^- in MAPS devices that feature a several micrometer thick active volume.

The signal collected on the charge collecting diode in the self-biased structure is proportional to the number of electrons, but the signal read out after the integration time is not linear. The discharge process is faster for larger signals and, therefore, more of the initial signal can be lost.

The self-biased structure, can be modeled as an RC circuit defined by the equivalent resistance of the forward biased diode and the capacitance of the reverse biased junction. When the structure is in equilibrium, the voltage on the n-well is approximately $V_{bias} - RI_{leak}$ and the equilibrium state can be described with

$$\frac{Q_{eq}}{C_d} + RI_{leak} = V_{bias} \tag{3.18}$$

where Q_{eq} is the amount of charge in equilibrium, R is the node resistance, C_d is the node capacitance, and I_{leak} is the diode's leakage current.

When an impinging particle delivers additional charge to the diode capacitance, this charge will have to be removed to restore the equilibrium. The discharge process can be described as the removal of the charge Q with the current I in time:

$$Q = -\int_0^\infty I(t)d(t) \tag{3.19}$$

This situation can also be presented as a complete discharge of an RC circuit:

$$\frac{Q_{eq} + Q(t)}{C_d} + R(I_{leak} + I(t)) = V_{bias} \tag{3.20}$$

Combining Equation 3.18 and 3.20 leads to:

$$\frac{Q(t)}{C_d} + R(I(t)) = \frac{Q(t)}{C_d} + R\frac{dQ(t)}{dt} = 0 \tag{3.21}$$

and the solution to this equation is:

$$Q(t) = Q_0 exp\left(-\frac{t}{\tau}\right) \tag{3.22}$$

where $\tau = RC_d$. For a 10 fF capacitance and resistance on the order of tera ohms, τ reaches approximately 10 ms.

Using this structure is beneficial when compared to the diode with a reset switch. The layout of the pixel can be simplified, as one digital signal (reset) can be suppressed. Another profit is that, in equilibrium, the voltage level does not change and there is no pedestal to be removed during signal extraction. Nevertheless, for proper signal extraction, a subtraction of two samples is required forcing the use of CDS or similar processing. The shot noise of this structure is calculated differently than for the reset diode. Two junctions are present and the noise will be the sum of the two noise sources. At present, the question of correlations between the two noise sources stays unanswered. A few prototypes proved that this structure is well performing and the total noise performance is superior compared to structures with the reset switch. Most of the prototypes described in this work exploit the self-biased structure as the sensing part. The self-biased structure is also proposed and implemented in prototypes for the STAR vertex detector upgrade.

Table 3.3: Comparison between a self-biased structure and a diode with a reset switch

Structure	Advantage	Disadvantage
diode with reset switch	single readout to extract signal	subtraction of pedestal needed reset noise
self-biased	no reset noise no pedestal simpler pixel layout	CDS to extract signal

Pixel operated in current mode

The usual approach to charged particle detection in MAPS consists in the conversion of the collected charge to voltage inside a pixel and further processing of voltage signal. Detectors with pixels generating current signals are an alternative to the voltage-mode pixels. An important advantage of operating in current mode is the large dynamic range of signals that is not restricted by power supply voltages. Two examples of pixels operated in current mode are DEPFET, implemented on high resistivity silicon substrate, and PMOSFET with floating gate and n-well tied together, built in an SOI process [75]. A new scheme for the operation in current mode, called PhotoFET, has been proposed by the IPHC group, bearing implementation in a standard CMOS process [76]. The advantages gained with the operation in current mode are high swings of the output signals regardless of limited power supply voltages and ease of implementation of basic signal treatment, requiring simple arithmetic operations, such as addition and subtraction on the pixel and chip level (e.g. [77]).

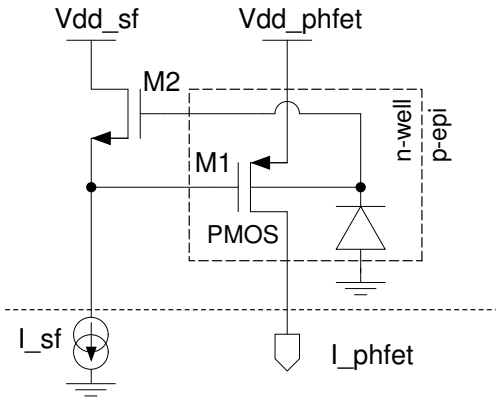


Figure 3.10: Schematic of a PhotoFET cell composed of a n-well/p-epi charge collecting diode and a PMOS transistor. Charge collected in the n-well modulates the PMOS transistor current through the bulk effect.

The principle of operation of the PhotoFET cell (shown in Figure 3.10) is, to some extent, similar to the self-biased structure. The p+/n-well junction created by the source of a PMOS transistor, which is implemented in the charge collecting n-well, biases the n-well through a high resistance. The charge generated in the n-well shifts the voltage of this node and, through the bulk effect, modulates current in the PMOS transistor. The trace of a particle is seen as a variation of the signal superimposed on the DC current of the PMOS transistor.

One of the prototypes studied within this work was based on this new principle. Results and discussion of the obtained performance and its comparison to the classical voltage operation will

be presented in Chapter 5.

3.4 Sensor thinning

To exploit the high single point resolution of MAPS, sensors need to be thinned to a few tens of micrometers to avoid deteriorating the resolution by multiple Coulomb scattering. Sensor thinning for MAPS devices was investigated at IPHC and LBL. This section focuses on aspects crucial for vertex detector development, but they were not part of this PhD work.

Decreasing substrate thickness

The first attempts to thin MAPS to several tens of micrometers were made in 2004. The thinning procedure applicable on a wafer scale was developed in collaboration with an industrial partner. Reducing the wafer thickness down to 120 μm has been accustomed for wafers with the large scale device, MIMOSA V. The quality of the process is satisfactory and no performance losses were observed on several chips tested. Few wafers were also thinned to 70 μm and trials to reach 40 μm will be attempted in the next step. The goal thickness is 50 μm.

In parallel to developments at IReS, the LBL group worked on back-thinning of pre-diced wafers with the MIMOSA V sensor to the thickness of approximately 40 μm [78]. The thinning was performed by an external company specialized in thinning for semiconductor industry. The process used for thinning utilizes a proprietary hot wax formula to attach wafers or dice to stainless steel grinding plates. Wax used as an adhesive facilitates handling of thin parts that leads also to elimination of damages caused by electrostatic discharge (ESD). The back-thinning is based on a wet grind process with a rust inhibitor for cooling the chips. This keeps the grind wheel free of debris which could damage thin chips. Backgrinding followed by polishing that minimizes the stress from backside of the device allows reaching thicknesses below 50 μm. The yield of the process depends mainly on the quality of silicon. However, for very thin specifications, the doping of the wafer and the front-side processing factors, such as oxides or polyamides, may cause stress in the silicon lattice that could result in failures. A few MIMOSA V chips were thinned to approximately 50 μm and one to approximately 39 μm. At the latter thickness, chipping of the sensor edges was observed and further thinning was aborted. The damage was observed at the very periphery of the device, outside of the guard ring area, and did not affect the electrical functionality of the chip. Tests performed with the thinned devices showed no degradation of performance as compared to the full-thickness sensors [78].

Back illuminated devices

Another thinning issue addressed during MAPS development was substrate removal. The development of sensors for medical applications required building devices capable of detecting low energy electrons (a few keV). These electrons can travel in silicon only a few to several μm. The device cannot be front illuminated as almost no particles would reach the epitaxial layer. Therefore, substrate removal and back-side exposure are necessary.

A few wafers with the MIMOSA V device were thinned to the epitaxial layer. Special care was taken to protect the thinned surface of the wafer. A passivation layer (entrance window) was created to restore the electric potential profile pushing the electrons from the interface into

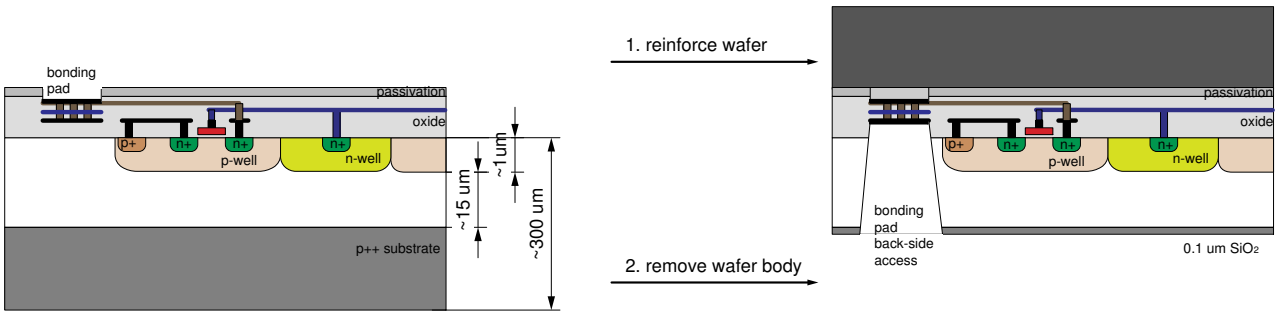


Figure 3.11: The procedure includes the following steps: adding a reinforcing wafer, removing the original wafer body, creating deep trenches to provide contacts to original pads, and passivating the back side of the new structure.

the epitaxial layer. This limits charge trapping and recombination of electrons on the interface, similarly to the reflective barrier existing in the sensor before thinning. Different entrance windows were formed (75, 110, 160 nm) [79].

The thinning process is schematically depicted in Figure 3.11. The original wafer thinned to the epitaxial layer would be exposed to significant in-material tensions leading to its destruction. Therefore, in the first step, the wafer is mechanically reinforced on the front side by adding a support wafer. Then, the p++ body is removed and the exposed silicon is passivated, resulting in thin SiO_2 entrance window. The bonding pads of the original chip are now inaccessible, being covered by the supporting wafer. To allow electrical connections to the chip, chunks of silicon beneath the original pads have to be removed. The aluminum pad plates become reachable in deep trenches, allowing bonding the detector to a printed circuit board or a VLSI package. Test results show noticeable charge losses, with respect to standard thickness devices. It was observed that the charge collection efficiency in thin devices reached 60% ([65]), while it is typically on the order of 90% for full thickness MAPS. This loss can be attributed to the removal of the epitaxial layer and electron recombination at the interface of the sensor and the epitaxial layer. The latter indicates that the potential barrier created in the passivation process is not sufficiently efficient and its improvement should be addressed in the future.

Chapter 4

MAPS with voltage mode signal processing

The previous chapter introduced a distinction between sensors converting collected charge into voltage and current signals. This chapter focuses on pixel architectures processing voltage signals and provides basis for rudimentary in-pixel signal processing that is necessary for building large sensors capable of fast readout. The study of different voltage amplifier architectures suitable for compact, NMOS transistor based, implementation inside pixel cells is presented. Design aspects and measurements with dedicated prototypes provide basis for development of sensors with in-pixel signal processing.

4.1 Pixel architectures

Building a sensor requires careful verification of its performance during the design process and in the post-fabrication tests. The process of designing integrated circuits is very strongly aided by dedicated tools. In general, these tools are known as Computer-Aided-Design (CAD). The three biggest companies on the market specialized in providing CAD tools for electronics engineering are Cadence Design Systems, Synopsys and Mentor Graphics. Development of MAPS at IPHC is based on the Cadence package for sensor design and verification. This includes SPECTRE as an analog simulator and DIVA as the layout extraction tool. The following sections will discuss the requirements for the design of a pixel operated in voltage mode with built-in signal amplification as used in MAPS.

4.1.1 In-pixel amplifier and restrictions on its design

In the most common approach to the MAPS design, the signal generated by an impinging particle in a pixel is typically on the order of several mV, assuming the capacitance of the charge collecting diode of about 10 fF and the collected charge of a few hundreds of electrons. The voltage signal generated on the charge sensing node is then readout by a source follower with a gain factor of about 0.7–0.8. This relatively small signal is affected by electronic noise determined mainly by the charge collecting diode and in-pixel electronics. In addition, such weak signals can be easily influenced by noise generated in other parts of the analog readout chain.

Thus obtaining a satisfactory signal-to-noise ratio is strongly limited by the performance of the entire readout chain. If the sensor requires any data treatment, such as storing or subtracting samples, the noise introduced by the processing circuitry can become a severe limitation to the signal-to-noise ratio. Signal amplification in the very beginning of the readout chain, i.e., in each pixel, can help to overcome this problem. If the signal is sufficiently large, the S/N ratio will be fixed at this point and the rest of the readout chain should have a negligible influence on the noise performance of the sensor. This issue is crucial for on-chip data digitization.

Obtaining high gain in a pixel cell is not an easy task. The advantage of CMOS processes, i.e., using NMOS and PMOS transistors, can not be used in MAPS at the pixel level. Design of amplifiers is effectively limited to the use of NMOS transistors only, as explained in section 2.4.2. Simple amplifier structures should allow achieving gain on the order of four to five. This small amount of gain can significantly improve the sensor performance. The readout speed requirements for the MAPS sensors are very tight and the on-chip data sparsification becomes a necessity for future applications. In-pixel amplifiers become unavoidable. Important requirements for their design include a compact layout, low noise operation and low power consumption. In the following chapters selected examples of particular solutions will be presented.

Current MAPS generally reach noise performance at the level of about 15 e^-. Implementing an on-chip ADC requires that the dynamic range of the ADC and noise of the pixel be adjusted. A classical ADC designs can reach LSB at about 1 mV. If the LSB is supposed to correspond to noise level then the gain of about 67 $\mu V/e^-$ is required between the charge sensing diode and the ADC input. Assuming the input capacitance (diode and the gate of the input transistor) at about 10 fF, the charge-voltage conversion is approximately 16 $\mu V/e^-$. This shows that additional gain of about 4.2 in the readout chain is needed. The most critical part of the readout chain is inside a pixel, therefore, this is the most preferable location for an amplifier.

In addition to the restriction on the use of PMOS transistors, an in-pixel amplifier design is also bound by limits imposed on power consumption. As an example, the expected performance for the ILC vertex detector [80] assumes that the innermost layer power dissipation is limited to less than 0.7 W/cm^2. This translates to 1 mW/column, which includes a pixel, ADC, and the readout circuitry. A reasonable division of this power between the above components leaves approximately 150 μW for the pixel cell, including its readout based on a source follower. For large chips that have large capacitance associated with each readout line, a fast readout is only possible when the minimum of 40-50 μA are drawn from the source follower. This restricts the power budget for the in-pixel amplifier, limiting the number of possible amplifier designs. Despite important limitations on the amplifier design, the advantages of having this stage in the readout chain are significant.

The first prototypes dedicated to STAR (see Chapter 6) feature a simple pixel architecture without in-pixel signal amplification. The PIXEL detector power requirement of less than 100 mW/cm^2 is relatively easy to achieve with limited power consumption in a pixel and a slow, sequential readout of the pixel array.

An additional concern related to noise is the pixel-to-pixel gain uniformity. When all pixels from one column or a section are readout through the same chain, and the signal is to be conditioned on the fly, then any nonuniformity of the in-pixel gain will manifest itself in additional system noise. Therefore, mismatches in the amplifier circuit need to be considered. A reasonable value for the maximum allowable gain dispersion of the in-pixel amplifier is less than 4%. This value can be extracted from the fact that MAPS in the beam tests showed signal-to-noise ratio

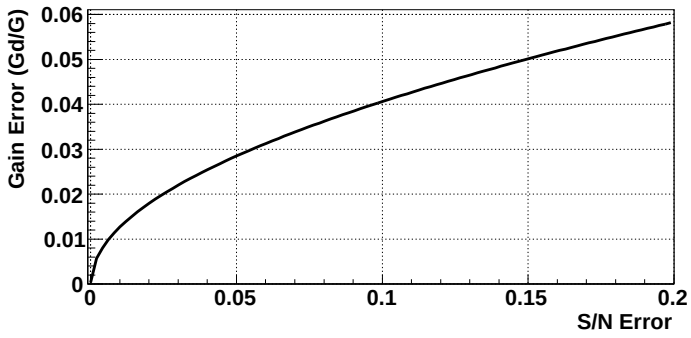


Figure 4.1: Maximum allowable gain dispersion for an in-pixel amplifier. The value is extracted from the acceptable degradation of the signal-to-noise performance. The S/N error is assumed for the typical S/N=5 that corresponds to the low energy tail for signal collected in one pixel.

of about 5 at the low tail of the signal distribution. To apply signal cuts without significantly degrading detection efficiency, the variation of the S/N in that region can be assumed at 10%, i.e., S/N variation of 0.5 at 3σ. It is reasonable to limit the allowable S/N error to $1\sigma = 0.1$ at the pixel level to accommodate for dispersions in the rest of the readout chain. This can be expressed in equations 4.1 and 4.2, where Δ is the S/N error and G_d is the gain variation superimposed on the design gain G . The gain dispersion G_d/G can be extracted from Equation 4.2 by substituting $S_{in}/N_{in} = 5$.

$$\frac{S^2}{N^2} = (5 \pm \Delta)^2 \tag{4.1}$$

$$\frac{S^2}{N^2} = \frac{S_{in}^2 \times G^2}{N_{in}^2 \times G^2 + S_{in}^2 \times G_d^2} \tag{4.2}$$

The solution of Equation 4.2 as a function of Δ is plotted in Figure 4.1. This plot shows that if the S/N=5 is allowed to vary by less than 0.1, the acceptable in-pixel gain nonuniformity is below 4%. The achieved gain uniformity of in-pixel amplifiers implemented in MAPS prototypes will be discussed in section 4.2.4.

4.1.2 Diode-Amplifier connection

A successful implementation of an in-pixel amplifier needs to comply with the restrictions on the amplifier architecture, including the exclusive use of NMOS transistors and the size and number of transistors used. An example of a simple amplifier satisfying these criteria is the common-source (CS) amplifier. Such an amplifier is presented in Figure 4.2, where M1 is the input transistor, M2 is the load of the amplifier and M3 is a switch for pulsed-power operation. The input voltage to the CS stage should be higher than the threshold voltage. For an NMOS transistor in the AMS 0.35 process, the threshold voltage is approximately 0.5 V. When the source of the input transistor is grounded, the input voltage should be at the level of 0.7-0.8 V to provide an operating point with the required gain and dynamics. If the input of the amplifier is connected directly to the charge sensing node then the bias on the charge collecting diode

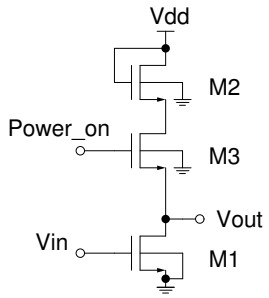
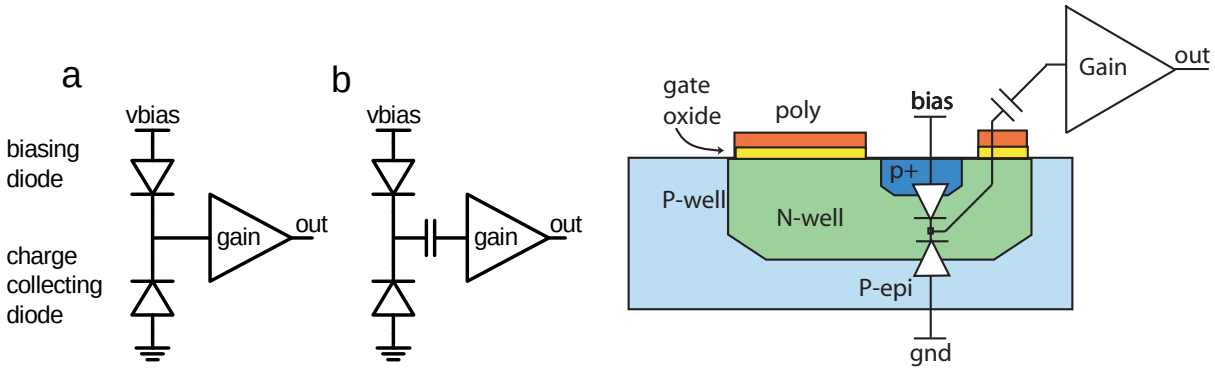


Figure 4.2: Schematic diagram of a simple in-pixel amplifier in the common-source configuration.



(a) DC and AC coupling (b) cross section

Figure 4.3: AC coupling of an in-pixel amplifier and a charge collecting diode: schematic, (a), and a cross section view through the layout-efficient implementation, (b). The coupling capacitance is implemented by creating a polysilicon layer on top of the charge collecting n-well.

has to be adjusted accordingly to provide proper biasing of the amplifier. Typically, the voltage on the charge collecting node is at the level of 3 V and needs to be lowered. Lower voltage on the charge collecting diode results in increased input capacitance and decreased depleted volume of the junction. Both effects can be considered as a detriment to the sensor performance, as the charge-to-voltage conversion ratio and the charge collection efficiency will be reduced. A possible solution to avoid this drawback is to separate the two nodes. Two basic types of in-pixel amplifiers can be distinguished based on their connection with the charge collecting node. The architecture, where the voltage of the charge sensitive node is directly connected to the input transistor, will be referred to as DC coupled (Figure 4.3(a)). The bias of the charge collecting diode determines the operating point of the amplifier. Adding a series capacitor, between the charge collecting node and the input of the amplifier, results in a DC separation of the two nodes, referred to as AC coupling. Changes of the voltage in the charge sensing node will be transferred to the amplifier through the capacitive coupling. Expected advantages of such configuration arise from the fact that the operating point of the amplifier is independent of the diode bias. The voltage bias of the latter can be increased to enlarge the depleted region of the charge collecting diode and, therefore, to improve the charge collection efficiency. The disadvantage is the necessity of adding circuitry which assures proper biasing of the amplifier. Furthermore, a

capacitive voltage divider is created by the AC coupling capacitor and the input capacitance of the amplifier. The capacitance ratio of the coupling capacitor to the input capacitance needs to be high to minimize signal attenuation.

The AC coupling seems to be a quite attractive solution, but the use of it is limited by the pixel area required for the coupling capacitor. In MAPS prototypes the compromise was found and the coupling capacitor was implemented as the gate oxide layer on top of the charge sensing n-well (Figure 4.3(b)). Other solutions, not available in all CMOS processes, such as a poly-poly or metal-metal capacitors, would require additional area and would inherently feature more parasitic capacitance. For example, in the AMS 0.35 OPTO process, the area capacitance of the gate oxide is about 4.54 fF/ μm^2 compared to 0.86 fF/ μm^2 of the poly-poly structure. Most of the in-pixel amplifiers discussed in the scope of this work are connected to the charge collecting node by AC coupling.

4.1.3 In-pixel CDS processing

Introducing signal amplification into a pixel cell is just one way of improving the sensor performance. Noise performance can also be improved by special techniques for signal processing.

One possible way to suppress the kTC noise is to perform the *Correlated Double Sampling* [81]. It is based on comparing two samples following one reset phase and, therefore, independent of the noise introduced by the reset operation. Other methods, called *active-reset* are discussed in [82, 83]. For the first MIMOSA circuits, the CDS operation was performed by software during off-line data processing. The useful signal is calculated as the difference between two consecutive samples acquired from each pixel after the reset. Reading out pixels in the sensor is continuous and the device integrates charge during the time equal to the readout time of one full frame. Assuming that each pixel is readout during one clock cycle, the integration time is equal to $\tau = \frac{N_{pix}}{f_{clk}}$, where N_{pix} is the total number of pixels connected to one serial output line and f_{clk} is the read-out clock frequency. Subtraction of two signal samples separated by the integration time can be transformed into the frequency domain using the Laplace transform. The Laplace transform of a signal delayed in time domain by τ is expressed in frequency domain by multiplication of the corresponding signal transform by $e^{-s\tau}$. Therefore, the transfer function of the CDS operation can be expressed by Equation 4.3. Using the Euler formula[1]and the double angle identity[2], Equation 4.3 can be simplified to Equation 4.4.

$$|H_{CDS}(f)|^2 = |1 - e^{-2j\pi f\tau}|^2 \tag{4.3}$$

$$|H_{CDS}(f)|^2 = |1 - (\cos(2\pi f\tau) - j\sin(2\pi f\tau))|^2 = 2(1 - \cos(2\pi f\tau)) = 4\sin^2(\pi f\tau) \tag{4.4}$$

The sinusoidal function in Equation 4.4 reveals that CDS removes low frequency signals. Using CDS is advantageous for rejecting low-frequency noise from different sources. In addition to the kTC noise, majority of the flicker noise (1/f) present in the pixel structure is removed. This allows for significant simplifications in the noise analysis of MAPS performance. Double

[1] $e^{ix} = \cos x + i\sin x$

[2] $\cos 2A = \cos^2 A - \sin^2 A = 2\cos^2 A - 1 = 1 - 2\sin^2 A$

sampling allows also for efficient removal of the fixed pattern noise. A small penalty for using the CDS operation for minimizing two types of low-frequency noise is the increase of the white noise. The subtraction of two samples results in doubling of the power density of the uncorrelated high-frequency noise.

The removal of the low-frequency noise component requires the comparison of two samples distinct in time for each pixel and is independent of the type of the charge collecting diode used in the sensor. In the case of the diode with the reset transistor, this technique eliminates the reset noise. In the case of the self-biased structure, this technique is necessary for extracting useful signals generated by impinging particles. The implementation of this technique on the chip level improves noise performance, minimizes FPN, and removes pedestals, making it the necessary first step to the on-chip data sparsification.

One possible implementation of the on-chip CDS would require the signal read out from all pixels to be stored in an analogue or digital form at the bottom of the sensing matrix for subtracting it from the next frame. For large scale devices this would require complicated analogue circuitry or a large additional area for digital memory, leading to a significant dead area in the sensor. This is not practical and other solutions need to be investigated. The most promising approach is based on memorization of two or more samples in each pixel. The subtraction can be accomplished in-situ or at the bottom of the sensor matrix. In this work the two methods are discussed and examples of implementation are given.

4.2 Pixel design

4.2.1 Gain and noise considerations

The simplest structure that allows for signal amplification in a pixel cell is based on the common-source amplifier configuration. A CS amplifier, presented in Figure 4.4, composes of a transistor M1 that is the amplifying stage and M2, in a diode configuration, operating as an active load.

The diode configuration results from the fact that the transistor is always in saturation since the $V_{DSsat} = V_{GS} - V_T$ and its $V_{GS} = V_{DS}$. Therefore, its current-voltage characteristic is quadratic (equation 4.5) for positive values of V_{DS} and there is no conduction for negative values.

$$i_{DSsat} = K' \frac{W}{L} (V_{GS} - V_T)^2 \tag{4.5}$$

Analysis of the small-signal equivalent circuit reveals that the small signal resistance of the transistor in a diode configuration is expressed by $1/g_m$, where g_m is the transconductance.

Voltage gain of the common-source amplifier can be expressed by $V_{out}/V_{in} = G = -g_m R_{load}$ where g_m is the transconductance of the input transistor and R_l is the load resistance. If the input transistor is connected to the transistor in the diode configuration than the gain is approximated with $G = -g_{m1}/g_{m2}$.To achieve high gain, the transistors should be designed in a way to maximize g_m and to minimize g_{m2} (in saturation $g_m = K' \frac{W}{L}(V_{GS} - V_T)$).

The frequency response of the circuit can be analyzed looking at the influence of each transistor capacitance separately: the gate-source capacitance C_{GS}, the drain-source capacitance C_{DS}, and the drain-gate capacitance C_{DG}. Each of them will introduce a pole at $f_{c1} = \frac{1}{2\pi R_S C_{GS}}$, $f_{c2} = \frac{1}{2\pi R_L C_{DS}}$, $f_{c3} = \frac{1}{2\pi M R_S C_{DG}}$, respectively. The R_S is the source resistance seen by C_{GS}. The

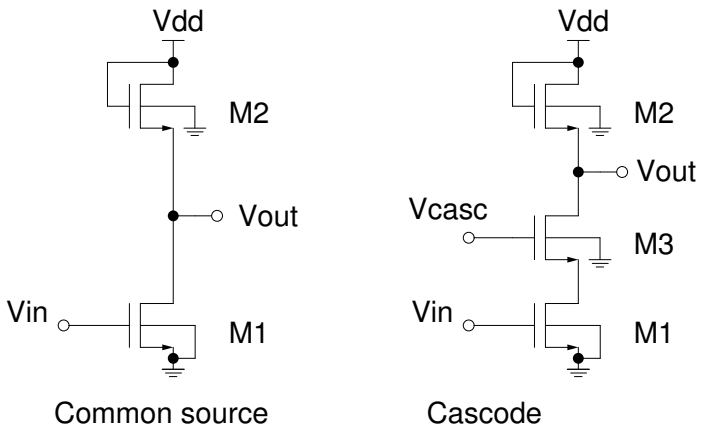


Figure 4.4: Common-source and cascode structures for simple in-pixel amplifiers.

multiplication factor M is equal to $(1 + G)$, where G is a low frequency gain of the amplifying stage. This is the Miller effect. It originates from the fact that a capacitance coupling the input and output of any amplifier can be replaced with the equivalent input capacitance of $C(1 + G)$ and the output capacitance of $C(1 + 1/G)$. It is clear that the first capacitance can have a significant effect on the circuit, while the second one can usually be neglected.

Depending on the gain in the design and the required operation speed, the Miller effect can lead to an excessive bandwidth reduction. However, for the MAPS architectures discussed in this chapter, it is not a limitation. The bandwidth is limited by the load capacitance that is in parallel with C_{DS} and leads to the -3 dB frequency at f_{c2}.

Although the Miller effect does not affect the frequency response in the discussed MAPS prototypes, it does significantly influence the input capacitance. The Miller capacitance is added in parallel to the capacitance of the charge collecting diode. Since both of them are on the order of fF, the Miller effect will result in reduction of the voltage signal fed to the amplifier.

A simple circuit, which is not affected by the Miller effect, could be a very attractive solution for an in-pixel amplifier. The Miller effect is strongly reduced in the cascode amplifier because the load of the transistor M1 is a small resistance of the M3 transistor and the Miller multiplication equals approximately $M = 1 + gm1/gm3$ that is typically close to one. The gain of the cascode amplifier is approximately the same as the gain of the common-source amplifier for the same load transistor. The bandwidth of a cascode structure will also be limited by the dominant pole set by the load capacitance.

The amplifier from the MIMOSA IX prototype can serve as an example. The gate capacitance of the input transistor is equal to about 3 fF. When the amplifier is operating the transistor is in saturation. In this state the gate-source capacitance is equal to about 2/3 of the gate capacitance or approximately 2 fF[3]. Simulations for the studied amplifier structures show that the gate-drain capacitance, the capacitance affected by the Miller effect, is on the order of 0.5 fF. Simulated gain of the amplifier is about G=5.5. Therefore, the input capacitance of the cascode amplifier will be equal to about 2.5 fF, while for the common-source amplifier, because of the Miller effect, it will total approximately 2 fF + 0.5 fF × G = 4.75 fF. To complete this discussion, the total

[3]To be precise it is the overlap capacitance C_{GS0} plus 2/3 of the oxide capacitance [24].

input capacitance needs to be estimated. Assuming the charge collecting diode capacitance of approximately 7 fF, the total input node capacitances during the amplification phase is 9.5 and 11.25 fF for the cascode and the common-source amplifier designs, respectively. This will lead to the 25% larger input signal in the pixel with the cascode amplifier.

The noise performance of a common-source stage can be described by the equivalent input noise ($\overline{dv_{itot}^2}$)

$$\overline{dv_{itot}^2} = \overline{dv_{ie}^2} + \frac{\overline{di_L^2}}{g_m^2} \tag{4.6}$$

where $\overline{dv_{ie}^2}$ is the transistor equivalent input noise voltage, $\overline{di_L^2}$ denotes the noise current of the load resistor R_L. Substituting $\frac{8kT}{3}\frac{1}{g_m}$ for $\overline{dv_{ie}^2}$ and $4kT/R_L$ for $\overline{di_L^2}$, we can estimate the excessive noise as

$$\frac{\overline{dv_{itot}^2}}{\overline{dv_{ie}^2}} = 1 + \frac{1.5}{g_m R_L} \tag{4.7}$$

This shows that the equivalent input noise of the amplifier depends mostly on the noise of the input transistor. For low noise applications, the transistor transconductance should be as large as possible, which in this case is compatible with obtaining large gain.

In the cascode structure, the current passing through the transistor is not affected by the gate voltage. It is determined by the cascode biasing and input current. Therefore the output noise current caused by the input equivalent voltage noise for this transistor is equal zero. This holds true for relatively low R_L, which is the case of the designs discussed later. In general, for large R_L the noise will begin to be amplified linearly to the R_L up to the gain over the cascode transistor itself.

The noise performance of cascode and common-source amplifiers in MAPS will be similar and dominated by the noise of the input transistor.

4.2.2 Tools for design verification

Three important tools that aid transistor level simulations and allow for verification of the robustness of a design are:

- layout extraction - to estimate influence of parasitic components
- Monte Carlo simulations - to estimate influence of process dispersion
- noise simulations

Layout extraction

Layout extraction is one of the basic tools which allows a designer to verify operation of his circuit. It translates the integrated circuit layout into the electrical description, typically in the form of a netlist. As a result, the circuit description will contain the components placed by the designer and new, parasitic elements that are not intended but are inherent in the layout of the circuit. Parasitics result from real interconnections and orientation of components. Layout extraction tools allow, with certain accuracy, to identify parasitic resistances, capacitances and diodes. Back annotating these extracted components to the original design allows more realistic

evaluation of the circuit's performance and to avoid malfunctioning devices. Differences are usually small. For example, for pixels in the MIMOSA IX prototype that contain in-pixel amplifiers (presented in Chapter 4.2.3), the bandwidth of a pixel readout chain is 4.0 MHz and 3.8 MHz for the schematic design and extracted layout, respectively.

The extraction of parasitic components can be performed on a flat design or based on the hierarchical structure. The first one is more robust but it is also much slower for large designs. All the extractions discussed in this work concerned mainly single pixel structures and were performed on flat designs. Simulations after the extraction are very important in the design of integrated circuits and many designs turn out to be very layout sensitive, for example MIMOSA VI and MIMOSA VII discussed later.

Monte Carlo simulations

Fabrication of microcircuits in silicon wafers is inevitably bound to be influenced by variations in the manufacturing process parameters. Analog IC can be highly sensitive to these uncontrollable random variations, such as slight changes to the amount of diffusion time, uneven doping levels, oxide thickness, and threshold voltage. Process variations will affect the circuit yield as well as its performance. On the micro scale, it will result in differences between the identical, from the design point of view, components placed in one chip. On the macro scale, circuits may exhibit different behavior depending on their exact placement on the processed wafer. Each manufacturer delivers dedicated tools for estimating circuit performance as a function of process parameter variations.

Statistical analysis allows microcircuit designers to study the relationship between the performance of the circuit and process variations. Unlike the deterministic worst-case (corner) analysis, the statistical analysis determines the probability distribution for a chosen parameter. This is achieved with Monte Carlo simulations. For MAPS aiming at the on-chip data sparsification, the uniformity of the pixel array is a crucial issue and this type of simulations is used extensively. An essential part of a statistical analysis is device models with assigned statistically varying parameter values. The shape of each statistical distribution represents the manufacturing tolerances on a device. The statistical analysis performs multiple simulations and each simulation uses different parameter values according to the assigned statistical distributions.

Typically, this statistical analysis supports simulation of device mismatches on a single wafer level and/or process level. Monte Carlo simulations performed in the studies of in-pixel amplifier structures presented in this work are based solely on mismatches on a wafer level.

For example, results of a Monte Carlo simulation for one of the in-pixel amplifier architectures implemented in the MIMOSA IX prototype are presented in Figure 4.5. Variations of three crucial parameters are presented for 300 iterations. The first parameter is the gain of the amplifier stage. The mean gain value is around 6.2, with the standard deviation of 0.063 that is equivalent to a 1% variation. The second parameter, the gain at the pixel output is expected to average at 5.1 with 0.8% variation ($\sigma = 41$ mV). The last parameter, which is the DC voltage level at the output of the pixel, reaches 590 mV with 43 mV, or 7%, variation. The level of dispersions at the output of the amplifier is expected to be on the same order of magnitude as the amplified signal generated by an ionizing particle. These numbers prove that it is crucial to minimize dispersions between pixels before the read out signal can be discriminated with a threshold that is common to many pixels.

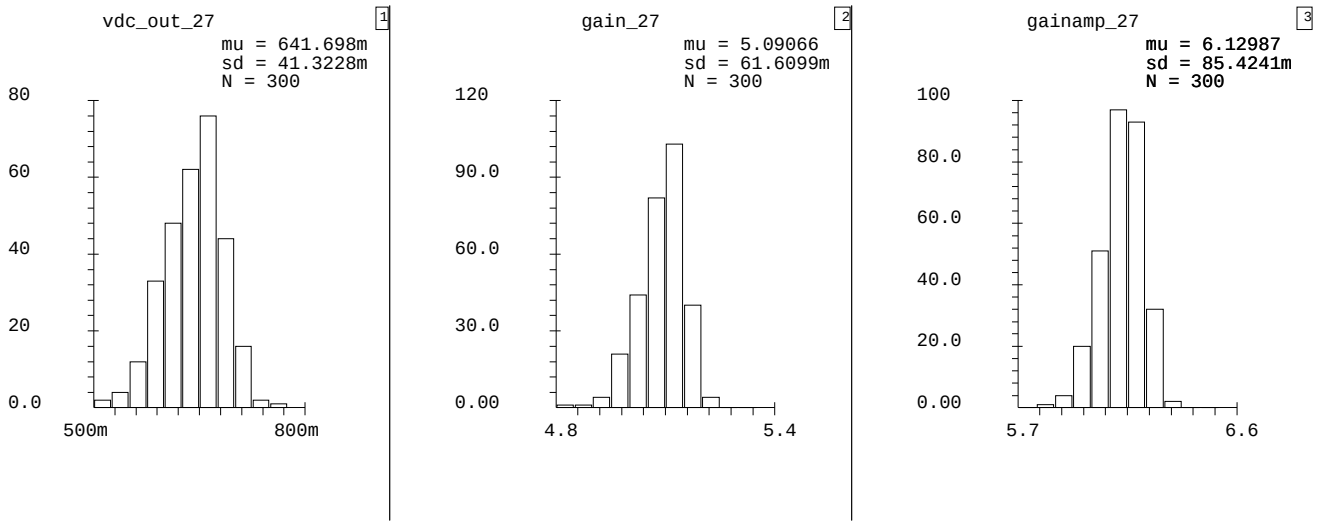


Figure 4.5: Results of Monte Carlo simulations for pixel1 implemented in MIMOSA IX. The voltage level at the output of the amplifier (1) varies with the standard deviation of 40 mV. The variations of the amplifier gain (3) and the gain of the full readout chain (2) are on the order of 1.4% and 1.2%, respectively.

Noise simulations

Design of low noise devices requires tools that provide precise estimations of noise performance. The CAD tools available on the market allow for different types of analysis of which DC and AC analyses are the most popular. DC analysis calculates the operating point of a circuit while neglecting all capacitances and inductances. AC analysis is a small signal analysis used when frequency response is of interest.

The AC analysis simulates noise in the frequency domain. However, this approach is limited to circuits which exhibit time-invariant, steady state operation and cannot be used for time varying and switching circuits. Methods called periodic analyses overcome this limitation and provide IC designers with detailed insights into the noise behavior of circuits such as PLL dividers, voltage controller oscillators (VCOs), phase detectors and switched-capacitor filters. These methods calculate the total time-averaged noise over a given frequency range. An example of such an analysis available in SPECTRE simulator in the Cadence package is the Periodic Steady-State (PSS) analysis and a set of Periodic Small-Signal analyses that include noise calculations. PSS is a large signal analysis that directly computes the steady-state response of a circuit with a simulation time that is independent of the circuit's time constants. The small signal analyses are similar to the conventional methods but can be applied to periodic circuits where frequency conversion plays a critical role. These methods linearize the circuit about the periodic operating point and include frequency conversion effects.

A more accurate noise analysis of switched circuits can be accomplished using a transient analysis method. This method is referred to as *transient noise analysis*. This analysis associates a source of noise with each noisy element to generate temporal noise according to the assumed spectral density. Since the transient noise analysis is more direct for pixel simulations than periodic analyses, it was used in this work for simulating noise performance of MAPS prototypes. For example, the current integrating transimpedance amplifier implemented in the MIMOSA VII

prototype and based on switched capacitors was simulated using this approach. The software used for the transient noise analysis was the Spice-like simulator ELDO by MentorGraphics [84].

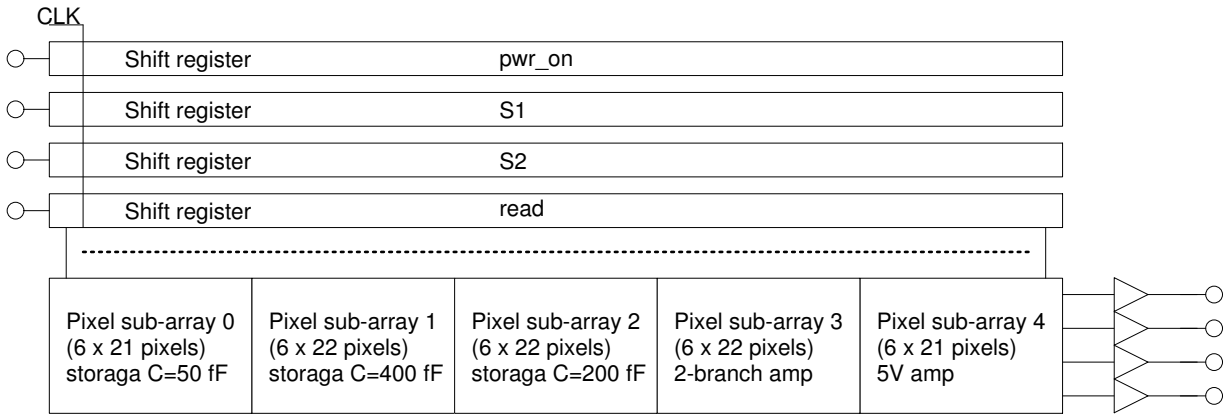
4.2.3 MAPS prototypes with in-pixel amplifiers

Several amplifier structures were studied and tested on small scale prototypes within this work. Most of them included the pixel architecture presented in Figure 4.6(b). The following pixel components can be distinguished:

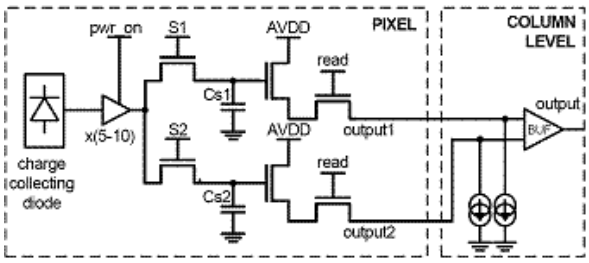
- charge collecting diode in the self-biased configuration and AC coupling to the amplifier,
- small gain NMOS amplifier,
- two memory capacitors for storing two consecutive in time voltage samples for CDS processing,
- subtraction of the two stored samples performed outside of pixel.

The first verification of the feasibility and flexibility of the in-pixel amplification was attempted in the MIMOSA VI prototype, prior to the work presented in this thesis. The same prototype tested the idea of storing two voltage samples in one pixel for their later subtraction. Also, the functionality of comparators implemented at the column level was demonstrated. Unfortunately, the performance of MIMOSA VI was significantly below expectations and high pixel-to-pixel output level dispersions were observed, preventing complete tests of the chip. The pixel pedestal variations of approximately 120 e^- and the ENC noise of 20 e^- were measured [85]. This lead to more recent developments of new pixel designs exploiting the amplification and in-pixel storage. The MIMOSA IX prototype was fabricated in the AMS 0.35 OPTO technology with the epitaxial layer thickness of about 14 μm. The main part of the sensor was dedicated to testing different ideas for improving radiation tolerance. In addition, different sizes of charge collecting diodes and different pixel pitches were used to optimize the signal-to-noise ratio and spatial resolution. The MIMOSA IX prototype contains four arrays of pixels with a square pitch varying from 20 μm to 40 μm. The array size is 64×64 pixels for the 20 μm pixel pitch and 32×32 for other arrays. The implemented pixel architectures are based on the 3-transistor pixel cell and the self-biased 2-transistor cell. The signal from the pixel array is readout through a buffer stage with the gain of five.

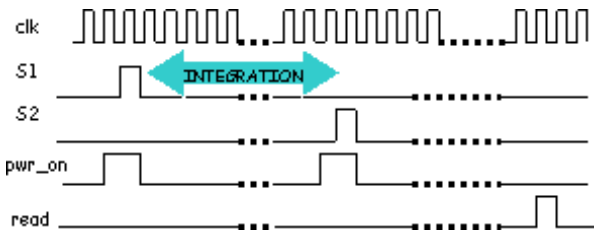
The improvement on the radiation resistance is based on the elimination of thick oxides present near the charge collecting diode that are responsible for charge trapping and surface damages induced by radiation. The thick oxide is removed from the vicinity of the charge collecting diode using special layout techniques that introduce diffusion regions and polysilicon layers. Presence of diffusion or polysilicon layers eliminates the growth of thick oxides in these regions. An example of such design is presented in Figure 4.7(b) where the field oxide (FOX) cannot be created in the vicinity of the n-well due to the highly doped n+ region (refer to steps in the planar CMOS process in [22]). For comparison, a standard diode design with thick oxide regions is presented in Figure 4.7(a). The achieved improvement in radiation tolerance is highlighted in Figures 4.7(c) and 4.7(d). The radiation-induced increase of leakage current in the structure with the improved layout is reduced by a factor of approximately 5, compared to the standard structure.



(a) architecture



(b) pixel structure



(c) timing diagram

Figure 4.6: The architecture of the test structures with various in-pixel amplifiers and storage capacitors implemented in the MIMOSA IX chip, (a). A general schematic diagram of pixel cells, (b), and the timing diagram of the control sequence, (c).

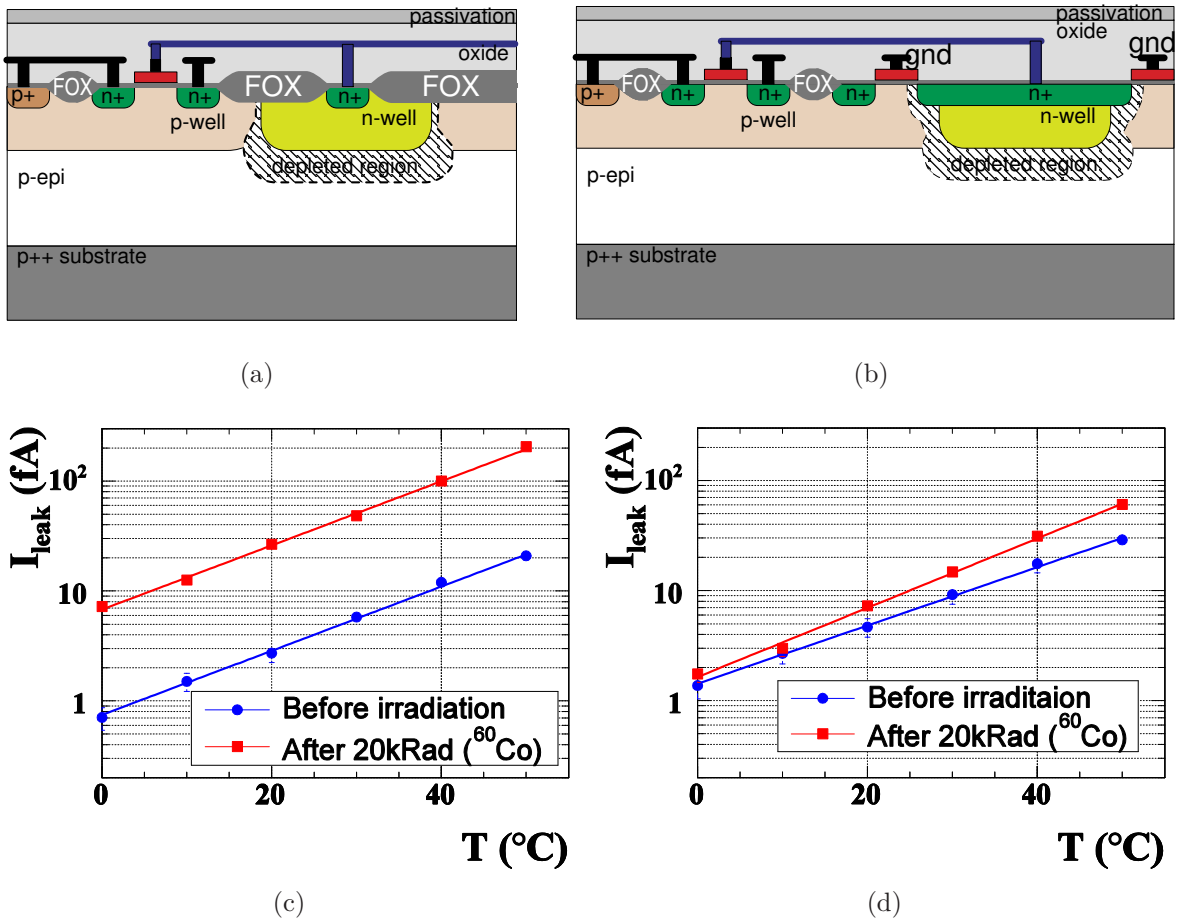


Figure 4.7: Cross section view through a standard charge collecting diode, (a), and through the MIMOSA IX/MIMOSA XI pixel diode with increased radiation tolerance. The increased radiation tolerance results from elimination of thick layers of the field oxide form the vicinity of the charge collecting diode. The leakage current increase for the standard, (c), and thin-oxide diode, (d), as a function of temperature before and after receiving the ionizing radiation dose of 20 krad.

A test structure with a novel pixel architecture was included in the MIMOSA IX design. The structure consists of in-pixel voltage amplifier AC coupled to the charge collecting diode and followed by two analog in-pixel memory cells. The memories hold continuously the signal from two successive frames. During the write phase, the signal is stored alternatively on one of the memories. During the readout phase, the two samples are readout in parallel and subtracted by an external differential amplifier. The pixel structure, which is sketched in Figure 4.6(b), includes part of the circuitry needed for the CDS operation. This pixel structure separates the integration time from the readout time of the sensor. In-pixel signal sampling can be performed at one pace, while pixel readout can be synchronized with a different clock frequency. This architecture is suitable for applications that require a triggered readout, i.e. where the readout phase is initialized with an external trigger pulse.

Several versions of in-pixel amplifiers were implemented in MIMOSA IX. The most basic design, employing a simple cascode structure, aimed at providing the voltage gain of five. A higher gain of approximately 10 was to be obtained in amplifiers using thicker gate oxides available in the technology used. More details on the pixel structures will be given in section 4.2.4. All groups of pixels are organized into 6 columns of 128 pixels each (4 columns for parallel readout and 2 dummy boundary columns to assure array uniformity). The access to rows of pixels is accomplished with four shift-registers, with the length equal to the number of rows. Each shift register propagates one digital signal controlling a switch or switches inside a pixel. These signals include *sample 1*, *sample 2*, *power on*, and *read*. An external logic circuit provides these signals as well as the clocking signal. An example of the control sequence is presented in Figure 4.6(c).

Results obtained with the MIMOSA IX prototype for both radiation tolerant diode designs and new pixel architectures containing in-pixel amplifiers lead to the next iteration of the prototype called MIMOSA XI. The new sensor was fabricated using the same technology and with a similar architecture. The main four matrices are built from two sub-matrices each. Each sub-matrix is built from 21×42 pixels with a pitch of 30 μm. All structures contain self-biased diodes. What distinguishes sub-matrices are details in the radiation tolerant layout. Different layouts eliminate thick oxide from different locations in the surrounding of the charge collecting diode. Similarly to the test structures in the MIMOSA IX chip, test structures with nine different types of in-pixel amplifiers were implemented as an array of 6×108 pixels. The digital control of the array was implemented in the same way as in MIMOSA IX and all digital signals were delivered from an external source. This sensor allowed better understanding of the in-pixel amplifiers and was aimed at explanation of problems observed on MIMOSA IX. The next section describes the results obtained with MIMOSA IX and MIMOSA XI prototypes.

The study of radiation tolerant pixel layouts with MIMOSA IX and later with MIMOSA XI, which is beyond the scope of this work, allowed establishing a structure with performance that should satisfy the STAR upgrade requirements for 2007. Important results will be presented in later chapters when the dedicated prototype called MIMOSTAR2 is discussed. The additional description can be found in [62].

Different in-pixel amplifier architectures have been studied and implemented in MIMOSA IX and MIMOSA XI prototypes. The structures of amplifiers were based on a simple cascode architecture but used different techniques to optimize the gain of this stage (schematics of these amplifiers are provided in Appendix B):

- amplifiers in the cascode configuration (Figure B.1(a));

- double branch structure - the first branch is a typical input amplifier load; the second branch increases the transconductance of the input amplifier by delivering higher current (Figure B.1(b));
- cascode amplifier benefiting from the 5 V transistors, available as an option in the AMS 035 process, with thicker gate oxide compared to standard 3.3 V devices. The expected advantage from this amplifier results from increased conductance of the load transistor compared to a default transistor (Figure B.1(c));
- cascode amplifier with feedback circuit for stabilizing the input voltage for the AC coupled configuration (Figure B.1(d)).

The amplifier structures were studied in simulations that were completed with measurements. The most important parameters for MAPS optimization that were investigated included: power dissipation, bandwidth, noise performance, pixel-to-pixel dispersions, in-pixel gain and its linearity. The results are presented next.

4.2.4 Performance of in-pixel amplifiers

The most important parameters studied for optimization of MAPS performance included: power dissipation, bandwidth, noise performance, pixel-to-pixel dispersions, in-pixel gain and its uniformity. All the results are summarized in Table B.1 in Appendix B.

The power dissipations simulated for one pixel is typically between 20 and 30 μW. This is a relatively small value that should satisfy stringent power consumption requirements for vertex detectors. It also leaves room for improvements.

The bandwidth of the readout chain was studied at two points: at the amplifier output which was coupled with an in-pixel memory cell and at the output of the pixel with an assumed 5 pF capacitance for the full length of the readout line. The bandwidth of the amplifier can be optimized by selecting an appropriate value of the in-pixel memory cell. The capacitance has to be chosen to provide satisfactory speed of pixel operation and, at the same time, to limit the influence of high-frequency noise at the output of the amplifier. All of the studied structures worked with bandwidths of several mega hertz which should be suitable for sensors that will require a pixel readout time of about 1 μs.

The noise performance was simulated for the amplifier alone and with the addition of other pixel components up to the complete readout chain, including CDS operation. The measured performance is within 50 to 80 mVrms and closely matches simulation results. The values translate to equivalent noise charge of about 20 electrons at room temperature with the smallest value of 12 electrons achieved for a pixel with DC coupling. The lower noise for the DC coupled amplifier results from the higher gain of this structure, as explained in Chapter 4.2.7.

The gain of the pixel was measured by three different methods. One method was the ^{55}Fe calibration. The other methods were based on variation of the amplifier input voltage when the sensor readout was running continuously (referred to as a dynamic measurement) and when the readout was stopped on one pixel (static measurements). In all cases the gain measured was smaller than simulated. The worst result was obtained with static and dynamic measurements where the discrepancy was the largest (up to a factor of 4 for the amplifiers with gain of 9 - two-branch amplifier and the structure with 5 V transistors). A set of simulations was performed with

different parameters and parasitics to explain the observed behavior, but it was unsuccessful. Calibrations with iron source revealed gain of only 70% of the expected value.

A plausible explanation for the missing gain pointed towards the new implementation of the AC coupling of the amplifier and the charge collecting diode. To verify this, a separation of the diode and the amplifier was performed through a cut of the metal path connection with a Fixed Ion Beam ([86]) in three pixels in the sub-array with classical cascode structure. However, the gain measured before and after the cut was comparable. The result invalidated the initial explanation.

Simulations of gain for all amplifiers show that the uniformity of gain at the ±5% level corresponds to the variation of operating points of 40 mV, for the two-branch amplifier, and up to 95 mV, for classical cascode structures. The gain uniformity influences pixel-to-pixel dispersions due to variations of the operating point and the resulting gain. Simulated fixed pattern non-uniformities reached 70 mV for high gain amplifiers (two-branch and 5 V transistor structures), to about 40 mV for classical cascode structures, and to only 12 mV for the amplifier with a feedback stabilization of the operating point. The measured FPN for different pixels is higher than the theoretical estimations. The highest discrepancy is close to the factor of three for the DC coupled amplifier, for which the simulated FPN value is 40 mV. However, CDS processing of the stored samples reduces the FPN below 10 mV for all pixel architectures. The effect is due to good matching of the two in-pixel source followers used for reading out the two stored samples. Simulated gain uniformity is in all cases below 2%, satisfying the requirement introduced in Chapter 4.1.1.

Amplifiers with the input PMOS transistor were also studied at IPHC, but their optimizations led towards the structure of the PhotoFET cell, which is presented in Chapter 3.3.1. At the time of the study, the most reliable and well performing amplifier structure available was based on NMOS transistor amplifiers, DC coupled with the charge collecting diode. Details explaining the lack of the expected improvement in performance of the proposed AC coupling are presented in Chapter 4.2.7.

4.2.5 Further optimization of pixel structures

The study summarized in the previous chapter guided the amplifier development towards simple structures based on NMOS transistors. Shortly after finishing the study presented, one of the designers at IPHC proposed a new amplifier architecture [87]. The gain of the amplifier is improved by replacing the NMOS load transistor with a pair of NMOS transistors. Such combination of transistors allows the gate of the load transistor to change together with the output voltage, emulating a PMOS transistor. The circuit provides higher AC gain while the operating point remains the same. A simplified schematic view of the amplifier is presented in Figure 4.8.

The gain of the amplifier can be calculated based on a small signal equivalent circuit. A small-signal equivalent circuit is a linearized circuit picturing the relationships between the small-signal voltages and currents in a linearized circuit. In a small-signal equivalent circuit model, the signal variations around the dc-bias operating point are very small. A simplified equivalent circuit for a single transistor is presented in Figure 4.9(a). The bulk effect is not presented, since typically MOS transistors operate at a constant source-bulk voltage.

In the calculations presented below, the parasitic capacitances were omitted to simplify the

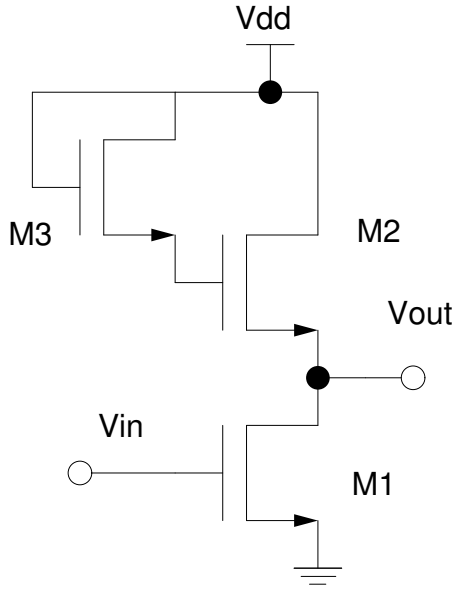


Figure 4.8: Simplified schematic of an in-pixel amplifier with high gain. Switches necessary for pulsed-power operation are not shown. The classical load of the common-source amplifier (M2) is modified with an additional transistor (M3) to enhance the gain of the structure.

analysis and to show the main principle of operation of this amplifier structure. The amplifier from Figure 4.8 can be analyzed with an equivalent circuit as presented in Figure 4.9(b). The transistor labeled M3 is in diode configuration and, therefore, can be presented as a resistance of $1/g_m$ (Figure 4.9(c)). The only important capacitance for this simplified analysis of the circuit is the gate-source capacitance of the load transistor (M2) that contributes to the increased gain and is presented as C_{gs}. The circuit can be further transformed and simplified to the diagram presented in Figure 4.9(d).

Kirchhoff's current and voltage law equations[4] for this circuit lead to the set of two equations (Equation 4.8). Solving these equations for gain of the amplifier gives Equation 4.9.

$$\begin{cases} V_{g2} = V_{out}\left(\frac{j\omega C}{j\omega C+g_{m3}}\right) \\ V_{out} = -\left[g_{m1}V_{in} - g_{m2}\left(V_{g2} - V_{out}\right)\right]\frac{1}{g_{ds1}+g_{ds2}+\frac{j\omega C g_{m3}}{j\omega C+g_{m3}}} \end{cases} \tag{4.8}$$

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2} + \frac{j\omega C g_{m3}}{j\omega C+g_{m3}} + g_{m2}\frac{g_{m3}}{j\omega C+g_{m3}}} \tag{4.9}$$

The increased gain of this amplifier results from the fourth factor in the denominator. The value of g_{m3} is very small compared to any other transconductance in the circuit. For low

[4]Kirchhoff's circuit laws express conservation of energy. Kirchhoff's current law: The amount of current entering a circuit node equals the amount of current leaving a circuit node. Kirchhoff's voltage law: Any closed loop of circuit branch voltages sums to zero.

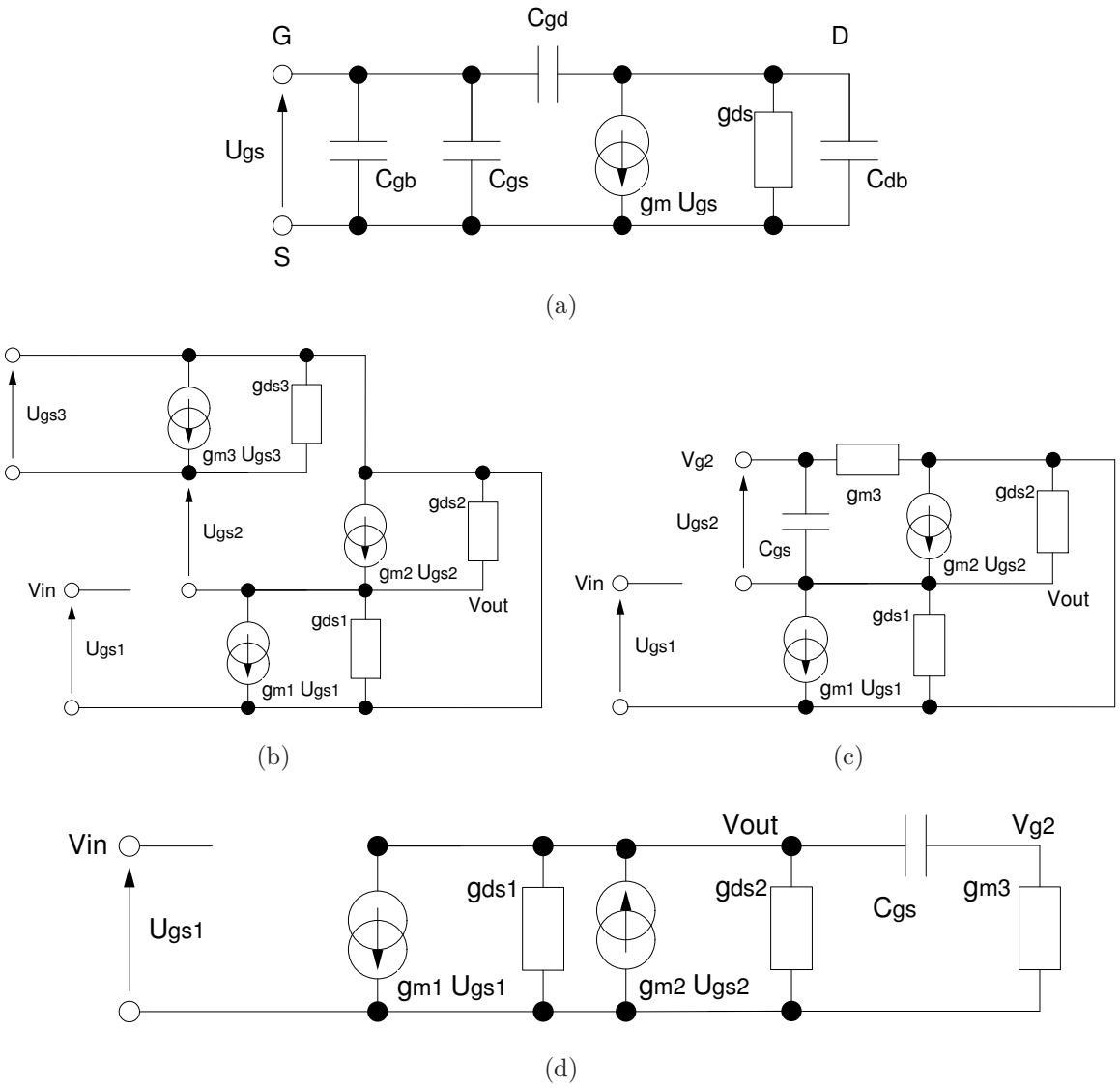


Figure 4.9: Analysis of a high-gain in-pixel amplifier. Simplified small-signal model for a MOS transistor (a). Small-signal model for the amplifier structure, (b). The same circuit after simplifications and addition of the gate-source capacitance for the first of the load transistors (c). The final small-signal circuit used for calculations that are presented in the text (d).

frequencies, the small value of $j\omega C$ can be neglected and the gain of the circuit simplifies to:

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2} + g_{m2}} \tag{4.10}$$

Since $g_{ds1} + g_{ds2}$ is typically smaller than g_{m2}, the gain simplifies to the simple approximation of the common-source amplifier, where $G = -g_{m1}/g_{m2}$.

For higher frequencies, the value of $j\omega C$ decreases the value of the multiplier of g_{m2} and leads to a smaller value of the denominator and, therefore, increases gain. The maximum gain would be expressed by Equation 4.11, however, it is reduced by other parasitic capacitances and bulk effects that add in the denominator but were omitted for simplifying these calculations.

$$\frac{V_{out}}{V_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2}} \tag{4.11}$$

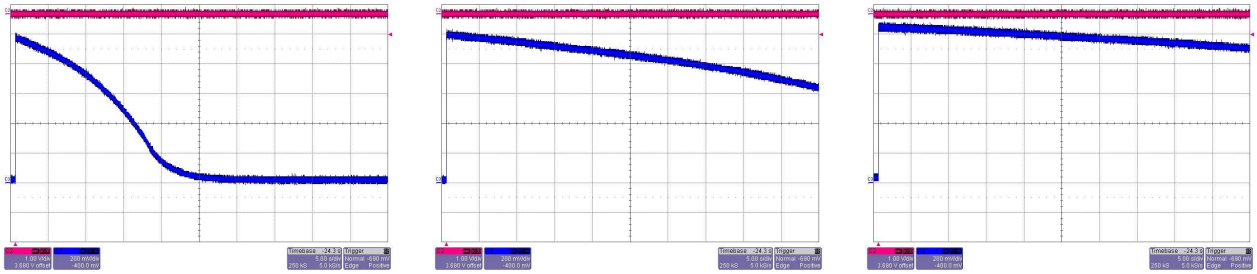
Further improvement in the performance of pixel cells has been observed with negative feedback between the output of the amplifier and the biasing voltage of the charge collecting diode.

4.2.6 Discharge time of memory capacitors

The in-pixel memory is crucial for on-chip signal processing. It has to be large enough to store the signal information until it can be read out. In the case of MAPS, the time between storage and readout is typically the readout time of a complete pixel array, hundreds of microseconds to a few milliseconds. The physical size of the storage capacitor might be important for sensors with small pixels or sensors that require a certain number of storage cells in each pixel. The most compact voltage memory cell can be accomplished with a transistor, because of the high value of the area capacitance of gate oxide (several fF/ μm^2).

Pixels implemented in test structures in the MIMOSA IX chip contained different sizes of memory capacitors that allowed studies of memory cell discharge time. Three sizes of memory capacitors were implemented in the MIMOSA IX prototype pixels: 52 fF, 200 fF and 400 fF. The capacitors were built from NMOS transistors with the width and length of the gate set to W=1.7 μm L=6.8 μm, W=6.8 μm L=6.8 μm, W=9.4 μm L=9.4 μm, respectively.

The measurement was performed with an oscilloscope probe connected to one of the output lines. The array of pixels was continuously powered and one of the memory capacitors was continuously sampling signal from the amplifier. After tens of write/read cycles, the *sample* signal was switched off, while *read* and, a few clock cycles later, the clock signal for the readout sequence were stopped, locking the readout on one chosen pixel. At that point, the trigger signal for the acquisition was issued. The capacitor discharge curve was registered on the oscilloscope. The results are presented in Figure 4.10. The shape of the discharge curve is affected by the voltage on the gate node of the transistor. The discharge curve is linear for gate voltages above the transistor's threshold voltage, since the capacitance and leakage current are constant. Below the threshold voltage, the capacitance starts to decrease and the discharge curve exhibits larger slope. Visual inspection of the graphs indicates that the discharge time from the initial level of 1 V to about 800 mV is approximately 50 s for the largest capacitor, 25 s for the middle sized one, and approximately 7 s for the smallest one. This is linearly proportional to the size of the capacitor. One can conclude that for storing times on the order of milliseconds, a few tens of



(a) 50 fF (b) 200 fF (c) 400 fF

Figure 4.10: Discharge curves for signals stored on in-pixel memory capacitors of 52 fF, 200 fF and 400 fF implemented in the MIMOSA IX prototype. The time scale in the presented plots is 5 s/div and the amplitude is 200 mV/div.

femto farads should be sufficient. Similarly, the discharge time of two capacitors from the same pixel was compared on several pixel samples. Visual inspection of the results did not show any discrepancies between capacitors from the same cell. However, this method was not sufficiently precise to quantify the differences more accurately than to within several percent.

4.2.7 Advantages of AC and DC coupling

Charge collection efficiency, CCE

To prove the expected advantages of the AC coupling of the charge collecting node with the in-pixel amplifier, a series of calibrations with ^{55}Fe was accomplished with different bias voltages on the charge collecting node. The test results acquired with different prototypes clearly show an increase of the charge collection efficiency, CCE, proportional to the applied biasing voltage. CCE is defined as the ratio of the signal peak reconstructed in a cluster to the amplitude of the calibration peak. An example of the CCE measured for two different prototypes as a function of biasing voltage is presented in Figure 4.11.

The change of CCE with bias voltage is clearly visible; however, the magnitude of the change is approximately 5% in the whole voltage range. The difference between results obtained with MIMOSA VIII and MIMOSA XI prototypes can be attributed to different fabrication processes. MIMOSA VIII was built in the TSMC process with a thin epitaxial layer, less than 8 μm thick. MIMOSA XI was built in the AMS 0.35 OPTO process on the epitaxial layer twice as thick. Charge diffusion in a thicker epitaxial layer will affect a larger area and, for this reason, MIMOSA XI collects less charge in a 9-pixel cluster used in this study.

The influence of the increased collection efficiency on the detection efficiency remains not quantified. The reason is that the sensing arrays were too small to be studied in a MIP test beam. At the same time, the MIMOSA XI and MIMOSA VIII prototypes showed a slight noise increase of approximately 5 and 7%, respectively. Judging from the small increase of the charge collection efficiency and negligible noise performance variations, an assumption of low improvement on detection efficiency could be justified. Tests with a simple DC pixel structure (self-biased + 2T) can help to get a better insight to this assumption. MIMOSTAR2 (Chapter 6) served as subject to these tests. Tests of the MIMOSTAR2 sensor with diode biasing voltages of

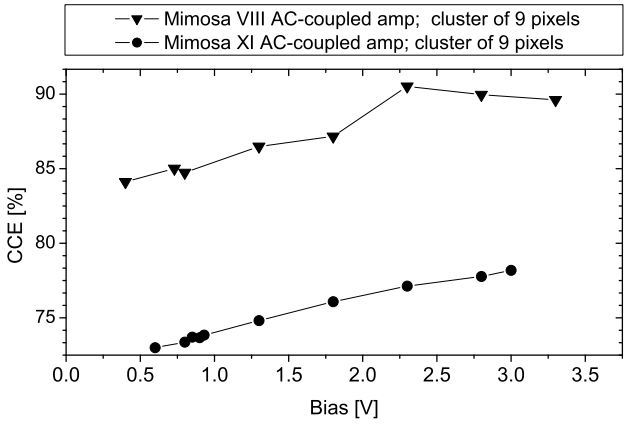
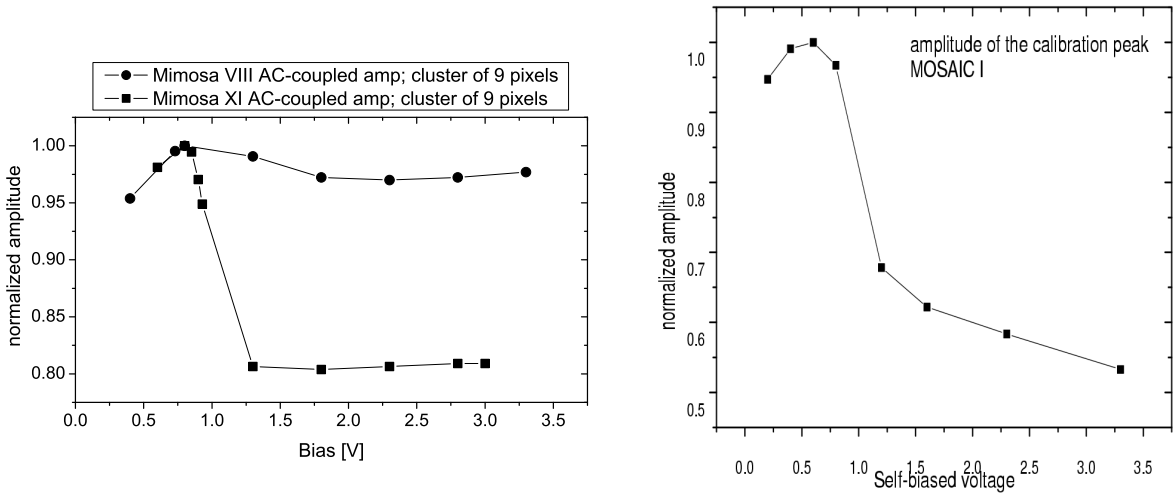


Figure 4.11: Charge-collection efficiency measured for different biasing voltages on the self-biased structure.



(a) (b)

Figure 4.12: Calibration peak amplitude as a function of the diode biasing voltage in MIMOSA VIII, MIMOSA XI, MOSAIC1(MIMOSA XII)). The plots are normalized to the highest measured value.

3.3 and 2.2 V were performed during tests with an electron beam at DESY, Hamburg. Details of the test setup will be presented in Chapter 6.3.4. The results showed no visible change in the charge collection efficiency. Furthermore, no difference in detection efficiency between the two bias points was observed.

The tests with a variable biasing voltage on the charge collecting diode revealed another property of the AC coupling. The magnitude of the calibration peak, and therefore the charge-to-voltage conversion gain, was dependent on the bias voltage applied. This is shown for three prototypes (MIMOSA VIII, MIMOSA XI and Mosaic1) in Figure 4.12. The magnitude is normalized to its highest value. It is easily noticeable that all the curves have maximum located at

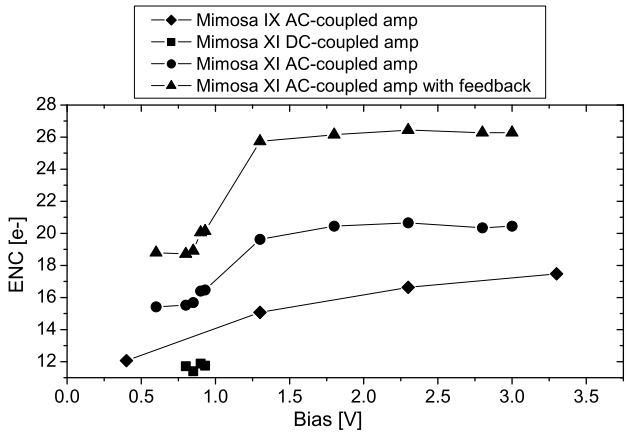


Figure 4.13: ENC as a function of the diode biasing voltage measured for four different pixel structures.

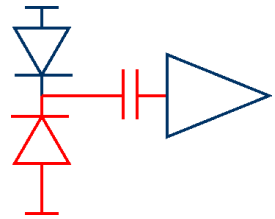
about 0.7 V and that for higher bias values the magnitude decreases. The difference between the shape and amplitude between prototypes can be attributed to different technologies. Different thickness of gate oxide in MIMOSA VIII and MIMOSA XI leads to different capacitances of the coupling capacitors, which results in different amplitudes of the calibration peak.

The calibration peak amplitude is used for extracting equivalent noise charge for sensors. The ENC of the prototypes tested is presented in Figure 4.13 as a function of the biasing voltage. As expected, the increase of the amplitude of the calibration peak, presented in Figure 4.12, corresponds to a lower value of ENC. It can be observed, that the best noise performance has been achieved with a DC coupled amplifier.

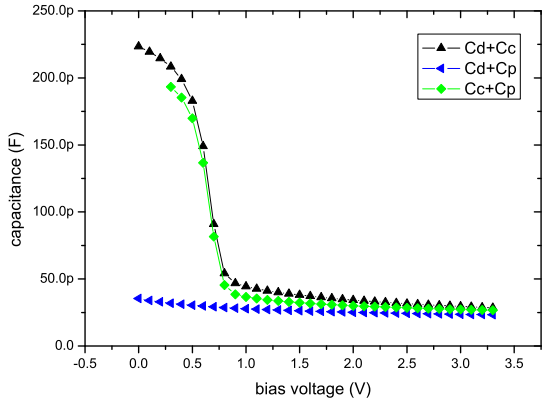
The AC coupling presented in Chapter 4.1.2 can be expected to function as a MOS capacitor. To better understand the AC coupling and its properties, a simple test structure was implemented in the MIMOSA XII (Mosaic1) prototype [88]. This device was fabricated in a technology with high resistive substrate. The main array structure allowed performing tests of charge collection as a function of the diode biasing voltage. A small test structure implemented in this prototype was designed for directly testing the AC coupling. It was composed of the charge collecting diode and the gate oxide on top of the n-well forming the coupling capacitor (red part in Figure 4.14(a)).

The measurement results show that the capacitance of the coupling capacitor changes as a function of the biasing voltage (Figure 4.14(b)). In addition, simulations based on the Variable-Capacitance[5] ([89]) component were performed (Figure 4.14(c)). The component is similar to a PMOS transistor but its drain and source nodes are replaced by n++ regions. The test structure in MIMOSA XII did not have these highly doped regions. Nevertheless, the capacitance measurement results agree qualitatively with simulations.

[5]MOS varactors are commonly used in integrated Voltage Controlled Oscillators (VCO).



(a)



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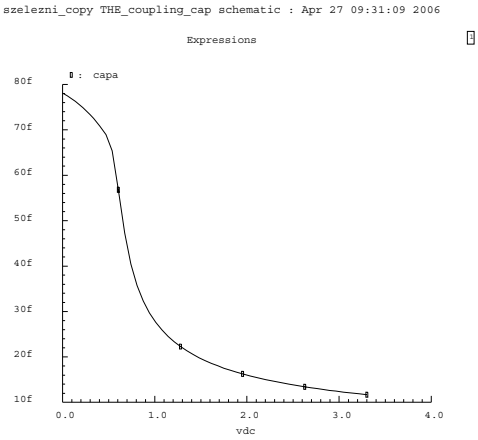
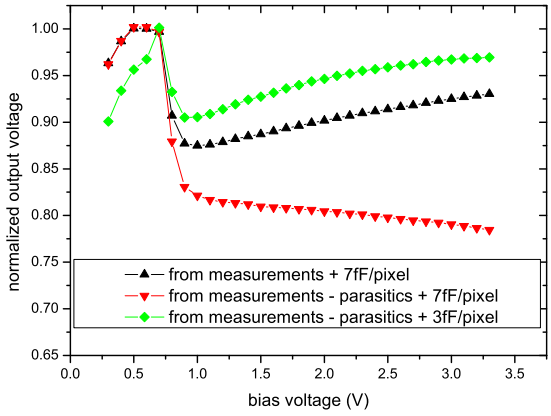


(c)



(d)

Figure 4.14: Schematic of the MIMOSA XII test structure for investigating in-pixel AC coupling, (a). Characteristics of AC coupling: capacitance measurements on the test structures in the Mosaic1 prototype (b), simulations of the variable capacitance element CVAR (c), model of pixel gain derived from capacitance measurements, (d). Capacitance between all three terminals was measured to extract the diode capacitance (Cd), the coupling capacitance (Cc), and the parasitic capacitance (Cp). For the model of pixel gain, the parasitics in the structure were estimated from the extracted layout. Different slopes of the curves reveal that the modeled behavior depends strongly on parasitic capacitances and pixel capacitance values.

4.3 On-chip data sparsification

Several readout schemes can be imagined for MAPS sensors. The classical approach to the readout of MAPS sensors is based on a rolling shutter mode with the integration time equal to the readout time. Sending information to a data acquisition system, in the simplest implementation, can be implemented as serial analog readout of all pixels. The disadvantage of this technique is the fact that for large matrices the readout of the whole detector is very slow. Modifying this scheme by dividing the pixel array into sub-arrays and parallelizing outputs increases the readout speed and shortens the integration time. When a very short readout time is required a high parallelism is indispensable.

Very fast analog readout can be used in systems based on single sensors. However, for complex systems such as micro vertex detectors, where tens of sensors operate in parallel, a high readout speed produces an enormous data flow. Transferring correctly all data and storing it into mass storage systems becomes a very difficult task. It is apparent that the important information in one event in the detector is enclosed in a limited number of sensors and pixels. The other parts that are not touched by traversing particles do not produce any relevant information. If the STAR PIXEL detector built form two barrels of 6 and 18 ladders and containing 10 sensors on each of them was readout in 4 ms with an external analog-to-digital conversion on 12 bits, the complete system would require data throughput of 280 Gb/s. At the same time, for the goal luminosity of the RHIC II, 50 incidental clusters per cm^2 and per second are expected. For a detector size of about 2 cm $\times$ 2 cm and assumed cluster size of 10 pixels per single hit, these numbers give 2000 pixels with meaningful information compared to 400 k pixels in total. The possible reduction of the data flow is significant.

Data sparsification in the system has a fundamental meaning. The algorithms should be implemented as close to the pixel as possible, i.e., at the ladder level or, in the best case, on-chip. Combination of the two techniques, parallel readout and data sparsification allows reaching high detector readout speeds with reasonable data flows. These two design directions are currently followed in MAPS developments at IPHC.

For the STAR upgrade originally planned for 2007, a large area chip ($\sim$ 2 cm $\times$ 2 cm), divided into 10 sub-arrays readout in parallel was proposed. Data from parallel outputs would be multiplexed on two fast, differential current-mode drivers. This structure would provide a 4 ms signal integration time, equal to the full-detector readout time. The analog signals would be converted to digital at the ladder level with a zero suppression algorithms placed in FPGA devices, as discussed in Chapter 7.3.

There is, however, one drawback of on-chip sparsification. A detector with complicated readout electronics will have an increased power consumption/heat dissipation compared to a simple design. In the STAR environment, where only forced air-flow cooling is allowed, it might be more efficient to place signal processing off-chip, reducing the heat dissipation and the particle insensitive chip area (material budget). Additional electronics needed for signal processing could be placed outside of the low-mass region, where additional cooling might be provided.

On-chip data digitization

On-chip digitization of signals read from pixels is an important aspect of data flow reduction and the on-chip data sparsification. This problem was addressed with two MAPS prototypes

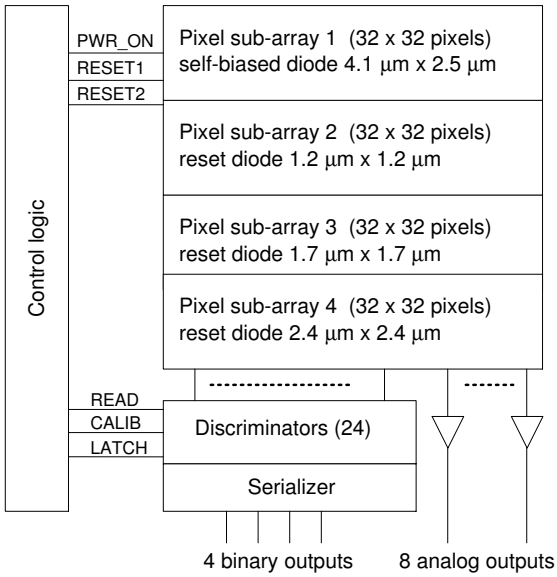


Figure 4.15: Architecture of the MIMOSA VIII chip. The pixel array in MIMOSA VIII is divided into four sub-arrays with different pixel architectures. All columns are read out in parallel - 24 are read out through on-chip discriminators and 8 columns are optimized for analog readout.

developed in collaboration between the IReS and DAPNIA[6] groups. The MIMOSA VI prototype did not allow testing the full functionality of the complete readout chain due to large pixel-to-pixel dispersions. This was the first attempt to build a MAPS sensor with digital binary readout.

The second prototype with a similar architecture, called MIMOSA VIII, featured in-pixel signal amplification and signal discrimination implemented at the column level. Detailed description of the design aspects and test results is not in the scope of this work (for details see [90]) and only information relevant for general discussion of MAPS architectures will be presented. The sensor was designed aiming at the architecture suitable for the ILC vertex detector. The architecture of this prototype is schematically presented in Figure 4.15. The test chip was designed in the 0.25 TSMC technology on a substrate with a thin epitaxial layer ($\sim$ 8 μm). The chip consists of four sub-arrays of 32×32 pixels, with a pitch of 25 μm. All columns are readout in parallel. Eight of them have analog outputs and the other 24 end with signal discriminators and six 6-to-1 multiplexers for digital readout on 4 outputs [91, 92]. One sub-array features self-biased structures AC coupled to the in-pixel amplifier. The other sub-arrays are based on reset-diodes of different dimensions ($1.2 \times 1.2, 1.7 \times 1.7, 2.4 \times 2.4$ μm^2)

The sequencer managing the array readout has the same architecture as the one that was implemented in the MIMOSA VII prototype (Chapter 5). The control pattern is programmed by a custom serial interface and controls access to and operation of all pixels. The architecture of a single pixel is presented in Figure 4.16(a). The pixel contains a charge sensing element AC or DC coupled to the preamplifying stage based on a common-source configuration, providing signal gain of about 4, and a circuit (one reset switch and one serial capacitor) performing double-sampling. The double sampling circuitry is based on a clamping capacitor. Full readout cycle begins with the reset of voltages on the charge collecting diode and the input of the source-

[6]CEA Saclay, DAPNIA, 91191, Gif-sur-Yvette Cedex, France

follower. The resulting voltage is stored on the in-pixel capacitor. After the integration time, at the next access to the pixel, the new voltage is stored on the same capacitance. Since the second node of the capacitor is floating, the voltage at the input of the source follower corresponds to the differences of voltages in both samples. The pixel is readout twice on a single access: shortly after the second sample is stored and immediately after the reset phase. The second correlated double sampling is performed at the column level and removes process mismatches between source followers in different pixels. The samples acquired during reset of the clamping circuitry and during signal readout are subtracted. The result is a signal free of the offset of the source-follower stage. The stimuli for pixel operation are presented in Figure 4.16(b).

The sensor architecture uses CDS technique twice. The first operation, performed in the pixel, eliminates reset noise. The second operation, at the bottom of each column, minimizes pixel-to-pixel dispersions caused by mismatches of the threshold voltage of the in-pixel source follower. The operation can be explained as follows:

1. After resetting the internal node, the voltage across the capacitance is $V_{CAP} = V_{REF} - V_{S1}$ The V_{REF} voltage is also sampled at the bottom of the column.

2. After the integration time, the voltage across the capacitance does not change and the voltage equation can be written as $V_{OUT} - V_{S2} = V_{CAP}$, which leads to the output voltage $V_{OUT} = V_{REF} + V_{S2} - V_{S1}$. The output voltage is the second sample for the column level CDS.

3. Performing the column level CDS results in signal equal to the difference of the two registered in-pixel samples: $V_{signal} = V_{S2} - V_{S1}$

Twenty four columns of pixels are equipped with comparators. All pixels in one column share one comparator. The offset compensating comparator is based on an auto-zeroed amplifying stage and a dynamic latch, as shown in Figure 4.16(a). The discriminators subtract voltage from the READ phase from the voltage in the CALIB phase for each pixel, and compare it with the reference differential voltage $V_{ref} = V_{R2} - V_{R1}$ that sets the threshold level.

The operation of the autozero technique is simple. During the first read phase (READ), which is the auto-calibration phase of the comparator, the output of the second stage amplifier is shorted to $V2$ and the plates of the capacitors C are connected to $A_1((V_{READ} - VR1) - V_{off1})$. Basic operational amplifier equations show that $V_{in} = V2$ and $V_{out} = V3 = -A_2(V_{in} - V_{off2})$ for the open-loop configuration, where V_{off2} is the offset of the second amplifier stage. Therefore, in the auto-calibration phase $V_2 = \frac{A_2}{1+A_2} V_{off2}$. The voltage on the second plates of the capacitors C is equal $A_1((V_{READ} - VR1) - V_{off1})$. The voltage across the capacitors is stored, and during the operation phase of the comparator (CALIB), it is inserted into the signal path. The equation for the readout phase (corresponding to CALIB) can be written as:

$$\begin{aligned} V_3 = -A_2 \left(-A_1 \left(V_{CALIB} - VR2 - V_{off1}\right) - V_{off2} + \right. \\ \left. + \left(\frac{A_2}{1+A_2} V_{off2} + A_1 \left(V_{READ} - VR1 - V_{off1}\right) \right) \right) \end{aligned} \tag{4.12}$$

$A_1 V_{off1}$ is directly subtracted while V_{off2} is multiplied by $1/(1+A_2)$. For large A_2, the influence of the offset is reduced. If the offset can be neglected, Equation 4.12 simplifies to:

$$V_3 = A_2 A_1 \left((V_{CALIB} - V_{READ}) - (VR2 - VR1)\right) \tag{4.13}$$

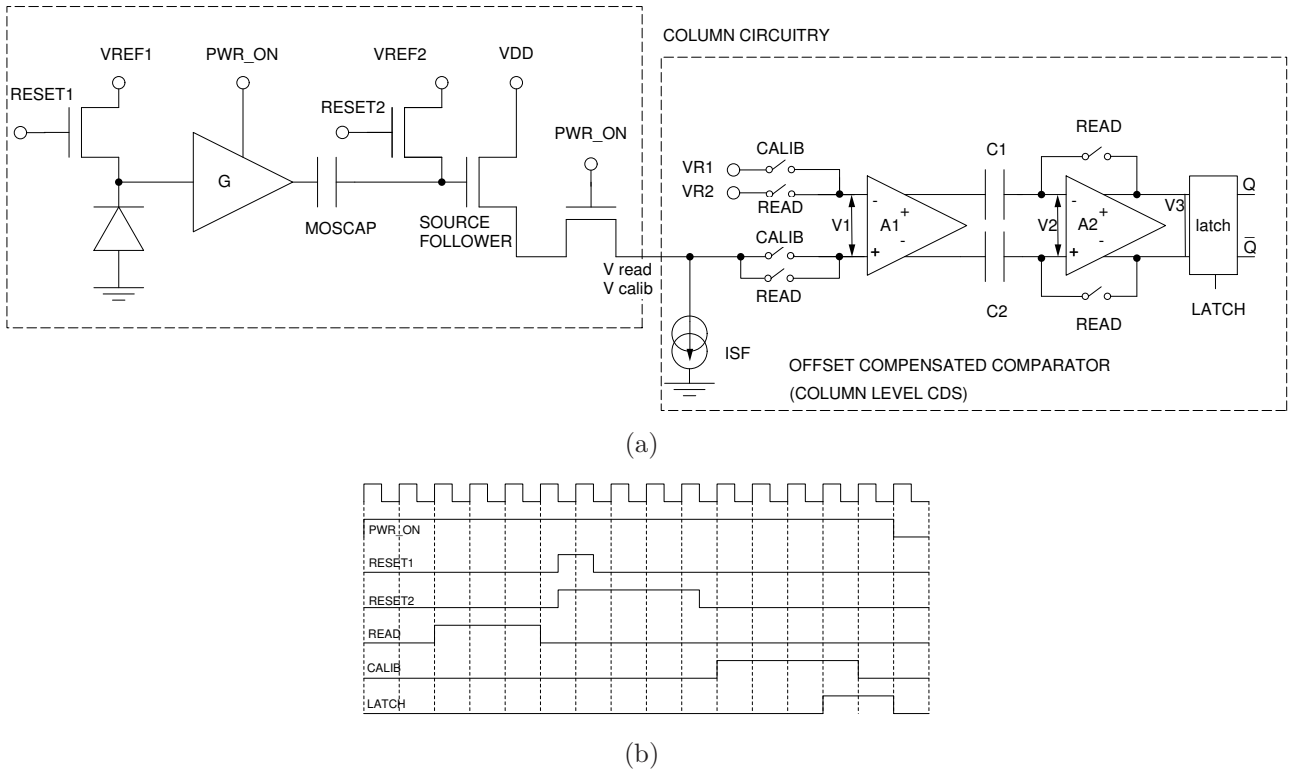
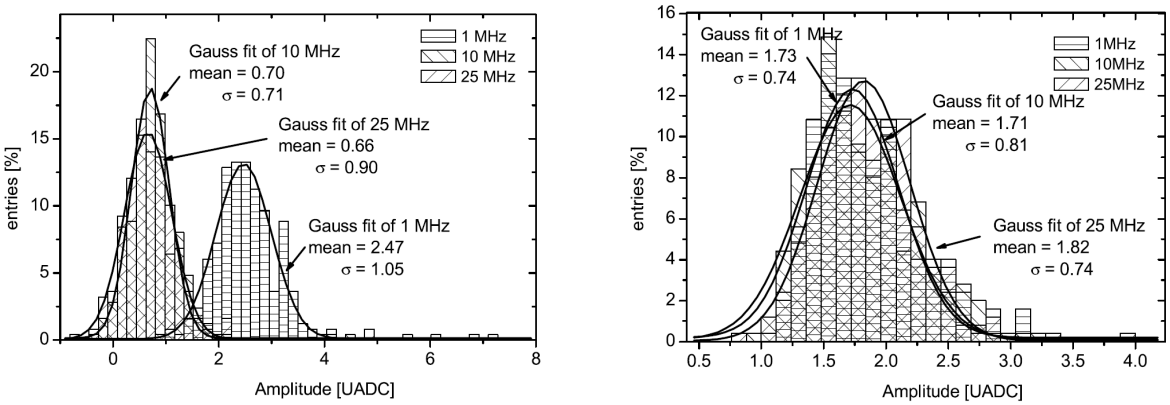


Figure 4.16: Schematic diagram of the pixel and column circuitry in MIMOSA VIII, (a). The column readout is based on an offset compensated comparator. The timing diagram of stimuli, (b), illustrates the operating sequence of the circuit.

In summary, during the readout phase the amplified input signal is compared to the threshold level, the mismatches are subtracted, and the resulting logic state is latched.

Part of the work within this thesis was the study of performance of the two-level CDS architecture. Laboratory tests of the prototype, performed with the analog set of outputs, reveal that the distribution of pixel-to-pixel dispersions at the sensor level is strongly suppressed. The pixel-to-pixel dispersion is below the level of temporal noise. The result is illustrated in Figure 4.17. Pixel-to-pixel dispersion is presented as a distribution of average signal levels for all pixels. Gaussian fits to the distributions reveal mean values of 0.66, 0.70 and 2.47 ADC counts for 25, 10, and 1 MHz main clock frequency, respectively. One ADC count corresponds to 0.5 mV. The shift of the mean value at the slowest clock frequency (longest integration time) is caused by the leakage current affecting pedestals. The dispersions expressed as standard deviation are below 1 ADC unit (0.90, 0.71, 1.05 for 25, 10, and 1 MHz, respectively). The histogram of temporal noise reflects the distribution of the mean noise value for all pixels. The measured mean value is lower than 2 ADC units and reaches 1.82, 1.71, and 1.73 ADC units for 25, 10, and 1 MHz, respectively.

Tests of the digital part of the circuit show good performance of the discriminators. Threshold variation is at the level of 0.3 mVrms and the temporal noise at 1 mVrms, measured at 40 MHz main clock frequency [93]. Beam tests performed at DESY with a 5 GeV electron beam and



(a) (b)

Figure 4.17: Distribution of the pixel-to-pixel dispersions, (a), and the rms values of the temporal noise, (b), measured in MIMOSA VIII for the full readout sequence with on-pixel CDS and column level offset subtraction at different readout frequencies.

at the main clock frequency of 40 MHz, show that a good detection efficiency (approximately 98%) can be reached by both the analog and digital part of the sensor. For high detection efficiency (99%) low discriminator threshold (2.5 mV) is required. This leads to the fake hit rate (false hits resulting from high temporal noise) at the level of 10^{-3} hits/pixel/frame. For higher thresholds (above 5 mV) the fake hit rate decreases below 5×10^{-5}, but the detection efficiency is suppressed below 90% [93].

This prototype was the first fully successful implementation of on-chip signal discrimination in the MAPS development at IPHC. The importance of the obtained results can not be overestimated. The architecture paves the way for future developments of fast sensors for imaging and tracking of ionizing particles. Current results do not satisfy requirements for vertex detectors, where high detection efficiency (above 99%) and low fake rates (below 10^{-5} are required. Improvement on the signal-to-noise ratio is necessary. The enhancement can be obtained by switching to technologies with thicker epitaxial layers that would collect more charge, or, to some extent, by providing higher in-pixel signal amplification.

4.4 Overview of different pixel architectures

Continuous development of MAPS in the MIMOSA family is driven mainly by possible applications in future high energy physics experiments. Different sensor architectures at the pixel level are considered depending on the requirements for a given application.

MAPS are proposed for the vertex detector upgrade at the STAR experiment at RHIC scheduled for 2009. The architecture proposed is based on a simple two-transistor pixel circuitry and the selfbiased structure as illustrated in Figure 4.18(a). It is suited for long integration time on the order of 4 ms, room-temperature operation and minimum power dissipation (below 100 mW/cm^2) in agreement with the STAR requirements.

Implementing an in-pixel amplifier allows new sensor architectures to take advantage of the

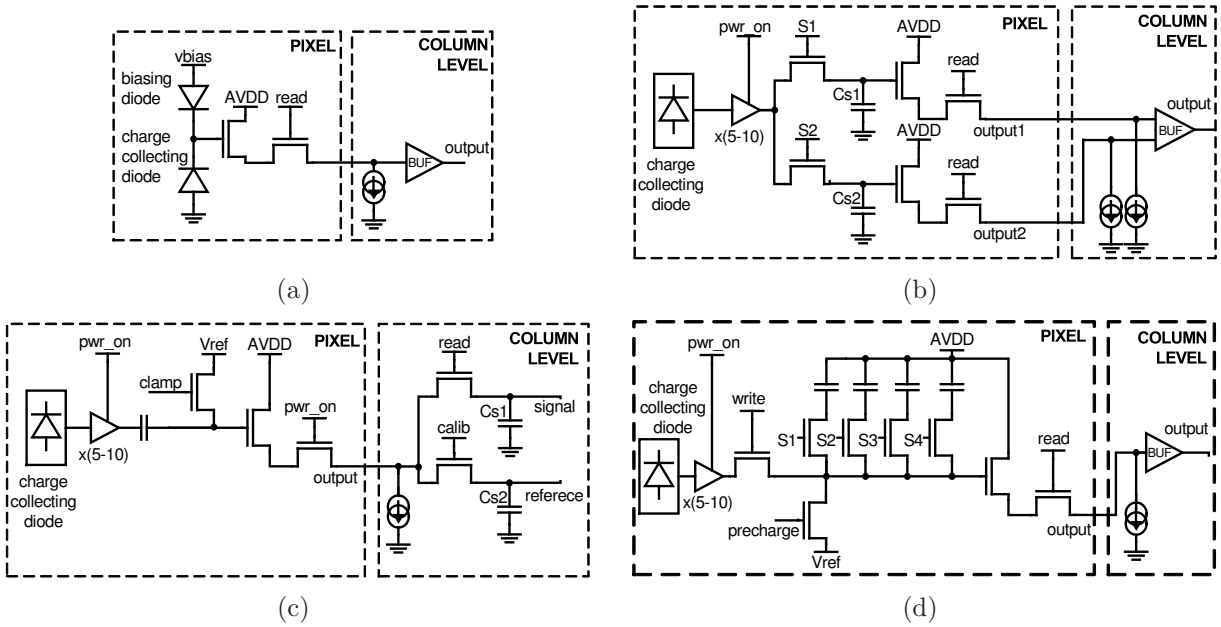


Figure 4.18: Architectures of MAPS optimized for different applications: proposed for the first upgrade of the STAR vertex detector (a), featuring in-pixel CDS with a possibility of decoupling integration and readout times (b), featuring in-pixel CDS for on-chip data discrimination (c), and capable of multiple-sample storage at the pixel level (d).

increased signal level for storing or processing purposes. Three examples of such structures, well suited for detectors with short integration times, are presented next.

Most of MAPS prototypes work in a rolling-shutter mode and their readout times are equal to integration times. A pixel architecture that allows for the adjustment of the integration time independently of the full frame readout time has been studied in MIMOSA IX and MIMOSA XI prototypes (Figure 4.18(b)). Decoupling the integration time from the readout sequence is possible due to memories implemented in the pixel. The readout is not continuous as in the previous scheme, but follows only a trigger decision. The possibility of decoupling the integration time from the readout time was proposed to solve the problem of leakage current increase after irradiation of the detector. If the leakage current, in the given integration time, increases too much and induces an excessive noise, the integration time could be shortened without affecting the readout time.

In modern detector system the requirements for the readout speed are very exigent. To fulfill the requirements, a rudimentary on-chip data sparsification is required to reduce the amount of data transferred to an acquisition system. For these fastest systems, such as inner layers of the ILC or the ultimate sensor for the STAR at RHIC II luminosity, a circuit allowing fast frame scans together with on the fly hit selection and sparsification performed on the detector is required. The MIMOSA VIII prototype circuit is based on a double readout and reset noise cancelation that reduces FPN below temporal noise (Figure 4.18(c)). In addition, the prototype successfully performs on-chip signal discrimination. The sensor's satisfactory performance makes its architecture the most promising one for the future developments of MAPS with fast readout.

An extension of the architectures discussed is a pixel structure that contains several in-pixel memory cells. The design is suitable for fast storing of several samples at the pixel level for speeds that would exceed the possibilities of on-the-fly readout. The use of this architecture will be limited by the large pixel size that limits the achievable resolution. Such a pixel is schematically presented in Figure 4.18(d). It is one of the options considered for outer layers of the ILC vertex detector based on MAPS [88]. The resolution requirements for the outer layers are not as strict as for the inner layers of the vertex detector. At the same time, storing multiple samples for later readout is compatible with the ILC beam structure.

4.5 Summary of sensors operated in voltage mode

Different pixel architectures that are presented in this chapter provide interesting solutions for designing application specific devices. The discussed advantages of the self-biased diode over the classical diode with a reset transistor make it a well suited solution for the STAR vertex detector upgrade. In addition, the study of a few simple in-pixel amplifiers indicates that simple architectures combined with in-pixel CDS circuitry can provide satisfactory results for simple on-chip analog data processing. Two approaches for connecting the charge collecting diode and an in-pixel amplifier were studied. Results show that the improvement in charge collection obtained with the layout optimized AC coupling (on the order of a few percent) does not increase the signal-to-noise ratio. Signal becomes limited by the parasitic capacitive voltage divider that is associated with the proposed structure.

The importance of efficient removal of fixed pattern noise is undeniable. The solution for removing FPN that was implemented in the MIMOSA VIII prototype proves to be very efficient in reducing FPN below temporal noise and guides towards future development. This architecture is especially interesting for the ultimate sensor for the STAR vertex detector that will need to operate with integration times at the level of 200 μs, or lower, to deal with the increased luminosity of RHIC II. To achieve very high detection efficiency of more than 90% and, at the same time, low fake-hit rate, it is necessary to increase signal-to-noise ratio at the discriminator level. The improvement could be achieved through a sensor implementation in a technology with a thicker epitaxial layer that should allow collecting more charge. Some room for improvement exists at the amplifier stage, where higher gain could be achieved by using, for example, the structure presented in Chapter 4.2.5.

Chapter 5

MAPS with current mode signal processing

MAPS prototypes operated in voltage mode studied in the previous chapter present the most widely adapted approach to sensor development. Complementary to these sensors, there has been significant advancement in development of sensors operated in current mode. This chapter presents the study of a MAPS prototype with charge-to-current conversion and in-pixel current signal processing.

The first results, obtained by the LEPSI/IReS group with a simple, single pixel PhotoFET (introduced in section 3.3.1) test structure were encouraging. Tests with an ^{55}Fe source and a pixel signal sampled in about 1 ms intervals showed sensitivity about 330 pA/e^-, at a constant DC bias current of approximately 5 μA. The measured noise was close to five electrons of ENC at room temperature. The direct current output of the PhotoFET cell was connected for the continuous conversion to the resistive feedback transimpedance amplifier built with a discrete operational amplifier. Good noise performance was achieved due to the absence of any switching activity, high conversion gain, and a narrow frequency bandwidth over a dozen of MHz. The implementation of a full matrix was the challenging next step. The design of the MIMOSA VII (MVII) aimed at validation of the adequacy of an array of PhotoFET cells as a high sensitivity device in tracking of charged particles. A summary of the following sections can be found in [94].

5.1 Chip architecture

The fabrication process, in which MVII was implemented, is a 0.35 μm commercial CMOS process. The results obtained previously on a single pixel structure from MIMOSA IV needed to be verified with a full matrix design to test the robustness of the approach [95]. The array structure in MVII allowed testing the detector's performance under the presence of parasitic effects, such as pixel-to-pixel dispersions of currents, operation of the cell with a switched bias current, sensitivity to biasing currents, distortions from coupling to digital lines driving a pixel, charge injection from the in-pixel transistor switches, etc. A simplified diagram of the MVII chip is sketched in Figure 5.1.

The device contains an array of 18×64 pixels, where the first and the last column are dummy columns not connected to the readout circuitry. All 16 columns have their own buffering blocks

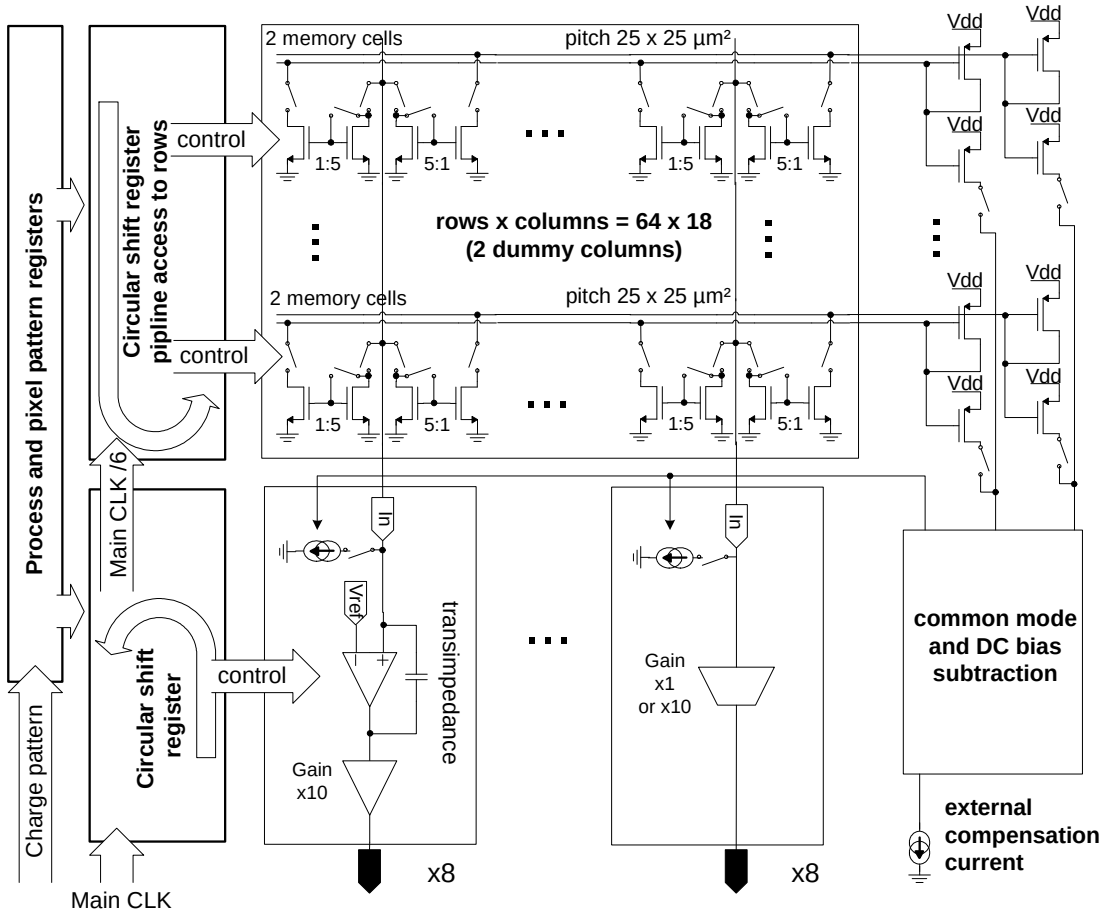


Figure 5.1: Block diagram of the MIMOSA VII chip. Each PhotoFET-based pixel features two current-mode memories for storing two consecutive current samples. Eight pixel columns are read out in current mode and the signal from the other eight columns is converted to voltage in the on-chip integrated transimpedance amplifiers.

and can be read out in parallel. The integrated digital sequencer, programmable from outside with the custom serial port interface, controls the operation of the chip. The sequencer is shown on the left side in Figure 5.1 It is built of a set of circular shift registers, propagating a programmed pattern. One part of the sequencer asserts series of signals needed to perform sampling operations in the pixel and selecting individual cells for readout. The second part of the sequencer orchestrates the column level readout circuitry. The synchronization with access to rows of pixels is provided. In the case of a discrete implementation of the readout circuitry, presented later in this chapter, the synchronization was achieved by reproducing the required signals from MVII in a CPLD chip. One, complete readout of the chip, starting at the first row and finishing at the last one, is referred to as a frame. The sensor is read out in a continuous way. After reaching the last row, an immediate passage to the first row of the matrix takes place. The currents from the first eight columns of the array are processed by the block of eight current integrating transimpedance amplifiers, described in Chapter 5.4.4.

The current signals from pixels are converted to voltages and subtracted. The resulting signals are read out on eight dedicated pads. The part of the readout chain, associated with the

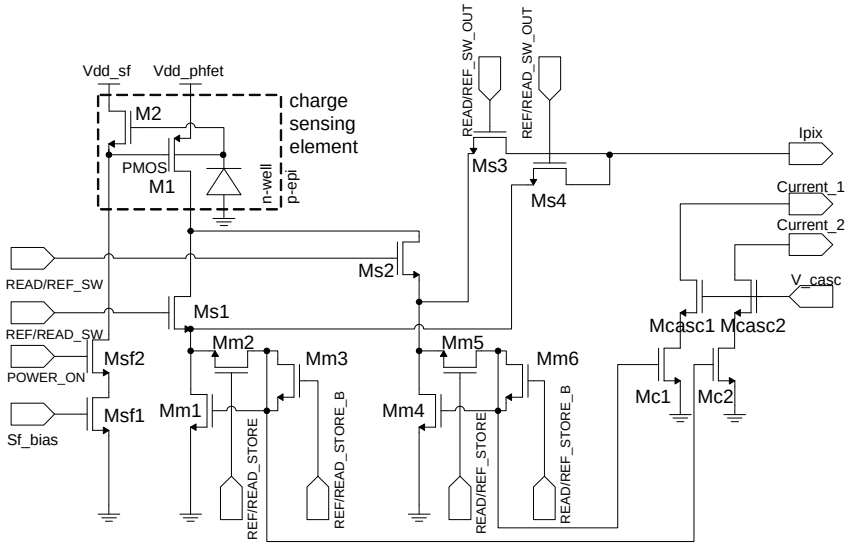


Figure 5.2: Schematic diagram of the pixel from the MIMOSA VII chip. The charge sensing element is the PhotoFET cell. The pixel contains two current-mode memories that store two consecutive signal samples for performing on-chip CDS.

first eight columns, embodies a novel implementation of the on-chip CDS processing. Current integrating transimpedance amplifiers are very sensitive to the DC component of the integrated current signal. The design of amplifiers was driven by maximization of the gain, assuming that the average value of current for all pixels can be subtracted at the input of the amplifier. The signal swing should allow sufficient room for pixel-to-pixel dispersions of the DC component. Too large dispersions of the DC current component may imperil the transimpedance amplifiers, leading to their early saturation. The magnitude of dispersions could not be estimated during the design. Thus, the second eight columns were designed as a backup with the direct current readout. This second set of eight columns is not subjected to any processing on the chip, giving a direct access to the current signals. The current from addressed pixels can be read out in a direct mode or it can be amplified by a factor of ten with a block of eight current amplifiers, as it is shown in the bottom part of Figure 5.1 The operation of the chip requires clock signal with the frequency of up to 100 MHz. The sequence, used for running the transimpedance amplifiers, is shifted with the main clock. The pattern, sent to rows, is propagated in shift registers with clocks derived from the main clock in division by 10 and 6 in order to reduce the switching activity in the chip.

Architecture of the pixel, containing two memory cells, is presented in Figure 5.2. The charge-sensing element, PhotoFET, is built of the n-well/p-epi charge collecting diode and transistors M1 (PMOS) and M2 (NMOS). The collected charge alters the threshold voltage of M1 through the drop of the n-well potential and hence modulates the channel current of the transistor M1. The sensitivity is increased by applying the n-well potential to the gate of M1 via the source follower transistor M2 [76]. The current of the PhotoFET cell contains two components; the first one is a DC component, which is of the order of several μA, and the second component is a signal, left as a footprint of an impinging particle, which in turn is of the order of tens of nA. The DC component does not convey any useful information, and it has to be subtracted in

order to avoid saturation of transimpedance amplifiers at the column ends. The on-chip circuitry allows subtracting the DC current component defined by an external source. The source region of the transistor M1 is an anode of the forward biased diode in the CRB scheme (continuous reverse biasing). Operation of the charge-sensing element in current mode is very convenient for implementation of a current mode memory cells in each pixel. The number of memory cells can be more than two. The limiting factor is constraint on the pixel size. However, only two memory cells are required for an efficient extraction of signals due to particles by subtracting two samples acquired in consecutive moments in time.

The presented design features two current mode memory cells correspondingly built with transistors Mm1-3 (Mem1) and Mm4-6 (Mem2), as it is shown in Figure 5.2. The gate-to-source capacitances of transistors Mm1 and Mm4 store voltages corresponding to the sampled currents. The choice of the column parallel readout is dictated by the need of providing fast, dead-time-free frame scans. In this scenario, whole rows of pixels are selected at once in the continuous, wrapped around readout of the matrix. The access to an individual pixel is divided into two phases, i.e., the write phase and the read phase. The access to rows is pipelined. In the first step, the actual current value is sampled on one of the two memory cells. The second memory stores always the sample from the previous access. During the second step, both current samples are sent in sequence on the Ipix terminal for readout by activating switches Ms3 and Ms4. The operation in pipeline means that two consecutive rows of pixels are being processed simultaneously. The difference is that while the data sampling is performed in the leading row, the current samples are being readout from the previous row. Storing signal samples in memory cells is accomplished in turns. For the sake of distinction, a notion of even and odd frames can be introduced. Samples from every even frame are stored in Mem1 while samples from every odd frame in Mem2. During the readout phase, both current samples are read-out successively. The reading order of the stored samples is alternated every frame. For even frames the contents of Mem1 is readout first and followed by the contents from Mem2. For odd frames, the order is reversed. This approach assures subtraction of the reference level from the actual one in the column-end circuitry. This complication of the system provides one desirable polarity of the electrical signal as a response to the particle impact.

The matrix of pixels is divided in three sub-blocks. The division is made horizontally. The first 32 rows are built of pixels with 100 fF capacitances in memory cells, and with charge injection compensation switches. The switches are shown in Figure 5.2 as transistors Mm3 and Mm6. Next 16 rows contain pixels with the same 100 fF capacitance value but the switches for charge injection compensation are not connected to the driving lines. The related transistors are still present in the layout, but they are only dummy switches. Pixels in the last 16 rows contain 50 fF storing capacitors with active switches for compensation of the charge injection. The pixel size is 25×25 μm^2. The transistors Mc1 and Mc2 are a part of the system, distributed to each pixel, aiming at derivation of the mean current for each row for subtraction as a pedestal at each column end.

5.2 Test bench

Three different readout schemes for the tests of the MVII chip were developed and tested in order to extract different information about the chip. First, the direct current outputs were

examined using off-chip transimpedance amplifiers with resistive feedback. The functioning of PhotoFET cells in an array structure was tested by performing appropriate software analysis on the recorded raw data. Then, after the discovery that DC current components show a significant pixel-to-pixel dispersions, two external implementations of subtracting circuits, based on the same principle as the integrated in-chip amplifier but having less gain, were used to process the signal from direct current output columns. Two alternative circuit topologies were examined. Both were performing the analog operation on the data in synchronization to the access to the pixel rows. At the last step, the high gain CDS amplifier implemented in the chip was tested. More details on the system setup are given in Appendix C

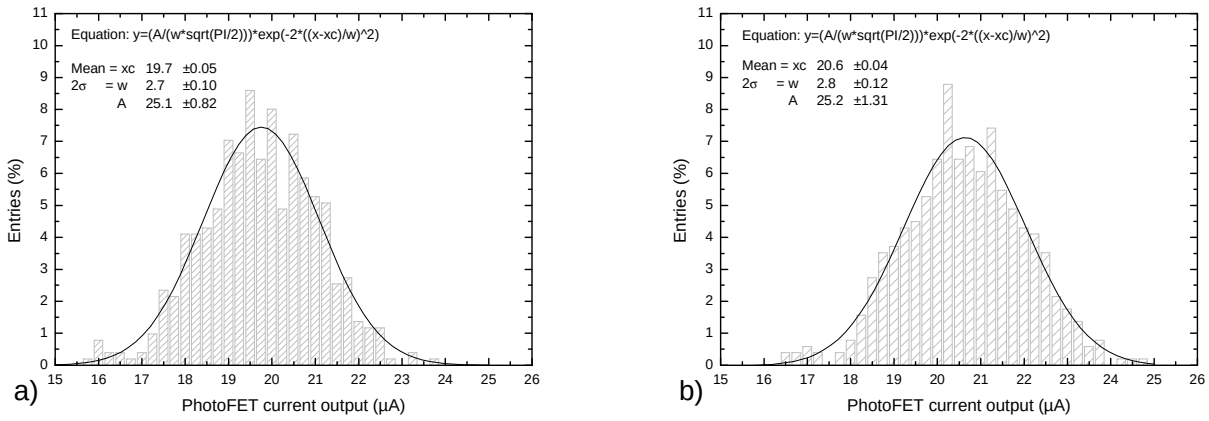
5.3 PhotoFET measurement results

5.3.1 Pixel characterization

The tests performed on the direct current outputs, allowed insight into the operation of individual PhotoFET cells. The setting of references and power supplies according to prior simulations and measurements performed on a single cell [95] were used to start the tests. The power supply of the PhotoFET (vdd_phfet) was set to 3.3 V and the DC bias current of the PhotoFET source follower was about 40 nA. These conditions assured a few μA current in the PhotoFET cell and a low power consumption. Later analysis showed, however, that better noise performance could be achieved at higher source follower currents.

The potential on the n-well/p-sub charge collecting diode is set automatically to the level of the PhotoFET power supply reduced by the voltage drop across the bulk-to-source junction biased in forward direction by the leakage current of the charge collecting diode. The potential of the virtually floating n-well implant was almost equal to the power supply. The value of the subtracted DC component of the PhotoFET output current was set to about 20 μA. The main clock with a frequency of 10 MHz was used initially to cadence the chip. The clock frequency defined a sampling period of 192 μs for the current from the PhotoFET cell. There is no reset system integrated in the pixel, thus this period is equal to the signal integration time.

Proximity board with a bonded chip was placed in a light-tight box at a constant, controlled temperature inside. Most of the tests were performed at room temperature of about 20°C and an internal current gain of 10 was used. Taking into account the on-chip gain, the gain of the transimpedance amplifier of 13 kΩ and the gain of the differential line driver of about 1.5, the total transimpedance gain of the readout chain was 200 kΩ. The raw data stored to the disk were analyzed with dedicated software. The software analysis included the calculation of average signals (pedestals) and calculation of noise, individually for each pixel. The next step was the hit finding analysis that was sensitive to signals above a set threshold. The analysis was possible for both samples stored in a pixel and read out separately and on their difference calculated in software. The latter operation is equivalent to the CDS processing. Hits, within the time since the last readout, could be extracted and the amount of charge released in the active detector volume due to their impact could be measured.



(a) (b)

Figure 5.3: Distribution of currents from PhotoFET cells of the entire matrix for the first (a) and second (b) memory cell.

5.3.2 Measurement of fixed pattern noise

FPN has the same spatial arrangement and statistics from one image sample to another. Two different components fall under this noise category, i.e., dark signal nonuniformity (DSN), including deterministic shifts of signal due to mismatches of components, and charge conversion nonuniformity (CCN).

In the particle detection system, DSN of an active pixel matrix can be much higher than magnitudes of signal expected from a particle impact. This type of noise is relatively easy to filter out. Filtering can be achieved in different ways, e.g. by estimating mean values for each pixel from a number of images acquired unexposed, and subtracting this mean from the sample image. The construction of an intelligent particle detector aims at a system, which would allow real-time extraction of particle impact events. For the compactness and efficiency of the design, it is desired to accomplish the whole processing on the chip. Implementation of circuit blocks serving whole groups of pixels and making decision on occurrence of an event based on the signal height requires equalizing output levels from pixels. Storing the whole image of mean values on the detector is questionable, because it would require an additional memory introducing considerable dead area of the detector. The current work addresses the elimination of DSN by subtracting samples distant in time and stored directly in each pixel. On the other hand, CCN is less detrimental in practice for a particle-tracking detector as long as it is limited to a few percent. In the case when the accurate amplitude of the measured signal is requested, the appropriate correction can be applied off-line on the sparsified data acquired by DAQ using a gain-mapping table.

The distributions of currents sank by pixels are shown in Figure 5.3. They were measured for the sub-matrix built with 100 fF storage capacitors. This figure shows mean values of currents for all first and all second memory cells calculated for 4500 frames. The constant component, subtracted in the measurements, is included. The assumption on a Gaussian form of DSN is not

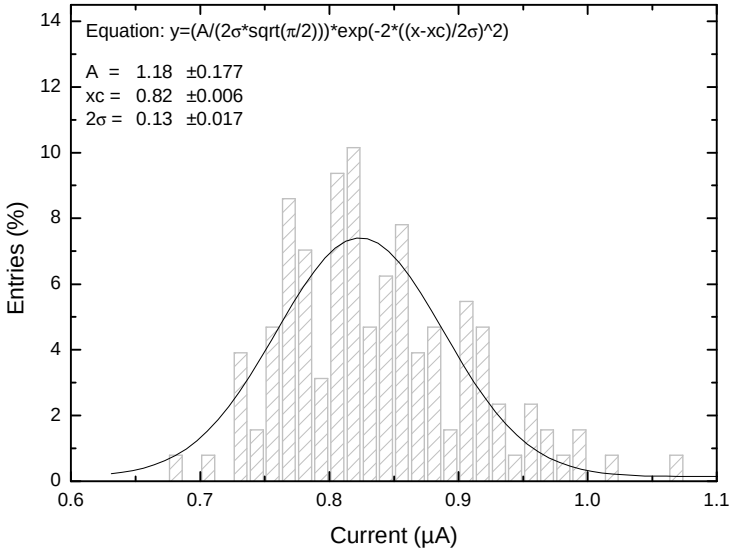


Figure 5.4: Distribution of the subtracted samples for the sub-matrix with pixels built with a 100 fF storage capacitor.

always valid. The form of the distribution can be asymmetric, especially in detectors where DSN is dominated by a spread of leakage currents of the charge collecting diodes [96]. The symmetrical form of distributions in Figure 5.3, suggest that the dominant effect is a dispersions of transistor parameters, such as transistor threshold voltage, geometrical dimensions and transconductance coefficients. The width of the PhotoFET current distributions, calculated with the Gaussian fit, is about 1.4 μA and is equal for both memory cells. The mean values are however different by about 1 μA. In an ideal system, current samples from both capacitors should be the same in absence of the radiation source. The results of the subtraction of the current samples from the first and the second memory cell for the same pixel are shown in Figure 5.4. The width of the distribution is 65 nA. This shows more than 20 times reduction of DSN after the CDS processing. A leakage current of the charge collecting diode introduces a voltage drop across the source-bulk junction of the PMOS transistor in the PhotoFET cell. The spread of the leakage current contributed to the total current dispersions of the PhotoFET cell, shown in Figure 5.3.

The subtraction of two samples, stored in pixel, resulted in an automatic elimination of the leakage current component from DSN. However, a significant constant shift of the mean value equal to about 0.8 μA is still observed. The origin of the shift may be in layout asymmetries in the design of both memory cells in the pixel design, or in a feedthrough of switching signals from control lines, passing nearby to the memory cells. The dispersions of samples after subtraction are low. However, the significant shift of the mean value from the expected zero position was identified as a substantial problem for the operation of the current integrating transimpedance amplifiers. The shift of the mean value forces current integration with a substantial DC component that cannot be subtracted as one common factor. In classical 3T pixels, practically the only source of dispersions of the charge to output signal conversion gain is the spread of junction and

interconnection capacitances seen at the charge collection node. The dispersion of the conversion gain does not exceed a few percent [95] in most cases. An additional source of dispersions is the conversion of the voltage change on the diode to the increment of the output current in a current mode pixel. The absolute value of CCN can be expressed by:

$$\Delta CQI = CQV \times g_{mt} \left(\frac{\Delta g_{mt}}{g_{mt}} + \frac{\Delta CQV}{CQV} \right) \tag{5.1}$$

where CQI is the charge-to-current conversion gain of the PhotoFET cell, g_{mt} is the total small signal transconductance of the PhotoFET cell, referred to the bulk-source voltage of the PMOS transistor M1, and CVF is reciprocal of the capacitance seen at the node where charge is collected. The g_{mt} component is given by:

$$g_{mt} = g_{mbM1} + g_{mM1} \times \frac{g_{mM2}}{g_{mM2} + g_{mbM2}} = g_{mM1} \times \frac{n^2 - n + 1}{n} \tag{5.2}$$

where g_{mbM1} and g_{mM1} are small signal transconductance parameters of the transistor M1 and n is the subthreshold slope factor, assumed here to be equal for a PMOS and NMOS transistor. The drain current of a MOS transistor is a quadratic, steeply raising, function of its gate-source voltage. It can be concluded that the main source of current dispersions of the PhotoFET cell are pixel-to-pixel variations of the source-gate voltage of the source follower transistor M2 and the threshold voltage of the PMOS transistor M1. Assuming the operation of M1 in a strong inversion region, the relative dispersion of the transconductance parameter is easily calculated by:

$$\frac{\Delta g_{mt}}{g_{mt}} = \frac{\Delta I_{M1}}{2 I_{M1}} \tag{5.3}$$

Substituting numerical values extracted from Figure 5.3 to Equation 5.3 and taking n=1.2, the relative variation of the transconductance component is equal to 3.5%. One of the observations, made during the tests, was a high value of the DC component compensation current for the PhotoFET cell. The PhotoFET current was estimated to a few μA only in the simulation of the design for bias conditions as listed earlier. The use of a typical bias, with a floating substrate, for the transistor M1 raised doubts about validity of its SPICE modeling. The measurements showed a significant increase of the sampled current of the PhotoFET. The discrepancy between measurements and simulation estimations might result from an incomplete representation of the switching effects of the bias current. The bulk-to-source voltage of the transistor M1 barely achieves a few tens of mV under constant bias conditions. Incorporation of the switching effect results in a capacitive induction of the n-well potential drop. The change of the n-well potential V_{n-well}, when bias in the pixel is switched on, is estimated by:

$$\Delta V_{n-well} = \frac{C_{ox} \frac{W_{M1}}{L_{M1}} \times \Delta V_{sM2}}{C_{n-well}} + \frac{C_{bdM1} \times \Delta V_{dM1}}{C_{n-well}} \tag{5.4}$$

where Cox is the oxide capacitance per area unit of a MOS transistor, W_{M1} and L_{M1} are geometrical dimensions of the transistor M1, V_{sM2} and V_{dM1} are voltage steps on the source of the transistor M2 and the drain of the transistor M1, respectively, at the moment of switching on the pixel. C_{bdM1} and C_{n-well} are bulk-to-source junction capacitance of the transistor M1 and the

total n-well region to ground capacitance, respectively. Equation 5.4 includes two dominant contributions only. Substituting numerical values for quantities in Equation 5.4 (C_{ox} = 4.6 fF/ μm^2, W_{M1}=0.8 μm, L_{M1}=0.4 μm, C_{n-well}=10 fF and C_{bdM1}=1.5 fF), the step of the n-well potential can be estimated to be in the range from 300 mV to 500 mV.

The voltages V_{sM2} and V_{dM1} were calculated assuming that the considered points drift to the power supply rail when the bias in the pixel is switched off. This significant increase of the bulk-to-source voltage was identified as a source of boosting of the PhotoFET current during sampling.

5.3.3 Measurement of temporal noise

An oscilloscope screenshot, showing current samples from six pixels in one column after conversion to voltage is given in Figure 5.5. The indicators in this figure mark off boundaries of the access to individual pixels and to the current memory cells inside pixels. The first three pixels in Figure 5.5 are the last pixels from the frame, numbered n, and the next three are the first pixels from the frame n+1. The step, present on the signal when moving from the first to the second memory cell in each pixel, reflects readout of two slightly shifted current samples from in pixel memory cells. The levels, corresponding to the cells Mem1 and Mem2, are marked with (-1-) and (-2-), respectively. The distribution of signal samples obtained for one selected typical pixel built with the storing capacitance of 100 fF is presented in Figure 5.6. The histograms were built for 4500 acquired frames. Two histogram groups, reflecting a systematic shift between samples from both memory cells, are clearly visible. The dispersion of samples around mean values in both peaks is random and it corresponds to the total temporal noise associated with the pixel readout. Gaussian fits to both histogram groups yield mean values of 19.5 μA and 20.4 μA, respectively, and standard variation of 45 nA.

The artefact of a systematic shift between samples can be explained by an unequal coupling

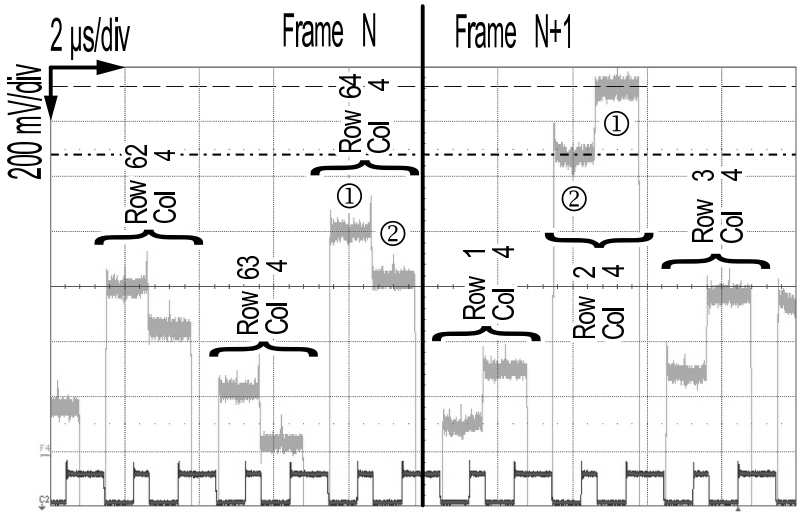


Figure 5.5: Oscilloscope trace of a signal from six, consecutively read out PhotoFET pixels. The figure highlights the consecutive readout of the two in-pixel memories, (1) and (2), and the alternating readout of memory cells in odd and even frames.

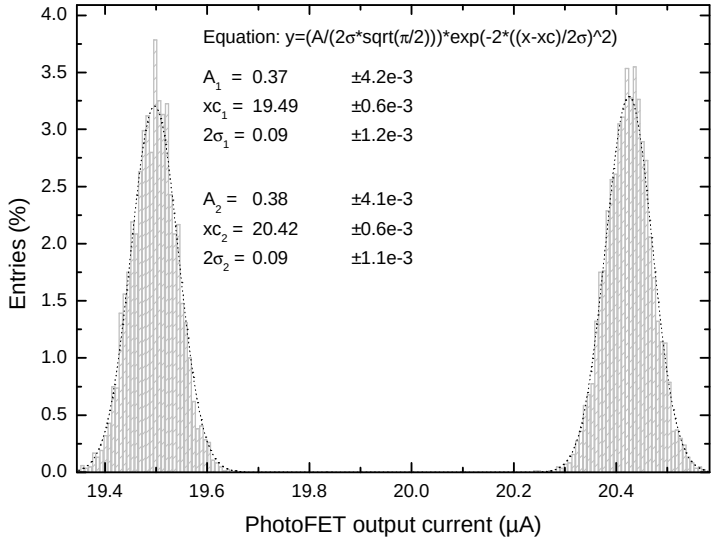


Figure 5.6: Signal distribution from a single PhotoFET cell comprising a storage capacitor of 100 fF.

of digital signals to the plates of capacitors in two memory cells or to the floating node of n-well in the PMOS transistor M1. In the case of coupling to memory cells, the step voltage, induced on the capacitance in a memory cell due to a capacitive division of the digital step, results in the readout of a current sample different from the stored one. In the coupling to the floating n-well area, the voltage step, resulting from a capacitive division of the step voltage between the coupling capacitance and the n-well capacitance to ground, is converted to current and sampled as it was a regular input signal. A very high sensitivity of the charge-sensing element may results in a large change of the transistor M1 current.

A careful symmetrical layout minimizing, or at least equalizing, the coupling of the digital signals to the sensitive parts of the pixels was one of the goals for the design. Both in-pixel memory cells required separate control signals, asserted on separated lines. The coupling between control lines and capacitances in memory cells was strongly reduced by screening the capacitances with a metal1 plane connected to ground. Parasitic, interlayer, capacitance components were extracted using the DIVA tool from Cadence in the design process of the pixel. The extracted values of capacitances that could account for coupling to memory cells were up to a few tens of aF. They were too small for their unequal distributions to induce differences of voltages on 100 fF memory capacitors high enough to explain the shift observed in Figure 5.6. On the other hand, a post measurement analysis of the pixel layout revealed that one of the digital lines on metal2, this used for activating of a charge injection compensation switch in one of the two memory cells, lays in the distance of 0.4 μm from one side of the n-well. The estimated value of the coupling capacitance was about 90 aF. Assuming a negative step from 3.3 V to 0 V on the digital line, a 10 fF capacitance of the n-well region to ground and the total transconductance g_{mt} of the charge sensing element about 45 μS, the change in the output current is equal to about 1.1 μA.

Table 5.1: Summary of pedestal and noise measurements

Pixel	S1-S2 (odd frame) [nA]	S1-S2 (even frame) [nA]	Standard deviation [nA] (ADC)	DAQ Noise [nA] (ADC)
50 fF	1220	-1130	53 (21.3)	2.3 (0.9)
100 fF no comp	840	-800	38 (15.0)	2.3 (0.9)
100 fF comp	840	-780	38 (15.0)	2.3 (0.9)

The value, estimated in this way, shows a very good agreement with the shift depicted in Figure 5.6. The coupling can easily be avoided by pushing away all control lines from the n-well region, and by introducing shielding around the latter on the next prototypes. Nevertheless, it was unexpected. The shift between samples does not cross out the idea of the high sensitivity detector of weak signals from charged particles. The shift is systematic, having a small variation around its mean value, can be flattened out by subtracting a programmed value for even and odd frames by a circuitry that can be integrated on the next version of the detector.

The statistical analysis on differences of two current samples from in-pixel memory cells was performed for each sub-matrix. The noise performance of the system was measured. The measurements were performed at the temperature range from 0 °C to 30 °C and frequencies of the main clock from 10 MHz to 50 MHz, translating to the frame integration time from 19.2 ms to 3.8 ms.

The results did not show dependence of pedestals and noise on temperature and clock frequency within the ranges examined. The same variance was measured independently for current samples from both memory cells. The results, including the mean value calculated for odd and even frames, temporal noise for the whole system and the noise of only the data acquisition system with PB but without the MVII chip, are shown in Table 5.1.

It is noticeable, that the noise level is significantly higher for the pixel with a smaller capacitance of the memory cell. The same noise performance was observed for pixels with memory cells equipped with dummy switches, to compensate for charge injections from channels of the active switches, and pixels with disconnected dummy switches. The use of compensation switches adds additional complexity and does not improve the performance according to presented measurements. A distribution of current signals, after the CDS operation, is presented in Figure 5.7 for a single arbitrarily chosen pixel with 100 fF storing capacitor. This histogram was built for 4500 frames. In order to reduce the difficulty of the data analysis, it was decided to examine separately odd and even frames. This allowed considering only one polarity of signals and led to an easier extraction of signals generated by ionization. The tests, performed with external 13 kΩ transresistance amplifiers on the proximity board (PB), required using current amplifiers, implemented on the MVII chip. The latter were simple current mirrors with a gain of 10. They were biased at a constant 50 μA current in the input branch. The DC component of the pixel current was subtracted at the input of the current mirror. This configuration did not allow the optimum noise performance, however the amplification of the output current from MVII allowed neglecting contributions of the external stages to the total noise. The bandwidth of the PhotoFET circuit during sampling, f_{up1} was defined by:

$$f_{up1} = \frac{g_{mMm1,Mm4}|_s}{2\pi C_{gMm1,Mm4}} \tag{5.5}$$

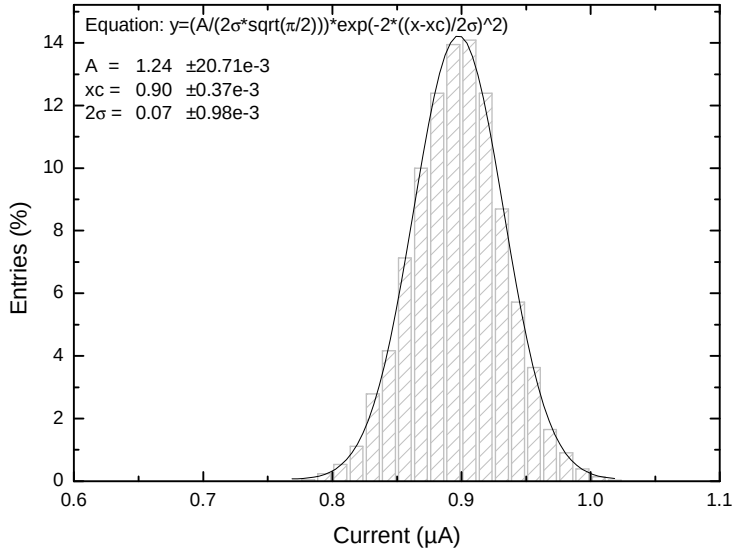


Figure 5.7: Distribution of a single PhotoFET pixel current after CDS. The distribution is shown for a pixel with the storage capacitor of 100 fF and limited to even frames only.

where $g_{mMm1,Mm4}|_s$ is a small signal transconductance of current sampling transistors in a pixel during sampling, and $C_{gMm1,Mm4}$ is the capacitance of a memory cell. The capacitance $C_{gMm1,Mm4}$ is not constant in sampling and readout periods.

The transistors Mc1 and Mc2, used in a system allowing the calculation of the average current from the whole row, are not turned on when the current of the transistor M1 is sampled in a memory cell. They are turned on during read out of the stored samples, thus the capacitance is decreased by a factor of about 1/3 of the oxide capacitance of the transistors Mc1 and Mc2 during the readout. This results in an increase of the memory current by a factor G.

The transresistance amplifiers on PB, being the slowest component of the system, defined the frequency bandwidth. The bandwidth of the system during the readout f_{up2} was estimated in simulations, using proprietary SPICE models of operational amplifiers, to be about 20 MHz. The choice of the bias point of the pixel cell was not really optimized for the best noise performance in the current design. Biasing currents and voltages were selected for flexibility of testing and studying performances in different conditions. For the same reason, the bandwidth of the PhotoFET was not limited by any additional capacitive load. As a result, the noise was sampled on the current memory cells in a much wider bandwidth than required by the read out speed. The bandwidth of the PhotoFET cell,f_{up1} was equal to about 200 MHz and about 70 MHz for $C_{gMm1,Mm4}$ equal to 50 fF and 100 fF, respectively, at the bias condition at which the readout current of the PhotoFET cell was about 20 μA. Identification of the main noise contributors and correlation of noise calculation with noise measurements, presented later in this chapter, can be used as guidelines for next designs. The transistors, contributing in a significant amount to the total output noise, can easily be targeted and their contributions quantified. The root mean square current noise values referred to the output node Ipix from pixel are given by Equations 5.6

to 5.10.

$$\overline{\langle i_{M2}\rangle} = \sqrt{\int_0^{f_{up1}} \frac{8}{3} kT \frac{1}{g_{mM2}} g_{mM1}^2 G^2 df} \tag{5.6}$$

$$\overline{\langle i_{Msf1}\rangle} = \sqrt{\int_0^{f_{up1}} \frac{8}{3} kT \frac{g_{mMsf1}}{g_{mM2}^2} g_{mM1}^2 G^2 df} \tag{5.7}$$

$$\overline{\langle i_{M1}\rangle} = \sqrt{\int_0^{f_{up1}} \frac{8}{3} kT g_{mM1} G^2 df + \int_0^{f_{up1}} \frac{8}{3} kT g_{mbM1} G^2 df} \tag{5.8}$$

$$\overline{\langle i_{Mm1,Mm4}\rangle} = \sqrt{\int_0^{f_{up1}} \frac{8}{3} kT g_{mMm1,Mm4}|_s G^2 df + \int_0^{f_{up2}} \frac{8}{3} kT g_{mMm1,Mm4}|_r G^2 df} \tag{5.9}$$

$$\overline{\langle i_{\Sigma MIgain}\rangle} = \sqrt{\int_0^{f_{up1}} \frac{8}{3} kT \left(\Sigma_{input} g_{mNMOS,PMOS}\right) df + \int_0^{f_{up2}} \frac{8}{3} kT \frac{1}{10} \left(\Sigma_{output} g_{mNMOS,PMOS}\right) df} \tag{5.10}$$

where k is the Boltzmann's constant, T=300 K, all g_m components represent small signal transconductances. The subscripts at symbols of individual current noise components refer to appropriate transistors as noise sources. The last component represents the noise of the current buffer with two sums of transconductances of transistors at the input and at the output of the current mirror, including also the transistors used for the subtraction of the DC current component. Substituting numerical values, estimated at the chosen operating point used in noise measurements, (g_{mM2}=20.0 μS, g_{mM1}=44.0 μS, g_{mbM1} =6.9 μS g_{mMsf1}=10.9 μS, $g_{mMm1,Mm4}|_s$=44.0 μS (63.0 μS), $g_{mMm2,Mm5}|_r$= 49.0 μS (69.3 μS), G=1.2), the constituent noise contributions are equal to: $\overline{\langle i_{M2}\rangle}$ = 11.0 nA (18.3 nA), $\overline{\langle i_{Msf1}\rangle}$ = 8.1 nA (13.5 nA), $\overline{\langle i_{M1}\rangle}$ = 8.0 nA (10.5 nA), $\overline{\langle i_{Mm1,Mm4}\rangle}$ = 8.5 nA (15.3 nA), and $\overline{\langle i_{\Sigma MIgain}\rangle}$ = 12.0 nA.

The first values correspond to estimations for 100 fF capacitances and values in brackets are calculated for 50 fF capacitances. The total noise current $\overline{\langle i_{total}\rangle}$ = 22 nA (32 nA). Assuming subtraction of two samples, the final theoretical nose value increases approximately by a factor $\sqrt{2}$ resulting in $\overline{\langle i_{totalCDS}\rangle}$ = 31 nA (45 nA). The presented noise analysis includes only thermal noise. Flicker noise was not considered, assuming its partial reduction in the subtraction process. The use of the current buffer was only provisional in MVII. The goal was to use a low noise, integrated transresistance amplifier. Substitutions of numerical values in Equations 5.6 to 5.10 reveal that the source follower is the dominant contributor to noise. The methodology to decrease the noise of the source follower is to limit the bandwidth of the PhotoFET pixel during current sampling and to increase the transconductance of the transistor M2. The bandwidth can be limited to allow only correct settling of signals when the pixel is powered on. The bandwidth of the PhotoFET cell in MVII was incommensurably wide with respect to the time during which pixels are switched on. In matrices of image-sensing elements, the rate at which an individual pixel can be addressed is typically determined by the speed of transfer of signals from a pixel to the column end. Generally, the columns lines are loaded with multi-picofarad capacitances. Hence, a frequency of the clock selecting pixels may be up to a few tens of MHz. Having as much time for in-pixel current sampling as for reading out the sampled data from pixel, the bandwidth of the PhotoFET cell can be decreased in the optimized design with respect to the current design. This will result in a similar degree of noise reduction.

The transconductance of M2 can be increased by allowing more current in the source follower. The absolute noise contribution of the source follower increases with increasing transconductance of the transistor M1. However, the noise, referred to the n-well node, depends only on the transconductances of M2 and the diode-connected transistors Mm1 and Mm2 in memory cells through the frequency bandwidth. The increase of gate-to-source voltage of the source follower transistor translates to an increase of the current of the transistor M1 and transistors in the memory cells. Their transconductances and noise spectral densities of noise sources associated with these transistors increase accordingly. Since the increments of transconductances of M2 and Mm1 and Mm2 increase proportionally, input referred ENC does not depend on the current in the branch M1-Mm1 (-Mm2). The noise contribution of transistors Mm1 and Mm2 is proportional to the square of their transconductances, thus these transistors, as well as the transistor Msf1, should be designed with the minimized width to length ratio. It was observed in the measurements that the current level of the transistor M1 depended on the power supply vdd_phfet. The increase of the current occurred for increasing power supply voltage at the bias current of the source follower. The effect resulted from a strong body effect showed by the transistor M2. The increase of its gate potential resulted in its higher gate-to-source voltage, leading to the increase of the current of the transistor M1. The increase of the bias current of M1 has no effect on noise originating in the PhotoFET cell. The increased transconductance of the transistor M1 allows reducing the contributions of signal processing stages, placed downstream, to the input referred ENC.

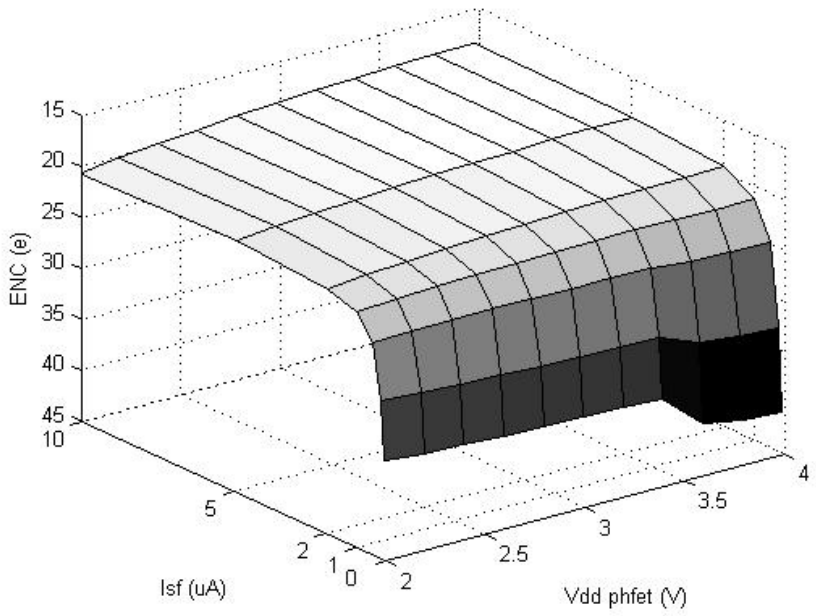


Figure 5.8: Simulation of ENC vs. bias current of the source follower and power supply voltage for the PhotoFET cell implemented in MIMOSA VII

The illustration of the input-referred ENC is shown in Figure 5.8 as a function of bias conditions for the current design of the PhotoFET cell. ENC is plotted vs. the power supply voltage Vdd_phfet, defining the potential on the charge collecting diode, and the current of the

source follower. The optimum operation point of the cell lays at the source follower current above 1 μA. A reasonable value, regarding power consumption and dynamic swing, of the bias current of 15 μA was found for vdd_phfet equal to 2.7 V. The choice of the bias conditions, obtained in simulations performed with SPECTRE from Cadence, was in a good agreement with the measurements. However, the conclusions from these simulations, reached after the first measurement results were available, suggested operation at higher bias currents than initially considered.

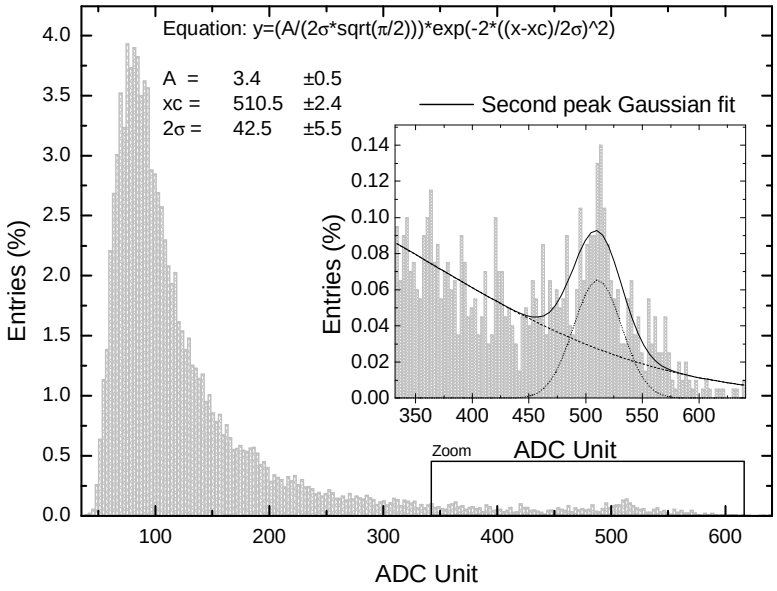


Figure 5.9: Distribution of signals from PhotoFET pixels exposed to ^{55}Fe and passing the criteria of signal-to-noise ratio higher than five.

The distribution of signals from single pixels in MVII in the calibration with ^{55}Fe is shown in Figure 5.9. The spectrum was obtained for S/N superior to five. One million of frames were scanned for hits. Two peaks are visible in the spectrum. The first peak, at approximately 100 ADC counts, represents the charge collected by a single pixel because of a thermal diffusion process. The second peak, placed at about 510 ADC, is the calibration peak due to the complete collection of the 1640 e^- liberated by an X-ray photon. One ADC count corresponded to 500 μV. The transimpedance gain of the analog chain was 200 kΩ. Thus the charge-to-current conversion factor was approximately 770 pA/e^-, resulting in S/N equal to 34. The absolute value of ENC calculated for the PhotoFET element in the optimum bias current configuration was 50 e^- after the CDS processing.

5.4 Implementation of CDS

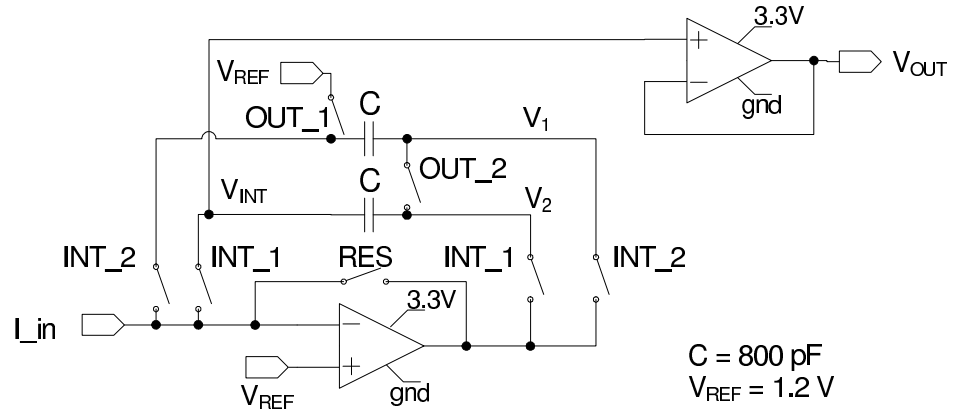
5.4.1 CDS with discreet components

The pixel in the MVII chip produces two current samples in each access. A circuitry for subtracting two samples is required to extract signals generated by ionizing particles. An approach, based on the current integration and subsequent subtraction of the resulting voltages, seemed to be appealing. Different practical implementations of an analog subtraction circuit can be proposed. Beside the need for high gain, low offset and noise, immunity to interferences, and a high speed of operation, the criterion of choosing the architecture of the circuit for the high performance and parallel processing is minimum power consumption and minimal occupied area.

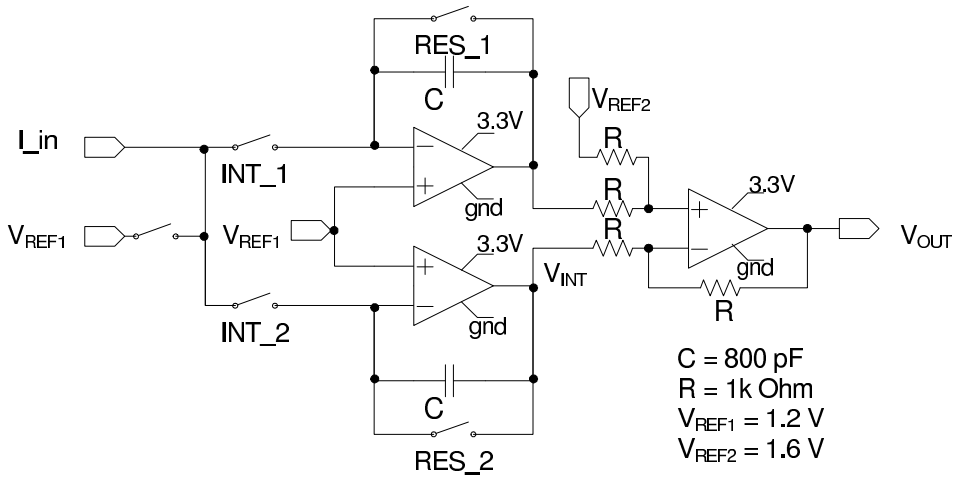
In the current work, one solution to process signal currents directly on the chip, at the column ends, was adopted and integrated in MVII. The estimation of pixel-to-pixel dispersions of currents had a considerable bearing on the functionality of the circuit. The design kit for the process used did not contain enough information to assess these dispersions during the design. In order to validate the readout approach with current integrating transimpedance amplifiers and DAQ developed, two sister architecture blocks, subtracting two current samples, were implemented using discrete components on a dedicated proximity board. The first solution employed one operational amplifier and two integrating capacitors switched successively in the feedback path, as presented in Figure 5.10(a). The second solution, illustrated in Figure 5.10(b), was built with two separate amplifiers and two integrating capacitances, each connected permanently in the feedback path of the amplifier. The first architecture was topologically a duplication of the circuit implemented in the MVII chip.

The two discrete implementations were tested in order to compare their performance. In the ideal case, both configurations of the current integrating transimpedance amplifiers should yield a similar performance for gain and speed. The first amplifier requires less power consumption and it occupies less area. The current integrating capacitors need however to be switched in the amplifier's feedback path in order to process two current samples and to perform its subtraction exploiting the capacitor arithmetic principle. The switching process and switches that are not ideal elements may introduce an excess noise. The second architecture uses two amplifiers biased continuously, thus its power consumption and the occupied area are larger than for the first circuit. The noise of one-amplifier (1-amp) transimpedance block could be better than the two-amplifier (2-amp) circuit, because samples of noise, originating in the operational amplifier, are correlated on two capacitances and can be subtracted during the readout. The 1-amp circuit requires an increased switching activity that could yield a higher sensitivity to interferences and noise due to charge injections.

The test of the discrete implementations of transimpedance block with direct current outputs from MVII were performed to select better architecture for next integrated submissions. All parasitic capacitances are even three orders of magnitude larger in a discrete implementation, compared to its integrated counterpart. Much larger current integrating capacitors, aiming at reduction of the charge sharing on parasitic capacitances, had to be used. In order to measure comparable voltages, the input currents had to be amplified and the integration intervals had to be accordingly extended. The high performance discrete transistor switches used (ADG712) were characterized by input and output capacitances of a few pF. Therefore, in order to minimize effects of charge sharing, large 800 pF integrating capacitors were used. The current signals were



(a)



(b)

Figure 5.10: Schematic diagrams of two CDS schemes envisaged for the PhotoFET readout. The first implementation is based on a single integrating amplifier and two integrating capacitors, (a), while the second architecture comprises two integrating amplifiers (b).

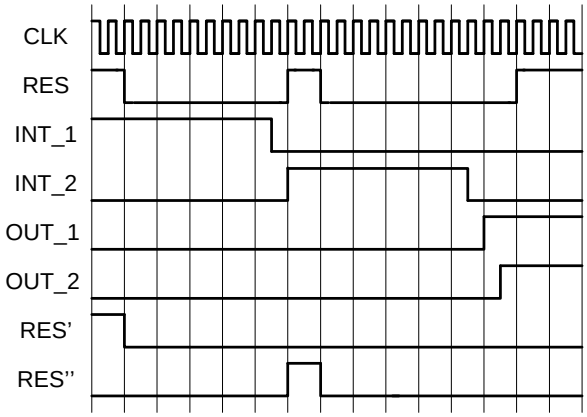


Figure 5.11: Timing diagram for controlling transimpedance amplifiers presented in Figure 5.10

additionally amplified with the gain of 100. Both transimpedance amplifiers were built with fast, low noise CMOS operational amplifiers OPA355. The schematic diagrams of two CDS circuits are shown in Figure 5.10. The first transimpedance amplifier requires two integration phases. Each phase is preceded by a reset of the capacitor used in that phase for current integration. The reset was executed by asserting the RES signal. The selection of current signal from the first and the second memory cell in a pixel was determined by signals INT_1 and INT_2. During the integration phase, the current sample was converted into voltage on the feedback capacitor according to:

$$V_{cap1,2} = \frac{I_{1,2} \times T_{1,2}}{C_{1,2}} \tag{5.11}$$

where T is the integration time and subscripts 1, 2 make distinction between the first and the second sample.

The output signal was read out by connecting both capacitances in series by means of signals OUT_1 and OUT_2 and clamping one terminal of the series combination of capacitors to a stable reference potential. The resulting voltage equals the reference level shifted by the difference of two samples:

$$V_{OUT} = V_{REF} + V_{cap1} - V_{cap2} = V_{REF} + \frac{I_1 \times T_1}{C_1} - \frac{I_2 \times T_2}{C_2} = V_{REF} + \Delta I \times \frac{T}{C} \tag{5.12}$$

where V_{OUT} is the output voltage during the readout phase, $V_{cap1,2}$ are signal voltages sampled on both integrating capacitances, and assuming $C1 = C2 = C$ and $T1 = T2 = T$. From Equation 5.12, the theoretical gain is equal to T/C. Introducing $T = 0.9$ μs and C =800 pF and the current gain of 100, the transimpedance gain equals 112 kΩ.

The second structure was designed with two independent integrators. The two current samples from a pixel were integrated in two consecutive phases with the INT_1 and INT_2 signals accordingly asserted. Both integrations were preceded by a clear of the integrating capacitors, closing the reset switches RES_1 and RES_2. The subtraction of the voltages, resulting from current integrations, was completed by a differential amplifier with a resistive feedback network. The result of the subtraction was available immediately after the second integration. The first transimpedance amplifier required additional switching cycles before the difference value could

be read out. The theoretical transimpedance gain can be calculated by the same formula as for the 1-amp design.

Charge injections associated with closing and opening of switches may have an important influence on the operation of the amplifier with switched capacitors [97]. The 2-amp solution should be affected less by the charge injections accompanying the switching activity than the 1-amp design. The timing diagrams of signals driving switches in both designs are presented in Figure 5.11. All external control signals are synchronous to the operation of the MVII chip. The frequency of the main clock CLK in the tests was 10 MHz. This was the maximum frequency for the operation of the discrete transimpedance amplifiers. The value was assessed in transient simulations performed with the ELDO simulator. At this frequency, the current amplifying circuitry, depicted in Appendix C Figure C.2, was sufficiently fast to allow current signals to reach stable values at the beginning of each integration phase. The total transimpedance gain of the readout chain from the pixel level to DAQ was estimated at approximately 180 kΩ.

5.4.2 Performance of two CDS circuits

A theoretical analysis of the two discrete solutions focused on comparing their noise performances. Both transimpedance amplifiers were examined with ELDO simulations. Switches were modeled as illustrated in the schematic diagram in Figure 5.12. The switch model included the digital feedthrough effect manifested by charge injections through the capacitances C_{rec}. It took also into account the input and output capacitances of the switch C_{in}, C_{out}, respectively. Numerical values were obtained directly or calculated from the switch data sheet ($C_{rec} = 1.25$ pF, $C_{in} = C_{out} = 10.75$ pF, $R_{on} = 4\ \Omega$). Detailed models of the operational amplifier, available from the manufacturer, were used in transient simulations to examine timing dependencies and signal waveforms. Transient noise simulations were performed using a simpler, linear, 2-pole ELDO macromodel for an operational amplifier to reduce the simulation time. The noise of the amplifier was modeled with the ELDO voltage noise source, having a specific spectral characteristics, i.e., a combination of white noise and flicker noise based on numerical values extracted from the data sheets (white noise level $16 \cdot 10^{-18}$ V^2/Hz, flicker noise level at 1 Hz $6 \cdot 10^{-12}$ V^2/Hz$^{(1-\alpha)}$, where $\alpha = 0.95$ is the exponent of flicker noise).

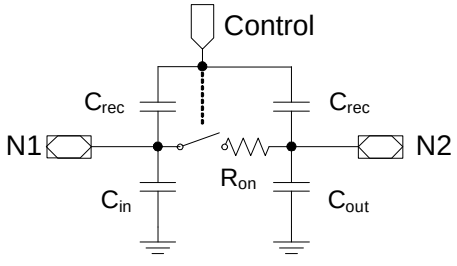


Figure 5.12: Model of a transistor switch used in simulations. Charge injection in the switch is modeled by Crec capacitors that couple the control signal with the input and output nodes.

Transient noise simulations proved that the circuit built with one amplifier demonstrated better noise performance. During the readout phase, the rms noise voltage of the 1-amp solution was about 2.5 times smaller than for the 2-amp version, i.e., 18 μV and 70 μV rms, respectively. A significant portion of noise was added by the output stages in both cases, i.e., by the output

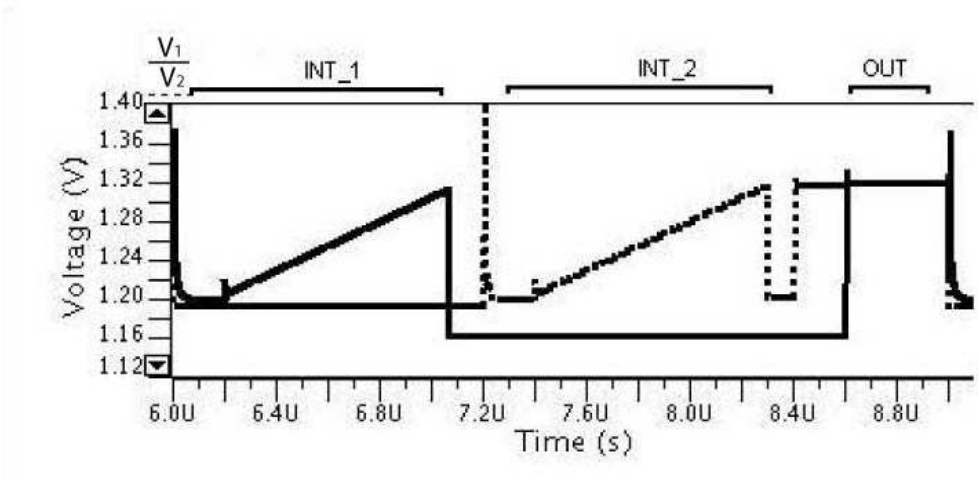
buffer and by the subtracting circuitry. The total noise contribution of the switches amounted to only 7 μV and 2 μV rms in the 1-amp and the 2-amp design, respectively, and could practically be neglected. The rms noise voltage at the output of the 1-amp circuit is lower because of a partial correlation of noise generated by the operational amplifier in the samples stored on both integrating capacitors. The correlated component of noise is removed during the readout phase as a result of the capacitance arithmetic:

$$\begin{aligned} V_{OUT} &= V_{REF} + (V_{cap1} + V_{nc1} + V_{nn1}) - (V_{cap2} + V_{nc2} + V_{nn2}) \\ &= V_{REF} + (V_{cap1} + V_{nc1}) - (V_{cap2} + V_{nc2}) \end{aligned} \tag{5.13}$$

where $V_{nc1,2}$ is the correlated component of the sampled noise and $V_{nn1,2}$ are not correlated noise components sampled on the first and the second integrating capacitor.

Both transimpedance amplifiers track the same noise performance tendency in the range of the simulated integration times from 0.22 μs to 5.5 μs. Unfortunately, a direct comparison in measurements of both transimpedance circuits, implemented in a discrete form was not possible. The noise was dominated by DAQ at the level of a few hundreds of μV rms. If integrated, the 1-amp transimpedance circuit may have significant advantages, especially when this circuit is used as the first amplification stage in the analog readout chain due to its noise cancelation feature.

An example of the ELDO transient noise simulation is presented in Figure 5.13. The figure illustrates transient signal waveforms for both integration phases and the time dependent rms voltage of the output noise in a full readout cycle for one pixel. The simulation was performed for the main clock frequency of 10 MHz and the input current of 100 μA. Two consecutive integration phases INT_1,2, of about 0.9 μs each, and the 0.4 μs long readout phase OUT, following the integration, are clearly distinguishable. The signals of two current samples, integrated on two capacitors, are presented in Figure 5.13(a) for the 1-amp solution. The output voltage waveform, marked with a thick solid line VOUT, the rms noise value associated with this node, marked with a dark hackly line, and the rms value of noise measured at the input of the voltage buffer VINT, marked with a thin dashed line, are presented in Figure 5.13(b). Output voltage signal VOUT, marked with a thick solid line, and the rms noise value, marked with a dark hackly line, for the 2-amp solution are presented in Figure 5.13(c). Noise rms voltage simulated at one of the input nodes VINT of the subtracting circuitry in also shown in this figure below the output noise waveforms. The noise at the output of the 1-amp transimpedance amplifier is dominated in the readout phase by the noise generated by the output buffer. In the case of the 2-amp version, the noise is a quadratic sum of equal noise components from both current integrating branches and the subtracting circuitry. The current integrated in both phases was equal and therefore the output level during the readout phase returns to the reference level of 1.2 V and 1.6 V in the case of the 1-amp and 2-amp design, respectively.



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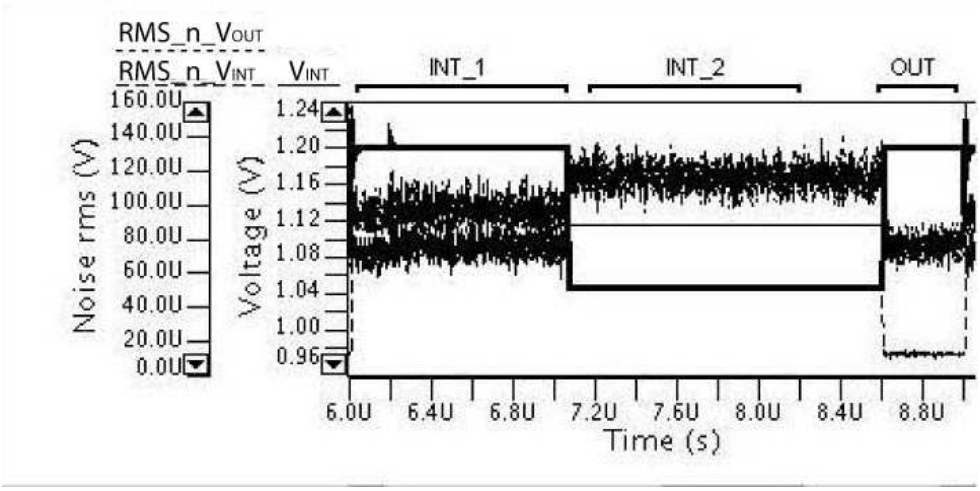

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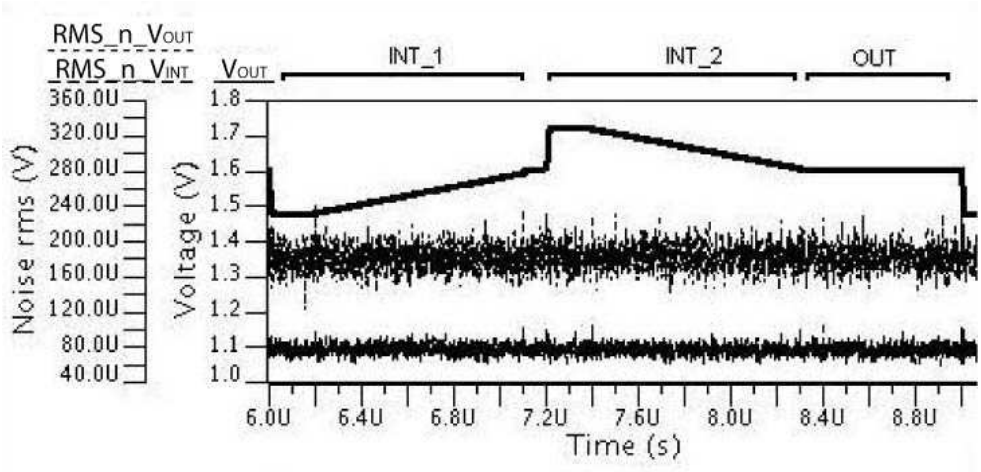
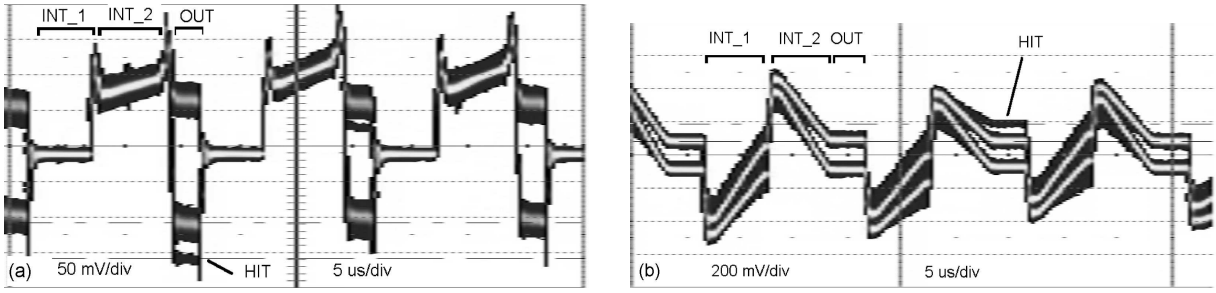


(c)

Figure 5.13: Simulated transient signal waveforms of the output signal and rms voltage noise associated with this output during one readout cycle for the 1-amplifier, (a, b), and 2-amplifiers, (c), implementations of transimpedance amplifiers. The two consecutive integration phases and the readout phase are marked as INT_1, INT_2, and OUT, respectively. Signal names correspond to net names in Figure 5.10.

5.4.3 Tests with direct current outputs

Both versions of discrete implementations of transimpedance amplifiers, implemented on a dedicated proximity board, were tested with direct current outputs of the MVII chip. The bias conditions of the PhotoFET cell were set to: $vdd\_phFET = Vdd\_sf = 3.0\ V$, $Isf < 100\ nA$. The average value of current, sourced by PhotoFET cells in the matrix, was 15 μA for these conditions. The on-chip current source was set to 15 μA by an external current reference. The bank of the on chip current amplifiers was used to provide a current gain of 10 for the output signals. An additional current gain of 10 was used on PB before transimpedance amplifiers. The sensor was exposed to X-ray photons from an ^{55}Fe source.



(a) (b)

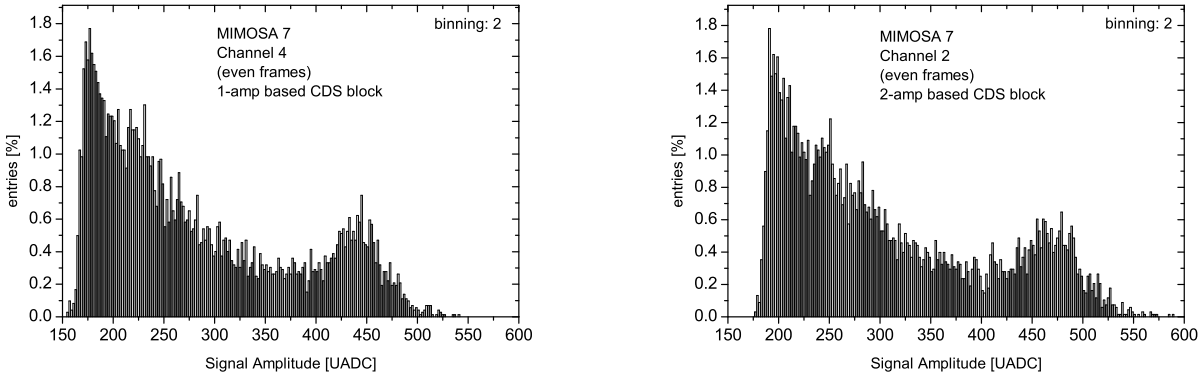
Figure 5.14: Oscilloscope output signal waveforms for both designs of the transimpedance amplifier for MIMOSA VII; version 1-amp (a), version 2-amp (b). The signals were observed at one line of the differential output of the proximity board.

An example of the voltage waveforms recorded with an oscilloscope is presented in Figure 5.14. Outputs of the two versions of transimpedance blocks are plotted. The gain for signals in Figure 5.14 is decreased by a factor 2 with respect to the gain in the DAQ acquisition card, because only one of the two lines from a differential line driver was visualized on the oscilloscope. The main clock frequency, driving the MVII chip and defining the readout cadence, was 10 MHz. Time intervals corresponding to the first and the second integration (0.9 μs) and the readout phase (0.4 μs) are labeled in the plot in Figure 5.14 as INT_1, INT_2 and OUT, respectively. The waveforms are presented using the "persistency" operating mode of the oscilloscope. Two levels shifted vertically one with respect to another in the readout phase correspond to even and odd frames. Events, when the voltage level significantly changes during the readout phase can be observed as occurring randomly in time on the oscillograph. These events, marked with the HIT pointer in Figure 5.14, indicate conversion of X-ray photons in the active layer of the MVII sensor. Waveforms measured for the 1-amp and 2-amp transimpedance amplifier are presented in Figure 5.14(a) and Figure 5.14(b), respectively. The polarities of X-ray generated signals in Figure 5.14(a) and Figure 5.14(b) are opposite, because lines of opposite polarities from differential outputs were monitored.

The operation of the DAQ was programmed to sample the signals during the readout phase and to store one sample for each pixel to the disk. The track of even and odd frames was kept to ease a later statistical analysis. The analysis of the data registered aimed at the estimation of residual pedestals and noise and the extraction of single photon signals for each pixel. The chip

Table 5.2: Noise measured in discrete CDS circuits.

Pixel	1-amp CDS [nA](ADC)	2-amp CDS [nA](ADC)
50 fF	65 (22.0)	70 (24.0)
100 fF w/o compensation	50 (17.0)	56 (19.0)
100 fF w/ compensation	48 (16.5)	54 (18.5)



(a) (b)

Figure 5.15: Spectrum of X-ray photons obtained for the MIMOSA VII pixels comprising 100 fF memory capacitor and read out through external transimpedance amplifiers. Gaussian fits to the calibration peaks for 1-amp, (a), and 2-amp, (b), architecture extract $\sigma = 23.6$ ADC and $\sigma = 27.9$ ADC counts, respectively.

was not exposed to X-ray photons for the measurements of the intrinsic noise of the sensor. The results of noise measurements are presented in Table 5.2. All measurements were performed with the chip under tests kept in a light-tight box and at ambient and not stabilized temperature. It is noticeable that the first 16 pixels featuring the smallest, 50 fF memory capacitor, exhibit the highest noise. The dominant source of noise is in a pixel. The contribution to the total noise of the readout chain, remaining after disconnecting the MVII chip, including DAQ, is very limited. A similar conclusion, concerning the lack of influence of in-pixel charge injection compensation switches on the noise performance, can be drawn for the system with discrete transimpedance amplifiers.

The calibration of the conversion gain of the system, consisting of the MVII detector and both external CDS implementations, was performed with X-rays from an ^{55}Fe source. The calibration was performed in the same bias conditions as noise measurements. Histograms, corresponding to the data obtained with the 1-amp and 2-amp transimpedance amplifiers, are shown in Figure 5.15(a) and Figure 5.15(b), respectively. These histograms were constructed with signal samples above 10 times the noise level. Both figures show histograms calculated for even frames only. Histograms created for odd frames were identical. The position of the calibration peak can easily be extracted from both figures at approximately 470 and 440 ADC

counts for the 1-amp and 2-amp transimpedance amplifiers, respectively. The calibration peaks translate to CQI of the PhotoFET cell equal to 840 pA/e^- and 790 pA/e^-. A slightly higher value of the conversion gain in one case is accompanied by a higher value of noise measured.

The estimation of S/N gives the same (within 5% accuracy) result of about 25 for both readout channels with both versions of transimpedance amplifiers. These results prove that both CDS solutions implemented in the testing board were fully functional and can be considered as candidates for future integration.

The width of the calibration peak carries information about pixel-to-pixel gain dispersions. Gaussian fits to the calibration peaks in Figure 5.15 yield $\sigma_p = 23.6$ and $\sigma_p = 27.9$ ADC counts, for the 1-amp and the 2-amp transimpedance amplifier, respectively. The width of the peak is a quadratic sum of temporal noise σ_t, dispersion of the conversion gain due to differences in the transistor M1 bias current, ΔQCI_I, and a spread of the conversion gain due to pixel-to-pixel variation of the n-well/p-sub capacitances, ΔQCI_C. The dispersion of the charge-to-current conversion factor due to the spread of n-well/p-sub capacitances is given by:

$$\Delta CQI_C = \sqrt{(\sigma_p)^2 - \left((\Delta CQI_I)^2 + (\sigma_t)^2\right)} \tag{5.14}$$

σ_p is calculated from the width of the calibration peak, σ_t is the temporal noise. Substituting a numerical value for ΔCQI_I =3.5%, as it was estimated in one of the previous chapters, ΔCQI_C equals to about 2.9%. It is a typical value for classical photodiode active pixel sensors.

5.4.4 Integrated CDS

The choice of a transimpedance amplifier for the integration in the MVII prototype was strongly determined by the requirement of reduced power consumption. Additionally, the solution occupying less silicon area was preferred. The MVII chip was designed to test a PhotoFET cell in a full matrix structure with a prototype readout chain. The chip integrated the CDS circuitry in current mode, investigating the feasibility of the first stage of signal sparsification implemented on-chip.

A conceptual schematic of the MVII transimpedance amplifier, which was placed at the ends of eight columns of the pixel matrix, is shown in Figure 5.16. Conversion of current to voltage is achieved through current integration. The design of the amplifier is based on a principle of a switched capacitors circuit. The design is an integrated version of the 1-amp amplifier. The two-phase operation of the integrated amplifier is identical to the discrete implementation. The advantages include cancelation of correlated noise components from an operational amplifier, low power consumption and silicon area efficiency. However, the design entails certain amount of risk related to the switching activity. A careful approach to the design of a physical layout of the circuitry was critical for minimizing all parasitic effects. An integrated circuit differs in several details from the discrete implementations discussed before. Each transistor switch has its complementary counterpart used for compensation of charge injection from a transistor channel and from a control signals feedthrough occurring during the switching operation. No charge injection compensation switches are depicted in Figure 5.16. There is an additional switch connecting the input column line to the reference voltage set to 1.2 V. The switch, activated by the PCH signal, allows pre-charging the parasitic stray capacitance of the column line before each integration phase. The two currents, sunk by pixel memory cells, are integrated

in sequence on two 200 fF capacitors. The operational amplifier design is a classical two-stage folded cascode amplifier with the DC gain of 72 dB and the unity gain frequency of 66 MHz. The current consumption is 100 μA in the differential pair and 18 μA in the two branches of the

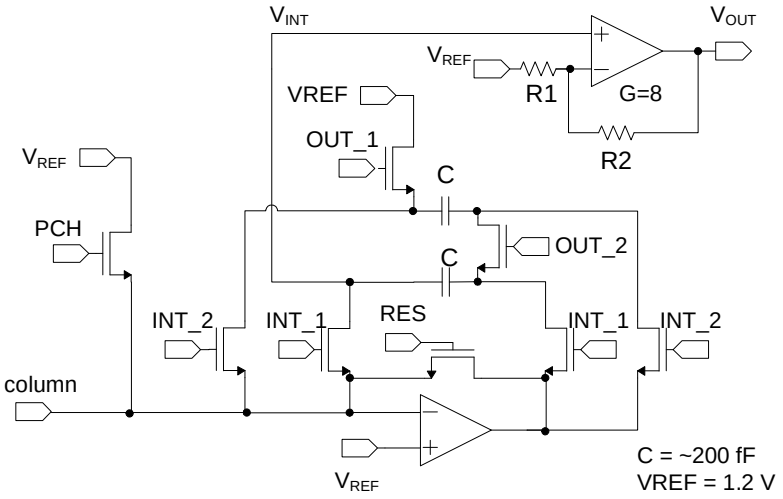


Figure 5.16: Schematic diagram of the current integrating transimpedance amplifier in the MIMOSA VII prototype.

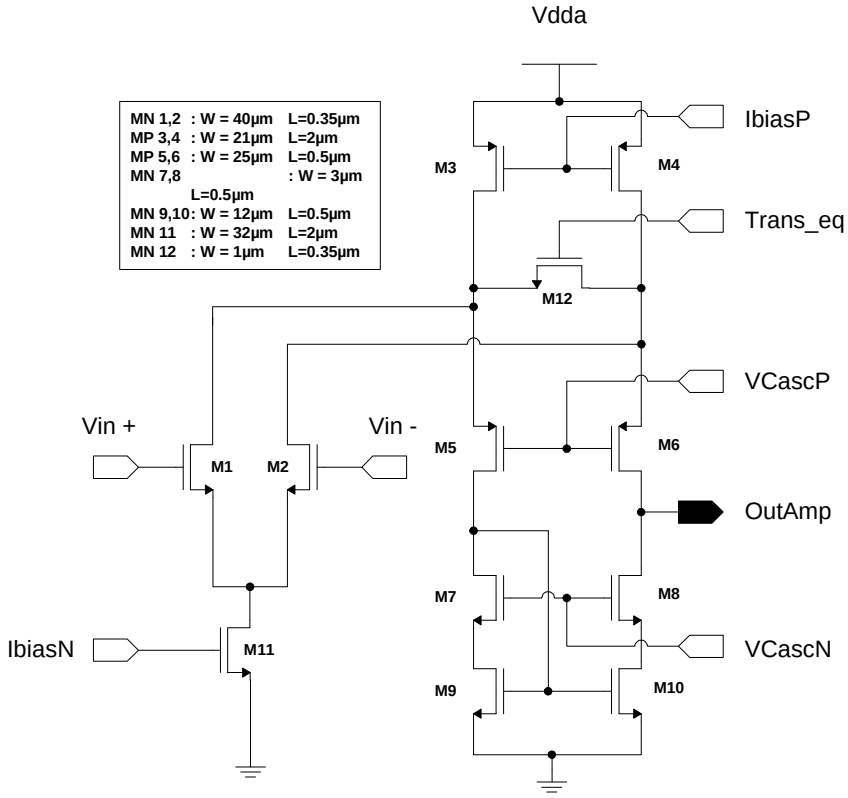


Figure 5.17: Schematic diagram of the folded cascode operational amplifier used in the MVII current integrating transimpedance amplifier

folded cascode. The schematic diagram of the folded cascode operational amplifier is shown in Figure 5.17. Using single integration time T = 100 ns and integrating capacitances C=200 fF, the transimpedance gain is equal to 500 kΩ according to Equation 5.11.

The operation of the transimpedance amplifier was examined in simulations using the SPECTRE simulator and transistor models for the fabrication process used. The post layout simulated gain was reduced almost by a half to 280 kΩ. The decrease of the transimpedance gain resulted from a voltage attenuation on a capacitive divider between the equivalent capacitance of a series connection of two current integrating capacitors and the parasitic capacitance associated with the input of the voltage buffer. The noise performance of this amplifier was estimated in transient noise simulations with ELDO. The results showed that the expected noise level during the readout phase was approximately 300 μV rms. This translates to about 1 nA rms of the input referred noise current and, assuming the PhotoFET charge-to-current conversion factor of 770 pA/e^-, gives less than two e^- ENC.

5.4.5 Feedback from tests

The transimpedance amplifiers integrated in the MVII chip were connected to eight columns of pixels. The compensation current was delivered for subtraction of the DC current component at the input of the amplifiers. Therefore, two testing modes were possible.

The first mode, which was actually a normal operation of the circuit, allowed testing of the whole readout channel, including pixels. The sources of the processed current signals were in-pixel current memory cells addressed sequentially for readout. The subtraction of the DC component was essential to avoid saturation of transimpedance amplifiers in this mode.

Another mode of tests, called also a static mode, consisted in conversion of the constant current from the DC component compensation circuit, while current sources in pixels were disabled. A readout pattern, in which signals activating pixels were not asserted, could be programmed into the chip through the serial interface.

Large pixel-to-pixel current dispersions, almost 9 μA peak-to-peak as it is shown in Figure 5.3, were measured in earlier tests of direct current outputs. An additional shift of about 1 μA was present between current samples from two current memory cells in the same pixel. The design of the transimpedance amplifier was driven by maximization of the transconductance and voltage gain of the circuit. The presence of the DC component in the signal to be amplified resulted in the saturation of the amplifier. The dispersions of currents had been underestimated in the design of the MVII chip, mostly due to the lack of any measurement data and good simulation models. The high gain of the amplifier determined the maximum value of the DC component in the input current to about 2 μA. This unfortunately impeded full functionality tests of the transimpedance amplifier with the matrix of PhotoFET pixels.

A solution to this limitation could be to work with two currents used for the subtraction accordingly from the first and the second memory cell. However, this mode of operation was not foreseen for the MVII chip and only tests in the static mode of operation were accessible. Fast switching between two slightly different values of the external current was not possible due to the very limited bandwidth of this path. Instead of varying the currents, different integration times for the first and the second sample were used. The gain was estimated by injecting a constant current from the compensation branch and varying one of the integration times, while the pixel currents were disabled. The default integrations time was equal to 100 ns and the

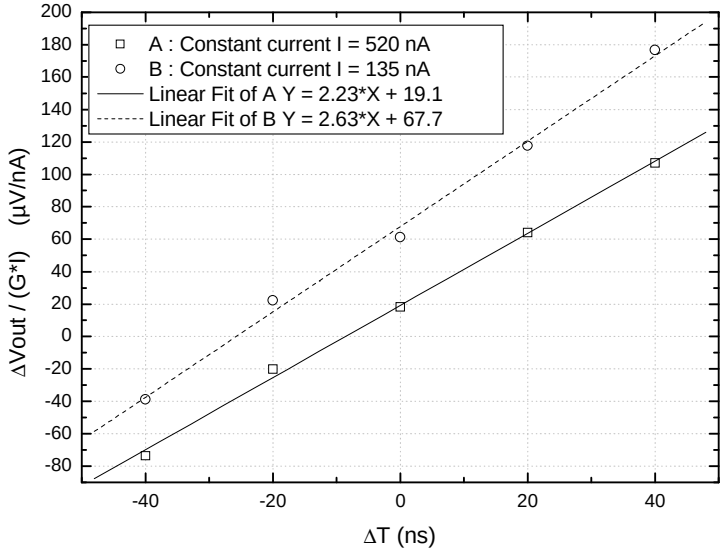


Figure 5.18: Gain of the MIMOSA VII transimpedance amplifier measured for two values of integrated current.

two integration times varied from 100 ns to 60 ns. The transimpedance amplifier was connected to a differential buffer in a non-inverting configuration with a gain of eight, as it is shown in Figure 5.16. The output voltage in this configuration is calculated using a basic operational amplifier theory by:

$$V_{OUT} = V_{INT}\left(1 + \frac{R_2}{R_1}\right) - V_{REF}\frac{R_2}{R_1} \tag{5.15}$$

In the notation for the ideal operation of the circuit, the voltage at the output of the transimpedance amplifier is given by:

$$V_{INT} = V_{REF} + I \times \frac{\Delta T}{C} \tag{5.16}$$

where I is a constant value of the integrated current and T is the difference between both integration intervals. Substituting Equation 5.16 to 5.15 and subtracting the reference voltage from the V_{OUT}, the estimation of the effective integration capacitance can be derived.

$$\frac{\Delta V_{OUT}}{\left(1 + \frac{R_2}{R_1}\right) \times I} = \frac{\Delta T}{C} \tag{5.17}$$

The plot illustrating this formula is shown in Figure 5.18 for two different values of the input current, i.e., 135 nA and 520 nA. The inverse of the slope of the linear fit to the measurement point gives directly the equivalent value of the integration capacitors. The transresistance gain of the amplifier can be calculated assuming the default integration time equal to 100 ns. The two fits, performed for two values of the integrated current, yield slightly different values of

the integration capacitances, i.e. 380 fF and 448 fF for the input current equal to 135 nA and 520 nA, respectively. The gain is accordingly equal to 263 kΩ and 223 kΩ .

The first observation is a decrease of the gain by a factor of two with respect to the value expected from the use of 200 fF physical capacitors. The drop of the gain results from the capacitive voltage division between the series connection of both capacitances in the transimpedance amplifier and the input capacitance of the buffer. The similar gain drop was found in prior simulations. Another observation from Figure 5.18 is the dependence of the response on the common and differential components of the integrated currents. The sensitivity to both components of the current is visible in the presence of the offset between two linear fits for T=0 and the change of their slopes. The vertical shift is equivalent to almost 100 nA for the higher value of the input current. The equivalent values of the current-integrating capacitors change due to a non-linear, signal dependent charge sharing between capacitances in the feedback path and parasitic capacitances, for example junction capacitances of the transistor switches. The performance of the integrated transimpedance amplifier can be improved by designing a circuit with larger current integrating capacitors. The drop of the transresistance gain should be compensated by an additional, placed upstream, current amplification in the next submission.

5.5 Summary of PhotoFET tests

The MIMOSA VII prototype was the first implementation of the PhotoFET cell in a full pixel array, including analog and digital readout circuitry implemented on the same chip. The readout of the chip was organized in a column parallel approach to improve the readout speed. The cell was characterized by a high, almost 1 nA/e^-, conversion factor and featured two current mode memory cells for the CDS operation, aiming at future implementation of the full sparsification processing to create an autonomous, intelligent charged particle detector. The high noise (ENC=50 e^-) found in the measurements was unexpected. However, the noise analysis allowed identifying the source of noise and drawing guidelines for the next optimized prototype.

The noise performance can be improved by lowering bandwidth of each part of the analog chain according to the goal requirements. The bandwidth of the PhotoFET cell could be decreased in an optimized design by several times with respect to the presented design. The same degree of noise reduction should be expected. The pixel design requires larger in-pixel sampling capacitors, improving also the immunity of the design to any external interference. Also other problems found in the measurements, such as a constant shift between two current samples from two memory cells in each pixel or an increased value of the PhotoFET bias current, were understood and quantified preparing the way for future improvements.

Two external solutions for subtracting signal samples, implemented with discrete components, were tested in a preparatory work for the fully operational integrated solution. Unfortunately, the present combination of a pixel and the integrated current signal treatment was not possible to be tested as one entity, because of the larger than expected current dispersion in the PhotoFET cell. However all ideas presented and building blocks tested were verified to be functional.

Although currently this structure is not in the mainstream of development dedicated to STAR, it might, in the future, offer an interesting alternative to the classical, voltage mode pixels.

Chapter 6

MAPS for STAR

MAPS performance established in the recent years with a number of prototypes indicates that this technology has a lot of potential for tracking applications, including the new STAR vertex detector. The first small-scale MAPS prototypes dedicated to the application at STAR have already been developed. The performance of this first generation of prototypes is studied and presented in this chapter, providing a solid base for development of next, large size prototypes.

6.1 Development plan

The high resolution of the PIXEL detector in the Heavy Flavor Tracker can only be achieved with a low radiation length detector that minimizes multiple Coulomb scattering. The material budget has to be restricted for all detector components in the low mass region of $-1 < \eta < 1$, including silicon sensors, mechanical support, and readout cables. In order not to introduce additional material, only an air-flow-based system can be used for sensor and readout cooling. Any liquid-based cooling would significantly increase material budget due to the mass of the liquid and its distribution system. This imposes severe limitations on power dissipation in the part of the detector where low mass is critical, i.e., near the interaction point. Power dissipation of sensors and readout electronics has to be minimized in this low mass region. Additional mass is not so much of a concern and power dissipation is not so strongly constrained further away from the interaction point and outside of the eta coverage of the detector system. Good noise performance, at close to ambient temperature, is required from the sensor and readout electronics. In addition, the PIXEL detector will be exposed in the environment of the STAR experiment to a moderate radiation (mostly caused by pions) up to about 30 krad per a year of operation.

The MAPS development for the STAR application is divided into four stages.

1. A small prototype based on MAPS architecture with a rolling shutter readout, radiation tolerant charge collecting diode, and pixel readout through a source-follower. The chip provides serial analogue readout of all pixels constituting the array. (MIMOSTAR2 prototype completed by 2006.);

2. A half-reticule sensor with the same properties as above. The chip features the readout and integration time of 4 ms. (MIMOSTAR3 prototype completed by 2007.)

3. A full size (full-reticule) sensor (2 cm × 2 cm). (MIMOSTAR4 prototype to be completed by 2008.);

4. the ultimate sensor for PIXEL that would be capable of working in the increased luminosity of RHIC II. The chip features include: short integration time of about 200 μs, binary readout, and on-chip zero suppression. (To be completed by 2010.)

6.2 Sensor requirements for the PIXEL detector

The performance of a MAPS detector depends strongly on signal to noise ratio that, in turn, depends strongly on the operating temperature. The charge collecting diode is the most sensitive part of a sensor. At higher temperatures the leakage current of the charge collecting diode increases, resulting in higher shot noise, especially for long integration times. Another mechanism responsible for increase of the leakage current is radiation damage. High operating temperature together with radiation harsh environment will have a critical impact on performance of a sensor.

Tests aimed at assessing the efficiency of air cooling were performed on a mockup ladder that had been designed at LBL and equipped with full MIMOSA V size sensors (see Chapter 7.1). Uneven heating profile designed into the heater in the cable was used to simulate temperature gradient across the sensors surface that is expected due to the grouping of digital and readout parts of a sensor at the edge of a die.

The test results show that silicon is a very good heat conductor and, despite of an uneven heating profile, the chip temperature remains uniform within about 1 °C over the whole surface [98]. In the case of no air cooling and power dissipation of about 80 mW/cm^2, the chip temperature reaches 53 °C limited by natural heat convection in air. The same study shows that any air flow of a few meters per second has a significant impact on the silicon temperature and can effectively limit the operating temperature of a chip. Figure 6.1 shows the rise of the chip temperature above ambient as a function of cooling air velocity. The velocity of 3 m/s is sufficient to limit the temperature rise to about 8°C above the ambient temperature. The expected operating temperature of an air cooled sensor that dissipates about 100 mW/cm^2 is at the level of 30 °C.

Radiation damage near the Si-Si0_2 interface leads to increased surface leakage current as described in Chapter 2.2.3. The effect of positive charge buildup in the silicon oxide layer is proportional to the oxide thickness. The thick oxide (field oxide) is inherently present in the diode surroundings as the result of silicon oxidation in one of the CMOS processing steps [22]. A cross section through a typical n-well/p-epi diode is presented in Figure 4.7(a). The field oxide region extends everywhere except for under transistor gates and on top of highly doped n+ and p+ regions. In these regions only thin oxide is grown and it is inherently less susceptible to the ionizing radiation damage due to its limited thickness. Typically thickness of thin/gate oxide is on the order of several nanometers compared to a few hundreds of nanometers for field oxide.

The sensor for the PIXEL detector designed in a standard CMOS process needs optimization of the charge collecting diode to minimize the radiation induced leakage current increase. The optimization of diode layouts tested in the MIMOSA IX prototype, showed that removal of the thick layer of silicon oxide from the vicinity of the charge collecting diode has an important impact on the leakage current [62].

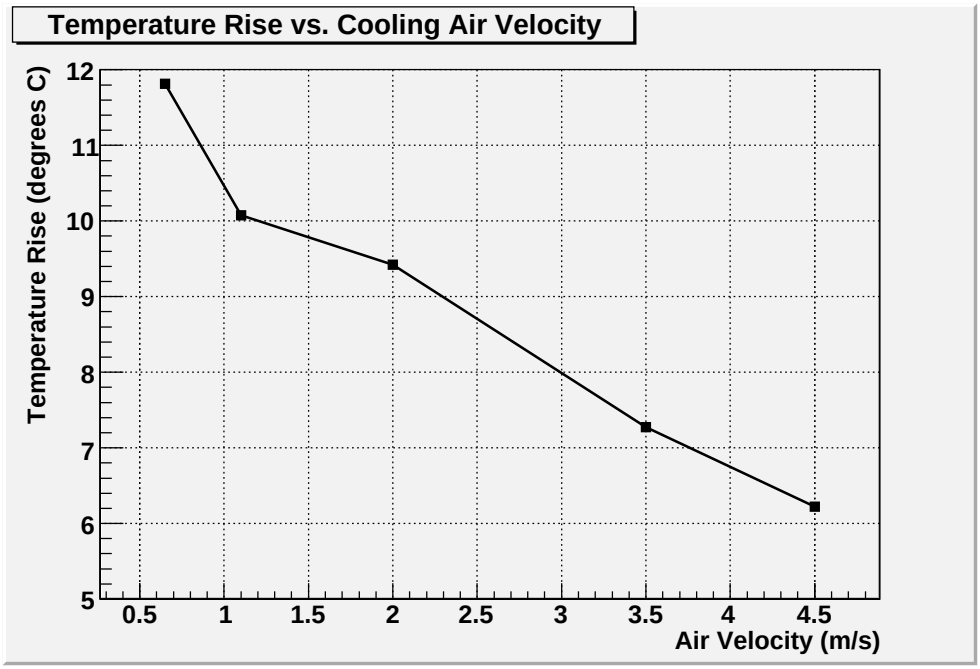


Figure 6.1: Temperature rise as a function of cooling air velocity measured on a prototype ladder design. The test was performed with full-reticule size dummy MAPS dies dissipating power of about 100 mW/cm^2.

To increase design immunity against ionizing radiation damages, it is necessary to eliminate as much of field oxide from the diode's surrounding as possible. A layout technique compatible with this approach is descried in [99]. A diode layout based on this idea has been proposed for the STAR PIXEL detector and is presented in Figure 6.2. The regions of field oxide are eliminated from the vicinity of the diode by introducing additional p+ regions near the n-well edges and by adding polysilicon gate outside of the n-well. Creating a design with a polysilicon gate that

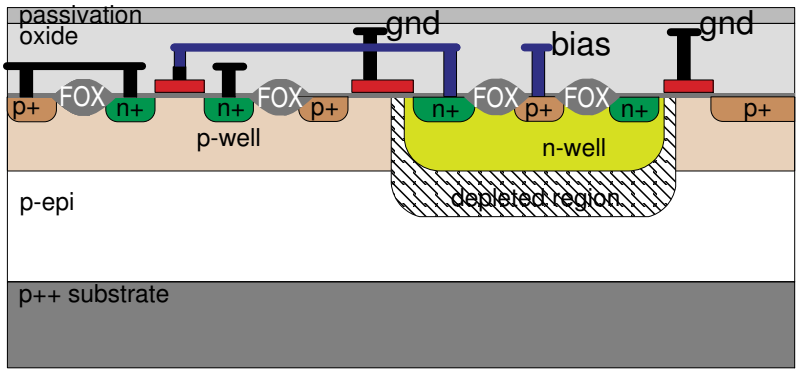


Figure 6.2: Cross section view of the self-biased diode with enhanced radiation tolerance implemented in the MIMOSTAR prototypes. The improvement of radiation tolerance is achieved through elimination of the thick (field) oxide (FOX) from the vicinity of the diode, as presented in Figure 4.7

is not part of a transistor is not a standard design technique. The improvement of performance is significant as can be seen from Figures 4.7(c) and 4.7(d). The leakage current of the standard diode increases significantly after integrating a 20 krad dose. For 4 ms integration time and at 30°C (the expected operating conditions at STAR), the shot noise contribution increases from about 12 electrons for a non-irradiated sensor to almost 40 electrons.

6.3 Evaluation of MIMOSTAR1 and MIMOSTAR2

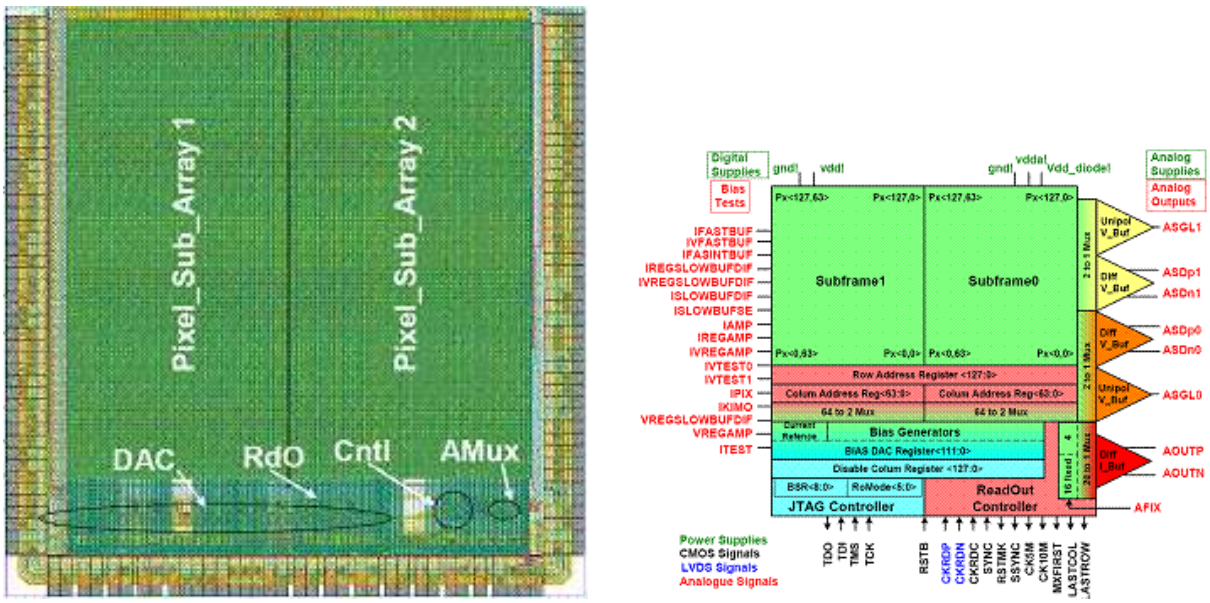
The STAR vertex detector upgrade, which was originally planned for 2009, calls for a sensor that can operate at ambient temperature and with a moderate ($\leq$ 4 ms) integration time. This is challenging mostly for the design of the charge collecting diode as this part is most sensitive to radiation damages and leakage currents. Power dissipation is yet another concern as it can deteriorate the noise performance by increasing, through the temperature effect, leakage currents. Fast analog outputs are sufficient for reading out a complete sensor array in about 4 ms and, therefore, the on-chip data sparsification is not required.

The first prototype, MIMOSTAR1, contains a simple pixel structure based on the self-biased charge collecting diode and two transistors for the readout, all optimized for radiation tolerance. The chip operation is controlled with the industry standard boundary scan JTAG interface[1]. This interface allows the access to internal registers of the chip, including the readout mode selection register and bias registers controlling internal DACs. This architecture minimized the number of external connections that is extremely important for the PIXEL system integration. The first prototype was fabricated in the TSMC 025 technology and, as it will be shown and explained later, turned out to be malfunctioning. To validate the architecture of the sensor it was translated to a different technology. The technology of choice was AMS035 OPTO, which had proven to be reliable for MAPS prototyping. Since MIMOSTAR1 and MIMOSTAR2 used the same architecture, only MIMOSTAR2 will be described.

MIMOSTAR2 is a Monolithic Active Pixel Sensor prototype dedicated to the upgrade of the STAR vertex detector foreseen for 2007. The layout and functional diagram of the chip are presented in Figure 6.3 The matrix is composed of 128 $\times$ 128 pixels with a 30 μm pitch and based on the self-biased diode structure. It is organized in two matrices, or sub-frames, of 128 lines $\times$ 64 columns, accessed in parallel during the readout. Each matrix contains a different pixel architecture. The first one is the *standard pixel* that has already been tested in different prototypes. The second pixel type is a new structure which should meet the radiation tolerance and the low leakage current requirements. The structure implemented as the radiation tolerant design was chosen based on the MIMOSA IX and MIMOSA XI test results. MIMOSTAR2 is a "downsized" prototype which emulates the final circuit of MIMOSTAR4 that is foreseen for 640 $\times$ 640 pixels grouped into 10 sub-frames of 640 lines $\times$ 64 columns. The access to pixels in each sub-frame is sequential and progresses from the upper left corner to the lower right corner of the sub-matrix. Analogue data are extracted via a selectable set of analogue buffers. The selection between serial and parallel readout of the two sub-matrices is provided. A set of selectable analogue buffers allows reading data in three different ways:

- Serial output of the multiplexed data through a differential, current output buffer. A readout speed of 50 MHz is supported.

[1] Joint Test Action Group - IEEE 1149.1 Rev 1999



(a) chip layout

(b) functional diagram of the chip

Figure 6.3: MIMOSTAR chip - layout, (a), and a functional schematic diagram, (b). The pixel array of 128×128 pixels is divided into two sub-arrays read out in parallel. Most of the biasing voltages and currents are generated with internal DACs that are controlled through the JTAG interface.

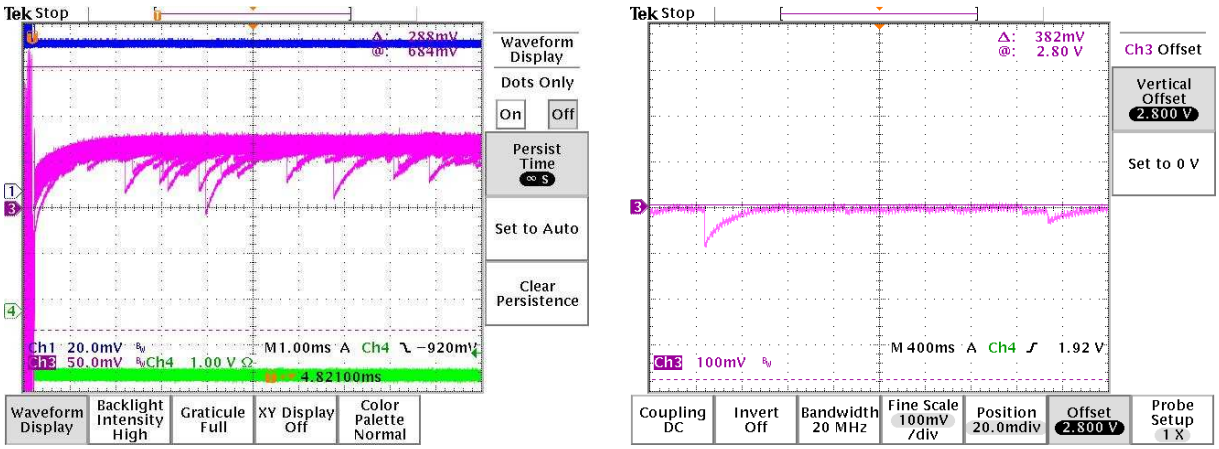
- Parallel output of the two matrices through differential, voltage output buffers (up to 10 MHz).
- Parallel output of the two matrices through single-ended, voltage output buffers (up to 10 MHz).

6.3.1 MIMOSTAR1 performance

A direct measurement of the leakage current on MIMOSTAR1 diodes revealed a moderate value for the standard diode design (0.9 fA per diode at 25°C) and a short circuit on the radiation tolerant design.

The first measurements of the MIMOSTAR1 chip with an iron source indicated problems with the charge collection process. Observation on an oscilloscope screen of the analog signal from a single pixel proved that the discharge time was much faster than expected. A graph of the discharge of a self-biased structure in a standard cell in the MIMOSTAR1 chip is shown in Figure 6.4(a). The observation was performed on one pixel by stopping the clock signal driving the chip during the readout sequence. Signals from several readouts are visible. An exponential fit to the discharge curve reveals the time constant of about 0.4 ms. This fast discharge time, compared to the goal integration time of 4 ms, prevents the operation of the chip at the nominal readout speed.

The discharge time for the self-biased structure is controlled by the time constant of the RC circuit formed by the high resistance (TΩ) of the forward biased diode and the capacitance of the charge collecting diode. Therefore, for a given capacitance of the reverse-biased diode,



(a) MIMOSTAR1 @ -10 deg (b) MIMOSTAR2 @ 30 deg

Figure 6.4: Signal discharge time in MIMOSTAR1 and MIMOSTAR2 observed for photons from an ^{55}Fe source. The measured signal discharge time was on the order of 1 ms in MIMOSTAR1 and 400 ms in MIMOSTAR2.

the equivalent resistance of the forward biased diode is critical. The value of the resistance may differ depending on the technological process and might also be related to the layout of the diode, including its size and spacing to other elements. In addition, increased current flowing through the forward biased diode will reduce its equivalent resistance. This current is the leakage current of the reverse-biased diode and, therefore, independent of the parameters of the forward-biased diode. Summarizing, the RC constant will depend on the process in which the structure is fabricated and on the n-well/p-epi diode leakage current that varies with temperature.

The diode in the MIMOSTAR pixel has a capacitance of about 8 fF. For the proper operation of the chip with an integration time of 4 ms, the full recovery time should be more than 40 ms ($\sim 6\tau$). The equivalent resistance of the forward biased diode can be estimated ($\tau = RC$) at about 0.8 TΩ. At the same time, the measurement shows that the equivalent resistance of the forward biased diode in the MIMOSTAR1 chip is close to 50 GΩ, too small by more than one order of magnitude.

The MIMOSTAR1 design was translated to the AMS 0.35 technology to validate the architecture of the sensor. Figure 6.4(b) shows a discharge/recovery time measurement performed with the MIMOSTAR2 chip. The discharge/recovery time observed varies with the temperature but in all cases is more than one hundred times longer than for MIMOSTAR1 and allows for proper registration of the signal deposited by photons from the ^{55}Fe source used for calibrations. Exponential fit to the presented curve indicates a time constant on the order of 0.15 s at 30 °C that increases to 1.16 s at 10 °C. The resistance of the forward biased diode is $R \geq 10$ TΩ .

Figure 6.5 shows histograms of signals induced by an ^{55}Fe source in the MIMOSTAR1 and MIMOSTAR2 chips. The histograms were obtained for seed pixels with the cut on S/N$\geq$5. The differences between two histograms include a slightly different gain in the two systems and different statistics collected. One of the histograms was scaled up and overlaid on the other in order to make a qualitative comparison of the observed distributions. The result obtained for MIMOSTAR2 is a classical calibration histogram, where two peaks corresponding to 5.9 and

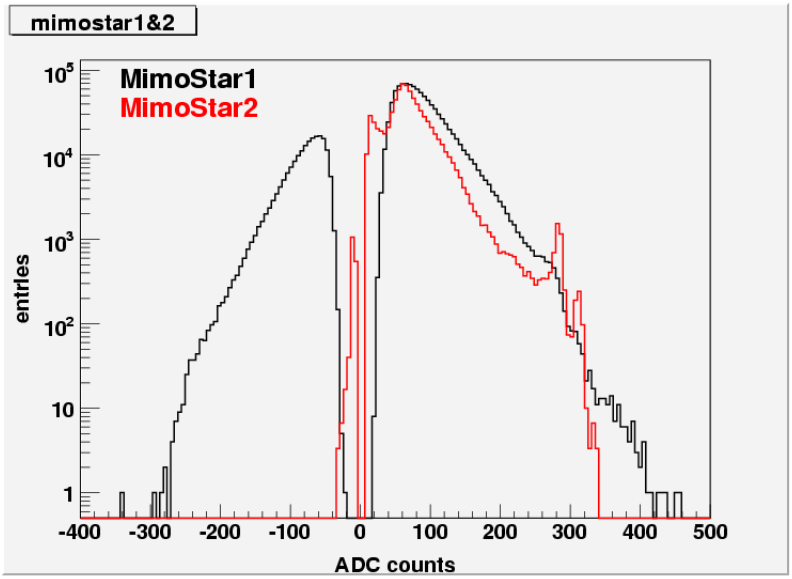


Figure 6.5: Comparison of ^{55}Fe signal spectra collected with MIMOSTAR1 and MIMOSTAR2 prototypes. The histograms are built with CDS processed data. In the case of MIMOSTAR2, the negative entries in the histogram originate from noise fluctuations. In the case of MIMOSTAR1, the large number of negative entries can be explained by a short signal discharge time.

6.4 keV photons are clearly visible. At the same time no peak was observed for MIMOSTAR1. Values below zero were obtained in a non-standard analysis for cases where subtraction of two samples resulted in negative signal with the absolute value that was sufficiently large to pass the cut. The distribution of hits with negative amplitudes results from the fast discharge time. Under normal conditions, the second registered sample should have the amplitude either lower, after a hit is registered, or close to the reference sample. With a short discharge time, the amplitude of the second sample can be significantly higher than the reference level (refer to Figure 3.9). Typically, negative hits should be the very small fraction of events that correspond to high temporal noise fluctuations.

6.3.2 Pixel-to-pixel dispersions in MIMOSTAR2

Pixel-to-pixel dispersion cannot be avoided on large scale devices. It becomes a critical factor for efficient signal processing performed on-chip. Evaluation of the pixel-to-pixel dispersion on MIMOSTAR2 chip is important for the development of sensors dedicated to the PIXEL detector. For some processes, including the AMS0.35 OPTO, there are no Monte Carlo models for diodes. Therefore, a complete pixel-to-pixel dispersion cannot be estimated based on simulations. Only measurements can quantify this effect.

In MIMOSTAR2, only dispersion in the complete readout channel can be measured. This includes the diode, the source-follower transistor, and amplifiers located downstream. The rms value for the DC voltage level of 8192 pixels was measured to be approximately 30 mV (300 mV peak-to-peak), after taking into account all gain in the readout channel. A dependency of the

dispersion on temperature has been observed. The aforementioned voltage level was measured at 30 °C, while the rms value decreases from about 50 mV at 0 °C to about 25 mV at 40 °C. This could suggest that increased leakage current compensates for diode-to-diode dispersions. The measurement was performed on two chips and no significant variation between the chips was observed.

The result can be compared with pixel-to-pixel dispersions of the source follower transistor. The measurement was performed on a prototype in which the diode could be disconnected from the readout chain. This prototype, MIMOSA XI, provided three sub-matrices, each with pixels arranged into 30 rows and four columns. The total number of tested pixels was 360. Results show that the rms values quantifying dispersions are at the level of 5-7 mV (20-29 mV peak-to-peak). This suggests that dispersions observed on MIMOSTAR2 prototypes are dominated by differences at the diode level. This conclusion should be taken cautiously, as the pixel arrays had significantly different sizes on both prototypes (360 pixels vs. 8192). This example shows clearly that for successful implementation of on-chip data processing/sparsification an efficient way of removing FPN is of paramount importance.

6.3.3 MIMOSTAR2 - ^{55}Fe calibrations

The performance of the MIMOSTAR2 chip was studied carefully to evaluate its compliance with the PIXEL detector requirements. The sensor underwent a series of laboratory tests at different operating temperatures and after different ionizing radiation doses. The calibration procedure was performed for a non-irradiated chip and for 3 different doses (10, 20, 50 krad)[2] at three different temperatures (20, 30, 40 °C).

The improved performance of the radiation tolerant design is clearly visible in Figure 6.6. As is shown, the predicted ionization dose in the STAR environment in three years of the detector operation slightly degrades the performance of the radiation tolerant structure. At the same time, the influence of increased temperature has a negligible effect on the shape of histograms. In the same conditions, the performance of the standard diode design is significantly deteriorated. For high temperature and high radiation doses the structure loses almost all charge due to the fast discharge process. The performance degradation of this simple architecture is significant and disqualified its use in the STAR environment. Loss of charge and increase of noise can be summarized by ENC that is presented in Figure 6.7 as a function of temperature and ionizing radiation dose. The curves in this plot show that the satisfactory level of about 15 e^- ENC can be reached with the radiation tolerant design for doses that do not exceed 20 krad and for temperatures of about 20 °C. At higher temperatures and for higher doses, the detection efficiency of the sensor is expected to decrease due to the increased number of accidentals generated by higher noise. The charge losses observed in the standard structure at high radiation dose and high temperature can be attributed to increase of the leakage current. Large leakage current leads to a faster signal decay that can remove part of the signal before the sample is registered.

The observed performance degradation can be compared to the MIMOSTAR1 case, where the low diode resistance resulted in a very fast signal removal. The plot in Figure 6.8 represents the same phenomenon for MIMOSTAR2 as Figure 6.5 for MIMOSTAR1.

[2]the 50 krad dose takes into account a safety margin of approximately two.

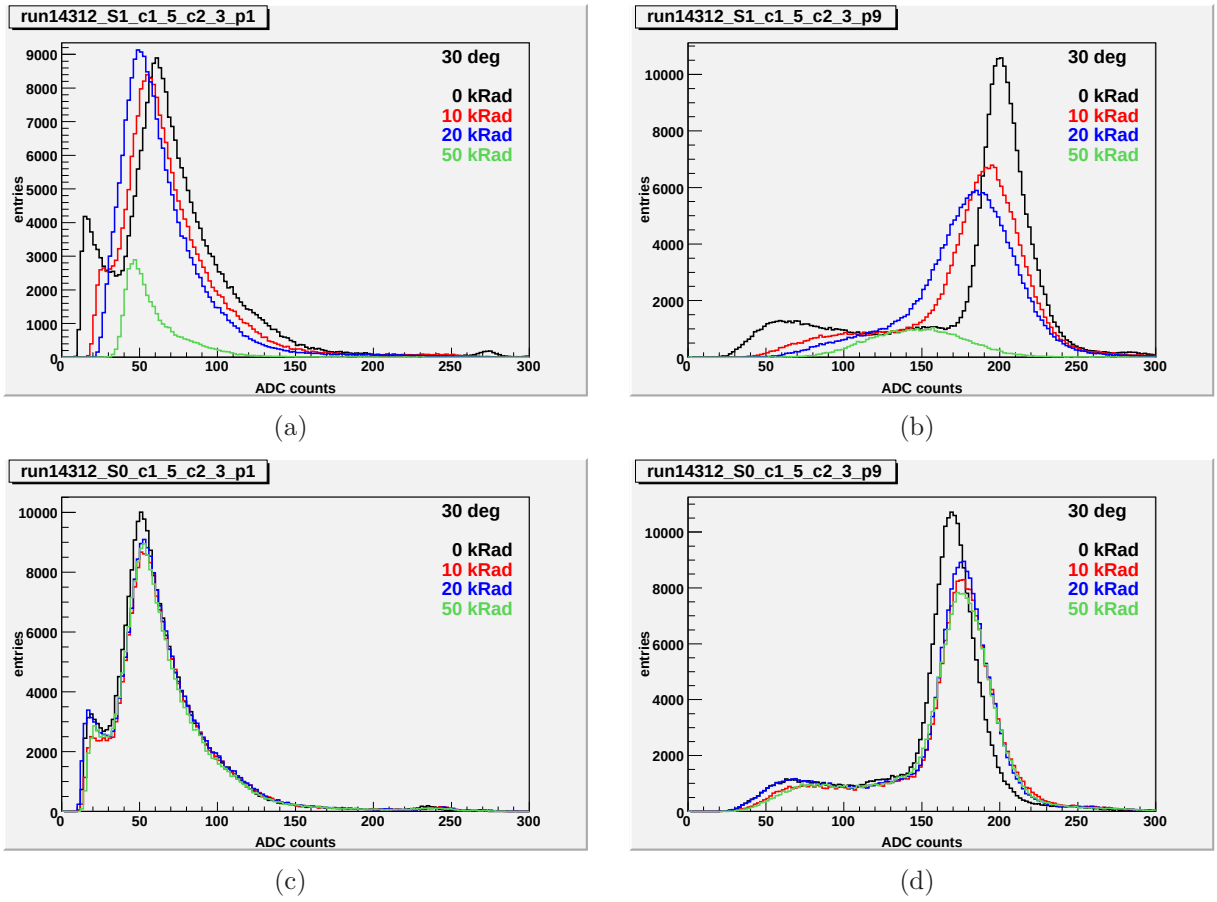


Figure 6.6: Calibration and cluster peak displacement as a function of radiation dose and temperature. Figure (a) and (b) show histograms for the standard structure, while figure (c) and (d) for the radiation tolerant design. Signal distributions on seed pixels are presented in figures (a) and (c) and nine-pixel cluster sums in figures (b) and (d). Results for additional temperature points are presented in Appendix D in Figure D.1.

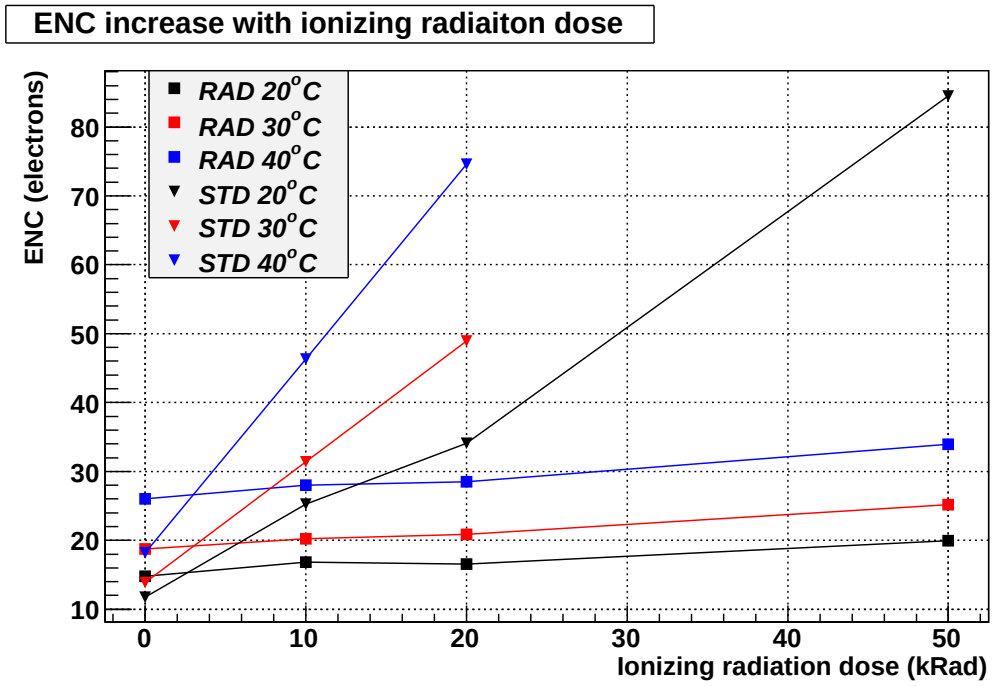


Figure 6.7: MIMOSTAR2 ENC as a function of radiation dose and temperature. Standard diode design provides a smaller leakage current in a non irradiated sensor but it quickly degrades with an ionizing radiation dose. Radiation tolerant diode starts with a higher noise but exhibits a relatively small increase of the leakage current with the integrated radiation dose.

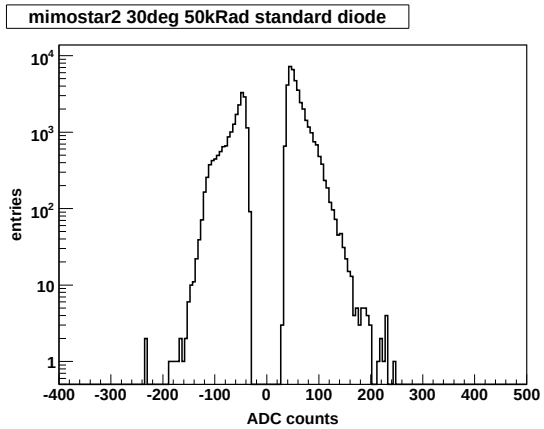


Figure 6.8: Signal spectrum measured with the MIMOSTAR2 standard diode array at 30°C and after accumulating the total ionizing dose of 50 krad.

6.3.4 MIMOSTAR2 - beam tests

Laboratory tests with an ^{55}Fe source are limited to the measurement of the charge conversion gain, ENC, and charge collection efficiency. Additional tests with a test beam at a dedicated facility are required to evaluate sensor response to minimum ionizing particles. MAPS prototypes developed at IPHC are typically tested using high-energy particle beams at CERN or DESY. The performance of the MIMOSTAR2 prototype was evaluated at DESY. The electron/positron synchrotron DESY-II test-beam area is schematically depicted in Figure 6.9(a). The electron beam is first converted to bremsstrahlung on a 10 μm carbon fiber target (primary target) and then is converted into electron-positron pairs on aluminum or copper targets of various thicknesses (secondary target). The momenta of electrons and positrons are selected with a bending magnet with a maximum of about 7 GeV before the beam is delivered to the testing hall through a collimator slit. The MIMOSTAR2 chip was tested with high energy electrons of 5 GeV at the DESY facility.

The tested prototype was mounted inside a high precision silicon reference telescope used for reconstruction of particle tracks [100]. The telescope, schematically presented in Figure 6.9(b), consists of eight planes of high-precision silicon microstrip detectors (single sided, AC coupled)

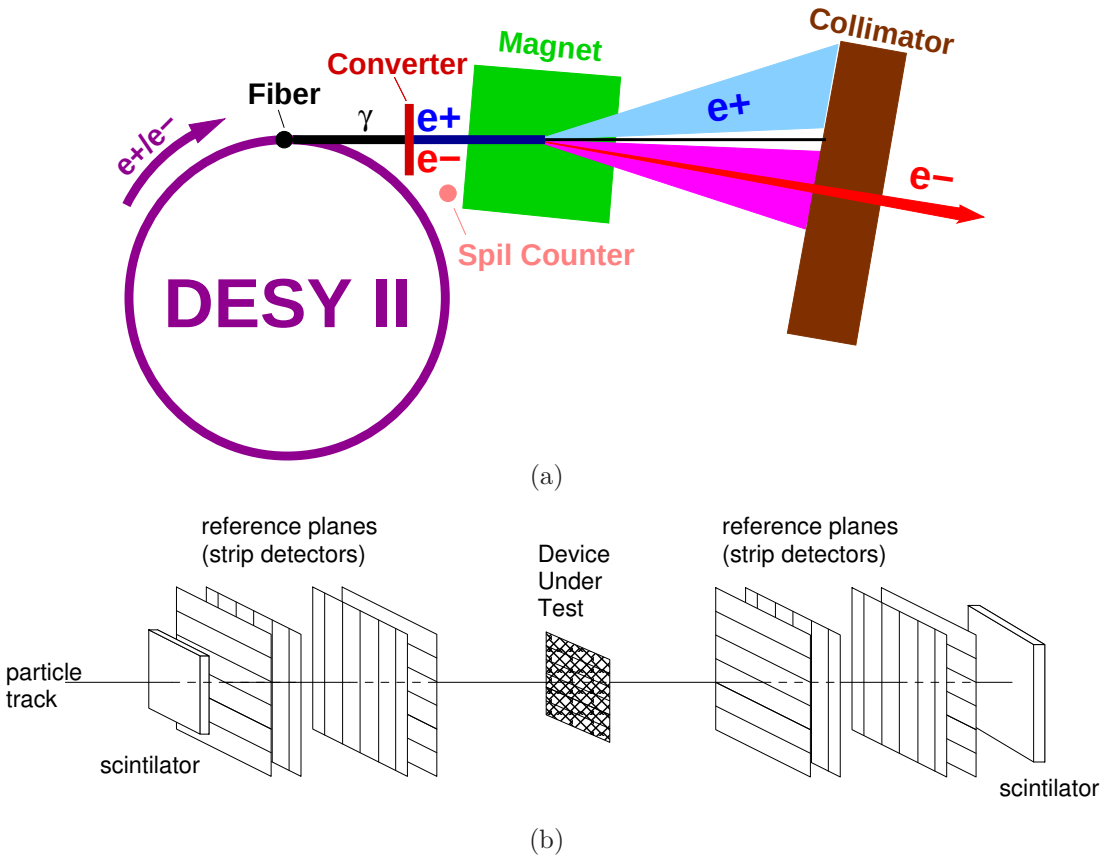


Figure 6.9: Schematic layout of a test beam at the DESY facility, where MIMOSTAR2 was tested with a 2 GeV electron beam, (a), and a simplified diagram of the silicon telescope used for tests of MAPS prototypes with MIP test beams (b).

with the size of 12.8 mm×12.8 mm and the thickness of 300 μm each. The strip pitch is 25 μm, while the readout pitch is 50 μm, i.e. only one strip out of two is read out. The sensors are fully depleted at a bias voltage of 60 V. The reference detectors, arranged in four pairs (planes), provide particle position in two orthogonal coordinates, XY, perpendicular to the beam axis, Z. The reference detector provides a signal over noise ratio higher than 100 and a point position with the precision of 0.7 μm in both coordinates, with a 98.7% efficiency.

The device-under-test (DUT) is mounted in parallel to the reference detectors. DUT is placed in a thermally isolated box on a support that provides cooling fluid flow for controlling the temperature of the tested device. Two scintillator pairs, with an active area of 2×2 mm^2 and 7×7 mm^2, are located at each end of the telescope. A coincidence between the two scintillator pairs generates a trigger signal that is used for reading out and storing data from all detector planes. The data acquisition system for the telescope is based on VME PowerPC as described in Chapter 3.2.3. The imager boards digitize data from the DUT and reference detectors. Digitized data is sent for archiving to a Linux PC via an Ethernet link. The speed of the system is typically limited by data transfer rates through the Ethernet link and write accesses to hard drives. Recorded data is typically analyzed off-line using a ROOT based program.

The data analysis procedure reconstructs particle trajectories from the reference planes and interpolates the particle impact point onto the prototype under test. To achieve tracking, alignment of all detector layers, including the tested prototype, needs to be performed in a common reference system. The alignment procedure estimates three parameters for each detector plane, i.e., the offsets in X and Y dimensions and the rotation angle around the beam axis. Parallel mounting perpendicular to the Z axis is assumed and Z coordinates for all layers can be measured. All other parameters are determined by minimizing the distance between the measured and predicted hit positions. Two internal pairs of the strip detectors are considered as reference planes. All other layers are aligned one after another with respect to the system coordinates. DUT is aligned last. The next few paragraphs give a brief description of the analysis procedure, while details can be found in [101, 102].

The alignment procedure corrects for two offsets and the rotation angle. This is achieved by plotting the residuals versus the predicted hit position. The predicted hit position is calculated under the assumption that the trajectory of any particle is a straight line. This holds true since the tests are performed without any electromagnetic field that could bend particle tracks. The other effect that could introduce deviations form a straight line is multiple Coulomb scattering. However, the scattering in sensor planes does not significantly affect the alignment procedure[3] for the given telescope geometry with the strip pitch of 50 μm and typical pixel sizes of 20-30 μm. The plot of residuals versus predicted hit position can be fitted with a linear function with coefficients corresponding to the rotation angle and the offset. Using the method of least squares, one finds that the coefficients satisfy two linear equations. Solving the equations yields the values for the offset and the rotation angle.

Hits within a given search window are considered for track calculations. The window is large at the beginning to detect large offsets but it also accepts background hits. To minimize errors introduced by background hits, the alignment procedure is iterative and in each iteration the search window is reduced. Typically several iterations are needed for a precise alignment.

[3]This is not true for measurements of the detector resolution. The multiple Coulomb scattering will significantly degrade the measured resolution if a beam of low energy particles is used for testing.

The results obtained with two MIMOSTAR2 prototypes are presented in Figure 6.10. Two sensors (Chip2 and Chip4) were readout through parallel single-ended outputs with 2 MHz and 10 MHz main clock frequencies, corresponding to integration times of 4.2 ms and 0.8 ms, respectively. Tests were performed at temperatures ranging from 0 to 40 °C. The subplots in Figure 6.10 show detection efficiency, S/N for the MPV, noise expressed in electrons, and charge collected in central pixel, all as a function of temperature. These results and laboratory tests show that variations observed between chips are insignificant. Noise performance is satisfactory at temperatures below 30 °C, where noise of less than 16 electrons can be achieved even for a 4 ms integration times required by the PIXEL detector. Any noise increase translates directly to a decrease of S/N to about 14 at 30 °C. The signal-to-noise ratio, combined with cluster search criteria (central pixel $S/N > 5$ and sum of S/N for 8 neighboring pixels larger than 2), results in high detection efficiency of more than 99.6%. At higher temperatures (40 °C), noise increases to more than 20 electrons, which decreases the S/N to about 10 and deteriorates efficiency to about 98.5%

If the PIXEL detector is operated with the 4 ms readout time, at the ambient temperature of $20 - 25$ °C, and the sensors are cooled with airflow of 2-3 m/s then the silicon should reach temperatures of about 30 °C. In these conditions, the detector with non-irradiated sensors should provide a detection efficiency of more than 99.0%.

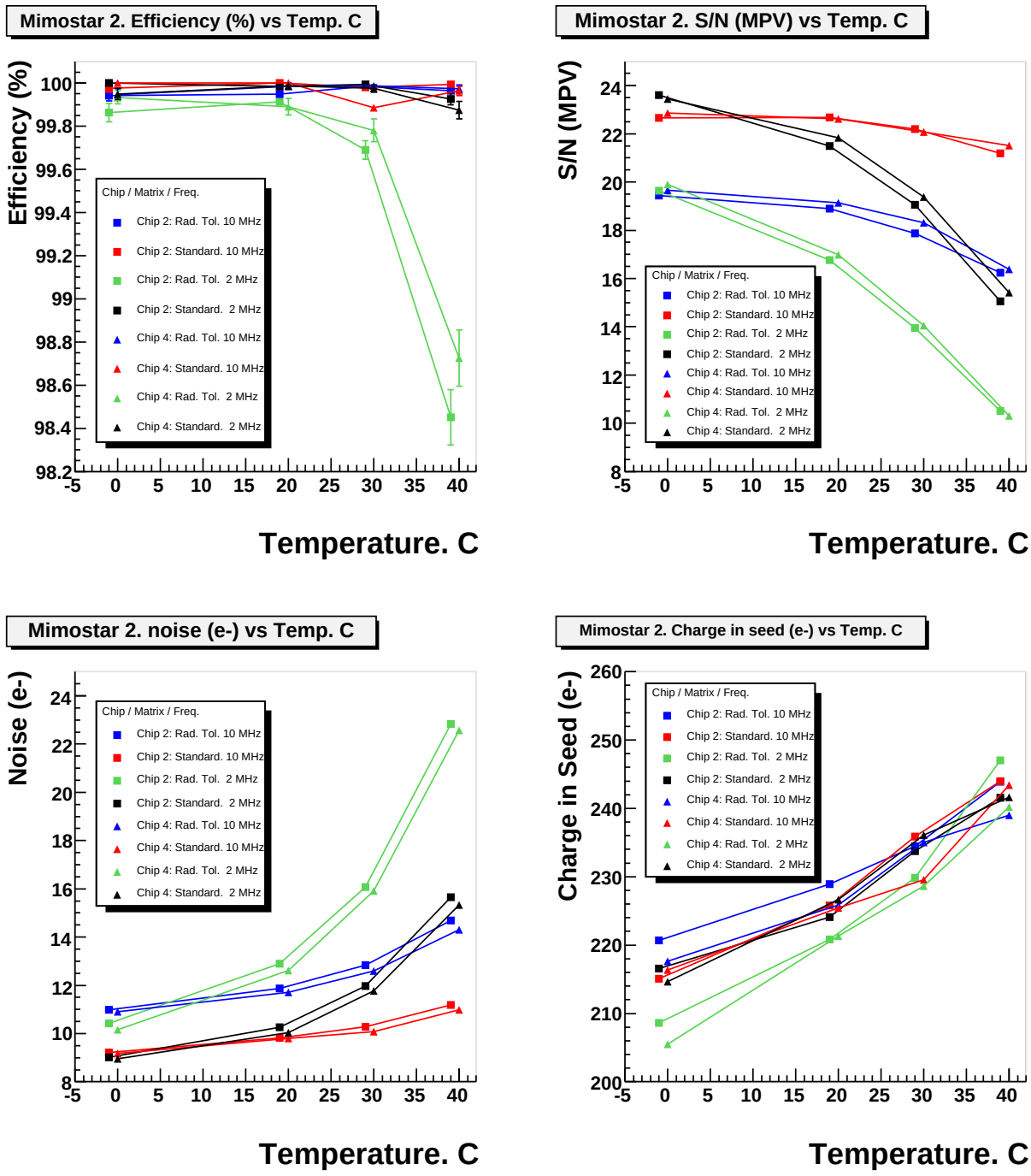


Figure 6.10: MIMOSTAR2 beam tests results for standard and radiation tolerant diode designs at two integration times: 0.8 ms and 4.2 ms. Upper left corner - detection efficiency as a function of temperature; Upper right corner - the most probable value of the signal-to-noise ratio for a MIP as a function of temperature; Bottom left corner - Input-referred noise as a function of temperature; Bottom right corner - The average charge deposited by a MIP in the central pixel of a cluster as a function of temperature.

6.3.5 MIMOSTAR2 - latch-up tests

Operating a sensor in a harsh radiation environment can result in a latch-up condition. Particles most likely to cause latch-up events are those depositing large amount of energy in silicon, for example highly ionizing low energy protons. The ongoing physics simulations that try to evaluate the amount of energy deposited in the detector material in the STAR environment ([102]) are performed with the GEANT detector description and simulation tool [103]. Early simulation results indicated that the expected latch-up rate in the detector could be at the level of one every few seconds. The simulation is especially sensitive to the ratio of the active to passive detector layers [104]. Recent tests with MAPS at the STAR environment (see Chapter 7.4.4) indicate that the actual latch-up cross section should be expected to be significantly lower.

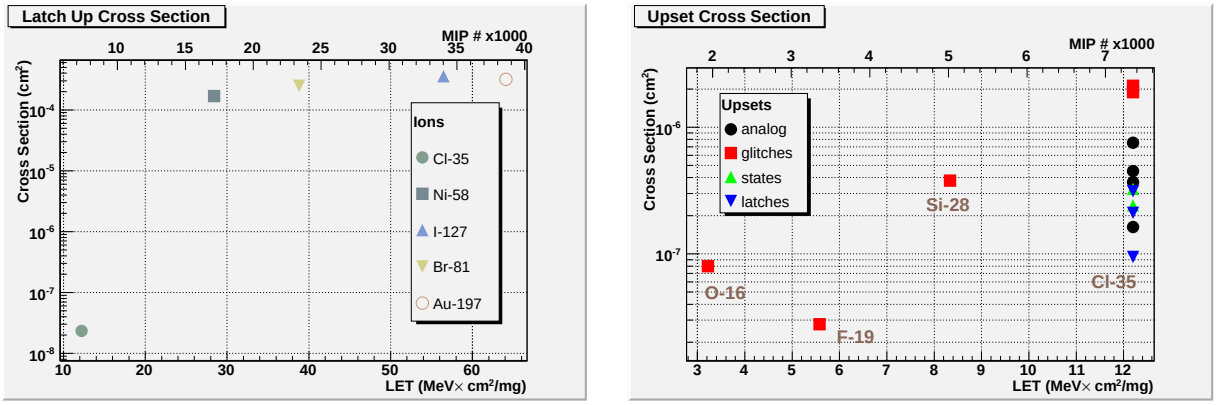
The tests of sensitivity of the MIMOSTAR2 prototype to single event upsets were focused on the latch-up effect. One chip was placed in a controlled environment in which the unfavorable conditions could be reproduced. The Single Event Upset Test Facility at BNL's Tandem Van de Graaff Accelerator Facility [105] provides the user with a flexible and user friendly system for investigating single upset failures. Different ion species are available for producing a uniform beam of ions with a defined flux and energy. Latch-up cross section is calculated based on the number of registered latch-up occurrences in the given exposure time.

Test setup

A MIMOSTAR2 chip was mounted to a test PCB and placed inside a vacuum tank. The complete setup used for latch-up tests is presented in Appendix D, Figure D.3. Latch-up condition is easily detected from the increase of current consumption by the chip due to the generated low resistance path between two areas with different potentials. The laboratory power supplies used for powering the chip were set with a relatively low over current protection. The voltage was continuously monitored with a small DAC/ADC card and a simple LabView based control interface that could connect/disconnect power supply by switching fast solid state relays. Increase of the current consumption above the threshold set resulted in a decrease of the voltage on the chip power supply and was considered a latch-up event. The chip digital power was supplied with 8 V bench supply regulated on the test card to 3.3 V, with the current limit set to 340 mA. The chip analog voltage was supplied at 3.3 V with the current limit of 40 mA. In response to a latch-up, the LabView software disconnected the power supplies from the chip. After powering down the chip, the software restores power to the chip and reinitializes MIMOSTAR2 operation. Two operating modes were foreseen:

1. Detecting latch-up failures in the digital part only - the operation of the chip was initiated by sending reset signal generated from the USB-6800 DAQ. The clock signal, CLK, and frame synchronization signals were constantly delivered by the USB2 Imager Card. This assured proper operation of the digital part of the chip.

2. Detecting latch-up failures in the analog and digital part - the operation of the chip was restored by reprogramming/reloading full JTAG sequence. JTAG programming was initiated by the control software when a TTL signal from the USB-6800 DAQ was received in the parallel port of the control PC. This procedure assured proper operation of both the analog and digital parts of the chip in between latch-up states.



(a) (b)

Figure 6.11: Cross sections for latch-up, (a), and observed upsets, (b), in the MIMOSTAR2 prototype as a function of LET and the number of MIPs.

A scan with different ions was performed to measure the latch up cross-section of MIMOSTAR2. Initially, for low Linear Energy Transfer, LET[4], values of about 3, 5, and 8 MeV $\cdot$ cm^2/mg, corresponding to 0-16, F-19, and Si-28, no upsets were observed. For high energy beams with LET of 12, 28, 38, 56, 64 MeV$\cdot$cm^2/mg (Cl-35, Ni-58, Br-81, I-127, Au-197, respectively) a number of latches was registered. The test results are summarized in Figure 6.11(a), where cross sections are presented as a function of LET (bottom axis) and as a function of the corresponding number of MIP particles(top axis). LET can be converted to MIPs, assuming 1.66 MeV $\cdot$ cm^{2}g^{-1} for a single MIP.

When the beam of Chlorine ions was used, in addition to the well defined latch-up conditions, a set of upsets was observed on digital marker signals generated by the chip and on the screen monitoring the analog signals readout from the chip. This led to an additional scan focused on soft upsets using ions with low LET. Results with "glitches"[5] are presented in Figure 6.11(b). A dependency on LET was observed; however, no quantitative conclusions can be drawn due to the limitation of the test setup.

In some of the tests a number of upsets, resulting in relatively low current consumption increase, were observed. For example, observing the power supplies controls, two or three gradual increases of the current were recognized before the system was capable of detecting a latch-up condition. Unfortunately there was no possibility to measure these events in an automatic way due to the limited sensitivity of the test system.

The latch-up cross section measured in these tests is between $2 \cdot 10^{-8}$ and $2 \cdot 10^{-7}$cm^2 for LET close to 12 MeV$\cdot$cm2/mg. Soft SEU with a cross section of about $2 \cdot 10^{-7}$ to $7 \cdot 10^{-7}$ cm^2 for the same LET value were also observed. There is a slight indication that a soft SEU might exist

[4]Linear energy transfer is a measure of the energy transferred to material by an impinging ionizing particle. It is used typically to quantify the effects of ionizing radiation on biological specimens or electronic devices.

[5]shifts in the digital marker pattern were referred to as glitches and changes in marker frequency (also pulse width) were referred to as "states". If a visible change in analog signal resulted it was classified as "analog" upset. However it is important to note, that "analog" upsets could result from upsets in the digital part of the chip as a consequence of modified settings.

for lower LET, but judging from the results presented such a conclusion can not be considered reliable.

The setup used for these tests had a number of shortcomings. The main limitations came from:

- the monitored power supply was common for the chip and readout electronics on the PCB. The power consumption of the fully operational setup (chip with correctly set internal biases) was 320 mA compared to 280 mA for the chip with only digital part operating. The over-current limit was set to allow operation of the chip with full functionality. Manual control of this threshold did not provide sufficient accuracy to detect small increases in current consumption.

- single event upsets observed in the test were unexpected. The available tool did not provide functionality for automatic measurements of this phenomenon. Consequently, the numbers obtained for these upsets have to be treated with caution.

In the future, the tests should be repeated with a much more robust setup that will overcome these limitations.

The next step required to complete this study is to examine the environment present at RHIC in the PIXEL detector location. The number for the latch-up cross section needs to be referenced to the real operation conditions before the validity of the chip design can be confirmed. The digital part of the MIMOSTAR2 prototype was designed using classical standard cells. If the environment at RHIC can lead to latch-up or soft errors in current prototypes, the new generation of MAPS for PIXEL will have to be designed with an increased radiation tolerance of the digital section of the chip. The improved latch-up tolerance can be achieved using radiation tolerant techniques, as described in Chapter 2.2.3, for designing standard cells. One of the simplest approaches is to increase spacing between PMOS and NMOS transistors to augment value of the shunting substrate path and well resistance.

6.4 Summary of MIMOSTAR2 tests

The failure of the MIMOSTAR1 prototype can be attributed to the parameters of the self-biased structure implemented in the TSMC 0.25 process. Nevertheless, the TSMC process is suitable for MAPS manufacturing as proven by other prototypes, including MIMOSA VIII. It is important to note that the implementation of the self-biased structure in the MIMOSA VIII prototype was successful. The obvious differences between the two prototypes include different technology runs and small differences in diode sizes (0.8×0.8 μm^2 in MIMOSTAR1 and 1.1×1.1 μm^2 in MIMOSA VIII). The effects of smaller effective resistance can also be reduced for short integration times. In the case of the MIMOSTAR1, however, even an integration time similar to the integration time in tests with the MIMOSA VIII AC pixel prototype (400 μs at 5 MHz input clock) would not solve the problem. In addition, a self-biased structure can be implemented by replacing the forward biased diode with a more complex and larger transistor in a diode configuration, which would eliminate the use of a p+/nwell diode structure.

The extensive studies of the MIMOSTAR2 prototype performance validate the choices of the technology and sensor architecture. Sensor tests with ionizing radiation integrated up to a 50

krad dose clearly indicate the improved radiation resistance with the radiation tolerant diode design. Increasing the radiation dose degrades the noise performance of a sensor operated at 30°C (the expected operating temperature of the PIXEL detector) from about 17 electrons to about 25 electrons ENC. Detection efficiency, measured in beam tests on a non-irradiated sensor, degrades at these noise values from above 99.8% to approximately 98.5%. Significant improvement can be obtained by lowering the operating temperature by several degrees. A considerable loss in efficiency should be expected when the temperature increases to 40°C. Additional detection efficiency tests were performed with irradiated MIMOSTAR2 sensors at the CERN SPS test beam. Results will soon be available. At this time it can be stated that new results are consistent with the ones presented throughout this chapter.

The latch-up cross section measured for the MIMOSTAR2 prototype was $2 \cdot 10^{-7}\text{cm}^2$. Combining the measurement result with detector physics simulations should provide an estimation of the expected latch-up rate for the PIXEL detector in the HFT. Early simulation results indicated that a latch-up event could occur every few seconds. It has been observed in recent tests performed in the STAR environment ([106], and see Chapter 7.4.4) that the actual rate can be expected to be lower.

The presented characteristics of the MIMOSTAR2 prototype indicate that the PIXEL detector equipped with the full size sensors (MIMOSTAR4) would meet the detector requirements for the 2009 run.

Chapter 7

PIXEL detector ladder and readout system

The data flow path from MAPS constituting the PIXEL vertex detector to an acquisition system requires dedicated sensor development, described in previous chapters, and a compatible readout system that manages transfers of large amounts of data. In the following section, architecture of the readout system, including an algorithm for reducing the amount of data sent from the sensors to the acquisition system, is presented and validated with a 3-sensor telescope prototype.

7.1 Ladder Design

The PIXEL detector is a complex design that requires not only sensor development but also a serious effort on building the mechanical structure for supporting the sensors. Mechanical design is beyond the scope of the work presented in this thesis, but several aspects influencing MAPS optimization will be mentioned. Constraints on the PIXEL detector include:

- power dissipated by chips and the resulting thermal stresses and cooling requirements;
- minimized radiation length, especially in the required eta coverage ($-1 < \eta < 1$). This is the eta coverage of the outer tracking detectors. The radiation length per detector layer is required to be less than 0.5% but a value as low as 0.25% is desired;
- two layers of detectors with each layer providing close to 100% space coverage, with only 20-50 μm gaps in lithography between stitched sensors;
- movable and modular structure of the detector that enables replacing the detector or its modules on a short time scale while all other detector systems are in place;
- mechanical positioning system has to guarantee position of pixels in the internal coordinate system with a precision on the order of 20 μm to take advantage of the high precision delivered by MAPS;
- each of 10 sensors located on a ladder requires two differential twisted pair cables for reading out signals. All control and readout signals will be delivered to sensors with a 4-layer Kapton cable with aluminum conductors.

Ladder Architecture

First ladder prototypes have been designed and fabricated by Leo Greiner at LBL (Figure 7.1). The ladder cross section is presented in Figure 7.2 and properties of all layers are summarized in Table 7.1. Conductors in the Kapton cable have been chosen to be Aluminum. This choice had been guided by the fact that the copper, typically used for PCB traces, has a radiation length that would double the overall radiation length of the ladder. The support for sensors uses a rectangular block of reticulated vitreous carbon foam (RVC) reinforced on both sides with thin layers of unidirectional carbon fiber composite. Such structure allows achieving sufficient stiffness while providing low radiation length.

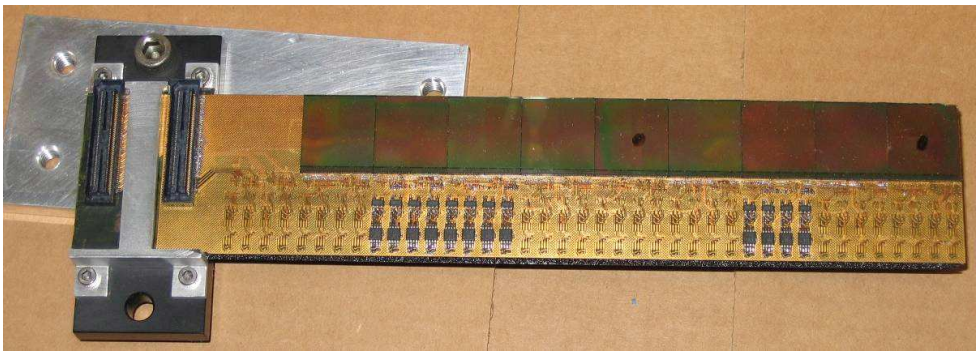


Figure 7.1: A prototype PIXEL ladder design fabricated on a copper conductor cable and populated with nine full-reticule size MIMOSA V sensors thinned to 50 μm. Three sensors had all four sectors fully operational. The prototype was constructed at LBL.

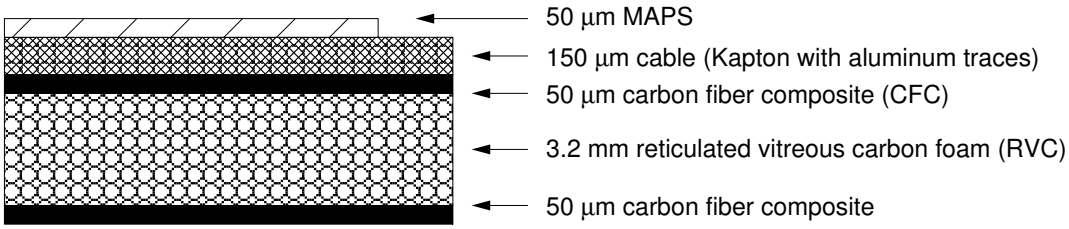


Figure 7.2: Expected composition of the PIXEL ladder.

Table 7.1: Constituents of conceptual design of one PIXEL ladder

component	% radiation length	Si equivalent (μm)
silicon	0.053	50
adhesive	0.014	13.39
cable assembly	0.089	83.92
adhesive	0.014	13.39
Carbon composite	0.11	103
TOTAL	0.28	264

The ladder design criteria affect the sensor architecture to some extent. The number of signal paths and the complexity of signal connections in the readout cable are limited by the low mass requirement. Therefore, only a limited number of signal lines per chip can be provided in the cable. This requires sensors to be designed with a few outputs per sensor, at the most. This is not a significant limitation in the case of moderate readout times available in the first series of MIMOSTAR prototypes. However, for the ultimate design, where parallel readout architecture provides short readout/integration times, it becomes critical to limit data throughput by implementing on-chip data sparsification. The data sparsification will guarantee data flow that can be handled with a reasonable speed on a limited number of outputs.

7.2 Detector readout

Important part of the sensor readout chain is external electronics. Naturally, the complexity of external electronics is inversely proportional to the processing power built into sensors. In the case of MAPS, integration of complex processing circuitry into sensors increases insensitive area and power consumption.

Construction of a prototype readout system for the PIXEL detector was necessary to validate the approach chosen for the detector architecture. The requirements for the prototype and final PIXEL readout system are very similar. They include:

- Triggered detector system fitting into the existing STAR infrastructure and interfaces to the existing Trigger and DAQ systems;
- Deliver full frame events to STAR DAQ for event building at approximately the same rate as the TPC;
- Reduce the total data rate of the detector to a manageable level (below TPC rate).

A prototype data acquisition system for the PIXEL detector has been designed at LBL. The system provides readout of large amounts of data for individual MIMOSTAR4 sensors followed by signal digitization and data compression. Sparsified data organized into events is sent for storage. Reading out the MIMOSTAR4 sensor in 4 ms and digitizing its analog signals with 12-bit ADCs will yield approximately 1.2 Gb/s per sensor chip. The complete detector with 330 sensors works with data rates on the order of 50 GB/s. A synchronous cluster finding algorithm that reduces data to addresses of central pixels in 3×3-pixel clusters created by impinging particles was introduced to reduce this enormous amount of data to a manageable rate. The expected data rates are presented in Figure 7.3. The numbers are calculated based on detector physics simulations that show 53.9, 10.75, and 8.76 hits/cm^2 expected in layers at 2.5, 6.5, and 7.5 cm radii from the center of the beam pipe, respectively[1]. The data rate at the PIXEL detector output, after cluster finding and zero suppression, is expected to be on the order of 115 MB/s.

It is crucial for the readout chain to have an efficient cluster finder algorithm that allows the detector to achieve high detection efficiency while minimizing the accidental hit rate. The

[1]The total rate includes charged particles and UPC electrons. For the inner layer of the detector it is 37 charged particles and 15.9 UPC (ultra peripheral collision) electrons while for the two outer layers the numbers are 1.46+0.29 and 8.66+0.1 correspondingly

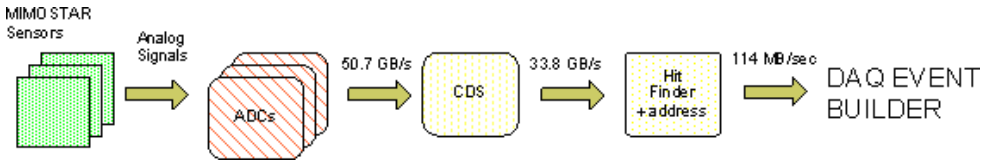


Figure 7.3: Data rates in the prototype PIXEL detector with a full frame readout time of 4 ms.

study of a cluster finding algorithm that was proposed for PIXEL is presented next. It will be followed by a description and test results of a scaled down version of the prototype PIXEL readout system.

7.3 Cluster finder algorithm

Integrated operation of the MIMOSTAR prototypes together with the rest of the readout chain envisaged for the PIXEL detector is of utmost importance. The performance of the complete system is significantly influenced by the cluster finding algorithm used for reducing the amount of information to be readout and stored. Two different cluster finding algorithms that could be used in the PIXEL readout system were studied by estimating single-hit detection efficiency and fake-hit rate as a function of different threshold criteria. To estimate these characteristics, a set of simulations was performed using real data generated with MIMOSTAR2 prototype pixel sensors.

Cluster finder algorithm

A commonly used cluster-finding algorithm is based on two cuts on signal-to-noise ratio (S/N): the first cut is on the central pixel and the second cut on the sum of S/N of all eight neighbors (often referred to as a crown). The S/N for the crown is calculated as the ratio of the sum of signals of individual pixels divided by the square root of quadratic sum of noise values. Typical threshold values are 5 and 2 for the central pixel and the crown, respectively. It provides very good detection efficiency and effectively filters accidentals caused by noise. This algorithm can easily be implemented in software. Implementation in hardware, either in a signal processing FPGA or on-chip, is possible but would require significant resources. In addition to multi-bit adder blocks, large blocks of memory are necessary to store the average noise value for each pixel.

A simpler algorithm was proposed for the implementation in the readout system of the PIXEL detector [107]. A cluster would be recognized when the signal in a central pixel passes a high threshold and, at the same time, at least one of the eight neighbors passes the second, lower threshold. The cuts are applied only to registered signals as opposed to the typically used S/N ratio.

Data used for testing of the algorithm

The study was performed using real data obtained by the IPHC group with a MIMOSTAR2 prototype. The data sample as collected in beam tests that took place in summer 2006 at DESY,

with a prototype operated at 20 °C and the integration time of 2.1 ms. The data used for the simulation consisted of 1897 5×5-pixel clusters[2] extracted as hits associated with particle paths reconstructed in MIMOSTAR2 and reference detectors. Another part of data was 4193 regions of 5x5 pixels containing noise signal extracted from a reference run taken without a beam and in the same running conditions. As a result of off-line processing, all signals in clusters were presented in electrons with a conversion rate of 7.1 e^-/ADC. All data was converted into ADC units for the simulation purposes. Standard deviation for noise samples was 2.14 ADC. The most probable value of signal in the central pixel of a cluster was approximately 30 ADC.

The data input into simulations contained clusters embedded into background signal. Events with a frame size of 15×15 pixels were formed from noise data, with the central 5×5 region replaced by a single signal cluster. To study fake-hit rate at the 10^{-6} level, the initial 104825 noise samples were used for generating 1.2 million noise samples. A pseudo-random number generator randomly selected samples from the initial set of data and built the large set used in the simulation. The distribution of the generated set of data was in agreement with the distribution of the original noise samples. The complete set of data used in this study consisted of 7588 frames and each signal cluster was used 4 times.

The efficiency reached with this approach needs to be scaled by the cluster reconstruction efficiency for the beam test data. However, this efficiency was above 99.98%, and for all practical reasons it can be assumed to be 100%.

Definitions

In the study of the cluster finding algorithm presented here, the following definitions are used for detection efficiency, eff, and fake-hit rate, FHR:

$$eff = \frac{N_{org}}{N_{TOT}} \times 100 = \frac{N_{org}}{N_{FRAMES}} \times 100 \quad [\%] \tag{7.1}$$

N_{org}- number of clusters detected in the original central 5x5 regions of all input events, N_{TOT} - the total number of clusters embedded in the central regions of input events equal to the number of frames ($N_{FRAMES} = 7588$).

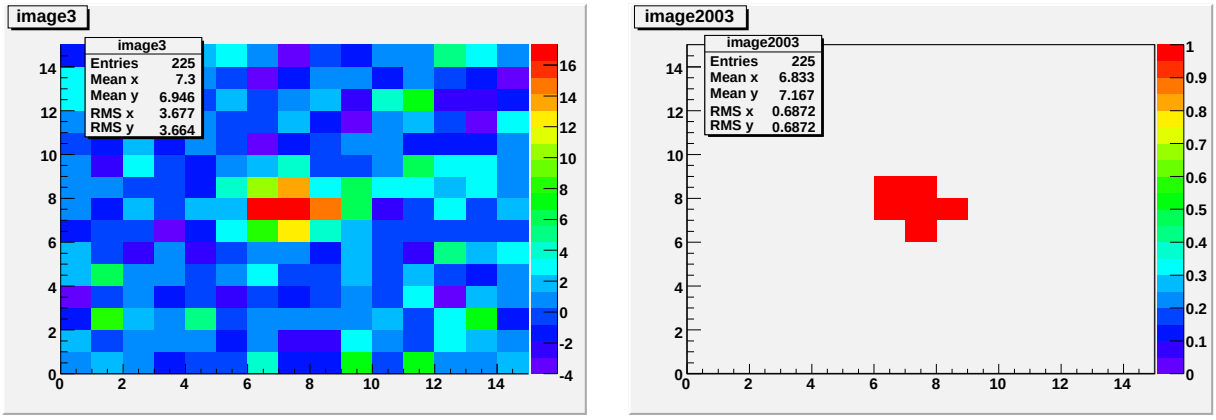
$$FHR = \frac{N_F}{N_{FRAMES} \times N_{PIX}} = \frac{\sum_{frames} (n_{det} - n_{org})}{N_{FRAMES} \times N_{PIX}} \tag{7.2}$$

N_F - number of fake clusters, n_{det}- number of clusters detected in one frame, n_{org}- number of clusters detected in one frame at the position where the original cluster was embedded, N_{PIX} =160 - number of pixels in one frame that are scanned for clusters, excluding the central cluster of 9 pixels and one row/column at each frame edge.

Procedure

Each frame was scanned with a 3×3-pixel window. The central pixel is considered as the center of a cluster when the cluster criterion is met. This can result in a number of pixels marked as belonging to one cluster. An example of this procedure is presented in Figure 7.4.

[2]Charge generated by an impinging particle is shared between several adjacent pixels. Cluster size of 5x5 pixels is large enough to enclose all pixels that collected charge.



(a) (b)

Figure 7.4: An example of pixel array images before and after applying the cluster finding algorithm.

Reconstruction of a cluster from a group of pixels was accomplished using a flood-fill algorithm. The binary image of the pixel array is raster scanned and when the first pixel of a cluster is found, the flood-fill algorithm is called. The algorithm checks if the neighboring pixels are part of the cluster in the following order:

1. next pixel in the same line,
2. pixel in the next line that is immediately below the starting pixel,
3. previous pixel in the same line,
4. pixel in the next line and in the next column,
5. pixel in the next line and in the previous column.

Starting with the initial pixel, the flood-fill algorithm is called recursively any time the next pixel of the cluster is identified. At the same time, the pixel that initiates the algorithm is ”cleared” and can not be counted again. The operation of the algorithm and the order of finding pixels are shown in Figure 7.5. The highlighted pixels that create a cluster are numbered in the order in which they are identified. The centroid of each cluster has to be found to estimate the hit position. A similar algorithm will be required for processing data from the PIXEL detector.

The distance between the hit position estimated from the center of mass of the original cluster and the centroid of a reconstructed cluster has the distribution presented in Figure 7.6. The mean value is compatible with a binary resolution that is expressed by Equation 7.3, derived from Equation 2.24.

$$\sigma = \frac{p}{\sqrt{12}} \tag{7.3}$$

where p is pixel pitch that, in this case, is normalized to 1.

The size of a cluster depends on the high cut on the central pixel. The average cluster size as a function of a cut on the central pixel is presented in Figure 7.7(a) and it varies from 4 to 2.6 pixels for lower and higher cuts, respectively.

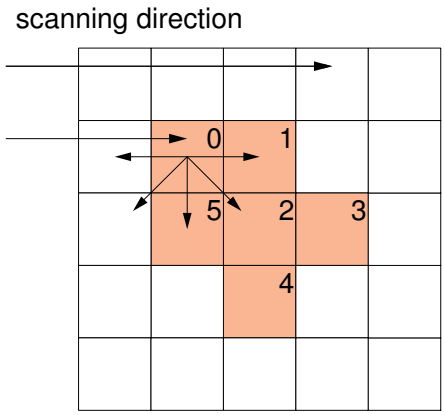


Figure 7.5: Flood-fill algorithm for merging neighboring pixels into a single cluster.

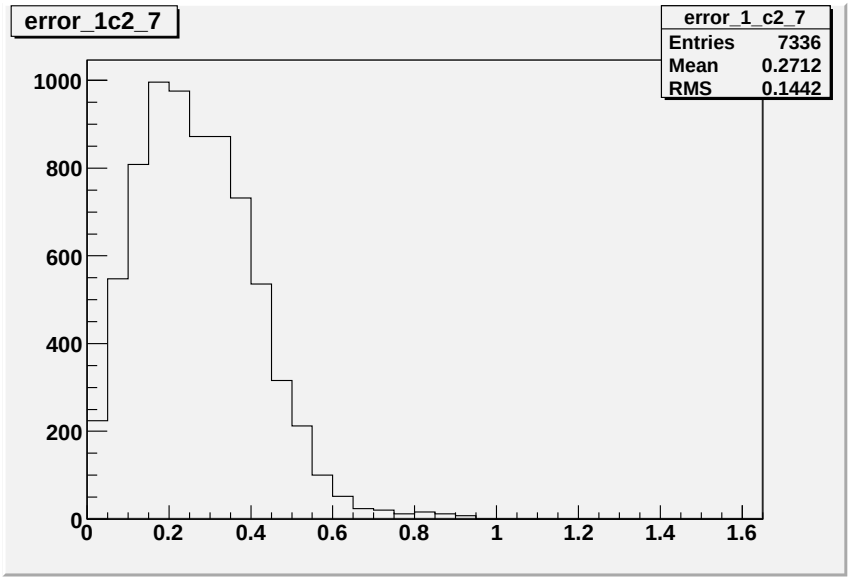
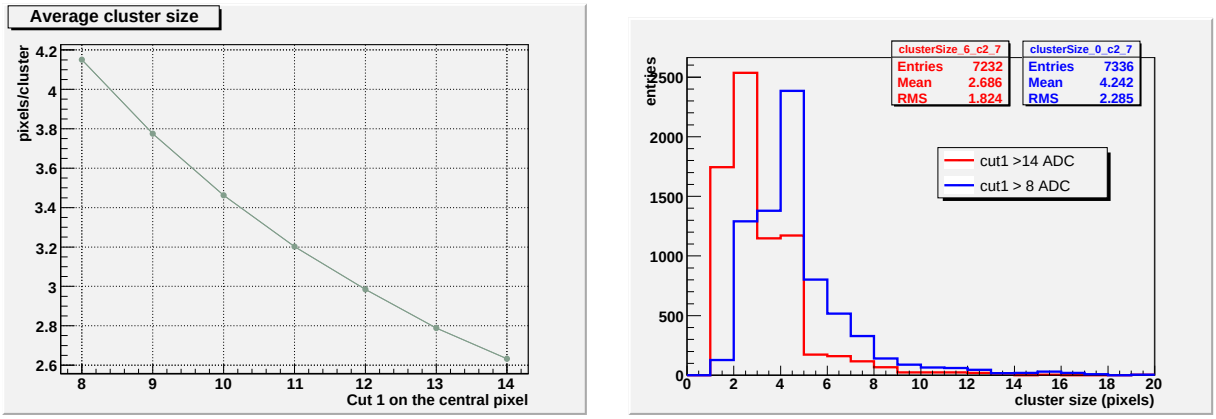


Figure 7.6: The distance between the center of mass for the original cluster (12 bit resolution) and the centroid of the reconstructed cluster.



(a) (b)

Figure 7.7: Average number of pixels in a cluster as a function of the high cut on the central pixel in the studied cluster finding algorithm, (a). Cluster size distribution for central cuts at 8 and 14 ADC counts, corresponding to the mean noise value multiplied by 3.7 and 6.5.

Results

Detection efficiency vs. fake-hit rate per pixel for the proposed two-threshold cluster finding algorithm is plotted in Figure 7.8, as function of applied cuts expressed in ADC counts. Figure 7.9 shows the same characteristics for the classical algorithm, where the second cut is performed on the sum of signals in 8 adjacent pixels. The points on the curves correspond to different thresholds applied to the central pixel, varying from 14 to 8 ADC units with a step of one ADC unit when tracked from left to right. Different colors represent different settings for the second cut. The fake-hit rate equal to 10^{-7} is an arbitrary number that corresponds to no fake hits detected.

Satisfactory performance of the PIXEL detector system requires a high detection efficiency ($> 99\%$) and a low fake-hit rate per pixel ($< 10^{-4}$). The two-threshold algorithm discussed above meets these criteria for various pairs of the two cuts, i.e., the center pixel threshold ≥ 10 ADC and low threshold < 5 ADC. This should allow comfortable adjustment of settings that will deliver the desired performance.

Although the classical algorithm based on sums of signals is much more flexible and the range of acceptable settings is much wider, the proposed two-threshold algorithm is more suitable to the PIXEL readout system. This is due to a very good performance achievable with an extremely simple architecture. This simple architecture can be easily implemented in an FPGA, and also seems to be an attractive solution for on-chip implementation. Implementation of this algorithm is certainly worth considering for the ultimate chip for the PIXEL detector that is planned to have a digital readout.

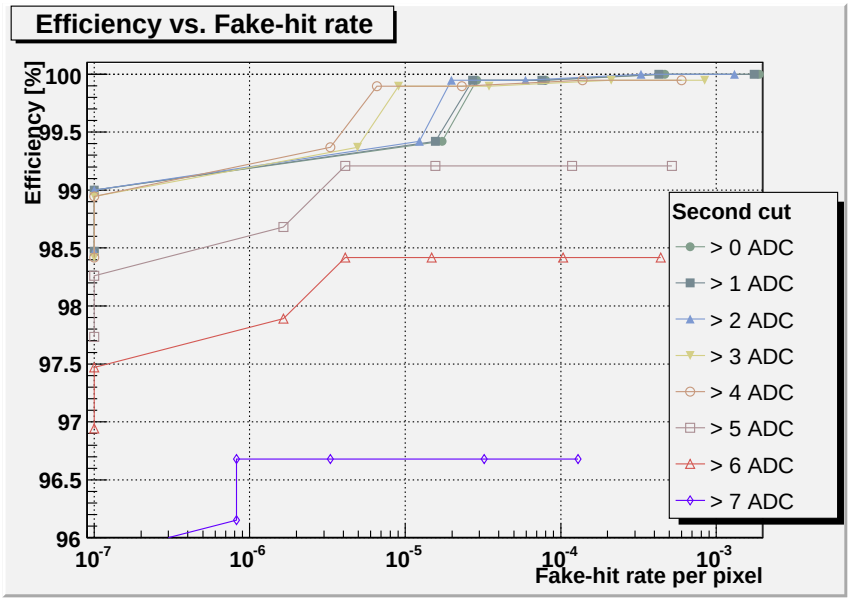


Figure 7.8: Efficiency vs. fake-hit rate per pixel for the cluster finding algorithm based on two thresholds: high cut on the central pixel and lower cut on one of 8 adjacent pixels. Cut on the central pixel varies from 14 to 8 ADC counts for data points from left to right.

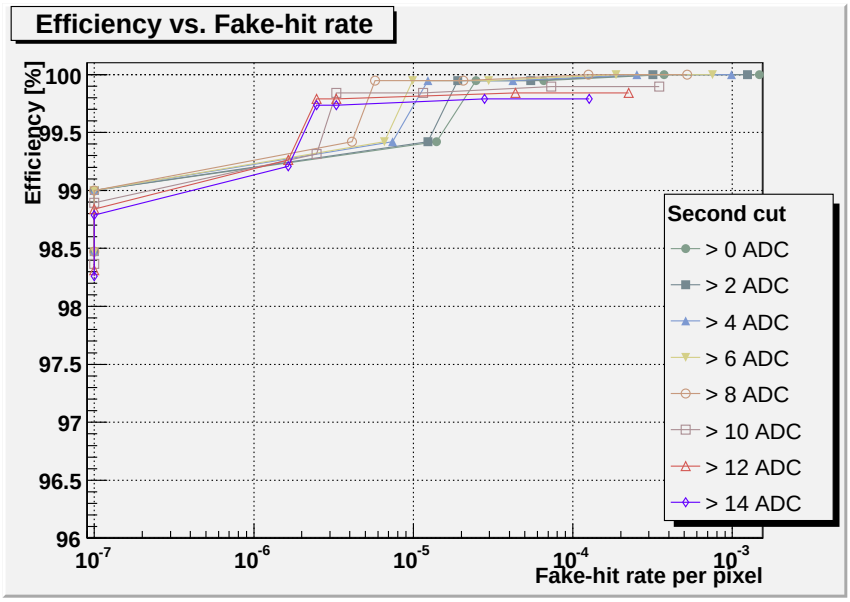


Figure 7.9: Efficiency vs. fake-hit rate per pixel for the cluster finding algorithm based on two thresholds: high cut on the central pixel and the second cut on sum of signals from all of 8 adjacent pixels. Cut on the central pixel varies from 14 to 8 ADC counts for data points from left to right.

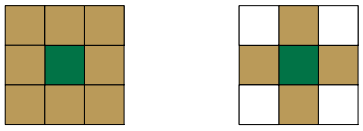
Additional considerations

In this study, a variety of cluster finder algorithms based on two different thresholds was investigated. The considered algorithms had the same cut on the central pixel but different cuts on the neighboring pixels:

- Any one pixel of 8 neighbors passes the lower threshold (described above),
- Any two pixels of 8 neighbors pass the lower threshold,
- Any three pixels of 8 neighbors pass the lower threshold,
- Any 2 adjacent pixels of 8 neighbors pass the lower threshold,
- Any 1 pixel of 4 neighbors passes the lower threshold (Figure 7.10(b)),
- Any 2 pixels of 4 neighbors pass the lower threshold (Figure 7.10(b)).

Compared to the first algorithm, all of them are much more rigorous. The increase of the lower threshold significantly reduces the fake-hit rate, but at the same time the efficiency is severely affected and drops below 99%. A very limited combination of settings would meet the stringent performance requirements.

The most interesting algorithm of those mentioned above is the one that checks the lower threshold against 4 pixels adjacent to the central pixel, as illustrated in Figure 7.10(b). The estimated detection efficiency and fake-hit rate are presented in Figure 7.11. The fake-hit rate decreases by a factor of two, compared with the original PIXEL algorithm, due to the reduced number of scanned pixels per cluster. The improvement is achieved at a small penalty in detection efficiency lowered by approximately 0.1%.



(a) (b)

Figure 7.10: Topology of cluster finding algorithms that check eight, (a), and four, (b), pixels adjacent to the seed pixel.

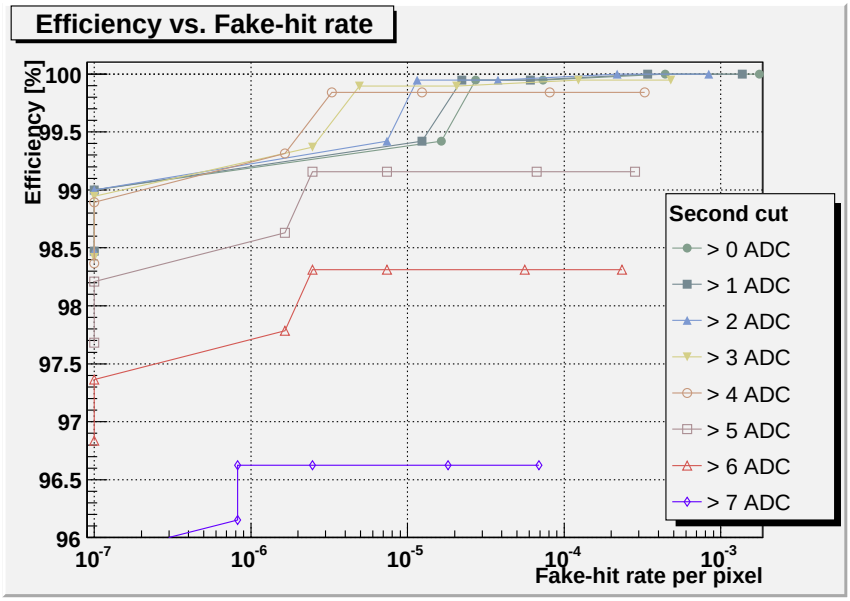


Figure 7.11: Efficiency vs. fake-hit rate per pixel for the cluster finding algorithm based on two thresholds: high cut on the central pixel and lower cut on one of 4 adjacent pixels forming a cross pattern. Cut on the central pixel varies from 14 to 8 ADC counts for data points from left to right.

7.4 Telescope prototype

7.4.1 System architecture

A prototype telescope system comprising three MIMOSTAR2 sensors and dedicated readout electronics, a prototype of the PIXEL detector readout, was built to:

- study the performance of the MIMOSTAR sensors in the STAR environment,
- observe the charged particle environment at STAR,
- verify performance of the cluster finding algorithm,
- verify the performance of the readout hardware and firmware as a complete system, and interfaces to other STAR subsystems.

The prototyped readout system is much simpler than the one of the PIXEL detector but it has the same readout architecture. All the elements of the designed system are scalable to the size of the final detector.

The overview of the system architecture is presented in Figure 7.12. Each of the three MIMOSTAR2 chips is glued and bonded to a dedicated Kapton cable, which has the thickness of 25 μm and two layers of copper. All three sensors are located in a plastic head and fixed

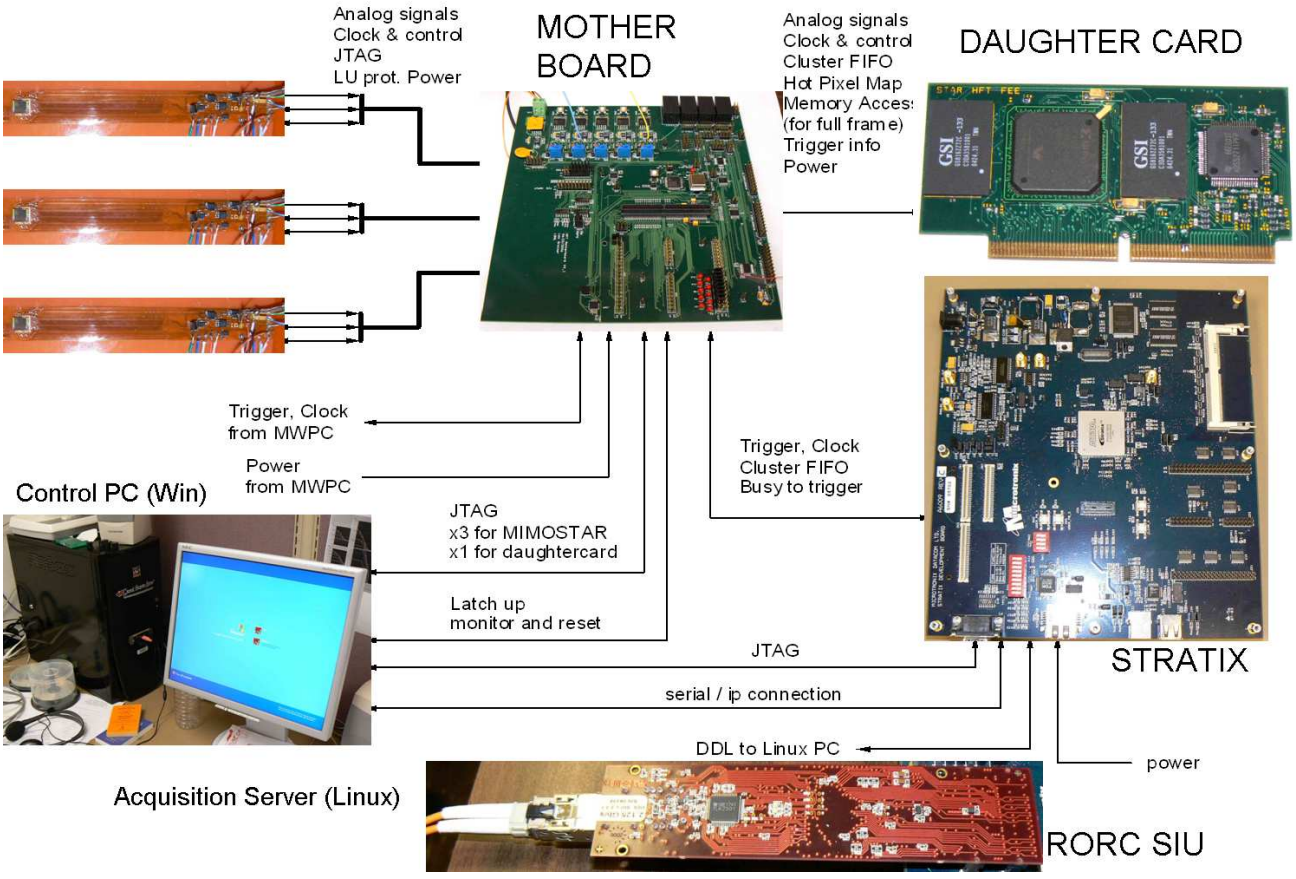


Figure 7.12: Architecture of the telescope prototype constructed with 3 MIMOSTAR2 sensors aligned in parallel.

Figure 7.13: Telescope head structure with three MIMOSTAR2 sensors arranged into parallel and coaxial planes.

with three L-shaped holders that align them into three parallel and coaxial planes (Figure 7.13). The chips are connected to the Mother Board from which they receive power and digital signals needed for their operation. The Mother Board receives clock and trigger signal from STAR trigger subsystem. The resulting dependency of the detector systems makes the prototype telescope a small subsystem of the STAR detector. The analog signals from the MIMOSTAR2 chips are delivered to the Daughter Card that is connected to the Mother Board. The signal processing modules located on the Daughter Card digitize signals and perform zero suppression. The Stratix Development Board provides the control shell and the interface for sending data out through a Detector Data Link (DDL)[3] The data is transferred to the acquisition PC and from there to the STAR DAQ.

The firmware and hardware architecture of the telescope prototype system is schematically shown in Figure 7.14. The three chips, working in parallel[4], are continuously readout and analog signals are digitized with 12-bit ADCs. The chips and ADC's work at 50 MHz, the speed that is compatible with the future full-reticule chip. The digitized data are subjected to subtraction of the consecutive frames (CDS), and then sorted for a raster scan in the cluster finder implementation. The cluster finder returns addresses of central pixels in 3×3 pixel clusters, as discussed in Chapter 7.3. When a trigger arrives, the cluster addresses start to fill a cluster FIFO for one event that lasts the same amount of time as the readout of one full frame. All these functions are implemented in the FPGA located on the Daughter Card. In response to

[3]Digital Detector Link is a system that was developed at CERN for the ALICE readout systems.

[4]The clock and synchronization signal are multi-dropped. This allows chips to be synchronized so that the new readout of the array begins at the same time. This, in turn, allows us to take only one feedback signal to correctly synchronize our readout system. All three chips form a daisy chain for JTAG programming.

a trigger, data from FIFOs[5] are sent to the Stratix FPGA where the event is formed[6] and sent out to DDL and, over the fiber optic connection, to the acquisition PC. The Stratix FPGA is also responsible for providing communication via DDL and for generating the JTAG sequence for programming MIMOSTAR2 sensors. DDL is a part of the STAR DAQ1000 upgrade [108], which focuses on the TPC readout electronics and increasing data rates by a factor of 10 (up to above 1 kHz) combined with elimination of dead time. The use of DDL in the readout system simplifies interface to the STAR system. To provide airflow in the confined volume of the telescope head, a vacuum cleaner based cooling system was used that pulled air in through perforated tip of the telescope head.

The work mode described above is referred to as *normal mode* because of being designed for the full detector readout. Another readout mode implemented in the system is the so-called *full-frame readout*. In this mode, the 12 bit samples registered for a chosen chip are transferred via DDL to the acquisition PC. Data acquisition is limited to a single chip due to the very high data rates associated with this readout mode. The full-frame readout provides an additional tool for chip characterization and an additional mean for verification of the readout system components, especially the cluster-finder. This mode is not compatible with the STAR DAQ format and is exclusively used in the stand-alone operation.

The prototype telescope was subjected to a series of laboratory tests and tests with minimum ionizing particles to verify the performance of the complete system.

7.4.2 Telescope performance

The assembled system was carefully calibrated with ^{55}Fe. The average noise observed for both pixel types was approximately 6.5 ADC counts. The calibration peak was measured at the level of 350 and 300 ADC counts for the standard and radiation tolerant diodes, respectively. These values translate to the ENC of about 30 and 35 electrons at the temperature of 28°C. The unexpectedly high noise value was found to be related to a flaw in the system structure. MIMOSTAR2 was a small size prototype with many outputs intended only for testing purposes. When the telescope system was designed, the layout of the flex cables, to which the chips were to be mounted, was optimized for minimum size and minimum mass as would be expected in the real detector. This resulted in several chip outputs that were left unbonded. Unterminated DAC outputs were responsible for the increased noise level. The only way to fix the problem would be to redesign the Kapton cables. However, this was impossible due to the time constraints on the access time to the test facilities (Advanced Light Source at LBL, and STAR at BNL).

The tests at the Advanced Light Source were performed on a booster ring, which accelerates electrons before injecting them to the storage ring. The access to the beam was possible in the time between fills. The telescope was located in a beam line and exposed to an electron beam with energy of 1.2 GeV. The telescope head was placed perpendicularly to the beam, in a distance of a couple of meters downstream from collimators and bending magnets. Therefore, for small surface sensors, the assumption of the beam perpendicular to sensor planes is justified.

[5]There are five FIFOs per chip; each dedicated to a single event. This allows the system to handle triggers in 1 ms intervals (TPC trigger rate) even though the readout time of the full-reticule sensor is 4 ms.

[6]Data format contains a 64 byte header followed by variable length data section and 4 byte termination word. The information included in the header contains, among other information, a unique STAR trigger token and the system status bits.

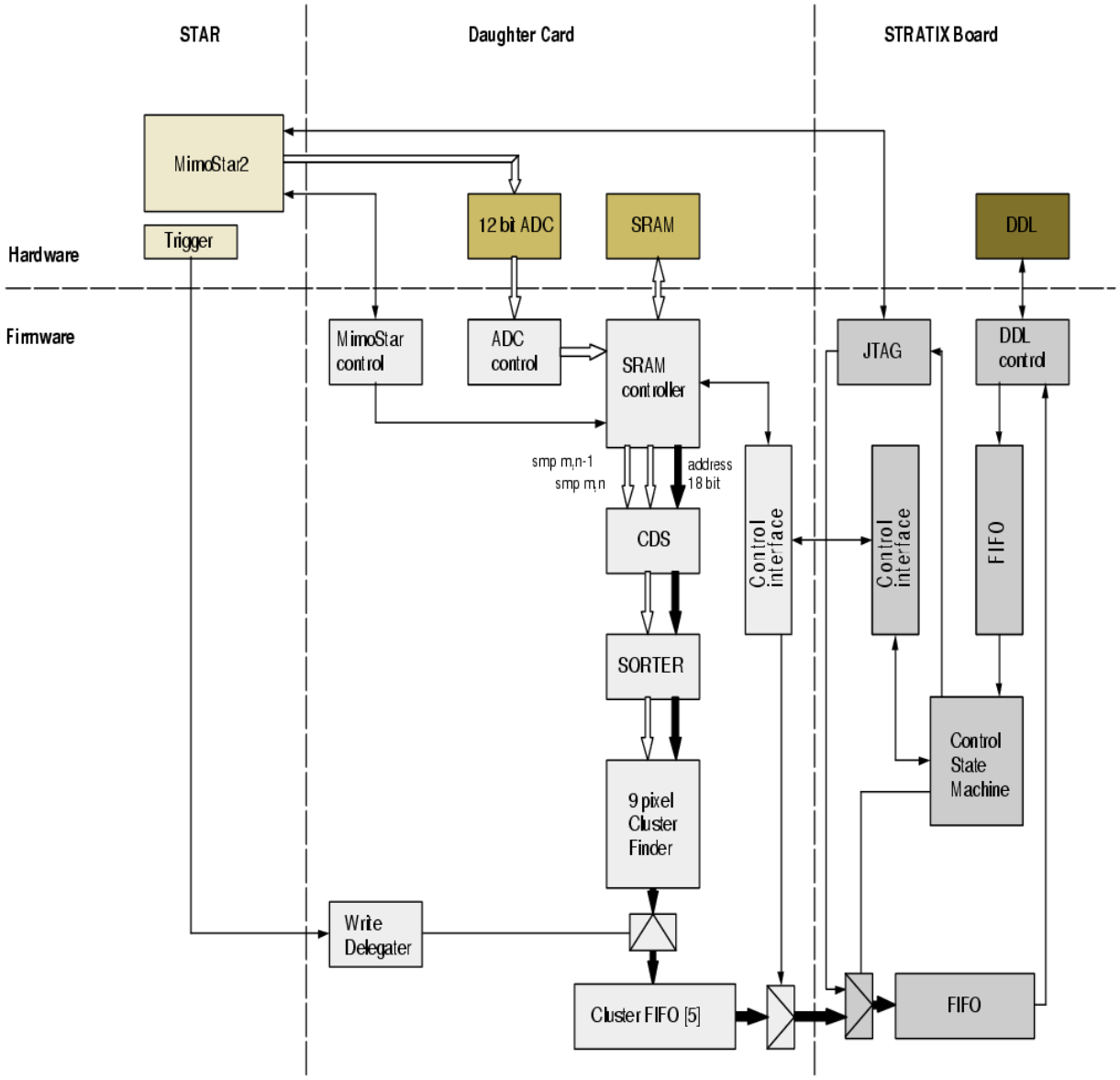


Figure 7.14: Firmware and hardware architecture of the telescope prototype readout. Firmware was divided between two FPGAs: signal processing was implemented in the Virtex2 FPGA on the custom-built daughter card, and interface to the fiber optic readout was designed in the Stratix FPGA on the Stratix development board.

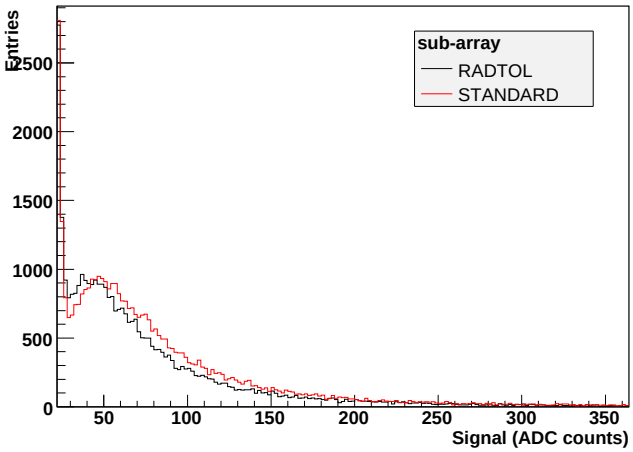


Figure 7.15: Signals from minimum ionizing particles registered with the telescope system for both types of diodes implemented in the MIMOSTAR2 sensor.

The noise of the sensors increased compared to the lab calibrations due to operation at increased temperature in a confined space in the telescope head. The airflow induced by the cooling system significantly reduced the temperature rise limiting the noise increase. The noise performance degraded to approximately 34 and 38 electrons for the standard and radiation tolerant structure, respectively. In the full-frame readout mode, a landau distribution for MIP particles was clearly observed. Plots showing the distribution of signal in seed pixels are presented in Figure 7.15. The observed MPV is at 49 and 43 ADC counts for the standard and radiation tolerant structure, respectively. When converted to electrons (G_{STD} = 4.7 e^-/ADC, G_{RAD} = 5.5 e^-/ADC), the MPV is comparable to the value estimated earlier in MIMOSTAR2 beam tests, approximately 230 electrons (Figure 6.10).

7.4.3 Tests with an electron beam

A set of runs with different cuts on the central and neighboring pixel in the cluster finder was acquired in the normal readout mode to evaluate performance of the complete processing channel. The cut on neighboring pixels was set to 14 ADC counts (approximately $2 \times Noise$) and the cut on the central pixel varied from 20 to 150 ADC counts.

Alignment procedure

The sensors in the telescope head were mounted with a limited precision. Proper analysis of the data acquired with the telescope system necessitated a precise alignment of all layers. The alignment procedure used in this work is derived from the assumption that the layers/planes are parallel and one can be transformed into another through geometric transformations limited to rotation and translation. More precisely, the alignment is extracted from transformation of points between two layers corresponding to the same particle tracks. It is assumed that tracks are perpendicular to the detector planes.

Assuming that the translation (h, k), where h is the offset in x-direction and k in y-direction,

is applied first and followed by a rotation about the coordinate origin by the angle α, the following equations hold true:

$$\begin{bmatrix} x' \\ y' \\ 1 \end{bmatrix} = \begin{bmatrix} \cos\alpha & -\sin\alpha & h\cos\alpha - k\sin\alpha \\ \sin\alpha & \cos\alpha & h\sin\alpha + k\cos\alpha \\ 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} x \\ y \\ 1 \end{bmatrix} \tag{7.4}$$

$$\begin{bmatrix} x \\ y \\ 1 \end{bmatrix} = \begin{bmatrix} \cos\alpha & \sin\alpha & -h \\ -\sin\alpha & \cos\alpha & -k \\ 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} x' \\ y' \\ 1 \end{bmatrix} \tag{7.5}$$

where (x, y) are coordinates of one point in the reference plane and (x', y') are coordinates in the transformed plane in the Cartesian coordinate system.

To calculate the misalignment, the plane of the most forward sensor was considered as the reference plane. It should be noted that the above set of equations uses three variables (h, k, α) and, therefore, is an undetermined system and does not allow to find a unique solution. A simple way to solve it is to introduce a second pair of points $((x_2, y_2),(x_2', y_2'))$ and to create a system of four equations. Selecting all pairs of points in one layer and transforming them into all pairs in the second layer will yield a distribution of solutions with a correlation peak that provides information about the alignment. The minimum distance between two points in one layer was limited to 30 pixels to avoid large inaccuracies in calculations when the chosen pairs do not correspond to the same set of hits. The rotation angle was constrained to less than 90° by the telescope assembly. As a consequence, pairs of points were analyzed in one orientation, excluding the equivalent solution rotated by 180°. A generalized example of the transformation procedure is illustrated in Figure 7.16.

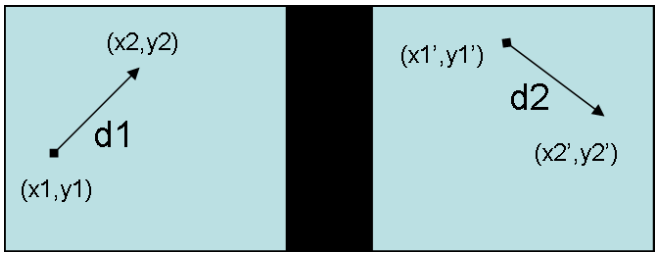


Figure 7.16: Example of two points on a plane before and after transformation.

Solving the set of four equations for $\sin\alpha$ and $\cos\alpha$ yields:

$$\begin{aligned} \sin\alpha &= \frac{(y_1-y_2)(x_1'-x_2')-(y_1'-y_2')(x_1-x_2)}{-(y_1'-y_2')^2-(x_1'-x_2')^2} \\ \cos\alpha &= \frac{(y_1-y_2)(y_1'-y_2')-(x_1'-x_2')(x_1-x_2)}{(y_1'-y_2')^2+(x_1'-x_2')^2} \end{aligned} \tag{7.6}$$

And the final set of solutions is given by:

$$\begin{cases} \alpha = \arctan\left(\frac{\sin\alpha}{\cos\alpha}\right) \\ h = x_1'\cos\alpha + y_1'\sin\alpha - x_1 \\ k = -x_1'\sin\alpha + y_1'\cos\alpha - y_1 \end{cases} \tag{7.7}$$

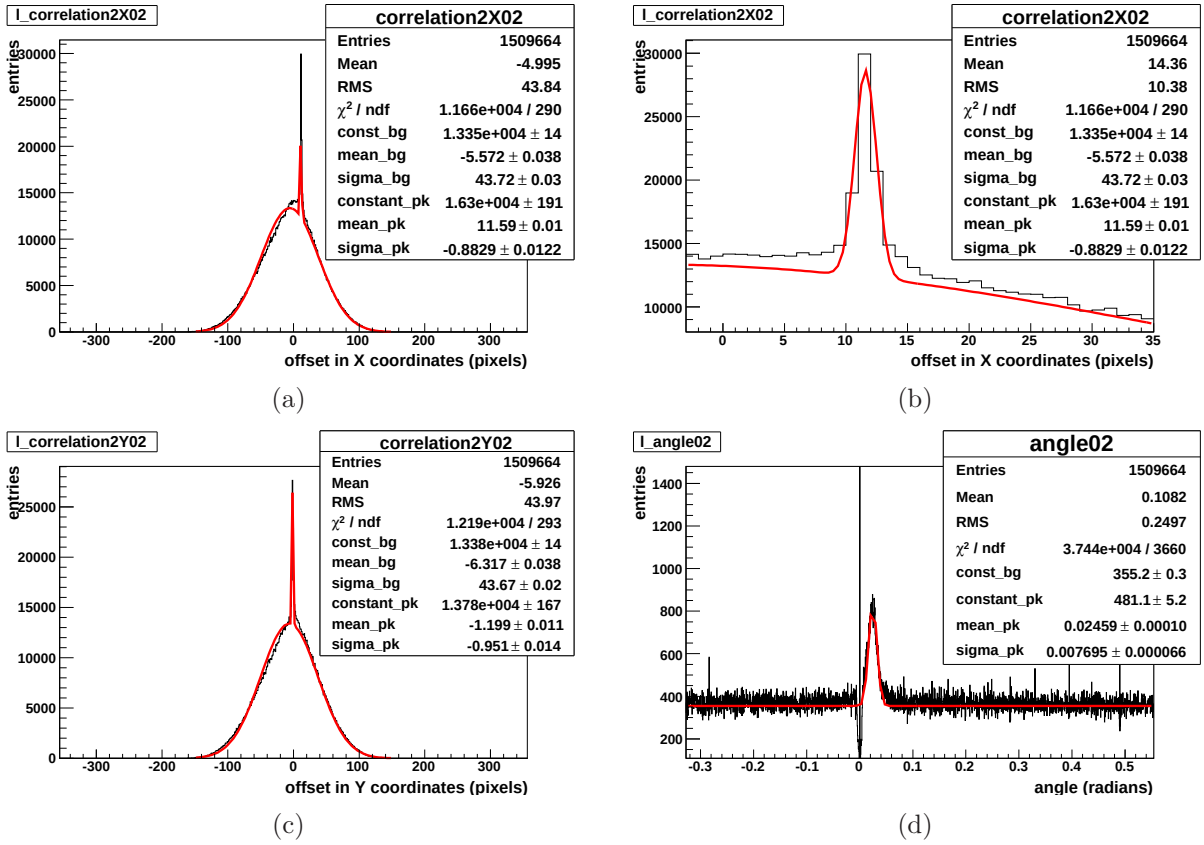


Figure 7.17: An example of distributions and correlations of alignment parameters between layers 0 and 2 in the telescope prototype. Peaks on top of random background distributions represent correlations that quantify the offsets between layers.

The distribution of solutions for all possible combinations was further constrained assuming the rotation angle below 45°. This results in $|\sin\alpha| < \sin(\pi/4)$, $\cos\alpha > \cos(\pi/4)$, and $(\sin\alpha/\cos\alpha) < 1$. An example of the distributions obtained is presented in Figure 7.17. The offset distributions for the h and k parameters can be fitted with two Gaussian distributions, representing background and a Gaussian-shaped correlation peak. The values of the translation parameters returned by this procedure and expressed in units of pixel size and radians are $h = 11.12\ \sigma\ 0.8$, $k = 15.54\ \sigma\ 0.7$, $\alpha = 0.0003\ \sigma\ 0.0002$ for the second layer, and $h = 11.56\ \sigma\ 0.9$, $k = -1.19\ \sigma\ 0.9$, $\alpha = 0.0246\ \sigma\ 0.0001$ for the third layer.

Efficiency of the telescope layers

The most important information about the operation of the telescope system can be expressed with a detection efficiency and fake-hit rate. This information was extracted from the acquired data after applying correction for the misalignments between sensor layers. The cuts used for collecting data were set to 14 and 25 ADC counts for the crown and central pixel, respectively.

An example of an integrated image for all three layers of the telescope prototype is presented in Figure 7.18. The inaccuracy of the alignment is clearly visible.

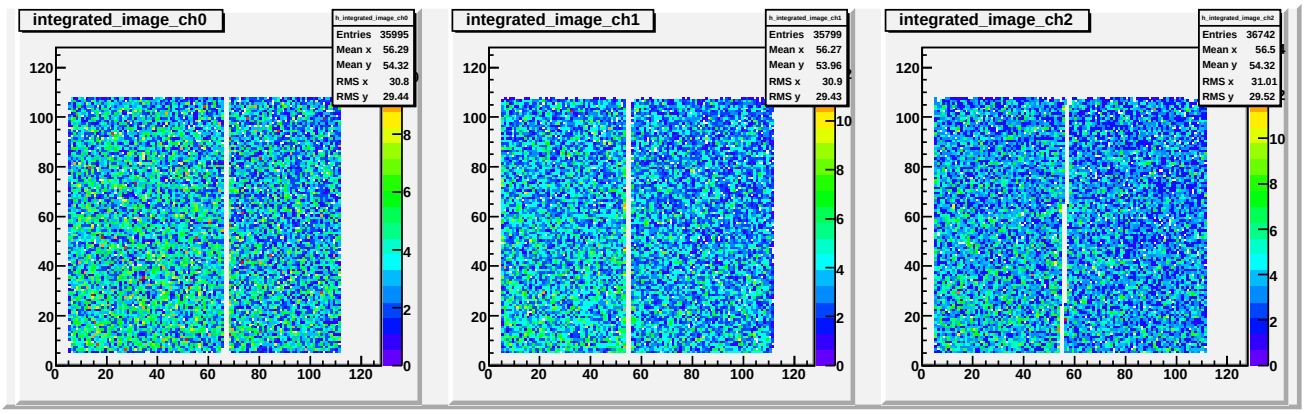
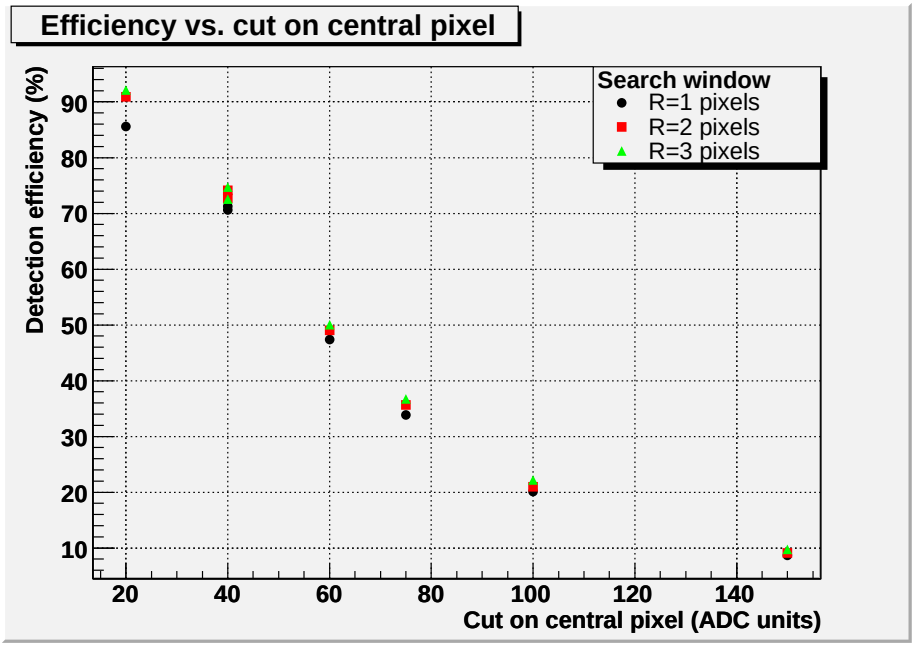


Figure 7.18: Integrated images of hits for all three layer of the telescope prototype. The common area for all chips after alignment is presented. The rotation angle in the third layer is clearly visible by looking at 2 columns of marker pixels present in the middle of the pixel array. Marker pixels are typically inserted into the sensor readout stream for synchronization purposes. They are virtual pixels with a constant voltage level and do not generate any hits.

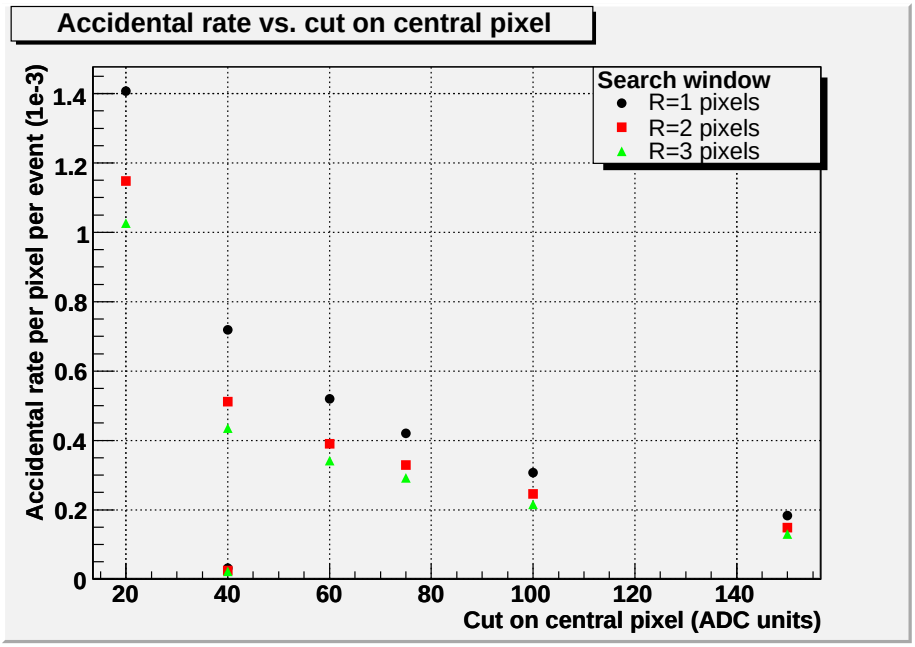
Two layers of the telescope can be used as reference planes to estimate the efficiency of the third layer. If a hit in one of the reference planes has a corresponding hit in the other plane, at the same location and within a specified search window, then these hits are associated with a particle track. The presence/absence of a hit in the third layer within a specified search window counts towards increased/decreased efficiency of this layer. At the same time, if there are hits in the layer of interest that are not part of tracks and cannot be associated with any hit in any other layer within the search window, these hits are classified as accidentals or fake hits. In case the hit in the layer of interest is not part of a track, but can be associated with one hit in any of the two other layers, it is assumed to be a part of an incomplete track and influences neither efficiency nor fake-hit counts for this layer. The plots of detection efficiency and accidental rate as functions of the cut on the central pixel are presented in Figure 7.19(a) and 7.19(b).

The obtained detection efficiency can not be directly compared with the study of the cluster-finder algorithm, because the signal-to-noise ratio is different in the two cases. The signal-to-noise ratio in the study presented in Chapter 7.3 was equal to 14. In the case of the telescope system, the ratio is 7.5 and 6.6 for the standard and radiation tolerant diodes, respectively. Thus detection efficiency can not be compared directly for the same set of cuts.

The accidental hit rate, however, can be compared. For example, for the set of cuts (center/crown) equal to 20/14 (3 $\times$ noise/ 2 $\times$ noise) the fake rate is about 10^{-3}, as expected. For the cut 40/14 (6 $\times$ noise/ 2 $\times$ noise), the rate measured is 0.4×10^{-3}, while the expected value would be at the level of 0.5×10^{-5}. The set of runs used in the efficiency scan was acquired for high beam luminosities. In case of the low luminosity run that used the same cut but was acquired a priori to the scan, the fake-rate was estimated at the level of 3×10^{-5}. This run is shown in Figure 7.19(b), very close to the horizontal axis. This result is compatible with the cluster-finder study. Electrons interacting with materials in the testing area and generating tracks that are not perpendicular to the telescope surface cold provide a plausible explanation for differences observed between runs with different beam luminosities.



(a)



(b)

Figure 7.19: Detection efficiency, (a), and accidental rate per pixel and per frame, (b), in telescope layers as a function of the cuts applied on the pixel signal and the search window radius.

7.4.4 Tests in the STAR environment

The fully tested and calibrated system was mounted inside the STAR detector to measure the performance of the telescope system in the real STAR environment. The test focused on checking for environmentally induced noise, measuring the charged particle density in STAR, and performing limited tracking. Integration of the system with the STAR control and trigger subsystems was an important milestone.

The system was mounted inside the STAR TPC for the last three weeks of the 2006-2007 Au-Au run. The sensor head was placed near the interaction diamond with the sensor plane approximately perpendicular to the beam axis. The final location of the telescope head was approximately 5 cm below the beam pipe and approximately 145 cm from the center of the interaction region. The electronics box containing the prototype readout system was located inside the STAR magnet pole tip, at approximately the position expected to be used for the final PIXEL detector electronics. The whole assembly operated in the nominal STAR magnetic field at 0.5 T. The telescope with the readout system was integrated with STAR DAQ trigger, run control, and slow control. The data stream was delivered to the DAQ standard readout PC but was not collected by the STAR event builder. The telescope system was operated at 50 MHz giving the integration time of approximately 1.7 ms.

The measured noise in the system installed in STAR was 7.48 ADC counts (ENC = 38 e^-), comparable to the laboratory and ALS environments. The stability of noise performance validates the system design. However, the overall increased noise level from the unterminated DAC test pads could still mask some small environmentally induced noise increase.

The charged particle density observed with the telescope assembly was about 25 clusters per cm^2. The average cluster size was about 3.9 pixels. The average RHIC luminosity during these tests was at the level of $8 \times 10^{26} cm^{-2} s^{-1}$.

Data taken during the normal STAR operation included background tracks, the majority of which can be expected to originate from the beam-gas type interactions, and charged particle tracks originating at the collision point. A plot of the angular distribution of tracks registered by the telescope system is presented in Figure 7.20. The measured peak in the angular distribution is similar to the geometrically calculated peak from the known distribution of tracks in the STAR interaction diamond. The measured distribution is wider, which we attribute to scattering in the beam pipe. For a short run the RHIC particle beams were displaced and did not collide in the interaction region. The measured angular distribution of the background tracks is also presented in 7.20. It peaks at zero degrees showing tracks parallel to the beam pipe. All curves in the plot are scaled arbitrarily. Tracks in this analysis were reconstructed from three hits that aligned along straight lines with deviations limited to a few pixels.

Through the duration of the test at STAR, no latch-up events were observed in the telescope system. This is an important observation for the latch-up tests described in Chapter 6.3.5. Although the location of the sensor head was not exactly the same as for the PIXEL detector, the result provides an important indication that the possible latch-up rate will be much lower than the prediction based on the on-going physics simulations of this process.

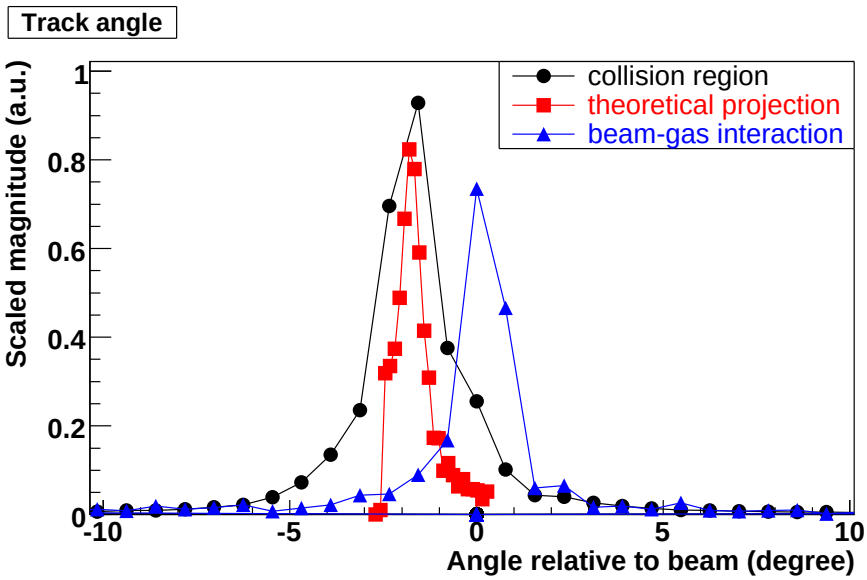


Figure 7.20: Angular distribution of tracks registered with the telescope in the STAR environment. The angular distribution of tracks measured during normal triggered data acquisition is shown. It is compared with a calculated distribution corresponding to the beam interaction diamond at STAR. The angular distribution of background tracks was obtained in a special run in which RHIC beams were displaced not to collide in the interaction region.

7.5 Summary of the PIXEL detector readout

The limited material budget in the low-mass area of the detector severely restricts the number of output channels in MAPS sensor. The number of signal paths and the complexity of signal connections in the carrier cable for a ladder structure are limited. This imposes a requirement on the sensor design with a few signal outputs per chip, at the most. For the PIXEL detector built with MIMOSTAR4 sensors each ladder populated with ten chips would require 20 differential pairs for the analog signal readout. The average amount of data available at the sensor level at 50 GB/s needs to be reduced at the output of the PIXEL detector to a manageable rate of about 100 MB/s. An efficient cluster finding algorithm necessary for data sparsification in the detector system has been studied. The algorithm reconstructs clusters based on a high signal cut on a central pixel and a low cut on the signal collected in one of the eight neighboring pixels. Detailed analysis indicates that detection efficiency above 99% with a fake-hit rate below 10^{-5} is achievable. The simplicity of this algorithm accompanied by high performance makes it an attractive solution for on-chip implementation in future MAPS sensors.

The algorithm has been tested with a prototype PIXEL readout system. The readout architecture was a scaled down version of the system for a complete detector. Three MIMOSTAR2 sensors combined into a 3-layer telescope were coupled with the prototype readout system and studied extensively. The operation of the ensemble was tested in laboratory conditions and with MIPs at the ALS and in the STAR environment. No distortions from the operation in a magnetic field and no noise pick-up were observed. However, due to the increased noise of the MIMOSTAR2 sensors in the prototype implementation to about 35 electrons, a small environment-dependant noise increase might have been masked by the inherently high noise

level. The integration of the prototype readout system with the STAR detector was successful. Triggers received form the STAR trigger subsystem were properly processed resulting in complete events with an embedded, unique trigger ID token.

The MAPS pixel technology used in MIMOSTAR sensors has proven to be compatible with the charged particle densities observed in the STAR environment. The final Pixel detector at STAR is expected to operate at the RHIC II luminosity of approximately $8 \times 10^{27}\text{cm}^{-2}\text{s}^{-1}$ but with a much reduced integration time of 200 μs. The expected hit densities in the final Pixel detector are 24 clusters/cm^2 on the outer sensors and 246 hits/cm^2 on the inner sensors. The presented test results strongly indicate that MAPS devices will correctly operate at the expected charged particle environment of the RHIC II luminosities.

The presented readout system will need to be slightly modified when the second generation MAPS prototypes become available. The signal processing will be shifted to the on-chip electronics simplifying the readout system architecture. However, multiple event buffering, event building and possibly on-the-fly cluster reconstruction will still be implemented in the system's FPGAs.

Chapter 8

Summary and Conclusions

8.1 Summary and future development

On-going and new research in the high energy particle physics domain, including investigations of the charm meson flow and jet quenching at STAR, or b-physics at the b-factory at KEK, or new physics, such as Higgs physics, couplings of gauge bosons, and supersymmetry at the future ILC, call for vertex detectors of unprecedented precision. Position sensitive silicon detectors currently represent the most viable solution for high-precision vertex measurements. The large fluxes of charged particles transiting detector layers introduce severe requirements on the sensor architecture and technology. Especially important are fast readout speeds to avoid pile-up of consecutive events and radiation tolerant designs to minimize radiation effects that are unavoidable in the extreme conditions present near collision regions. Several viable detector technologies exist, including the emerging, cutting-edge MAPS technology, which is one of the most attractive solutions. MAPS provide performance not achievable with other technologies. Among other features, MAPS offer fast readout speeds, possibility of building thin sensors, and good radiation tolerance. As this relatively new technology matures, plans for building vertex detectors with MAPS sensors emerge. One of such applications is the vertex detector for the upgrade of the STAR experiment planned for the year 2011.

8.1.1 MAPS structures for future development

The variety of pixel architectures presented in this work provides interesting solutions for designing application specific devices. The discussed advantages of the self-biased diode over the classical diode with a reset transistor make it a well suited solution for the STAR vertex detector upgrade. In addition, studies of a few simple in-pixel amplifiers indicate that simple architectures combined with in-pixel CDS circuitry (implemented as voltage memory on an NMOS transistor) can provide satisfactory results for simple on-chip analog data processing. Low power consumption requirements on the order of several microwatts per pixel can be achieved. A small in-pixel gain of 4-5 can be implemented with simple common-source or cascode amplifiers. Implementation of amplifiers with higher gain, at the level of 10, demonstrated gain reduction below 70% of the design value that has not been completely explained.

Two approaches for connecting a charge collecting diode and an in-pixel amplifier have been studied. Results show that charge collection efficiency can be improved by a few percent, when

the layout optimized AC coupling is implemented. As a side effect, signal becomes limited by a parasitic capacitive voltage divider that is associated with the proposed structure, leading to an even smaller signal-to-noise ratio compared to a DC coupled structure.

A MAPS prototype operated in current mode has been thoroughly studied. The PhotoFET structure that offers possible advantages of lower power consumption with signal amplitude unlimited by power supply voltage appears to be very sensitive to even small layout and operation asymmetries and, at the preset stage, does not provide a viable solution for reliable detector implementation. Nevertheless, its novelty and possible advantages deserve further investigation and future prototyping.

8.1.2 MAPS for STAR

A careful study of the performance of a MAPS prototype dedicated to the STAR vertex detector upgrade has been presented. It shows that MAPS have the potential to meet the requirements of the STAR vertex detector in low power dissipation and operation in high temperature in a moderately harsh ionizing radiation environment. A satisfactory signal to noise ratio of 15 can be achieved with a simple two transistor pixel architecture and the self-biased diode structure for charge collection. A small scale prototype proved to be radiation resistant in the ionizing radiation dose of interest. In addition, no latch-up occurrences were observed neither at the dedicated test facility at BNL nor in the STAR environment in close proximity of the beam pipe.

The limited material budget in the low-mass area of the detector severely restricts the number of output channels per sensor. The number of signal paths and the complexity of signal connections in the carrier cable for a ladder structure are limited. This imposes a requirement of at the most a few signal outputs per chip. A PIXEL detector built with ten MIMOSTAR4 sensors on each ladder would require 20 differential pairs for the analog signal readout. The average data rate of 50 GB/s at the sensor level needs to be reduced at the output of the PIXEL detector readout to a manageable rate of a few hundreds MB/s delivered to the STAR DAQ. An efficient cluster finding algorithm for data sparsification in the detector system has been studied. The algorithm reconstructs clusters based on a high signal cut on a central pixel and a low cut on the signal collected in one of the eight neighboring pixels. Detailed analysis indicates that detection efficiency above 99% with a fake-hit rate below 10^{-5} is achievable. The simplicity of this algorithm accompanied by high level of data suppression makes it an attractive solution for on-chip implementation in future MAPS sensors.

This algorithm has been tested with a prototype PIXEL readout system. The readout architecture was a scaled down version of a system for a complete detector. Three MIMOSTAR2 sensors, combined into a 3-layer telescope, were coupled with the prototype readout system and studied extensively. The operation of the ensemble was tested in laboratory conditions, with MIPs at the ALS, and in the STAR environment with heavy ion collisions. No distortions from the operation in a magnetic field and no noise pick-up were observed. However, due to the implementation details, the MIMOSTAR2 sensors operated in the prototyped telescope system exhibited noise of 35 electrons. This inherently high noise level might have masked a small amount of environment-dependant noise increase. The integration of the prototype readout system with the STAR detector was successful. Triggers received form the STAR trigger subsystem were properly processed, resulting in complete events with an embedded and unique trigger ID

token.

It is clear from the study presented that for more advanced designs, necessary for the final STAR detector that will be operated at an increased luminosity of $8 \times 10^{27}\ cm^{-2}s^{-1}$, in-pixel signal amplification and on-chip data sparsification will be required. The PIXEL vertex detector will need to operate with integration times at the level of 200 μs, or less, to cope with the increased luminosity of RHIC II. On chip data sparsification is necessary to reduce data rates that otherwise would reach an unacceptable level of tens of GB/s. To perform on-chip data processing it is critical to efficiently remove the fixed pattern noise. The solution for removing FPN that was implemented in the MIMOSA VIII prototype proves to be very efficient in reducing FPN below temporal noise and guides future development. The performance of MIMOSA VIII as a sensor for a vertex detector is limited. To achieve very high detection efficiency of more than 90% and, at the same time, low fake-hit rate, it is necessary to increase signal-to-noise ratio at the discriminator level. An improvement over the current prototype could be achieved through a sensor implementation in a technology with a thicker epitaxial layer that should allow collecting more charge. Some room for improvement exists at the amplifier stage, where higher gain could be achieved.

The possibility of decoupling the integration time from the readout time, proposed to solve the problem of leakage current increase after irradiation of the detector, was demonstrated. If the leakage current, in the given integration time, increases too much and induces an excessive noise, the integration time could be shortened without affecting the readout time. The architecture that allows this mode of operation is based on an in-pixel amplifier and an independent two-sample in-pixel signal storage. The readout would not be continuous as in the classical scheme, but would follow a trigger decision.

A triggered sensor is an attractive solution for a vertex detector that is inherently a triggered system. However, in the case of MAPS, operation in the classical rolling shutter mode imposes some limits on the achievable speed of operation. A latency associated with a trigger system can lead to a dead area in sensors if data related to a part of the pixel array is overwritten before the trigger can be processed. A solution to this would be on-chip buffering. This, however, is limited by the amount of buffering that is reasonable to be implemented in a chip. At the same time, it does not allow to process triggers that, in case of the STAR, could occasionally arrive more frequently than the expected 200 μs integration time. Dropped triggers would result in dead time in the detector operation. For the above reasons, it is important to consider sensor architecture together with readout of the detector system. A large part of the required data processing can be performed in FPGAs that would typically be located outside of the low-mass region. On chip signal sparsification will minimize data rates to a level at which the whole detector can be readout in less than the integration time. If the readout is continuous, data can be buffered in the readout FPGA that would also be responsible for processing triggers and associating them with appropriate sections of the data stream.

8.1.3 Future development of MAPS for STAR

When first MIMOSTAR sensors were designed, the expected luminosity of RHIC was lower than what is currently planned. As the consequence of the increased luminosity, the expected radiation dose in the PIXEL detector inner layers has increased by a factor of approximately 5 to 150 krad/year [109]. If the radiation damage in the inner layers becomes substantial under

these conditions, the possibility of replacement of the PIXEL detector during a RHIC run is envisioned. This is compatible with the HFT mechanical design that provides the capability for a simple insertion and removal of the PIXEL detector.

Another possibility to reduce the effects of radiation damage in MAPS sensors would be to operate the detector at lower temperatures. This option is currently under investigation and cooling systems that could blow cold air are being considered. A hermetic enclosure that would eliminate water condensation would add complexity to the already difficult mechanical design.

The radiation tolerance of MAPS could also be increased through the use of novel techniques, such as graded substrate for MAPS fabrication that is being investigated at IPHC [110]. Graded substrate could introduce additional shaping profile for charge collection that, according to TCAD simulations, reduces charge collection times by one order of magnitude, from typical 100 ns to approximately 10 ns.

Recently, due to the fast progress in maps development in the past two years, the use of MIMOSTAR4 prototype for constructing the STAR vertex detector demonstrator has been abandoned. The new goal is to provide a full size sensor that is based on the MIMOSA VIII architecture. This sensor will feature a 640×640-pixel array with the pixel pitch of 30 μm. The binary pixel information for the complete array will be read out on four digital outputs in approximately 640 μs.

A more advanced sensor will be developed for operation at the final RHIC II luminosity. The final CMOS chip is planned to be operated with the integration time on the order of 200 μs, or less, to reduce the effect of pileup. This requires very fast readout of the pixel array that can be achieved with on-chip data sparsification. The chip architecture will be based on the MIMOSA VIII prototype with massively parallel pixel column processing. On-chip data sparsification, based on finding hits that pass above a configurable threshold, is currently at a prototyping stage at IPHC.

8.2 Spin-off applications of MAPS

High-energy particle physics are the main driving force for development of advanced MAPS sensors but other fields of science can also vastly benefit from this technology. In addition to the core of the research presented in this thesis, the author participated in testing of MAPS devices for possible application in electron microscopy and in development efforts for medical imaging devices.

8.2.1 Electron microscopy

Electrons are used as probes in several research areas, such as chemistry, material science and biology. These probes reveal structural information with high spatial resolution better than 1 Å, short acquisition time, and limited beam exposures. Currently, electron microscopy (EM) requires an imaging device that will provide large spatial resolution at high speed for processing large sets of data to enable observation of short-lived phenomena. CCD cameras coupled with phosphor scintillating screen suffer from limited resolution, while photographic films and imaging plates are not adequate for fast processing or handling of large volumes of data.

The one-mega pixel MIMOSA V prototype, though not optimized for the use in electron microscopy, was used to demonstrate suitability of the CMOS technology for this application. Direct detection of electrons was characterized by a good point spread function (PSF), allowed for distinguishing single electrons with sufficient S/N, and provided high-resolution diffraction patterns. The prototype used for the tests exhibited the Modulation Transfer Function (MTF) at the level of current scintillator-coupled CCD imaging systems. The MTF in MAPS could be improved by limiting charge sharing between neighboring pixels. Radiation damage effects were observed during tests, proving that the radiation resistance of MAPS needs to be improved for applications in electron microscopy.

8.2.2 SUCIMA project

Medical applications are another example for multidisciplinary use of MAPS devices. The SUCIMA project (Silicon Ultra-fast Cameras for Electron and Gamma Sources in Medical Applications) focused on optimization of MAPS performance mainly for beam monitoring in hadrontherapy, but also for radioactive sources dosimetry in brachytherapy. Hadrontherapy uses hadron beams (proton or carbon beams accelerated to 200 MeV and 4700 MeV, respectively) to selectively remove tumor cells, due to the well defined hadron range energy function. The advantage of hadrontherapy over traditional X-ray irradiation is based on the precise energy deposition that minimizes damage to the overlying tissue, especially useful for removal of deep seated tumors.

MAPS allowed delivering a novel beam monitoring tool for on-line observation of the beam profile and intensity during the on-going patient treatment. The SLIM (Secondary emission for Low Interception Monitoring) utilizes MAPS for the collection of secondary electrons emitted from a thin aluminum foil (0.2 - 0.4 micrometers) that does not perturb the passing hadron beam. The liberated electrons, accelerated to 20 keV and focused with dedicated optics, reach the MAPS sensor and penetrate it to several micrometers. A back-thinning method that exposes the epitaxial layer from the bottom of the chip was developed for this purpose (see Chapter 3.4).

Appendix A

A.1 Simple model for pointing accuracy

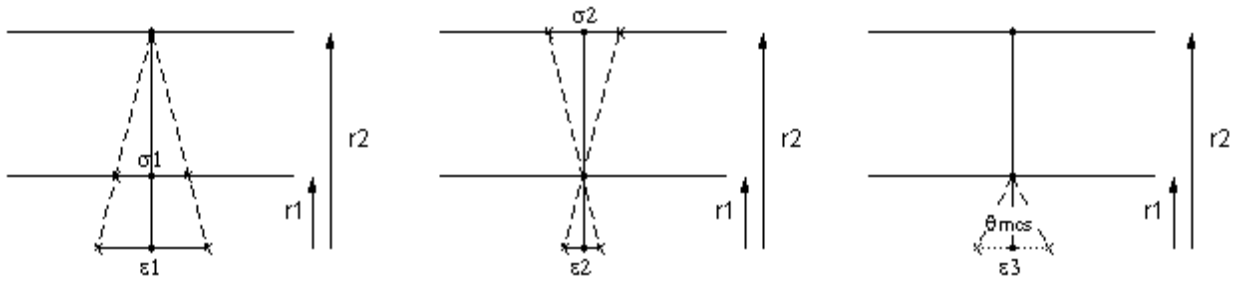


Figure A.1: Derivation of a simple model for the pointing accuracy of a two layer detector.

A simple model for the pointing accuracy of a two layer detector can be derived based on three consecutive assumptions:

1. the spatial resolution of layer one is σ_1, while the layer two is perfect and introduces no uncertainties

2. the spatial resolution of layer two is σ_2, while the layer one is perfect and introduces no uncertainties

3. both layers introduce no uncertainties and all the uncertainty results from the multiple Coulomb scattering

All three cases are illustrated in Figure A.1. The radii of layers one and two are r_1 and r_2, respectively. A reconstructed track is presented with black dots. In all three cases, the uncertainty of the vertex location can be estimated from similarity of triangles.

In the case 1 and 2, the pointing accuracy is expressed by Equations A.1 and A.2, respectively.

$$\epsilon_1 = \frac{r_2 \sigma_1}{r_2 - r_1} \tag{A.1}$$

$$\epsilon_2 = \frac{r_1 \sigma_2}{r_2 - r_1} \tag{A.2}$$

In the case 3, the particle travels from the interaction point towards the external layer of the detector. The deflection angle resulting from multiple Coulomb scattering in the layer one, θ_{mcs}, introduces uncertainty in layer two. However, when the tracking is performed, the path is traced backwards based on one point in each layer. Assuming that the points in both layers are without any uncertainties, the uncertainty from multiple Coulomb scattering translates to the origin point of the track. The same deflection angle can be interpreted as illustrated in the third sub-figure of Figure A.1. The uncertainty of the vertex location can be expressed by Equation A.3. In the equation, the track is tilt by the angle θ that extends the arm from r_1 to $r_1/\sin\theta$.

$$\epsilon_3 = \frac{\theta_{mcs} r_1}{\sin\theta} \tag{A.3}$$

The pointing accuracy of a two layer detector is a squared sum of all above errors, expressed by Equation A.4.

$$\sigma^2 = \frac{\sigma_1^2 r_2^2 + \sigma_2^2 r_1^2}{(r_2 - r_1)^2} + \frac{\theta_{mcs}^2 r_1^2}{\sin^2\theta} \tag{A.4}$$

A.2 Silicon properties

Table A.1: Silicon properties at 300K (after [111], [112])

Property	Symbol	Units	Value
Atomic number	Z		14
Atomic mass	A		28.09
Density	ρ	[g cm^{-3}]	2.33
Dielectric constant	ϵ		11.7
Energy gap	E_g	[eV]	1.12
Energy per electron-hole pair	E_{e-h}	[eV]	3.6
Intrinsic carrier concentration	n_i	[cm^{-3}]	1.45×10^{10}
Intrinsic resistivity	ρ	[k$\Omega \cdot$ cm]	230
Electron mobility	μ_e	[cm^{2}V^{-1}s^{-1}]	1400
Hole mobility	μ_h	[cm^{2}V^{-1}s^{-1}]	480
Electron lifetime	τ_e	[s]	$> 10^{-3}$
Hole lifetime	τ_h	[s]	2×10^{-3}
Breakdown electric field	E_{max}	[V μm^{-1}]	30

A.3 Bulk and epitaxial CMOS processes

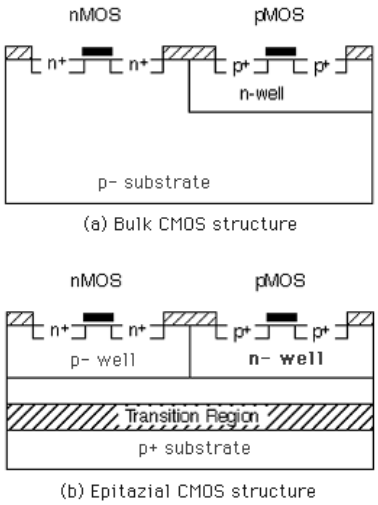


Figure A.2: Cross sections of bulk and epitaxial CMOS processes.

CMOS devices can be fabricated in a number of different ways. Structures, presented in Figure A.2, use a separate n-well region to fabricate p-channel devices. Maintaining a reverse bias across the well-substrate junction isolates the well region from the p-substrate. This well structure has no direct function other than providing an isolated region for the p-channel devices.

In the so-called bulk CMOS process, the complementary transistors are insulated from each other by placing one of them in a well with opposite doping with respect to the original bulk material (A.2(a)).

An alternative approach is the twin well (twin tub) process, where both types of transistors are implemented in p-wells and n-wells implanted on an epitaxial layer. In this approach, a highly doped p+ silicon can be used as substrate. The highly doped, low resistivity substrate has inherently smaller substrate resistance, making latch-up less likely compared to standard bulk processes. Another advantage of twin well processes over bulk processes is the fact that a low-resistivity substrate reduces the amount of charge that can be collected from the n+ drain, improving resistance to single-event upsets.

Appendix B

In-pixel amplifier designs

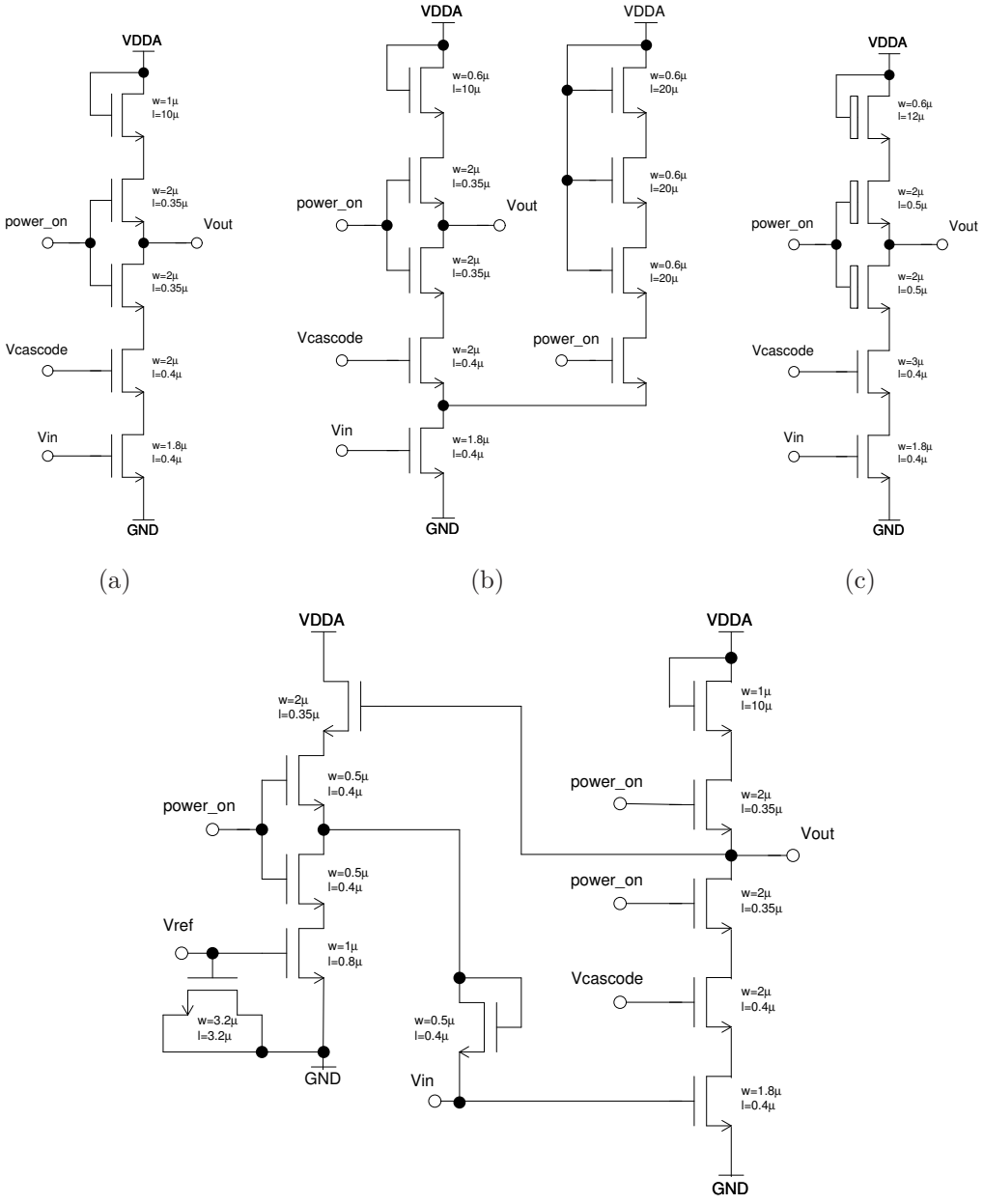


Figure B.1: Schematics of studied amplifiers. The most basic structure in the cascode configuration, with two switches for enabling operation of the amplifier at access to the pixel, (a). Cascode amplifier with an additional branch for increasing amplifier's gain, (b). Cascode amplifier benefiting from the use of 5V transistors available as an option in the AMS 0.35 process, (c). Cascode amplifier with a feedback loop for stabilization of the amplifier's operating point, (d).

Table B.1: Summary of performance parameters for in-pixel amplifiers implemented in test structures in prototype sensors MIMOSA IX and MIMOSA XI. The table shows results of simulations, (sim), and measurements, (meas), for the following set of parameters: (1) power dissipation, (2) bandwidth simulated for the amplifier with in-pixel memory circuit and for the full path, including a source follower transistor and the readout line capacitance (Cline), (3) noise simulated for the in-pixel amplifier, amplifier and the source follower stage, the readout chain including the charge collecting diode and the CDS operation, (4) measured noise performance, (5) ENC extracted from ^{55}Fe calibrations, (6) FPN measured before and after CDS, (7) simulated gain of the in-pixel amplifier with and without the source follower stage, (8) amplifier and source follower gain measured in static, dynamic, and ^{55}Fe calibration measurements; the value in parenthesis is estimated for the amplifier only, (9) width of the linear range (to within 5%) of the amplifier with and without the source follower stage, (10) dispersion of the pixel output voltage level (FPN), (11) gain variation at the pixel output, (12) gain variation for the amplifier stage only.

		Power dissip. (sim) (μW)	BW (lf,hf) (amp+mem)/ /(amp+sf+Cline(5 pF)) (sim) (MHz)	Noise (12 fF coupling) amp/+sf/+diode/cds (sim) (mV)	Noise (meas) (mVrms)	ENC (meas) (e^-)	FPN /after CDS STD (meas) (mVrms)
m9	CS 1branch AC 3T arr	18.5	4.2/3.3	0.41/0.32/1.3/0.46	0.52	20	75/9.0
	CS 2branch AC 3T arr	19	4.8/3.7	0.66/0.50/2.4/0.78	0.77	20	95/10.0
	CS 5V AC 3T arr	28	4.5/3.5	0.72/0.56/2.3/0.81	0.81	18	81/8.6
m11	CS DC arr	30	7.3/5.2	0.45/0.34/1.7/0.53	0.44	12 (vdiode 0.8V)	109/6.6
	CS AC 1T arr	20	7.3/5.2	0.45/0.34/1.7/0.55*	0.48	20	32/7.0
	CS AC+Feedback arr	21.5 (+3.3)	7.7/5.2	0.46/0.34/1.4/0.50	0.58	26	<25/6.6

		gain amp/+sf (sim)	gain stat/dyn/calib (meas)	linearity gmax +-5% amp/+sf (sim) (mV)	offset dispersions (sim) (mV)	pixel gain dispersions	amplifier gain dispersions
m9	CS 1branch AC 3T arr	6.2/5.1	1.5/-/3(4)	110/95	529 σ 43	5.14 σ 0.041	6.2 σ 0.063
	CS 2branch AC 3T arr	10/8.2	2/-/4.5(6)	50/40	527 σ 74	8.10 σ 0.145	9.8 σ 0.120
	CS 5V AC 3T arr	11/9.17	2/-/5(6.6)	100/90	688 σ 76	9.15 σ 0.040	11.0 σ 0.066
m11	CS DC arr	6.2/5.1	3(4.2)/4(5.7)/3.7	120/95	433 σ 41	5.14 σ 0.034	6.31 σ 0.028
	CS AC 1T arr	6.2/5.1	n/4(5.7)/2.6(3.5)	120/95	630 σ 46	5.11 σ 0.056	6.18 σ 0.082
	CS AC+Feedback arr	6.3/5.2	n/4(5.7)/1.8(2.4)	n.a.	576 σ 12	5.16 σ 0.022	6.26 σ 0.029

Appendix C

Test bench for MIMOSA VII

Three different readout schemes for the tests of the MIMOSA VII chip were developed and tested in order to extract different information about the chip. First, the direct current outputs were examined using off-chip transimpedance amplifiers with resistive feedback. The functioning of PhotoFET cells in an array structure was tested by performing appropriate software analysis on the recorded raw data. After discovering that DC current components show a significant pixel-to-pixel dispersion, two external implementations of subtracting circuits, based on the same principle as the integrated in-chip amplifier but having less gain, were used to process the signal from direct current output columns. Two alternative circuit topologies were examined. Both of these circuits operated in synchronization with access to the pixel rows. In the last step, accessible tests were performed using the high gain CDS amplifier implemented in the chip. Such approach stipulated the development of a flexible test bench dedicated to the tests of this

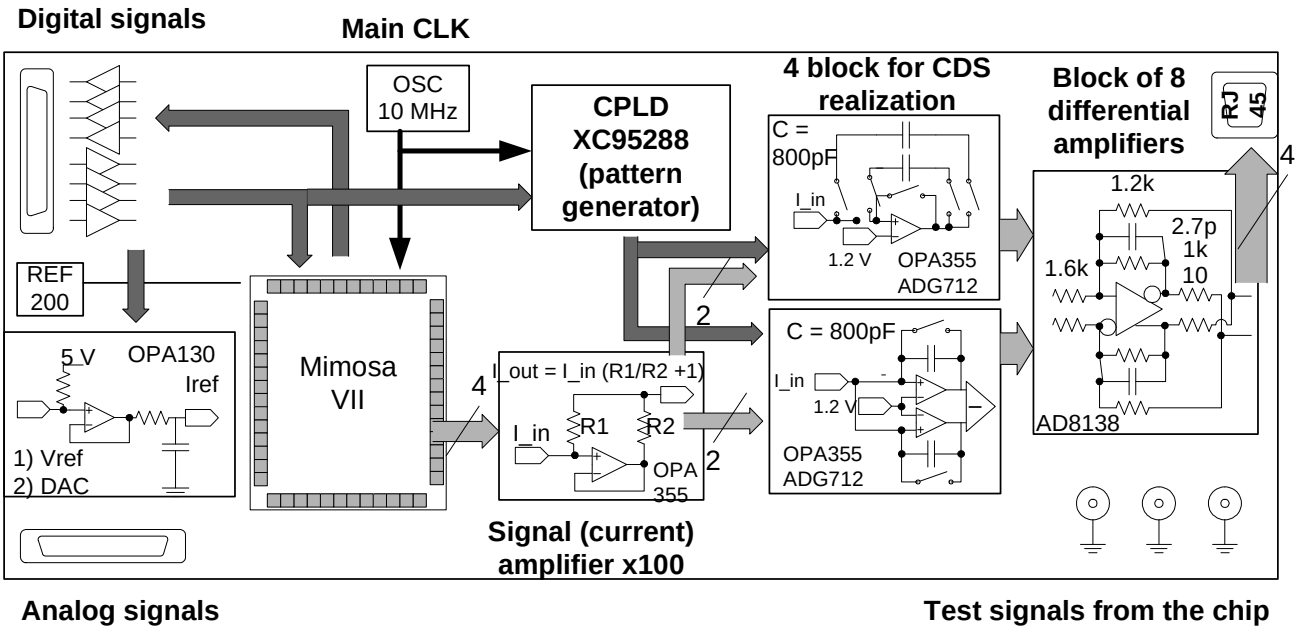


Figure C.1: Block diagram of the version A of the proximity board for tests of the MIMOSA VII direct current outputs.

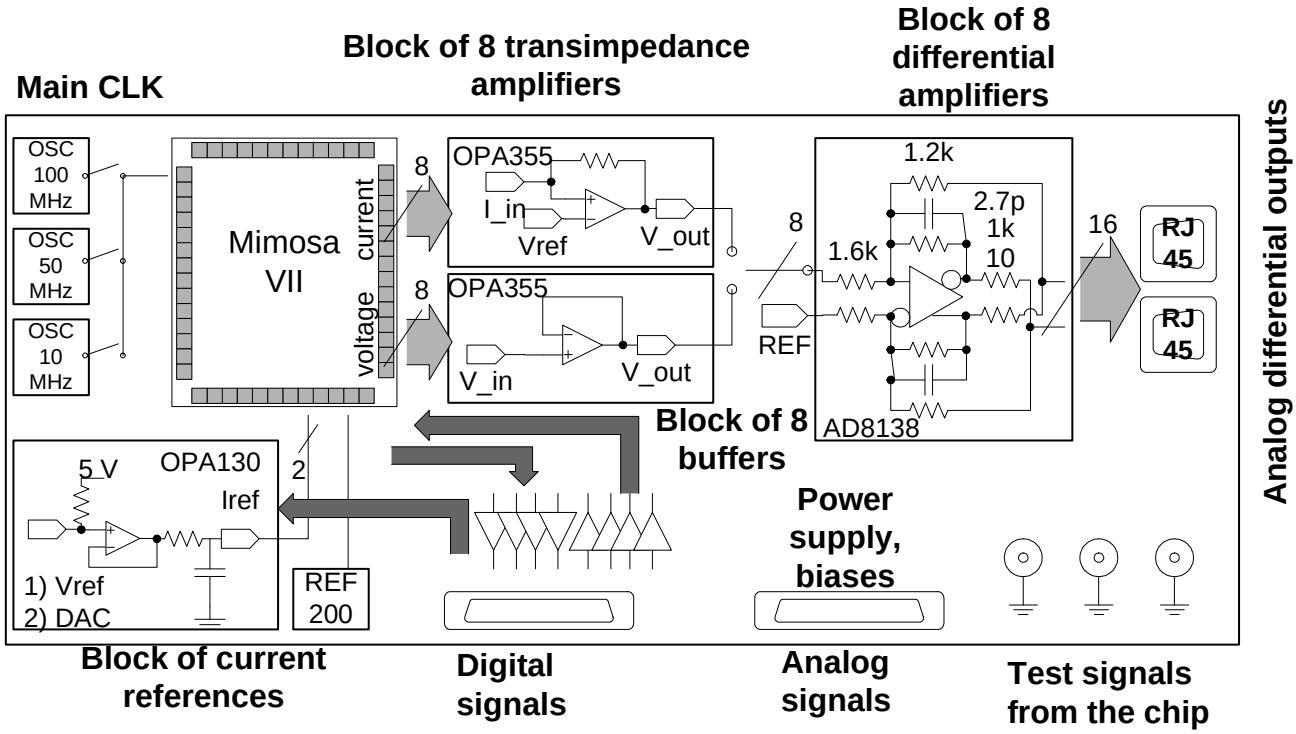


Figure C.2: Block diagram of the version B of the proximity board for tests of discrete implementation of CDS and subtraction of current signals from the MIMOSA VII chip

chip.

The schematic diagram, shown in Figure 3.7, shows a general view of the setup. The test system was constituted of three main parts: the proximity board (PB) on which the chip under test was located, the intermediate board (IB), and the acquisition card, being the main part of the data acquisition system (DAQ). Two versions of PB were designed. The first version, called A, was used for testing both direct current outputs and the on-chip implemented CDS readout. The schematic diagram of this board is shown in Figure C.1. The version B of the card, which details are sketched in Figure C.2, comprised external implementations of the CDS circuit.

PB was directly coupled to IB using flat ribbon cables for digital and analog signals. The latter card contained functions such as: generation of the reference voltages for the chip, LVDS conversion and buffering of digital signals for sending to DAQ and loading digital pattern from a PC computer to the chip under test. The flow of analog and digital data to the distant acquisition card was set up with shielded twisted pair Ethernet type cables.

Another component of the system was a small auxiliary card, where the bare MIMOSA VII chip was bonded. The card contained decoupling capacitors and could be plugged onto PB using miniaturized multi-pin connectors. The chip under test could be easily exchanged in this way.

Proximity Cards

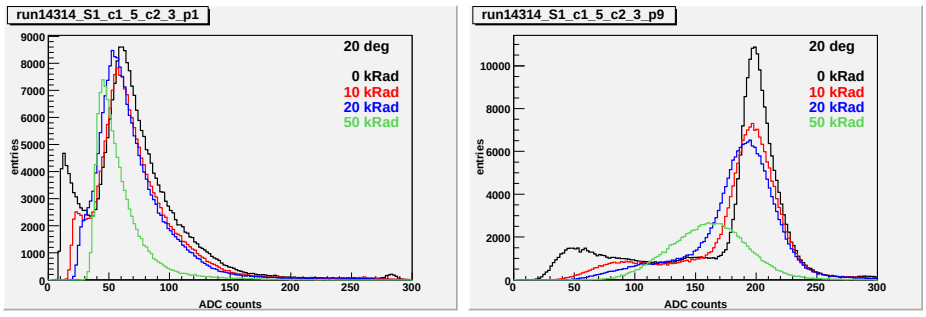
The operation of the card A could be configured using switches to work with eight outputs of direct current signals, converting them to voltages, or with voltage signals from the on-chip CDS processing. The card contained a bank of eight transimpedance amplifiers, built with an operational amplifier and resistance in the feedback loop, providing transresistance of about 13 kΩ for current-to-voltage conversion. In the case of voltage outputs from the MIMOSA VII chip, simple voltage followers, built with operational amplifiers, were used to buffer the signals before conversion to differential signals. Single-ended to differential voltage converters, providing a gain of about 1.5, were used to drive the lanes directly to DAQ.

The whole read out chain was designed to be fast and to operate at low-noise for the main clock frequency of up to 100 MHz. The source follower in the PhotoFET cell required current reference defined externally to the chip. This reference was fixed with a resistor on PB to the default value ranging from a few tens of nA up to 100 nA. Another current reference, common for the whole array, was used for the subtraction of the signal DC current component. An 8-bit digital-to-analog converter, placed on PB, controlled the current value. A configuration word for programming the current value in the range from tens of nA to 50 μA was defined on IB.

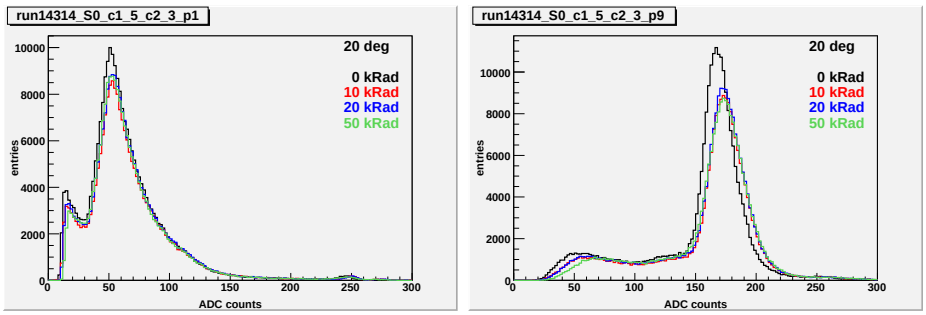
The discrete implementations of transimpedance amplifiers required a relatively large PCB area. Thus the card B was designed for processing of only four direct current outputs. The design of the card B is presented in Figure C.2. The processing chain on the card B consisted of current conveyors, for amplifying current by 100, and two types of circuitry for integrating currents and subtracting the results of integration to produce the final result that could be sampled by DAQ. Amplifiers identical to those placed on the card A were used for converting single-ended signals to differential. In addition, the card B contained a programmable logic device that generated a control sequence for switches in the CDS blocks in pace with the operation of the MIMOSA VII chip. A quartz oscillator and current references, required for the sensor operation, were also located on the card.

Appendix D

Additional MIMOSTAR 2 tests



(a) (b)



(c) (d)

Figure D.1: Displacement of the calibration peak and 9-pixel cluster signal as a function of radiation dose, measured at 20 °C. Signal distributions on seed pixels are presented in sub-figures (a) and (c). Signals in 9-pixel clusters are shown in figures (b) and (d). Sub-figures (a, b) show data for the standard diode structure and sub-figures (c, d) for the radiation tolerant design.

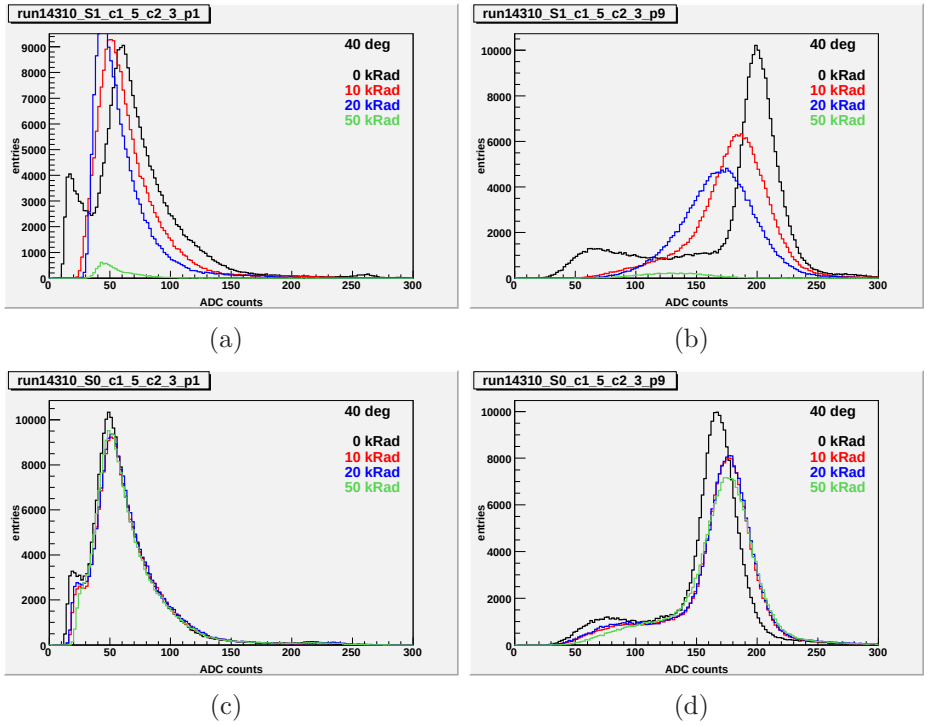


Figure D.2: Displacement of the calibration peak and 9-pixel cluster signal as a function of radiation dose, measured at 40 °C. Signal distributions on seed pixels are presented in sub-figures (a) and (c). Signals in 9-pixel clusters are shown in figures (b) and (d). Sub-figures (a, b) show data for the standard diode structure and sub-figures (c, d) for the radiation tolerant design.

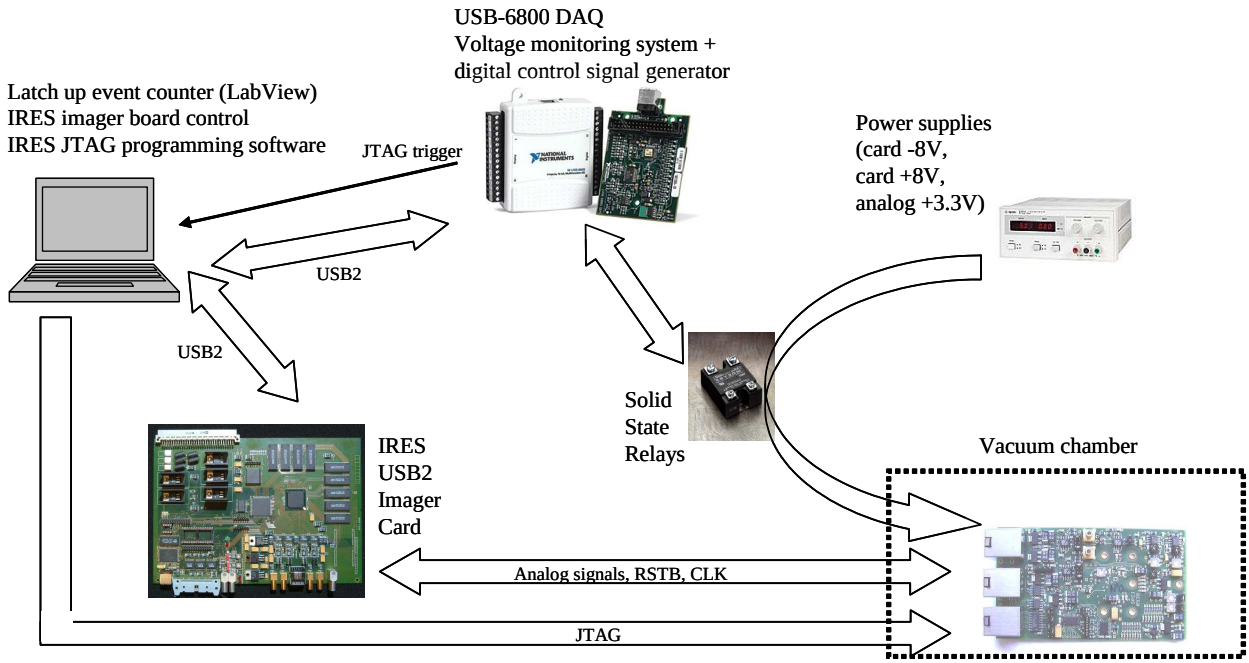


Figure D.3: Diagram of the setup for latch-up tests with the MIMOSTAR2 prototype. USB2 based acquisition system was used for providing all signals necessary for chip operation. Latch-up monitoring was built with a multi-purpose DAC-ADC module controlled through the LabView environment. When a voltage drop was detected, indicating a latch-up condition, solid state relays disconnected power supply form the sensor testing board. Shortly after removing the latch-up action, the power supplies were reconnected and the operation of the sensor was restored.

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RESUME

Ce travail contribue au programme de recherche et de développement des détecteurs monolithiques à pixels actifs (MAPS) pour la construction du prochain détecteur de vertex dans l'expérience STAR du collisionneur RHIC. Le détecteur à 135 million pixel, prévue pour 2011, augmentera le programme de physique grâce à sa résolution de pointage prévu du 30 µm. La collaboration STAR développe ce détecteur dans la nouvelle technologie des MAPS qui fournit un capteur et l'électronique de lecture intégrée dans les processus standard de CMOS. Le travail présenté dans cette thèse, décrit la progression du développement des MAPS d'une simple architecture jusqu'à des conceptions plus complexes qui intègrent le traitement des signaux sur le circuit. Une étude un amplificateur d'entrée intégré au niveau d'un pixel avec une consommation de puissance faible et à faible bruit, est présenté avec les résultats expérimentaux associés.

L'intégration des capteurs MAPS au détecteur du vertex a été étudié dans ce travail avec un télescope de détecteurs composé de trois prototypes MAPS et un prototype du système de lecture. La réduction du débit des données d'un système portant sur plusieurs millions de pixels a été étudiée avec un algorithme trouvant dynamiquement les pixels touchés par le faisceau .

L'opération du RHIC à une luminosité ultime exige des architectures plus avancées que la simple conception mise en application dans de premier prototype consacré à STAR. Dans ce travail les solutions présentées indiquent le chemin de développement pour les capteurs finaux avec une amplification du signal intégré dans les pixels et une numérisation des données sur le détecteur.

Mots clés : Détecteurs à pixels, Monolithic Active Pixel Sensors, CMOS, Détecteur de vertex, STAR.

ABSTRACT

This work is part of the Monolithic Active Pixel Sensor (MAPS) R&D program that is directed towards construction of a new, 135 million pixel vertex detector for the STAR experiment at the RHIC collider. The new detector is planned to be installed in 2011 to extend the current physics capabilities of the system by providing a pointing resolution of 30 µm. The STAR collaboration is actively pursuing detector development in MAPS technology that offers thin monolithic detectors fabricated in standard CMOS processes. The work presented addresses the development of MAPS from basic architectures to simple integrated on-chip signal processing. A common element for most of the presented readout schemes is a compact low-noise, low power consumption, compact in-pixel amplifier. A review of possible solutions for this element together with experimental results is presented. MAPS operating in current mode have been investigated in this thesis as an alternative to the classical voltage mode.

Integration of MAPS sensors in a complete detector system has been investigated with a prototype readout system coupled to a detector telescope composed from three MAPS prototypes. The optimization of the readout of a multi-million pixel detector has been addressed with a study of an "on-the-fly" cluster finding algorithm reducing the data rates.

The operation of RHIC with increased luminosity will require more advanced pixel architectures than the simple design implemented in the first prototypes. The solutions presented indicate a development path for the final sensor with in-pixel signal amplification and on-chip data digitization.

Keywords: Pixel detectors, Monolithic Active Pixel Sensors, CMOS, vertex detector, STAR .