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Özge TÜZÜN

Polycrystalline Silicon Films by Aluminium Induced Crystallization and Epitaxy: Synthesis, Characterizations and Solar Cells

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Membres du jury

Directeur de thèse	: M. Abdelilah Slaoui, Directeur de Rech., CNRS
Rapporteur externe	: Mme. Anne Kaminski-Cachopo, Maître de Conf., INSA Lyon
Rapporteur externe	: M. Pere Roca i Cabarrocas, Directeur de Rech., CNRS
Examinateur	: M. Aziz Dinia, Professeur, Université de Strasbourg
Examinateur	: M. Alain Straboni, Professeur, Université de Poitiers
Examinateur	: M. Ivan Gordon, Ingénieur de Rech., IMEC, Leuven (B)

Institut d'Electronique du Solide et des Systèmes - InESS **UMR 7163**

DEDICATION

To my parents,
Özcan and Şener Tüzün,
for their support and patience.

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ABSTRACT

Thin-film polycrystalline-silicon (poly-Si) with a grain size between 0.1 and 100 μm has triggered great interest in the field of photovoltaics as a promising alternative to silicon wafers and amorphous silicon (a-Si) thin films. Large grained p-type polysilicon films, 200nm thick, can be fabricated by aluminum-induced crystallization (AIC) of a-Si at temperatures below 500°C. In addition, n-type poly-Si thin films may present many advantages compared to p-type such as higher lifetime and better tolerance to defects.

In this thesis, we have prepared p- and n-type poly-Si seed layers by AIC on alumina and glass-ceramic substrates, followed by epitaxial thickening using low pressure chemical vapor deposition (LPCVD); and HIT solar cells (Heterojunction with Intrinsic Thin layer) were then fabricated. The structural quality of the Si films was monitored by optical microscope and electron back scattering diffraction technique (EBSD). Polycrystalline silicon layer with quite large grains with an average grain size value of ~26μm can be formed by AIC technique at 475°C on glass-ceramic substrate while it is only 7.6μm for AIC layer alumina substrate. While the surface roughness of susbtrate has a great influence on grain size, there is no effect on preferred orientation that is <100> for both types of samples. We have shown that the main crystallographic defects present in the continuous polysilicon layers are the low-angle grain boundary (LAGB, angle<2°) and the coincident site lattice (CSL) boundaries consisting of twin boundaries of first order (Σ3), second order (Σ9) and third order (Σ27) while the majority of crystallographic defect is Σ3 independently from substrate choice. A graded doping profile was obtained by out-diffusion of phosphorus from the overdoped seed layer during the epitaxial thickening. The grain size conservation for epitaxial layer was observed with that of the underlying AIC poly-Si seed layer. We have also prepared for the first time n-type based polysilicon solar cells ($n^{+}np^{+}$) with AIC approach on alumina substrate. An efficiency of about 5.5% realized in our n-type cells without texturization that should be compared to 3.2% for p-type cells. In addition to cell efficiency, the spectral response of the n-type cell is also much widen than that of p-type cell, over a large part of the spectrum. This lead to an enhancement in L_{eff} for n-type cell (~2.6μm) compared to that of p-type (0.9μm). Analysis of the best n-type based cells with Sun-V_{oc} apparatus, neglecting therefore the contacts resistivity, led to an efficiency value of 6.1%, showing the potential of the n-type polysilicon solar cells without any optimisation of the hydrogenation step, the heterojunction passivation and junction formation, nor the surface texturing. It is considered that this last step is capable to boost the efficiency by a factor a least of 2.

RESUME DE THESE

Films de Silicium Polycristallin Obtenus par Cristallisation Induite par Aluminium et Epitaxie: Croissance, Caractérisations et Cellules Solaires

Parmi les orientations actuelles de recherche dans le domaine de la conversion photovoltaïque, il y'a l'émergence de cellules en couches minces (Si, CdTe, CIS). En particulier, l'utilisation de films minces en silicium polycristallin (<10µm d'épaisseur) déposés sur des substrats étrangers divers et peu coûteux (verre, céramique…) est aujourd'hui en pleine exploration car elle offre les avantages d'un faible coût et d'une grande stabilité. Il existe deux approche pour réaliser le film Si polycristallin (poly-Si) : (i) le dépôt direct par dépôt chimique en phase vapeur (CVD) à haute température (>1000°C) et temps court (<5min) ou la cristallisation en phase solide (SPC) d'un film de silicium amorphe à basse température (<500°C) mais pendant de longues heures (>24h). Dans ce cas, le film poly-Si présente des petits grains (1-3µm) avec une grande distribution, ce qui limite les performances par l'importante densité des joints de grains, (ii) la formation d'une couche poly-Si par cristallisation de silicium amorphe induite par métaux (MIC) ou par laser (LIC). L'objectif étant de réaliser une couche poly-Si à très gros grains, exemptes de défauts intra-grains et servant de couche « germe » ou tampon pour la formation d'une couche poly-Si plus épaisse par épitaxie.

Parmi les approches à couche tampon, il y a la formation du silicium polycristallin par le procédé de cristallisation du silicium amorphe induite par aluminium (AIC) qui permet de former une couche mince de silicium polycristallin (<0.5µm) à larges grains (>5µm) dopé à l'aluminium ($2.10^{18}cm^{-3}$). La méthode consiste à recuire une bicouche a-Si/Al/substrat à des températures inférieures à l'eutectique (T_{eu} =577°C) pendant quelques heures. Durant le recuit, la structure initiale a-Si/Al/substrat permet d'inverser la structure en formant la couche poly-Si directement sur le substrat et l'excès d'aluminium n'ayant pas participé à la transformation se retrouve en surface de la structure et peut donc être facilement décapé. Une des clés de l'échange est la présence d'une couche d'oxyde d'alumine très fine entre les couches d'aluminium et de silicium amorphe, qui joue un rôle de membrane perméable. La couche poly-Si formée par la méthode AIC est trop mince (<0.25µm) et fortement dopée de type p ($\sim 2\times 10^{18}Al/cm^3$). Elle ne peut pas servir comme matériau de base pour la conversion photovoltaïque. Ainsi, la couche AIC doit être épaissie par épitaxie à basse température ou à

haute température. Le choix de la méthode d'épitaxie dépendra également du substrat choisit compte tenu de sa compatibilité avec les gaz utilisés et la température employée. Par ailleurs, il est établit que le silicium de type n pourrait présenter des avantages pour le rendement des cellules, notamment à cause de la grande mobilité des porteurs minoritaires et d'une plus grande tolérance aux défauts.

Dans ce travail, nous avons étudié d'abord la croissance du silicium polycristallin (couche germe AIC) sur substrats d'alumine ou vitrocéramiques par le procédé de cristallisation induit par aluminium du silicium amorphe. Les études ont concerné la cinétique de croissance de la couche AIC en fonction de plusieurs paramètres expérimentaux (température, temps, épaisseur du films Si amorphe, la teneur en hydrogène,…) et la détermination des défauts de structure inter-grains (joints) et intra-grains (macles). Nous avons également recherché à réaliser des films tampon de type n par surdopage et évaluer son efficacité. Nous avons étudié les propriétés structurales et opto-électroniques des couches épaisses silicium obtenues par épitaxie sur les couches tampon AIC. Nous avons utilisé deux méthodes de croissance de la couche absorbante: l'épitaxie en phase vapeur (VPE) à haute température ou l'épitaxie en phase solide (SPE) par dépôt d'une couche Si amorphe et recuit. Enfin nous avons réalisé des cellules photovoltaïques sur ces matériaux afin de valider leur potentiel pour la future génération de cellules solaires. Nous avons ainsi réalisé des structures de cellules de configuration n^+pp^+ sur poly-Si de type p mais également des configurations p^+nn^+ sur poly-Si de type n. La région « émetteur » des cellules a été réalisée soit par diffusion de dopants à partir d'une source solide, ou par dépôt d'une double couche ultra-fine de silicium amorphe l'une intrinsèque et l'autre fortement dopée. Ce travail s'inscrit en partie dans le cadre d'un projet national ANR intitulé POLYSIVERRE dans lequel les sociétés CORNING, AET, et TOTAL, et les académiques LPICM, INL et EMSE sont impliqués.

Dans le premier chapitre, nous avons présenté une étude bibliographique exhaustive nous permettant de poser les bases de la problématique du sujet traité. Cela a commencé par un rappel des différents matériaux et technologies photovoltaïques existantes à nos jours, leurs avantages et leurs inconvénients. Ensuite, nous avons abordé l'approche des couches minces pour le photovoltaïque, et plus particulièrement celle du silicium polycristallin sur substrat céramique qui fait l'objet de ce travail.

Dans le deuxième chapitre, nous avons rappelé les propriétés optiques et électroniques du silicium polycristallin, en relation avec la taille des grains, la densité des joints de grains et des défauts intra-grains. Ensuite, nous avons présenté les différentes méthodes -basse et haute température-utilisées pour former le silicium polycristallin. Nous avons largement détaillé les

principes de la technique de cristallisation induite par métaux (MIC) du silicium amorphe, et en particulier le procédé de cristallisation induit par aluminium (AIC).

Le troisième chapitre présente nos résultats expérimentaux donnant les propriétés structurales, morphologiques et électriques des couches polycristallines de type p obtenues par le procédé AIC. En particulier, nous avons corrélé la cinétique de croissance aux paramètres techniques (température, temps) mais également au type de substrat céramique utilisé : alumine ou verre haute température. Grâce à des observations optiques et à des analyses EBSD (Electron Back-Scattered Diffraction), nous avons déterminé la distribution de la taille des grains, la densité des joints de grains et la densité des macles. Nous avons suivi l'évolution de ces différentes grandeurs en fonction de traitements thermiques postérieurs au procédé AIC pour suivre l'évolution de la cristallographie des grains. En utilisant des verres céramiques, nous avons pu réaliser des films poly-Si à T<500°C, présentant une taille moyenne de grains cent fois supérieure à son épaisseur (0.2µm d'épaisseur et 26µm en taille de grains), et des grains majoritairement orientées <100>. Nous avons montré que la densité des macles, en particulier Σ3, est réduite en diminuant la température de cristallisation. Les raisons de ce comportement sont largement discutées.

Une partie de chapitre concerne également la transformation des films silicium AIC de type P (P-AIC) en matériau de type n (n-AIC) par diffusion à partir d'une solution siliçeuse contenant du phosphore. En variant les conditions expérimentales, des couches N^+ avec des concentrations de porteurs libres de 10^{19} à $6\times10^{20}cm^{-3}$ et des mobilités de $50\text{-}60cm^2/Vs$ ont pu être réalisées sur des couches de 0.2µm. Le dopage élevé de cette couche est essentiel pour assurer un champ arrière efficace, et également comme source de dopants lors de la croissance épitaxiale sur cette couche n-AIC.

Dans le chapitre 4, nous décrivons les deux méthodes de croissance de couches épaisses sur nos films p-AIC et n-AIC par épitaxie. L'épitaxie en phase solide a consisté dans le dépôt d'un film de silicium amorphe de 2µm d'épaisseur par CVD assisté par micro-onde (MW-CVD) suivi d'un recuit thermique conventionnel ou rapide (à lampes halogènes) mais à haute température (>900°C). Nous avons montré que la présence d'une grande concentration d'hydrogène dans la couche amorphe, qui exo-diffuse lors du recuit, ne permettait pas d'obtenir une bonne épitaxie. Par opposition, l'épitaxie en phase vapeur (VPE) consistant à craquer SiH_4 ou $SiH2Cl_2$ à haute température (>900°C) a permis d'obtenir des couches épitaxiales de très bonne qualité cristallographique. Grâce à des observations de morphologie et des analyses en micro-Raman, nous avons pu identifier également le taux de contraintes dans les couches en fonction des conditions d'épitaxie. Nous avons également suivi l'évolution

du dopant (aluminium, phosphore) dans les couches épitaxiales par SIMS ou par mesures électriques. Nous avons ainsi pu mettre en évidence la formation d'une distribution graduelle $n^{+}n$ très souhaitable pour les composants photovoltaïques.

La deuxième partie du chapitre 4 est consacrée aux cellules photovoltaïques tests, afin de tester la potentialité de tels matériaux pour une conversion efficace de l'énergie solaire. En particulier, les premières cellules réalisées sur des couches poly-silicium à base de p-AIC ont montré des rendements de 2.8% et 3.3% sur substrats d'alumine ou verre céramique. Comme attendu, nous avons mesuré un rendement de l'ordre de 5.5%, pour les cellules préparées par VPE sur couche tampon n-AIC. Il faut rappeler qu'aucun confinement optique ni architecture spécifique n'a été utilisé. Les caractéristiques impliquant les mesures des différentes grandeurs des cellules et la réponse spectrale, ont permis une analyse fine des régions de pertes de la conversion. Ces résultats photovoltaïques sont largement discutés en relation avec les propriétés des matériaux, et les améliorations sont proposées.

CHAPTER 1: INTRODUCTION

1.1 PHOTOVOLTAIC ENERGY SOURCE

Since 2003, total PV production grew in average by almost 50%, whereas the thin film segment – starting from a very low level – grew in average by over 80% and reached 400MW or 10% of total PV production in 2007. Production data for the global cell production in 2007 vary quite significantly between 3.733MW and 4.279MW (Figure 1.1) [1]. The Photovoltaic world market grew in terms of production by more than 60% in 2007 to approximately 4GW. The market for installed systems also grew more than 60% to reach 2.825MW. Like in the last years, Germany was the largest single market with 1.100 MW, followed by Spain with 341MW, Japan with 210MW and the US with 205MW.

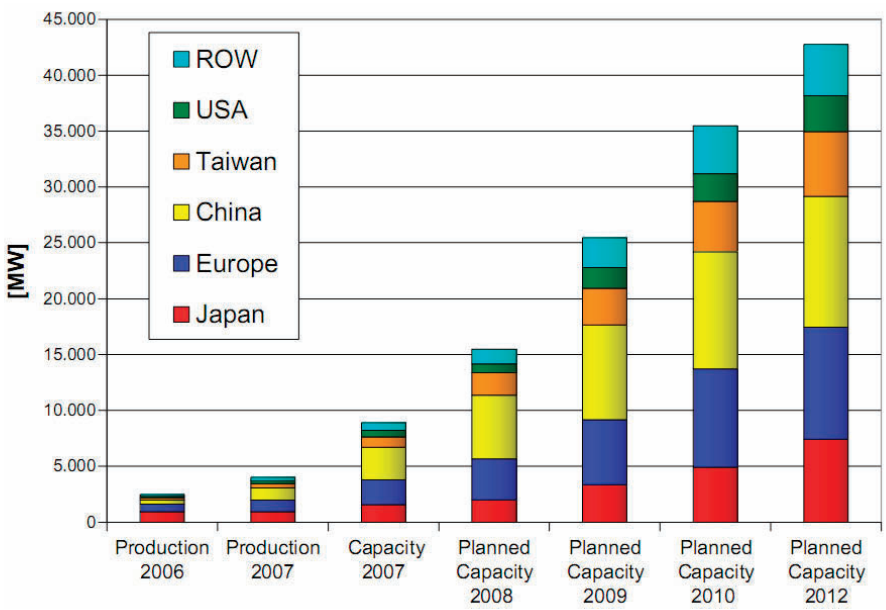


Figure 1.1: Worldwide PV Production 2006/7 and planned production capacity increases [1].

The Photovoltaic Energy Barometer reported that Europe had a cumulative installed PV system capacity of 4.7GW in 2007. Despite the fact that the European PV production grew again by almost 60% and reached 1040MW in 2007 while the Japanese market saw a further decline to 210 MW of new installations, 36% lower than in 2006. Then in 1998, progressive and supportive government policies in many European countries and in Japan resulted in a substantial increase in production. These policies were driven partly by a strong commitment to CO_2 reduction as proscribed by the Kyoto Protocol. Figure 1.1 shows the

announced and estimated increase of production capacities by 2006/7. Besides the exponential increase of the world market, the even more rapid increase of the Chinese production capacities is of particular interest. If the announced production increases can be realized, China will represent about 27% of the worldwide 42.8GW. Europe will then be second with almost 23% and Japan third with 17%.

About 90% of the current production uses wafer-based crystalline silicon technology. Up to now the main advantage of this technology was that complete production lines could be bought, installed and be up and producing within a relatively short time-frame. However, the ongoing shortage in silicon feedstock and the market entry of companies offering turn-key production lines for thin film solar cells led to a massive expansion of investments into thin film capacities. Thin film segment, starting from very low level, grew by almost 80% and reached 400MW or 10% of total PV production in 2007. The high growth rate of thin film production and the increase of the total production share indicate that the thin film technology is gaining more and more acceptance. For 2010, roughly 10.5GW of thin film production capacities are announced, an increase of almost 4GW compared to the 2009 figures. A thin film market share of 25 to 30% in 2010 seems not to be unrealistic. This takes into account the fact that more and more PV manufacturers are diversifying their production portfolio and that the current market leader First Solar will reach an annual production capacity of more than 1GW by 2010 [1]. Should the announced increases be realized, total production capacities in 2012 could then stand at 42.8GW, of which 15GW could be thin films as shown in Figure 1.2.

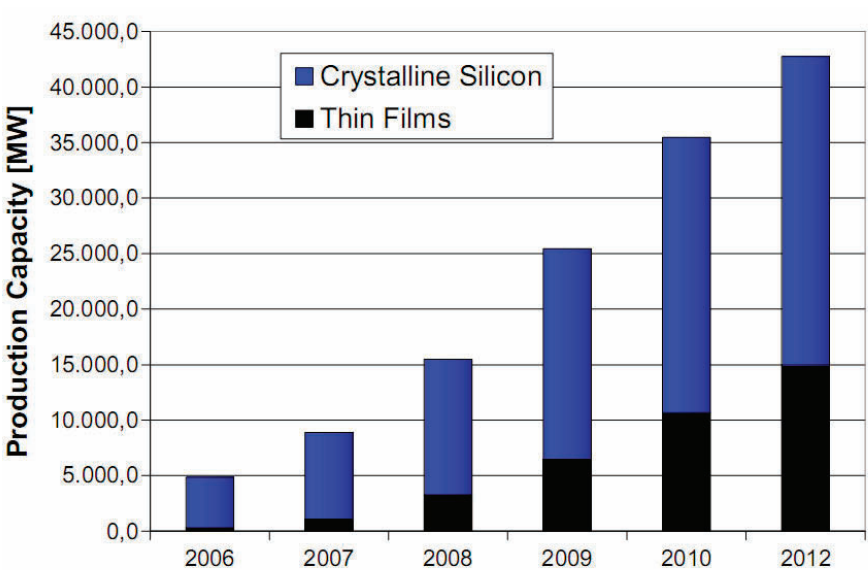


Figure 1.2: PV Production Capacities 2006 and planned production capacity increases [1].

The current solar cell technologies are well-established and provide a reliable product, with sufficient efficiency and energy output for at least 20 years of lifetime. This reliability, the increasing potential of electricity interruption due to grid overloads, as well as the rise of electricity prices from conventional energy sources, add to the attractiveness of Photovoltaic systems.

1.2 PHOTOVOLTAIC MATERIALS & TECHNOLOGIES

New products have been entering the market, enabling further cost reduction. Equally competitive technologies are amorphous/micromorph Silicon, CdTe and $Cu(In,Ga)(S,Se)_2$ thin films. In addition, dye-cells are getting ready to enter the market as well. The growth of these technologies is accelerated by the positive development of the PV market as a whole. The technology as well as the company distribution varies significantly as shown in Figure 1.3. The majority of 47 companies is silicon based. And year to year thin film production capacity increases.

1.2.1 Bulk Silicon Solar Cells

Figure 1.3 shows that c-Si, as either single or multicrystalline wafers or ribbons or amorphous Si/c-Si (heterojunction cells), was responsible for more than 90% of worldwide PV production in 2007. How did its dominance occur? First, there was a tremendous worldwide scientific and technical infrastructure for Si starting in the 1960s. Huge government and industrial investments were made in programs for understanding the chemical and electronic properties of Si, how to grow it with the required purity and crystalline structure, and to create the equipment needed to perform all the processing steps. The silicon band gap, of 1.1eV, is almost optimum to make a good solar converter. In addition, Si is one of the most abundant minerals in the Earth's crust. Thus, there was no physical limitation to providing a huge fraction of the Earth's electricity needs with the known Si reserves. However, for mechanical reasons (it is brittle), silicon requires relatively thick cells, with a typical wafer thickness of about 300µm. Therefore, some of the electrons pumped by the photons to the conduction band have to travel large distances, on the order of the thickness. Consequently, a good material with high chemical purity and structural perfection is required to fight the natural tendency of the conduction-band electrons to return to the valence band which is recombination. To process high-quality Si wafers, high-temperature treatments (>800°C) for the formation of pn junction, the anti-reflection layer

coating and the annealing of the contacts are necessary processes. The wafers are saw out of an ingot obtained by the float zone (Fz) or Czochralski (Cz) extrusion process for single crystalline, or by solidification for multicrystalline silicon materials.

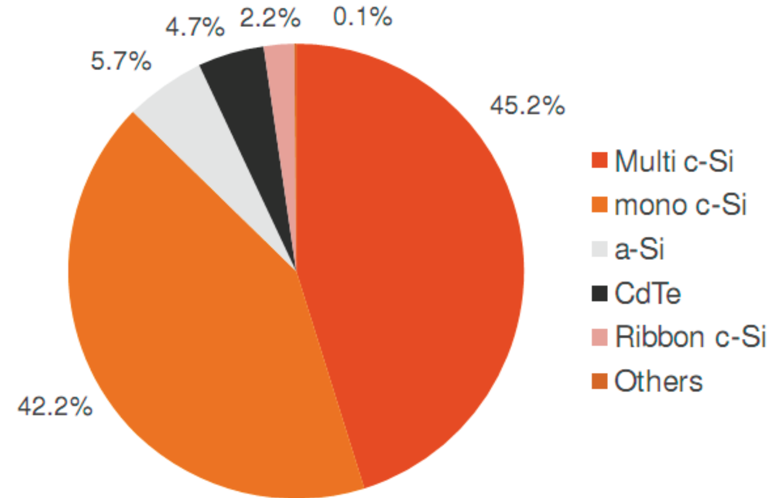


Figure 1.3: Cell technology market shares in 2007 [2].

An efficiency of 24.7% in UNSW has been achieved for single-crystal silicon laboratory cells in a long complex process where every possible efficiency-improving detail has been implemented to produce a complicated but nearly ideal device structure. However, most factories use some variation of the wafer and cell fabrication process, including the screen-printing process, which leads to 15% single crystal cells or 13% multicrystal cells. In modules, these efficiencies are reduced to 14% or 12%, mainly due to the redefinition of area that now includes the module frame. This process is considered the best compromise between costs and performance. The existence of the large efficiency gap between laboratory and commercial cells, together with the increasing markets, suggest that novel, high efficiency commercial cell processes will appear in the next years. Some companies (BP Solar or Sanyo, for instance) are already on this path and have different processes leading to 17 to 18% cells in production. The costs distribution for the industrialist is approximately 50% for material, 30% for setting in module and 20% for the processes of development of the cells [3]. The lowest (publicly offered) module selling prices in 2002 were about 3$/Wp. The wafer itself represents about 65% of the module cost, approximately equally divided between purification, crystallization, and sawing. An important advance in solar cell fabrication was the demonstration that solar cells with high efficiency can be fabricated from wafers containing hundreds of large-grain (1–10mm) multicrystals, called multicrystalline (multi-Si) or

polycrystalline (poly-Si), although this later term is less favored because it may cause confusion with the feedstock (polysilicon). The multi-Si growth procedure is much faster and the wafer is cheaper.

The loss of efficiency of a few percent (absolute) caused by the random orientation of crystalline grains in a multi-Si wafer compared to a single c-Si wafer is balanced by the lower cost so that the price per watt peak is the same on a module basis. But the simplicity of the multi-Si wafer-growing equipment and process is producing a clear trend towards the use of the multicrystalline option.

An interesting option in Si solar cell manufacturing is the growth of ribbons [4]. Ribbons do not require the expensive sawing process. However, the growth of the ribbon crystal is slower because they usually grow in the plane perpendicular to the ribbon surface, with very small area (the ribbon width times the thickness). In contrast, wafers grow in the plane of the wafer surface whose area is the wafer area. The standard ingot solidification process is a very effective purification process due to the preferential segregation of impurities to the molten silicon. However, in ribbon Si the plane of solidification moves faster (although with very small area), so the segregation is less effective. In summary, the ribbon cells are almost as good as the multicrystalline bulk-grown cells and possibly cheaper. Challenges lie in increasing the growth speed and the resulting cell efficiency.

In good single crystal Si cells, the manufacturing yield is 95%. Many supposedly cheap technologies find their Achilles' heel in the low yield. Finally, the module fabrication requires interconnecting and encapsulating the cells. These steps also have room for some cost reduction. The use of cheaper materials may help somewhat, as well as better automation, better module interconnection, and integration designs.

1.2.2 Thin Film Compound and Organic Solar Cells

a. Thin film compound solar cells:

Today's mainstream PV technology is based on crystalline Si wafers. This is robust and proven PV technology, however, its cost reduction potential seems limited. Due to greatly reduced semiconductor material consumption and ability to fabricate the solar cells on inexpensive large-area foreign substrates and to monolithically series-connect the fabricated cells, thin film PV has the potential of achieving module fabrication costs of well below 1€/Wp [5]. When Si is so well established a totally different semiconductor technology for photovoltaics are developed to achieve lower cost and improved manufacturability at larger

scales than could be envisioned for Si wafer-based modules. The c-Si that led to the early investigation and eventual commercialization of alternatives has the disadvantages since Si crystals were expensive and slow to grow. It was also recognized that of all the viable semiconductors, Si would require the greatest thickness to absorb sunlight, due to its unique optical properties. Si is the most weakly absorbing semiconductor used for solar cells because it has an indirect band gap while most of the other semiconductors have a direct band gap. Therefore, at least ten times more crystalline Si is needed to absorb a given fraction of sunlight compared to other semiconductors like GaAs, CdTe, $Cu(InGa)Se_2$, and even other forms of Si such as a-Si. Thicker semiconductor material means higher material volume, but also a higher quality material because of the longer paths that the high-energy electrons excited by the photons must travel before they are delivered to the external circuit to produce useful work. All this leads to high material cost.

The main advantage of thin film solar cells (TFSC) is that they will eventually have lower costs than c-Si-wafer PV technology when they are produced in sufficiently large volumes to off-set the initial capital investment. The lower costs of TFSC derive from the following characteristics: they are typically 100 times thinner than Si wafers (~1–3µm for all the semiconductor layers) deposited onto relatively low-cost substrates such as glass, metal foils, and plastics; they are deposited continuously over large areas at much lower temperature (200 to 500°C vs ~1400°C for c-Si); they can tolerate higher impurities (thus needing less expensive purification of raw materials); and they are easily integrated into a monolithic interconnected module. For a reference, the semiconductors in typical TFSC are 10 times thinner than a human hair. TFSC are either polycrystalline with small ~1µm sized grains such as $Cu(InGa)Se_2$ or CdTe, or else amorphous like a-Si. TFSCs typically consist of 5 to 10 different layers whose functions include reducing resistance, forming the pn junction, reducing reflection losses, and providing a robust layer for contacting and interconnection between cells.

The materials based on $CuInSe_2$ that are of interest for photovoltaic applications include several elements from groups I, III and VI in the periodic table. These semiconductors are especially attractive for TFSC application because of their high optical absorption coefficients and versatile optical and electrical characteristics which can in principle be manipulated and tuned for a specific need in a given device. CIS is an abbreviation for general chalcopyrite films of copper indium selenide (**C**u**I**n**S**e$_2$), CIGS mentioned below is a variation of CIS. CIS films (no Ga) achieved greater than 14% efficiency. However, manufacturing costs of CIS solar cells at present are high when compared with amorphous silicon solar cells

but continuing work is leading to more cost-effective production processes. The first large-scale production of CIS modules was started in 2006 in Germany by WURTZ Solar. Manufacturing techniques vary and include the use of Ultrasonic Nozzles for material deposition. Electro-Plating in other efficient technology to apply the CI(G)S layer.

When gallium is substituted for some of the indium in CIS, the material is referred to as CIGS, or copper indium/gallium diselenide, a solid mixture of the semiconductors $CuInSe_2$ and $CuGaSe_2$, often abbreviated by the chemical formula $CuIn_xGa_{(1-x)}Se_2$. Unlike the conventional silicon based solar cell, which can be modelled as a simple pn junction, these cells are best described by a more complex heterojunction model. The best efficiency of a thin-film solar cell as of March 2008 was 19.9% with CIGS absorber layer for small cells [6]. However, the technology has proved difficult to commercialise. The best commercial modules are presently 11-13% efficient. Higher efficiencies (around 30%) can be obtained by using optics to concentrate the incident light or by using multi-junction tandem solar cells. The use of gallium increases the optical bandgap of the CIGS layer as compared to pure CIS, thus increasing the open-circuit voltage, but decreasing the short circuit current. In another point of view, gallium is added to replace indium due to gallium's relative availability to indium. Approximately 70% of indium currently produced is used by the flat-screen monitor industry. However, the atomic ratio for Ga in the >19% efficient CIGS solar cells is ~7%, which corresponds to a bandgap of ~1.15eV. CIGS solar cells with higher Ga amounts have lower efficiency. For example, CGS solar cells, which have a bandgap of ~1.7eV, have a record efficiency of 9.5% for pure CGS and 10.2% for surface-modified CGS. The main technical issue of the CIS technology is associated with the complexity of the CIS absorber layer (a 5-element system), which imposes significant challenges for the realisation of uniform film properties across large-area substrates using high-throughput equipment. This affects the yield and the cost (€/Wp) of the modules. Other issues are the use of cadmium (as previously noted) and the use of the scarce element indium. Estimates indicate that all known reserves of indium would only be sufficient for the production of a few GWp of CIS PV modules [5].

Polycrystalline layers of CdTe have been investigated for photovoltaics since the 1970s. A CdTe solar cell is a solar cell based on CdTe, an efficient light-absorbing material for thin-film cells. Compared to other thin-film materials, CdTe is easier to deposit and more suitable for large-scale production. The pn junction is formed by first depositing an n-type layer of CdS on a transparent conductive oxide substrate followed by the CdTe layer and appropriate chemical annealing. Once the solar cell is made, the CdTe films are slightly p-type, typically, 2 to 8μm thick and have crystallites or grains on the order of 1μm. The highest

reported efficiency for solar cells based on thin films of CdTe is 18%, which was achieved by research at Sheffield Hallam University for small-area cells while the best commercial modules are presently 10-11% efficient. The main technical issue of the CdTe technology is related to the back contact. Specifically, the relatively light p-type doping of the CdTe layer complicates the realisation of a low-resistance, long-term-stable back contact. The standard method for realising the back contact structure of CdTe solar cells presently consists of chemical etching of the CdTe surface, followed by the deposition of a p^+-type buffer layer and then the metal film [7]. Another technical issue is the activation step, which involves a toxic atmosphere and thus should be modified or eliminated. The main issue of the CdTe PV technology, however, is related to the toxicity of Cd. Even if proper recycling of the modules is offered by the module manufacturers, it is questionable whether the production and deployment of Cd-based modules is sufficiently benign environmentally to justify their use instead of less problematic PV technologies. Furthermore, Te is a scarce element and hence, even if most of the annual global Te production is used for PV, CdTe PV module production seems limited to levels of a few GWp per year [5].

b. Organic solar cells:

Organic solar cells and Polymer solar cells are built from thin films (typically 100nm) of organic semiconductors such as polymers and small-molecule compounds like polyphenylene vinylene, copper phthalocyanine (a blue or green organic pigment) and carbon fullerenes and fullerene derivatives such as PCBM. Energy conversion efficiencies achieved to date using conductive polymers are low compared to inorganic materials, with the highest reported efficiency of 6.5% for a tandem cell architecture. However, these cells could be beneficial for some applications where mechanical flexibility and disposability are important.

These devices differ from inorganic semiconductor solar cells in that they do not rely on the large built-in electric field of a pn junction to separate the electrons and holes created when photons are absorbed. The active region of an organic device consists of two materials, one which acts as an electron donor and the other as an acceptor. When a photon is converted into an electron hole pair, typically in the donor material, the charges tend to remain bound in the form of an exciton, and are separated when the exciton diffuses to the donor-acceptor interface. The short exciton diffusion lengths of most polymer systems tend to limit the efficiency of such devices. Nanostructured interfaces, sometimes in the form of bulk heterojunctions, can improve performance. Additionally, the operational lifetime of organic solar cells must be improved to extend beyond 5 years.

1.2.3 Thin Film Silicon Solar Cells

A major cost limitation of the current dominant silicon solar cell technologies, which are fabricated using traditional monocrystalline and multicrystalline silicon based processes, is with the large volume of material used and the associated expensive assembly and interconnection methods required to produce the large area products required for substantial power generation. Thin-film 'coating' technologies, which avoid these problems, have achieved substantially lower manufacturing costs, but market acceptability has been compromised by the much lower power conversion efficiencies achieved so far.

Thin-film approaches aim to reach low cost by starting with a low-cost (or potentially low-cost) material system; a thin layer of semiconductor is deposited on a low-cost substrate. If high efficiency and reliability is indeed achieved, thin-film solar cell technologies could reach substantially lower costs, 0.5$/Wp and even below. Although thin-film solar cells have been announced for a long time as the next best thing, they have not yet had a breakthrough. The development of these technologies has in fact been rather slow, not faster than the bulk Si technology which, however, started much earlier. Recently, because of the Si feedstock shortage, the thin-film technologies have received new momentum. Because of the limited possibility to invest in conventional Si technology due to the shortage, substantial investment capital has flown into thin-film initiatives and led to the creation of many new companies [8].

Using Si for the active material instead of other semiconductors presents a number of advantages for thin-film technologies. Si is nontoxic, which makes it easily accepted by the public. Moreover, Si is abundantly available in the earth crust, so that its availability (at least in its raw form) will never be an issue. Finally, Si solar cell technologies can build further upon the extensive know-how accumulated over the years in the IC industry (for crystalline Si) and the display industry (for amorphous and microcrystalline Si). The term "thin-film crystalline Si" is in fact quite broad. It covers a wide range of technologies, from amorphous Si to monocrystalline lift-off Si solar cells.

Thin silicon solar cells is actually an umbrella term describing a wide variety of silicon photovoltaic device structures utilizing various forms of silicon (monocrystalline, multicrystalline, polycrystalline, microcrystalline, polymorphous, amorphous), and made with an almost incredibly diverse selection of deposition or crystal growth processes and fabrication techniques. Thin silicon solar cells are distinguished from traditional silicon solar cells that are comprised of ~0.3mm thick wafers or sheets of silicon. The common defining

feature of a thin silicon solar cell is a relatively thin (<0.1mm) "active" layer or film of silicon formed on, or attached to, a passive supporting substrate.

Silicon thin-film cells are mainly deposited by chemical vapor deposition (typically plasma-enhanced, PE-CVD) from silane gas and hydrogen gas. Depending on the deposition parameters, these silicon thin films can be based on one or a combination of these materials:

1. Amorphous silicon (a-Si or a-Si:H) or polymorphous silicon
2. Microcrystalline silicon
3. Polycrystalline silicon (poly-Si).

These silicon thin film materials can be characterized by their grain sizes ranging from none (amorphous) to large silicon (~100μm) for polysilicon. The crystalline silicon TF presents dangling and twisted bonds, which results in deep defects (energy levels in the bandgap) as well as deformation of the valence and conduction bands (band tails). The solar cells made from these materials tend to have lower energy conversion efficiency than bulk silicon, but are also less expensive to produce. However, recently, solutions to overcome the limitations of thin-film crystalline silicon have been developed. Light trapping schemes where the weakly absorbed long wavelength light is obliquely coupled into the silicon and traverses the film several times can significantly enhance the absorption of sunlight in the thin silicon films. Thermal processing techniques can significantly enhance the crystal quality of the silicon and thereby lead to higher efficiencies of the final solar cells.

i) Amorphous Silicon (a-Si:H) Solar Cells

Amorphous silicon (a-Si:H) is the best developed thin film material and has been in commercial production since 1980.

As a material for photovoltaics, it has been the advantages of relatively cheap, using layers of a-Si:H only a few hundreds nanometers thick, low temperature (<300°C) deposition and the possibility of growing on a variety of substrates, including glass and ceramics, metals such as stainless steel, and plastics. This means that they use less than 1% of the raw material (silicon) compared standard crystalline Silicon (c-Si) cells, leading to a significant cost saving. The amorphous nature has several important consequences for photovoltaics. Absorption of visible light is better than for crystalline silicon, but doping and charge transport are more difficult that limits the conversion of sunlight quite as efficiency. The availability of alloys with different band gap enables the design of heterostructure and tandem devices.

Unlike crystal silicon, in which atomic arrangements are regular, amorphous silicon features irregular atomic arrangements. For this reason, the reciprocal action between photons and silicon atoms occurs more frequently in amorphous silicon than in crystal silicon, allowing much more light to be absorbed. As a result, instead of the indirect bandgap of crystalline Si, it basically has a direct band gap. The absorption coefficient in a-Si is, therefore, much higher than that in crystalline Si, and, therefore, a much lower thickness is required to achieve the same absorption. However, the bandgap is also larger, 1.7 to 1.9eV. Therefore, a large part of the infrared light cannot be absorbed in amorphous Si. Alloys can be deposited by adding germanium (to forma-SiGe:H) or carbon (to form a-SiC:H) precursors to the gas flow, so that the bandgap can be tuned to some extent. Finally, amorphous cells with different light absorption properties deposited continuously, one on top of another, to capture the broad solar spectrum more effectively. This increases the energy conversion efficiency of the multi-cell device and improves performance stability.

Amorphous silicon films are fabricated using plasma vapor deposition techniques to apply silane (SiH_4) to the substrate or other beneficial film, allowing large-area solar cells to be fabricated much more easily than with conventional c-Si. Three amorphous silicon layers, p-layer, i-layer, and n-layer, are formed consecutively on the substrate.

The current status of a-Si:H is that: i) a-Si:H single junction p-i-n laboratory cells with highest confirmed stable efficiency of 10.1% as recently reported by Oerlikon Solar were obtained on low-cost, commercially mass-fabricated float line transparent conducting oxide (TCO) glass, ii) rapid deposition processes are being refined so that high rate, high quality can be achieved, iii) research into light degradation remedies will provide for cells with efficiencies comparable with c-Si cells, and iv) new applications for a-Si cells are being sought such as building-integrated PV, space power, consumer electronics, grid integration, and large scale power generation [9].

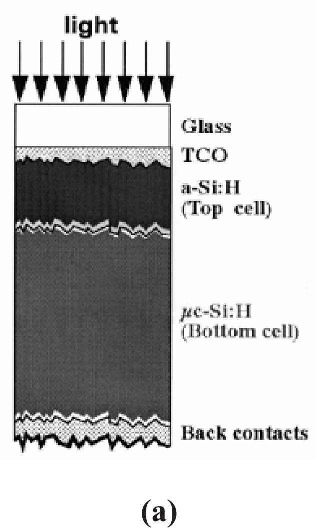
When silicon thin films are deposited by plasma enhanced chemical vapor deposition in a plasma regime close to powder formation, a new type of material, consisting of an amorphous matrix in which silicon nanocrystallites are embedded is obtained. This material, named hydrogenated polymorphous silicon (pm-Si:H), exhibits enhanced transport properties with respect to state-of-the-art hydrogenated amorphous silicon (a-Si:H). Hydrogenated polymorphous silicon has developed as an alternative to a-Si:H and its application to p-i-n solar cells has resulted in devices with improved stability, i.e. lower defect density and longer diffusion length. [10]. It has a lower initial and stabilized density of states, and a hole mobility

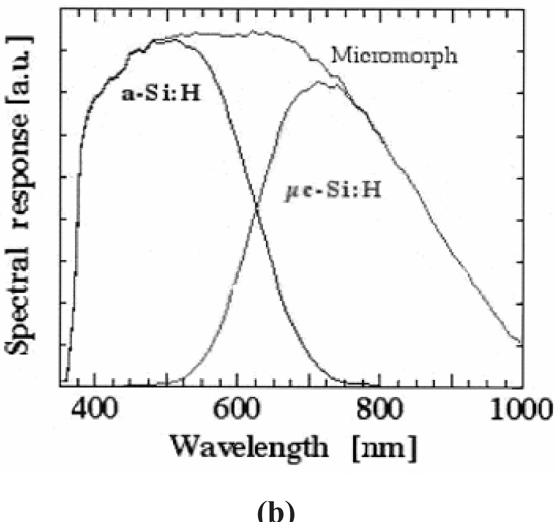
considerably higher than state-of-the-art a-Si:H, which makes this material an interesting candidate for solar cell applications. Stable single-junction p-i-n solar cells based on polymorphous silicon with efficiencies close to 10% were demonstrated [11].

ii) Micromorph (a-Si/µc-Si) Silicon Solar Cells

The silicon-based tandem concept based on superposing an amorphous and a microcrystalline silicon layer is commonly called the “micromorph” concept. The details on a-Si structure and formation were discussed above. When we consider the microcrystalline silicon (µc-Si:H) as component of the micromorph concept, microcrystalline Si is grown using a strong hydrogen dilution of silane. This material has an optical absorption coefficient quite similar to that of polycrystalline silicon and its optical bandgap energy is around 1.0eV [5]. It contains both amorphous and crystalline regions [12]. The columnar grains can be several 100nm wide and several µm long. The space between these crystalline grains is filled with amorphous silicon and/or voids. The crystalline volume content of the films depends on the deposition conditions, in particular the silane concentration in the gas mix. The regime around 6% silane concentration is called the “transition region” and gives the best µc-Si:H solar cells [13].

For micromorph tandem cell concept, amorphous and microcrystalline silicon pin based cells are used in a top and a bottom photovoltaic cell as depicted in Figure 1.4a. The industrial relevance of µc-Si:H solar cells improves enormously if they are combined with thin a-Si:H top cells, forming a 2-cell tandem stack in which the a-Si:H cell faces the sun. This device structure has been pioneered by University of Neuchatel in the 1990s. Sharp produces cells using this system in order to more efficiently capture blue light, increasing the efficiency of the cells during the time where there is no direct sunlight falling on them. The micromorph solar cell concept is the key for achieving high efficiency stabilized thin film silicon solar cells. Micromorph tandem solar cells showed under outdoor conditions higher short-circuit currents due to the enhanced blue spectra of real sun light and therefore higher efficiencies than under AM1.5 solar simulator conditions. Furthermore, a weak air mass dependence of the short-circuit current density could be observed for such micromorph tandem solar cells. It absorbs a broader spectrum of light as shown in Figure 1.4b since current matching (between top and bottom cell) is a crucial factor in tandem cells, the efficiency measured strongly depends on having a precise incoming light spectrum.





(a) **(b)**

Figure 1.4: (a) Schematic structure, and (b) corresponding spectral response of a typical micromorph tandem [13].

Tandem solar cells present an elegant way of obtaining higher efficiencies and overcoming the efficiency limits of single-junction cells. They are specially interesting for thin-film solar cells, and are presently widely used in the case of single-junction (SJ) a-Si:H solar cells. It must be notice that, the optimum top a-Si:H i-layer thickness is larger for tandem cells than for SJ cells because the slightly reduced or unaltered tandem cell current overcompensates a drop in FF.

From the practical technological point of view, a tandem cell is especially interesting, if the same deposition process and the same process temperature can be used for the bottom and for the top cell. This is the case for tandems containing amorphous silicon and amorphous silicon–germanium alloys. This is also the case for the combination of amorphous silicon and microcrystalline silicon.

From the theoretical point of view, a tandem cell is interesting if the bandgaps of the two partial cells can be properly adjusted. According to numerical calculations reported in [14] the optimal bandgap combination for a tandem cell would be $E_{g\text{-}top}$=1.73eV and $E_{g\text{-}bott}$=1.16eV. This is very near the actual bandgap combination obtained with an a-Si:H top cell and a μc-Si:H bottom cell. Therefore, provided all technological problems can be overcome, cell efficiencies significantly higher than those for single-junction μc-Si:H cells (i.e. significantly higher than 10%) should become possible for such a micromorph (μc-Si:H/ a-Si:H) tandem cell combination. Recent test results from Oerlikon Solar's pilot production line in Switzerland show that full-size Micromorph modules (1.4m^2) have 151W initial power or 11% initial power conversion efficiency.

However, there are several problems for micromorph cells presently faced fall into three categories. The first one is interface and interdiffusion problems, especially with respect to the critical tunnel junction between the two partial cells. The second problem is thickness-related problems. Because of the light-induced degradation (Staebler–Wronski effect) prevailing in a-Si:H solar cells, the amorphous top cell has to be kept thin (d_{top}≤0.3μm). In order to avoid long deposition times (of more than 1h), the microcrystalline bottom cell has also to be kept relatively thin (d_{bottom}≤2μm), as long as deposition rates for device-quality intrinsic μc-Si:H layers are not substantially over 10Å/s. Thus, the short-circuit densities obtained are rather low. The third and last one is light trapping problems. It is especially difficult to obtain effective light trapping for the *amorphous top cell*, unless an 'intermediate mirror' (e.g. an intermediate ZnO layer) between the top and the bottom cell, could be successfully used. This is one of the reasons why most of the early micromorph tandems have been top-cell limited [13].

iii) Polycrystalline (poly-Si) Silicon Solar Cells

Table 1.1 depicts the grain size range depending on the type of the silicon. In this table, polysilicon is defined as having a grain size between 1μm and 1mm. In any case, this type of material has much smaller grains than standard material used for solar cells, namely multicrystalline silicon, which confusingly is still often referred to as 'polycrystalline'. The grain size is, however, much larger than for the material commonly called 'microcrystalline silicon', but also 'nanocrystalline silicon', a material typically obtained by plasma enhanced chemical vapor deposition (PECVD) at very low temperature (~200°C). This material has a typical grain size of a few tens of nanometers, still contains a substantial fraction of amorphous silicon, and in fact has the best quality in the transition region between amorphous and microcrystalline. In contrast to microcrystalline silicon, this material does not contain any amorphous tissue, or only a very small amount (well below 1%). One could think that the border between microcrystalline and polycrystalline silicon is not very sharp. In practice, there is a very clear distinction between the two materials because polysilicon is very far from the amorphous-to-crystalline transition, and always involves much higher temperatures than those used for microcrystalline silicon. Furthermore, polycrystalline silicon is composed of many silicon crystalline grains of varied crystallographic orientation.

Presently, polysilicon is commonly used for the conducting gate materials in semiconductor devices such as MOSFETS. It has also a potential for large-scale photovoltaic devices. Thin-film polysilicon solar cells have active layers that are usually thinner than 5μm,

often about only 2μm. Hence, the use of polycrystalline silicon in the production of solar cells requires less material and therefore provides for higher profits and increased manufacturing throughput. Polycrystalline silicon does not need to be deposited on a silicon wafer to form a solar cell; rather it can be deposited on other-cheaper materials, thus reducing the cost. Not requiring a silicon wafer alleviates the silicon shortages occasionally faced by the microelectronics industry [15].

Type of Silicon	*Abbreviation*	*Crystal Size Range*	*Deposition Method*
Single-crystal silicon	sc-Si	>10cm	Czochralski, Float zone
Multicrystalline silicon	mc-Si	1mm – 10cm	Cast, sheet, ribbon
Polycrystalline silicon	poly-Si	1μm – 1mm	Chemical-vapor deposition (at High temperature ≥1000˚C)
Microcrystalline silicon	μc-Si	10nm – 1μm	Ex.: Plasma deposition
Nanocrystalline silicon	nc-Si	1 – 10nm	(at Low temperature <600˚C)

Table 1.1: Crystal size ranges and deposition methods depending on the crystal silicon

On the other hand, grain size has been shown to have an effect on the efficiency of polycrystalline silicon based solar cells. The solar cell efficiency increases with grain size. This effect is due to reduced recombination in the solar cell. Recombination, which is a limiting factor for current in a solar cell, occurs more prevalently at grain boundaries. Figure 1.5 shows the effect of grain size range on open-circuit voltage value. The larger grain size, higher V_{oc} is depicted. Additionally, thin-film solar cells of polycrystalline silicon can be manufactured with cost-beneficial deposition processes on inexpensive substrates. For instance, such solar cells can be deposited on a large-area, have a relatively high efficiency, and require less material in comparison to crystalline solar cells. As the technology does not require a thick transparent conducting oxide (TCO) layer to provide lateral conductance, it involves the least active material of all the traditional thin-films. Very effective light-trapping is the key to this minimal material use. Moreover, the key materials are silicon and its oxide and nitride rather than the complex and often metastable phases required by other thin-film technologies [16]. The other advantage is rapidly increasing performance, with small module efficiency presently in the 10–11% range, but improving steadily towards a value that appears

to lie in the 12–13% range. For instance, the best efficiency of thin film poly-Si obtained so far with this so-called CSG (Crystalline Silicon on Glass) technology is 10.4% with a 94-cm^2, 20-cell mini-module. The polysilicon devices show high manufacturing yields of >90%. CSG, where the polycrystalline silicon is 1-2µm, is noted for its stability and durability; the use of thin film techniques also contributes to a cost savings over bulk photovoltaics. Despite the numerous advantages over alternative design, production cost estimations on a per unit area basis show that these devices are comparable in cost to single-junction amorphous thin film cells [17]. Thereof, the progress of thin film polycrystalline silicon in the last few years has been very fast. Further, polycrystalline silicon solar cells can be interconnected in integrated fashion to form modules, are environmentally safe, and have excellent long-term stability.

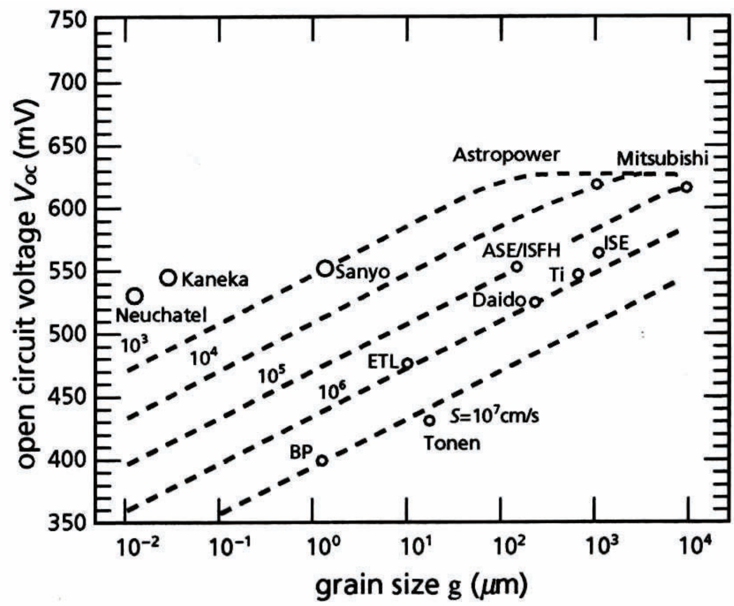


Figure 1.5: Grain size range dependent open circuit voltage results considering different technologies [18].

1.3 OBJECTIVE AND OUTLINE OF THE THESIS

The aim of this thesis is to fabricate p- and n-type polycrystalline silicon thin films by a combination of aluminium induced crystallization and epitaxy, and to study their structural, crystallographic and electrical properties in view of producing thin film silicon solar cells on foreign substrates. The manuscript is composed of four chapters:

In *Chapter 1*, we give an overview on the status of the photovoltaic industry as well as a brief description on the present materials and technologies used nowadays for the production of photovoltaic cells and modules. The advantages and particularities of the polycrystalline silicon based solar cells are closing this chapter.

Chapter 2 presents more extensively the crystallographic and electrical properties of the polycrystalline silicon material. In particular, the effect of the grains size, as well as grains distribution, and inter and grain defects types and density on the solar cell performances are shown. We have also displayed the various techniques of direct deposition and/or crystallization of amorphous or microcrystalline silicon to make large grains polycrystalline silicon layers. The Chapter 2 ends with a detailed overview on principles of metal-induced crystallization of amorphous silicon, more particularly the aluminium-induced crystallization (AIC) which is the skeleton of this thesis.

In *Chapter 3*, we present our experimental results on the crystallization kinetics and polysilicon growth on foreign substrates by the aluminium induced crystallization of a-Si. We investigated the effect of different experimental parameters on the crystallographic properties of the grown AIC polysilicon films on alumina or glass ceramic substrates, especially the crystallographic orientation, grain size and defects in the Si layers. Additionally, the formation of n-type AIC seed layer and the electrical analysis of n-type polycrystalline silicon films as a function of the phosphorus diffusion conditions are also studied.

Chapter 4 mainly focuses on the comprehensive results of epitaxial thickening methods on AIC seed layer and the performance of polysilicon solar cells. The limitations of cell performance in terms of dopants distribution and cell fabrication methods are discussed in this part.

In *Chapter 5*, the concluding remarks as well the prospectives of this work are presented.

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CHAPTER 2: POLYCRYSTALLINE SILICON THIN FILMS

2.1 PROPERTIES OF POLY-SI

Polycrystalline silicon films are composed of independent crystalline grains which are bounded by interfaces with the substrate or with the adjacent grains named as grain boundary. A schematic view of polycrystalline silicon on a substrate is shown in Figure 2.1. Their properties and characteristics are inherently those of the grains and grain boundaries. Therefore the grain structure is of importance in the application of polycrystalline thin films.

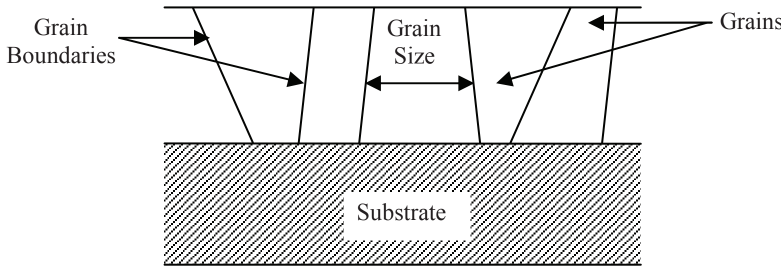


Figure 2.1: Schematic cross section of a polycrystalline silicon thin film on a substrate.

The silicon grains are arranged with random orientations to each other. The material is crystalline over the width of a grain, which is typically of the order of µm. Since the grains are large in terms of quantum mechanical, the band structure, and therefore the absorption coefficient, is virtually identical to that of the single crystal material. However the transport and recombination properties are strongly affected by the presence of the grain boundaries and intra-grains defects.

2.1.1 Crystallographic Properties of Polycrystalline Materials

A polycrystalline material is commonly formed of an aggregate of single crystal grains. The size of the grains can range from micrometres to being visible to the naked eye. Even within the single crystal grains the lattice is not perfect and can contain defects which have important effects on the mechanical and electrical behavior of the material. The microstructure of a material refers to the assemblage of grains together with other microscopic constituents such as pores and inclusions. Depending on the observe region, optical microscopy (OM), scanning electron microscopy (SEM), electron back scattering diffraction (EBSD) and transmission electron microscopy (TEM) are often used to examine the

microstructures. In particular, the EBSD technique can serve as a powerful tool to extract from the same data much information such as the texture, the grain sizes, the type of grain boundaries and the density of defects. As an example, Figure 2.2 displays surface images of the same area of a polycrystalline silicon film as deduced by EBSD.

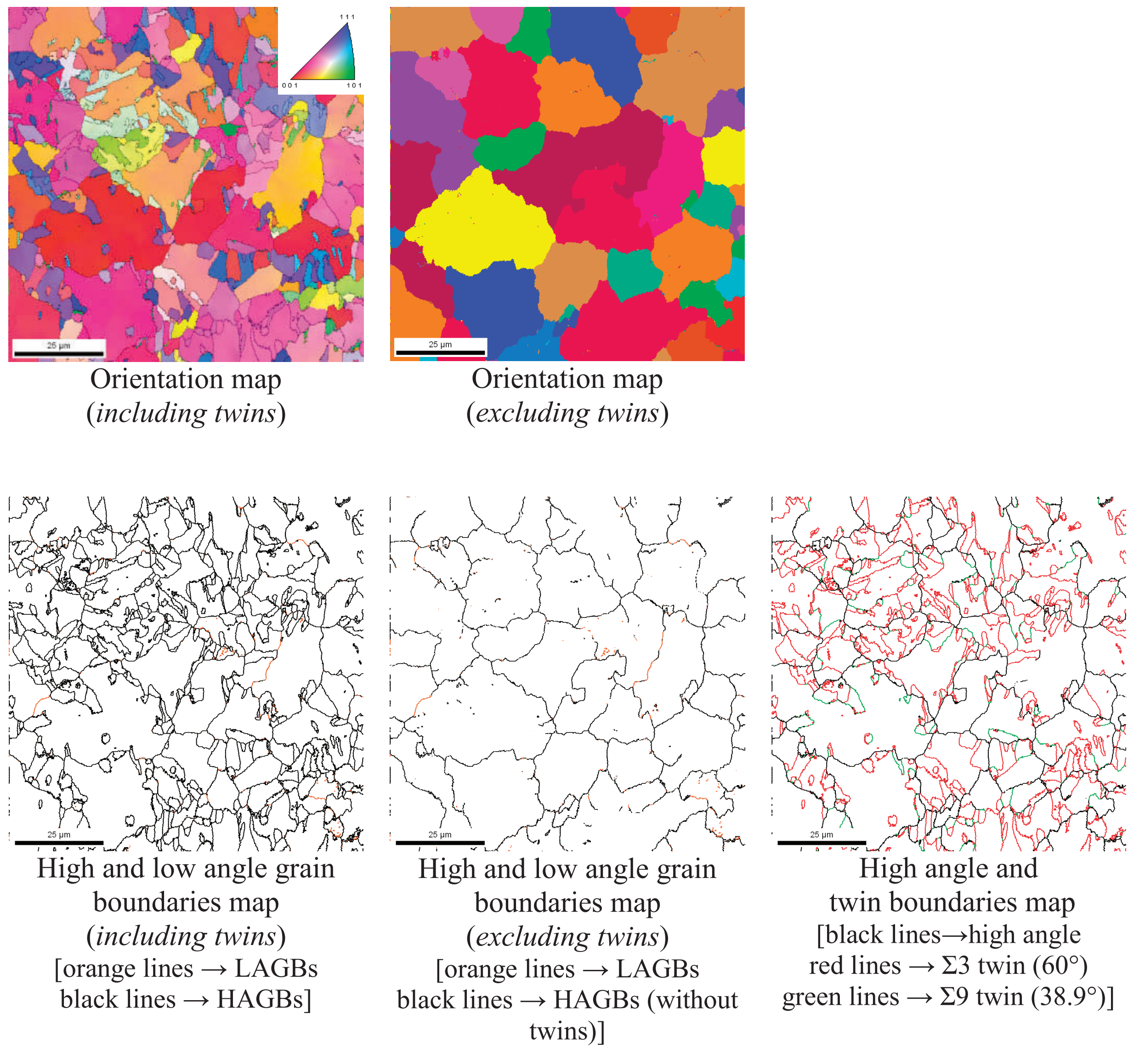


Figure 2.2: EBSD analysis of a polycrystalline silicon.

Each image of Figure 2.2 is providing a valuable information of the observed silicon surface ranging from the crystallographic orientation of each grain composing the layer to the type and density of intra-grains defects. Before to go into details, let's recall the definition of twins in crystalline materials in general.

Twinning represents a change in the crystal orientation across a twin plane, such that a certain symmetry exists across the plane. In case of a twin boundary, the atomic arrangements on each side of it are mirror images of each other without changing any bond lengths or bond

angles as shown in Figure 2.3. The symmetry of the lattice may permit the relationship to be established by other lattice transformations as well as the reflection operation. These lattice transformations are simply ways of mathematically transforming the lattice to the twin relation. Rotation twins occur when the lower crystal can be brought into correspondence with the upper section by a 60°, 90°, or 180° rotation. In addition to these relations there are others defined by various crystallographic operations.

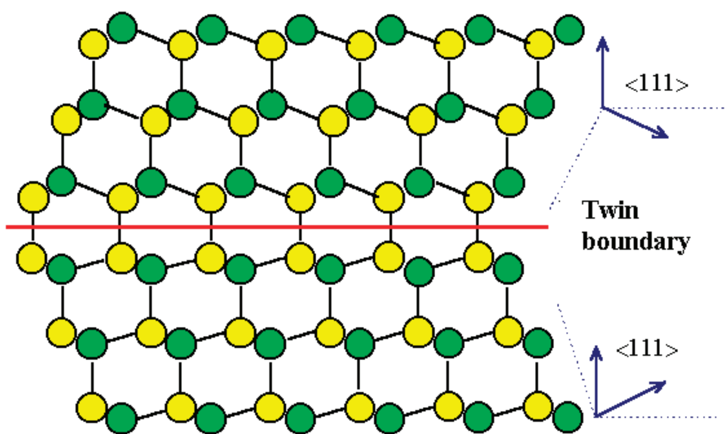


Figure 2.3: A schematic diagram of twinned crystals [1].

Figure 2.2a and 2.2b exhibit the crystalline orientation map of the grains including and excluding twins, respectively. The grains in polycrystalline materials are not usually oriented randomly. The grains often cluster close to certain orientations. The way in which the orientations cluster is called the texture. The different colors of the orientation map correspond to the different crystallographic orientations of the grains. The meaning of orientation of each is given by a color chart that is the inset figure of the orientation map including twins. When excluding the twin boundaries during the data plot, the grain size drastically increases. The crystalline orientation map gives thus information about the orientation of the grains and the preferred orientation of the surface. For example, the preferred orientation of the EBSD analyzed poly-Si film sample is <100>.

In polycrystalline materials, lattice misorientations between the adjoining, randomly oriented crystallites result in *grain boundaries* (see Figure 2.2c). A grain boundary represents a transition between crystals having no particular orientation relationship to one another. The grain boundary is considered as a two-dimensional defect, but in reality there is a specific thickness associated with this defect. In general, the grain boundaries contain high density of interface states that may trap free carriers, cause carrier scattering, and act as sink for the impurity segregation [2].

It is usually convenient to separate grain boundaries by the extent of the misorientation between the two grains:

➔ The low angle grain boundaries (LAGBs) are those with a misorientation less than about 11 degrees. Generally speaking they are composed of an array of dislocations and their properties and structure are a function of the misorientation.

➔ The high angle grain boundaries (HAGBs) whose misorientation is greater than about 11 degrees (the transition angle varies from 10-15 degrees depending on the material) are normally found to be independent of the misorientation. However there are "special boundaries" at particular orientations whose interfacial energies are notably lower than those of general HAGBs.

There are two types of LAGBs that are tilt and twist boundaries. The most simple boundary is that of a tilt boundary where the rotation axis is parallel to the boundary plane. This boundary can be conceived as forming from a single, contiguous crystallite or grain which is gradually bent by some external force. The energy associated with the elastic bending of the lattice can be reduced by inserting a dislocation, which is essentially a half-plane of atoms that act like a wedge, which creates a permanent misorientation between the two sides. As the grain is bent further, more and more dislocations must be introduced to accommodate the deformation resulting in a growing wall of dislocations - a low-angle boundary. The grain can now be considered to have split into two sub-grains of related crystallography but notably different orientations.

An alternative is a twist boundary where the misorientation occurs around an axis that is perpendicular to the boundary plane. This type of boundary incorporates two sets of screw dislocations. If the Burgers vectors of the dislocations are orthogonal then the dislocations do not strongly interact and form a square network. In other cases the dislocations may interact to form a more complex hexagonal structure. However, the majority of the low-angle grain boundaries are of tilt type, i.e. the rotation axis is located in boundary plane, parallel to the dislocations lines.

While the dislocations in the boundary remain isolated and distinct the boundary can be considered to be low-angle. If deformation continues the density of dislocations will increase and so reduce the spacing between neighbouring dislocations. Eventually, the cores of the dislocations will begin to overlap and the ordered nature of the boundary will begin to break down. At this point the boundary can be considered to be high-angle and the original grain to have separated into two entirely separate grains.

In comparison to LAGBs, high-angle grain boundaries (HAGBs) are considerably more disordered with large areas of poor fit and a comparatively open structure. For larger angles, i.e., for high-angle grain boundaries, the boundary structure cannot be resolved into dislocations and it must be analyzed as a defect in its own right. Indeed, they were originally thought to be some form of amorphous or even liquid layer between the grains. However, this model could not explain the observed strength of grain boundaries and, after the invention of electron microscopy, direct evidence of the grain structure meant the hypothesis had to be discarded. It is now accepted that a boundary consists of structural units which depend on both the misorientation of the two grains and the plane of the interface. The types of structural unit that exist can be related to the concept of the coincidence site lattice where regions of poor fit occur between points where the two lattices happen to fit together.

Certain high angle boundaries have a high symmetry, and many of the atom sites are common to both grains. These are often called special boundaries or *coincidence site lattices* (*CSL*), and an example of this is the twin boundary in the fcc structure. CSL model is to this day still one of the most successful attempts to describe special cases of high-angle grain boundary structure. CSL boundaries are low energy configurations and therefore more stable than general boundaries. Their boundary diffusivity is typically smaller than that of general grain boundaries. Boundaries are designated with a Σ number derived as the reciprocal of the fraction of coincident sites present. However, the CSL approach to identifying degradation-resistant boundaries has been criticized because the Σ value does not directly specify the crystallography at the boundary itself. The two factors that exert the most influence on the number of CSLs in a sample are the presence of a strong texture, resulting in Σ1 boundaries, and the amount of twinning, resulting in Σ3 and $\Sigma3^n$ boundaries. CSL boundaries are mainly twin boundaries of the first order (Σ3), second order (Σ9) and third order (Σ27). Note that the CSL designation is based entirely on the misorientation, and than the position of the grain boundary plane is secondary. The orientation and inclination of the boundary plane will however determine how many coincident sites that will actually be present inside the grain boundary, and can thus also play a major role in determining how stable the boundary is. Higher order twins are formed by the subsequent influence of twinning or by the reaction of lower order twins [3]. For example, the presence of a Σ9 boundary is usually the result of an encounter between two Σ3 boundaries according to the relationship of $\Sigma9 \rightarrow \Sigma3 + \Sigma3$ while the Σ27 boundary is formed by Σ3 and Σ9 boundaries like $\Sigma27 \rightarrow \Sigma3 + \Sigma9$ [4]. CSL boundaries generally present low-energy configurations compared to random grain boundaries [5]. Table 2.1 shows the geometrical details of main CSL boundaries where *UVW* and θ are the

misorientation axis and angle of boundary, respectively. Notice that only odd values of Σ arise for cubic crystal systems. Note also that in the general case the deviation from exact CSL will be on the axis as well as the angle of misorientation.

Knowledge of the density of these twins is very important in order to understand the formation of these twins and to improve the crystalline quality of the polycrystalline material. On the other hand, reports in the literature show that coherent first-order twins are electrically inactive. Higher order twins and faceted twin boundaries, e.g., coherent first-order twins with incoherent segments, are in most cases only weakly electrically active. A secondary dislocation network need not, but frequently does, lead to electronic levels in the band gap and thus to electrical activity in terms of minority carrier recombination and potential barriers. Thus these highly disordered grain boundaries, if not neutralized, could be detrimental for electronic transport in silicon solar cells devices.

Σ	*θ*	*UVW*	*Planes of Mirror Symmetry*	
3	60	111	111	211
9	38.94	110	221	411
27a	31.58	110	511	552
27b	35.42	210	721	

Tablo 2.1: Several important angle and axis of misorientations and twinning planes for CSL [6].

Twins or grain boundaries represent a large area discontinuity in the lattice. The crystal on either side of the discontinuity may be otherwise perfect. However the other important crystallographic impurity-related defects are due to the introduction of an impurity atom into the lattice.

2.1.2 Impurities in polycrystalline materials

Precipitates of impurity or dopant atoms constitute the other class of crystallographic defects. *Impurities* may introduce into a crystal during crystal growth, doping of the crystals and/or the formation of the contacts for solar cell applications. Every impurity introduced into a crystal has a certain energy levels that are shallow and deep levels. A deep level impurity may have several energy levels, with each energy level being either an acceptor state or a donor state. A deep level may act either as a trap or as a recombination centre. These deep-level traps act as recombination centers, which reduce the minority-carrier diffusion length

and depend on the impurity, temperature, and other doping conditions, for minority carriers in the junction space-charge region of the solar cells, and are responsible for the increase in the recombination current and the decrease of conversion efficiency [7]. Figure 2.4 shows the effect of presence of some impurities in n-type silicon based solar cells on the quantum efficiency. A very small amount of Mo in the silicon is enough to reduce drastically the efficiency while Al and Cu can be more tolerated. A special caution is therefore needed to avoid in-situ or ex-situ contaminations during processing. For polycrystalline silicon, some impurities have the ability to easily segregate at the grain boundaries or twins, affecting more strongly the cell efficiency. Additionally, it must be noticed that n-base devices are generally less affected by several impurities than are the corresponding p-base devices (not shown here) [8].

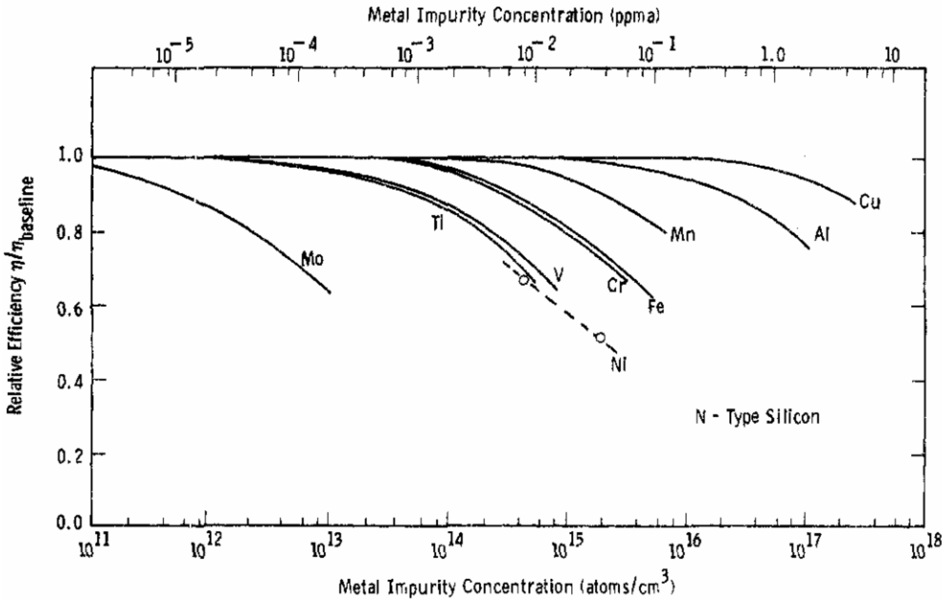


Figure 2.4: Solar-cell efficiency vs. impurity concentration for 1.5Ω.cm n-type silicon [8].

2.1.3 Electrical Properties

In the generally accepted model of polycrystalline silicon, the material is viewed as composed of small crystallites jointed together by grain boundaries [9,10], as shown in Figure 2.5. Inside each crystallite, the atoms are arranged in a periodic manner forming small single crystals, while the grain boundaries are composite of disordered atoms and contain large number of defects due to incomplete bonding. The high concentration of defect and dangling bonds at the grain boundaries are the origin of the trapping states and the dopant segregation sites around which the carrier-trapping and dopant-segregation models were developed.

Furthermore, the electrical transport properties of polycrystalline silicon films are governed by carrier trapping at the grain boundaries.

When current is flowing across a grain boundary, the potential barriers slow down the transport of the majority carriers, limiting the majority carrier mobility, while the potential wells drive minority carriers towards recombination centers at the grain boundary, reducing the minority carrier diffusion length and life time. The size of these effects depends upon the doping, the density of interface states and photogenerated carrier density.

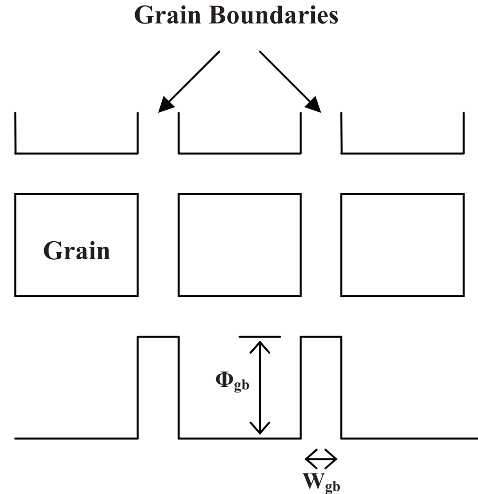


Figure 2.5: Schematic representation of potential barriers generated by the grain boundaries.

In order to model the effect of the grain boundaries on the electrical properties of polycrystalline silicon, some basic assumptions about the properties of the grain boundaries have to be made [11]. As a first one, the nature of the grain-boundary material can be considered to be between that of a completely ordered single crystal and that of highly disordered amorphous material. Therefore, the energy gap of the grain boundary material (1.5-1.6eV) can be expected to be somewhat larger than the energy gap of the single crystalline silicon (within 1.12eV) crystallites. Secondly, the high concentration of defects and dangling bonds at the grain boundaries provide ideal sites at which each donor dopant atom (for n-type material) at the grain boundary could have all of its five bonds saturated. Consequently, the dopant atoms at the grain boundaries have no weakly bound carriers, and the Fermi level is pinned near band gap at the grain boundaries. As a result of these assumptions, a heterojunction is formed at the interface between a crystallite and a grain boundary, with the grain-boundary material behaving as an intrinsic wide-band-gap

semiconductor. Therefore, the effect of the grain boundaries can be modeled by potential barriers, as shown in Figure 2.6 for n-type polycrystalline silicon.

In this figure, the height of potential barriers $q\Phi_{gb}$, relative to the Fermi level, is equal to $E_{gb}/2$, where E_{gb} is the band gap of the grain-boundary material, and the width of each of these potential barriers W_{gb} is approximately equal to the width of grain boundary. Thus in order to move from one crystallite to another, the carriers have to either tunnel through a grain-boundary barrier or be sufficiently energetic to be thermally emitted over the barrier.

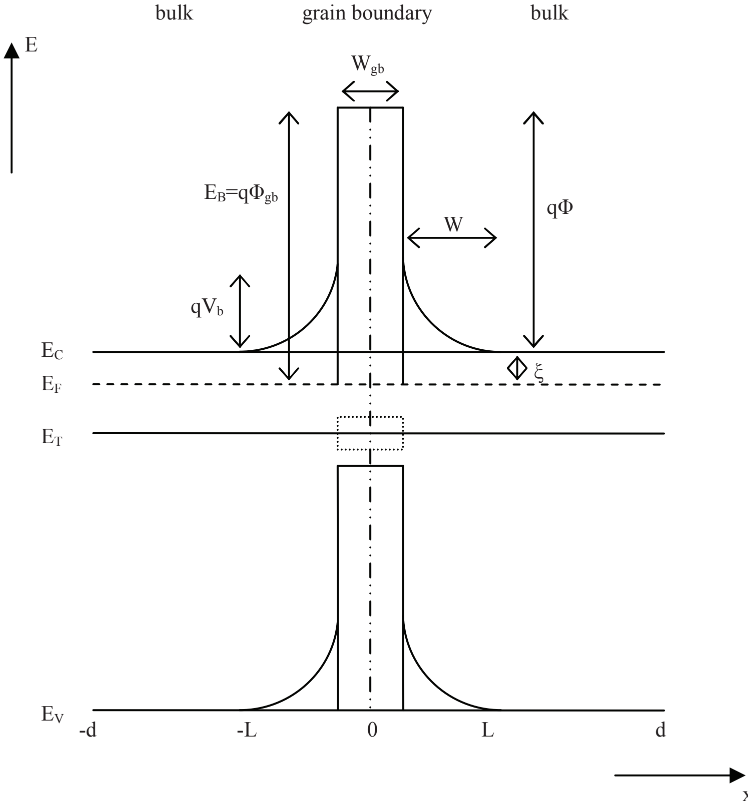


Figure 2.6: Energy band diagram for n-type polycrystalline silicon near a grain boundary under zero applied voltage

The high concentration of defects and dangling bonds at the grain boundaries cause trapping states capable of immobilizing both dopant atoms and charge carriers. As a result, a portion of the dopant atoms segregate to the grain boundaries where they are trapped and become electrically inactive [12,13]. The remaining dopant atoms can be distributed uniformly within the grains and can be ionized. Some of the resulting carriers are trapped at the grain boundaries, depleting a portion of each grain and creating additional potential-energy barriers in the depleted regions of the grains near the grain boundaries as shown in Figure 2.6 [14,15].

The potential energy in the depletion region has a maximum value qV_b given by:

$$qV_b = q^2 \frac{Q_t^2}{8\varepsilon N_G} \quad (2.1)$$

where Q_t (cm^{-2}) is the density of trapping states at the grain boundaries, and N_G is the average dopant concentration remaining in the grains after considering the dopant segregation at the grain boundaries. The minority carriers, whose forward-directed kinetic energies are less than qV_b, have insufficient energy to overcome the potential barrier, are trapped on their original side of junction and cannot contribute to the diffusion current, reducing thus the solar cell performance. The diffusion current increases if the potential barrier decreases. The Q_t and N_G have a significant influence on the potential barrier. In this case, considering Equation 2.1, density of traps should be decreased and/or average dopant concentration should be increased to reduce the potential barrier, i.e. to improve the cell performance.

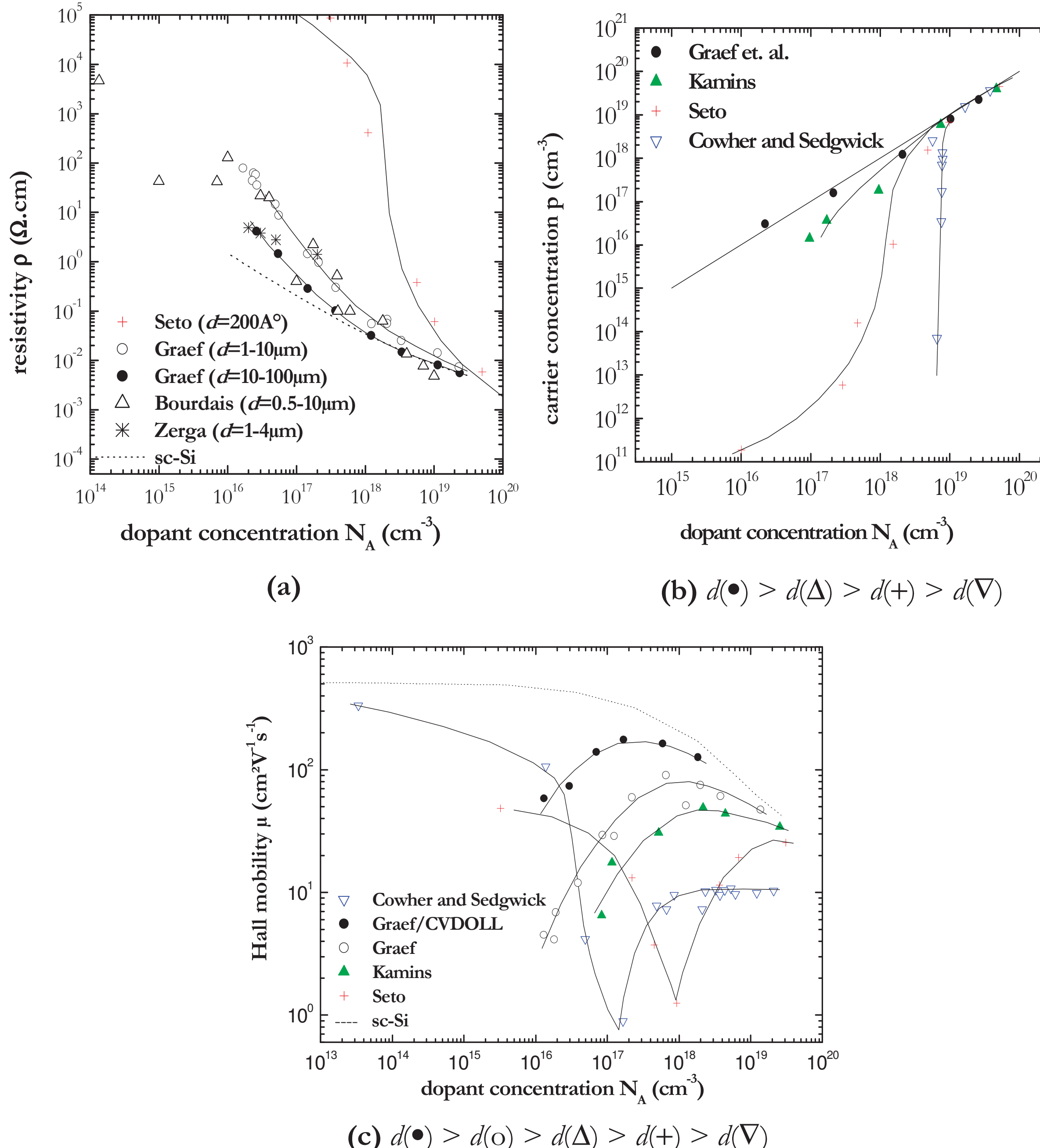
To enables the solution of the carrier transport problem in the silicon and hence the characterization of the device performance, the majority and minority carrier transport in polysilicon should be defined.

i) Majority carrier transport

In polysilicon, carrier mobilities and lifetimes depend not only on doping concentration and temperature but also on grain microstructure. It is widely viewed that transport parameters inside grains are the same as those in monosilicon, but that behavior of carrier mobilities and lifetimes at the grain boundaries are quite different from those in monosilicon. The polysilicon mobility and lifetime values are combinations of the values within the grains and at the grain boundaries. For this reason, parameters of majority carriers' transport in polycrystalline silicon reveal significant differences compared to those of single-crystalline silicon as depicted Figure 2.7. These differences depend on the doping concentration and grain size of polycrystalline material.

In Figure 2.7a, it is noted that the resistivity ρ of polysilicon silicon is significantly higher compared to that of single-crystalline silicon in particularly at low levels of doping. This difference is even more important when the grain size d is small. However, the concentration of carriers in single crystal silicon is equal to the concentration of dopants (Figure 2.7b), whereas it remains very low levels below the doping of polycrystalline silicon. For large grain sizes, it is comparable to that of monocrystalline silicon. This is mainly due to trapping of carriers at the grain boundaries. Furthermore, at low dopant concentrations, the

mobility increases as the doping is increased but the mobility is always much smaller than that in sc-Si (Figure 2.7c).



(a)

(b) $d(\bullet) > d(\Delta) > d(+) > d(\nabla)$

(c) $d(\bullet) > d(\mathrm{o}) > d(\Delta) > d(+) > d(\nabla)$

Figure 2.7: Influence of grain size and doping concentration on the of transport properties of majority carriers in the p-type polycrystalline silicon: (a) Resistivity, (b) Concentration of carriers, and (c) Mobility. (according to Seto [9], Graef [16,17], Kamins [18], Cowher and Sedgwick [19], Bourdais [20], Zerga [21])

In literature, several authors have attempted to explain the differences in transport parameters only by the dopant segregation phenomenon for p-type poly-Si. Unfortunately,

this only justifies partly the differences in the resistivity or the carrier concentration and it provides no satisfactory explanation to the existence of the minimum mobility at intermediate doping range. Therefore, additional work modeling parameters of transport in polycrystalline silicon have been developed by incorporating the mechanism of free carriers trapping at the recombination centers located in the grain boundaries.

According to Seto [9], there is a critical ratio (N^*) between the density of traps located at grain Q_t and grain size d. This report revealed three possible cases depending on the level of doping N_A as shown in Figure 2.8.

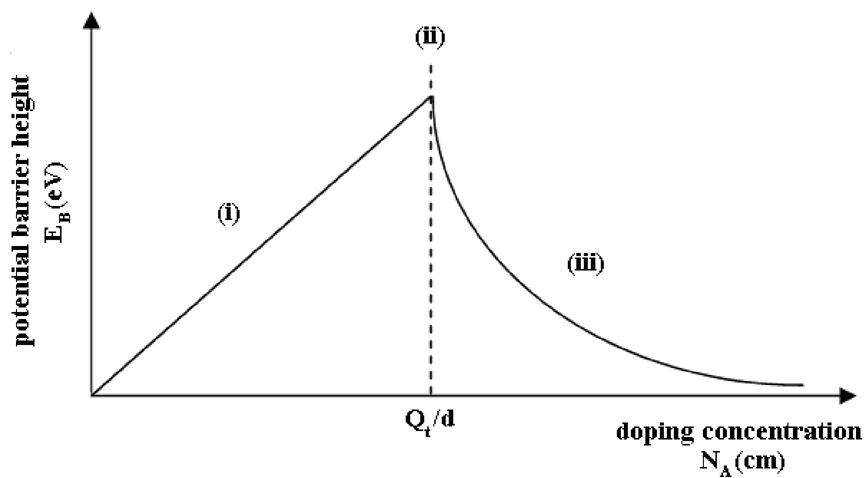


Figure 2.8: Potential barrier as a function of doping concentration for Seto model [9].

According to Seto model, the three different areas of the potential barrier E_B depending on the doping level N_A in Figure 2.8 are interpreted as follows:

(i) When the doping level is low ($N_A < Q_t/d$), all majority carriers are trapped at the interface states at the grain boundaries (grains depleted completely), which results in a extremely low carrier concentration and dominated by high resistivity.

(ii) $N_A = N^* = Q_t/d$ is an intermediate situation where majority carriers in the grains and traps at the grain boundaries are cancelled exactly. This is reflected by a sharp drop in mobility (Figure 2.7c). Indeed, it is found that the grain size increases where the minimum mobility shifts to the low doping concentrations (and also the reduction of free carriers).

(iii) For high doping levels ($N_A > Q_t/d$), all traps are saturated and the space charge region is no longer occupy. It is a neutral zone in the grain where the density of carriers to be confused with the concentration of dopants. This gives a density of free carriers of all material closing to that of single-crystalline as doping increases or the depletion region shrinks.

Martinez et al [22] have developed a theoretical model for the calculation of resistivity and mobility of majority carriers in multicrystalline silicon. They used the grain resistivity ρ_{gb} and width of space charge region $2L$ and the resistivity of the grain considered as a single-crystal. The resistivity depends obviously on the density of grain boundaries and, thus, of the grain size d:

$$\rho = \frac{2L}{\varphi}\rho_{gb} + \left(1 - \frac{2L}{\varphi}\right)\rho_{mono} \tag{2.2}$$

This expression is general and applies also when the grain is completely depleted. In this case we have $2L = d$ and remains only the term related to the resistivity for the grain boundaries (ρ_{gb}). However, it must be noticed that if the grain is not completely depleted, the negative contribution of the grain boundaries is reduced directly by increasing the grain size.

According to Seto's theory, the dominant transport mechanism in polycrystalline silicon film is the thermionic emission over the barriers. When the voltage applied to the crystallite is small, that is $V \ll kT/q$, the thermoionic theory leads to the following expression of the current density [Seto]:

$$J = \frac{q^2 N_C v_c}{kT}\exp\left[-\frac{\left(E_G/2 + E_B - E_F\right)}{kT}\right]V \tag{2.3}$$

where E_G is the band-gap energy, E_B is the barrier height, E_F is the Fermi energy referred to the intrinsic Fermi level in the neutral region, N_C is the effective density of states relative to the conduction band, and $v_c=(kT/2\pi m^*)^{1/2}$ is the collection velocity.

To explain the electrical properties of poly-Si, two basic models are mainly considered; carrier trapping model and dopant segregation model [11]. The first model, the carrier-trapping model, postulates that the dopant atoms are uniformly distributed throughout the material and that conductivity is limited by carrier trapping at the grain boundaries, where the trapped carriers create potential barriers which impede the transport of free carriers between the grains [23,24]. The high resistivity observed at low dopant concentrations is explained by the trapping of most of the carriers at grain boundaries, leaving few free to contribute to the conduction. As the dopant concentration is increased, the number of trapped carriers increases and eventually approaches saturation. Upon further increase in dopant concentration, the number of trapped carriers does not increase appreciably; consequently, the potential barriers decrease, resulting in a sharp reduction in resistivity. Finally, at high dopant concentrations, the potential barriers at the grain boundaries become very small and no longer

limit the conductivity of the samples, and the properties of the material approach those of the grains.

The second model, the dopant-segregation model, as developed by Cowher and Sedgwick [19] and Fripp and Slack [25], hypothesizes that conductivity is controlled by the segregation of dopant atoms to the grain boundaries, where the atoms themselves are trapped and become electrically inactive. Here the variation in the resistivity is explained by the hypothesis that, for low dopant concentrations, most of the atoms segregate to the grain boundaries, leaving few to contribute to conduction. As the dopant concentration is increased, more atoms remain inside the grains, and thus the resistivity approaches that of single-crystal silicon.

Although both models were successful in explaining the variation of resistivity with total dopant concentration, the carrier-trapping model has been more generally accepted because the dopant-segregation model cannot explain either the temperature dependence of the film resistivity or the minimum in Hall mobility observed at intermediate dopant concentrations.

ii) Minority carrier transport

Transport properties of the minority carriers (lifetime, diffusion length) play an important role in determining the photovoltaic performances of solar cells. In the case of polycrystalline silicon, these properties depend not only on the crystalline quality, purity grain size, doping, but also and especially of the electrical activity of the grain such as recombination of the minority carriers at the grain boundaries.

In semiconductor physics, photons with the energy greater than or equal to the width of the band gap E_G are absorbed and generate electrons - holes pairs. However, an excess of carriers (Δn, Δp) forms the balance between the generation rate G (cm^{-3}s^{-1}) and recombination rate U_R (cm^{-3}s^{-1}). The mechanism of recombination of the minority carriers in n-type material is characterized by the lifetime τ:

$$U_R = \frac{\Delta p}{\tau_p} \tag{2.4}$$

where $1/\tau_p$ is a constant. This leads us to a simple differential equation governing the recombination process as:

$$\frac{d\Delta p}{dt} = G - U_R = G - \frac{\Delta p}{\tau_p} \tag{2.5}$$

This recombination process mainly depends on the material, level of doping and the density of trap states in the band gap. There are mainly three recombination processes in semiconductors [26]: (i) direct band-to-band radiative recombination, (ii) indirect phonon-assisted recombination (Shockley–Read–Hall (SRH) recombination) and (iii) Auger recombination. Of these, the first two processes are two-carrier processes while the third one is a three-carrier process.

In indirect recombination (SRH recombination) process, an electron in the conduction band falls down to an intermediate energy level in the band gap. Then a hole ascends from the valence band to the intermediate level, followed by electron–hole recombination. This can also be considered as a two-stage or two-step fall of the electron: in the first step from the conduction band to an intermediate state and in the second step from the intermediate state to the valence band. These intermediate states behave symmetrically as sites for recombination and generation of carriers. Hence, they are called recombination– generation centers or simply recombination centers, for brevity.

In Auger recombination process, three carriers participate, either two electrons and one hole, or two holes and one electron. The momentum of the two recombining carriers and the energy liberated during recombination are imparted to the third surviving carrier.

Direct band-to-band radiative recombination process occurs in direct band gap semiconductors like GaAs, GaAsP, InP, etc., which are therefore used for the fabrication of optoelectronic devices. But it is unlikely in indirect bandgap semiconductors such as Si and Ge. This is difficult to understand from the E-x energy band model but is readily evident on examining the E–k plots for the above semiconductors. Therefore changes in crystal momentum must also be considered. In direct band gap semiconductors like GaAs, the conduction band minimum and valence band maximum are both located at k=0 while in indirect band gap semiconductors such as Si and Ge, they lie at different values of k. Thus in a direct band gap semiconductor, both energy and momentum conservation conditions are met by photon emission whereas in an indirect band gap semiconductor, the involvement of phonon is mandatory to account for the large change in crystal momentum accompanying the recombination process. Recombination requiring the conservation of both energy and momentum is not possible without phonon emission, i.e., without interaction with the lattice.

Each of the above recombination processes has a lifetime associated with it. Thus, effective lifetime τ_{eff} in the volume of silicon depends on the lifetimes corresponding to mechanisms of recombination by SRH traps (τ_{SRH}), radiative (τ_{rad}) and Auger (τ_{Aug}) and given by:

$$\frac{1}{\tau_{eff}} = \sum_i \frac{1}{\tau_i} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Aug}} \tag{2.6}$$

When we consider polycrystalline silicon, there are three important components for the recombination of minority carriers. These contributions can be in grain, along the grain boundaries and at the surface. The polysilicon lifetime is the combinations of the values within the grains and at the grain boundaries due to the grain the different behavior of lifetimes at the grain boundaries.

In particular, significant recombination takes place at the grain boundaries in polysilicon. At equilibrium, net grain boundary recombination is zero. Under increasing illumination, the net charge at the grain boundary decreases so that the barrier height decreases, and the enhancement of the recombination rate due to the decrease of depletion region.

To evaluate the overall effect on the minority carrier transport characteristics, the grain boundary recombination effect must be added to other principal recombination mechanisms. We can define a minority carrier lifetime for a grain boundary recombination from the grain boundary recombination rate per grain, (i.e., a volume recombination rate)

$$\frac{1}{\tau_{gb}} = \frac{S_{gb}}{d} \tag{2.7}$$

where S_{gb} is the effective interface recombination velocity and d is the grain size. Then an effective minority carrier lifetime τ_{eff} for the polycrystalline silicon can be defined by adding grain boundary recombination to the other mechanisms,

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Aug}} + \frac{1}{\tau_{gb}} \tag{2.8}$$

According to this expression, lifetime in the polycrystalline silicon is proportional to the grain size d. Figure 2.9 illustrates the influence of grain size on the duration of effective lifetime for the polycrystalline silicon, according to the model of Ghosh et. al.[27].

An effective diffusion length L_{eff} of polycrystalline silicon can be derived from τ_{eff} in the usual way,

$$L_{eff} = \sqrt{D_{eff}\tau_{eff}} \tag{2.9}$$

When the grain boundary recombination dominates, i.e. low doping, high grain boundary defect density and low illumination, the overall effective lifetime and diffusion length will be bias and intensity dependent, through the bias dependence of S_{eff}. At higher

intensity levels the other mechanisms take over, and L_{eff} increases towards a saturation value. In polycrystalline silicon, L_{eff} has been observed to increase with generation rate up to a saturation level.

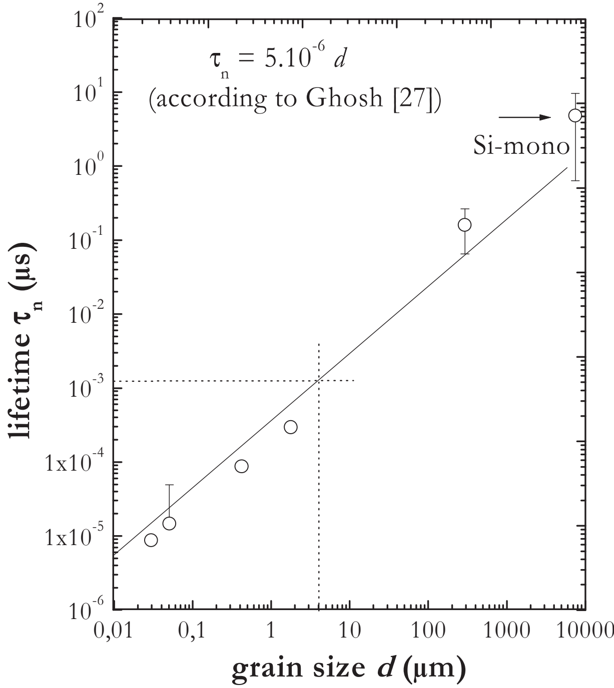


Figure 2.9: Influence of grain size on the effective lifetime for p-type polycrystalline silicon.

iii) Comparison of electrical properties of n-type and p-type Si materials

a. Resistivity and mobility:

The electrical characteristics of n-type poly-Si show that its properties are different from those of p-type poly-Si. The peculiar behaviour of resistivity is shown in Figure 2.10a. The resistivity of a polycrystalline material either for n-type or p-type is high at low doping levels, falling very rapidly at some intermediate doping levels until finally it compares with crystalline values at high doping concentrations. However, for dopant concentrations between 10^{17}-10^{20}cm^{-3}, the n-type and p-type poly-Si materials exhibit a significant difference. In this dopant range n-type poly-Si has lower resistivity compared to that of p-type poly-Si.

Figure 2.10b depicts the room-temperature carrier Hall mobility as a function of annealing temperature that activates and redistributes implanted dopant atoms. Polycrystalline silicon films doped by ion implantation with arsenic, phosphorus and boron with an average dopant concentration of 2×10^{19}cm^{-3} were studied. As shown the mobility increases from its

initial 1000°C value (dashed lines) on additional annealing at lower temperatures (solid lines). Furthermore, the carrier Hall mobility is found to be significantly higher in phosphorus doped poly-Si films then in films doped with arsenic and boron with the same total dopant concentration. It was found that the Hall mobility of phosphorus doped poly-Si films (n-type) are almost 3 times more than that of boron doped films (p-type).

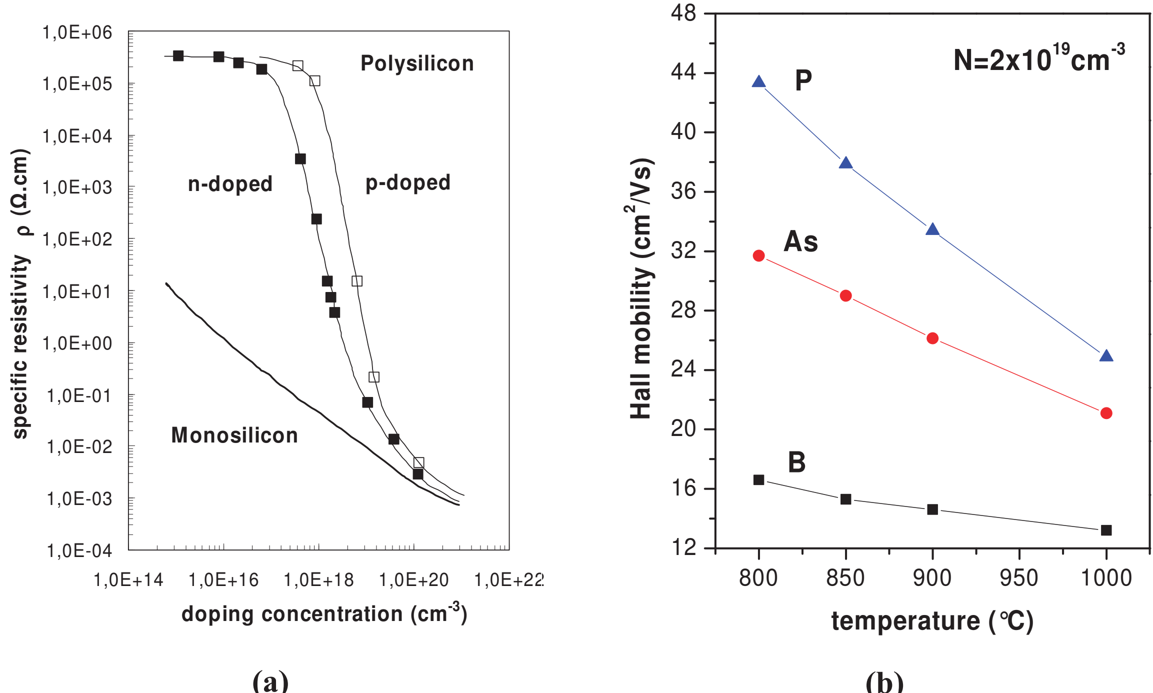


Figure 2.10: (a) Resistivity of polysilicon and monosilicon as a function of doping level (according to Moller [28]), and (b) Room temperature mobility poly-Si films as a function of annealing (according to Mandurah et. al. [11]).

b. Minority carrier lifetime and diffusion length:

The measurements of minority carrier lifetime are lacking in literature. The comparison between p- and n-type silicon minority carrier properties will be done here using the properties of single crystalline (sc-Si) or multicrystalline (mc-Si) materials or cells.

Figure 2.11a and 11b shows the doping concentration dependent minority carrier properties in sc-Si at 300K. Lifetime (Figure 2.11a) and diffusion length (Figure 2.11b) are plotted as a function of hole concentration for n-type silicon and electron concentration for p-type silicon. These data are deduced from Ref. [29].

As depicted from both figures the minority carrier lifetime and diffusion length for n-type silicon are significantly higher compared to those of p-type material. Especially for lower

donor concentrations (10^{17}-$10^{18}cm^{-3}$), the difference in diffusion length is quite important. According to these results, using n-type polycrystalline material might lead to improved solar cells performances.

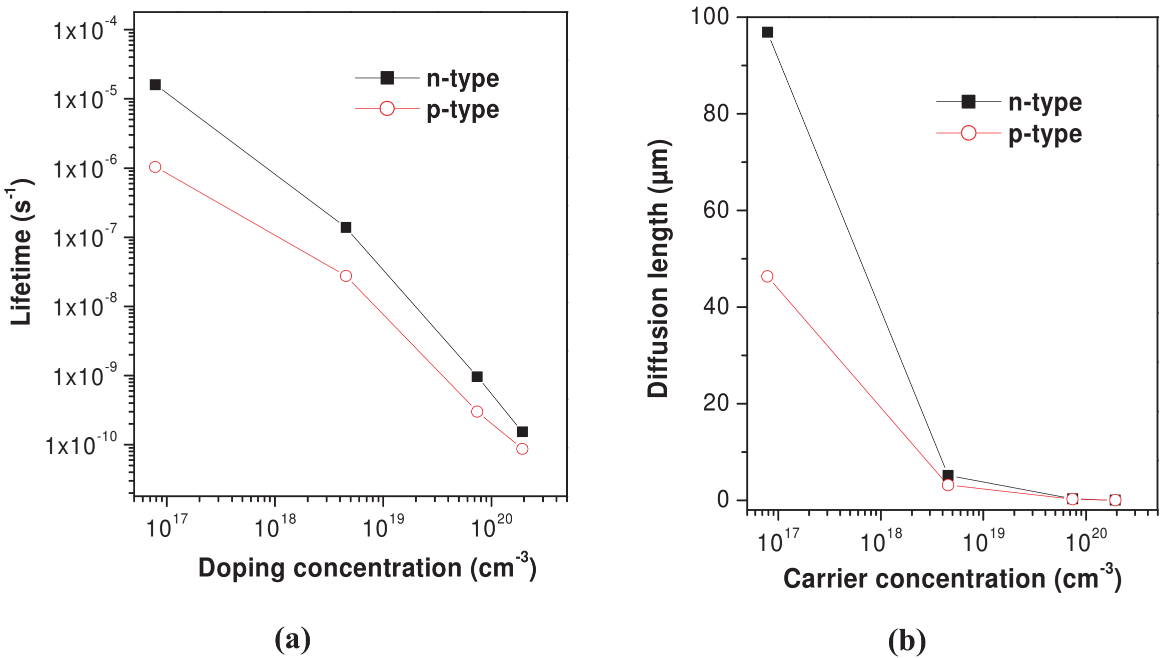


Figure 2.11: Lifetime (a) and diffusion length (b) of minority carriers in n-type and p-type silicon (according to Hull [29]).

Considering literature, S. Martinuzzi et. al. [30] studied the comparison of p- and n-type multicrystalline silicon in terms of minority carriers lifetime (τ) and minority carriers diffusion length (L). The multicrystalline silicon films are characterized by an inhomogeneous distribution of point and extended defects, like dislocations and impurities. Recombination centers generated at grain boundaries and dislocations or come from segregated and dissolved transition metal atoms are the limitation for τ and L. The electrical characterization of these parameters were done by mapping techniques such as electron beam-induced current (EBIC) and light beam-induced current (LBIC). It was found that in n-type wafers the mean value of τ_p and L_p are in the range of 80-120µs and 200-300µm while in p-type material the minority carrier lifetime and diffusion length have smaller values that are 60µs and 120µm, respectively, due to recombination centers. This higher τ_p and L_p can be explained by the low capture cross section σ of metallic impurities for minority carriers in n-type materials. There are no boron-oxygen complexes, the lifetime of minority carriers does not decrease with the injection level [31], the cells work efficiently at low illumination levels and the minority carrier capture cross sections of metallic impurities frequently found in processed silicon are

markedly smaller for holes than for electron. The n-type silicon is electrically less sensitive to metallic impurities because the minority carriers capture cross sections of the recombination centres induced by these impurities are much lower in n-type Si compared to p-type Si. This is particularly valid for impurities such as iron (Fe), titanium (Ti) and vanadium (V). Thus, the MCL, consequently the minority carrier diffusion lengths, are much higher for n-type silicon than for p-type Si for a fixed impurity concentration [32]. Furthermore, a significant reduction of recombination at grain boundaries and surface defects was found in phosphorus-doped samples [33].

Additionally, Cuevas from University of Canberra (Australia) has demonstrated a minority carrier lifetime of ~1ms for an n-type multicrystalline silicon wafer [31], which is equivalent to the values reported for single crystalline p-type silicon wafers!!! The minority carrier lifetime is not degraded even at high temperature processing [34].

A comparative study for p- and n-type poly-Si materials has been done above in terms of minority carrier transport parameters that have an active role on the performance of solar cells. The n-type material has remarkable advantages over p-type material. These results show that phosphorus doped, i.e. n-type, materials can lead to better photovoltaic performances.

2.2 POLYCRYSTALLINE SILICON LAYER FORMATION METHODS

The deposition of crystalline Si films on foreign substrate can be classified into three categories: (i) in the low temperature range, nc-Si films grow with electrically well passivated grain boundaries, and (ii) in the medium temperature range (T > 500°C) grain growth can be columnar and individual grains with a suitable orientation grow from the surface of the substrate to the surface of the film. Grain boundaries are usually electrically active and, due to grain orientation selection, grain size and thus minority carrier diffusion length increases with film thickness. Polycrystalline Si directly deposited on glass in the medium temperature range is therefore in general not suited for solar cell applications. A large-grained Si seeding layer is required if one aims at a poly-Si film with a grain size d larger that its thickness t. Therefore, as we will see later a two-layer sequence consisting of a crystalline seeding layer with pancake-like grains and an epitaxially grown absorber film on the seeding layer is required for a large-grained Si film grown in the high temperature range, polycrystalline silicon.

2.2.1 Direct Deposition Approach

i) Chemical vapor deposition (CVD) at high temperature (≥1000°C)

Chemical vapor deposition (CVD) is a chemical process used to produce high-purity, high-performance solid materials. The process is often used in the semiconductor industry to produce thin films. In a typical CVD process, the wafer (substrate) is exposed to one or more volatile precursors, which react and/or decompose on the substrate surface to produce the desired deposit.

CVD consists of depositing a solid material through a chemical reaction from gaseous reactants. The transfer of silicon from gaseous–phase compounds to solid phase incorporated into a growing polycrystalline silicon layer on a planar substrate is performed by CVD that allows excellent dopant concentration and layer thickness control.

Silane (SiH_4) for LPCVD or chlorine containing gases such as dichlorosilane (SiH_2Cl_2) or trichlorosilane ($SiHCl_3$) can be used a silicon precursors while hydrogen is the carrier gas in all cases. Depending on the precursor, deposition takes place between 800°C and 1200°C.

The aim for direct deposition of polycrystalline silicon layers on foreign substrates (such as th-SiO_2, graphite, ceramics or glass-ceramic) is to obtain large grain size. In the case of CVD, the final grain size is determined by nucleation phase and by competitive grain growth.

The direct deposition generates poly-Si thin films whose grain size is relatively inhomogeneous with the log-normal type distribution. When Si is directly deposited on the foreign substrate, the grain size is going to be determined by the nucleation phenomenon in the early stage of deposition as shown in Figure 2.12. During the nucleation phase, nuclei are formed and start capturing free Si atoms on the substrate surface. While these existing grains grow, new ones may be formed in the spaces between them. After coalescence, however, grains grow further epitaxially, continuing the underlying crystalline structure throughout the layer. As the crystallites have different crystal orientations, they form grain boundaries when they reach each other [35] (See Chapter 4 for the detailed discussion about the nucleation and growth of poly-Si by CVD technique). The number of nuclei determines the grain size by $n_x \approx= d^{-2}$ where n_x is the nucleus density and d is the grain size in the final layer. According to this relation, the lower the nucleus density, the larger the grains will be. The average sizes of grains vary from 0.5 to 10μm in general [20,36] while 30μm diameter can be obtained as a largest size if nucleation density is controlled perfectly by a control of the gas flow [37].

Concerning the preferred orientation, previous reports of direct CVD on foreign substrates mention a strong <110> preferential orientation [38,39].

Photovoltaic results of cells formed by direct deposition using CVD on alumina ceramic and th-SiO_2 is listed in Table 2.2. A polysilicon film on alumina has lower solar cell performance than th-SiO_2. There can be two main reasons for this result. Firstly, the impurities coming from the substrates into the Si film during the high-temperature deposition results in a lower crystal quality and lower cell performance. As a second one, the roughness effect of the surface. Alumina ceramic has a quite rough surface compared to th-SiO_2 which provides more nucleation sites and therefore reduces the crystallographic quality of the films [40].

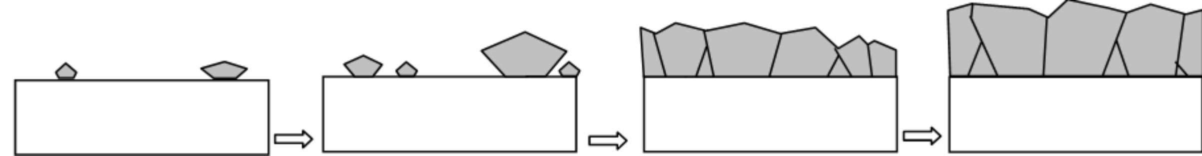


Figure 2.12: Nucleation and growth process steps of Si on foreign substrate [21].

Substrate	*Technology*	*S* (cm^2)	*t* (µm)	V_{oc} (mV)	I_{sc} (mA)	*FF* (%)	*Eff.* (%)	*Ref.*
Al_2O_3	Direct CVD	1	15	302	12.2	58	2.1	[36]
SiO_2	Direct CVD	1	15	448	18.8	66	5.5	[41]

Tablo 2.2: Results of the cells carried out by direct CVD on foreign substrate.

As a summary, the direct deposition of poly-Si on foreign substrate results in a wide grain distribution but containing many small grains. Because of the V growth behavior, large grains (>20µm) can be observed at the surface if the deposition time is long, meaning a very thick polysilicon film. Since the minority carrier diffusion length of such thick polysilicon films is small, it will limit the solar cells efficiency.

ii) Solid Phase Crystallization (SPC)

The solid phase crystallization process or SPC consists generally speaking in depositing an amorphous Si film on glass substrate followed by a thermal anneal for an extended period of time. This crystallization process of the film leads to the formation of silicon grains. The thin film remains in the solid phase during the whole process, which is why this kind of process is called solid-phase crystallization. Among semiconductor crystal growth techniques, SPC received extensive attention starting in the late 1970's. The most

extensively studied method to obtain poly-Si and the most successful at solar cell level is the SPC of amorphous silicon deposited by PECVD, sputtering, or simple evaporation [42,43]. The advantages of using SPC of a-Si are that it is simple and cost-effective, requires a low process temperature, and produces a relatively high-quality silicon layer. The grain enhancement in this process results from a movement of GBs activated by the heating. An increase in the time or temperature, or both, can further promote the grain growth. Typically the amorphous silicon fims are between 1 and 3µm thick, and can either be undoped, moderately doped or highly doped, or consist of multiple layers with different doping levels. After deposition, the films are annealed at temperatures between 550 and 700°C, for a long period of time, typically several tens of hours. The higher the temperature, the faster full crystallization will be reached, but the smaller the grains will be. If the temperature is too low, full crystallization is not reached within a reasonable time. A workable compromise is 600°C [35]. Solar cell grade SPC films have a typical grain size of 1–2µm. For all SPC annealing temperatures, there is generally a log-normal distribution of grain sizes which inevitably results in a large proportion of small grains. The average grain size is a factor of 3–5 times smaller than the maximum grain size. This is especially important for solar cell applications, since the open-circuit voltage decreases significantly if even a small proportion of the grains have a diffusion length which is small compared with the grains in cell [44]. Moreover, the intragrain quality is far from being perfect, featuring many defects such as twins and dislocations. In contrast with other types of polysilicon, SPC material tends to show a <111> preferential orientation [45,46]. This has been attributed to the anisotropic rate of crystallization, which favors grain growth of grains with a <111>.

Crystalline silicon on glass (CSG) technology using SPC technique has reached a significant performance milestone by achieving its first independently confirmed mini-module efficiency of 10.4% that is the highest cell results for polycrystalline silicon thin film solar cells as shown in Table 2.3.

Company	*Substrate*	t (µm)	*Technology*	V_{oc} (mV)	J_{sc} (mA/cm^2)	*FF* (%)	η (%)	*Ref.*
Sanyo Electric	metal	~5	SPC	553	25.0	66.4	9.2	[47]
CSG Solar AG	textured glass	2.2	SPC+ RTA	492	29.5	72.1	10.4	[48]

Tablo 2.3: Illuminated *I-V* parameters of thin film Si solar cells by SPC on foreign substrate.

Although SPC has several advantages, such as simple, cost effective, etc. (as discussed above), the major drawback of the thermal annealing process is that it requires a long time. A typical annealing process will take 20 to 40h [49]. Additionally, the difficulty to reach the structurally excellent material is the other disadvantage of SPC technique to use for the formation of poly-Si thin films.

2.2.2 Seed Layer Approach

In contrast to the direct deposition (nucleation control) approach, the seed layer approach totally decouples initial nucleation from the actual growth of the active layer. It is schematically illustrated in Figure 2.13. First, a thin continuous layer with large grains is formed, the seed layer. This seed layer shows good crystallographic quality, but it is either too thin or too highly doped, or both, to be used as an active layer in a solar cell. In the second phase, an epitaxial deposition process is applied, that is a deposition process that reproduces the underlying crystal structure, to create the absorber layer. Note that two completely different film formation techniques are used for the seed layer and the active layer. The seed layer approach decouples the issues of achieving good crystallographic quality on one hand, and of depositing a layer with the required doping profile and with an adequate growth rate on the other hand.

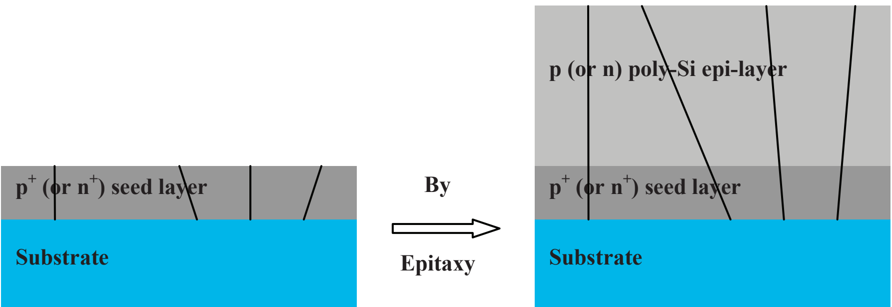


Figure 2.13: Formation of polycrystalline silicon using seed layer approach.

Mainly there are 3 prominent techniques to form polycrystalline seed layer on foreign substrate:

i) Zone Melting Crystallization (ZMC)

In this approach, a microcrystalline silicon layer is first deposited by any technique and it is recrystallized in the second step. Zone-melting recrystallization (ZMR) is one of the possible methods. The principle of this technique is shown in Figure 2.14, where a focused

light from halogen lamps are used as heat sources. Meanwhile the zone melting heater moves across the wafer with a speed of 20mm/min. During the zone melting recrystallization the silicon is locally molten at 1410°C. Furthermore, a very low impurity level (i.e., below ppb) is needed for the active silicon layer to achieve reasonable conversion efficiencies. Common to all ZMR methods is the creation of a narrow molten zone that is scanned across the thin film. Behind the focal line, the melt cools below the melting point and heterogeneous nucleation starts. Stable crystallites develop and act as seeds for further growth. Due to the anisotropic crystal growth speed grains with a particular crystal direction soon prevail. Grains grown by ZMR reach up to several millimeters in width and several centimeters in length [50].

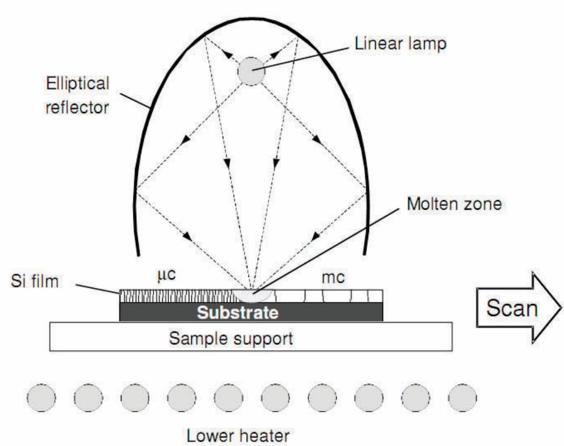


Figure 2.14: Principle of ZMR using linear halogen lamp heaters [50].

The ZMR silicon seed layer is heavily contaminated due to the high-temperature melt process, even though its crystallinity may be excellent. Epitaxy preserves the crystallinity and maintains low impurity levels in the active absorber layer by a lower-temperature process.

The choice of heat source significantly affects the temperature gradient and therefore the film quality. Strip and lamp heater sources produce much lower temperature gradients than laser or electron beam heat source. Due to this reason, lamp or strip heater produce better crystallographic quality than laser or electron beam ZMR. When the recrystallization is performed under the right conditions, the resulting layers show multicrystalline silicon with elongated grains of mm to cm in size and a dominant <100> texture. The experimental investigations showed that the percentage of <100> oriented grains depend on the silicon film thickness and the scan speed [51].

Table 2.4 summarizes the cell results on foreign substrates. Because the thin film is heated to the temperature around the melting point of silicon (~1200°C), this method is not suitable for the crystallization of an a-Si film on a conventional glass substrate with a low

soften point; only ceramic substrates are suitable to withstand temperatures above 1000°C without deforming or significant out-gasing of impurities. Investigated substrates were graphite, SiC, Al_2O_3, low cost silicon, mullite, Si_3N_4-ceramic. Only few substrate materials meet both physical requirements and cost goals for this so-called high-temperature approach. Samples with intermediate ONO-layer on Si_3N_4 showed the largest grains after ZMR: grain sizes of up to three millimetres width and several centimetres length could be obtained. ZMR on samples without intermediate layer did not yield large-grained silicon layers [52].

Substrate	*Technology*	*S* (cm^2)	*t* (µm)	V_{oc} (mV)	I_{sc} (mA)	*FF* (%)	*Eff.* (%)	*Ref.*
Graphite, SiC	ZMR	1	30	570	25.6	75.5	11.0	[53]
Graphite, SiC	ZMR	1.3	30	561	20.1	73.6	8.3	[54]
Si_3N_4 + ONO	ZMR	1	30	539	26.1	67	9.4	[55]
Mullite + ONO	ZMR	1	35	525	23.8	66	8.2	[56]
Al_2O_3 + Si_3N_4	Laser-ZMR	0.01	4.2	480.0	25.5	53	6.5	[57]
Ceramic	Silicon-FilmTM (Astropower)	240	100	581.9	27.4	76.5	12.2	[58]

Tablo 2.4: Illuminated *I-V* parameters of thin film silicon solar cells by ZMR technique on foreign substrate (AM1.5, 100mW/cm^2).

On conductive substrate, except graphite, reflectors covered with Si-SiC, efficiency of 11% and 8.3% were obtained by using this method. On non-conductive substrates (such as mullite, alumina ceramic), the vertical emitter channel penetrating through the whole thickness do not lower the efficiency due to an insulating substrate, they even help to increase the carrier collection, since charge carrier pairs generated in the depth of the material near to a crack have a shorter diffusion path to the pn junction, i.e., their collection probability is increased [52]. ZMR was able to increase the efficiency of thin film Si based solar cells since value up to 11.0%. However, the combination of ZMR and CVD requires several additional steps, e.g. deposition of a silicon oxide capping layer, the ZMR process itself and at least two etching process. Therefore, the implementation of ZMR to a solar cell production is still doubtful, since its additional steps will increase the total cost of the final solar cell.

ii) Laser-Induced Crystallization (LIC)

Laser crystallized silicon is used by the electronics industry to obtain thin film transistors (TFTs) for flat panel displays. There are several different techniques used to laser crystallize materials over large areas. The standard technique for TFT's at present is excimer laser annealing (ELA), in which a thin amorphous Si layer is crystallized by repeated pulses of a wide excimer laser beam. XeCl excimer laser recrystallization (ELR) and annealing (ELA) of a-Si has been studied extensively in recent years. Although most works are concentrated on the use of this method for thin-film transistor (TFT), it is also used for solar cells. The focused short-pulsed laser beam is scanned over the a-Si or μc-Si thin film to heat the sample. Laser crystallization makes use of laser light pulses to melt the silicon locally, inducing crystallization. As only a small volume of silicon is liquid for only a very short time, the substrate itself remains at low temperature. Laser crystallization is therefore compatible with cheap low temperature substrates. High electronic quality can be achieved, with excellent homogeneity over large areas, even on ordinary glass substrates. In laser recrystallization, depending on the power of the incident light, the part of the thin film under illumination can be either in liquid phase (melted totally) or in liquid + solid phase (partly melted), which will result in different grain sizes. It is interesting that the grain size does not increase even though the temperature in the thin film is around the melting point of Si. Because short-pulse laser is used, the temperature of the substrate can be much lower than that of the film; this is a major difference between ZMR and ELR. By placing a thin oxide and/or nitride layer between the substrate and a-Si, both heat transfers from the thin film to the substrate and impurity diffusion from the substrate to the thin film can be dramatically reduced. This technique results in a material with a relatively small grain size (0.1–0.5μm). Newer techniques are being investigated, which generate polysilicon layers with better structural quality and larger grains. The most promising is the sequential lateral solidification (SLS) process [59,60]. In this process, a small area of a few mm in width and more than 100mm in height of the initial a-Si film is sequentially (completely) molten by successive laser pulses. Between two subsequent laser pulses, the substrate (oxidized silicon wafer) was moved over a distance of approximately 1mm. In this way, the grains grow from the interface of the previously processed area into the molten zone. This method demonstrated the crystallization of high quality poly-Si with grain sizes of several tens of mm [61]. The grain width has been found to depend on the a-Si thickness, the laser power and the pulse frequency. The lower the film thickness, the laser power or the pulse frequency, the higher the quenching rate is [62]. A high quenching rate means fast crystallization and small grains. The

SLS process has been successfully used for the formation of polysilicon materials with typical grain size in the range 2–4µm [63] and up to 7mm under some specific conditions [64].

Copper vapor lasers may have an additional advantage against excimer lasers, because the laser wavelength of 511 or 578nm is in the visible, whereas excimer lasers operate in the UV and VUV at wavelengths of 351 down to 157nm. The considerably longer laser wavelength of copper vapor lasers enables the crystallization of several 100nm thick amorphous Si films without heating low cost glass substrates. The absorption length of these wavelengths in amorphous Si is around 100nm, low cost glass is transparent in the visible but strongly absorbs in the UV and VUV. Figure 2.15 shows a sketch of the experimental set-up used by Bergmann et. al. [61].

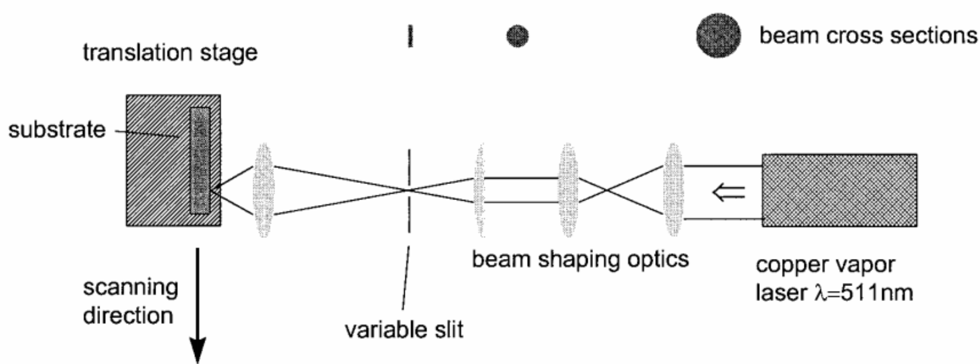


Figure 2.15: Experimental set-up for the sequential lateral solidification (SLS) of Si films [61].

The main advantage of laser processing is the possibility to use cheap glass or flexible substrates. Critical issues for a possible industrial application are throughput (scanning over the whole device area with a narrow beam is usually slow) and maintenance costs. However, with constant progress in laser technology, these issues might be successfully addressed. At present, solar cells fabricated on laser-crystallized Si have achieved conversion efficiencies close to 9% [65]. In principle, if the a-Si is moderately doped, active layers for solar cells can be formed directly by laser crystallization. This was done, for instance, by a team at the Electrotechnical Laboratories in Tsukuba, reporting efficiencies of up to 6.5% on very small area devices on ceramic [66,67]. However, it seems difficult to achieve large devices in this way, due to the lack of dopant profile control. As the whole Si volume goes through the liquid phase, the resulting doping level is uniform over the whole thickness. It is therefore impossible to create a highly doped back region, which is needed for lateral transport of the

majority charge carrier. Therefore, laser crystallization is mainly applied on highly doped layers to create seed layers for subsequent epitaxial deposition [68].

iii) Metal-Induced Crystallization (MIC)

The conventional SPC process enables direct formation of microcrystalline top polycrystalline silicon with small grains and large distribution (0.1-3µm). The SPC method can also be used to prepare the seed silicon layer provided it allows the formation of large silicon grains (>10µm). On the other hand, it has been reported that the SPC temperature of a-Si can be lowered by the addition of some metals such as Al, Ni, Pd [69] that are also catalyzes to reach larger grains. This method is called metal induced crystallization (MIC). In metal/Si systems, stable metal silicide phases exist in thermal equilibrium and play an important role during the crystallization process. Metals lead to a lower thermal annealing temperature below the eutectic temperatures of the Si/metal systems for the crystallization of a-Si by forming a metal silicide, by eutectic-alloy formation, by migration of metal silicide, or by some combination of these [44]. In metal/Si systems, it is not the metal itself that directly mediates the crystallization process. Table 2.5 gives the crystallization temperature of silicon contacting with some selected metals and the eutectic temperature of metal/Si bilayer system. MIC of a-Si can be used to produce poly-Si with grains larger than those achievable either by thermal annealing of a-Si or by direct deposition of poly-Si by CVD. If a-Si is deposited at low temperatures on substrates coated with certain metals, and then heated to a temperature >300°C, the a-Si film can be converted to poly-Si. Alternatively, if the deposition of a-Si can be carried out at such higher temperatures on these metals, one can obtain large-grain poly-Si films directly. Here the metal acts as a catalyst to induce crystallization. MIC involves intermixing of metal with Si and the formation of a high concentration of metal alloy in the amorphous/crystalline interface. Furthermore, it was found that the growth of the crystalline phase would stop when no more metal is available. It must be noticed that using gold and aluminium metals make it possible to crystallize amorphous silicon with very low temperatures (<150°C). Speeds of crystallization from amorphous phase to crystalline phase can be increased up to the factors of about 50 for gold and 66 for aluminium [70]. Additionally, the metal concentrations are very important for the speed of metal induced crystallization. In these cases, the segregation of metal is observed between amorphous silicon and the crystal. Low crystallization temperature of metal/a-Si systems makes it compatible with the use of conventional low cost soda-lime glass substrates.

metal/a-Si	T_{eutec} (°C)	T_{crist} (°C)	*Reference*
Al/a-Si	577	150	[71]
Ag/a-Si	830	200	[72]
Au/a-Si	360	130	[73]
Sb/a-Si	630	430	[74]
Cu/a-Si	802	485	[75]
Ni/a-Si	964	485	[69]
a-Si (SPC)	-	570-600	[76]

Tablo 2.5: Eutectic and crystallization temperatures of metal/Si systems and a- Si.

In the case of Ni, the Ni atoms on a-Si, after thermal annealing at ~500°C for 20h, form octahedral $NiSi_2$ precipitates in the a-Si matrix [44,77]. The $NiSi_2$ precipitates are formed at the stage of thermal annealing and act as sites for crystallization. Needle-like Si crystallites are grown by silicide-mediated crystallization (SMC) of a-Si and the migration of $NiSi_2$ precipitates through the a-Si network as showed in Figure 2.16. More recently, nickel-nucleated lateral solid-phase epitaxy was achieved by nickel particles applied by means of a nickel colloidal "ink" [78]. The amorphous silicon layer is fully crystallized before the onset of random nucleation, with each nickel particle seeding one grain, achieving grain sizes >100μm. Ni induced polycrystalline Si has a preferred <110> texture. These grains, however, contain many low angle subgrain boundaries and are heavily metal contaminated.

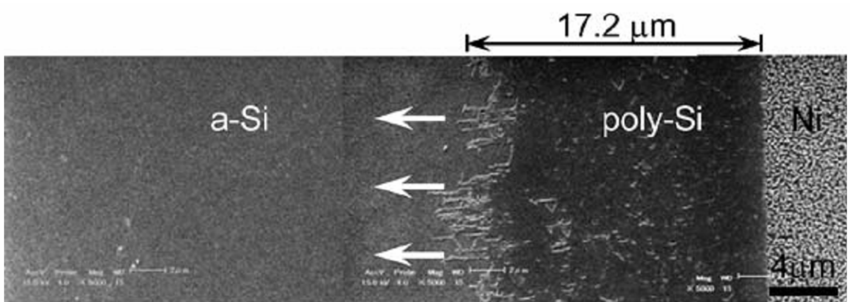


Figure 2.16: SEM micrographs of Ni-induced crystallization [79].

In spites of the low-temperature crystallization of a-Si, this method suffers from drawbacks such as metal contamination of the crystallized Si matrix and long time for crystallization. To avoid contamination, aluminium is preferred, as it acts as an acceptor dopant in Si and diffuses relatively slowly in Si. The Aluminium Induced Crystallization or AIC technique leads to a thin crystalline layer with a high Al concentration. Such a p^+ layer is not a problem in a photovoltaic device. It is in fact a feature that is present in most Si solar

cell designs. AIC method has been investigated to crystallize amorphous silicon layers on foreign substrate such as glass [80] and ceramic [81]. Aluminium induced crystallization (also called Al induced layer exchange or ALILE) is based on the overall layer exchange of adjacent Si and Al films and transformation of amorphous to polycrystalline Si during thermal annealing [35,82]. The Si and Al layers, each a few hundreds of nm thick, are generally deposited by evaporation, magnetron sputtering or PECVD. The initial a-Si needs to be slightly thicker than the initial Al layer in order to form a continuous layer. Importantly, a thin (a few nm) AlO_x membrane should be formed between the initial Al and a-Si layers prior to Si deposition. This AlO_x inter layer plays a crucial role throughout layer exchange process by remaining in position, separating top and bottom layer and behaving as a membrane that controls the diffusion [83]. The resulting polycrystalline silicon layers are quite smooth and continuous. Additionally, large grained (≥10μm) and <100> preferential orientated polycrystalline films are formed by AIC method

The poly-Si seed layers being too thin (~200nm) and highly doped ($C\sim2\times10^{18}cm^{-3}$ for p-type film or $C\sim2\times10^{21}cm^{-3}$ for n-type film when P509 doped), an epitaxial thickening step is necessary to form the absorber layer based solar cell with a thickness of 2-5μm.

The chapter 3 will develop more deeply the AIC process, while the used thickening method namely the solid phase epitaxy (SPE) and the vapor phase epitaxy (VPE) will be detailed in Chapter 4.

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CHAPTER 3: ALUMINIUM INDUCED CRYSTALLIZATION

3.1 PRINCIPLE OF ALUMINIUM INDUCED CRYSTALLIZATION

The general idea and the advantages of aluminium induced crystallization (AIC) method as discussed in Chapter 2 are simple processing, low annealing temperature below eutectic temperature of Al/Si system (T_{eu}=577°C) and short crystallization time compared to solid phase crystallization (SPC). In this part the detailed theory of AIC technique is studied.

An AIC process is based on the fact that amorphous silicon, when in contact with certain metals, transforms into crystalline Si at temperatures much lower than the commonly reported temperature for solid phase crystallization of a-Si. Although, the actual mechanisms of the interdiffusion and the associated (re)crystallization in the aluminium/amorphous-silicon (Al/a-Si) system and the driving force for layer exchange are not well understood, some studies have been done to explain this crystallization process. There are still some parameters that must be understood clearly.

3.1.1 Solid Solubility of Al/Si System

If the Al/Si system is under thermal annealing, the thermal equilibrium between pure Al and a-Si breaks resulting a solid Al solution with Si solute. Al/Si system is a simple binary eutectic with limited solubility of aluminium in silicon and limited solubility of silicon in aluminium. Figure 3.1 depicts the binary Al/Si equilibrium phase diagram that shows the relationships among various phases that appear within the Al/Si system under equilibrium conditions. There is an equilibrium eutectic reaction at approximately 12.2at.% silicon at the eutectic temperature (577°C). At this particular temperature the solubilites of silicon in aluminium and aluminium in silicon are 1.65at.% and 0.5at.%, respectively. On the other hand, the solubility of silicon decreases to 0.05at.%, 0.2at.% and 0.8at.% at 300°C, 400°C and 500°C, respectively, as shown in Figure 3.1 [1]. When the temperature approaches that of the eutectic temperature (577°C), rapid solid-state diffusion occurs, and the silicon segregating from the diffusion interface migrates through the aluminium. There is only one invariant reaction in the Al/Si phase diagram, namely

$$L \rightarrow \alpha + \beta \text{ (Eutectic)} \quad (3.1)$$

In Equation 3.1, L is the liquid phase, α is predominantly aluminium, and β is predominantly silicon. Generally phase diagrams represent the relationship between temperature and composition under atmospheric pressure. Figure 3.1 shows that the Al/Si eutectic can form as follows:

i) Directly from the liquid in the case of a silicon concentration of 12.2% (i.e., for a eutectic aluminium-silicon alloy),

ii) In the presence of primary aluminium in the case of silicon contents <12.2% (i.e., for hypoeutectic aluminium-silicon alloys), and

iii) In the presence of primary silicon crystals in the case of silicon contents >12.2% (for hypereutectic aluminium-silicon alloys).

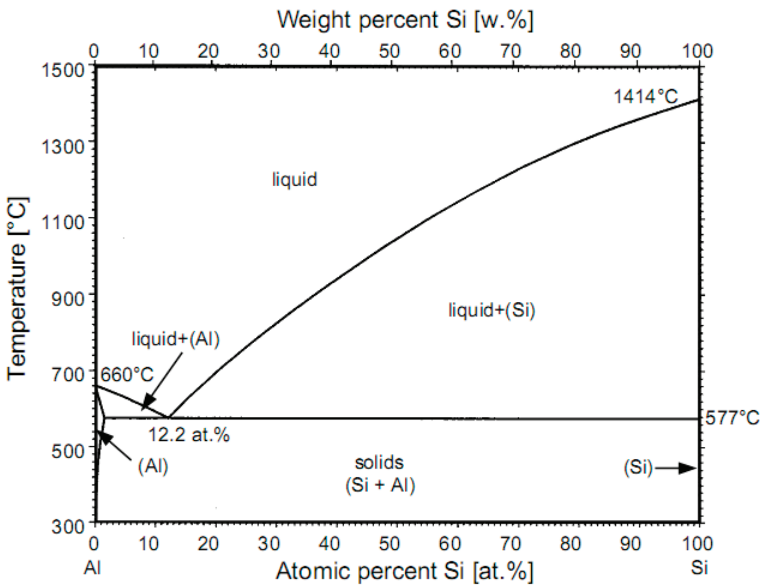


Figure 3.1: Al-Si equilibrium phase diagram [2].

3.1.2 *Diffusion of Silicon in Aluminium*

At annealing temperatures below the eutectic, the solid Al dissolves the silicon and permits it to diffuse more rapidly than in wrought (shaped) Al as shown in Figure 3.2. The diffusion coefficient (D) of Si in solid aluminium becomes enhanced as much as 1.5 orders of magnitude for evaporated aluminium. Specimens annealed at the same temperature but for different times show that the enhancement in D decreases for longer annealing duration. This can be due to imperfections in the Al film. The amount of grain boundary in the film must be decrease, however, other imperfections such as dislocations that remain at high concentration and cause to the lower diffusivity at higher temperatures. The activation energy (E_A) is also

quite different for evaporated- and wrought-Al systems. The activation energy is 0.79eV and 1.36eV for evaporated Al and conventional Al, respectively. This difference can be explained by the accelerated diffusion at the diffusion levels in aluminium (such as boundaries and dislocations). The diffusion coefficient of about 5×10^{-7}-2×10^{-8}cm^{2}s^{-1} in the temperature range of 400-500°C for solid Al is lower than that of liquid phase Al (>10^{-4}cm^{2}s^{-1}) [3].

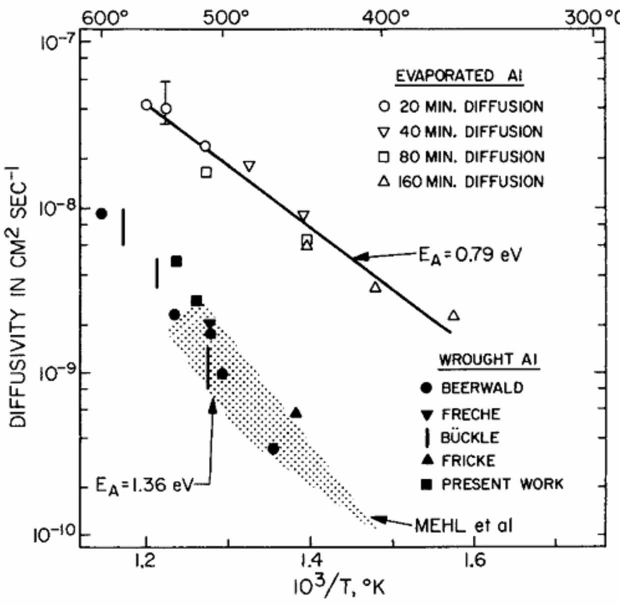


Figure 3.2: The diffusivity of silicon in solid aluminium [4].

3.1.3 Thermodynamics and Kinetics of Al/Si Bilayers

Gibbs's classification serves as the fundamental basis for division of phase transformation processes. For this reason, to understand the thermodynamic and kinetics of crystallization of a-Si in contact with Al, Gibbs energy changes caused by this layer exchange process in Al/Si bilayers must be considered. Although, at the beginning of the process sublayers contain either pure Al or pure Si, the sublayer sequence is completely reversed upon annealing. Gibbs energy changes (ΔG) of the bilayer system, i.e. the Gibbs energy after layer exchange minus the Gibbs energy before layer exchange, are calculated per unit area parallel to the surface. The Gibbs free energy diagram for amorphous-crystal system is shown in Figure 3.3.

The driving force of dissolution of silicon in contact with aluminium at constant temperature is the difference of Gibbs energy ($\Delta G_{a\rightarrow c}$) between the metastable amorphous silicon phase (G_a) and the stable crystalline silicon phase (G_c):

$$\Delta G_{a \to c} = G_a - G_c \tag{3.2}$$

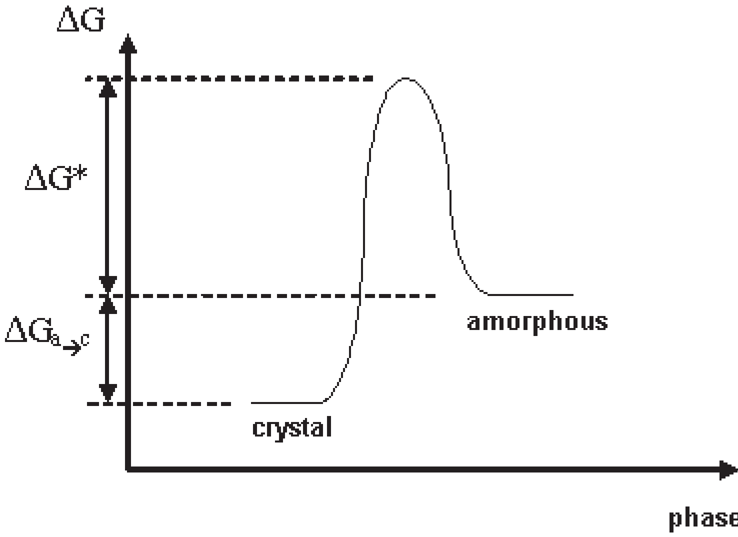


Figure 3.3: Variation of Gibbs free energy depending on the silicon phase.

The Gibbs free energy of a system at any moment of time is defined as the enthalpy of the system minus the product of the temperature times the entropy of the system:

$$G = H - TS \tag{3.3}$$

where H is the enthalpy, S the entropy, and T the absolute temperature. The Gibbs free energy of the system is a state function because it is defined in terms of thermodynamic properties that are state functions. The change in the Gibbs free energy of the system that occurs during a reaction is therefore equal to the change in the enthalpy of the system minus the change in the product of the temperature times the entropy of the system.

$$\Delta G = \Delta H - \Delta(TS) \tag{3.4}$$

If the reaction is run at constant temperature, this equation can be written as follows:

$$\Delta G = \Delta H - T\Delta S \tag{3.5}$$

where ΔH and ΔS are the corresponding enthalpy and entropy changes. A consequence of the Second law of thermodynamics is that spontaneous reactions occur at constant temperature and pressure when ΔG is negative, i.e., $\Delta G<0$. This condition implies that a system will naturally tend to minimize its free energy by successively proceeding from a value, G_i to a still lower, more negative value, G_f until it is no longer possible to further reduce G. When this happens, $\Delta G=0$, the system has achieved equilibrium and there is no longer a driving

force for change. On the other hand, for a process that cannot occur, $\Delta G>0$. It is important to note that neither the sign of ΔH nor that of ΔS taken individually is sufficient to determine reaction direction; rather, it is the sign of the combined function ΔG that is crucial in this regard. The concept of minimization of free energy, as a criterion for both stability in a system and forward change in a reaction or process, is a central theme in materials science. The balance between the contributions from the enthalpy and entropy terms to the free energy of a reaction depends on the temperature at which the reaction is run.

The other main question is: How does silicon (a-Si) dissolve, diffuse (in Al) and grow into crystalline phase by annealing the system? To answer this question this transformation must be analyzed deeply.

The detailed interaction mechanism of amorphous silicon/polycrystalline Al bilayers was studied by Y.H. Zhao et. al. [5], D. He et.al. [6] and J.Y. Wang et. al. [7]. The peculiar exchange observation of the locations of Al (bottom to top) and Si (top to bottom) sublayers may have a kinetic origin, a thermodynamic origin, or both. Generally, the unexpected transformations can occur through the kinetic origin. Therewithal, the formation of amorphous reaction layers at interfaces and the formation of amorphous oxide layers on metal surfaces can have a thermodynamic origin different from kinetic origin thought [8,9]. However, tiny energy difference can have a great effect on the microstructural evolution. Therefore, the energy changes occurring in the Al/Si bilayer upon transformation must be clarified.

The schematic representation of the transformation of Al (50nm)/a-Si (150nm) bilayer annealed at 250°C is given in Figure 3.4. At the beginning of the annealing at 250°C, the amorphous Si layer and the Al layer are subjected to a compressive macrostress and microstrain. This stress in sublayer is composed of the stress after layer deposition at room temperature and the thermal stress due to heating up to annealing temperature. The thermal stress is caused by the difference in thermal expansion of the substrate and Al layer. At the end of the annealing, the Al and Si layers exchange their locations, and a-Si crystallizes into polycrystalline silicon. The grain size of Al increases laterally and the macrostress and microstrain of Al layer is relaxed. According to results, the stress in Al layer has relaxed entirely during the annealing. Upon annealing, the Gibbs energy of thin film system can be reduced. This is the driving force for layer exchange. The driving force determines not only the overall direction of the kinetic process, i.e. change from a non-equilibrium state to an equilibrium state, but also the process rate.

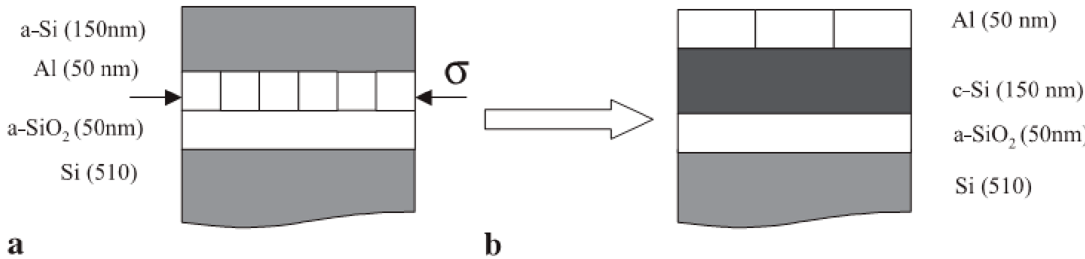


Figure 3.4: Schematic representation of the layer exchange for Al (50nm)/a-Si (150nm) bilayer annealed at 250°C [5].

For the aluminium induced layer exchange (ALILE) process, the total Gibbs energy change of the bilayer per unit area parallel to the surface, ΔG, can be explained as:

$$\Delta G = D_{Si}\Delta G_{\langle Si\rangle-\{Si\}} + D_{Al}\Delta G_{Al} + \left(\gamma_{\langle Al\rangle} - \gamma_{\{Si\}}\right) + \left(\gamma_{\langle Al\rangle-\langle Si\rangle} - \gamma_{\langle Al\rangle-\{Si\}}\right) + \left(\gamma_{\langle Si\rangle-\{SiO_2\}} - \gamma_{\langle Al\rangle-\{SiO_2\}}\right) \quad (3.6)$$

Here $\langle\ \rangle$ and $\{\ \}$ symbolize crystalline and amorphous phases, respectively. To understand the Equation 3.6, each term could be explained step by step. The five contributions to the Gibbs energy change are as following:

1. $\Delta G_1 = D_{Si}\Delta G_{\langle Si\rangle-\{Si\}}$: This term is the Gibbs energy difference per unit area parallel to the surface between c-Si and a-Si. The D_{Si} and $\Delta G_{\langle Si\rangle-\{Si\}}$ are the a-Si layer thickness and the Gibbs energy difference between c-Si and a-Si per unit volume, respectively.

2. $\Delta G_2 = D_{Al}\Delta G_{Al}$: The second term is energy change per unit area parallel to the surface between the annealed Al layer and the as-prepared Al layer. The D_{Al} and ΔG_{Al} are the Al layer thickness and the Gibbs energy difference between the annealed and unannealed Al layers per unit volume. Here the energy difference is also due to change of grain size and the energy released by relaxation of residual macrostress and microstrain. At the Al/Si bilayers, the grain size increases laterally upon annealing and remain almost constant in the columnar direction.

3. $\Delta G_3 = \gamma_{\langle Al\rangle} - \gamma_{\{Si\}}$: This describes the surface energy difference between c-Al ($\gamma_{\langle Al\rangle}$) and a-Si ($\gamma_{\{Si\}}$).

4. $\Delta G_4 = \gamma_{\langle Al\rangle-\langle Si\rangle} - \gamma_{\langle Al\rangle-\{Si\}}$: This is the sublayer interface energy difference between c-Al/c-Si ($\gamma_{\langle Al\rangle-\langle Si\rangle}$) and c-Al/a-Si ($\gamma_{\langle Al\rangle-\{Si\}}$).

5. $\Delta G_5 = \gamma_{\langle Si\rangle-\{SiO_2\}} - \gamma_{\langle Al\rangle-\{SiO_2\}}$: The last and the fifth term is the bilayer-substrate interface energy difference between c-Si/a-SiO_2 ($\gamma_{\langle Si\rangle-\{SiO_2\}}$) and c-Al/a-$SiO_2$ ($\gamma_{\langle Al\rangle-\{SiO_2\}}$). In this interfacial energy difference, a-SiO_2 can be approached as a liquid and the change in the energy for solid (crystalline)/liquid (amorphous) interfaces upon layer exchange can be ignored since it is about one order of magnitude smaller than that of the solid/solid interface.

It is clearly found that, ΔG_1 and ΔG_2 are negative, driving the transformation of the Al/a-Si bilayer system upon annealing, whereas ΔG_3 and ΔG_4 are positive and thereby counteract the transformation of the Al/Si bilayer. However, the Si crystallization process takes place locally and does not involve mass transport, by means of that release of crystallization energy of a-Si (ΔG_1) has no contribution to the driving force for the layer exchange. Therefore, the net driving force for the layer exchange can be defined as $-(\Delta G_2 + \Delta G_3 + \Delta G_4)$.

A tiny net driving force, due to the decrease of microstrain, relaxion of macrostress, and Al grain growth in the Al phase, controls the kinetics of the ALILE process. Driving force can be explained individually by the thermodynamic basis for each process steps. The first step is inward diffusion of Si along grain boundaries of Al layer. When a-Si layer is in contact with the Al layer, the free electrons of Al layer near the interface have a Coulomb screening effect on the adjacent Si atoms, which leads to a weakening of the covalent bonds of the adjacent Si atoms [7,10]. Upon annealing, free Si atoms may diffuse into the Al layer along the grain boundaries of Al phase because of energy decrease which is the energy difference between two times the $\langle Al\rangle/\{Si\}$ interface energy and the Al grain boundary energy. Additionally, experimental analysis of interdiffusion in Al/Si system shows that the activation energy of this process is indicative of diffusion of Si along grain boundaries in Al.

The second step is the nucleation and crystallization of Si at grain boundaries in the Al layer. The possibility of crystallization of a-Si in contact with Al at relatively lower temperature is ascribed to the presence of free Si atoms in contact with Al. Indeed, because of the weakened chemical bonding of the free Si atoms, the nucleation barrier of Si crystallization for these Si atoms is expected to be significantly lower than that for the "bulk" Si atoms. Crystallization of the free Si actually occurs if a thermodynamic driving force exists. Silicon layer keeps its amorphous state until attaining a critical thickness. Beyond this critical thickness, nucleation of Si crystallization can start. The critical thickness for nucleation for Si crystallization at the Al grain boundary is ~4ML (0.88nm) of Si atoms.

The third and final step in the process is the lateral growth of Si grains in the Al layer. Once crystallization of the Si layer at an Al grain boundary has occurred, the original Al grain boundary has been replaced by two $\langle Al\rangle/\langle Si\rangle$ interfaces. Upon further annealing, the weakly bonded Si atoms at the original c-Al/a-Si interface may also diffuse into the newly developed $\langle Al\rangle/\langle Si\rangle$ interfaces because also this leads to a decrease of energy. Hence, a positive driving force exists for the diffusion of Si atoms into the $\langle Al\rangle/\langle Si\rangle$ interfaces. Upon the diffusion of Si atoms into the $\langle Al\rangle/\langle Si\rangle$ interface, the original Al grain and the new c-Si grain are separated by those Si atoms (an amorphous Si layer). Then, two cases are possible: (i) they may join the already existing c-Si grain or (ii) form a new c-Si nucleus at the $\langle Al\rangle/\langle Si\rangle$ interface after reaching a critical thickness upon further annealing. In case (i) the existing c-Si grain grows laterally and in case (ii) a new c-Si nucleus establishes two new interfaces (i.e., $\langle Al\rangle/\langle Si\rangle$ and $\langle Si\rangle/\langle Si\rangle$ replacing the earlier formed $\langle Al\rangle/\langle Si\rangle$ interface). However, the Si atoms diffusing into the $\langle Al\rangle/\langle Si\rangle$ interfaces would prefer to join the already existing c-Si grain instead of forming a new c-Si grain at the $\langle Al\rangle/\langle Si\rangle$ interface. Therefore, upon continued diffusion of Si atoms from the original a-Si layer into the $\langle Al\rangle/\langle Si\rangle$ interfaces, the c-Si grains formed originally at the Al grain boundaries grow laterally. The microstructure of as-deposited Al layer and annealing temperature determine the grain size of c-Si. The degree of mass transport, in other words the exchange process from Al to Si layer, depends on the diffusion length of Si along Al grain boundaries ($\sqrt{D_{gb}(T)t}$), the sublayer thickness, the original grain boundary density and configuration in the original Al sublayer.

To cross the ΔG energy barrier the system must be heated. Furthermore, the nucleation of Si grains occurs when the Si concentration in the Al layer exceeds the solid solubility limit for crystalline silicon, C_{sa}, and is related to the change of the Gibbs energy of the Al/Si system. During the nucleation, Gibbs energy increases due to the formation of interfaces between the Al and c-Si and decrease due to the Si bulk formation [11]. The critical radius of crystal silicon cluster, R_c, is referred to as the radius at which the Gibbs energy of the cluster has its maximum value. The value of the critical radius depends on the supersaturation ($S = C_{Si} / C_{sa}$ where C_{Si} is the Si concentration and C_{sa} is the saturation concentration) and the annealing temperature (T_A). According to this model, the critical radius of cylindrical grain is:

$$R_c = \frac{\sigma\Omega}{kT_A \ln S},\ S \rangle 1 \tag{3.7}$$

This explanation can be correlated to change of the Gibbs energy as:

$$\Delta G_c = \frac{\pi\sigma^2 d_{Al}\Omega}{kT_A \ln S} \tag{3.8}$$

where σ is the Gibbs energy per unit area of the interface between the Si grain and Al, Ω=2x10^{-29}m^3 is the atomic volume of Si, and k=8.6×10^{-5}eV/K is the Boltzmann constant.

Assuming diffusion-limited growth, the growth rate is in first-order approximation proportional to the difference of silicon concentration far away from grain-to-silicon concentration just in front of the grain. The growth rate is given by $J_G \alpha C_{Si} - C_{sa} = C_{sa}(S-1)$, therefore, proportional to the supersaturation. Grains grow when the silicon concentration exceeds the saturation concentration [12].

3.2 STATE OF THE ART OF AIC PROCESS

In order to obtain a continuous poly-Si layer on large area substrate without metal contamination, aluminium induced crystallization method was developed. AIC technique was firstly used for layer exchange process by McCaldin et. al. [13,14] in 1976. They used n-type wafer with open window Si oxide layer made by photolithography. A 1µm Al was evaporated on top of the oxide, then the system was annealed at 500-550°C for 10min or 20min. After the structure was cooled down in vacuum, a 900-5000Å thick Si was evaporated on the wafer. The wafer was then heated at 475-525°C for 10min or 20min. Finally, it was found that evaporated a-Si reacts with underlying Al as resulting the refilling of the window with crystalline Si.

The aluminium induced crystallization was also studied with the aim of forming a device. Majni and Ottaviani [15] studied the uniform epitaxial growth obtained on different oriented Si substrates by dissolution and transport of an evaporated Si film over an evaporated Al film at temperatures below 500°C. Laboratory of PHASE/CNRS was involved in this research as well [16]. It was found that the kinetics of process were strongly depending on the level of oxidation at Si substrate/Al interface and Al/a-Si interface or on the orientation of the single crystalline Si substrate. According to Majni et. al. [16], the activation energy of growth, of about 1.2eV, is the same for all orientations. However, growth on <100> oriented substrate is much faster than that of other orientations, for a given temperature.

The first photovoltaic application utilizing aluminium induced crystallization of a-Si to produce p-n junction on n-type Si substrate was investigated by Tsaur et. al. [17]. A very promising conversion efficiency of 10.4% at AM1 was obtained for <100> single crystal silicon while that is 8.5% on polycrystalline silicon. These results are without using a passivation layer, an antireflection coating or a back surface field. In 1998, Koschier et. al. [18] used the aluminium induced layer exchange process for the formation of p-n junction or back surface field (BSF) in silicon solar cells. A 0.6µm thick layer of aluminium was evaporated on both p- and n-type crystalline silicon substrates. Following the a-Si deposition on Al, the samples were heated at 500°C for more than twelve hours. It resulted in an epitaxially grown silicon film with high crystal quality, low resistance and a p-type doping level of $2\times10^{18}cm^{-3}$. These results show the suitability of these films to form a pn junction or BSF.

Initially, O. Nast et. al. [19] showed that the aluminium induced crystallization on sc-Si substrates can be adapted to form a continuous polycrystalline silicon (poly-Si) thin film on glass substrate with grain size of about 5-10µm. When amorphous silicon is deposited on initial aluminium layer and the system is annealed below eutectic temperature of Al/Si system, aluminium induced layer exchange (ALILE) process results the continuous poly-Si layer. The steps of ALILE process developed by O. Nast are shown in Figure 3.5. This process can be described in 4 steps as:

Step 1: Interaction of amorphous silicon with Al and the dissociation of the amorphous phase through the Al/Si interface.

Step 2: Si atoms dissolve and diffuse within the aluminium sublayer.

Step 3: The c-Si nucleation takes place when a certain concentration of Si in the Al grains of the Al sublayer exceeded. A Si nucleus is formed within the Al layer at the Al/a-Si interface after short-time (~5min) thermal annealing.

Step 4: The Si nuclei become grains and grain growth occurs in lateral directions due to the confinement by the interfacial oxide layer and the substrate until the Al sublayer is eventually replaced by the growing Si grains. Si nuclei grow into the Al layer up to touch the adjacent Si grain.

The Focused Ion Beam (FIB) images of ALILE process are exhibited in Figure 3.6. As shown in (d), a residual Al+Si layer is formed after exchange process. The Al part of this residual layer is due to the Al segregation to the top of the sample during the poly-Si growth. Otherwise, all the Si material is not incorporated into the poly-Si layer. Hence, Si material forms small Si crystals within the newly evolved Al layer. To carry out the epitaxial

thickening of the AIC poly-Si seed layer, this residual Al+Si layer must be etched by the selective chemical etchants.

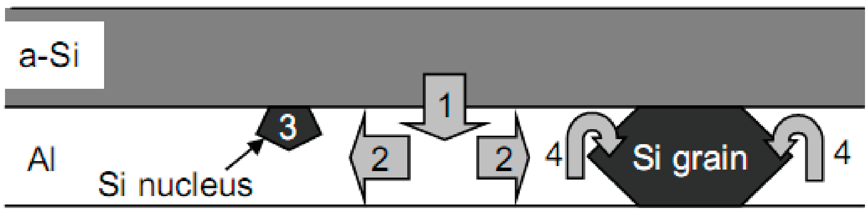


Figure 3.5: Aluminium induced layer exchange (ALILE) model suggested by O. Nast [20].

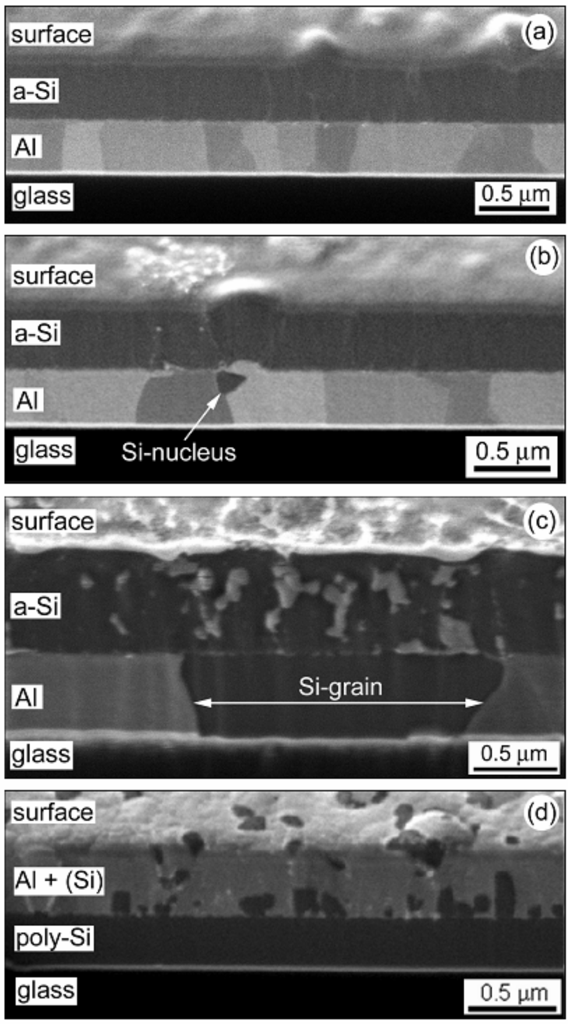


Figure 3.6: Cross-section FIB image of AIC process. (a) before annealing with structure of glass/Al/a-Si, (b) after annealing at 500°C for 5min, (c) annealing at 500°C 10min annealing; (d) 60min annealing at 500°C as a result of glass/poly-Si/Al+Si [20].

3.3 ANALYSIS OF POLY-SI FILMS FORMED ON ALUMINA AND GLASS-CERAMIC

The aim of the aluminium induced crystallization method is to obtain high quality and continuous polycrystalline silicon in a short time with easy processing. However, many physical parameters on the reaction of aluminium and a-Si have important influence for the formation of a continuous poly-Si film. The identified important parameters are schematically summarized in Figure 3.7.

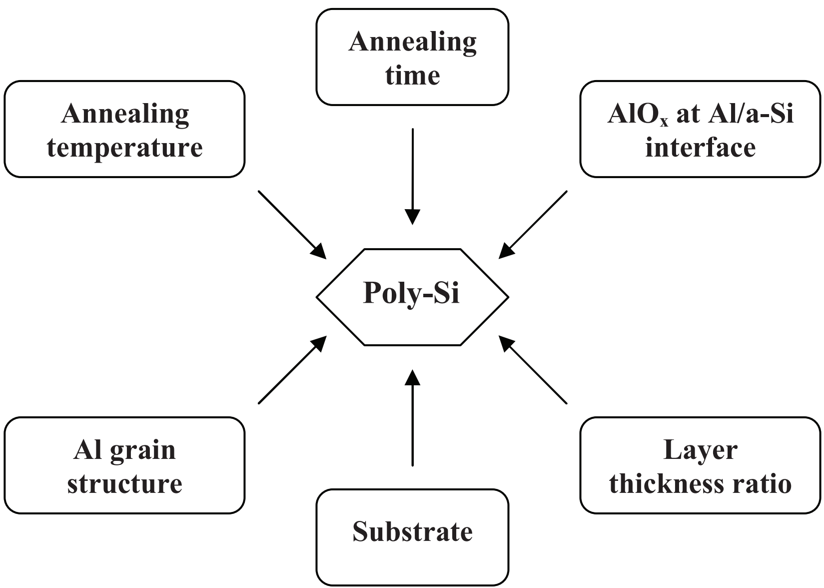


Figure 3.7: Illustration of the parameters that influence on the aluminium induced crystallization process.

In the following paragraphs, we describe and clarify the effects of each parameter on the aluminium induced crystallization process for the formation of poly-Si seed film. Especially Al structure, Al/Si interface, substrate and the exchange annealing conditions are investigated in terms of crystallographic quality of the polycrystalline silicon film.

3.3.1 Experimental Process for Formation of AIC Layers

Transparent glass-ceramic (Corning Inc.) and ceramic alumina (CoorsTek ADS996R) were used as substrates for AIC process. Before starting the processing, the substrates must be cleaned by chemical solutions. The cleaning procedure of alumina consists of following steps: boiling nitric acid (HNO_3-69%) at ~80°C, deionised water (DI-H_2O) with ultrasounds, hydrofluoric acid (2%, HF-50%,), DI-H_2O with ultrasounds (2 times), isopropanol with ultrasounds. Then the ceramics are baked at 200°C during one night and stored in a dry

atmosphere. The cleaning procedure for glass-ceramic differs from that for alumina: we used ethanol with ultrasounds, isopraponal, and HF (2%). The glass-ceramics were then stored in the clean room to avoid contamination.

Prior to the seed layer formation, the FOx-25 was spun on alumina, while a SiN_x layer was deposited on glass-ceramic by PECVD system. An aluminium layer was evaporated by electron beam evaporation system. For both kinds of substrates (alumina/FOx and glass-ceramic/SiN_x) evaporator TEMESCAL allows a good homogeneity of the layers thanks to a rotating holder. Moreover, the deposition is performed at room temperature because of the thermal inertia of the mechanical stands and the long distance between target and substrate (~50cm).

Table 3.1 summarizes the experimental conditions of aluminium deposition. The standard thickness (200±10nm) used here corresponds to the "optimized" conditions on FOx-coated alumina and SiN_x-coated glass-ceramic. This optimization is considered with respect to a decrease in the aluminium thickness, i.e. to increase the speed of exchange process, and to acquire high quality nucleation.

Parameter	*Value*
Purity source Al	5N
Vacuum (before deposition)	6-7 10^{-6} mbar
Vacuum (Beginning of deposition)	1-2×10^{-5} mbar
Fine deposit (1μm)	6-7×10^{-6} mbar
Speed of evaporation	16-18Å/s
Grain size Al	100-400nm
Orientation Al	Mainly <111> (XRD)
Thickness	Standard: 200±10nm

Tablo 3.1: Conditions of aluminium deposition in the evaporator TEMESCAL.

An important experimental parameter for AIC is the interfacial aluminium oxide (AlO_x) layer. It was formed by exposing the aluminium layer to ambient air for 1 week in clean room to set similar temperature and humidity for all prepared samples. The thickness of AlO_x layer after 1 week oxidation is 4.5nm deduced by spectroscopic ellipsometry measurement (UVISEL, HORIBA Scientific).

The formation of the AlO_x layer was followed by the amorphous silicon (a-Si) deposition. The a-Si was deposited using an electron cyclotron resonance plasma enhanced

chemical vapor deposition system (ECR-PECVD, Roth & Rau; see Appendix A). Deposition of a-Si was performed at an RF bias of 50V and a substrate temperature of 250°C for duration of 16min to 22min30sec. The microwave power was fixed at 500W and the silane/argon flows (in sccm) ratio was kept constant at 10/15. The optimized standard thickness is 370±10nm for FOx-coated alumina and SiN_x-coated glass-ceramic substrates. All these experimental conditions are summarized in Table 3.2.

Parameter	*Value*
Microwave power (W)	500
Growth temperature (°C)	250
Pressure (mbar)	8.5×10^{-3}
SiH_4 flow rate (sccm)	10
Ar flow rate (sccm)	15
Deposition rate (nm/min)	22.2

Tablo 3.2: Operational parameters for a-Si deposition in the ECR-PECVD reactor.

To crystallize the a-Si by the layers exchange process, the substrate/Al/a-Si structure was thermally annealed in a tube furnace (CARBOLITE) under nitrogen flow. Due to the eutectic temperature limit for Al/Si structure, the tube furnace was used at temperatures between 450°C and 500°C for the aluminium induced exchange process. Finally, the "substrate/poly-Si/(Al+Si)" structure was obtained after thermal annealing.

In order to characterize the resulting crystalline silicon layer, the residual Al+Si layer formed on top of the structure must be removed. This residual layer can be removed by two different ways depending on the subsequent processes: a mechanical polishing with colloidal silica to prepare the samples for EBSD measurements or a wet chemical etching for the preparation of seed layers for epitaxial thickening. For the first, a colloidal silica (ESCIL, POM 9) with grain size of 150nm and pH of 9 is used as chemo-mechanical polish, i.e., it combines the effect of mechanical polishing with etching. For the chemical treatment two steps are used. First, the aluminium excess is etched by the following selective composition: 16cc phosphoric acid (H_3PO_4-85%), 2cc DI-H_2O, 1cc nitric acid (HNO_3-69%), 1cc acetic acid (CH_3COOH-100%) at 40°C. The etching rate of selective composition for aluminium is 600nm/min at 40°C. Then the Si islands are etched by the second chemical etchant that is nonselective: it is composed of 72.5cc nitric acid (HNO_3-69%), 1.5cc hydrofluoric acid (HF-50%) and 28cc DI-H_2O. The etching rates for Si and Al are 0.8µm/min and 1.1µm/min, respectively, at room temperature.

The resulting AIC poly-Si layers formed at the temperature range of 450-500°C were characterized using microscopical (optical microscopy, electron backscatter diffraction (EBSD), interference microscopy), spectroscopical (micro-Raman spectroscopy, UV/VIS/NIR spectroscopy) and electrical (four point probe measurement system, Hall Effect system) techniques.

3.3.2 Effect of the Interfacial Oxide Layer (AlO_x)

In the broadest sense of the term, diffusion barriers of thin films are used to separate materials from direct contact in order to prevent them from reacting. Diffusion barriers are used in thin-film crystallization systems, an example being silicides to prevent direct Al-Si contact. Ideally, a barrier layer X sandwiched between Al and a-Si layers: i) should constitute a kinetic barrier to the traffic of Al and a-Si across it. In other words, the diffusivity of Al and a-Si in the layer X should be small; ii) should be thermodynamically stable with respect to Al and a-Si at the highest temperature of use, further, the solubility of X in Al and Si should be small; iii) be easy to form, adhere to the involved films, possess low stress, and be compatible with other processing [21].

In our case the interfacial aluminium oxide layer (AlO_x) formed by a native way is used as a barrier layer, which influences the exchange process between Al and a-Si. This oxide layer is formed on top of the aluminium layer prior to amorphous silicon deposition. The AlO_x layer behaves as a membrane by allowing the diffusion throughout the process without participating in the layer exchange process. Hence, this native oxide layer remains in position and separates top and bottom layers during the exchange process of layers. For this reason, an aluminium oxide interfacial layer is necessary during the exchange process in order to form a continuous poly-Si film [22]. The purpose of AlO_x layer formation was explained in Ref. [23]. As shown in Figure 3.8b, the aluminium oxide interfacial layer leads to a continuous poly-Si layer while the porous silicon (Figure 3.8a) is formed when the AlO_x layer is not present. Silicon islands are formed on top of the poly-Si surface, which are originating from the secondary crystallization. These islands can be cleaned by the nonselective chemical etching as described in experimental procedures.

The formation of aluminium oxide was studied by L.P.H. Jeurgens et. al. [24]. It has been demonstrated that an amorphous oxide film of relatively uniform thickness is formed when the sample was exposed to oxygen at low temperatures (≤100°C). In this study, this uniform oxide layer is approximately 2-3 oxide monolayers thick (~0.6nm) after 100s of

oxidation due to very low mobility of the oxygen species. At higher temperatures (≥200°C), an amorphous oxide film is formed initially, which gradually becomes crystalline γ-Al_2O_3. Both lateral diffusion of the oxygen species and the rate of oxide formation increase with increasing temperature. For this reason, the thickness is in the range of 2-4nm for a growth temperature higher than 200°C. Due to exposure at room temperature, i.e. ~20°C, oxide layer has an amorphous structure. Hence, the amorphous nature can possibly change towards crystalline phase during the crystallization annealing.

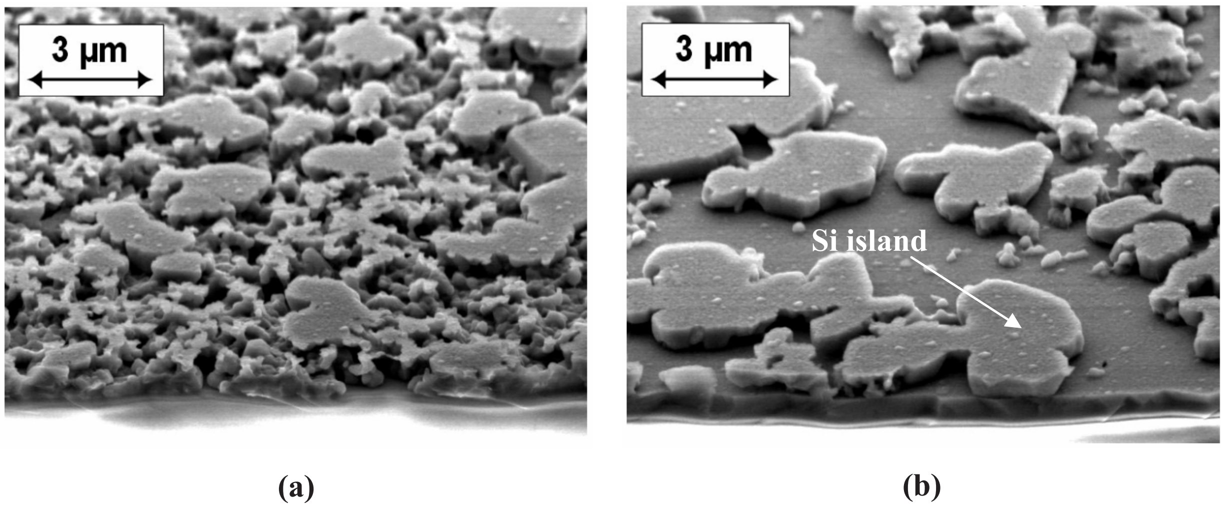
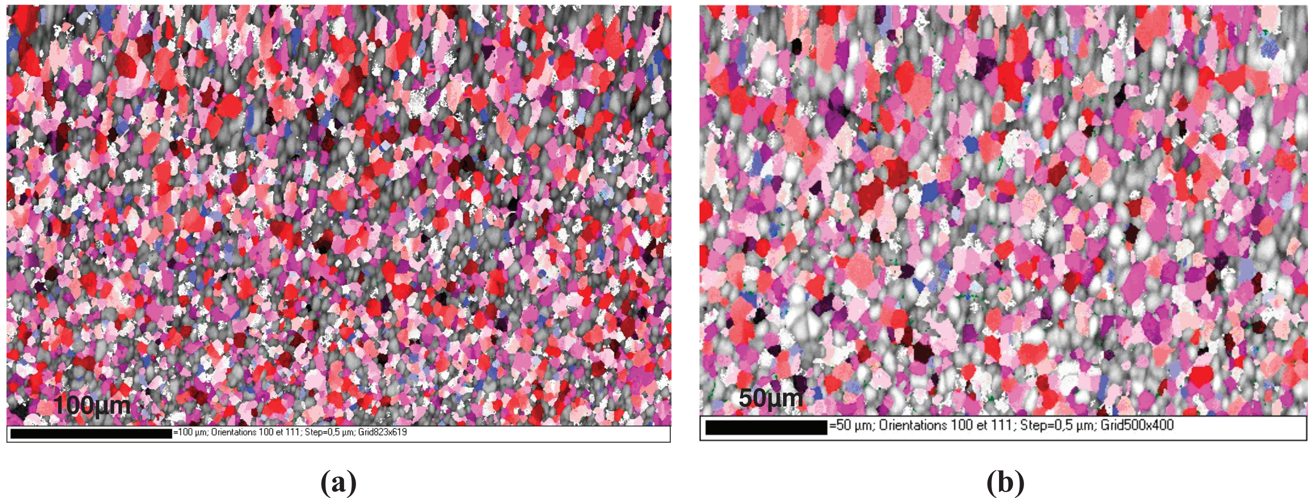


Figure 3.8: SEM images of crystallized silicon after residual aluminium etching: (a)without AlO_x interfacial layer, (b) with AlO_x layer [23]

Aluminium forms a thin layer of amorphous native AlO_x upon exposure to oxygen or dry air at room temperature. The thickness of native AlO_x was verified by using spectroscopic ellipsometry measurements. Concerning these measurements, it was observed that there is an increase of the native AlO_x layer on evaporated Al. The samples were stored in clean room during oxidation. By this way, the contamination possibility that can occur during extended storage time between sequential depositions was avoided. Furthermore, the effective parameters that have a critical role for the structure of AlO_x can be fixed independently from temperature, pressure and humidity. The first measurement was taken 3min after unloading the Al film from the deposition chamber. Then the measurements were repeated 1 day and 1 week later. The Al oxide thickness became 4.5nm after 1 week oxidation duration while the thicknesses of 2.7nm and 3.7nm were measured after 10 minutes and 1 day oxidation, respectively. The AlO_x thickness increased by about 0.8nm after the evaporation period of 1 week for the thermal evaporated Al.

The effects of oxidation duration on crystallography of final poly-Si film formed by AIC method were studied using EBSD. The aluminium layers of 300nm evaporated by using the same conditions for both cases were exposed to ambient air for 1 day and 1 week prior to 550nm thick a-Si layer deposition. The crystalline orientation maps for poly-Si layers formed on FOx-coated alumina at 500°C for 5h as a function of aluminium oxidation duration are shown in Figure 3.9a and 3.9b. Orientation maps have 420×275µm^2 and 250×175µm^2 surfaces for (a) and (b), respectively, with a mapping step of 0.5µm. The colors of orientation mapping show the crystallographic orientation of grains. The mean of each color is written at the figure caption. Other orientations are shown by grey color. Black points represent defects in AIC grown layer.



(a) **(b)**

Figure 3.9: Crystalline orientation map of the grains for fully crystallized poly-Si layer at 500°C for 5h: (a) one day aluminium oxidation; (b) one week aluminium oxidation (the colors indicate: red=<100>±9°, blue=<111>±9°, violet=<103>±9°).

The continuous poly-Si film was obtained with the average and maximum grain size of 10µm and 18µm, respectively, for 1 week oxidation of Al. Even if the oxide layer for 1 week exposure becomes thicker, which influences the crystallization time by increasing the crystallization duration [20], the crystallization was fully completed by annealing at 500°C for 5h. Furthermore, we show for the first time that more than 85% of the surface of the AIC films grown on alumina substrates are <103> preferentially oriented, instead of <100> commonly found. And there isn't any twins for <100> orientation, whereas the other orientations present twins. For the crystallographic analysis of poly-Si layer whose aluminium oxide was formed with 1 day exposure, the grain size shows difference from 1 week-oxide film. The grain size tends to decrease by reducing the thickness of aluminium oxide layer. The average grain size

becomes almost half of that of 1 week-oxide films by the value of 5µm; and the maximum grain size is 14µm. However, the crystallographic orientation analysis shows the similarity between two types of samples. In this case, it can be concluded that the oxide layer thickness affects only the grain size parameter while keeping the grain orientation properties independently. The EBSD analysis clearly shows the difference of nucleation by changing the oxidation duration, i.e. oxide layer thickness. Lower nucleation rate and bigger grain size was observed after 1 week oxidation time. Additionally, these results show that the interfacial oxide layer has a critical role that influences the crystallography of final poly-Si.

As a summary of this part, it can be concluded that aluminium oxide (AlO_x) interface plays an important role in controlling the exchange process and the diffusion of a-Si into the Al. The thickness of AlO_x depends on exposure duration in ambient air. The oxide layer thickness affects the nucleation, i.e. the grain size; but no significant effect on the grain orientation properties. As a fact, lower nucleation rate and bigger grain size was observed with thicker oxide layer thickness.

3.3.3 Effect of the Aluminium Layer

The crystallization of amorphous silicon occurs in the aluminium layer. Thereof, the structure of aluminium has a key role in aluminium induced crystallization process and the quality of formed poly-Si film. There are two parameters concerning the aluminium layer that influences the nucleation rate of Si, namely the oxygen concentration and the grain size of aluminium.

The oxygen present during the aluminium deposition has a strong influence on the morphology of grains and on the kinetics of growth as reported in Ref. [25]. Klein et. al. showed that the exchange process time and the grain size of final poly-Si are affected by oxygen in Al layer. Figure 3.10 depicts the influence of oxygen flow (f_{O_2}) during aluminium deposition on annealing time.

The layer exchange could be completed in 90min without oxygen flow; only the annealing time of 17min is enough in case of presence of 2sccm oxygen flow during aluminium deposition. The reason of this drastic decrease in the annealing time with the aluminium deposition under O_2 can be correlated to the faster diffusion of Si atoms through Al/a-Si interface and within the aluminium layer. The aluminium layer with a higher oxygen

concentration can include more density of defects that may cause faster diffusion in grain and thereby resulting in a reduced process time.

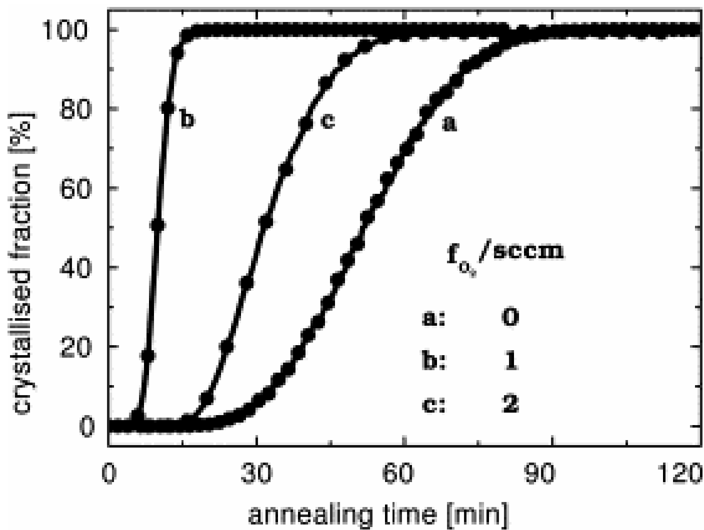


Figure 3.10: Crystallized fraction as a function of annealing time for samples with different oxygen flows (f_{O2}) during aluminium deposition: (a) f_{O2}=0sccm, (b) f_{O2}=1sccm, and (c)f_{O2}=2sccm [25].

In present investigations, the effect of oxygen within aluminium layer is studied by changing the vacuum level of the electron beam system during Al deposition. Two samples named A and B were prepared to analyse this effect on final poly-Si properties. For both conditions, FOx-coated alumina substrates were used. The difference between A and B is the vacuum level during the aluminium deposition. Sample A was prepared with a high vacuum of 2×10^{-6}mbar, while low vacuum of 1.2×10^{-2}-1×10^{-4}mbar was used during aluminium deposition for sample B.

The EBSD technique was used to elucidate the crystallographic texture, preferred orientation and defects for the A and B poly-Si films. The sample areas as shown in Figure 3.11a and 3.11b are $240\times140\mu m^2$ and $405\times220\mu m^2$, respectively, with a mapping step of 0.5µm. The different colors of the orientation map correspond to the different crystallographic orientations of the grains. The corresponding orientation for each color is written in the figure caption. Other orientations are shown in grey. Black points are defects in the AIC layer. The average grain size can be found from this figure. The inverse pole figure that identifies the orientation by the color codes is shown in Figure 3.11c and 3.11d.

Thus, the average grain size is 10µm and 6µm for sample A and B, respectively. Many grains are <100> oriented for sample A as identified from Figure 3.11c. In contrast, there is

no significant preferred orientation for sample B. It means that higher oxygen content in Al results in lower crystal quality. This result can be deduced also from Figure 3.11d, whereas the orientation gradient is very few as defined in its color chart. It can be concluded that the lower vacuum level during aluminium deposition influence strongly the crystallography of aluminium. The defects, which are the result of increased oxygen content, enhance the nucleation rate and cause the smaller average grain size.

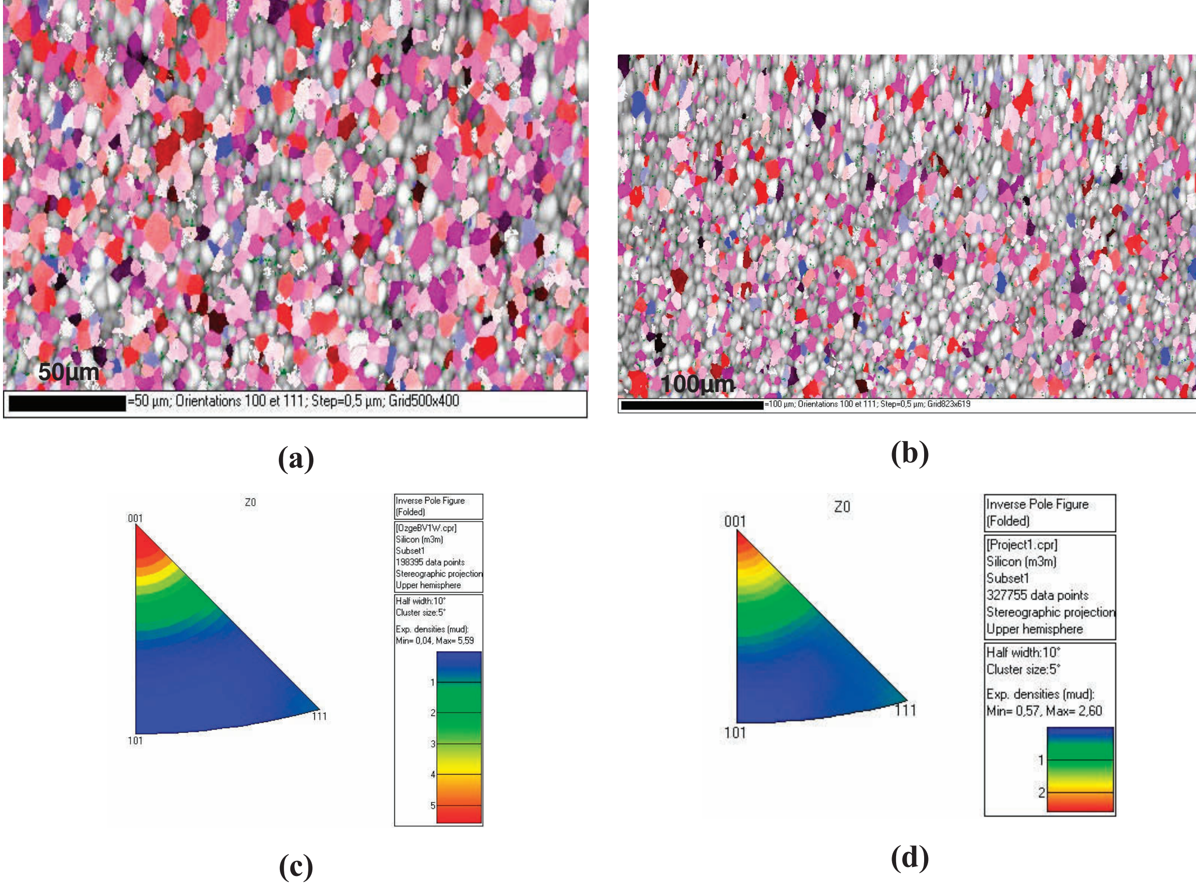


Figure 3.11: EBSD analysis of the polysilicon films sample A (a) and B (b) giving the crystalline orientation map of the grains (the colors indicate: red=<100>±9°, blue=<111>±9°, violet=<103>±9°), (c) and (d) Inverse Pole figures for sample A and B, respectively.

The second parameter that strongly affects the nucleation of Si is the grain size of the aluminium layer. Indeed, the final grain size of poly-Si film depends on the crystallization rate and thereby on the size of Al grains. The exchange process is faster with smaller Al grain size that gives rise to higher nucleation rate and smaller final Si grain size [20]. The grain size of the polycrystalline aluminium depends on the evaporation rate of the system [26]. There is a direct correlation between these parameters: higher the deposition rate, larger the grain size. This dependence is depicted in Figure 3.12. The grain size of 1µm thick aluminium films

deposited on silicon wafers is shown to be a function of deposition rate and substrate temperature.

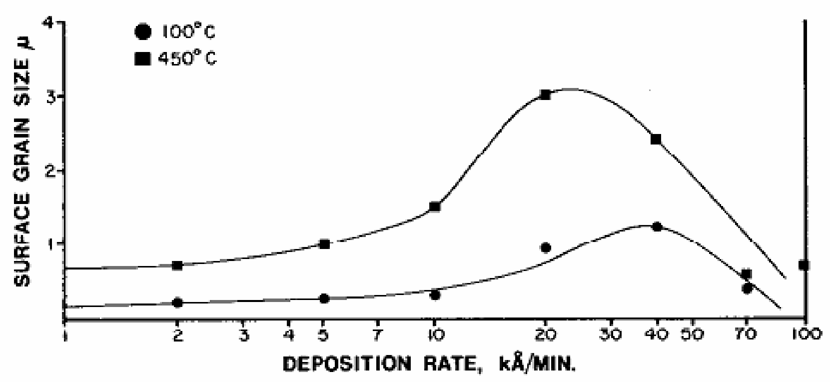


Figure 3.12: Grain size of aluminium evaporated at 10^{-5}Torr versus deposition rate as a function of substrate temperature [26].

To check the effect of aluminium grain size on polysilicon grain size two different electron beam evaporation system have been used to change the deposition rates of the aluminium layer on FOx-coated alumina.

Two samples named C and D were prepared for this study. The samples differ by the electron beam evaporation systems used for Al deposition. The differences between these evaporation systems are the deposition rate of Al and the distance between the target and substrate. The Al deposition rates for C and D are 16Å/s and 25Å/s, respectively, and the distance between the target and substrate is 1m and 0.5m, respectively. These characteristics most probably affect the morphology and structure of the polycrystalline aluminium film, and therefore on the AIC layers exchange. An overview of the deposition systems used for samples C and D and of grain sizes are given in Table 3.3.

Name	*Al Deposition Rates* (Å/s)	*Mean Grain Size* (μm)	*Maximum Grain Size* (μm)
C	16	15	65
D	25	7	24

Tablo 3.3: Deposition rate of aluminium; and mean and maximum grain sizes as deduced for samples C and D.

The electron backscattering diffraction (EBSD) tool was used to characterize samples C and D. The crystalline orientation map for C and D are shown in Figure 3.13a and 3.13b, respectively. The average and maximum diameters of the grains are about 15μm and 65μm,

respectively, for sample C. However smaller grain sizes were obtained for sample D that are about 7µm and 24µm for the average and maximum diameters of the grains, respectively. On the other hand, more than 50% of the surface of the AIC films grown on alumina substrates are <103> preferentially oriented for C and D (see Figure 3.13c and 3.13d). This is different from the usually represented data when preferential <100> direction is commonly found [19,27]. Furthermore, no twins are observed for the <103> oriented grains for C and D, whereas the other orientations present twins. A careful look on EBSD analysis shows that there is an orientation gradient at <100>, where the graded color code is used for the orientation images. In fact, according to EBSD results, the crystallographic orientation properties are almost the same for samples C and D, except for the grain size. Clearly, the grain size of the AIC layer depends on the Al deposition method. By changing the electron beam evaporation systems, which have different deposition rates and different distances between the target and substrates, the grain size of the polysilicon AIC layer changes. It can be concluded that lowering the Al deposition rate may increase the Al grain size resulting in poly-Si film with larger-grain sizes.

The EBSD data can also be used to identify random grain boundaries (RGB), low-angle grain boundaries (LAGB, angle<2°) and coincident site lattice boundaries (CSL) that are Σ3, Σ9 and Σ27. Crystallographic defects and the comparison of defect distributions for sample C and D are shown in Figure 3.14.

Random grain boundary, low-angle boundaries and twin boundaries of Σ3 (59-60°), Σ9 (38-40°) and Σ27 (35-37°) are observed. The distribution of RGB is almost the same for both samples, and the Σ3 boundary is also dominant for both cases. For sample C, a very high distribution of Σ3 twin boundaries is observed while no third order (Σ27) twin boundaries are present. The distribution of LAGB is lower for sample D. If the twin boundaries of sample D are as compared with those of sample C, the distribution of high-energy grain boundaries (Σ9 and Σ27) increase while Σ3 (low-energy grain boundary) is decreasing. Furthermore, distribution of low-energy CSL boundary (Σ3) is significantly higher than that of high-energy grain boundaries.

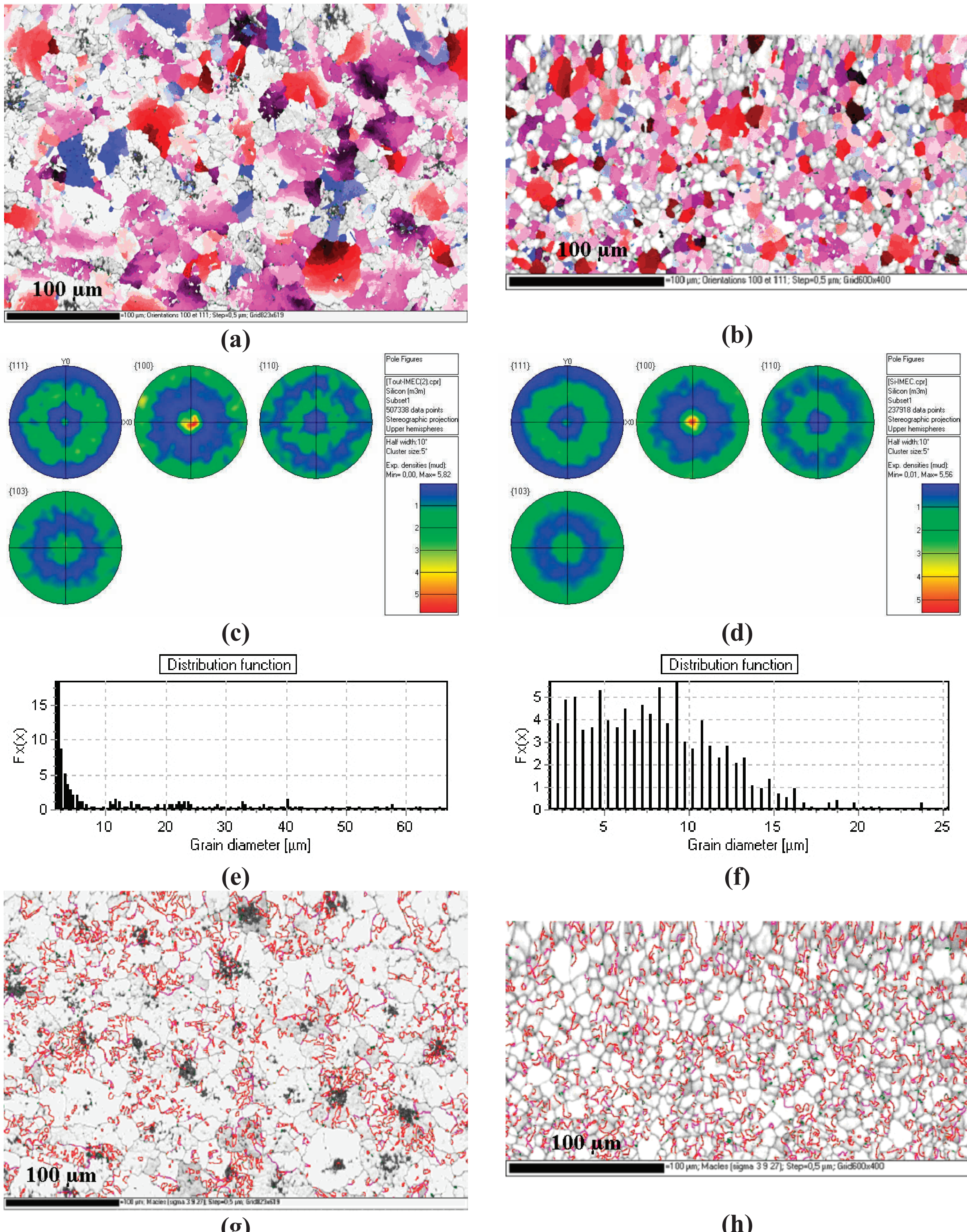
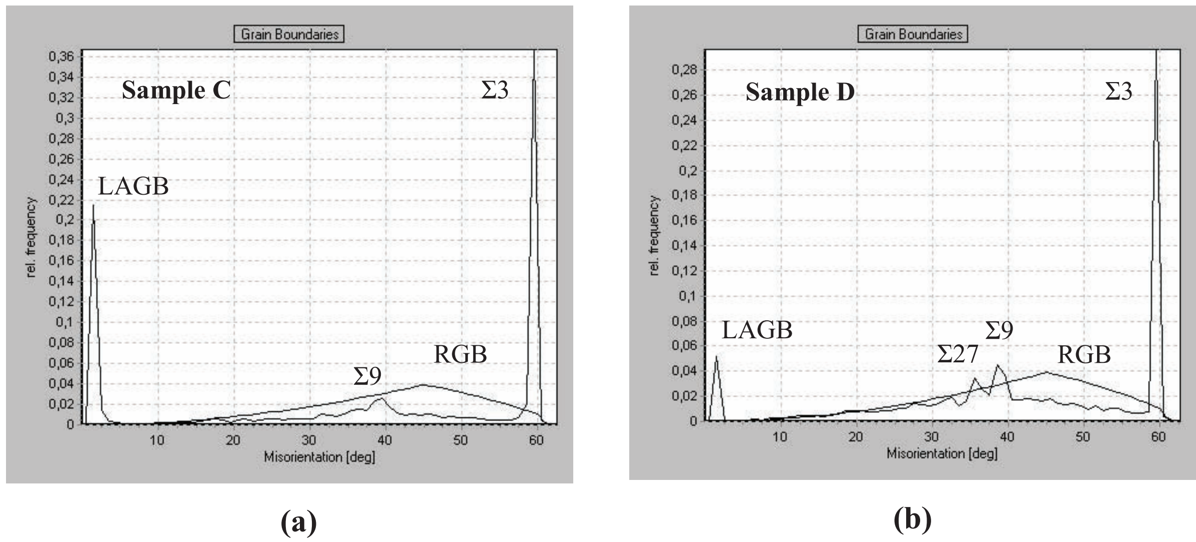


Figure 3.13: EBSD analysis of the grains for sample C and D: (a) and (b) Crystalline orientation map of the grains (the colors indicate: red=<100>±9°, blue=<111>±9°, violet=<103>±9°); (c) and (d) Pole figures; (e) and (f) grain size distribution; (g) and (h) map of the twins (red=Σ3, purple=Σ9, yellow=Σ27).



(a) **(b)**

Figure 3.14: Distribution of coincident site lattice boundaries and random boundaries: (a) for sample C; and (b) for sample D.

This distribution difference of CSL boundaries can be attributed to low-energy CSL boundaries, which are more likely to be growing on larger area. During grain growth, some grain boundaries are eliminated when two grains separate or a tetrahedral grain disappears, while others are created when two grains impinge. Because of the fact that the grain growth leads to a reduction in the total interfacial area, more grain boundaries must be eliminated than created. However, higher-energy grain boundaries are preferentially eliminated from the network during grain growth that leads to a higher population of low-energy grain boundaries [28]. The lower-energy boundaries, that are growing, have larger areas than the higher-energy boundaries. With reference to this, the bigger grain size and higher Σ3 distribution for sample C can be explained.

As a summary of this part, we have shown that the amount of oxygen as a pollutant during the aluminium deposition, and the grain size of aluminium layer strongly affect the morphology of grains and on the kinetics of growth. Aluminium layer with a higher oxygen concentration gives more defective Al layer; and this may cause faster diffusion in grains. Hence, enhancement in nucleation and reduction in grain size can be the result of increased oxygen content during Al deposition. Additionally, higher oxygen concentration during Al decreases the Al quality and hence affecting the final poly-Si quality. Finally, poly-Si films with larger grain size are formed by lower Al deposition rate.

3.3.4 Effect of Substrate

i) Potential substrates

One of the key technological challenges to achieve a commercially viable thin-film polycrystalline silicon (<10µm thick) solar cell technology is an optically, mechanically and chemically compatible substrate. The requirements for the substrate material are severe [29]. From a fabrication standpoint, the substrate must be inert to all of the process chemicals and temperatures. Mechanical strength and thermal expansion coefficient (TEC) matching are needed to prevent the film from excessive stress, breakage and/or cracks in the cooling phase after high temperature processing. There are several good candidates for thermal expansion matched ceramic or some glasses. The substrate must also provide good wetting and nucleation during the film growth process without contaminating the film. The substrate can be conducting or insulating, depending on device requirements. For solar cells process fabrication the substrate must be flat and the surface must be smooth and free of defects. Another thermal property to be mentioned is the material's thermo shock resistance, for which the substrate must be compatible with the heat up and cool down ramps applied during the high temperature processes. The substrate-silicon interface must provide a high degree of diffuse reflectivity and surface passivation. Finally, the substrates must be low cost. The cost of the substrate plus the active Si thin film must be substantially lower than that of standard multicrystalline wafers; otherwise the c-Si thin film solar cell cannot be cost effective. Many substrates have been utilised to fabricate thin silicon solar cells, namely glass [30,31], ceramics [32,33], glass-ceramic [34,35], steel [36,37], graphite [38,39], upgraded metallurgical silicon sheets or wafers [40,41]. The main properties for candidate substrate materials are listed in Table 3.4.

Thus, a variety of metals can be used for thin film technology. In general, the advantages of metal substrates are high thermal conductivity and relatively low cost. But their high TEC is mismatching to silicon. Graphite has unique physicomechanical and chemical properties, of which the main ones are the high resistance to thermal shock, high thermal conductivity, high strength, low TEC. The main disadvantages using of graphite in high-temperature processes are the low heat resistance and the erosion and burning in gas flows [42]. Soda-lime glass has been widely used in the fabrication of flat panel display devices as a transparent glass substrate and in photovoltaic module production. When transparent insulator substrate is composed of soda-lime glass, a silicon oxide coating or a tin oxide coating must be applied on the surfaces of the substrate. These coatings are preferable since they serve as

buffer films to prevent the alkali metal components in soda-lime glass from eluting and diffusing into the surface. Even though soda-lime glass is mass-produced with a large volume flat at low cost, the lower softening temperature (~580°C) is the disadvantage for high-temperature processing.

Material	*Estimated Price of substrate (€/m²)*	*Softening point (°C)*	*TEC ($10^{-6}K^{-1}$)*	*Transparent*	*Conductive*
Silicon	30-40	1400	4.2	no	yes
Stainless steel	4–10	>1000	12	no	yes
Graphite	10-100	>1410	4.5	no	yes
Soda-lime glass	3–7	~580	80	yes	no
Borosilicate glass	20–40	~820	3	yes	no
Mullite ceramic	30–40	>1410	5	no	no
Alumina ceramic	30-40	2054	7.5	no	no
Glass-ceramic	~30	~1100	3.5-4	yes	no

Tablo 3.4: Properties of substrate materials for thin film solar cells.

Ceramics are among the most frequent used substrate materials. Ceramics, mainly alumina (aluminium oxide, Al_2O_3) and mullite ($3Al_2O_3$-$2SiO_2$), are the most promising substrate materials in high-temperature electronic packaging technologies [43,44]. This is because of their dielectric behaviour, thermal and chemical resistance, low thermal expansion and low cost. The drawback of ceramics is the warped and rough surface. In particular, the higher surface roughness and lower thermal conductivity are the disadvantages of mullite ($3Al_2O_3$-$2SiO_2$) substrates when compared to alumina (Al_2O_3). On the other hand, glass-ceramic (GC) materials share many properties with both glass and more traditional crystalline ceramics. It is formed as a glass, and then made to crystallize partly by heat treatment. Glass-ceramic is a mechanically strong material and can sustain repeated and quick temperature changes up to 1100°C. At the same time, it has a very low heat conduction coefficient and low TEC, which is quite compatible with silicon's, and can be made nearly transparent.

In this work, we have mainly used alumina and glass-ceramic as substrates for the AIC seed layer and subsequent thickening. The alumina substrates are provided by COORS Company while the glass-ceramics were made specifically by CORNING in the frame of a

national project called POLYSIVERRE and funded by the French National Research Agency. Such glass-ceramics possess a thermal expansion close to that of silicon. Both substrates are insulating, but alumina can be used in a substrate configuration while the glass-ceramic allows the superstrate configuration. Both can be made at large area (>1m^2).

ii) Properties of used substrates and their coating

Since the roughness and composition of the substrate can control the nucleation rate and therefore the final crystallographic quality of the formed poly-Si seed layer by AIC, we have investigated the morphology of the alumina and GC substrates before and after being coated with a silicon oxide or a silicon nitride layer, respectively. Many experimental studies were done showing that the roughness of the substrate plays an important role on the Si thin film properties [45,46].

For the surface morphology study, we have used the optical interferometry technique. With white light scanning interference microscopy, surface roughness from nanometers to many microns can be measured rapidly and non-destructively [47]. In fact, interference microscopy provides a convenient solution for profiling difficult surfaces, giving a large axial dynamic range (3nm–100µm in our system), a higher lateral resolution (<0.4µm) than that of stylus profilometry. Two microscopes were used in this work: a Leitz microscope with a ×50 (NA=0.85) Linnik objective and an incandescent bulb for producing white light, and a Leica DMR-X microscope with a ×40 (NA=0.6) Mirau objective and a halogen bulb with an interference filter (centre wavelength of 448nm) to provide blue–violet light. A Sony XC-75E CCD camera with a standard 8 bit imaging board was used for imaging up to 760×572 pixels. The sample was mounted on a piezo-controlled table with LVDT position control (sensitivity 10nm), giving an axial range of 100µm, mounted on precision stainless steel *XY* motorised tables.

a. Aluminium substrate

The alumina substrates have usually a quite rough structure due to open pores at the surface of the ceramic relating to grained structure of alumina powder and the fabrication techniques by using this alumina powder. Mainly this rough surface structure is undesired condition for the formation of high quality Si films. The alumina substrates used here are produced by Coors ADS996 Company. Figure 3.15a shows the surface morphology of the bare alumina substrate. The image area is 43x43µm^2. It is found that the peak to valley

roughness is very high, reaching about 5.6µm. Such roughness is not suitable for the foreseen application.

To reduce the surface roughness of alumina substrate, flowable oxide (FOx-25, provided by Dow Corning) solution is spun on the surface with an acceleration of 5000rpm/s during 2s and a speed of 3000rpm. The FOx-25 liquid solution is a 2.5µm thick resin and allows an effective planarization due to its liquid phase up to 400°C. The FOx solution contains a Hydrogen Silsesquioxane Resin [HSQ: $(HSiO_{3/2})_n$]. After spin coating, the solution was baked at 150-350°C and thermal annealed at around 800-1000°C in order to evaporate the organic solvents and impurities resulting in a solid barrier layer. The aim of using the FOx layer is to decrease the surface roughness of bare alumina, since a smoother substrate surface leads to AIC layers of improved structural and electrical quality [48].

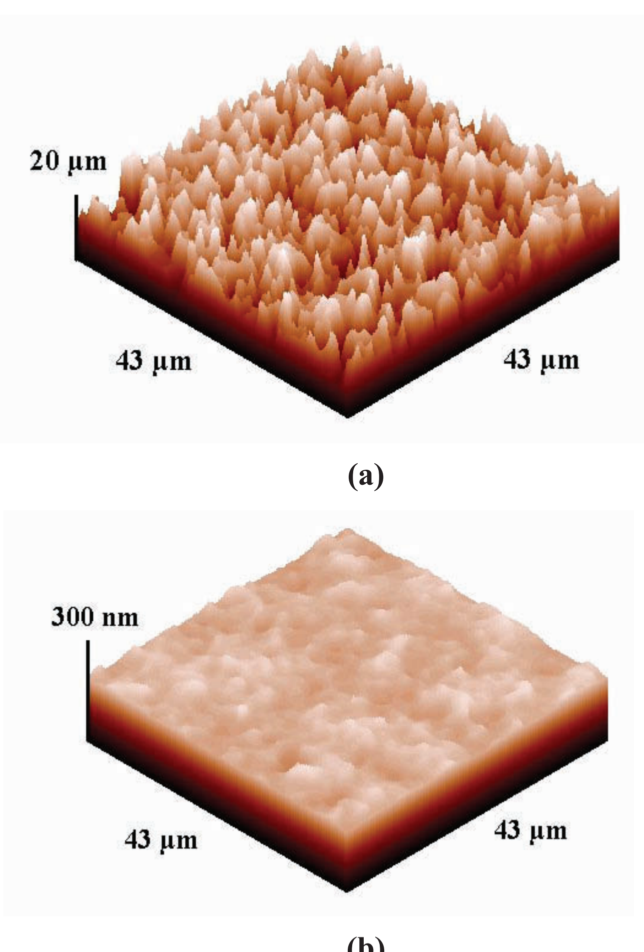


Figure 3.15: Interference microscopy measurements showing the surface morphologies of: (a) bare alumina, and (b) FOx-coated alumina.

Figure 3.16 plots the infrared absorption spectrum of the FOx solution coated silicon after baking at 200°C for 15min on hot plate and annealing at 1000°C for 1min under Ar flow

in a rapid thermal process (RTP). As shown in Figure 3.16, the FOx coated film consists of only silicon-oxide bonds, which means that FOx-25 turns into SiO_2 after annealing. The FOx coated layer has another important function of a barrier layer that acts against the exo-diffusion of impurities from alumina substrate into the silicon film during the AIC layer formation and subsequent high temperature epitaxy. This possible contamination study was discussed in detail in Ref. [49]. Deep level transient spectroscopy (DLTS) measurements were used for impurities detection showed the main harmful impurities such as Mg, Mn and Fe in silicon are drastically reduced when coating the alumina substrate with FOx.

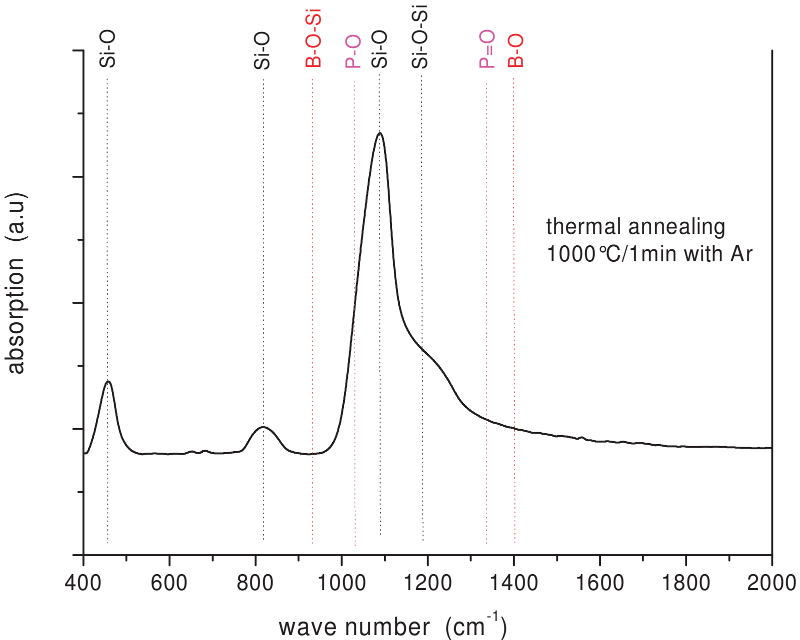


Figure 3.16: Infrared absorption spectra for FOx layer. This layer was spun on silicon substrate, baked at 200°C for 15 min and annealed at 1000°C for 1min under Ar flow [50].

The surface roughness of FOx coated alumina substrate is shown in Figure 3.15b. It is found that the peak to valley roughness strongly decreases from 5.6µm for the bare alumina substrate to 0.16µm for the FOx-coated substrate. This is expected since the main function of the FOx layer is the planarization of the rough surface. Thus, the FOx-alumina substrate is much smoother compared to bare alumina. Besides, a significant enhancement in the average grain size of the resulting poly-Si on substrates coated with FOx has been already for this reason in the following parts, only FOx-coated alumina substrates are used.

b. Glass-ceramic substrate

Glass-ceramic is another promising candidate for high temperature approach that can offer to minimize the defects density and enlarge the silicon grains of the structure. However, glass-ceramic might also be highly contaminated with impurities. Therefore, the glass-ceramic substrates need to be coated with a barrier layer to prevent the out-migration of some substrate's elements into the Si thin film during high temperature processing. SiN_x is a good candidate as a diffusion barrier for potential contaminations (O, B, Na, K, Al, Fe, etc.) from the glass.

Glass-ceramic substrates provided by CORNING are 1mm thick. The deposition of the SiN_x layer on the GC was performed by using the electron cyclotron resonance plasma enhanced chemical vapor deposition system (ECR-PECVD) as described in Appendix A. However, the experimental parameters for SiN_x deposition shown in Table 3.5 are chosen such that the barrier film can also play the role of antireflection coating layer in the superstrate configuration. The thickness of SiN_x is ~85nm.

Parameter	*Value*
Microwave power (W)	500
Growth temperature (°C)	400
Pressure (mbar)	$2.2x10^{-2}$
SiH_4 flow rate (sccm)	14
NH_3 flow rate (sccm)	21
Deposition rate (nm/min)	9.7

Tablo 3.5: Operational parameters for SiN_x deposition in the ECR-PECVD reactor.

One important advantage of the use of glass-ceramic as a substrate is its optical transparency that should be kept up to the end of the different low and high thermal processes to make the polysilicon cells. This is vital for superstrate cell configuration, where the glass substrate is not only used as supporting structure but also as window for the illumination and as part of the encapsulation. We have measured the optical transmittance of glass-ceramic substrates before and after different thermal annealing. The spectra were obtained using a PERKIN ELMER Lambda 19 UV/VIS/NIR spectrometer within the wavelength range of 250–1200nm. The transmittance spectra are shown in Figure 3.17.

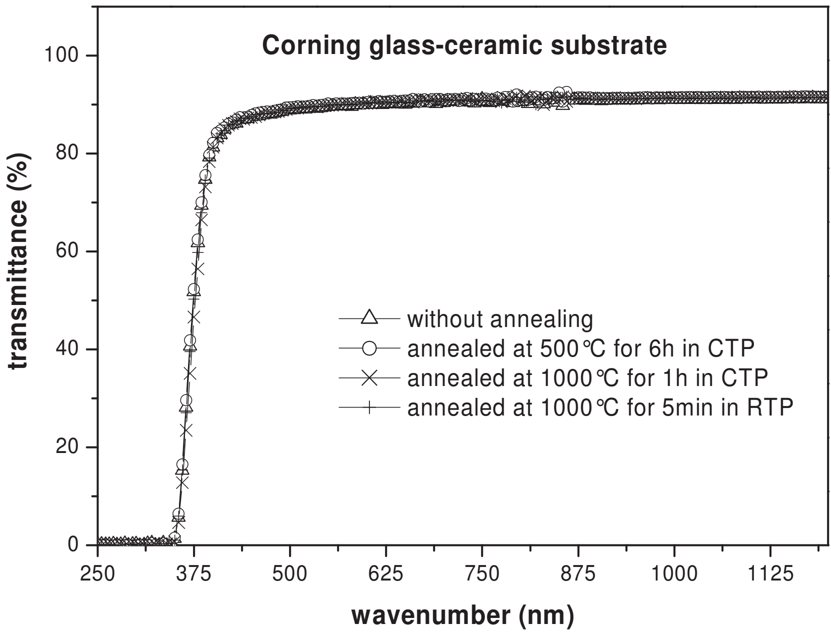


Figure 3.17: Optical transmittance spectra of Corning glass-ceramic before and after thermal annealing.

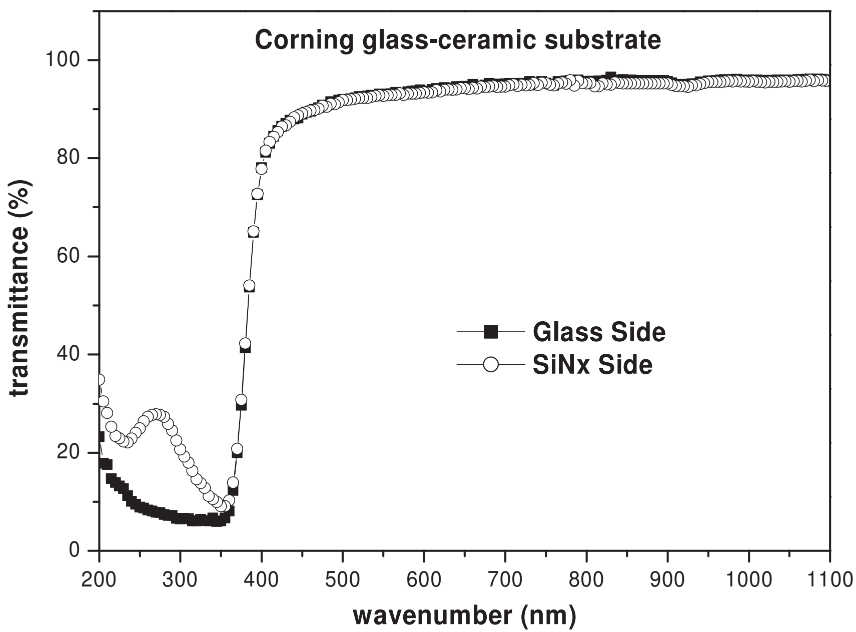


Figure 3.18: Transmission spectra of SiN_x layer coated glass-ceramic, measured from glass side and SiN_x side.

A transmittance value of about 92% is recorded for the non-annealed glass-ceramic substrate. Heating it at 500°C for 6h (like for AIC process) or at 1000°C for 1min or 1h (like during epitaxy) did not affect the optical transmission of the glass. The glass-ceramic keeps its

optical transparency even after the post high-temperature process. These results show the suitability of such glass-ceramics for the high temperature (~1000°C) applications.

The transparency of the glass-ceramic substrates was measured also after they were coated with SiN_x layer. These transmittance measurements were performed either from glass side or from SiN_x side to analyze if the superstrate configuration is judicious. As shown in Figure 3.18 (open circles), the optical transmission of the SiN_x coated GC is almost 93% in the visible range (400–800nm), similar to that of the bare GC. The optical transmittance carried out from different sides looks similar except in the deep UV side. The behaviour of the transmittance curves observed between 200-400nm when illuminating from the SiN_x side is due to the interference effect between the SiN_x layer (~85nm thick) and the glass (1mm thick). As a result, we can conclude that the SiN_x coated glass-ceramic is suitable for being used in a superstrate configuration.

What about the roughness?? Similar to the alumina case, we have used the white light scanning interference microscopy to investigate the surface morphology of bare and SiN_x coated glass-ceramic substrates. Figure 3.19 shows a 79x119μm^2 sized image for both substrates. The bare GC has a peak to valley roughness of 18.5nm, quite reasonable. After SiN_x coating, the roughness is reduced to 8.2nm. Thus, deposition of the barrier layer clearly decreases the surface roughness of the as-grown glass-ceramic substrate. We might expect a higher-quality crystalline structure through an increase in the grain size [48].

Since the AIC process requires the deposition of an aluminium layer prior to the silicon deposition and exchange process, it is important to check if the aluminium deposition made by an electron beam affects the surface roughness of the coated alumina or glass ceramic substrates. The results are summarized in Table 3.6.

Substrate+coatings	*R* (*nm*)
Bare Al_2O_3	5600
Al_2O_3/FOx-25	160
Al_2O_3/FOx-25/Al	200
Bare glass-ceramic	18.5
glass-ceramic /SiN_x	8.2
glass-ceramic /SiN_x/Al	6.1

Tablo 3.6: Surface roughness *R* (peak to valley) of various coated and uncoated ceramics as measured by interference microscopy.

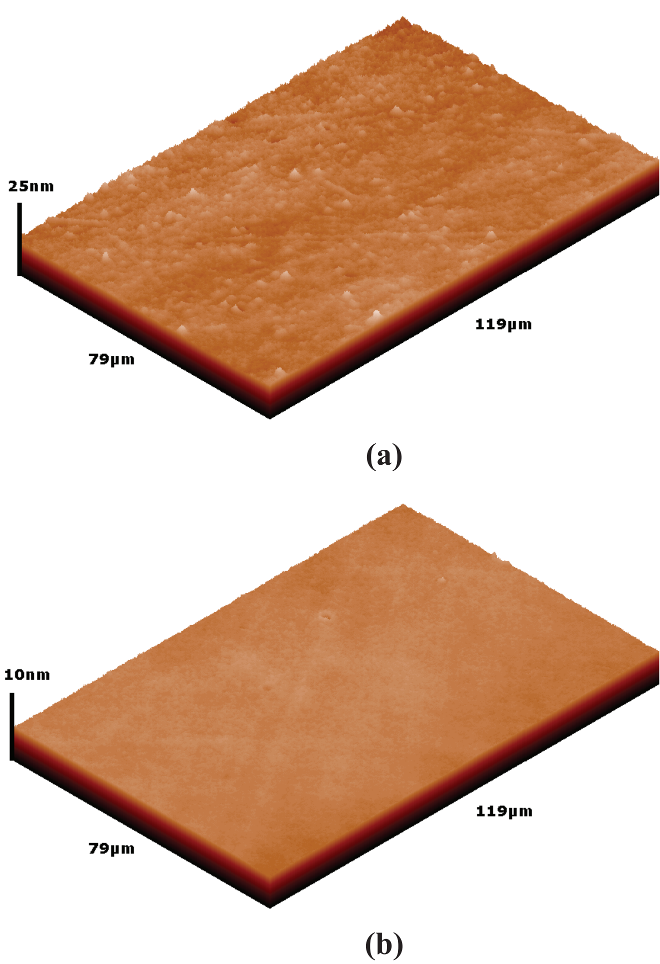


Figure 3.19: Evolution of surface morphology of: (a) bare, and (b) SiN_x-coated glass-ceramic, using interference microscopy 3D view after filtering.

The deposition of a 200nm thick aluminium film increases slightly the roughness of the alumina/SiO_2 sample, while it decreases for the glass/SiN_x sample. For both cases anyway the surface roughness is strongly decreased after coating, which is favourable for an efficient layers exchange.

iii) Effect of substrate on the crystallographic quality

In this paragraph, we compare the crystallographic quality of AIC grown polysilicon layers on the selected coated ceramic substrates. We used Raman spectroscopy and EBSD analysis as characterization tools.

Figure 3.20 plots the Raman spectra of poly-Si seed layers grown at 500°C for 5h on alumina/SiO_2 and GC/SiN_x substrates. The Raman analysis was performed using a RENISHAW RAMASCOPE 2000 micro-Raman spectrometer with an excitation wavelength of an Ar^+ laser at 488nm. The resolution of micro-Raman system is $1.0cm^{-1}$. The spectra were

normalized with respect to the LO/TO line of crystalline silicon at 520.1cm^{-1}. Very sharp peaks at 520cm^{-1} are observed for both cases, which definitely indicate very good silicon crystallization. As the peak position is close to that of the sc-Si (520.1cm^{-1}), it means that the film is under negligible stress. The other important parameter extracted from the Raman analysis is the full width at half maximum (FWHM). The FWHM value describes the crystallization quality for the poly-Si films. From Figure 3.20, the FWHM value for GC/SiN_x/Si is 5.9cm^{-1}, which is very close to that of reference single crystalline silicon, while it is 7.04cm^{-1} for alumina/SiO_2/Si. Thus, the roughness of the substrates has an effective role on the final film quality. These results augur well for a higher silicon crystalline quality for AIC films on glass ceramics compared to those on alumina.

To have more insights on the silicon quality, complementary crystallographic characterizations were carried out on the poly-Si formed by AIC on alumina and glass-ceramic using the EBSD technique. In this case, the annealing temperature of exchange process was fixed to 475°C. The annealing time was chosen longer (8h) for glass-ceramic than for alumina (6h) since the layer exchange rate on glass is slower.

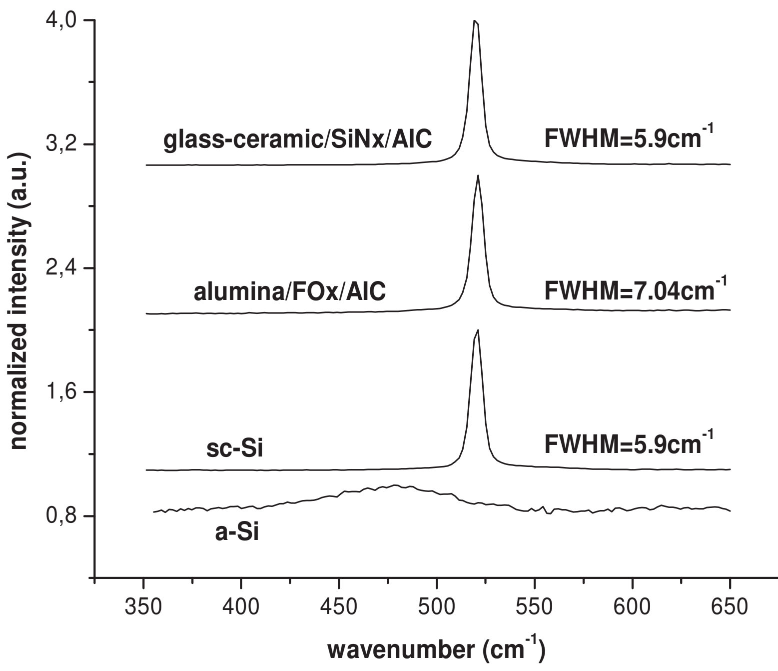


Figure 3.20: Raman spectra of poly-Si thin films formed on glass ceramic and alumina. The Raman spectra of sc-Si and a-Si are shown as a reference.

The EBSD results show that continuous poly-Si films were formed on alumina and glass-ceramic after annealing at 475°C for 6h and 8h, respectively. Figure 3.21 shows the crystalline orientation mapping images for the AIC poly-Si films formed on FOx-coated

alumina (a) and SiN_x-coated glass-ceramic (b). The orientation maps have 420x275µm^2 and 250x175µm^2 area for Figure 3.21a and 3.21b, respectively, with a mapping step of 0.5µm. The colors of the orientation mapping are indicative of the crystallographic orientation of the grains. The mean of each color is written in the figure caption. The other orientations are showed by the yellow color.

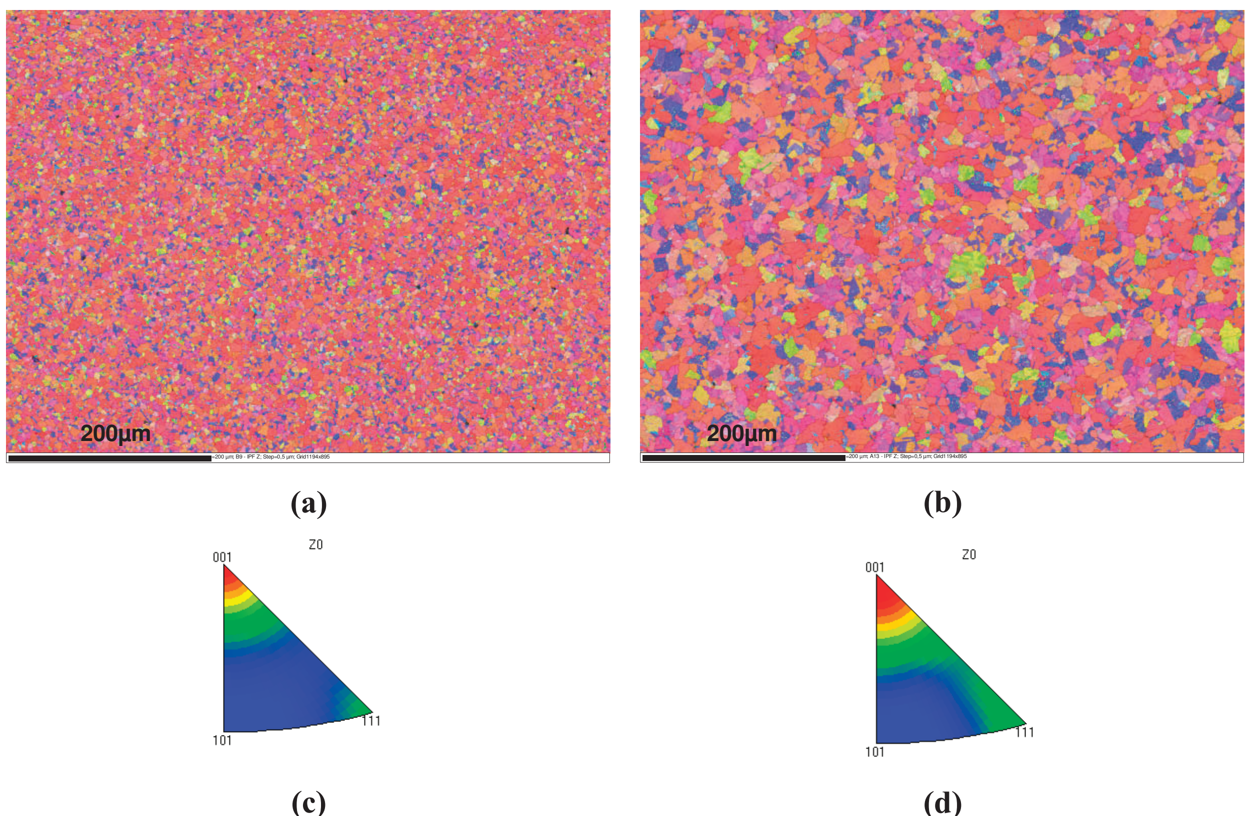


Figure 3.21: Orientation mapping analysis of poly-Si layers formed by AIC at 475°C on; (a) FOx-coated alumina, and (b) SiN_x-coated glass-ceramic. Inverse Pole Figures in the z axis correspond to: (c) alumina sample, (d) glass-ceramic sample. The colors indicate: red=<100>±15°, blue=<111>±15°, green=<101>±15°.

Such orientation maps are very useful to evaluate the grain size. The difference in grains size for both samples is obvious. The grains size can be estimated by summing up over number of data points in each grain. The grain diameter is deduced by assuming a circular disklike geometry of similar area. The grains size distribution as extracted from the EBSD map is shown in Figure 3.22. The mean grain diameter derived from grain surface, the standard deviation, as well as the number of analyzed grains was extracted from Figure 3.21. The shape of the distribution profile is significantly different with the substrate. The distribution of the grain size is more homogenous for glass-ceramic (σ=10.8µm) than that of

alumina (σ=5.1µm). This means that the nucleation rate during the crystallization process is constant in case of using SiN_x coated glass-ceramic substrates [51]. The Si AIC layer formed on GC at 475°C attains 25.2µm average grain size, while it is close to 8µm for alumina samples. The small average grain size and the very broad grains distribution observed for alumina/SiO_2/Si can be correlated to the important roughness of the surface prior to the silicon deposition and the exchange process. The higher surface roughness favours enhanced nucleation rates resulting in competing grown grains and, finally, in small grains.

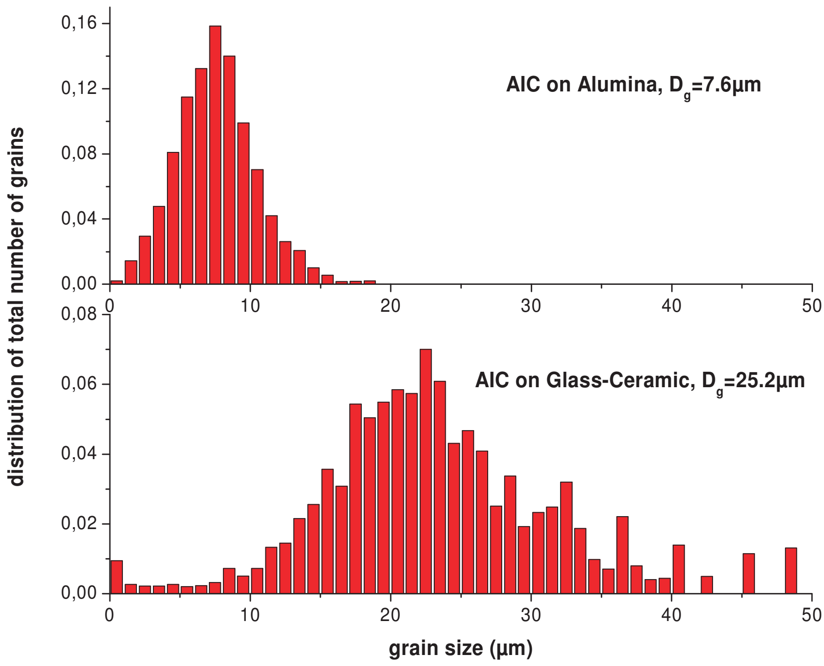


Figure 3.22: Average grain size (D_g) and grain size as a function of substrate for the poly-Si films formed by AIC at 475°C on alumina and glass-ceramic substrates.

The Inverse Pole Figures of Figure 3.21c and 3.21d represent a description of the samples orientation with respect to the crystal coordinate system. The mapping images of AIC layers indicate that there is a preferential crystalline orientation for both types of samples. The preferred orientation for alumina/SiO_2/Si and GC/SiN_x/Si is <100> as usually reported for AIC poly-Si layers. This well orientated grain structure corresponds to the high crystalline quality.

For more detailed analyze about the <100> fiber texture deduced from the EBSD maps, the distribution of the angular deviation (ϑ) from <100> orientation was investigated. The resulting frequency distribution (number of pixels for a given ϑ, binned every 5°, over total number of pixels) as a function of ϑ is given in Figure 3.23. The crystallographic

orientations are comparable for AIC layers formed on alumina and glass-ceramic. In this graph, the minimum deviation (5°) means a fully <100> oriented layer while the maximum deviation of 55° corresponds to the <111> plane. The majority of grains (60-70%) in these poly-Si films has an orientation deviation between 5° and 25° relative to <100> orientation. The occurrence of <100> orientation is almost the same for SiN_x-coated glass-ceramic and FOx-coated alumina used samples. The <110> orientated silicon is indicated by deviation angles in the range of 30-45° while that is in the range on 45-55° for <111> orientated silicon. Either <101> or <111> show the lower distribution for both case of samples than <100> orientation. A 74% of the total surface was covered by <100> for alumina used sample while surface coverage of <101> and <111> orientated grains is only 18% and 8%, respectively. The surface fractions of <100>, <101> and <111> are 72%, 20% and 8%, respectively, when considering glass-ceramic substrate used poly-Si film. This results show that <100> is the preferred orientation for both types of samples. No twins are observed for the <100> oriented grains, whereas the other orientations present density of twins. The reason for this behaviour is the orientation of the initial nucleus close to the <100> plane [27].

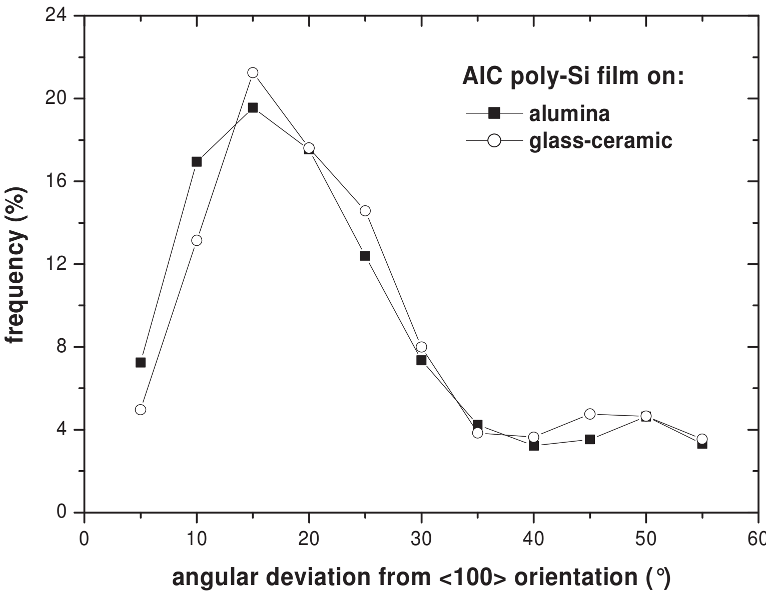


Figure 3.23: <100> fiber texture of the AIC samples formed on alumina and glass-ceramic.

Figure 3.24 plots the distribution of misorientation angles as deduced from the EBSD analysis for the poly-Si formed at 475°C by AIC on FOx-coated alumina and SiN_x-coated glass-ceramic substrates. The main crystallographic defects present in the continuous poly-Si layers are the low-angle grain boundary (LAGB, angle<2°) and the coincident site lattice (CSL) boundaries consisting of twin boundaries of first order (Σ3), second order (Σ9) and

third order (Σ27). Such defects are present for both used substrates and also for different annealing temperatures. Figure 3.24 shows that alumina/SiO_2/Si and GC/SiN_x/Si samples contains almost the same distribution of crystallographic defects. This seems to indicate that the type of defects present in the grains does not depend on the substrate, while the grains size does. This result means that it is important to privilege the conditions that allow the fabrication of very large grains polysilicon films, namely here using the glass ceramic substrate.

In the following, we have investigated the effects of the annealing parameters (temperature, time) on the quality of the AIC layer formed on glass ceramic substrates, using the optimized conditions.

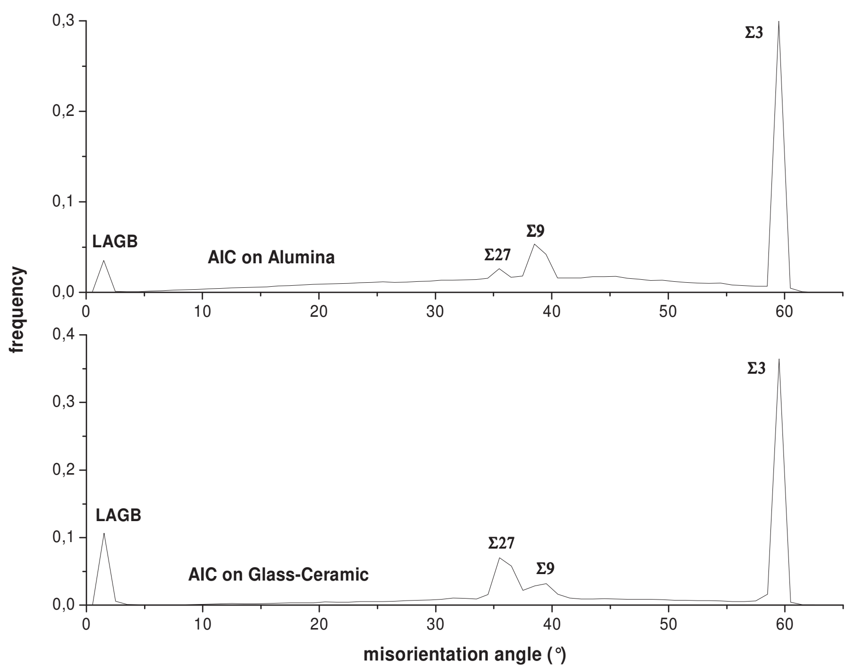


Figure 3.24: Distribution of misorientation angle for poly-Si formed by AIC on FOx-coated alumina and SiN_x-coated glass-ceramic substrates at 475°C.

To summarize, we have first identified alumina ceramic (Al_2O_3) and transparent glass-ceramic (GC) as substrates for this study due to the high temperature (≥1000°C) resistance and low thermal expansion coefficient values (TEC), which is quite compatible with silicon's processes. The bare alumina has a quite rough surface (*R*=5.6µm) while glass-ceramic is quite smooth (*R*=18.5nm). However, the surface roughness value of alumina is reduced to 0.16µm after flowable oxide spin coating (FOx-25). The smooth surface of glass-ceramic improves the crystal quality and favours an increase of the average grain size up to 25µm.

3.3.5 Effect of the Thermal Budget (Temperature and Time)

The annealing temperature and time being the crucial parameters of the Al/Si layers exchange process; we have investigated thoroughly their effect on the resulting polysilicon films. We have first studied the nucleation kinetics of silicon grains growth on glass-ceramic substrate under various annealing conditions. Mainly the crystallization includes two steps that are: i) nucleation of crystallites in the a-Si, and ii) crystallization of adjacent a-Si around initial nuclei up to touch each other to form a continuous layer [52]. Then, we present the optical and structural properties of the complete p-type polycrystalline silicon.

i) Nucleation kinetics during AIC

In order to study the growth kinetics of the Si grains on glass-ceramic substrate, Al/Si bilayer systems were annealed at 450°C, 475°C and 500°C for different times ranging from 5 to 300min. The samples were analyzed by optical microscopy after removing the top Al+Si layer formed on the poly-Si AIC film by means of mechanical polishing. The experimental definition of the crystallization and growth kinetics can be described through the analysis of the grains surface coverage and the density of the grains deduced from the optical microscope images. Figure 3.25 shows the optical micrographs of poly-Si films after annealing at 450°C/1h, 475°C/30min and 500°C/10min to compare the different nucleation rate while Figure 3.26 shows the time dependency of nucleation at the annealing temperature of 450°C for 1h, 2h and 3h. The black regions refer to the crystal silicon while white regions represent the remaining aluminium. The dentritic shape of the Si grains is observed for all annealing temperatures T and short times t. A crystallized fraction F_c, defined as the silicon surface area divided by the total area, can be deduced for each T/t couple.

Figure 3.27 plots the crystallized fraction (F_c) versus the crystallization time for different annealing temperatures of the Al/Si system. This figure shows that the low annealing temperatures slow down the crystallization process. About ~82% of the film was crystallized after 10min annealing for 500°C while it needs 30min at 475°C to reach the same crystallized fraction. Only 62% of the film can be crystallized after annealing at 450°C for 1h. These results show the dramatic decrease of nucleation rate when reducing the exchange annealing temperature from 500°C to 450°C.

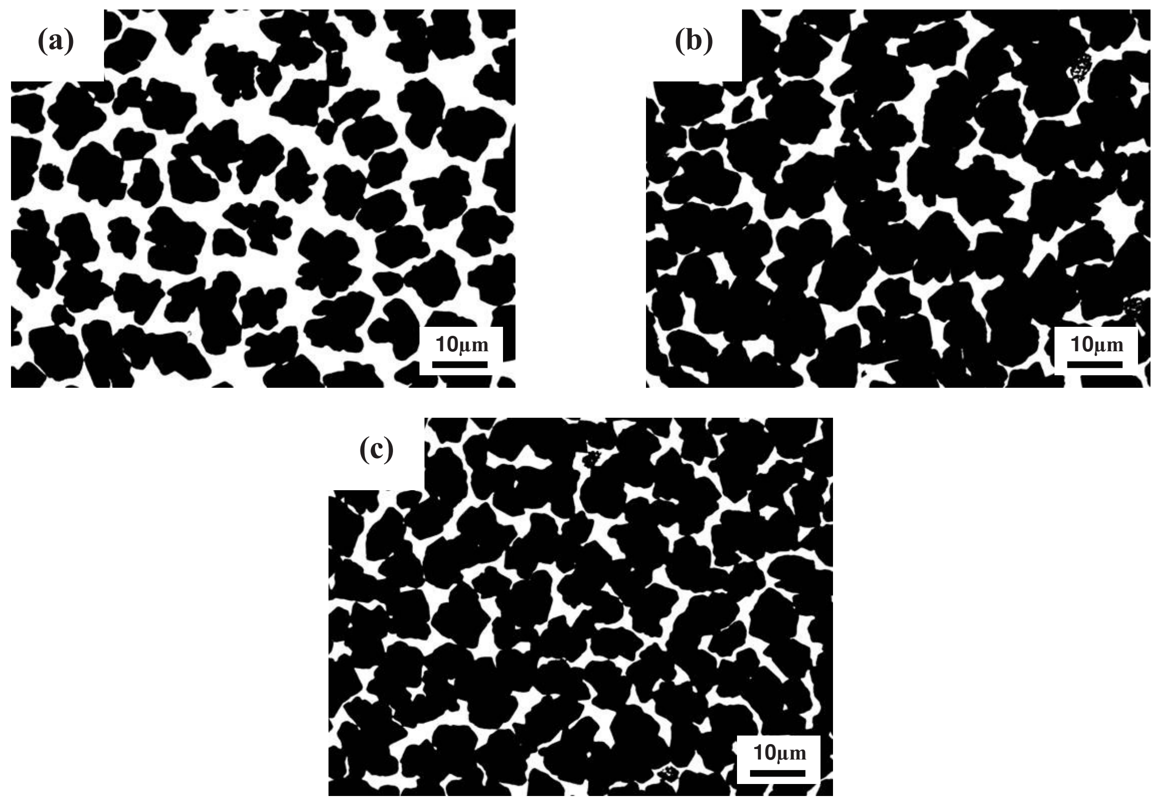


Figure 3.25: Optical microscope images of AIC poly-Si layer grown on glass-ceramic substrate after annealing at: (a) 450°C for 1h; (b) 475°C for 30min; and (c) 500°C for 10min.

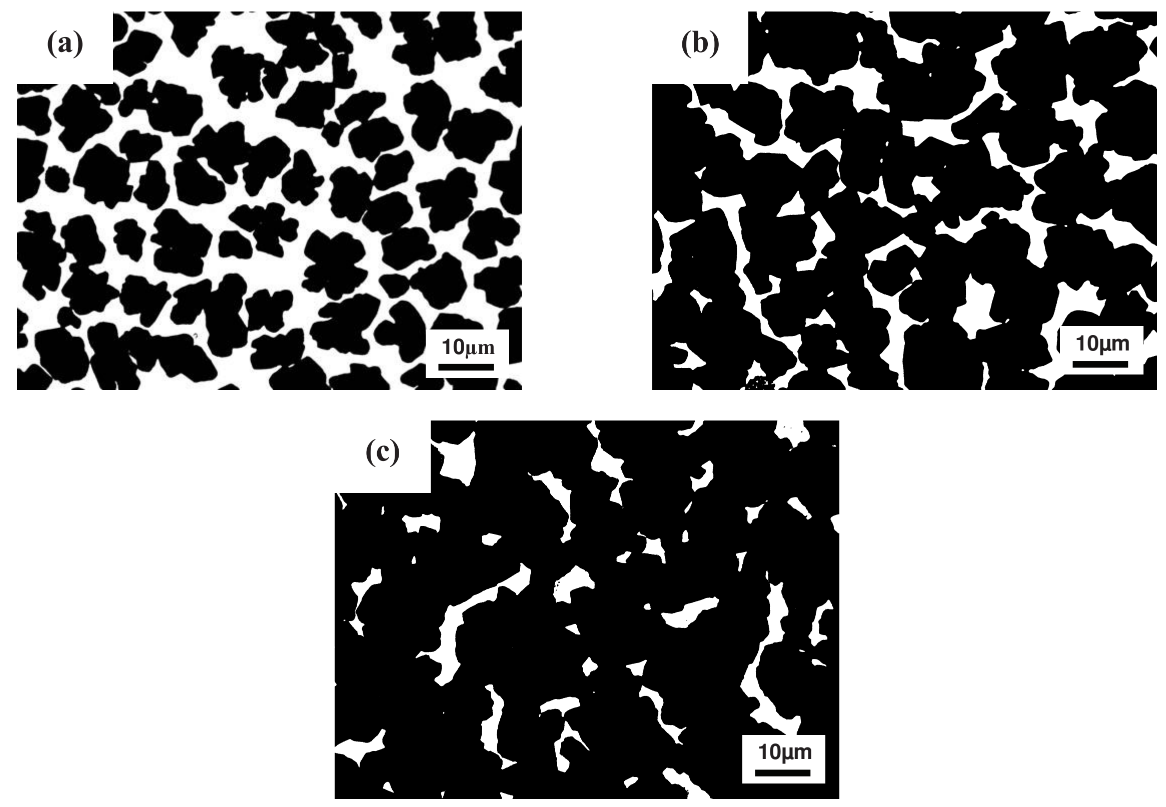


Figure 3.26: Optical microscope images of AIC poly-Si layer grown on glass-ceramic substrate after annealing at 450°C for: (a) 1h; (b) 2h; and (c) 3h.

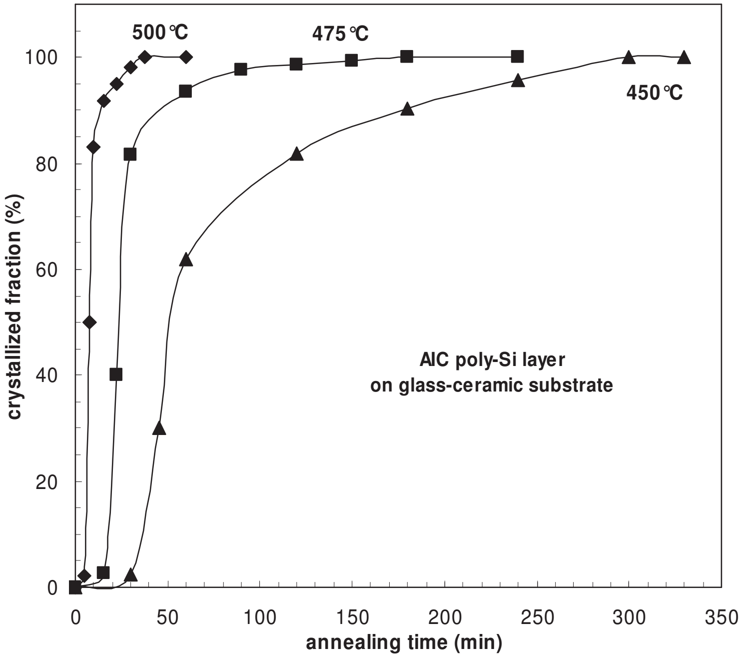


Figure 3.27: Crystallized fraction of polysilicon films formed at 450°C, 475°C and 500°C on glass-ceramic substrate as a function of annealing time.

The crystallization temperature and time strongly influences the nucleation kinetics: the increase slope of F_c is very fast (i.e. in shorter time) for higher process temperatures while it is smoother (i.e. the crystallization happens slowly) at lower temperatures. This observed behaviour at high temperatures can be correlated to the lower incubation time, which corresponds to the characteristic time needed for the formation of the first nuclei.

It can be noted that the kinetics of the nucleation during AIC can differ with respect to the used substrate. Indeed, the crystallization profile of a-Si by the AIC method has shown a different behaviour when using alumina ceramic substrates [53]. In particular the crystallized fraction for comparable annealing temperatures reaches 100% in a much shorter time for alumina compared to the glass-ceramic. This can be attributed to the thermal activation energy parameter expected to be different.

In order to determine the activation energy of the formation of the AIC polysilicon layer, data of Figure 3.27 are used to plot an Arrhenius graph for annealing times corresponding to crystallized fractions of 3% and 80%. The results are shown in Figure 3.28. An activation energy (E_a) of 1.7±0.1eV for F_c=80% is calculated for glass-ceramic over 450-500°C. It has to be compared to 1.44±0.03eV found for AIC on alumina [53]. In literature, the reported activation energy values are ranging between 1.2eV [54] and 1.8eV [55] depending on the Al/a-Si interface that controls the diffusion during the exchange process. Our activation

energy value of 1.7eV is fitting very well in this range. When this activation value is compared to that of solid phase crystallization (SPC) of a-Si, which is 3-4eV [56], there is a quite high difference that proves the different crystallization mechanisms of both techniques and explains the lower crystallization time of a-Si using AIC technique.

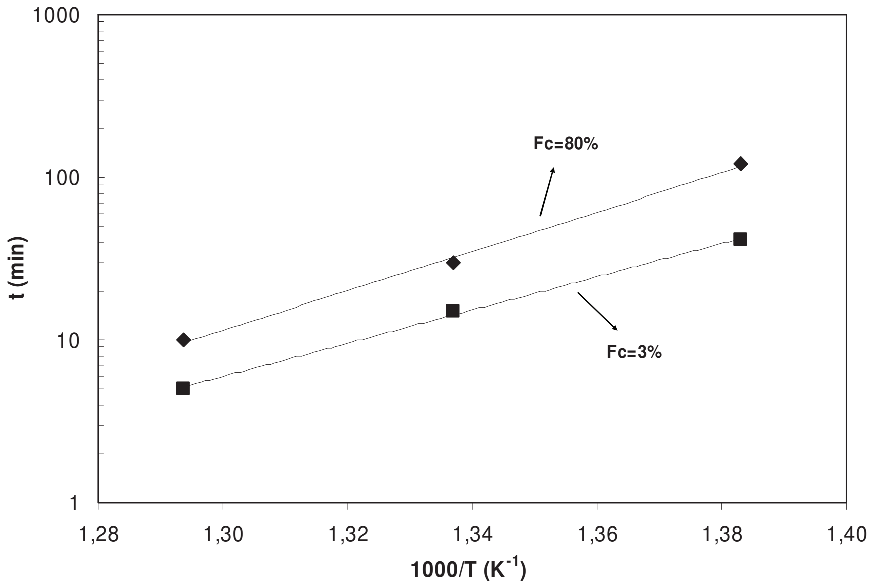


Figure 3.28: Arrhenius plot of temperature dependence of the time needed for 3% and 80% crystallization.

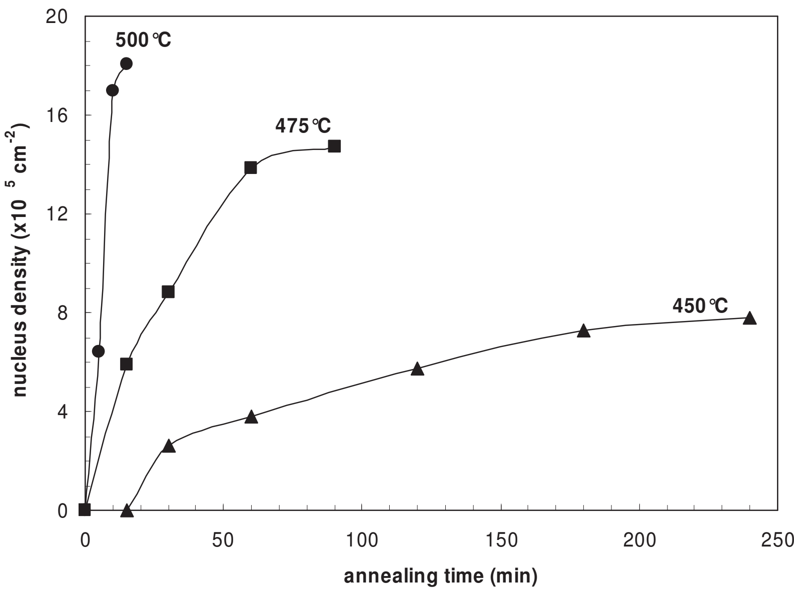


Figure 3.29: Nucleation density of polysilicon films formed at 450°C, 475°C and 500°C on glass-ceramic substrate as a function of annealing time.

Figure 3.29 plots the nucleus density as a function of annealing time for different temperatures. It can be noted that the nuclei density on glass-ceramic substrate decreases at lower temperatures, which led to the improved grain size. For longer annealing time, the Si crystals started to coalesce for all showed annealing conditions. Si nuclei grow inside the Al layer till touching each others. After some time, this gives rise to a continuous AIC poly-Si layer.

ii) Structural properties of continuous polysilicon films on glass-ceramics

Raman spectroscopy was used to evaluate the crystalline quality of the continuous silicon layers formed after complete exchange. Figure 3.30 compares the Raman spectra of poly-Si seed layers grown on glass-ceramic substrate at different exchange annealing temperatures. The spectra were normalized with respect to the LO/TO line of crystalline silicon at 520.1cm^{-1}. Very sharp and symmetrical peaks at 520cm^{-1} are observed for all annealing conditions. The peak position is similar to the Raman pattern of single crystalline silicon (sc-Si), which indicates that the polysilicon films are fully crystallized. It can be noted that the Raman peak at 480cm^{-1}, which is the signature of a-Si, is not observed. This also confirms the high rate crystallization of our poly-Si thin films after the exchange annealing conditions. Moreover, the peak positions being close to that of sc-Si (520.1cm^{-1}) represents that the films are under negligible stress. Additionally, the full width at half-maximum (FWHM) value of the Raman peak, which describes the crystalline quality for poly-Si films, depends on the exchange annealing temperature as shown in Figure 3.30. The FWHM value for 475°C/8h annealed sample is 5.9cm^{-1} proves once more the complete crystallization of the poly-Si seed layer as it is comparable to that of sc-Si. However, the FWHM value of 6.4cm^{-1} and 7.0cm^{-1} are obtained for 500°C/6h and 450°C/10h samples, respectively. These results show that crystalline quality of silicon on glass-ceramic substrate after annealing at 475°C for 8h is higher compared to those after 500°C/6h and 450°C/10h annealing.

Although Raman spectroscopy gives a preliminary indication for the good crystallographic quality of the poly-Si material, it is missing an in-depth crystallographic analysis. To do so, EBSD measurements were performed on poly-Si films formed by AIC on glass-ceramic substrate at different thermal budgets in order to deduce the grains orientation mapping, the defects type and density, the grain boundaries and the morphology. We have analyzed poly-Si seed layers on GC substrates prepared at 500°C/6h and 475°C/8h in a conventional furnace. In order to obtain a flat surface, the standard polishing procedure for surface preparation was performed prior to EBSD analysis.

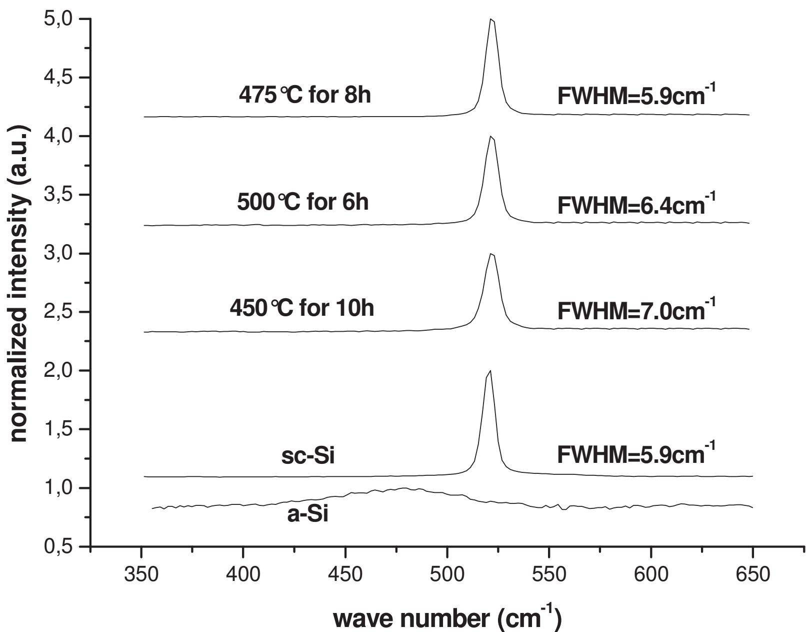


Figure 3.30: Raman spectra of poly-Si thin films formed on glass-ceramic after annealing at 450°C, 475°C and 500°C. The Raman spectra of sc-Si and a-Si are shown as a reference.

Typical surface normal direction orientation maps for these poly-Si seed layers obtained from EBSD technique are shown in Figure 3.31a and 3.31b. The samples area shown in the figures are 500×450μm^2, with a mapping step of 0.5μm. Each color in this orientation map indicates the specific crystallographic direction, and the standard color triangle that shows a prominent three dimensional texture is shown in inset of each figure. EBSD map can easily supply grain orientation related texture by examining the grains whose similar crystal orientations are shown in similar colors. Looking carefully to the mapping revealed a graded color within the grains than means a deviation from the main orientation.

To be quantitative, the distribution of analyzed pixels as a function of deviation angle θ is plotted in Figure 3.32. The deviation is accumulated by segments of 5° compared to the <100> orientation. In this graph, the minimum deviation (5°) means a fully <100> oriented layer while the maximum deviation of 54.7° corresponds to the <111> plane. The majority of grains (60-70%) in these poly-Si films has an orientation deviation between 5° and 25° relative to <100> orientation. The occurrence of <100> orientation is higher for 475°C/8h annealed sample than for 500°C/6h annealed sample as deduced from EBSD orientation map. The <110> oriented silicon is indicated by deviation angles in the range of 30-45° while that is in the range on 45-55° for <111> orientated silicon. Both <101> and <111> show lower distribution for when compared to <100> orientation. In fact 71% of the total surface was covered by <100> oriented grains for 475°C/8h annealed sample while the surface coverage

of <101> and <111> oriented grains is only 16% and 13%, respectively. The surface fractions of <100>, <101> and <111> are 62%, 23% and 15%, respectively, when considering 500°C/6h annealed poly-Si film.

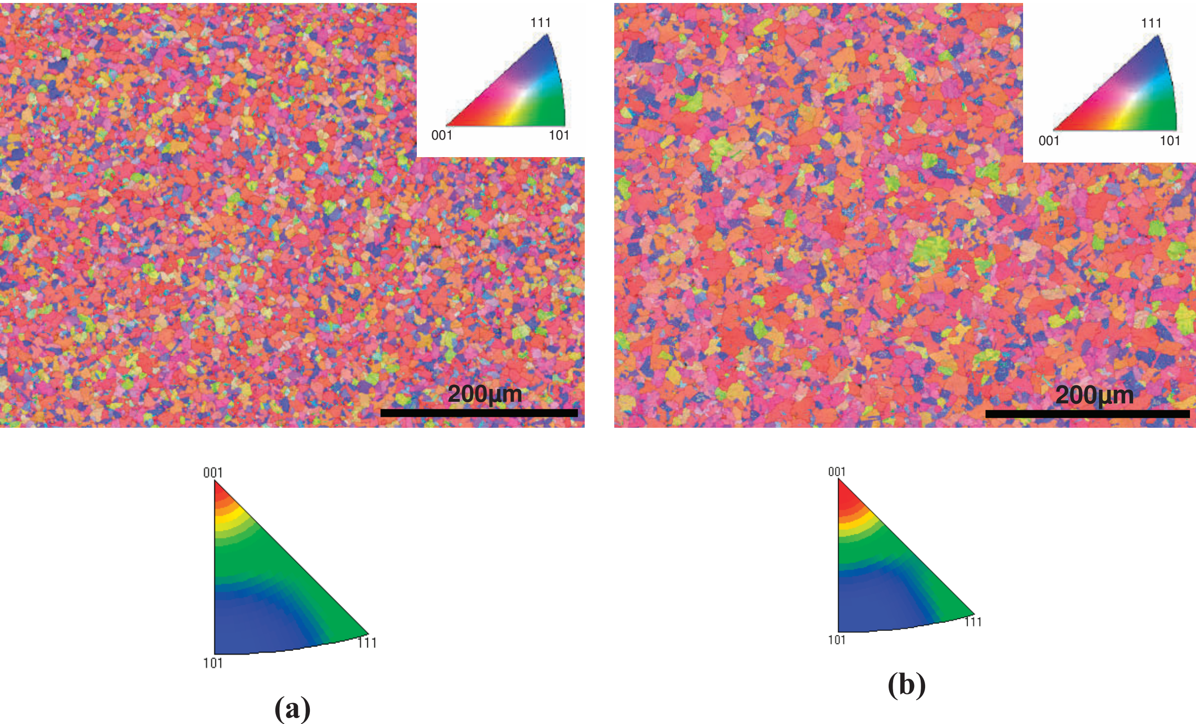


Figure 3.31: EBSD orientation mappings and the inverse pole figures in the sample normal direction for poly-Si films prepared at: (a) 500°C/6h, and (b) 475°C/8h.

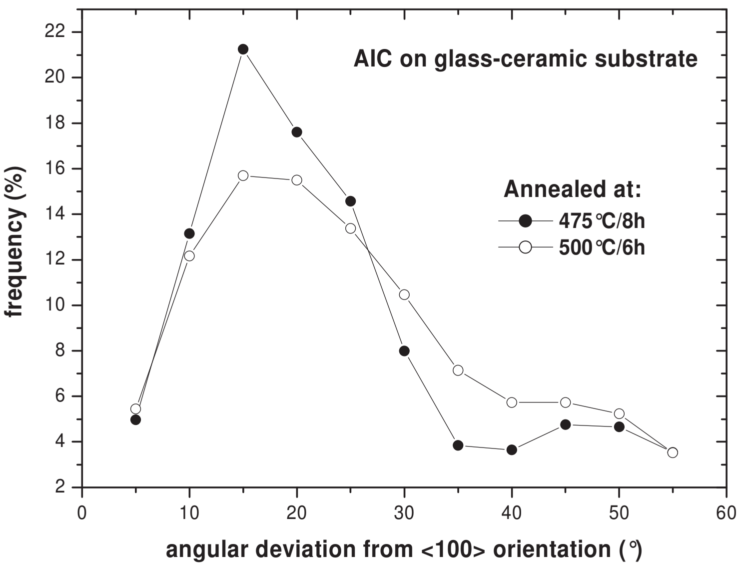


Figure 3.32: The deviation angle from <100> fiber texture of the poly-Si film formed on glass-ceramic by AIC at different temperatures

The present results say that <100> is the preferential orientation of the grains for both types of samples. No twins are observed for the <100> oriented grains, whereas the other orientations present a large density of twins. The reason for this behaviour is attributed to the orientation of the initial nucleus close to the <100> plane [27].

The influence of the various annealing conditions on the grain size of polycrystalline silicon thin films was also studied using the EBSD technique conditioned by two different criteria on grain boundary definition. These criteria consider excluding (criterion 1) and including (criterion 2) the twins. The average grain size for different exchange annealing depending on the criteria is listed in Table 3.7. When considering criterion 1, it can be noticed that the average grain size (D_g) reaches up to 12µm and 26µm for 500°C and 475°C annealing, respectively. The grain size distributions for 475°C/8h and 500°C/6h annealed samples are shown in Figure 3.33 based on criterion 1.

Annealing conditions	*Average grain size* (µm)	
	including Σ3	excluding Σ3
475°C/8h	16	26
500°C/6h	8	12

Tablo 3.7: Average grain sizes as a function of annealing temperatures by including and excluding the Σ3 twin boundary.

The low annealing temperature results in much larger grain size. The root mean square deviation (σ) of grain size distribution peaks are 3.6µm and 5.9µm for 500°C/6h and 475°C/8h samples, respectively. Such shape of distribution means that the process is diffusion controlled for 500°C/6h and 475°C/8h annealed samples instead of interface controlled [51]. The grain size distribution becomes less homogenous (σ=5.9µm) for 475°C/8h sample while the grain size is larger. Such a distribution is expected if the nucleation and growth rates are constant [27,51]. Let's consider the average grain size under criterion 2. The average grain size is 8µm and 16µm for 500°C/6h and 475°C/8h annealing, respectively. Although the reduction of grain size by including the twins is observed, the temperature dependent behaviour of grain sizes is the same for criterion 2.

The difference in the average grain size can be attributed to the growth morphology of the crystals which depends on the annealing temperature. A correlation between the exchange annealing temperature and the grain size can be found: lower the annealing temperature,

larger the grain size. Furthermore, the results can be concluded as follows: the grain size increases when the nucleation rate decreases by reducing the annealing temperature.

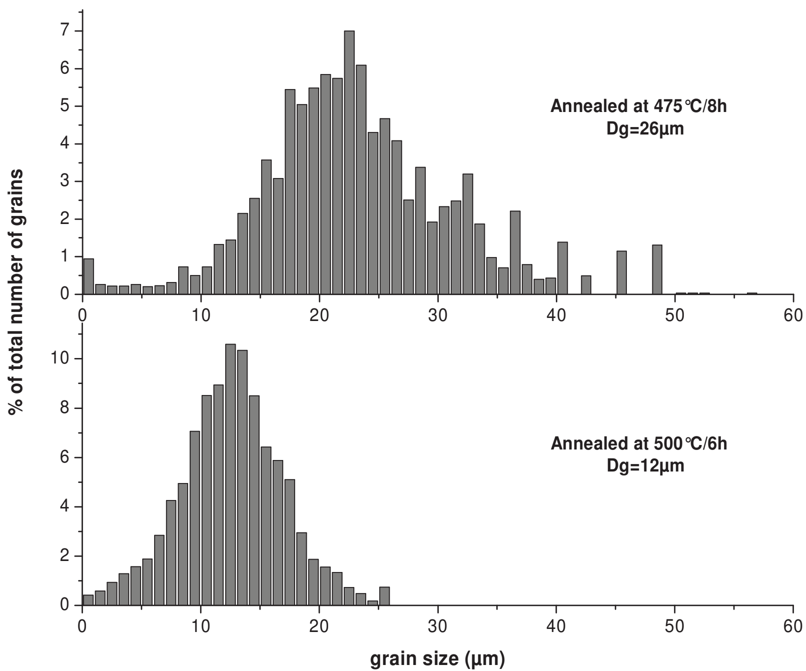


Figure 3.33: Grain size distribution of the poly-Si thin films prepared at 475°C and 500°C by considering criteria 1.

The identification of crystallographic defects and their respective density are essential in view of improving the crystalline quality of the films. We have used the EBSD data to identify the inter- and intra-grain defects in the grown AIC polysilicon films on GC substrates. For the studied polysilicon samples, low-angle grain boundaries (LAGB) (angle<2°) and coincident site lattice (CSL) boundaries consisting of twin boundaries of first order (Σ3), second order (Σ9) and third order (Σ27) are found in the continuous poly-Si films. More quantitatively, the AIC layers formed at 475°C for 8h contains about 38.6% of Σ3 twin boundaries, lower than that found in the 500°C/6h annealed sample (46.5%). The density of twin Σ9 (~5%) and Σ27 (~2%) boundaries are almost the same for both annealing cases and slightly higher (~5% for Σ9 boundary and ~2% for Σ27 boundary) when compared to Σ3 twin boundary. Thus, larger are the grains, less defective they are. It is clearly set that the AIC layer on GC formed at 475°C/8h has optimal structural properties in terms of grains size and defects.

To summarize the results of this study, we have shown that the nucleation kinetics on glass-ceramic (GC) substrate differs from that of on alumina due to the higher activation energy (1.7eV) that causes slower nucleation rate for glass-ceramic compared to alumina used process. From the crystallized fraction data versus the exchange annealing temperature, we have found that the crystallization is smoother for low-temperature processes. This can be correlated to the lower incubation time for higher temperatures. It can be noted that the nucleus density on glass-ceramic substrate decreases at lower temperatures whereas the grain size increases. The decrease of temperature from 500°C to 475°C increases the average grain size from 12μm to 26μm.

3.3.6 Electrical properties of the AIC polysilicon layer on glass ceramics

i) Hall Effect system

The investigation of the electrical parameters is an important task to monitor the structural quality of the film, especially when aiming at solar cell fabrication on those materials. In order to determine the main electrical properties Hall Effect measurements were performed at room temperature. The resistivity and Hall Effect mobility of polysilicon can vary over several orders of magnitude depending on its doping concentration. The Hall Effect measurements were done in van der Pauw geometry (Figure 3.34).

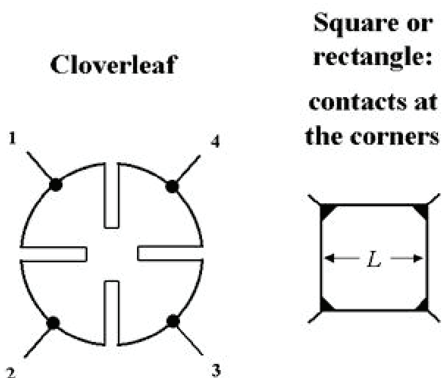


Figure 3.34: Some possible contact placements for Van der Pauw method.

According to van der Pauw method, the resistivity is given by [57]:

$$\rho = \frac{\pi t}{\ln 2} \frac{R_{12,34} + R_{23,41}}{2} F(Q) \tag{3.9}$$

where t is the thickness of the sample, $F(Q)$ is the geometric correction factor. The $R_{12,34}$ (or $R_{23,41}$) is the resistance. To make a measurement, a current flows along one edge of the sample

(for instance, I_{12}) and the voltage across the opposite edge (in this case, V_{34}) is measured. From these two values, a resistance (for this example, $R_{12,34}$) can be found using Ohm's law:

$$R_{12,34} = \frac{V_{34}}{I_{12}} \tag{3.10}$$

The Hall mobility can be determined by measuring the change of the resistance $R_{24,13}$ when a magnetic field is applied perpendicular to the sample. The Hall mobility is given by [58]:

$$\mu_H = \frac{d}{B}\frac{\Delta R_{24,13}}{\ell} \tag{3.11}$$

where B is the magnetic induction, $\Delta R_{24,13}$ is the change of the resistance $R_{24,13}$ due to magnetic field, and ℓ is the specific resistance of the material.

In our Hall Effect system, the measurements were performed at room temperature, and used a fixed magnetic field of 0.570T and an applied current at 1.0mA.

ii) Hall measurement on AIC approach

The p-type poly-Si seed layers were formed at 475°C on glass-ceramic substrate. The electrical parameters are listed in Table 3.8. As a result, resistivity (ρ), hole concentration (p) and Hall mobility μ_H of p-type film were 84.0mΩ.cm, 1.19×10^{18}cm^{-3} and 62.5cm^2/Vs, respectively. It can be indicated that mobility value for p-type film is comparable to those reported in literature [20,59] for polysilicon with similar grain structure.

Due to the temperature limitations in the fabrication of poly-Si seed layers, point-like and extended defects can be present in the films typically prepared by thermal crystallization of amorphous Si [60]. These defects provide recombination centres in the band gap, drastically reducing the minority carrier lifetime within the device. As such, the removal of these defects is mandatory and typically done via thermal annealing. This treatment can result in a significant improvement of the initial poly-Si films [61]. High-temperature annealing is traditionally done in roller or belt furnaces or in tube furnaces. Thermal annealing has been established since several years as an efficient annealing technology providing well controlled thermal budgets and a fast processing. These two properties are excellently fulfilling the requirements for an optimal defect annealing of poly-Si thin-films on glass substrates and its application in the production of Si based thin-film photovoltaic devices [62].

We have carried out a study on the effect thermal annealing in a tube furnace of our as grow AIC poly-Si films (see Table 3.8). We have measured the resistivity, the hole concentration and the Hall mobility before and after thermal annealing. We did not observe a significant difference between post-annealed and non-annealed samples. There is only a nominal enhancement in the mobility of the order of 2cm^2/Vs. This results show that the AIC films are quite stable since no degradation in the electrical parameters are detected. It also says that no improvement can be expected with a post-thermal treatment, even at high temperature.

Annealing condition	Resistivity (mΩ.cm)	Hole concentration (cm^{-3})	Hall mobility (cm^2/Vs)
Without annealing	84.0	1.19×10^{18}	62.5
900°C/15min	83.1	1.18×10^{18}	64.6

Tablo 3.8: Effects of post annealing on the electrical parameters of AIC seed layer.

3.4 FORMATION OF N-TYPE POLYCRYSTALLINE SILICON

The polycrystalline silicon films formed by AIC method are intrinsically p$^+$-type silicon materials, thanks to aluminium dopant. Indeed, p$^+$-type AIC poly-Si film is formed directly due to the presence of Al in poly-Si layer and serves as a back surface field with a carrier concentration of ~2x10^{18}cm^{-3}. In this case, the solar cell configuration could be a p$^+$pn$^+$ configuration. However, in Chapter 2, we have shown that n-type polycrystalline silicon based solar cells might provide better photovoltaic performances than p-type cells. The n-type cell can be ideal when considering its advantages such as higher diffusion length and lifetime, as well as better tolerance to defects than those of p-type. Besides, the recombination can be controlled by means of a preferential doping along the defects. Furthermore, a serious efficiency limitation is observed in solar cells made of boron-doped p-type silicon. The performances of the solar cells degrade by exposure to light. It could be attributed to the formation of boron–oxygen complex, which is highly recombination active [63]. For these various reasons, researches and developments of solar cells based on n-type Si single-crystalline and multi-crystalline silicon wafers are of interest for the last 10 years. A few works concerned to n-type polycrystalline materials and none on n-type doping of AIC layers. The following paragraphs will deal with our method of fabricating n-type polysilicon layers

and giving their electrical properties. We will first remind the basics for impurities diffusion in polycrystalline materials.

3.4.1 Ex-situ doping of polycrystalline silicon

Let's starts this paragraph with considerations about the diffusivity of dopants in polycrystalline silicon materials. The polycrystalline material is considered to be composed of single crystallites with various sizes that are separated by grain boundaries. Experimental results indicate that the impurity atoms inside each crystallite have diffusivities comparable to that found in the single crystal. Impurity atoms also diffuse along grain boundaries, so the diffusivity in a polysilicon film depends strongly on the crystallography of the film. Figure 3.35 illustrates this phenomenon of preferential doping diffusion along the grain boundaries. In this figure, we can notice that the preferential diffusion of dopants along the grain boundaries reduces the electrical activity of the grain boundaries. So, it has an effect of passivation of defects localized in the grain boundaries.

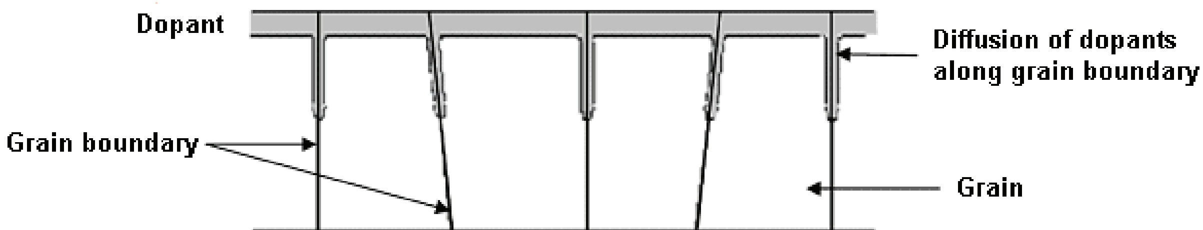


Figure 3.35: Preferential diffusion of dopants along the grain boundaries.

Impurity diffusion in polysilicon film can be explained qualitatively by a grain boundary diffusion model introduced by Fisher in 1951 [64]. This model assumes that the grain boundary can be modelled as a two-dimensional region between two-region representative semi-infinite grains. However, the diffusion coefficient at the grain boundary (D_{gb}) is considered very high when compared with that of grain (D). The diffusivity of impurity atoms that diffuse along grain boundaries can be about 100 times larger than the diffusivities in a single-crystal lattice. Experimental results indicate that the impurity atoms inside each crystallite have diffusivities comparable to that found in the sc-Si. Impurity atoms diffuse along grain boundaries as shown in Figure 3.35, so the diffusivity in a polysilicon film depends strongly on the texture of the film.

Experimental profiles in polysilicon films resemble simple diffusion result such as a complementary error function or a Gaussian function, which depends on the applicable

diffusion conditions. Because of this resemblance, the diffusivities can be estimated from the measured junction depth and the surface concentration using

$$C(x,t) = C_s erfc\left(\frac{x}{2\sqrt{Dt}}\right) \tag{3.12}$$

or

$$C(x,t) = \frac{S}{\sqrt{\pi Dt}} \exp\left(-\frac{x^2}{4Dt}\right) \tag{3.13}$$

where C_s is the constant surface concentration (in atom/cm^3), D is the constant diffusion coefficient (in cm^2/s), x is the distance coordinate (in cm), with x=0 at the silicon surface, t is the diffusion time (in s), *erfc* is the complementary error function, and S is the unit area. The solution of diffusion equation is Equation 3.12 for diffusion profile as complementary error function, while Equation 3.13 is used for diffusion profile with Gaussian distribution.

Physically, the diffusion coefficient interprets the speed of dopant diffusion; and it depends on the temperature and the species being diffused. According to the Arrhenius' law, the diffusion coefficient can be expressed in the form of:

$$D = D_0 \exp\left(-\frac{E_a}{k_B T}\right) \tag{3.14}$$

where E_a is the activation energy of the mass transport and T is the temperature of diffusion. Table 3.9 gives the values of the activation energy E_a and the diffusion coefficient D_0 used in the single-crystalline silicon technology.

An asymptotic solution was obtained by Le Claire for an insulated grain boundary constitute. The initial point of this analytical study is the diffusion of phosphorus in polycrystalline silicon. However, polycrystalline silicon consists of consecutive grains separated by grain boundaries. Therefore, a complete analytical study should be done for all grains and grain boundaries in terms of the kinetics of diffusion dopants in polycrystalline silicon. According to Harrison [65], there are three main types of dopant diffusion kinetics in polycrystalline silicon as represented in Figure 3.36. In this figure, d refers to grain size.

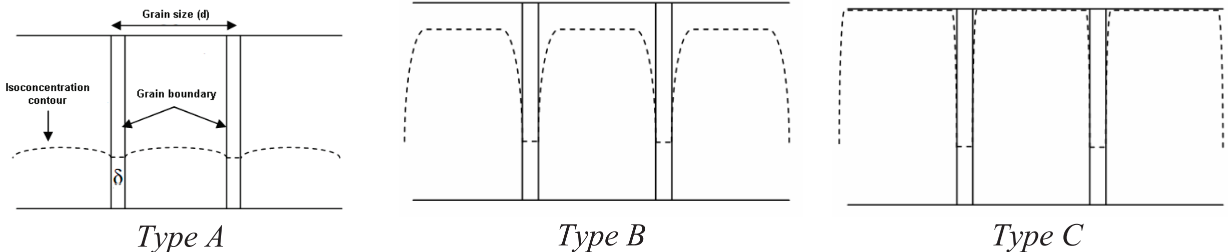


Figure 3.36: Different types (A, B and C) of phosphorus diffusion in poly-Si.

Type A: The diffusion of phosphorus in polycrystalline silicon is long time diffusion process and small grain sizes ($\sqrt{Dt} >> d$ or $D_{gb} \approx D$). However, the lateral diffusion in the grain from adjacent grain boundaries is important and leads to a high concentration of dopants in the grain.

Type B: This type is often encountered in practice and it is characterized by low lateral diffusion since the grain boundary compared to the volume diffusion of the grain boundary ($100\delta < \sqrt{Dt} < d/20$).

Type C: This type of distribution occurs when the diffusion time is very short or when D is negligible compared to D_{gb}. The diffusion only takes place along the grain boundaries and the concentration inside the grains is negligible.

In practice, the type B is the most common for the phosphorus diffusion in polycrystalline silicon for normal conditions of thermal annealing [66]. Moreover, many authors have attempted to develop a qualitative model for diffusion behaviour of phosphorus in the grain boundary from diffusion depths and intra-grain doping concentrations. However, the major problem remains the choice of diffusion coefficients that depend on the experimental conditions of diffusion. Thereby Ornaghi [67] chose the expressions reported in [68] and [69] in order to show variations in the depth of diffusion in grain and along grain boundary as a function of diffusion time and temperature. In this case, the equations for diffusion coefficients of phosphorus in grain (D) and along grain boundary (D_{gb}) can be expressed as following, using Equation 3.14:

$$D = 8\times10^{-3}\exp\left(-\frac{2.88eV}{k_B T}\right) \quad (cm^2 s^{-1})$$

$$D_{gb} = 4\times10^{-3}\exp\left(-\frac{1.71eV}{k_B T}\right) \quad (cm^2 s^{-1}) \qquad (3.15)$$

Table 3.9 gives most common diffusities of As, B and P in polysilicon films. Two values are given due to the effects of polysilicon textures, diffusion temperature or other factors.

Element	D_0 (cm^2/s)	E_a (eV)	D (cm^2/s)	T (°C)	*Ref.*
As	8.6×10^{4}	3.9	2.4×10^{-14}	800	[70]
As	0.63	3.2	3.2×10^{-14}	950	[71]
B	$(1.5\text{-}6)\times10^{-3}$	2.4-2.5	9×10^{-14}	900	[72]
B			4×10^{-14}	925	[73]
P			6.9×10^{-13}	1000	[74]
P			7×10^{-13}	1000	[74]

Tablo 3.9: Examples of diffusivities in polycrystalline silicon films.

To check how far the phosphorus will diffuse in our 200nm thick AIC layer, we have calculated the diffusion depth, using $L=\sqrt{Dt}$, for various diffusion temperatures, using Equations 3.15. Figure 3.37 plots the diffusion depth values along grain boundary and in grain as a function of temperature (800-1100°C) and diffusion time (1-4h).

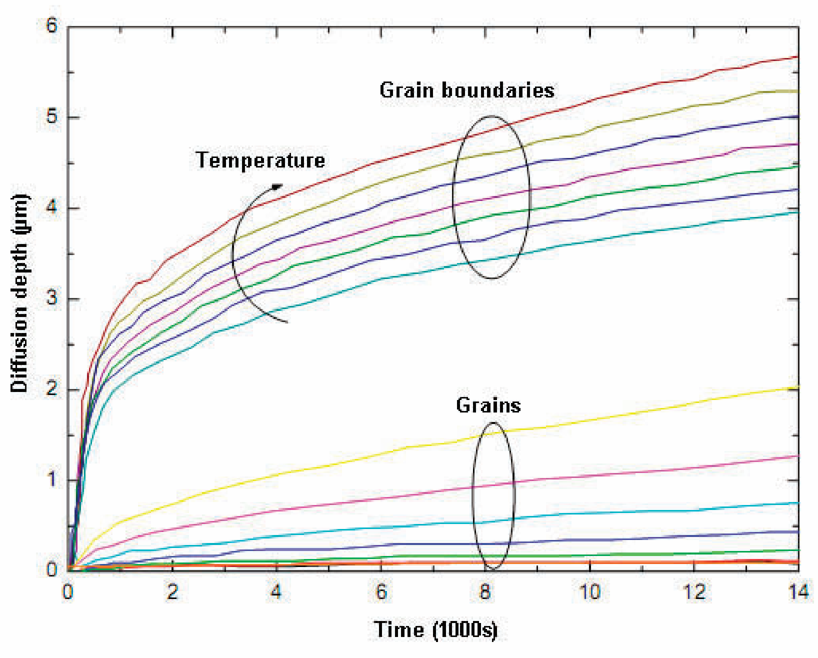


Figure 3.37: Variation of the diffusion depths of phosphorus along the grain boundary and in the grain as a function of diffusion time and temperature between 800°C and 1100°C [75]. The bottom curve corresponds to the lowest diffusion temperature.

The value of *D* ranged from about 10^{-16} to $10^{-13}cm^2s^{-1}$ at the temperature range of 800-1100°C, while the value of D_b varied from a minimum of 10^{-11} to maximum of $10^{-9}cm^2s^{-1}$. As expected, the phosphorus diffuses more deeply in grain boundaries than in grains.

The complete transformation of our p-type AIC polysilicon layer into n-type material assumes that the phosphorus diffusion occurs in the entire 200nm thick polysilicon layer. The data of Figure 3.37 were used to choose the appropriate temperature and time to insure the overall doping.

3.4.2 Formation of N-type Si by Phosphorus Doping of AIC Seed Layer

We have investigated the possibility of the formation of n-type polycrystalline silicon by direct doping of the p-type AIC layer from a solid doping source. We have studied the thermal diffusion of phosphorus in p-type seed polysilicon from a spin-on dopant (SOD) solution containing a high concentration of phosphorus atoms. The phosphorus distribution in the polysilicon film depends primarily on the surface concentration (source doping), the annealing temperature and time for diffusion.

In the semiconductor industry, the spin on glass (SOG), which is basically a SiO_2 after baking, has been widely used as a diffusion source or a planarizing dielectric for multilevel metallisation schemes in the fabrication of nowadays integrated circuits. SOGs are in general Si-O network polymers in organic solvents, and prepared through the hydrolysis-condensation reaction that implied the sol-gel technology. Films are normally formed from SOG sols using the spinning technique.

SOG materials when containing dopants (e.g. boron or phosphorus) are also used as diffusion sources in semiconductor technology. In this case the Spin On Glass (SOG) is called a Spin-On Dopant (SOD). The diffusion process uses the liquid doped sources and it has been applied since the seventies but recently SOD has become more popular in IC processing. Indeed, there are several advantages of the SOD diffusion technique: i) no implantation defects, thus no transient-enhanced diffusion and very shallow junctions could be obtained, ii) uniform and consistent doping with high yield, iii) elimination of use of toxic gases, iv) no storage of source wafers or use of costly ion implant equipment, and v) application for both planar and 3-D structures [76].

There are several techniques which use SOD as a diffusion source: one-step diffusion, two-step diffusion and proximity diffusion. The technique we have used is the one-step diffusion. Phosphorus-SOD solutions containing different content of phosphorus were used to

form the n^+ type AIC poly-Si film. The P-SOD solutions, provided by Filmtronics Ltd, are named P50x, where x (=5, 7, 8 or 9) correspond to a concentration of phosphorus in the starting solution (see Table 3.10).

P spin-on dopant	*P505*	*P507*	*P508*	*P509*
Dopant concentration (cm^{-3})	4.5×10^{19}	5.0×10^{20}	1.5×10^{21}	2.0×10^{21}

Tablo 3.10: The different phosphorus doped spin-on glass (SOD) solutions purchased from Filmtronics Ltd., and used as dopant source of the AIC layers.

The experimental procedure for overdoping or compensation the AIC layers is the following:

The p^+ poly-Si sample produced by AIC is placed on the spinner and the SOD is dropped on the centre of the wafer. Required SOD for a $5\times5cm^2$ sized sample is 1000µl. The rotation speed was 3000rpm (rotation per min) and the acceleration was 5000rpm/s for 2s. The films coated with P50x were baked in an oven at 80°C for 5min and 200°C for 10min for SOD densification and solvent evaporation. During the low-temperature baking, polymer cross linking takes place and a porous SOD structure was formed due to the solvent evaporation in the SOD layer. Thereafter the wafers were annealed in a conventional furnace at various high temperatures to diffuse impurities from the SOD source into the polycrystalline Si film. For conventional furnace diffusion, the chosen thermal budgets were 800°C, 900°C and 1000°C for 1h. According to these chosen annealing conditions and Equation 3.15, the diffusion depth of phosphorus in grain is 0.01µm, 0.04µm and 0.13µm while the diffusion depth along the grain boundary is 4.5µm, 9.9µm and 19.2µm for diffusion annealing at 800°C, 900°C and 1000°C for 90min, respectively. This overdoping process flow is illustrated in Figure 3.38. After thermal diffusion, the residual phosphorus was removed by a chemical solution, HF(5%):DI-H_2O (10:100).

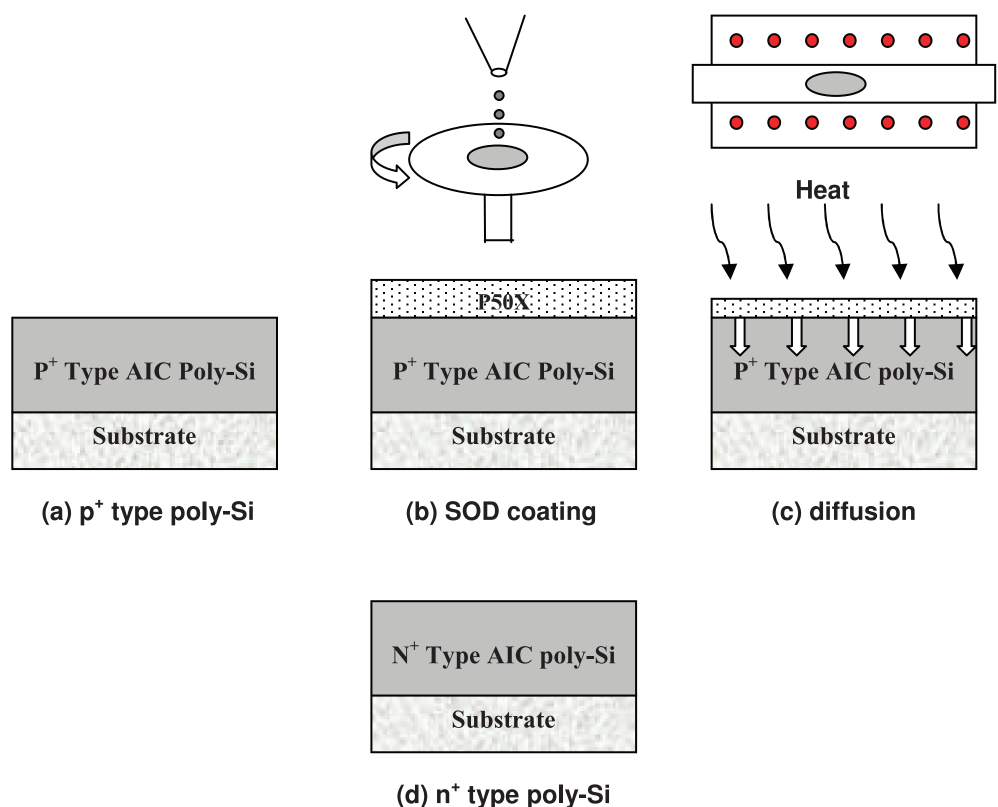


Figure 3.38: Process flow of n^+ type poly-Si film formation

To check the overdoping efficiency, the resistivity and carriers mobility were measured by means of Hall Effect measurement system while the four-point probe technique was used to determine the sheet resistance.

3.4.3 Electrical Properties of the N-type AIC Layers

The overdoping of the AIC poly-Si was first analyzed by the four-point probe method. As shown in Table 3.11, the sheet resistance values are reduced from 2700Ω/sq for the AIC layer down to 19.6Ω/sq after phosphorus diffusion at 950°C for 1h. We have checked the change in doping type using a copper probe connected to a galvanometer. This result shows that it is possible to efficiently convert a thin p-type polysilicon layer into a highly doped n-type poly-Si thanks to the phosphorus diffusion at high temperature. Taking into account the diffusion coefficient of phosphorus at 950°C in silicon, the thermal process time corresponds to a diffusion length of P into Si of 11.4µm, which is much larger than the AIC layer thickness. Considering the sheet resistance value of 19.6Ω/sq and the n^+-type seed layer thickness of 200nm, this corresponds to a resistivity of the n^+-type layer of about 4×10^{-4}Ω.cm, and therefore, to a carrier concentration of about $4\text{-}5\times10^{20}cm^{-3}$.

Thickness of AIC layer (nm)	R□, before P diffusion before epitaxy (Ω/sq)	Diffusion temperature of P to AIC layer (°C)	R□, after P diffusion (Ω/sq)
200±15	2700±100	900	21.3±2
		950	19.6±2
		1000	18.9±2

Tablo 3.11: An overview of sheet resistance (R□) values for various conditions of poly-Si.

The main electrical properties, such as resistivity (ρ), electron concentration (*n*) and Hall mobility (μ_H), of the n-type polycrystalline silicon layers formed at 475°C on glass-ceramic substrate were performed by Hall Effect measurements at room temperature. The resistivity and Hall Effect measurements of polysilicon can vary over several orders of magnitude depending on its doping concentration.

Figure 3.39 plots the measured resistivity as a function of the temperature of phosphorus diffusion. Two regions are clearly observed: in the range, 800-900°C the resistivity (ρ) rapidly decreases, and above 900°C it reaches a plateau: the resistivity value is almost the same for the P507, P508 and P509 used solutions. For instance, the resistivity of the P507 (5.0×10^{20} P/cm^3 in the solution) doped polysilicon layer decreases from 7.5mΩ.cm at 800°C diffusion temperature to 0.5mΩ.cm at 1000°C diffusion temperature.

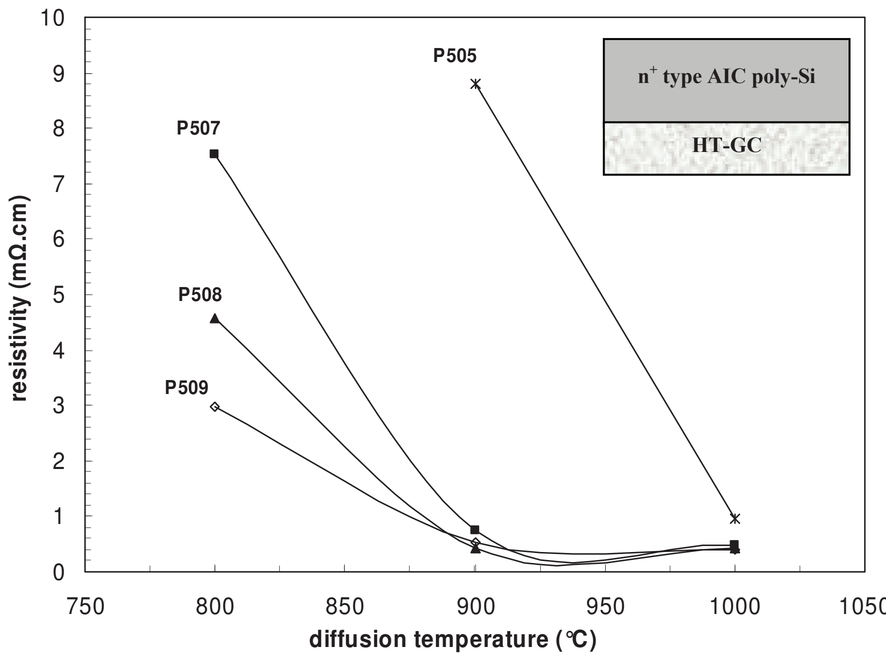


Figure 3.39: Effect of diffusion temperature and phosphorus concentration on resistivity.

For the low doped solution (P505), a diffusion temperature of 1000°C is needed to reach the resistivity value obtained at 900°C for highly doped solutions. The resitivity values can be converted into carriers concentrations, thanks to the Hall Effect system. The results are given in Figure 3.40.

The decrease of resistivity and the corresponding increase in the carrier's concentration with increasing the diffusion temperature are due to the incorporation and electrical activation of the phosphorus atoms in the polysilicon AIC layers. Higher phosphorus concentration in the dopant source solution results in a more efficient activation. The phosphorus diffuses into the grains as well in the grain boundaries and twins.

Polysilicon contains many grain boundaries and defects. These defects trap majority carriers (negatively charged electrons e^- in n-type Si), and due to the ionized intragrain dopant atoms (positively charged donors in n-type Si) a potential barrier is developed across the grain boundaries. This potential barrier Φ_b results in a higher resistivity and a lower mobility for majority carriers. It should be noted that the effect of doping concentration and trap density is to vary the barrier height Φ_b. Furthermore, minority carriers (positively charged holes h^+ in n-type Si) recombine at the defect levels with trapped majority carrier. However, the phosphorus doping of the sample results in a lower resistivity due to the smaller potential energy barriers at the grain boundaries. This explains the resistivity of phosphorus doped poly-Si layers can be determined by temperature dependent resistivity measurements. Additionally, the behaviour of the resistivity with temperature changes when the different phosphorus sources with different concentrations (C_{P505}=4.5×10^{19}cm^{-3}, C_{P507}=5.0×10^{20}cm^{-3}, C_{P508}=1.5×10^{21}cm^{-3}, C_{P509}=2.0×10^{21}cm^{-3}).

It should be mentioned that phosphorus doping of the layers is usually accompanied by a high-temperature anneal, which increases the thermal conductivity. The decrease in resistivity can be attributed to the higher amount of the filling of traps along the grain boundaries by increasing the phosphorus concentration. Additionally, the adsorption of phosphorus with in the grain boundary, acting to annihilate acceptor grain boundary states, increase grain size can be the effects of lower resistivity observed for higher temperatures. Poly-Si films doped at 1000°C are reported to have minimum resistivities approximately 4×10^{-4}Ω.cm. Kamins and Marcoux [77] reports a lower limiting resistivity for phosphorus (4×10^{-4}Ω.cm) for ion-implanted films that were subsequently annealed at 1000°C. It is thought that the number of electrically active phosphorus donors saturates at 2×10^{20}cm^{-3}. Moreover, solid solubility is thought to limit the resistivity of films doped over large temperature ranges and dopant solution.

Hall Effect method is the most common technique used to determine thin-film mobility and carrier concentration. Figure 3.40 shows the carrier concentration (n=1/R_H) and Hall mobility (μ_H=σ/ne) in the crystallites obtained from Hall measurements as a function of annealing temperature for the four different phosphorus concentration of C_{P505}=4.5×10^{19}cm^{-3}, C_{P507}=5.0×10^{20}cm^{-3}, C_{P508}=1.5×10^{21}cm^{-3}, C_{P509}=2.0×10^{21}cm^{-3}. The diffusion annealing temperature has a significant effect on the carrier concentrations that vary between 1.25×10^{19}cm^{-3} and 5.92×10^{20}cm^{-3}, which also depends on the phosphorus dopant concentration. The carrier concentration increased from 800°C value in all cases, with a larger change caused by annealing at lower temperatures. Since the dopant concentration is much higher than the number of trapped carriers, N^* (~3×10^{17}cm^{-3}), the carrier concentration n is a direct measure of the total number of ionized dopant atoms in the crystallites. In the polycrystalline films the dopant atoms in the crystallites, which can be assumed to have the nature of sc-Si, can also be assumed to be completely ionized, and the total dopant concentration in the crystallites can be directly equated to the carrier concentration obtained by the Hall measurements. Therefore, it can be concluded that the reduction of carrier concentration upon annealing at lower temperatures is caused by the reduction in the number of dopant atoms in the grains, that is, by the segregation of some of the dopant atoms to the grain boundaries. This conclusion is further strengthened by the observed reverse behaviour of the resistivity upon annealing at lower temperatures, as shown in Figure 3.39, which is a definite indication of the movement of dopant atoms between grains and grain boundaries and by the large change in the resistivity upon annealing for the lowest dopant concentration.

In general, a smaller value of Hall mobility (μ_H) is measured in polycrystalline semiconductors as a result of the smaller number of carriers that transfer charge between current contacts as compared with the potential barrier-free case. Hall mobility decreases with increasing diffusion process temperature, from 800°C to 1000°C. It has a maximum of 56.6cm^2/Vs at 900°C for P505 (4.5×10^{19}cm^{-3}) doping. This value is comparable with the results of Mandurah et. al. [59]. They found the Hall mobility of 33.8cm^2/Vs for phosphorus doped poly-Si film diffused at 900°C. Our experimental results give that almost 1.5 times more mobility for the same phosphorus concentration and diffusion temperature.

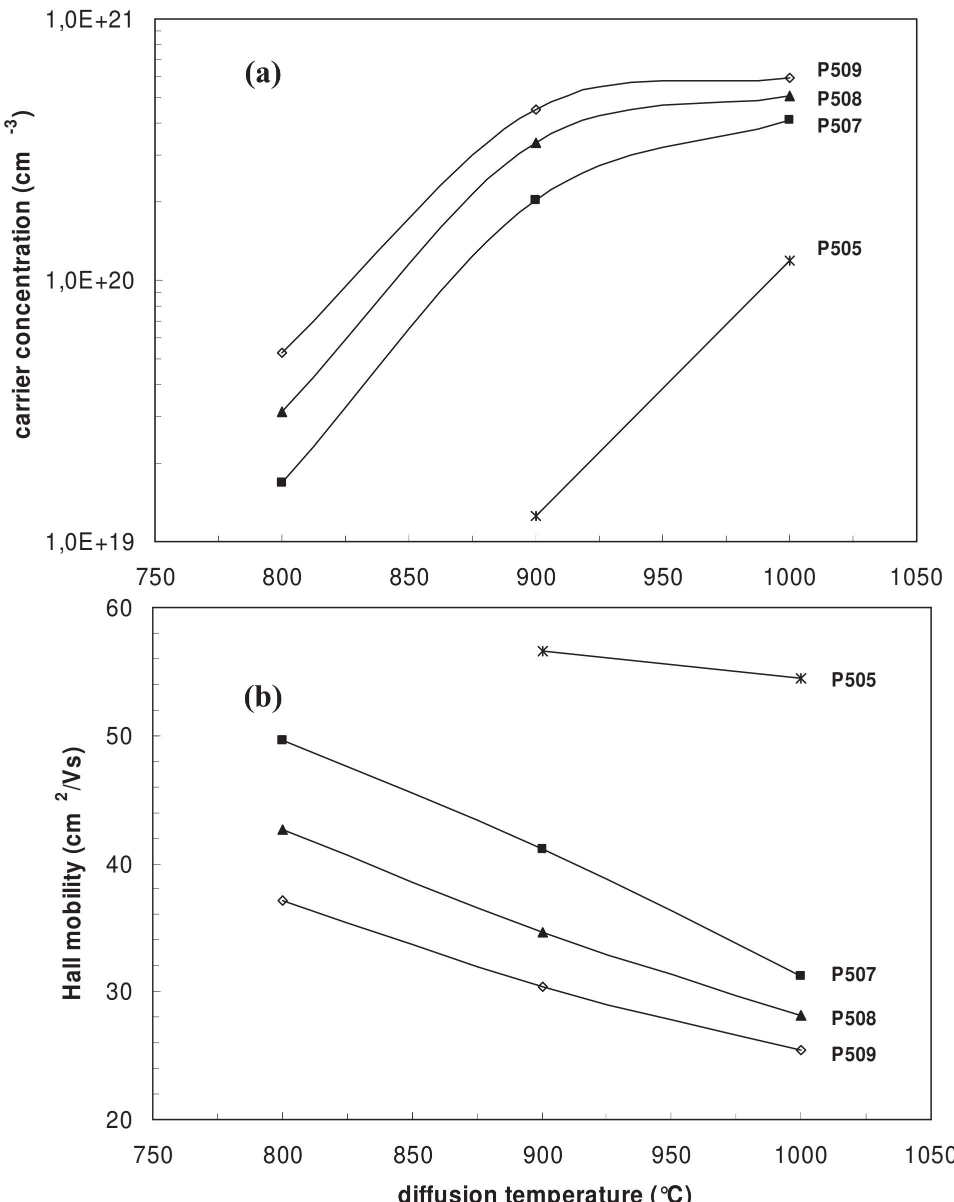


Figure 3.40: Results of Hall Effect measurements: (a) carrier concentration (n) in n-type polycrystalline silicon films as a function of annealing temperature, and (b) room temperature Hall mobility (μH) as a function of diffusion annealing temperature, for four different dopant concentrations. The films were annealed at 800°C, 900°C and 1000°C.

As shown in Figure 3.40, the increase in carrier concentration n is accorded with decreasing Hall mobility upon annealing in all cases. This change is more significant for higher concentrations. The lowest result of the Hall mobility (25.4cm^2/Vs) was correlated to the highest electron concentration (5.92×10^{20}cm^{-3}). This dopant concentration dependent variation of Hall mobility was explained by Kamins [78]. At low dopant concentrations the depletion regions extend completely through the grain, and the barrier height is small.

Thereby the mobility is high. When the dimensions of the depletion regions surrounding the grain boundaries become smaller than the grain size, neutral regions in the interior of the crystallites are surrounded by depletion regions, which present a barrier to current flow. In this intermediate range of doping, the conduction is activated process with an activation energy related to the barrier height. As the dopant concentration increases, more carriers are trapped, the barrier height increases, and the mobility decreases. Additionally, higher concentrations are correlated to lower mobilities indicating that impurity scattering is the dominant scattering process [79]. When the diffusion annealing temperature dependent Hall mobility profile is considered, the change in mobility is quite strong for phosphorus doped silicon with increase annealing temperatures. The mobility tends to decrease linearly from 800°C value in all cases for higher temperature processes. This can be attributed to the increase of the carrier concentration by increasing the diffusion temperature, resulting in lower mobility.

As a summary of this paragraph, we have shown that it is possible to efficiently convert a thin p-type polysilicon layer into a highly doped n-type poly-Si thanks to the phosphorus diffusion at high temperature. The electrical parameters of n-type seed layer strongly depend on the amount of phosphorus concentration and the phosphorus diffusion conditions such as diffusion temperature. The decrease in resistivity with increasing the diffusion temperature is due to the incorporation and electrical activation of the phosphorus atoms within the polysilicon AIC layers. The decrease in resistivity can be attributed to the higher amount of the filling of traps along the grain boundaries by increasing the phosphorus concentration. It can be concluded that the reduction of carrier concentration upon annealing at lower temperatures is caused by the reduction in the number of dopant atoms in the grains, that is, by the segregation of some of the dopant atoms to the grain boundaries. Addition to resistivity and carrier concentration, the other correlation is established between carrier concentration and Hall mobility: the increasing in carrier concentration is in agreement with decreasing Hall mobility upon annealing in all cases. This can be attributed to the increase of the carrier concentration by increasing the diffusion temperature, resulting in lower mobility.

3.4.4 Effect of Post-Annealing for N-type AIC Seed Layer

In this part, the influence of post annealing by classical thermal annealing (CTA) in tube furnace on the crystallography and electrical parameters of n-type AIC polycrystalline Si film on glass-ceramic substrate are investigated. The first aim of this post annealing is for the defect passivation [80]. Defect passivation is critical to device performance. Due to the temperature limitations in the formation of AIC seed layers, point-like and extended defects are present in the films typically prepared either by thermal crystallization of amorphous Si. These defects provide recombination centres in the band gap, drastically reducing minority carrier lifetime within the device. As such, the removal of these defects may be mandatory and typically done via thermal post annealing [81].

Secondly, the post-annealing effect is studied to simulate the thermal effects on AIC grain structure during the high-temperature epitaxial growth. In our case, the epitaxial growth is performed at quite high temperature for higher quality poly-Si film (≥1000°C). High-temperature epitaxy has an influence on the defect structure for the final poly-Si film. In order to eliminate the in-grain defects, the crystallization of a-Si should be performed at high temperatures [82] since the activation energy of the twins is very low, and they start to migrate at temperatures above 750°C. However, at this temperature the migration velocity of twin boundaries is very low. Therefore, higher thermal annealing temperatures (≤1000°C) must be preferred in order to accelerate and annihilate the twin boundaries, thereby improving the film quality.

The post-annealing effect on crystallographic properties is studied by EBSD analysis for n-type AIC seed layer formed at 500°C for 6h on glass-ceramic substrate. The comparison of crystallographic structure of AIC poly-Si films depending on the post-annealing process is illustrated in Figure 3.41. The samples area shown in the figures are $100\times100\mu m^2$, with a mapping step of 0.2µm. Each color in this orientation map indicates a specific crystallographic direction, and the standard color triangle that shows a prominent three dimensional texture is shown in inset of each orientation map. The grain orientation related texture can be examined by the grains whose similar crystal orientations are shown in similar colors can be easily. Preferred orientation for all samples is <100> independently from post-annealing process. However it must be noticed that the orientation maps shown in Figure 3.41 includes the twin boundaries as discussed in 3.3.5. The average grain size including and excluding twin boundaries, and other microstructure parameters such as preferred orientation

and grain boundary characters are summarized in Table 3.12 depending on the post-annealing conditions.

As depicted in Table 3.12, there is no significant difference on the crystal structure after post-annealing. The average grain size remains almost the same giving ~12µm (excluding twin boundaries) while the preferred orientation of the all samples is <100>. When the grain boundary character is considered for all samples, the same stability keeps on. The main defect is first order Σ3 twin boundary with and without post-annealing.

Finally it can be concluded that there is no noticeable difference after post annealing at high temperatures when the results are compared before post-annealing. Additionally, the AIC layer retained its crystallography during high-temperature epitaxial growth as will be discussed in Chapter 4.

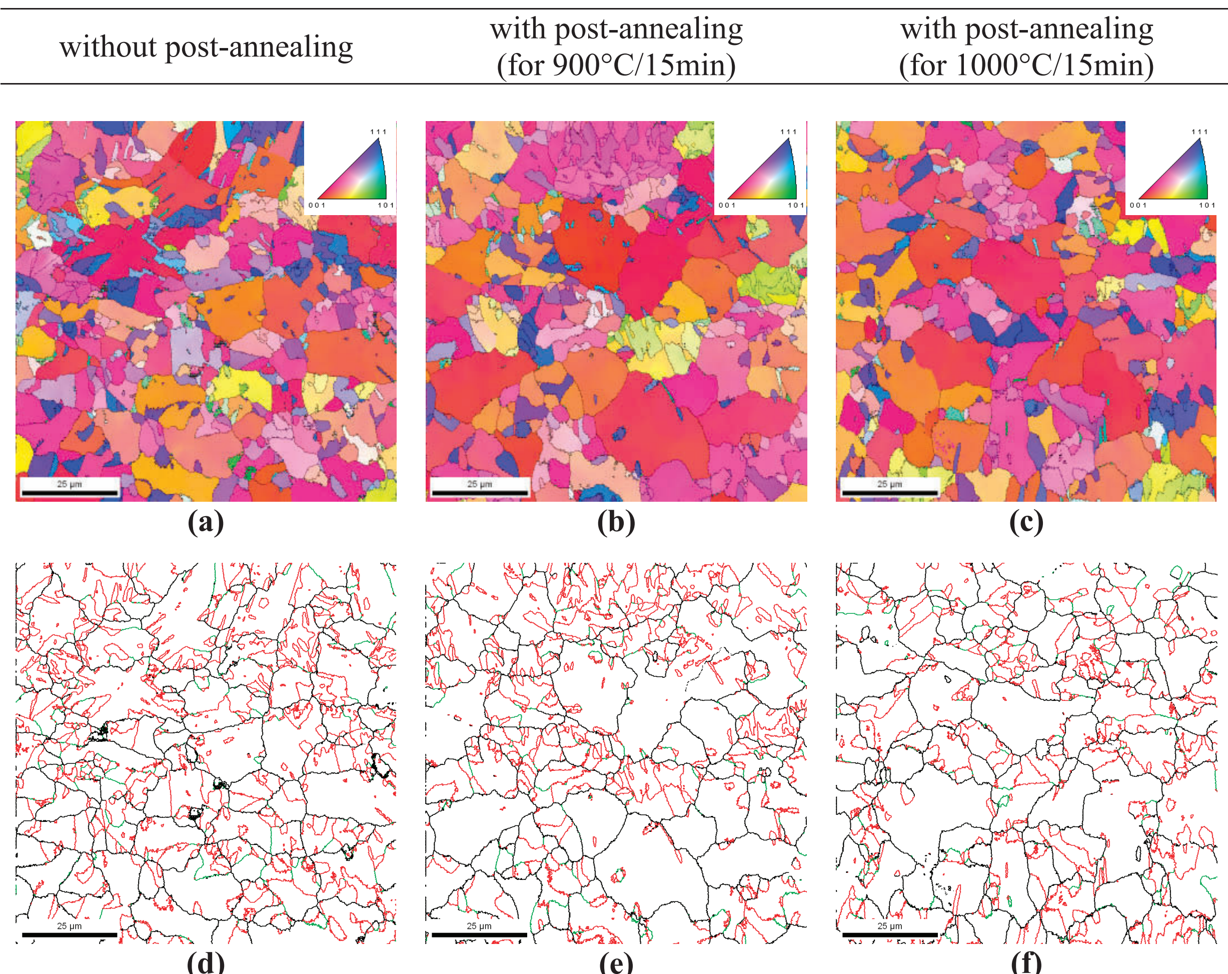


Figure 3.41: (a,b,c) Orientation maps deduced from EBSD analysis for the samples without and with post-annealing; and (d,e,f) high and twin boundaries maps [black lines: high-angle boundaries (>15°); twins → red lines: Σ3 (60°), and green lines: Σ9 (38.9°)].

Post Annealing	**Average grain size (µm)**		**Largest Grain Size (µm)**	**Preferred orientation**	**GB's Character Distribution (fraction no.)**				
	including twin	**excluding twin**			**LAGB's**	**CSL** (Coincident Site Lattice, twin boundary)			**HAGB's**
					2°<δ<15°	**Σ3**	**Σ9**	**Σ27**	**δ>15°**
Without	4.1	11.7	20	<100>	0.04	0.56	0.05	0.02	0.29
900°C/15min	4.5	13	23	<100>	0.03	0.57	0.05	0.03	0.27
1000°C/15min	4.6	10.6	20	<100>	0.07	0.49	0.07	0.01	0.33

Tablo 3.12: Summarized EBSD analyze results before and after post-annealing.

In summary of this part, we have investigated the effect of post annealing process at high temperatures (900°C and 1000°C) of n-type AIC seed layer on crystal structure. These temperatures are critical for the defect structure. However, it can be conclude that there is no difference either in grain size or grain boundary character after high temperature post-annealing of AIC layers. This is in agreement with the electrical parameters of the AIC layers as shown above, which did not change as well after post-thermal annealing.

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CHAPTER 4: POLYCRYSTALLINE SILICON SOLAR CELLS WITH AIC SEED LAYER APPROACH

Polycrystalline silicon layer with quite large grains can be formed by aluminium induced crystallization (AIC) technique on foreign substrates, as discussed in the previous chapter. However, the AIC poly-Si layers being too thin (~200nm) and heavily doped ($C\sim2\times10^{18}cm^{-3}$ for p-type film or $C\sim6\times10^{20}cm^{-3}$ for n-type film when P509 doped) to serve as a base for solar cell, therefore an epitaxial thickening step is necessary to form the absorber layer with a thickness of 2-10µm. On the other hand, these highly doped p^+- and n^+-type AIC polysilicon layers can be used for many meanings: as a seed for further growth, as a back surface field for carriers and more originally, as a doping source for the epitaxial layer when thickening. Our aim is to develop and study the cell configuration of p^+pn^+ an n^+np^+. The schematic diagram of these cell structures are illustrated in Figure 4.1a and 4.1b.

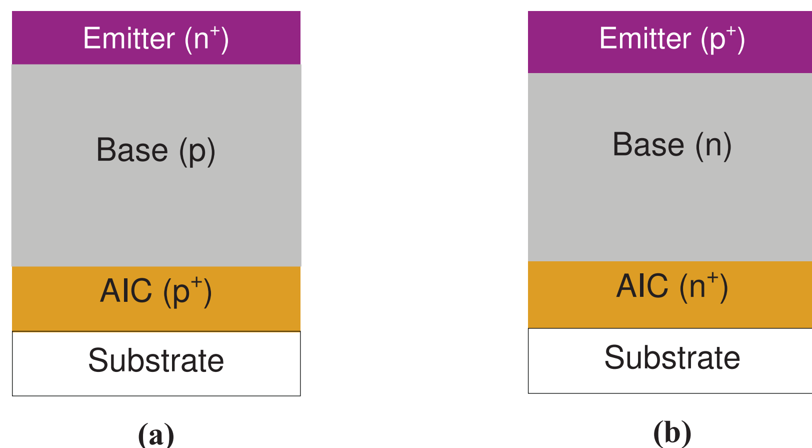


Figure 4.1: Diagram of possible cell structures by AIC seed layer approach on foreign substrates: (a) p^+pn^+, and (b) n^+np^+ cell configurations.

For p-type cell configuration (Figure 4.1a) the active layer was thickened by boron doped epitaxy. For n-type cell configuration, we used undoped epitaxial thickening as we benefit from the exo-diffusion of phosphorus during high-temperature epitaxy. In this work we have applied our processes on alumina or glass-ceramic substrates since they allow the epitaxial thickening at high temperatures (1000-1200°C). After the growth of p^+p or n^+n graded film structure, the emitter layer consisting of amorphous layers was formed on top of the base layer to form a heterojunction. The dopant type of the emitter depends on the cell

configuration: an n^+ type emitter was formed on top of the p-type base layer (Figure 4.1a), while a p^+ type emitter is formed on top of the n-type base layer (Figure 4.1b).

4.1 EPITAXIAL THICKENING ON AIC SEED LAYER

The basic idea here is that the thin p^+- or n^+-type AIC seed layer of excellent structural material quality acts as a crystal template for the crystalline layer that is grown on top of it. The crystal properties of the seed layer are transferred to the growing crystalline material via epitaxy. The main advantage of this method is that the properties of the seed layer and subsequently grown crystalline layer can be independently optimised, whereby the focus is on the structural quality and the grain size for the seed layer, and on the electronic quality for the epitaxial layer. The epitaxial layer is typically 1 to 20µm thick. It exhibits the same crystal orientation as that of the underlying crystalline substrate. For the fabrication of an epitaxial silicon layer on an AIC poly-Si seed layer are currently being explored: (i) low-temperature (<600°C) solid phase epitaxy (SPE) of evaporated a-Si [1] to smooth oxide-free AIC poly-Si seed layers on glass, and (ii) high-temperature vapor phase epitaxy (VPE) using silicon-chlorine based gases or silane (SiH_4) as silicon precursors on foreign substrates (Figure 4.2).

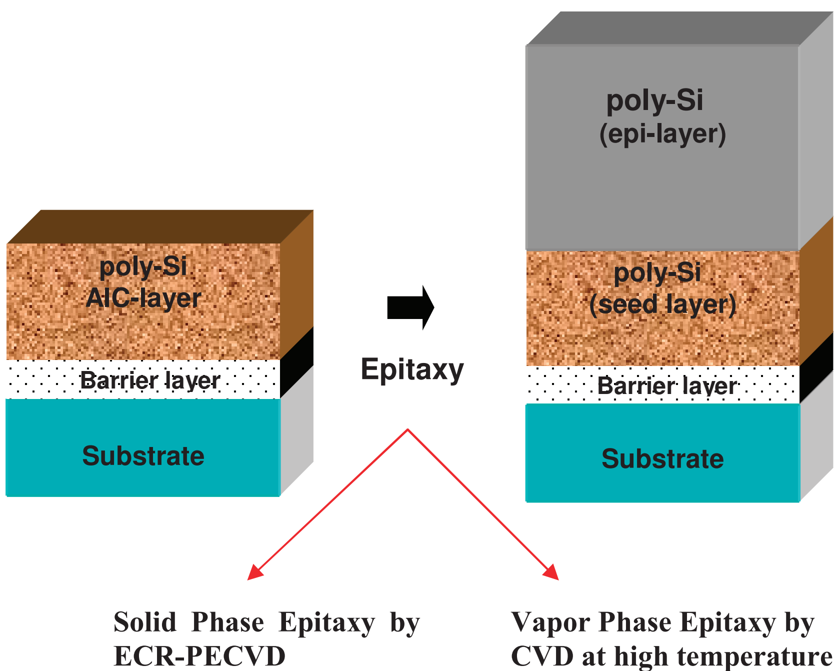


Figure 4.2: Schematic representation of epitaxial thickening for AIC seed layer on foreign substrate (not in scale).

More precisely the vapor phase epitaxy works on the principle of initiating a surface chemical reaction in a controlled atmosphere, resulting in the deposition of a reacted species on a heated substrate. In contrast to sputtering, VPE is a high temperature process depending on the system. VPE or Chemical vapor deposition processes are categorized as atmospheric-pressure (APCVD), low-pressure (LPCVD), and plasma-enhanced (PECVD), which also encompasses high density plasma (HDP-CVD). APCVD and LPCVD methods operate at rather elevated temperatures (600-1000°C). In PECVD and HDP-CVD, the substrate temperature is typically <600°C. Substrate temperature, gas flows, presence of dopants and pressure are important process variables for all types of CVD. Power and plasma excitation RF frequency are also important for PECVD. As for the silicon gas sources used during epitaxy, common ones are silane (SiH_4), dichlorosilane (SiH_2Cl_2), and silicon tetrachloride ($SiCl_4$) depending on the deposition method. Nominal growth rates are between 0.2 and 4µm/min, depending on the source gas and the growth temperature. Impurity dopants are simultaneously incorporated during the growth process by the dissociation of a dopant source gas in the same reactor. Arsine (AsH_3) and phosphine (PH_3), two extremely toxic gases, are used for arsenic and phosphorus (n-type) doping, respectively; diborane (B_2H_6) is used for boron (p-type) doping. Thus, chemical vapor deposition processes allow the deposition of polysilicon as a thin film on a silicon substrate with the desired type of dopants and its distribution over the grown layer. The film thickness can range between a few tens of nanometers to several micrometers. Structures with several layers of polysilicon are feasible.

In contrast to VPE methods, where impinging silicon material on the seed layer surface immediately forms a crystalline film via epitaxy, the SPE method consists of a two-step process: (i) deposition of a-Si in a solid phase on an oxide-free seed layer, and (ii) solid phase crystallization of the a-Si via epitaxy. More details about the process are given below

4.1.1 Solid Phase Epitaxy (SPE)

The solid phase crystallization (SPC) of amorphous silicon (a-Si) is extensively used nowadays to form poly-Si films mainly for thin film transistors sector. Matsuyama et al. [2] have developed an advanced SPC process for thin silicon films deposited by plasma-enhanced chemical-vapor deposition (PECVD) for solar cell application. Today, the company CSG Solar uses SPC of silicon for large area solar cell production. Recently, an efficiency of 10.4% was achieved on a 94cm^2 minimodule [3]. The drawbacks of SPC are however long thermal process (days), small grain size (1–2µm) and poor crystallographic properties [4]. On

the other hand, the aluminium induced crystallization which is a derivative of the SPC method can allow the formation of large-grained poly-Si films [5], which can serve as a seed layer for further thickening by epitaxy. The Solid phase epitaxy (SPE) method that uses the same equipment than the SPC for amorphous silicon deposition and maybe the same annealing furnace can be an interesting alternative to the VPE method. It combines the advantages of seed layer approach and SPC technique. In these regards, it is suggested that SPE might provide high quality poly-Si thin films by improving the crystallographic properties.

i) Principle of SPE

When we consider the SPE technique, theoretically, this technique is based on depositing an a-Si film on a crystal structure, and subsequently annealing to convert the deposited a-Si film into crystalline layer in registry with the seed layer (Figure 4.3). The basic "driving force" for such reaction is the lower energy of the ordered crystal compared to the amorphous state.

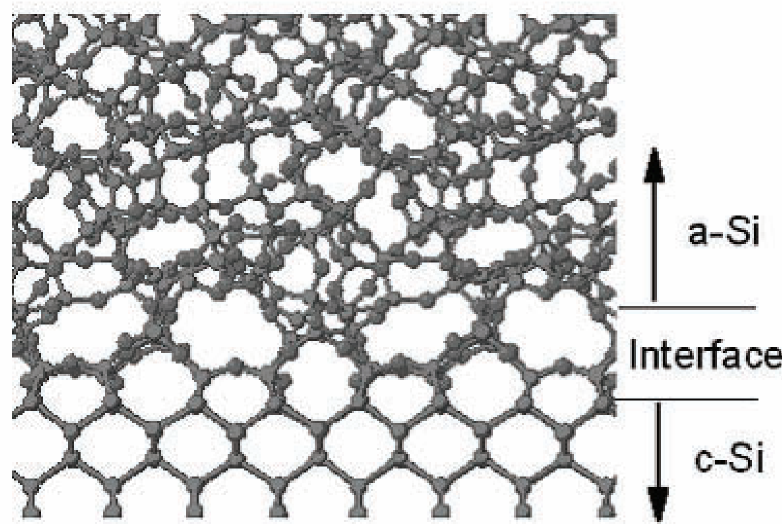


Figure 4.3: (a) Side view of the a-Si/c-Si (001) interface structure [6].

Heating at temperatures above 500°C usually induces a solid phase transition of a-Si into thermodynamically stable crystalline Si phase. In the case of a-Si layers on top of a single crystal substrate, this transition occurs by planar motion of the c-Si/a-Si interface from the interior towards the surface. This process is referred to as solid phase epitaxy (SPE).

Csepregi et. al. [7] explained the regrowth of the metastable amorphous phase by a bond-breaking mechanism, which allows the transfer of atoms at the c-Si/a-Si interface from irregular positions to regular lattice positions. Since the measured regrowth is epitaxial, it is

assumed that atoms can be transferred from amorphous to crystalline phase at positions, where at least two nearest-neighbouring atoms at the interface are already in the crystalline positions. On this basis, growth cannot occur in <111> direction, since alternate planes have atoms with only one bond along this direction. Csepregi et. al. suggest that growth along <111> direction involves nucleation, hence leads to nonuniform interfaces and twin formation. If Figure 4.4 is considered with respect to these explanations, the atoms marked as A will occupy the crystalline position first, then B, C, etc. Finally Csepregi et. al. showed that the other important parameter strongly influence the crystallization rate is the substrate orientation. For instance, the recrystallization on <110> and <111> oriented substrates is, respectively, 3 and 25 times smaller than recrystallization on <100> oriented substrate.

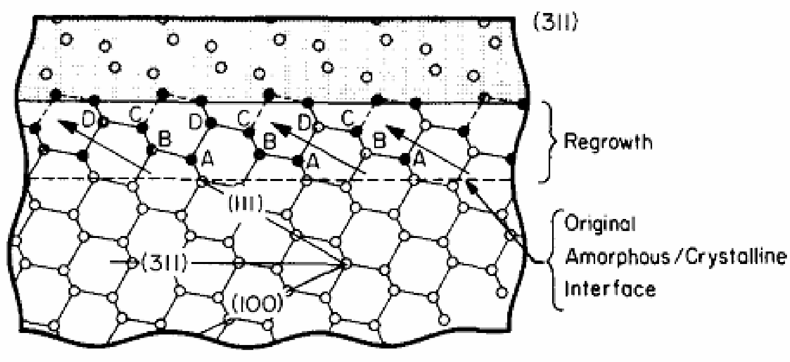


Figure 4.4: Section looking down the $[01\bar{1}]$ axis in Si.

Spaepen and Turnbull [8] developed this concept to construct a model of the c-Si/a-Si interface. According to their model, the interface should be highly saturated with few unbonded atoms. For this reason, a bond-breaking activation event is responsible for the activation energy for regrowth.

From practical point of view, the SPE method is a promising candidate for the poly-Si growth technology, in a conventional furnace, at temperatures not exceeding 600°C [4]. However, this crystallization process has limitations, due to long annealing time and the in-grain defect formation, namely microtwins [9,10]. In order to eliminate the in-grain defects, the crystallization of a-Si should be performed at higher temperatures [11] since the activation energy of the twins is very low, and they start to migrate at temperatures above 750°C. However, at this temperature the migration velocity of twin boundaries is very low. Therefore, higher thermal annealing temperatures (≤1000°C) must be preferred in order to accelerate and annihilate the twin boundaries, thereby improve the film quality.

Temperature dependent thermal crystallization rate of a-Si on <100> silicon substrate is shown in Figure 4.5. As shown, the growth rate of epitaxial crystallization is strongly dependent on temperature, and it presents an Arrhenius-like behaviour with unique activation energy of 2.68±0.05eV. Significantly, data from this study reflect some 10 decades of SPE growth rate over temperatures spanning 450-1350°C. For instance, at a temperature of 470°C, the crystallization rate is ~0.1nm/min, while this dramatically increases to ~0.5cm/min at 1000°C.

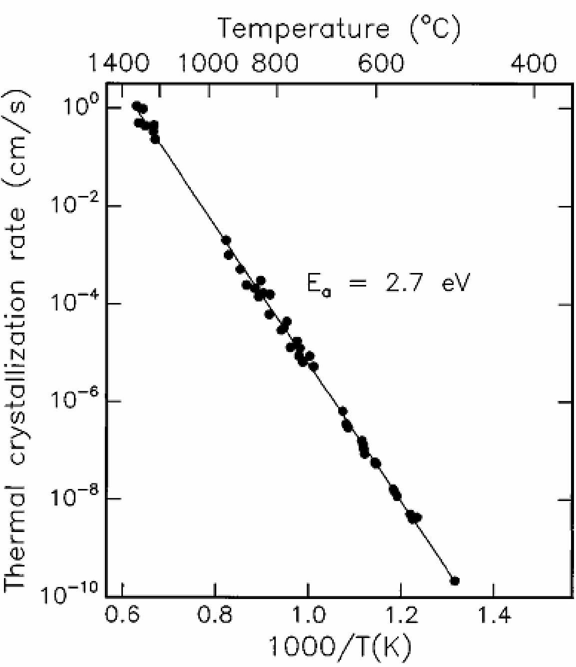


Figure 4.5: Temperature dependence of the thermal epitaxial crystallization rate for ion implanted a-Si layers on <100> silicon substrates [12]

ii) Experimental procedure for SPE on AIC layer

For the SPE study, poly-Si films formed by aluminium induced crystallization method and those converted into n-type AIC silicon were used as an underlying seed layer for the SPE process. The SPE step was performed at high temperatures (>700°C). FOx-coated alumina (Al_2O_3) substrates were used for these experiments. The effect of FOx solution on quite rough alumina surface has been discussed in Chapter 3. FOx coating on alumina substrates were followed by the AIC process to produce ~200nm thick poly-Si seed layer. AIC process includes Al and a-Si depositions, respectively. A 200nm thick Al was deposited by electron beam evaporation system. Prior to a-Si deposition the samples were exposed to ambient air

for one week to form aluminium oxide layer (AlO_x), which behaves as a permeable membrane separating the Al and a-Si layers during the AIC exchange process. It has been extensively shown that this layer controls the diffusion of silicon into the aluminium [13,14]. Then, 370nm thick a-Si was deposited by ECR-PECVD at deposition rate of 3.7Å/s. After the a-Si deposition, alumina/FOx/Al/AlO_x/a–Si structures were annealed at 500°C for 5h under nitrogen flow to complete the formation of the AIC layer by the layers exchange process. After the exchange, a residual layer consisting of Al+Si islands remains on top of the AIC layer [15]. This residual layer was cleaned by chemical etching.

The doped P505 and P509 solutions were used for converting the type of seed layer from p^+-type to n^+-type as described above. The phosphorus concentration of the P505 and P509 are $4.5\times10^{19}cm^{-3}$ and $2.0\times10^{21}cm^{-3}$, respectively. After P50X (X=5 or 9) coating by spin-on technique, the samples were baked at 80°C for 5min and subsequently at 200°C for 10min in order to remove the solvents. Then, the samples were annealed in a tube furnace at 1000°C for 1h under argon flow for the diffusion of phosphorus into the poly-Si seed layer. The residual phosphorus layer on top was then cleaned by HF(5%).

The n-type AIC seed layers were then coated with a-Si:H thick film and subsequently thermal annealed for the formation of the absorbing layer. The ECR-PECVD system (as described in Appendix A) was used to deposite the undoped a-Si layer at 250°C. The SiH_4/Ar mixture gas was fed into ECR-PECVD. Gas flow rates used were 15sccm of argon (Ar) as carrier gas and 10sccm of silane (SiH_4) as precursor gas. The total pressure during a-Si deposition was about 5.2mTorr and the microwave power was about 500W with the a-Si deposition rate of 22.2nm/min. By using these operational parameters 2µm thick films of a-Si were deposited on n^+ type poly-Si. After a-Si deposition, SPE crystallization and exo-diffusion anneals were performed in a rapid thermal furnace (RTP) using halogen lamps as heating source or in a conventional tube furnace (CTP) under argon flow. The temperature range was from 700 to 1100°C for CTP process while 1000°C was used as annealing temperature for RTP.

Poly-Si thin films with different anneal conditions were structurally characterized by optical microscope, micro-Raman spectroscopy, X-ray diffraction and UV/VIS/NIR reflectance spectroscopy. The phosphorous concentration profiles were analyzed by secondary ion mass microscope (SIMS).

iii) Structural properties of SPE films on AIC layers

Figure 4.6a and 4.6b exhibit the optical microscope images of the epitaxial formed silicon layers at 1000°C on n^+ type AIC layers in rapid thermal (RTP) and classical thermal furnaces(CTP) furnaces, respectively. The average grain size deduced from the optical microscope images vs. annealing time for both annealing processes is plotted in Figure 4.7. Polysilicon epi-layers with large grain structure were obtained after the crystallization annealing.

The epitaxial formation in a few seconds for RTP treatment can be explained by the incubation time. Indeed, RTP decreases the incubation time which allows the nucleation to starts earlier [16,17]. As a result, the crystallization can be completed in a shorter annealing time with larger grain sizes.

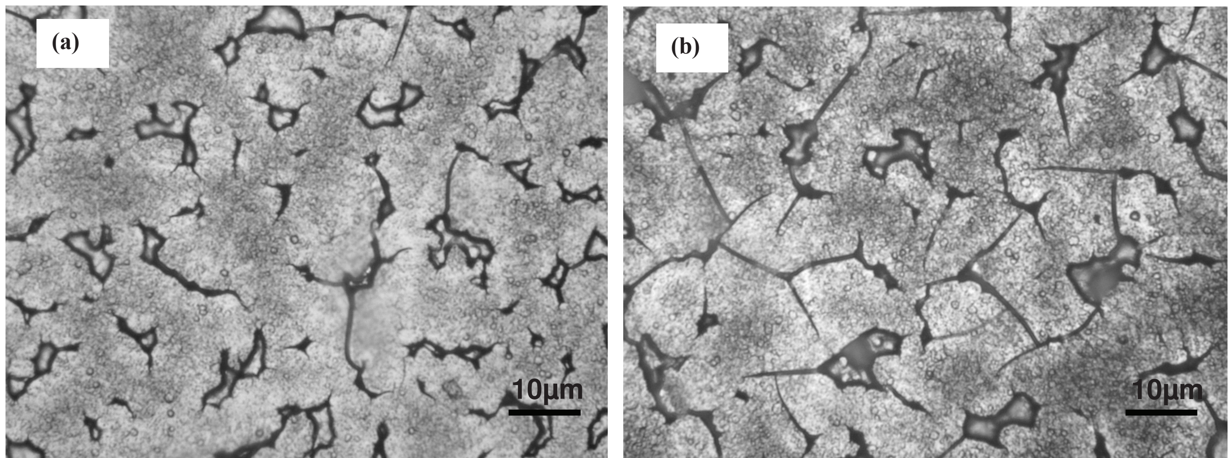


Figure 4.6: Optical microscope images showing the surface morphology: (a) in CTP at 1000°C for 30min, and (b) in RTP at 1000°C for 30 sec.

Figure 4.7 indicates that the poly-Si grain size increases with the longer annealing times for both RTP and CTP. Thus, quite large grains up to ~40µm are obtained by using SPE on n^+ type poly-Si. More importantly, less defective surface (Figure 4.6) and larger (average) grain sizes (Figure 4.7) were obtained after RTP. Clearly, low thermal budget for RTP treatment is very promising to obtain better quality polycrystalline silicon compared to CTP treatments for epitaxial growth on AIC poly-Si [17].

Conventionally, the solid phase epitaxy of amorphous silicon involves two steps, which are nucleation and growth [18]. The enhancement of the grain size and existence of fewer defects after RTP can be explained by a decrease in nucleation or an increase in the grain growth rate. The average crystallization rate was calculated for both RTP and CTP at 1000°C based on the optical microscope images. It is estimated to be ~5.0×10^{-5}cm/s and

~7x10^{-7}cm/s for RTP and CTP, respectively. The average crystallization rate is higher for RTP, speculating better surface results for RTP.

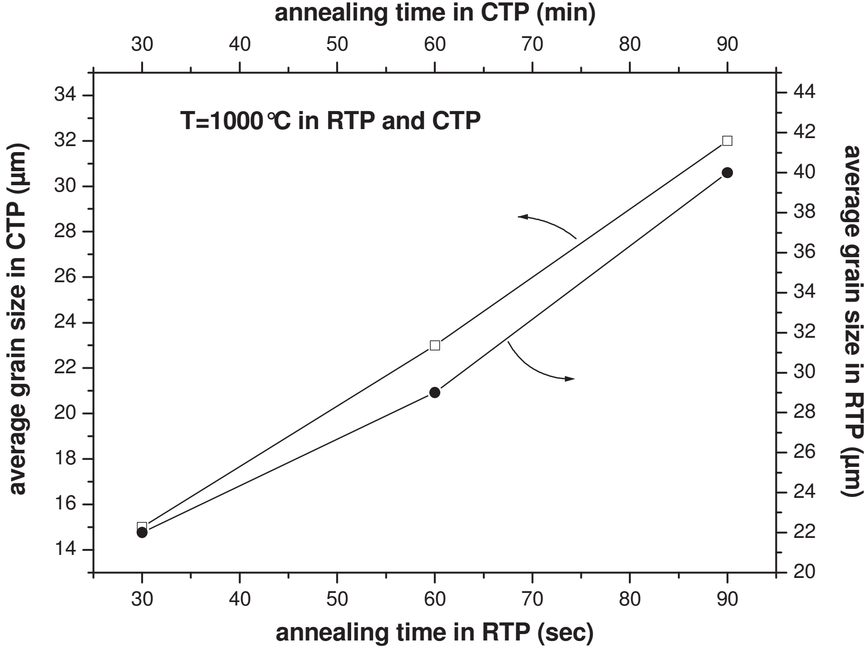


Figure 4.7: Average grain sizes of epitaxially grown poly-Si films on AIC layers using RTP or CTP at 1000°C for various annealing times.

The texture of epi-Si films formed on AIC poly-Si layer versus the experimental conditions can be assessed by X-ray diffraction (XRD). The XRD method has been carried out on the RTP's epi-films due to their larger grain size formation compared to CTP treated samples. In order to quantify the texture of the SPE poly-Si layers, crystallographic orientation factors Θ_{hkl} were normalized with respect to different diffraction peak intensities obtained on a randomly orientated polycrystalline powder taken as a reference. The crystalline preferential orientation $\Theta_{hkl}(\%)$ is defined for 6 chosen spectral lines by using [19,20]:

$$\Theta_{hkl} = 100 \frac{I_{hkl} / I_{0hkl}}{\sum_{hkl} I_{hkl} / I_{0hkl}} (\%) \tag{4.1}$$

where I_{hkl} and I_{0hkl} represent the diffracted intensities in the $\theta - 2\theta$ spectra of respectively the poly-Si film and Si reference powder, for each <hkl> orientation. The XRD peak height for poly-Si is normalized by $[1-\exp(-2\mu t / \sin\theta)]$. The reason of the normalization is to take the finite film thickness into consideration. In this normalization definition, μ, t and θ are the

X-ray absorption coefficient (=143.1cm^{-1}), the film thickness and the X-ray angle of incidence, respectively.

Figure 4.8 shows the preferential orientation factor of the epi-layers as obtained after epitaxy in RTP at 1000°C for 30sec, 60sec and 90sec. According to this figure, the samples are not randomly oriented, since three large diffraction peaks namely <100>, <331>, and <311> are clearly visible. However, the strong preferential orientation is obviously <100> for all annealing times. We have found that 40-50% of the total surface has <100>-oriented grains for all samples. The variation of crystallization fraction depends slightly on the annealing duration at 1000°C in RTP. However, <100> is the preferential orientation for all samples, irrespective of these annealing conditions. Based on the discussions above, this result is expected for poly-Si formed by thickening the AIC layer that has already a majority of <100>-oriented grains [21]. Moreover, the XRD data reveal that the RTP treated samples have almost completed their crystallization from amorphous to polycrystalline phase, and they have nearly the same crystallinity.

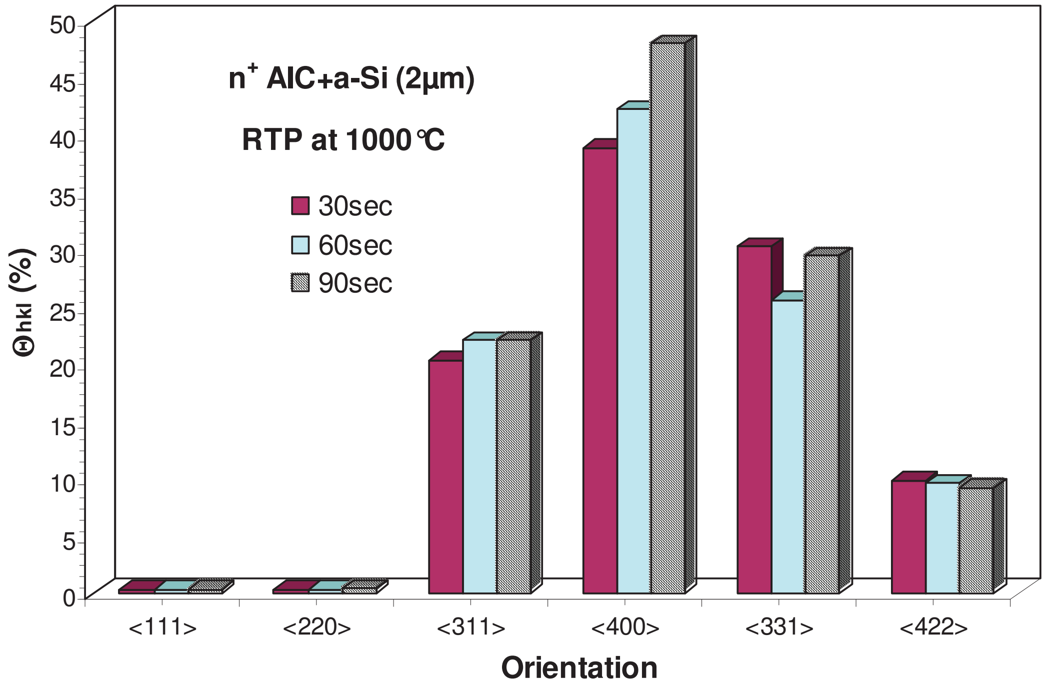


Figure 4.8: Preferential crystallite orientation, $\Theta_{hkl}(\%)$, of crystallized Si thin films by different annealing times at 1000°C in RTP.

iv) Crystallographic properties of SPE films on AIC layers

With respect to the analysis of poly-Si films on foreign substrates, micro-Raman and UV reflectance measurements have been employed to study the grain-dependent material quality. The purpose of structural analysis is the determination of crystallization, stress, crystal quality, etc., of thin films. These analyses were performed at various annealing conditions in RTP and CTP.

Micro-Raman spectroscopy is a straightforward, sensitive, fast and useful technique for characterizing the structure of poly-Si thin films. Thus, Raman spectroscopy is used for monitoring the crystal quality through the Si-Si band position, and its full width at half maximum (FWHM), crystallinity (crystalline fraction-X_c) and stress of the films. Firstly, the effects of recrystallization temperature in CTP are studied. Raman spectra of the poly-Si films after CTP at different temperatures, in the range of 700-1100°C, are shown in Figure 4.9. The epitaxial annealing time was fixed to 90min independently from annealing temperature.

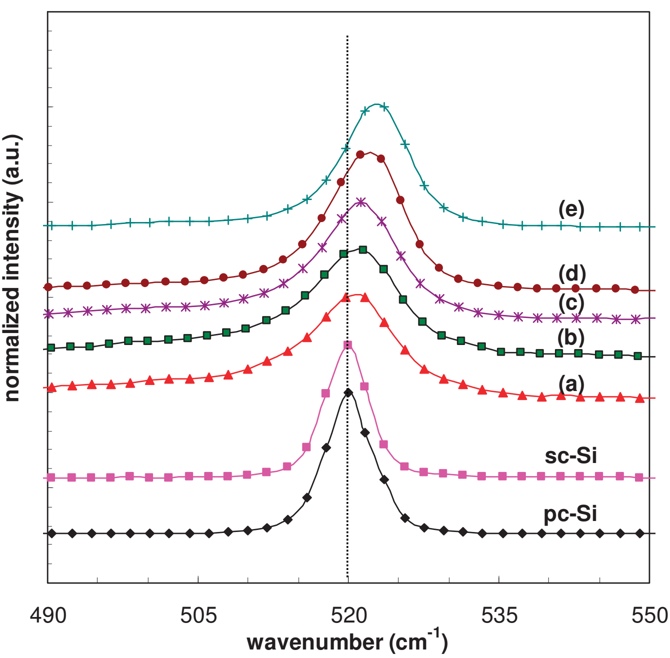


Figure 4.9: Raman spectra for the samples CTP heated at (a) 700°C, (b) 800°C, (c) 900°C, (d) 1000°C and (e) 1100°C, for 90min.

FWHM of Raman peak indicates the best crystallinity of the samples with the lowest FWHM value. Additionally, Raman spectra were used to analyze the crystalline fraction (X_c) of poly-Si films by integrating amorphous and crystalline areas of Raman spectra. To accomplish this, the total spectrum was deconvoluted in two sub-spectra, one corresponding

to the amorphous contribution and the other to crystalline contribution. Subsequently, the area under each sub-spectrum was calculated and the ratio of the integrated crystalline intensity to the sum of integrated crystalline intensity and integrated amorphous intensity was assigned. The X_c is calculated by [22,23].

$$X_c = \frac{I_c}{I_c + \gamma I_a} \tag{4.2}$$

In Equation 4.2, I_c and I_a are the integrated intensities of the crystalline component peaked at around 520cm^{-1} and the amorphous component peaked at around 480cm^{-1}, respectively, and γ=0.8 is a correction factor due to the different scattering cross section of amorphous and crystalline phases. The variation of the crystalline fraction and FWHM are shown in Figure 4.10 as a function of epitaxial temperature in CTP.

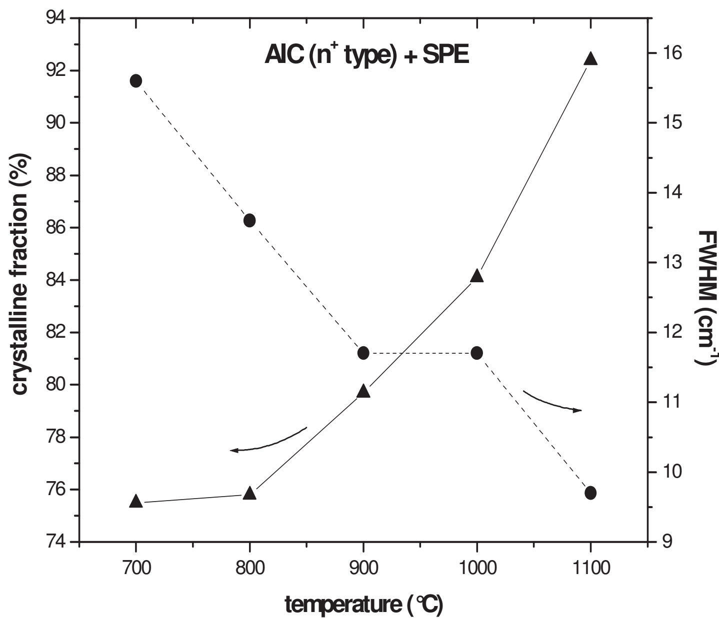


Figure 4.10: Crystallized fraction of samples and FWHM of Raman peaks as a function of CTP annealing temperature for samples grown by SPE on n$^+$-type AIC seed layer.

From this graph, it is obvious that the crystalline fraction of the films varies significantly with varying the annealing temperature from 700 to 1100°C (for 90min). Crystalline fraction increases up to 92% when the annealing temperature was increased, whereas FWHM decreases to 9.8cm^{-1} when the annealing temperature is increased up to 1100°C. FWHM of the Raman peaks depends on the crystallinity. The decrease in FWHM value of Raman peaks indicates an increase in crystallinity due to the similarity of sharp, narrow, and symmetric Raman peak of sc-Si. Additionally, the larger the FWHM is the

greater the defect amount namely dislocations and twinning, which are the main defects found within the poly-Si crystal grains [24]. It can be seen that FWHM of the Raman peaks reduces from 15.8 to 9.8cm^{-1} with increasing annealing temperature from 700 to 1100°C, since higher temperatures has more defect passivation by improving the crystal quality, as discussed above. The FWHM reduce with enhancement of crystallized fraction for higher temperature, so the high temperatures, such as 1000°C or 1100°C will be the preferable temperatures for the further experiments. The higher crystallization of poly-Si films annealed at high temperatures was expected, because increasing the crystallization temperature raises the crystal nucleation rate and the crystal growth rate. Even though the FWHM become 9.8cm^{-1} after annealing at high temperatures (~1000°C), the crystallinity of poly-Si films is still lower than sc-Si whose FWHM is 5.9cm^{-1}.

Due to the higher crystallization at high temperatures, we can fix the annealing temperature at 1000°C to study the effects of annealing time and annealing systems of RTP and CTP. Figure 4.11 shows the relationship between the crystalline fraction (X_c) and the annealing time for both RTP and CTP crystallization processes. Equation 4.2 was used to calculate the crystalline fraction of silicon films, deposited on AIC layer, and annealed as a function of annealing durations that are in the range of 10 to 90 min for CTP and of 10 to 90sec for RTP.

As shown in Figure 4.11, crystallinity of the films annealed at 1000°C strongly depends on the annealing time, while temperature is a factor for improving the crystallinity. The crystallization of the films becomes crystalline contents of as high as 81.5% by CTP crystallization at 1000°C for 90min annealing duration. X_c values increase gradually with increasing annealing time from 75.5% to 81.5% for CTP and from 73.0% to 76.0% for RTP. This result says that the structural order of Si-Si network in the films is improved with increasing annealing time [25]. The increase of the crystalline fraction can be strongly correlated to the enlargement of the grains for longer annealing time, as shown in Figure 4.7.

During the epitaxial process that involves the recrystallization, volume differences between the involved phases, coalescence of isolated crystallites, when forming a grain boundary, uncertain atomic compositions, structural arrangements, material geometry, thermal steps (due to different thermal expansion coefficients) defects in the crystalline matrix (twinning, dislocations and grain boundaries), microstructure (crystallinity, grain size and orientation) and interactions in crystallites and at the substrate/film interface can be the different origins of stress in film [26].

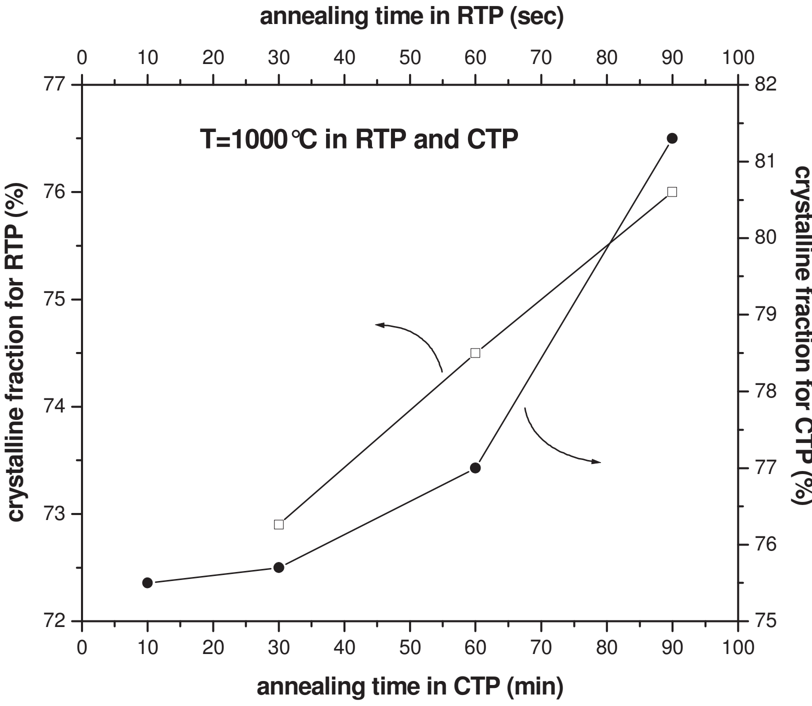


Figure 4.11: Crystalline fraction of recrystallized poly-Si films in RTP and CTP at 1000°C.

The determination of the stress level is very important to understand the thin film quality. There are many stress measurement techniques like X-ray diffraction (XRD) and cross-sectional transmission electron microscopy (XTEM). But these techniques are time consuming and lack spatial resolution or are destructive. Besides, micro-Raman spectroscopy is another technique that can be applied in stress characterization. Raman method is contactless and without sample preparation. Additionally, this method is non-destructive, fast, has high spatial resolution and has high sensivity for stress measurements [23]. Due to all these advantages, the stress of the thermal recrystallized poly-Si thin films was determined by using the micro-Raman spectroscopy.

The measured Raman spectra were de-convoluted for amorphous silicon ($480cm^{-1}$) and single crystalline silicon ($520cm^{-1}$) contributions using PeakFit computer programme. The Raman peak depends on the amount of residual stress in the material and is fitted with Lorenzian-Gaussian mix function to determine the wavenumber of the peak. The peak position of transverse optical (TO) Raman signal is at $520cm^{-1}$ for sc-Si. For this reason, the Raman peak at $520cm^{-1}$ is used as a reference for all our measurements. Figure 4.12 shows the Raman spectra of the epitaxial--Si films by CTP (a) and RTP (b) at 1000°C for various annealing durations. It can be noted that for CTP, the peak position of the films shifts with increasing CTP time towards higher wavenumbers. However, there is no peak position shift

from 520cm^{-1} after RTP crystallization. These results indicate that RTP treated poly-Si is stress free.

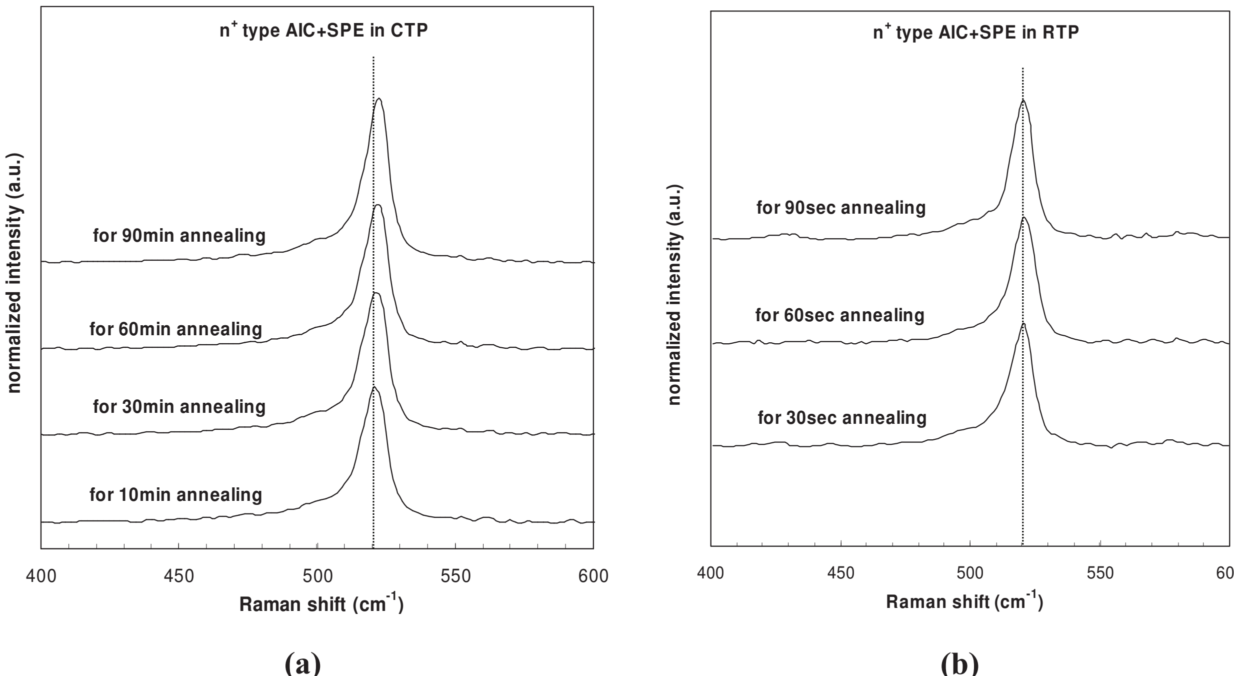


Figure 4.12: The Raman spectra of recrystallized poly-Si samples after annealing at 1000°C in: (a) CTP for 10min, 30min, 60min, 90min, and (b) RTP for 30sec, 60sec and 90sec.

Figure 4.13 plots the peak position and stress behaviour of the poly-Si samples calculated from Raman spectra as a function of the annealing time at 1000°C for CTP. Compressive stress affects the Raman peak by higher wavenumber shifts (blue shift) while the tensile stress shifts the Raman peak towards lower (red) wavenumbers [27,28]. It indicates that poly-Si thin films have compressive stress for all epitaxial annealing times in CTP due to the higher wavenumber located Raman TO peak position, while thin films have no stress for RTP without any wavenumber shift from sc-Si Raman peak position (520cm^{-1}). The correlation between the stress and Raman shifts can be determined from the relation [29,30]:

$$\sigma(Mpa) = -250(\omega_s - \omega_0) \quad (4.3)$$

where ω_s is the wavenumber of the stressed poly-Si and ω_0 is the wavenumber of the stress free single crystalline Si. We observed that stress varies with annealing temperature with a minimum of 325MPa for 10min annealing and maximum of 650MPa for 90min annealing. A Raman peak shift of 1.0cm^{-1} after 10min annealing means a stress of 325MPa. Higher annealing times cause further increase of the compressive stress up to 650MPa. Formation of

compressive stress after conventional furnace annealing of a-Si is well in agreement with previous studies [31,32].

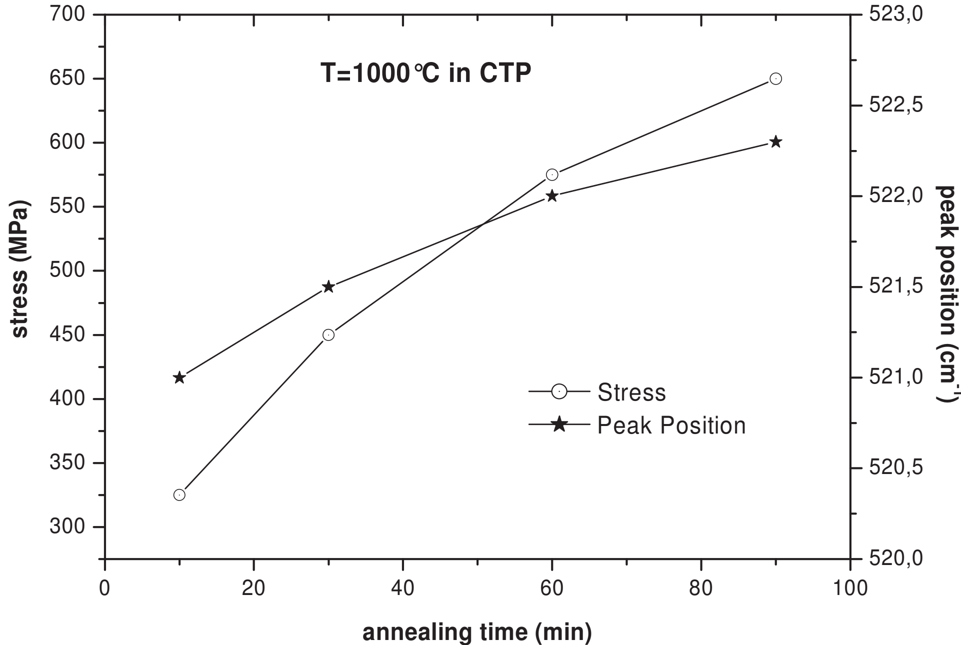


Figure 4.13: Peak position and stress profiles for epitaxial poly-Si samples in CTP at 1000°C versus annealing time.

Compressive stress is usually formed due to grain boundaries and annealing processes. Grain boundaries are known to compressively stress poly-Si films [33]. Thus, the variation in the compressive stress observed in the samples crystallized at 1000°C for this annealing range can be attributed to the stress induced by exposing the samples to quite high temperatures for longer time with the difference in temperature dependent thermal expansion coefficient (α_T) between alumina substrate and silicon layer [34,35]. Additionally, the time dependent stress gradient might arise from the change in the grain structure by annealing condition. Also, it can be declared that both high-temperature annealing for short time and lower-temperature annealing for longer time reduce the stress level in poly-Si film.

Another informative approach for crystallinity is the measurement of the hemispherical reflectance at short wavelengths (UV region, 250-450nm). UV reflectance measurements were carried out on all samples to determine crystallization of SPE poly-Si films epitaxially grown in various annealing conditions using CTP and RTP. Figure 4.14 shows the comparison of the total hemispherical reflectance at short wavelengths measured on poly-Si samples formed by SPE technique in CTP (a) and RTP (b). Additionally, Fz-Si wafer, a-Si film deposited by ECR-PECVD on glass, and poly-Si layer as-deposited by LPCVD

system on Fz-Si wafer were shown for comparison. The probed sample area was $1.25\times1.25cm^2$ in each case. Figure 4.14 plots the UV reflectance spectra for RTP and CTP treated samples. The degree of crystallinity of silicon is indicated by the reflectance peaks at $e_1\approx365$nm and $e_2\approx275$nm. The two prominent maxima in the reflectance spectrum of silicon layers lie at ~275nm ($\hbar\omega$=4.4eV) and ~365nm ($\hbar\omega$=3.4eV). They are caused by optical interband transitions at the X point along the Γ-L axis of the Brillouin zone, respectively [36], these maxima can still be discerned in the curve taken from the recrystallized poly-Si film but at a much lower level due to the surface roughness of sc-Si and recrystallized poly-Si films. When we consider the difference in maxima between the recrystallized poly-Si films, defects in the material lead to a decrease and broadening of the peaks, and hence, are a measure of the crystalline quality (i.e., the film quality) of the investigated silicon material (note that defects in the material lead to a decrease and broadening of the peaks [37]).

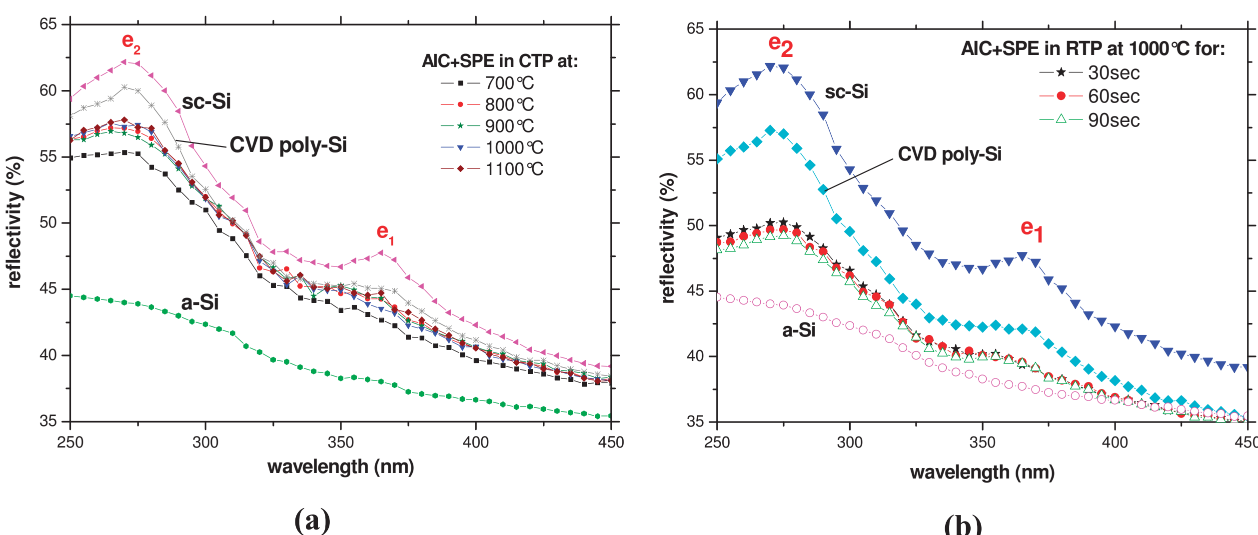


Figure 4.14: UV reflectance measured on a SPE film grown on an AIC seed layer and recrystallized after annealing: (a) in CTP at 700°C, 800°C, 900°C, 1000°C and 1100°C for 90min, and (b) in RTP at 1000°C for30sec, 60sec, 90sec. Also shown are the reflectance curves of sc-Si, poly-Si by direct high temperature–CVD and a-Si as reference.

Reflectance measurements are summarized in Figure 4.14 showing the main peaks in the wavelength range of 250-450nm. It is compared to the reflectance spectrum of a-Si deposited by ECR-PECVD, poly-Si by direct high temperature-CVD and crystalline Si wafer (sc-Si). As expected no signature of crystallinity is observed on the a-Si spectrum, while the two peaks are well defined for the single crystalline silicon (sc-Si). On the other hand, there is no significant difference in UV spectra for all poly-Si thin films, which indicates the

similarity in the crystalline quality of the samples. As shown in Figure 4.14, high quality silicon has R_{e1} =0.447 and R_{e2} =0.578 with CTP recrystallization at 1000°C for 90min while sc-Si has R_{e1} =0.477 and R_{e2} =0.622. It means that we can obtain quite good crystallization after CTP recrystallization at high-temperature annealing. However, as shown in figure, the recrystallization with RTP the reflectivity values are slightly lower by around 0.050 at the peaks than that of CTP values. The main effective parameter on this reduction can be the quite low thermal budget for RTP that cannot be enough sufficient to rearrange the a-Si atoms as a poly-Si. The reflectivity values might be enhanced by increasing the annealing time. The drawback could be then the control of the phosphorus exo-diffusion from seed layer through the Si layer which can be difficult, giving rise to high phosphorus concentration for epitaxial layer that can lead to minority lower life time and carrier diffusion length. Finally the reduction of the UV reflectance for poly-Si films compared to sc-Si and CVD can be attributed to the higher defect density (defects in grain and/or grain boundary) in the film or higher surface roughness due to use the alumina substrates.

The structural quality of a silicon film can be qualitatively assessed by the absolute heights of the e_1 and e_2 UV peaks. In the case of different crystalline-to-amorphous volume ratios in crystallized poly-Si films, UV reflectance spectrometry can be as an alternative technique for the evaluation of crystallinity. The quality factor can be calculated to find changes in the reflection peaks profiles for recrystallized SPE poly-Si films (i.e. to find the structural quality of the samples). The quality factor is defined as [38]:

$$Q = \frac{1}{2}\left[\frac{R_{e1}}{R_{e1.cSi}} + \frac{R_{e2}}{R_{e2.cSi}}\right] \tag{4.4}$$

where R_{e1} and R_{e2} are the sample's measured UV reflectance at e_1≈365nm and e_2≈275nm, and $R_{e1.cSi}$, and $R_{e2.cSi}$ are the corresponding values for the polished c-Si. The quality factor Q quantifies how closely the UV reflectance of sc-Si is mimicked by a particular sample and thus provides a qualitative measure of its area-averaged crystal quality. As discussed above, the UV reflectance of the ex situ annealed samples in RTP are lower than that of the ex situ annealed samples in CTP. The values of R_{e1}, R_{e2} and Q quality factor for all samples are listed in Table 4.1. By calculating Equation 4.4, the Q factor reaches 93% above 900°C while it is ~90%, ~91% and ~92% for annealing at 700°C, 800°C and 900°C in CTP, respectively. This result is compatible with the discussion above deduced from micro-Raman analysis. By calculating the Q for RTP annealed samples, the value of Q factor for 1000°C annealed samples enhance from ~80% after 30sec process to ~82% by annealing 90sec. As similar to

CTP annealing cases, these results are consistent with the results of μ-Raman analysis. It is worth to notice that the surface morphology as well as the roughness can attenuate the reflectance intensity for all poly-Si samples [36]. Thus the rough structure of the alumina affects the UV reflection spectra by decreasing its reflectivity and also the quality factor of the poly-Si thin films. Besides the quality of the films, this decrease in reflectance intensity is especially due to the reflection losses from the rough film surface.

Recrystallization Annealing Condition	*UV-Reflectance* (%)		*Q* (%)
	R_{e1} (e_1≈365nm)	R_{e2} (e_2≈275nm)	
700°C/90min in CTP	43.7	55.3	90.2
800°C/90min in CTP	43.9	56.2	91.2
900°C/90min in CTP	44.3	56.9	92.2
1000°C/90min in CTP	44.7	57.6	93.1
1100°C/90min in CTP	45.2	57.9	93.9
1000°C/30sec in RTP	38.7	48.8	79.8
1000°C/60sec in RTP	39.4	49.7	81.2
1000°C/90sec in RTP	39.8	50.3	82.1

Tablo 4.1: UV reflectance data from recrystallized samples subjected to RTP and CTP.

v) Dopants distribution in SPE film on AIC layers

Besides the recrystallization annealing dependent structural analysis, the other important concern is the possible diffusion of phosphorus from highly doped AIC seed layer used as a phosphorus source. During thermal annealing for epitaxial process, the phosphorus atoms can be activated through the epitaxial layer resulting in an n^--type layer for high crystallization temperatures (≥ 900°C) that are critical for the diffusion of phosphorus.

a. Solubility and impurity exo-diffusion

At a given temperature, there is an upper limit to the amount of an impurity, which can be absorbed by silicon (depending on the solid-solubility limit of impurity). At higher concentrations, only a fraction of the impurities actually contribute to holes or electrons for conduction. Figure 4.15a shows the solid solubility of different impurities in silicon. The solubility initially increases with temperature and then begins to decrease, as the crystal melting temperature is approached. When the maximum solubility is achieved at a certain temperature, the crystal is said to be saturated with the impurity at that temperature. If the

crystal is cooled to a lower temperature without removing the excess impurity, a supersaturated condition is created. The data shown in Figure 4.15a represents the solid solubility, not the electrically active dopant. Dopants introduced into silicon may occupy interstitial or substitutional positions in the silicon lattice. The method of introducing a dopant into silicon and subsequent heat treatments determine the amount of dopant that contributes to free carriers, i.e., electrically active. At high concentration the expression for the totally active phosphorus concentration is given by [39]:

$$C_T = n + 2.4\times10^{-43} n^3 \text{ atoms/cm}^{-3} \quad (4.5)$$

where n is the electron concentration or electrically active phosphorus concentration. This equation is valid within the temperature range of 900 to 1050°C. Phosphorus has a high solubility in silicon, and surface concentration of the order of ~10^{21}cm^{-3} can be achieved during high-temperature diffusion.

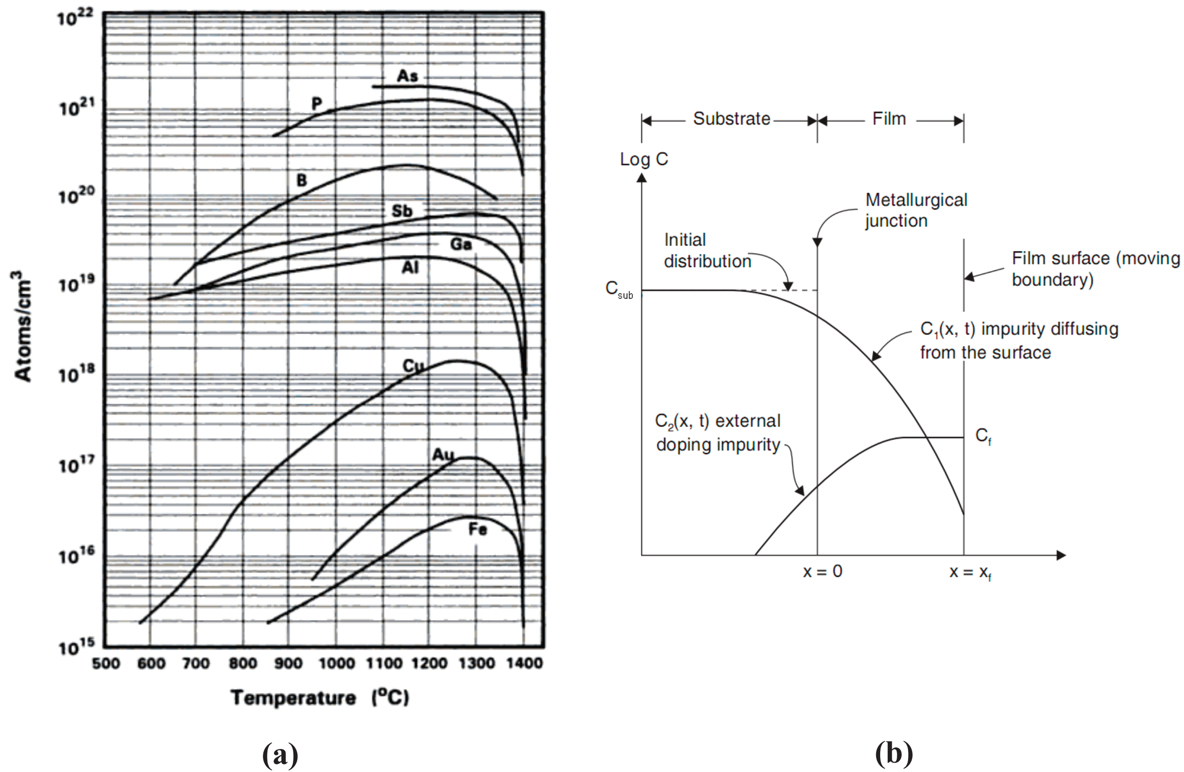


Figure 4.15: (a) Solid solubility of common impurities in silicon [40], and (b) impurity redistribution during epitaxial growth [41].

During the epitaxial thickening of highly doped substrate the redistribution of impurities incorporated in epitaxial layers occurs. Redistribution of the impurities during the epitaxial growth shows a different profile than diffusion for emitter formation which is

usually performed from an external source. During the high temperature epitaxial growth, the impurities diffuse up from the seed layer into the epitaxial film by exo-diffusion. Figure 4.15b schematically illustrates impurity redistribution during epitaxial growth.

During recrystallization many impurities move away from the c-Si/a-Si interface and relocate closer to the surface. In general, redistribution is more feasible at high impurity concentrations. By examining any one of the individual curves, one can see that the concentration of dopant at the surface is extremely high, falling off rapidly with distance into the epi-layer. For low-temperature SPE, there is a direct correlation between the magnitude of this redistribution effect and the impurity metastable solubility. After recrystallization, with SPE, annealing commonly leave residual damage in the silicon substrate, interstitial-diffusers are especially vulnerable to preferential diffusion toward the surface, where impurity atoms may be trapped, ultimately leading to a more shallow profile. Besides annealing conditions, this phosphorus profile is also dependent to the phosphorus concentration of seed layer, i.e. the phosphorus spin-on dopant. The duration (1h) of recrystallization in CTP process is enough for the dopant diffusion through epitaxially grown film. However, the speed of dopant diffusion is not as high as growth rate in RTP. For this reason, the phosphorus diffusion profile studies after SPE are focused on CTP annealing in this work.

b. Phosphorus distribution in the SPE epi-layer

Figure 4.16 shows the phosphorous concentration profile for the SPE n-type poly-Si on AIC seed layer as deduced from SIMS analysis. The SIMS technique measures the total impurity profile. Since, the sputtering rates generally range from less than one angstrom per second to several tens of angstrom per second, this technique is suited for measuring diffusion profiles for depths less than ~2µm.

SIMS profile is plotted for P5 (using P505 solution) and P9 (using P509 solution). The phosphorus concentration in the AIC layer is a plateau at about 2-3x10^{19}cm^{-3} for P5, while it is at about 2-3x10^{19}cm^{-3} for P9. A graded distribution is then observed, which is an indicative of the exo-diffusion of the phosphorus towards the epi-layer for both cases. But, P5 has a slightly downward P profile while P9 has an opposite behavior that is slightly upward around the interface between AIC seed layer and epi-layer. Then the profile followed by an almost constant concentration at about 0.5x10^{18}cm^{-3} and 1.0x10^{20}cm^{-3} for P5 and P9, respectively, when approaching the polysilicon surface. P9 has rather a high phosphorus concentration through the entire epi-layer (from the interface to the surface) resulting in an n^+n^+ structure. The high phosphorus concentration in the P509 solution and the difference of thermal process

for epitaxial growth can lead to this inconvenient phosphorus profile. In contrast, a graded n^+n structure is clearly obtained when using the P505 solid phosphorus source. Such graded n^+n structure is highly suited for the polycrystalline thin film silicon solar cells. Indeed, it induces a drift-field effect that as beneficial in the case of materials with low minority carriers diffusion length as it is the case for polysilicon films.

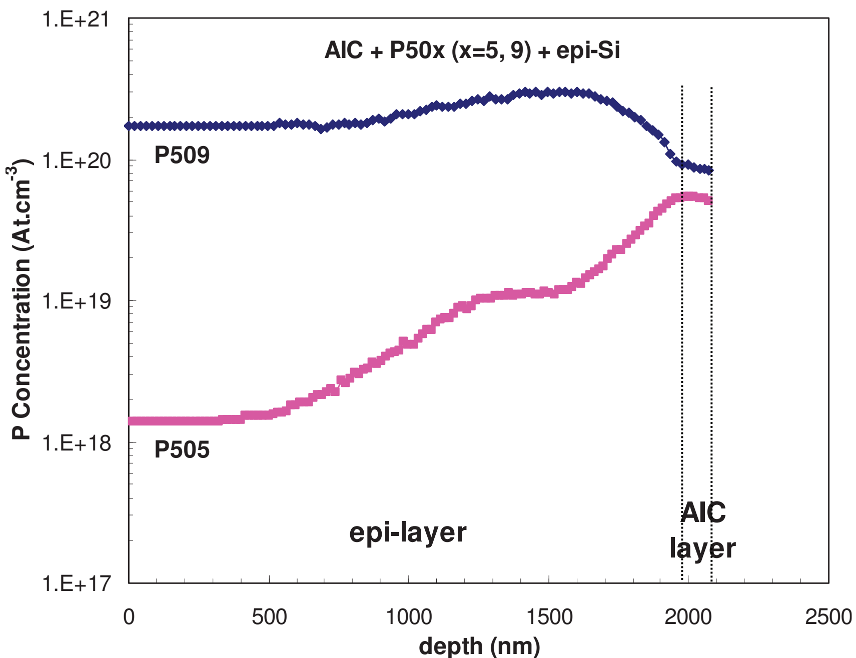


Figure 4.16: Depth profile of phosphorus measured by SIMS for n-type poly-Si formed by SPE on AIC poly-Si layer.

As a summary, the structural quality (crystallization, stress, etc.) of SPE-Silicon films depends on the recrystallization procedures that are temperature, duration and processing technique (RTP or CTP). Increasing the crystallization temperature raises the crystal nucleation rate and the crystal growth rate. Furthermore, longer annealing times show the enlargement of the grains at high temperatures due to the improved structural order of Si-Si network in the films. Rearrangement of the structure during recrystallization annealing may cause stress. However, RTP treated poly-Si films shows stress free behaviour while CTP treated poly-Si films have compressive stress. The amount of compressive stress strongly depends on the annealing time at high temperatures (~1000°C), which can be attributed to the difference in thermal expansion coefficient (α_T) between alumina substrate and silicon layer. Additionally, the time dependent stress gradient might arise from the change in the grain structure by annealing condition. Both high-temperature annealing for short time and lower-

temperature annealing for longer time reduce the stress level in poly-Si film. The crystal quality results deduced from micro-Raman technique is in agreement with the UV reflectance results. In particular, the UV reflectance spectra of alumina show low values that can be correlated to the surface roughness of the alumina substrate.

On the other hand, we have shown that phosphorus doping of epitaxial layer can be done successfully thanks to the exo-diffusion from AIC seed layer. However, the selection of the spin-on dopant is critical when looking for strongly graded n^+n structure.

4.1.2 Vapor Phase Epitaxy (VPE)

i) Principle of VPE

In contrast to low-temperature deposition for SPE, the epitaxial thickening by VPE is performed at high temperatures (>900°C) resulting directly in poly-Si layer without any ex-situ additional annealing as done for SPE. The VPE is a particular case of chemical vapor deposition that applies when the CVD is carried out on a layer of same composition than the desired epi-layer.

VPE or CVD is a process based on a solid material deposited from a vapor by a chemical reaction occurring on or in the vicinity of a normally heated substrate surface. Materials with different properties can be grown by varying the experimental conditions (such as substrate material, substrate temperature, composition of the reaction gas mixture, total pressure gas flows, etc.). In CVD, gaseous reactants are admitted into a reactor. Near or on a heated substrate surface, a chemical reaction of the following type occurs [42]:

Gaseous Reactants → Solid Material + Gaseous Products

Relatively high temperatures may be used during VPE. This means that various solid state reactions (phase transformations, precipitation, recrystallization, grain growth, for example) may occur during the process.

CVD processes are processed by chemical reaction schemes. However, use of overall CVD reactions enables a classification to be made. One of them is thermal decomposition reactions or pyrolytic reactions that a gaseous compound AX is thermally dissociated into A (a solid material) and X (a gaseous reaction product).

$AX(g) \rightarrow A(s) + X(g)$

Thermal decomposition reactions usually results in relatively pure coatings such as:

$SiH_4(g) \rightarrow Si(s) + 2\ H_2(g)$

Nucleation is the most important process in the deposition of materials, since the properties of a material are influenced by grain size, defects, etc… At the initial stages of growth, the nucleation on the foreign substrate determines the grain size and defects in the "first layer". In subsequent growth, secondary nucleation may occur with a generation of new grains, defects, inclusion of vapor species in pores, etc…

The reaction kinetics determines the rate at which a phase will form and whether its formation is limited by any step in the process. Figure 4.17 shows the seven mechanistic steps that have been hypothesized to occur during a vapor deposition process. These steps are:

1. Transport of reactant gases into the reaction chamber,
2. Intermediate reactants form from reactant gases,
3. Diffusion of reactant gases through the gaseous boundary layer to the substrate,
4. Absorption of gases onto the substrate surface,
5. Single or multi-step reactions at the substrate surface,
6. Desorption of product gases from the substrate surface, and
7. Forced exit of product gases from the system.

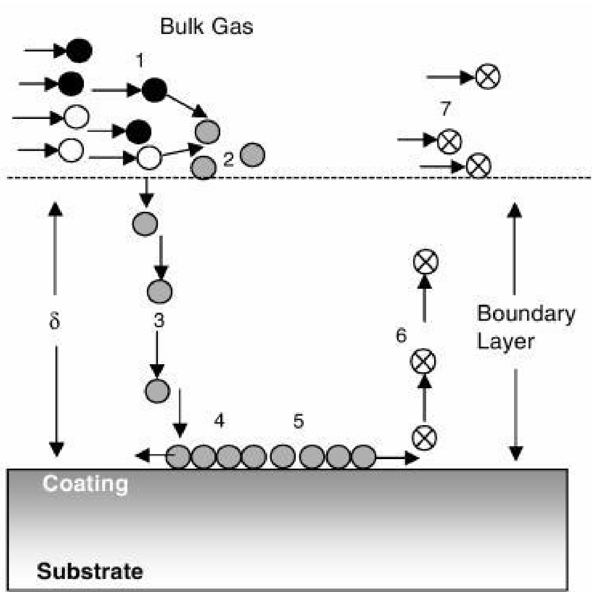


Figure 4.17: Schematic diagram of the mechanistic steps that occur during the CVD process [43].

In this model, the steps can be classified into two categories; mass transport and surface reaction steps. The slowest of these steps determines if the process is mass transport or surface reaction limited. At lower temperatures, the deposition rate is generally surface reaction limited. As the temperature increases, the surface reaction rate rises exponentially,

resulting in a mass transport limited because transport becomes the slowest step in the series of deposition steps.

The most important aspects of the deposition process are nucleation and growth. These phenomena can be understood in terms of the kinetics of formation of the nuclei of a solid phase by the clustering of atoms in a gas phase, followed by the interaction of further vapor atoms with the growing surface.

A nucleation during growth process can be explained in various steps as shown in Figure 4.18. Firstly, hydrogen and AX react with one another. The formed A atoms are adsorbed on the surface of the substrate. Afterwards, the adsorbed atoms may be desorbed from the substrate, diffuse into the substrate. In this case, probably an intermediate layer is formed or HX reacts with the formation of AX. Unstable aggregates of A atoms, embryos are formed after surface diffusion and direct impingement of A atoms from the vapor. Some of these embryos will grow at the expense of others and attain the status of stable A nuclei (supercritical A nuclei). An intact layer is formed after lateral growth and coalescence. Concentration of the adatoms determines the growth rate of the nuclei. Finally, the coalescence generates defects, i.e., grain boundaries.

The probability of generating new nuclei between the surface steps depends on the surface diffusion and the deposition rate (the impingement flux of the atoms). The adatoms have enough time for diffusion to reach the surface steps and be captured by them at a high temperature and a low deposition rate. However, a lower temperature and/or higher deposition rate results in shorter diffusion distances expediting clustering of adatoms between the steps resulting amorphous growth.

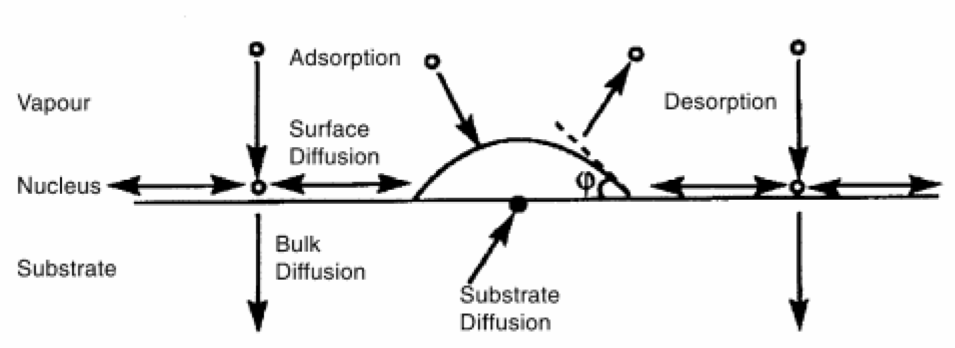


Figure 4.18: Various mechanistic pathways that can be followed by A [42].

The access to free surface sites is strongly affects the surface diffusion. In a CVD process, most of the surface sites are occupied by strongly adsorbed molecules. Layer growth

(no nucleation) can only be expected at high temperatures, low deposition rates, and low adsorption. This means long diffusion distances and the free incorporation of diffusing adatoms at the steps.

Certain time is required for one nucleus to become supercritical enough that is incubation time. After an incubation time, the nucleation rate becomes quite high ($\sim 10^{10} cm^2/s$). A saturation value of the nucleus density is achieved. The saturation value remains constant during relatively long period of time and is obtained at a stage when the mean diffusion distance is longer than half of the mean nucleus distance. Subsequently, the nuclei grow laterally and the nucleus density is constant until coalescence occurs. The saturation nucleus density is strongly dependent on the experimental conditions.

The effects of supersaturation and temperature on the structure of CVD materials are shown in Figure 4.19.

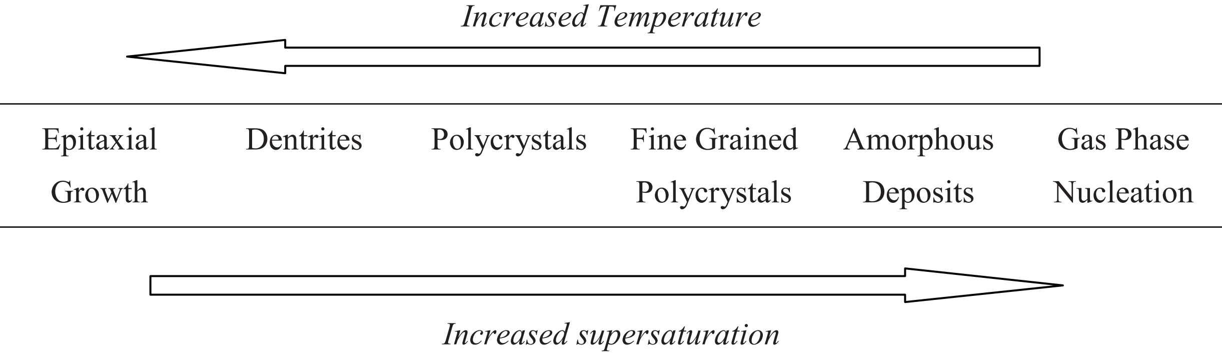


Figure 4.19: The effects of supersaturation and temperature on the structure of condensed materials [44].

Epitaxial growth is carried out at high temperature, as resulting poly-Si, in a reactor where precursor gases such as silane (SiH_4) or trichlorosilane ($SiHCl_3$) is used to deposit the silicon layer. The chemical reactions involved in silicon epitaxial growth and determining the kinetic of the silicon deposition are either

$$SiH_4(gas) \rightarrow Si(solid) + 2\ H_2(gas)$$

or

$$SiHCl_3(gas) \rightarrow SiCl_2(gas) + HCl(gas)$$

$$SiCl_2(gas) + H_2(gas) \rightarrow Si(solid) + 2\ HCl(gas)$$

If the deposition temperature is high enough (900-1250°C), the silicon atoms are not deposited in a random order. Rather, they position themselves in alignment with the Si atoms at the substrate surface, such as AIC poly-Si seed layer in our case.

Low pressure chemical vapor deposition (LPCVD) system with silane precursor at 1000°C or atmospheric pressure chemical vapor deposition (APCVD) system with trichlorosilane precursor gas at ~1100°C are used to deposit polycrystalline silicon layer that is the composite of silicon crystallites separated by grain boundaries and with the diameter range of 0.1-60µm.

ii) Experimental procedure of VPE on AIC layers

For this experiments, p-type and n-type AIC layers formed on alumina substrates (Al_2O_3) coated with a flowable oxide (FOx-25 from Dow Corning) [45] or glass ceramics coated with SiN_x. The n-type AIC poly-Si layers were formed by following the same procedures used for the SPE technique as described above.

The thickening of the AIC layers was carried out at 1000°C in a low pressure chemical vapor phase reactor (LPCVD) or rapid thermal atmospheric pressure chemical vapor deposition (RT-APCVD) reactor. For the latest, the samples were heated by 12 tungsten halogen lamps from topside through a double quartz window cooled by oil; trichlosilane ($SiHCl_3$) gas diluted in hydrogen was used as a silicon precursor gas. For LPCVD system, a conventional tube furnace was used where silane (SiH_4) diluted in H_2 was the precursor gas. The detailed description and the schematic diagrams of these CVD systems are discussed in details in Appendix A. The growth rate is of ~65nm/min and ~1.5µm/min for LPCVD and RT-APCVD systems, respectively. The thickness of deposited layer is between 2-6µm depending on the epitaxy system.

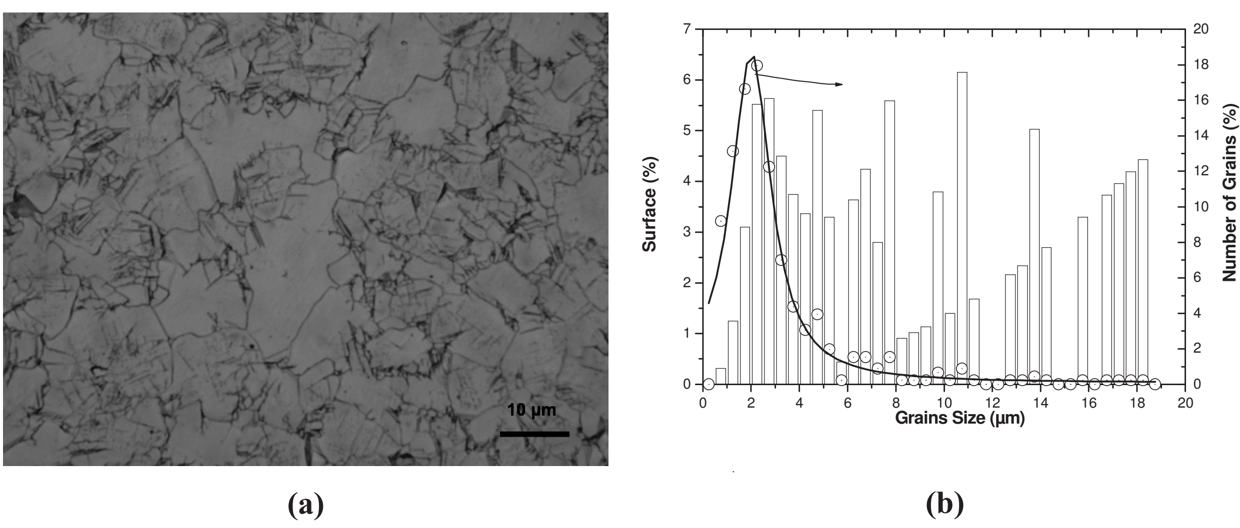
In the case of p-type AIC layers, B_2H_6 gas was introduced during the epitaxy process. For thickening the n-type AIC layers, no intentional doping gas was used during the epitaxy step. In this case, phosphorus exo-diffusion into the epi-layer occurred during the silicon without additional annealing. Thus, n-type poly-Si absorber layers were formed on the AIC layer. Consequently, an n-type poly-Si absorber layer is formed on AIC layer.

Surface morphology analyses of epitaxial grown poly-Si were carried out by optical microscope and electron backscattering diffraction (EBSD). The impurity concentration profiles in the resulting structures were analyzed by secondary ion mass microscope (SIMS).

iii) Structural analysis of the VPE-Si layers

In the following we present the morphology and structural properties of the epitaxial grown silicon on the n-type AIC layer. The results are the same on p-type AIC layer as far as the grain size and inter and intra-grains defects are concerned.

Figure 4.20a shows the optical microscope view of a 2µm thick epitaxial silicon film grown on the n^+-type Si seed layer on alumina/FOx in the LPCVD reactor. The image area is 89x67µm^2. The polycrystalline silicon layer was polished and subjected to Secco etching to reveal the grain boundaries and defects. The figures show that the Si adheres perfectly on the substrates, thanks to the FOx that reduces the surface irregularities and open pores at the starting bare surfaces. Home-made software was used to extract the average grain size and distribution from the optical images, assuming circular grains. From this procedure, we obtained the grain size distribution shown in Figure 4.20b [46]. The distribution (open dots), i.e. normalized frequency of grains, can be well approximated by a log-normal distribution [47,48]. The average grain size is found to be about 10µm. More importantly, the surface is covered by grains of a certain size because this is indirectly indicative of the density of grain boundaries. The covered area (in percentage) versus grain size is also plotted in Figure 4.20b (shown as bars) [49]. From this analysis about 65% of the total surface is covered by grains that have a diameter of more than 5µm.



(a) **(b)**

Figure 4.20: (a) Optical microscope surface view of n-type poly-Si deposited on FOx-coated alumina, (b) grain size, grain size distribution and area distribution extracted from optical image.

The grain size is only one of the parameters controlling the carriers transport in the polysilicon films and therefore the photovoltaic performances. The inner-grain structure, the

grain boundaries, and the grain orientation are of prime importance as well. Therefore we used the EBSD technique to investigate more deeply the crystallographic quality of the poly-Si on alumina and glass-ceramic substrate.

Figure 4.21a shows the crystalline orientation mapping image for the epitaxial poly-Si films formed by CVD at 1000°C on AIC seed layer on FOx-coated alumina substrate formed at 500°C for 4h. Different colors correspond to different crystalline orientations: graded red color highlights silicon grains with an orientation that differs less than 15° from the <100> parallel to the surface, while the blue and green colors corresponds to an orientation deviation of less than 15° from the <111> and <101>, respectively. Black points appear as defects in AIC layer. Orientation map is also used to evaluate the grain size. The grain size can be estimated by summing over the number of data points in each grain. The grain diameter is deduced by assuming a circular disklike geometry of similar area. The grain size distribution as extracted from EBSD is shown in Figure 4.21b. The distribution of the grain size is relatively homogenous (σ=3.7µm), which means the diffusion limited grain growth [50] for epitaxy of poly-Si on AIC seed layer during crystallization. The poly-Si absorber layer exhibits a ~6.9µm average grain size. This result is consistent with that of the underlying AIC poly-Si seed layer on alumina substrate that has an average grain size of 6.0µm.

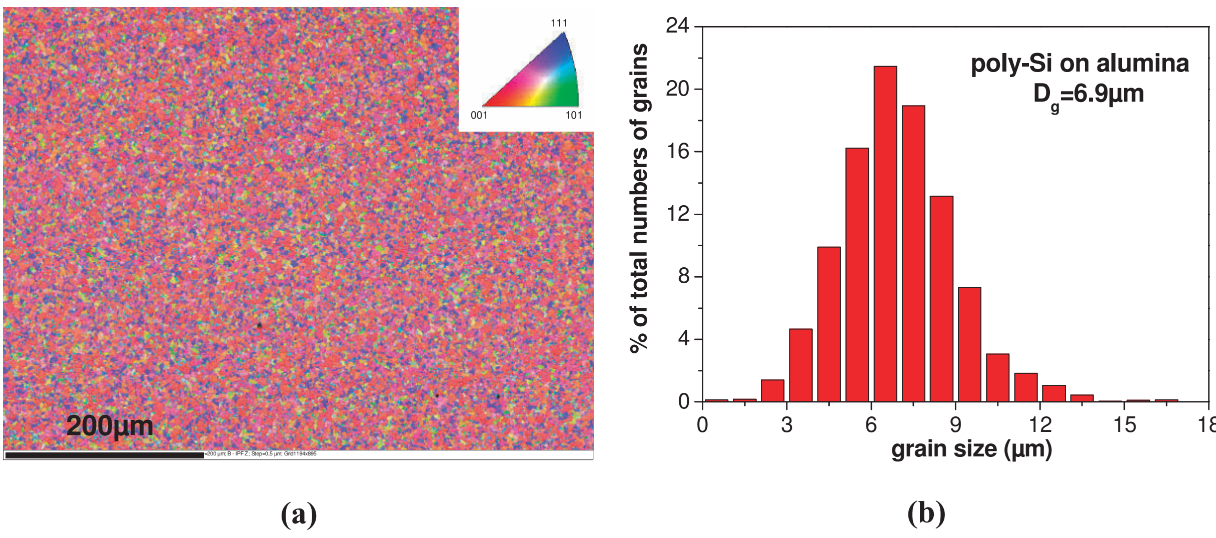


Figure 4.21: (a) Orientation mapping analysis, and (b) grain size distribution of epitaxial poly-Si layers on alumina.

To be more quantitative, the distribution of analyzed pixels as a function of deviation angle (θ) is plotted in Figure 4.22a. The deviation is accumulated by segments of 5° compared to the <100> orientation. In this graph, the minimum deviation (5°) means a fully <100>

oriented layer while the maximum deviation of 54.7° corresponds to the (111) plane. The majority of grains (64.6%) in these poly-Si films have an orientation deviation between 5 and 25°, which is indicative of <100> (5-25°) oriented grains. Besides, the distribution of <110> (30-45°) and <111> (45-55°) orientation for films are 17.1% and 18.3%, respectively. It means that the preferred orientation of poly-Si epi-layer formed by CVD system by VPE technique is <100>. This result is in agreement with the X-ray diffraction analysis reported in Figure 4.8 for epitaxial poly-Si formed by SPE technique, which confirms a tendency to preferential <100> oriented grains for poly-Si layers using seed layer approach. However, Bisaro et al. [51] suggested that the <110> texture corresponds to layers deposited directly in crystalline state.

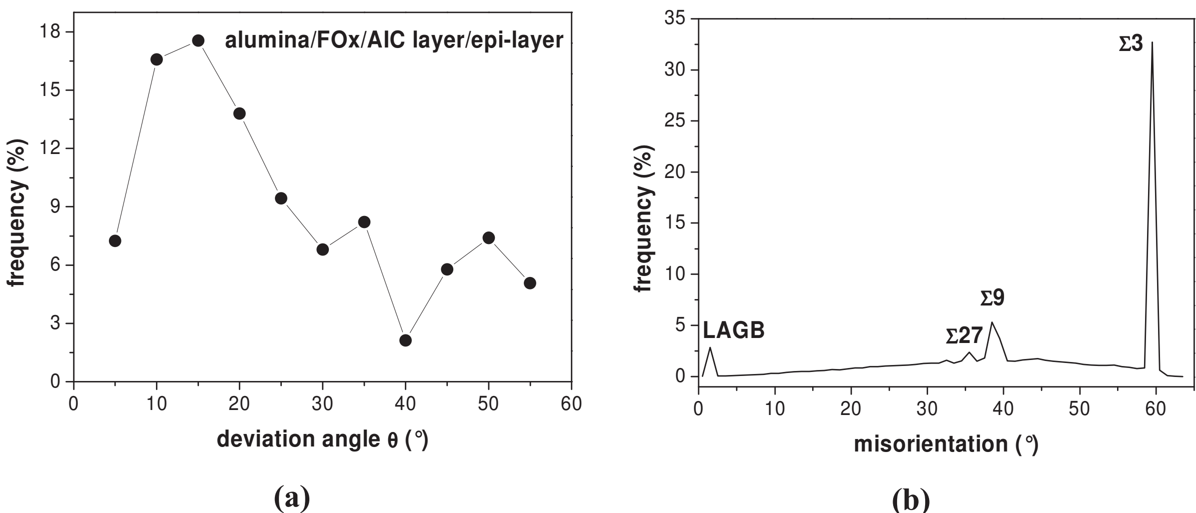


Figure 4.22: (a) Deviation angle from <100> fiber texture, and (b) distributions of coincident site lattice boundaries for the poly-Si layer deposited by CVD at 1000°C on FOx-coated alumina using AIC seed layer approach.

Besides the grain size and orientation, the EBSD micrograph reveals that some of the grains appear to contain subgrain-structures and numerous defects (Figure 4.21a). Identification of these defects was possible. Figure 4.22b shows that the main crystallographic defects present in the continuous poly-Si layers are the low-angle grain boundary (LAGB, angle < 2°) and the coincident site lattice boundaries are mainly twin boundaries of first order (Σ3) and less proportion in the second order (Σ9), and third order twins (Σ27). The high fraction of high-angle boundaries around 60° in poly-Si is due to the existence of Σ3 boundaries that has around 33% distribution. Such defects are present irrespective of the deposition temperature and substrate. Careful attention should be given to the fact that those types of defects are intra-grain defects, therefore, the grain size determination should take that

into account. Thus, assuming that a colored zone corresponds to a grain, the micrograph of Figure 4.20a clearly shows that the grains are slightly smaller than those determined by the optical microscopy. Average grain size reduces from ~10µm to ~6.9µm analyzing by EBSD technique instead of optical microscope images.

On the other hand, reports in the literature reveal that coherent first-order (Σ3) twins are electrically inactive. Higher order twins and faceted twin boundaries, e.g., in most cases, coherent first-order twins with incoherent segments are only weakly electrically active [52,53]. A secondary dislocation network need not, but frequently does, lead to electronic levels in the band gap and thus, to electrical activity in terms of minority carrier recombination and potential barriers. Random grain boundaries are generally electrically active [54]. Thus these highly disordered grain boundaries, if not neutralized, could be detrimental for electronic transport in silicon solar cells devices. Hydrogen passivation of such defected silicon layers might be needed. Hydrogenation effect on solar cells parameters will be discussed in coming parts.

Comparative study is done on glass-ceramic (GC) used poly-Si films formed by LPCVD system. As discussed in Chapter 3, using the glass-ceramic substrate instead of alumina results in a significant enhancement on the average grain size. For this aim, epitaxy was performed on AIC seed layer that was formed at 500°C for 6h. Figure 4.23 shows the orientation map (a), grain size distribution (b) and deviation angle from <100> (c) deduced from EBSD analysis for epitaxial poly-Si film on glass-ceramic substrate. The color code corresponding to grain orientation is depicted as an inset Inverse Pole Figure. As shown Figure 4.23b, the average grain size becomes 11.21µm using glass-ceramic, which is bigger than that of using alumina (D_g=6.9µm). Additionally, this grain size result is convenient to the average grain size of AIC seed layer on glass-ceramic (D_g=12.07µm). Using quite smooth glass-ceramic substrate is also improving the quality of epitaxial layer. Concerning the preferred orientation, more quantitative study was done using deviation angle from <100> plotting, as shown in Figure 4.23c. The majority of grains (62.8%) is orientated to <100> (5-25°) while 21.3% and 15.8% is for <110> (30-45°) and <111> (45-55°) orientations. According to these results; it is revealed that the prefer grains orientation for epi-layers is <100>, similar to that of the underlying seed layers formed on glass ceramic and alumina.

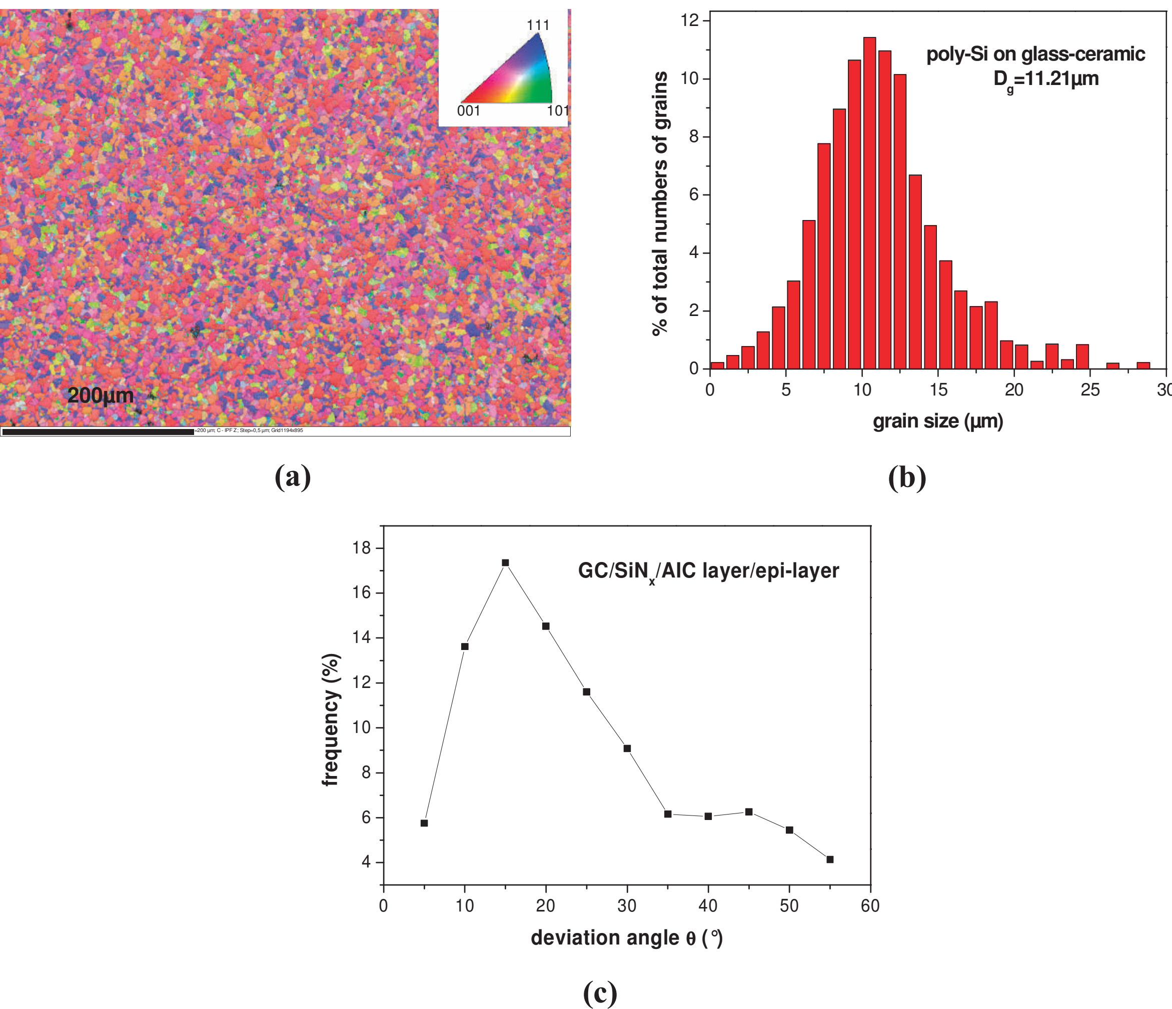


Figure 4.23: (a) Orientation mapping analysis, (b) grain size distribution, and (c)deviation angle from <100> fiber texture for the poly-Si layer deposited by CVD at 1000°C on SiN_x-coated glass-ceramic substrate using AIC seed layer approach.

Like for SPE grown samples, micro-Raman analysis was also performed to investigate the crystallization and especially, intrinsic stress of poly-Si films grown by VPE. As discussed above, we depict that the poly-Si films formed by SPE technique has recrystallization annealing temperature and time dependent compressive stress that can mainly attributed to rearrangement of structure from amorphous to crystalline. However, VPE technique has a quite different epitaxial meaning due to the high-temperature (1000°C) process that results in poly-Si directly without ex-situ annealing. Figure 4.24 shows the Raman spectrum of poly-Si filmed thickened by VPE on AIC layer formed on alumina and glass-ceramic substrates. As shown, for both alumina and glass-ceramic used poly-Si films there is a fully crystallization with the full width at half maximum (FWHM) value of 6.0cm^{-1} that is comparative with the value of sc-Si (5.9cm^{-1}). Quite sharp and symmetric Raman peaks are obtained without any

left shoulder that means absence of microcrystalline silicon structure. As for the stress analysis from the micro-Raman data, LPCVD thickened poly-Si films exhibit no stress, as the peak position appeared at 520.0cm^{-1}, which is a signature of sc-Si.

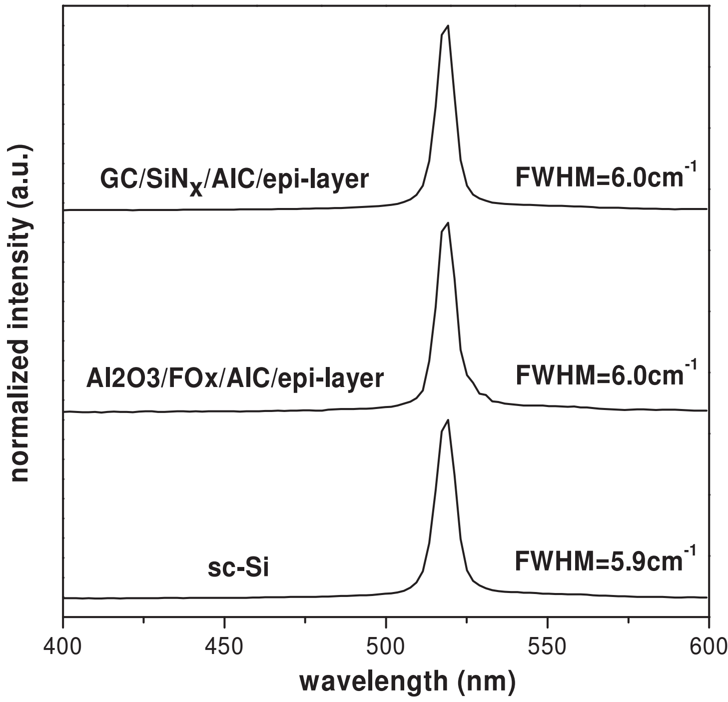


Figure 4.24: Raman spectrum of poly-Si film thickened by VPE on AIC layer. A Raman spectrum of sc-Si is shown as a reference.

Although, larger average grain size is observed for epitaxial poly-Si films formed by SPE technique, lack of stress for VPE technique gives an advantage for higher quality solar cell fabrication. Due to this reason, the solar cells are formed using only high-temperature processed VPE technique.

As a summary, VPE technique supplies directly poly-Si film without any additional annealing that thanks to the high temperature epitaxy processing. Grain size results are consistent with those of the underlying AIC poly-Si seed layer either on alumina or glass-ceramic. Using glass-ceramic substrate instead of alumina results in a significant enhancement on the average grain size of epitaxial layer as deduced for AIC seed layer. The main crystallographic defects present in the continuous epitaxial polysilicon layers are the LAGB and CSL boundaries consisting of twin boundaries of Σ3, Σ9 and Σ27 while the majority of crystallographic defect is Σ3, as convenient to the defect structure of AIC seed layer. Although smaller grain size is observed for VPE-Si, defect free, fully crystallized and

continuous poly-Si films are acquired using VPE, which are the advantages compared to SPE technique.

iv) Dopants distribution in VPE film on AIC layers

Due to the different epitaxial process mechanisms between SPE and VPE, the doping analysis must be investigated also for the VPE process. For this purpose, VPE growth was formed for different times by RT-APCVD system at 1050°C on n^+-type AIC layer. It results in epi-layers with different thicknesses.

We have first analyzed the sheet resistance of the resulting epi-layer on n-type AIC using the four-point probe method. Let's remind that the sheet resistance value of the 0.2µm thick n^+-type seed layer was about 20Ω/sq. Table 4.2 gives the sheet resistance measured after the epitaxy and subsequent annealing. Due to the quite short epitaxy time, an additional annealing process was performed after epitaxy. Phosphorus exo-diffusion into the epi-layer starts during the silicon deposition. The additional annealing process performed at 1000°C for 2 hours in a tube furnace under nitrogen ambient to complete the exo-diffusion.

Thickness of epi-layer (µm)	$R_\square$, after after epitaxy (Ω/sq)
1.5±0.1	414±25
3.6±0.1	65±10
2.5±0.1	91±10

Tablo 4.2: An overview of sheet resistance ($R_\square$) values for various conditions of polysilicon.

Consequently, an n-type poly-Si absorber layer was formed on AIC layer. Sheet resistance values from 400 to 65Ω/sq were obtained. Thinner is the epi-layer higher is the sheet resistance. The distribution of phosphorus atoms within the layer as well as the final surface concentration is more likely different for the grown epi-layers. The n-type doping type has been confirmed as well. These results indicate that the heavily phosphorus doped AIC layer has served as a doping source for the absorbing layer grown by vapor phase epitaxy.

The phosphorous concentration profile for the 3.6µm thick epitaxial film grown by RTCVD on the n^+ AIC layer, as deduced from SIMS analysis is shown in Figure 4.25. The phosphorus concentration in the AIC layer exhibits a plateau at about 2-3×$10^{19}$$cm^{-3}$. This value is lower than that calculated from resistivity data as a result of the thermal exo-diffusion

of phosphorus during the epitaxy step and subsequent thermal annealing. The observed graded distribution is indicative of the exo-diffusion of the phosphorus towards the epi-layer, followed by an almost constant concentration at about $10^{17}cm^{-3}$ when approaching the polysilicon surface. As a result, a $n^{+}n$ structure is clearly reached using this process. Once more, such a graded profile is of interest to solar cells structure, since the electric field drift driven from it is favourable for a higher minority carriers' diffusion length [55].

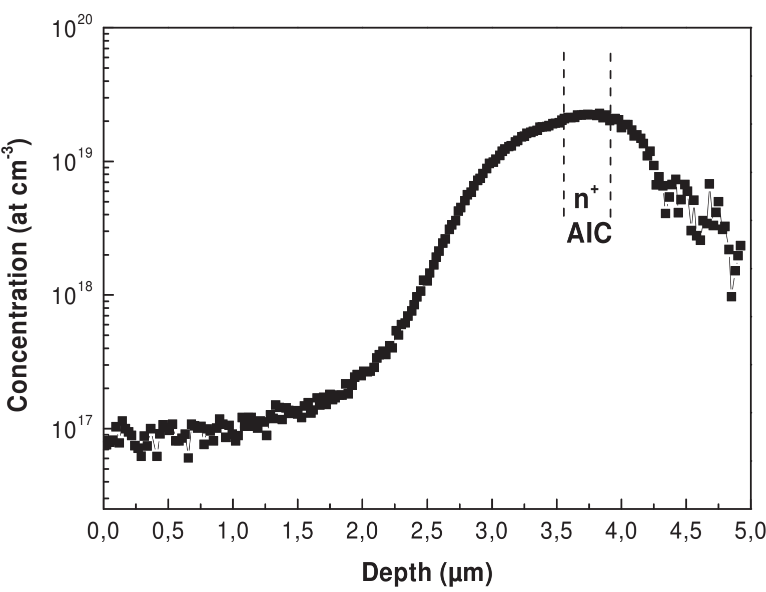


Figure 4.25: Depth profile of phosphorus for n-type poly-Si formed by RT-APCVD.

The phosphorus distribution in an epitaxial film grown on an n^{+} type AIC layer in the LPCVD reactor was also measured. No doping gas was added during epitaxy process at 1000°C on n^{+}-type AIC seed layers due to the lack of a P feeding line in LPCVD system, resulting in n-type absorber layers without real doping control. No post thermal annealing was applied because of the longer deposition time in LPCVD processing (i.e., 30min for 2µm epitaxial thickening). Indeed, the growth rate in the LPCVD system was around 65nm per minute, which gave sufficient time for the P out-diffusion from the seed layer to take place. Figure 4.26 shows SIMS results of grown $n^{+}n$ structure. The n^{+} AIC layers can be distinguished easily due to its quite high phosphorus concentration level of $\sim 1.3\times10^{20}cm^{-3}$. A gradually decreasing doping profile is formed through the entire epitaxial Si layer, resulting in an $n^{+}n$ structure. Within a distance of about 1µm from the front side of the cell, the P concentration is in the range of 10^{17}-$10^{18}cm^{-3}$. In this range, light-induced charge carriers are considered to be collected effectively. Such graded doping profile can be advantageous for the cell efficiency, as it gives rise to the gradient in the quasi-Fermi levels. The minority carriers

(holes) are then subjected to drift in the direction of the junction, which can increase the effective diffusion length.

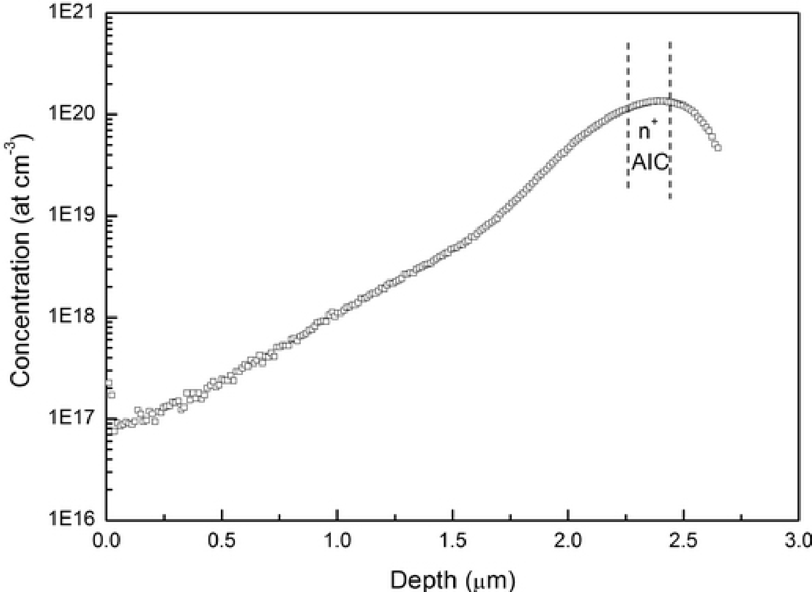


Figure 4.26: SIMS depth profile obtained on n-type solar cells using LPCVD system.

As a summary of this text, the exo-diffusion of phosphorus from the n$^+$ type AIC layer occurs during vapor phase epitaxial thickening using either RT-APCVD or LPCVD systems and resulting in graded n$^+$n structures. In fact, the out-diffusion of phosphorus can happen simply during epitaxy by LPCVD due to sufficient long epitaxy time (30min), while it requires an additional annealing at 1000°C after epitaxy in the RT-APCVD system.

4.2 THIN FILM SOLAR CELLS BASED ON AIC SEED LAYER

4.2.1. Important Steps for Polysilicon Solar Cells

Prior to form solar cells on AIC/epi based structure, we have studied different steps that are important for solar cells. Thus, it is well known that the electronic properties of the polysilicon based solar cells can be strongly improved by hydrogenation. We will present below the effect of plasma hydrogenation on poly-Si made by direct CVD on the open circuit voltage. On the other hand, because of the low minority carrier diffusion length in the poly-Si solar cells, the emitter structure and cell architecture are very important for carrier collection. We will compare cell properties with homojunction (HMJ) and heterojunction (HTJ) emitters as well as mesa and interdigitated contact cells.

i) Plasma hydrogenation

Formation of polycrystalline silicon (poly-Si) thin films on foreign substrates (glass, foils, and ceramics) by physical or chemical deposition techniques results on large-grained silicon (0.5-100µm) materials, and therefore to a large density of grain boundaries. Thus, the minority and majority carrier transport properties in such materials are mainly controlled by the electrical activity of these grain boundaries [56,57]. Getting good energy conversion efficiency from such materials needs either to enlarge the grain size or to neutralize the electrical activity of the grain boundaries. The latter is commonly achieved by incorporating atomic hydrogen either directly by immersion in a plasma hydrogen atmosphere or by diffusion of hydrogen from a top layer that serves as a source. For common solar cells, such as multicrystalline silicon-based solar cells, the most widely used hydrogenation technique employs a hydrogen-rich silicon nitride (SiN_x:H) layer deposited by PECVD to simultaneously provide an antireflection coating, surface passivation and, following hydrogen diffusion into the silicon during the contact firing step, bulk passivation [58]. For polysilicon materials, most of the studies are concerned about the hydrogenation of p- or n-type silicon and monitoring the majority carriers' properties (i.e. film resistivity). But, a few amount of research work is focused on the effects of direct or indirect hydrogenation on real p^+pn^+ cell structures and addressing their minority carriers related parameters through the open circuit voltage and short circuit current.

We have investigated the effect of plasma hydrogen treatment of polysilicon films by immersion in a dense hydrogen remote-plasma mode involving an electron cyclotron resonance (ECR) system [59]. The polysilicon films used for this study are obtained by direct CVD deposition. We speculate that the polysilicon formed by AIC and epitaxy will behave similarly. The plasma hydrogenation method presents many advantages, such as a low hydrogen consumption (pressure ~ mTorr) and a high flux of atomic hydrogen ions, H^+, due to acceleration of ions toward the substrate by electrostatic fields in the plasma. Thus, because of this acceleration, ions reach the surface with a large kinetic energy making them more likely to adsorb on the surface, once they reach it. Hydrogenation at moderated temperature (<500°C) induces hydrogen diffusion and therefore the defect passivation. The drawback of these energetic ions might be an etching of the surface and/or the generation of subsurface defects and surface damage that can be harmful to the poly-Si-based solar cells.

In this study, different operating parameters (substrate temperature, ECR power and RF dc bias voltage, hydrogen or SiH_4/NH_3 flow) were varied. The main objectives are an efficient defect passivation and a slight surface etching. The passivation effectiveness is

witnessed through the open-circuit voltage and short circuit current of mesa-structures on p^+pn^+ poly-Si films (fabricated by RT-APCVD), while the etching process is monitored via the sheet resistance of the n^+ emitter region.

Figure 4.27 plots the open circuit voltage of hydrogenated p^+pn^+ mesa cells versus samples temperature in the plasma system. The data of curve A corresponds to fast removing of the samples from the plasma reactor chamber, while the curve B are data for samples, which were cooled in the reactor chamber down to 150°C and then taken out. The aim of such experiments was to freeze maximum of hydrogen atoms in the silicon matrix.

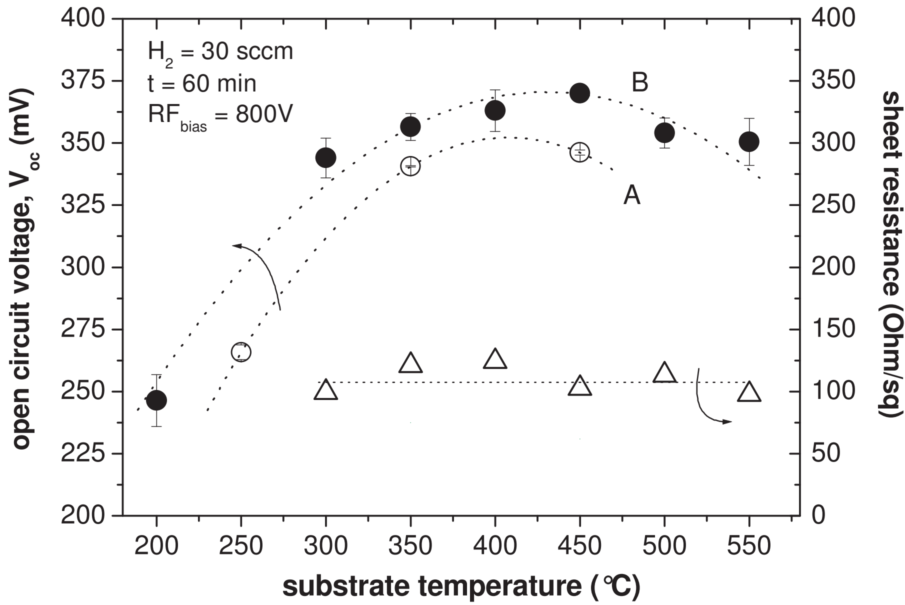


Figure 4.27: Open circuit voltage and measured emitter sheet resistance versus hydrogenation substrate temperature of p^+pn^+ Si mesa structure. Curve A corresponds to fast cooling after hydrogenation while curve B corresponds to slow cooling.

According to previous reports, hydrogen ions are positive in p-type doped silicon and negative in heavily n-type doped silicon (negative-U impurity) [60,61]. The hydrogen atoms entering the sample during the hydrogenation are immediately converted to H^- by reaction with electrons given by the n-type dopant in the n^+ region. The negatively charged hydrogen atoms diffuse slowly in the highly doped regions because the diffusion mechanism involves an energetically unfavourable neutral transition state [57].

For both operating conditions, the open circuit voltage increases drastically from 130-140mV before hydrogenation up to 350-380mV after plasma hydrogenation at 450°C. This is indicative of an efficient passivation by hydrogen atoms of grain boundaries and intra-grains

(*dislocation*) defects in our fine grained poly-Si films. Above 500°C, a decrease in V_{oc} is observed, resulting from a competition between in-diffusion and out-diffusion of hydrogen into silicon. Comparison of curves A and B of Figure 4.27 shows that faster cooling is not favourable to higher V_{oc}'s. Slower cooling could be favourable for better arrangement of hydrogen atoms into the silicon matrix leading to a slightly higher V_{oc} values.

Another important operating parameter for plasma hydrogenation is the RF dc bias. Figure 4.28 depicts the measured V_{oc} after plasma hydrogenation at 450°C under different RF bias. The RF bias has two major effects: higher biases lead to more energetic hydrogen radicals that can penetrate more deeply in the polysilicon layer and therefore passivate more dangling bonds. It results in larger V_{oc} values up to 370mV at 600V. Further increase of the RF bias up to 1000V diminish the V_{oc} because such high bias causes more collisions at the polysilicon surface, resulting in the formation of Si-H complexes that leave the material and induce an etching process of the emitter region [62]. This is further confirmed by the sheet resistance values of the emitter measured after hydrogenation as shown in Figure 4.28. The defects formation and etching step seems to increase gradually with the increase of the RF bias voltage. An enhancement of the sheet resistance by almost a factor 2 is observed. A compromise in the operating parameters of the plasma hydrogenation is therefore needed to reach high quality bulk materials with a minimum surface degradation.

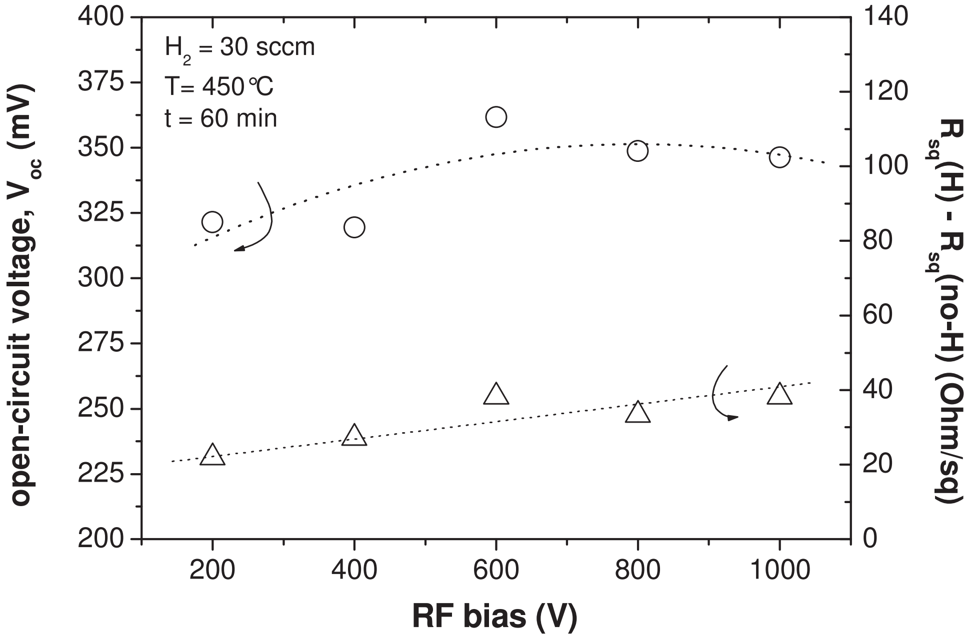


Figure 4.28: Evolution of open-circuit voltage and sheet resistance versus RF dc bias of p^+pn^+ poly-Si based cells measured after plasma hydrogenation. The hydrogenation was carried out at 450°C for 60 min.

After epitaxial growth of the samples (p^+p) were hydrogenated in a direct plasma-enhanced CVD (PECVD) system in IMEC. Just before loading, the samples are dipped in an HF-solution (2%) to remove the native oxide. This oxide layer prevents the H atoms to penetrate in the layer and might lead to a bad passivation [63]. After loading of samples, the system is evacuated and the temperature is stabilized for 10min in flowing hydrogen. The plasma is ignited at $77mW/cm^2$ and 2Torr after which the power and the pressure are immediately lowered to $62mW/cm^2$ and 1Torr. The hydrogenation temperature is around 400°C at which the hydrogen is relatively mobile. To avoid too much out-diffusion of hydrogen during sample unloading, the layers are cooled down in the system while keeping the plasma on [64]. After cooling down, the plasma is switched off and the samples are unloaded.

The influence of plasma hydrogenation is investigated on cell performance for as-grown polysilicon solar cells with a heterojunction emitter (0.3μm (p^+) / 1μm (p), $3\times10^{16}cm^{-3}$ doped). Table 4.3 summarizes the cell parameters depending on the hydrogen passivation treatment. The hydrogenation is performed for a few seconds at 385°C and for 30min during cooling down by direct PECVD system in IMEC. Hydrogenation has a significant effect on V_{oc} that increase from 417.0 to 511.5mV just after hydrogenation. Additionally, direct-plasma hydrogen treatment also enhances J_{sc} and *FF*, resulting in the cell efficiency by a factor of 2.4. Hydrogenation passivated the defects at grain boundaries and improves the cell quality.

Passivation	J_{sc} (mA/cm^2)	V_{oc} (mV)	*FF* (%)	*Efficiency* (%)
No	6.6	417.0	57.7	1.6
Yes	11.3	511.5	66.1	3.8

Tablo 4.3: Influence of hydrogenation on heterojunction, as-grown polysilicon solar cells [65].

Figure 4.29 shows external quantum efficiency (EQE) curves for both polysilicon layers with and without hydrogenation treatment. The hydrogenation of the heterojunction improves both the maximum EQE (from 50% to 60%) and the response at longer wavelengths (>400nm). The plasma hydrogenation passivates the defects at grain boundaries. Due to passivation, more e^-/h^+ pairs generated deep in the layer can be collected by grain boundaries without too much recombination [65]. The effective diffusion length (L_{eff}) can be calculated by using Taretto's method [66]. As a result, hydrogenation improves L_{eff} from 0.5μm to 1.4μm, explaining the higher EQE.

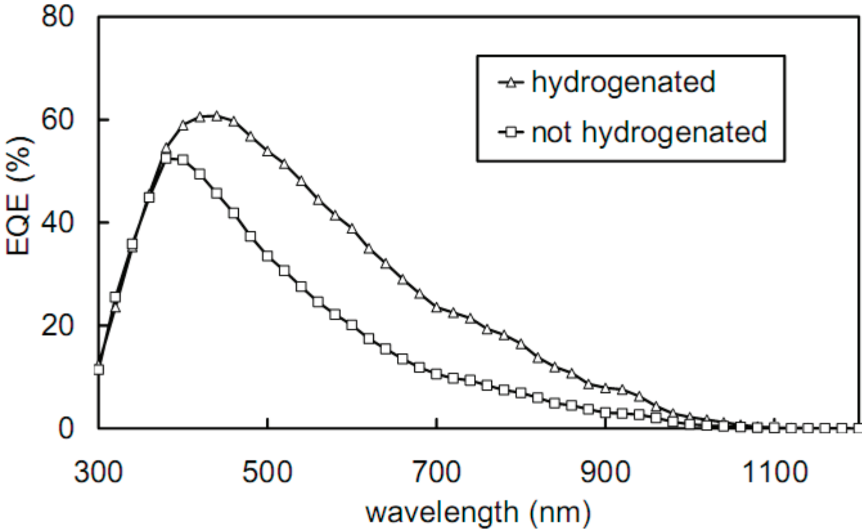


Figure 4.29: Influence of direct-plasma hydrogenation on EQE of polysilicon cells with a heterojunction emitter [65].

As a summary, we have shown that plasma hydrogenation of polysilicon based mesa cell structure is efficient to neutralize the electrical activity of the grain boundaries and induces defect passivation. We have demonstrated that substrate temperature and RF bias voltage during plasma hydrogenation have great influence on the open circuit voltage of the mesa cells. An optimal substrate temperature of 450°C is found. For temperatures above 500°C, hydrogenation process losses its effectiveness due to a competition between in-diffusion and out-diffusion of hydrogen within the silicon layer. Additionally, slower cooling could be favourable for better arrangement of hydrogen atoms into the silicon matrix leading to a slightly higher V_{oc} values. Another important operating parameter for plasma hydrogenation is the RF dc bias. Enhancement of RF bias up to 600V gives rise to larger V_{oc} values while further increases diminish the V_{oc}. The defects formation and etching step seems to increase gradually with the increase of the RF bias voltage. On the other hand, hydrogenation passivates the defects at grain boundaries and enhances the maximum EQE (from 50 to 60%), the response at longer wavelengths (>400nm), L_{eff} (from 0.5µm to 1.4µm) and the cell efficiency by a factor of 2.4.

ii) Homojunction (HMJ) versus heterojunction (HTJ) emitter based solar cells

To fabricate thin-film solar cells, an n^+ emitter created on p-type base layer by the conventional diffusion of phosphorous at high temperature (named homojunction emitter, HMJ) is usually used. Another possibility to create an emitter is by depositing thin amorphous silicon layers, forming a heterojunction emitter (HTJ). Heterojunction solar cells can

potentially lead to very high efficiencies, as demonstrated on high lifetime wafer material by Sanyo with their HIT^{TM} (Heterojunction with Intrinsic Thin layer) solar cell [67]. An important advantage of a heterojunction emitter is that its formation is carried out at relatively lower temperature (<250°C) in contrast to traditional P-diffused emitters (>850°C). For poly-Si TF solar cells, it was shown that the use of a heterojunction emitter prevents preferential P-diffusion along the grain boundaries and leads to much higher V_{oc} values than the use of diffused emitters [68].

We have prepared conventional diffused homojunction emitter (HMJ) and a low-temperature polycrystalline silicon-amorphous silicon heterojunction (poly-Si/a-Si:H) emitter (HTJ) on polycrystalline silicon deposited by thermal CVD and compared their photovoltaic performances. The two structures are schematically shown in Figure 4.30.

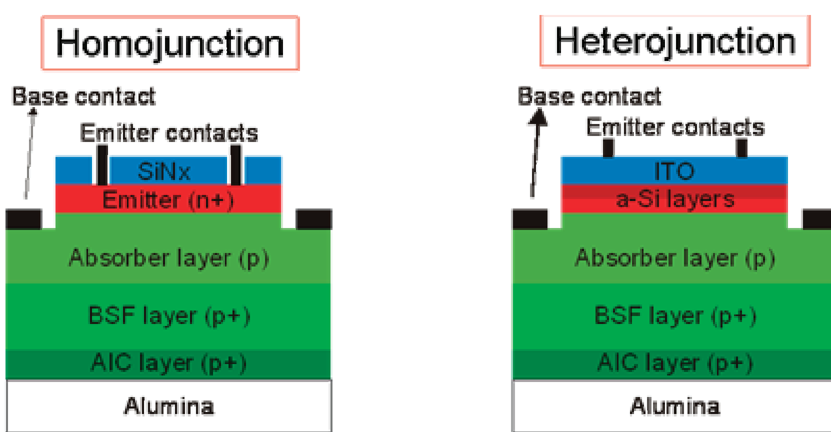


Figure 4.30: Cross-section of used structure for homojunction and heterojunction emitter polysilicon mesa cells (not in scale).

In the HMJ process, the emitter was formed by phosphorus diffusion from a spin-on dopant oxide source (P509, Filmtronics) at 850°C for 30min or by phosphorus diffusion from a P-doped pyrolithic oxide at 860°C for 10min. The resulting sheet resistance is around 80-100Ω/sq. After the diffusion, the samples are subject to plasma hydrogenation in a plasma-enhanced chemical vapor deposition system (PECVD) at 400°C for 30min. This passivation is followed by the deposition of a SiN_x:H anti-reflective coating in the same system. In contrast to the HMJ process, the hydrogenation in the heterojunction process is done prior to the emitter formation that consists of the deposition of a thin intrinsic amorphous silicon layer followed by the deposition of an n^+ doped a-Si:H layer. Both a-Si layers are deposited by PECVD at 180°C [69]. Since hydrogen has a low diffusivity at such temperature in poly-Si, hydrogen is not expected to come out during the amorphous silicon deposition. The thickness

of the heterojunction emitter is around 15nm. Otherwise, in order to attain a higher V_{oc}, it is very important to have high-quality intrinsic a-Si layers and excellent a-Si/c-Si interfaces. For this reason, the poly-Si surface must be cleaned by RCA before hydrogenation; and the HTJ emitter formation must be followed simultaneously just after hydrogenation without exposure to air. To minimize the reflective losses and to provide a conductive channel, an indium thin oxide (ITO) layer was deposited on top of the emitter.

As solar cell test structure, we used the side-contacted mesa process because it is easier to implement and allows quicker feedback. Access to the base and BSF was possible by plasma or wet chemical etching around the cell, thus forming a $1\times1cm^2$ mesa cell. Al base contacts and Ti/Pd/Ag top contacts were formed by e-beam evaporation in combination with photolithography.

Figure 4.31 compares the best illuminated current-voltage (*I-V*) characteristics of mesa cells with a heterojunction (a-Si/poly-Si) emitter and a diffused homojunction emitter. The metal contacts covered around 6% of the cell area for both cell types. The highest V_{oc} we obtained so far on polysilicon on alumina using a heterojunction emitter is about 500mV versus 394mV using a diffused emitter. The difference in V_{oc} is caused by a more efficient hydrogenation and a lower recombination in the space charge region for HTJ [70].

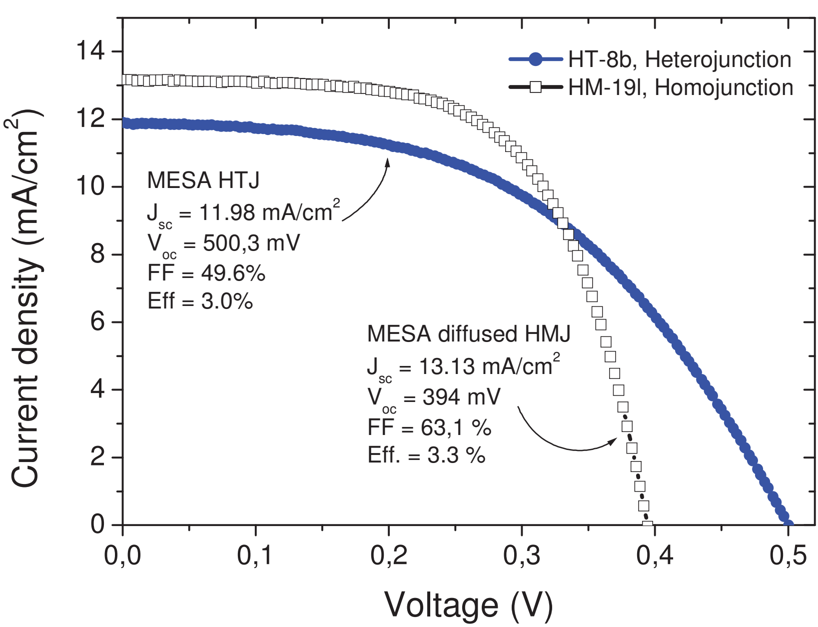


Figure 4.31: Illuminated current-voltage curves of mesa cells with diffused homojunction (sample HM-19l) and heterojunction emitters (sample HT-8b) made on poly-Si on FOx-coated ceramic substrates.

The high V_{oc} of the HTJ solar cell is achieved by the effective passivation of defects on the poly-Si surface with high-quality intrinsic a-Si. In opposite to the higher V_{oc} value, the heterojunction cells exhibit a lower J_{sc}. For a higher I_{sc} using HTJ emitter, optical losses such as absorption in the a-Si and TCO layers must be reduced. These optical losses are mainly caused by the optical absorption of a-Si and the free carrier absorption of TCO. Table 4.4 gives the properties of the cells.

Mesa type	Sample	t_{BSF} (p^+) (µm)	t_{Base} (p) (µm)	$t_{emitter}$ (µm)	R_s, (Ωcm^2)	R_{sh}, (Ωcm^2)	J_{sc} (mA/cm^2)	V_{oc} (mV)	*FF* (%)	*Eff.* (%)
Hetero-junction emitter	HT-8b	1	4	0.017	11.4	432	11.98	**500.3**	49.6	**3.0**
	HT-5b			0.017	14.4	662	10.16	491.7	49.5	2.47
	HT-4a	3	2	0.017	6.3	1326	8.71	497.2	61.8	2.68
	HT-2a			0.017	8.3	473	10.71	475.3	52.1	2.65
Homo-junction diffused emitter	HM-19l	6	4	0.6	1.9	1381	13.13	394	63.1	**3.3**
	HM-06c	4	2	0.6	1.2	185	14.5	306	55.0	2.4
	HM-03c	6	7	0.6	3.2	276	14.1	343	54.5	2.6

Tablo 4.4: Properties and illuminated current-voltage parameters (at 100mW/cm^2) of polysilicon mesa solar cells on FOx-coated alumina for both emitter types after hydrogenation and with antireflection coating.

The fill factor decreased from 63.1% for the HMJ cell to 49.6% for the HTJ cell due to an increase of the series resistance (R_s) by about one order of magnitude and a decrease of the shunt resistance (R_{sh}) by a factor of 3. This behaviour can be attributed to the difference in the BSF thickness of the cells, namely 1µm in the case of the HTJ cell (sample HT-8b) versus 6µm for the HMJ diffused emitter (sample HM-19l). Indeed, a thin BSF layer has a high resistance and leads to a higher series resistance and to a lower fill factor. Thus, in these HTJ cells, holes have to travel a long distance through this thin p^+ BSF layer to reach the base contact, leading to a high series resistance. This is witnessed by the parameters of sample 4a for which the thickness of the BSF was 3µm and which reached a fill factor up to 61.77% and a V_{oc} of 497mV but a relative lower short-circuit current (8.7mA/cm^2) because of the thin (2µm) absorber layer. If we assume that a fill factor of 61.7% is reachable, an estimation of the potential efficiency for a pc-Si cell with a HTJ emitter would be about 3.7%. This efficiency value can be reached by optimizing the thickness of the BSF layer for the HTJ cell.

Figure 4.32 plots the internal quantum efficiency (IQE) curves for both cells. It shows that the larger current collection in the case of the HMJ cell comes from a higher response at

long wavelengths (~440-750nm). At short wavelengths (~350-440nm), an increase in collection is seen for the HTJ cell due to its thinner dead layer and higher quality emitter layer. Indeed, the homojunction emitter is around 0.6µm thick, while the heterojunction emitter is only ~15nm thick (Table 4.4). On the other hand, the IQE hump starts already around 650nm for the HTJ cell but only around 800nm for the HMJ cell. This is due to the thinner BSF layer for the HTJ cell which gives more light of shorter wavelengths being reflected back by mullite ceramic towards the absorber layer. In addition it seems that the homojunction cell has a better material quality than the heterojunction cell (higher IQE peak and at longer wavelengths, i.e. deeper in the layer). The maximum at 0.44µm (HTJ) rather than 0.53µm (HMJ) (0.8µm for single crystal cells) is probably due to the small minority carrier diffusion length in the heterojunction cell compared to homojunction cell. This seems not due to the emitter itself because normally heterojunction emitters lead to slightly better layer quality due to the efficient plasma hydrogenation prior to emitter formation. One explanation could be that phosphorus spikes formed along the grain boundaries of the pc-Si during the emitter formation [70,71] enhances the current collection. This is the TREBLE (ThRee-dimensional Emitter based on Locally Enhanced diffusion) concept [72].

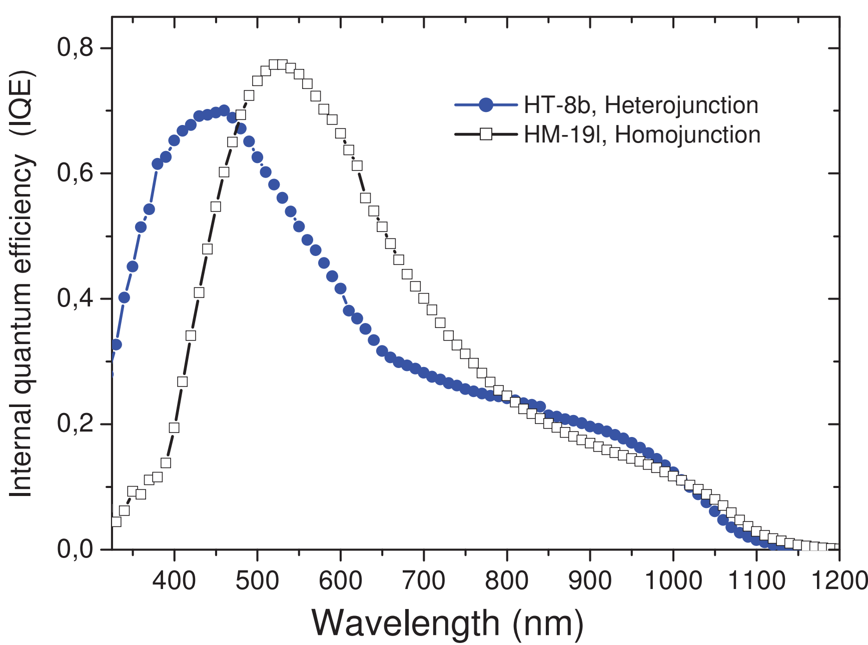


Figure 4.32: Internal quantum efficiency (IQE) curves of mesa cells with diffused homojunction (sample HM-19l) and heterojunction emitters (sample HT-8b) made on poly-Si on FOx-coated alumina substrates. Antireflection layers (SiN_x:H) and ITO were applied on HMJ and HTJ cells, respectively. (No textured surface was applied)

During formation of a diffused emitter, the phenomenon of preferential doping (enhanced diffusion of dopants along grain boundaries) dominates carrier collection, creating a collecting structure extending well below the surface. We have shown that such "preferential" diffusion allows the screening of the grain boundaries towards the minority carriers and therefore enhances the collection of the carriers [72]. This is particularly important in the case of columnar grains, and in <220> oriented polycrystalline silicon [71], which is our case. If the minority carrier diffusion length is lower than the absorber thickness and in the case of deep emitter spikes this can lead to a higher current density for HMJ compared to HTJ. We have indeed observed an improvements in solar HMJ cells quality through the short-circuit current (14.5mA/cm^2) but the drawback is a poor open-circuit voltage (394mV) due to a very large space charge region. Furthermore, the risk of shunting between the n and p regions, especially for the very thin silicon absorber films becomes important. As for the heterojunction cell, the results shows that we can reach even higher V_{oc}'s than 500mV provided the material is of better quality.

According to above discussions, the heterojunction emitter structure was applied on our AIC based solar cells structures.

iii) Mesa versus interdigitated contacts solar cells

Figure 4.33 compares the travel of minority carriers in mesa and interdigitated based solar cells structures. The longer carrier path in mesa cell gives rise to higher series resistance in contrast to interdigitated structure. In mesa structure, the p$^+$ BSF region should be highly doped and thick enough to assure a low series resistance. However, thick BSF layer will absorb more light without being electrically effective. Furthermore, from technological and cost points of view, thicker BSF requires longer time for processing.

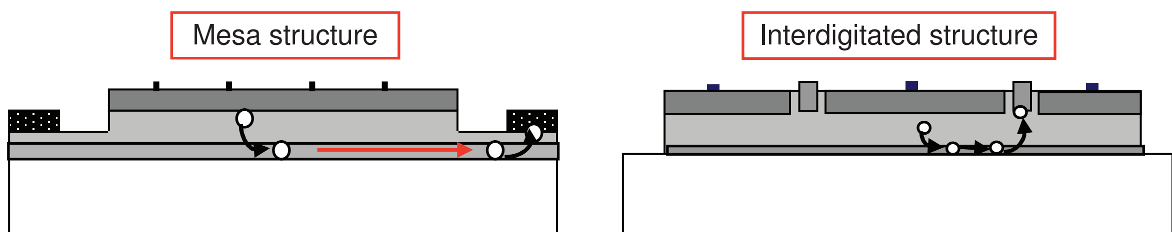


Figure 4.33: Cross-sectional compares of the travel of minority carriers in mesa and interdigitated based solar cells structures (not in scale).

By making the BSF layer very thin, the current density can be enhanced but then an interdigitated contact structure is needed to reduce the series resistance to enhance the

efficiencies [73] (Figure 4.33b). I. Gordon et. al. [74] reported a study on the development of a monolithic module process for thin-film poly-Si solar cells in substrate configuration, in which the cell interconnection is combined with the cell contacting with the contacts on top of the cells in an interdigitated pattern. They showed that interdigitated cells had much higher efficiency (~5.6%) than mesa cells (~3.5%) with base contacts at the periphery of the cells due to lower series resistances and higher current densities. Additionally, the higher current density arises from a much better spectral response of the interdigitated cells in the visible part of the light spectrum. Figure 4.34 shows the improvement of solar cell quality by using interdigitated contacts.

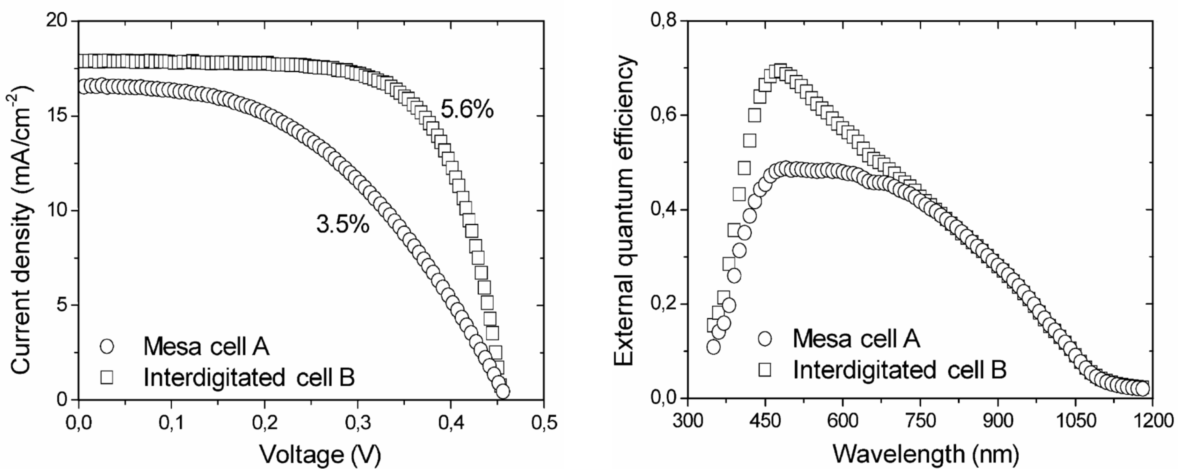


Figure 4.34: (a) Illuminated current–voltage characteristics, and (b) External quantum efficiency measurements of mesa (sample A) and interdigitated (sample B) cells on very thin poly-Si layers [74].

4.2.2. Solar Cells with AIC Seed Layer Approach

i) Solar cell structures

The process flow used for our poly-Si solar cells made on AIC seed layers is shown in Figure 4.35. The cells were prepared at IMEC (Leuven, Belgium). The process involves different steps:

- *Substrate:* FOx-coated alumina or SiN_x-coated glass ceramic.
- *Seed layer:* p^+-type or n^+-type AIC seed layer, which will serve as BSF layer since the cells will be tested in a substrate configuration (illumination from the contacts side).

- *Epitaxy:* the vapor phase epitaxy was carried out in a LPCVD reactor on p^+-type or n^+-type AIC seed layers.
- *Hydrogenation:* this step was realized in a plasma chamber using H_2 gas. The importance of such process will be detailed below.
- *Emitter formation:* it consisted in depositing a double amorphous silicon layer on top of the epitaxial film.
- *ITO coating:* this transparent conductive layer serves as an antireflection coating as well as a contact.
- *Metallization scheme:* an interdigitated contact is preferred instead of mesa contact. The reasons will be given later.

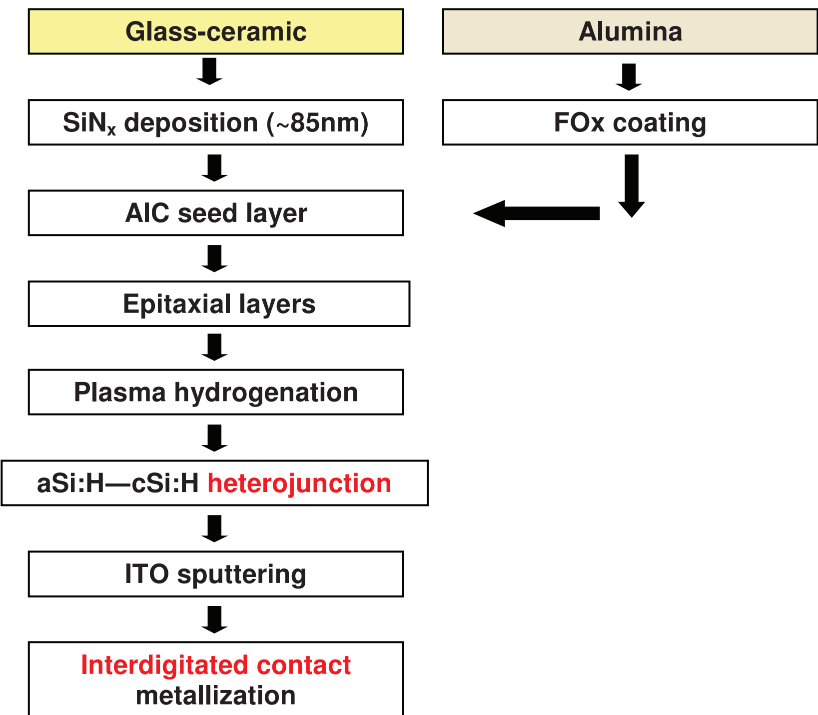


Figure 4.35: Process flow for hydrogenated, heterojunction emitter, interdigitated contact polysilicon solar cell production.

The process steps in the formation of interdigitated-contacted n^+np^+ and p^+pn^+ solar cells structures are summarized in Table 4.5. The epitaxy procedure on the AIC layers by LPCVD system was already described above. The formation of the poly-Si absorber layer was followed by hydrogen plasma for 30min with H_2=30sccm in a PECVD system. To prepare the p^+pn^+ or the n^+np^+ cells, thin intrinsic and doped amorphous silicon layers (respectively in$^+$ a-Si:H for p-type cells, ip$^+$ a-Si:H for n-type cells) were deposited consequently in the same direct PECVD system [75]. The thickness of the emitter region is around 15nm for both cases.

Process steps for interdigitated cell structure	*Schematically cross-section of the interdigitated cell structure*
1) Bulk Passivation by hydrogenation • RCA cleaning • Hydrogenation (400°C, 30min)	Absorber layer (n / p) AIC poly-Si layer (n^+ / p^+) Substrate
2) Formation of p^+ Heterojunction Emitter • Intrinsic a-Si deposition (t=8nm) and p^+ a-Si deposition (t=8nm)	Absorber layer (n / p) AIC poly-Si layer (n^+ / p^+) Substrate
3) Surface passivation and Anti-reflection coating (ARC) • ITO deposition by RF sputtering (t≈80nm)	Absorber layer (n / p) AIC poly-Si layer (n^+ / p^+) Substrate
4) Formation of Base contacts • Photolithography • Wet etching up to base contact in poly-etch solution (HNO_3:HF:H_2O (40:1:16)) • Al evaporation (t_{Al}=2.3µm) • Lift-off	Absorber layer (n / p) AIC poly-Si layer (n^+ / p^+) Substrate
5) Formation of Front contacts • Ti/Pd/Ag stack evaporation (t_{Ti}=70nm, t_{Pd}=50nm, t_{Ag}=3µm)	Ti/Pd/Ag contact Al contact ITO ARC i p^+/n^+ a-Si emitter Absorber layer (n / p) AIC poly-Si layer (n^+ / p^+) Substrate

Tablo 4.5: Process sequence for the formation of interdigitated cell structure (not in scale).

After the formation of heterojunction emitter layer, an indium tin oxide (ITO) layer was deposited by RF-sputtering to minimize the reflective losses and to provide a conductive channel, serving as transparent conductive oxide (TCO).

Indeed, the indium tin oxide (ITO) layer with a reflective index close to 2 and an appropriate thickness can provide an ARC for heterojunction emitter poly-Si solar cells. The effect of ARC, i.e. ITO, was determined by reflectance spectrum of an 80nm ITO-coated and –uncoated cells as shown in Figure 4.36. The figure depicts that the reflectance decreases drastically for whole spectrum by using ITO coating.

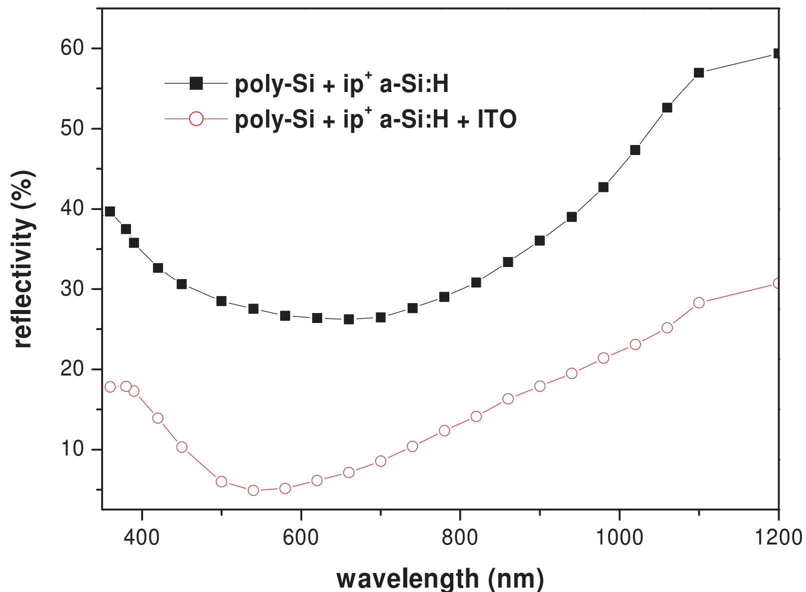


Figure 4.36: Reflectance spectrum for n-type polysilicon films before and after ITO coating.

The last step in fabricating the cell is the metal contacting. Thus, the base Al and Ti/Pd/Ag emitter contacts were deposited by electron beam evaporation in combination with lift-off photolithography and shallow mask, respectively. The emitter contact is the stack of Ti (70nm), Pd (50nm) and Ag (3µm). The Ti serves as a barrier for metal diffusion into the silicon, Pd serves as adhesion layer between Ti and Ag, and Ag contact is the conducting metal for electrons [65].

All the contacts are on top of the cell in an interdigitated finger patterns (Figure 4.37a). As demonstrated above, the advantages of using interdigitated contact are lower series resistances and higher current densities. The width of base and emitter contact fingers is ~40µm; and the distance of the emitter fingers as well as base fingers is 1.1mm. The metal coverage of surface due to interdigitated contacts is around 8%. Finally, the heterojunction devices were separated cells using photolithography and wet chemical etching. The cell unit

area is 1×1cm^2. Additionally top view of an interdigitated-contacted cell is shown in Figure 4.37b.

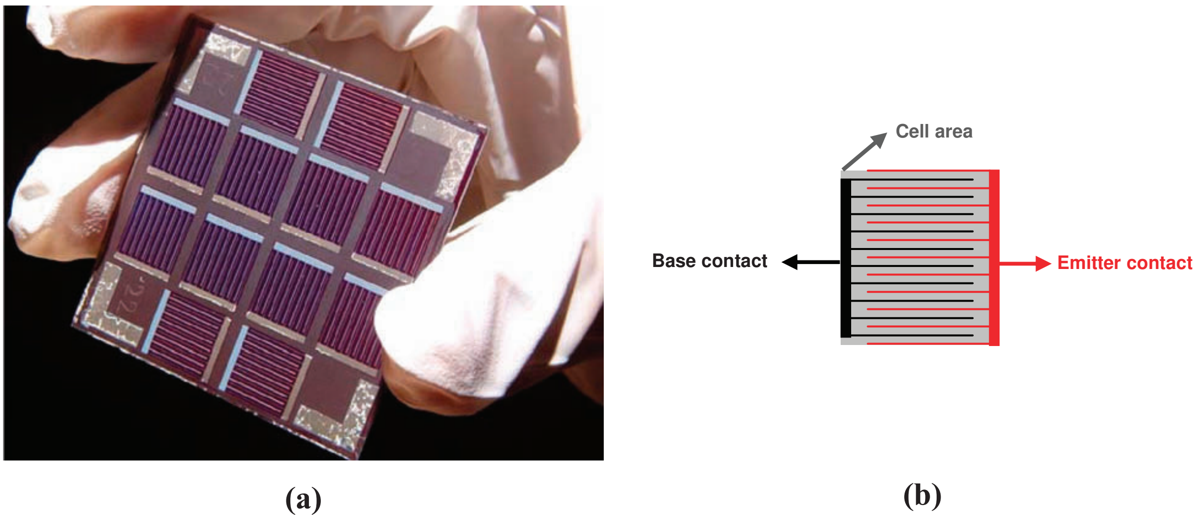


Figure 4.37: (a) Picture of an interdigitated cell on alumina substrate, and (b) Top view of a cell with interdigitated contacts.

ii) P-type based polycrystalline silicon solar cells made on alumina and glass-ceramic substrates

We have prepared p^+pn^+ solar cells using the AIC seed layer approach on alumina and glass-ceramic substrates. This study allows investigating the influence of surface roughness of the substrates on electronic quality of the poly-Si solar cells. As described in Chapter 3, after coverage of the alumina substrate by a single spin-on oxide layer, the roughness decreases to roughly 160nm. However SiN_x-coated glass-ceramic has a peak to valley roughness value of 8.2nm. A reduced surface roughness leads to less Si nucleation centers during the AIC process. AIC layers made at 500°C on glass-ceramic substrates, therefore, have a larger average grain size (~12µm) than similar seed layers on alumina substrates (6.0µm). After ~2µm thick epitaxial thickening by LPCVD system at 1000°C, the average grain of the absorber layers was around 11.2µm on SiN_x-coated glass-ceramic and around 6.9µm on alumina covered by a spin-on oxide.

Figure 4.38 depicts current–voltage (*I-V*) characteristics of interdigitated solar cells with a heterojunction emitter on SiN_x-coated glass-ceramic and on alumina covered by a single spin-on oxide layer. Additionally, the solar cell parameters are listed in Table 4.6. As depicted in this table, the smooth-surface glass-ceramic substrates with larger grain size of epitaxial poly-Si layer lead to poly-Si solar cells with higher V_{oc} values and higher efficiencies than smoothened alumina substrates. The seed and the absorber layers for both solar cells were made under the same conditions resulting almost in the same fill factor for both samples. While the short-circuit current densities of glass-ceramic had a slightly enhancement reaching

9.93mA/cm^2 compared to alumina, the V_{oc} increased significantly from 471.7mV on alumina to 502.0mV on glass-ceramic substrate. The SiN_x-coated glass-ceramic substrates resulted in a relative increase of the energy conversion efficiency by ~15%. Finally, 3.3% efficiency value considering the total area is achieved for poly-Si solar cell on glass-ceramic substrate while it is 2.9% when using the alumina substrate.

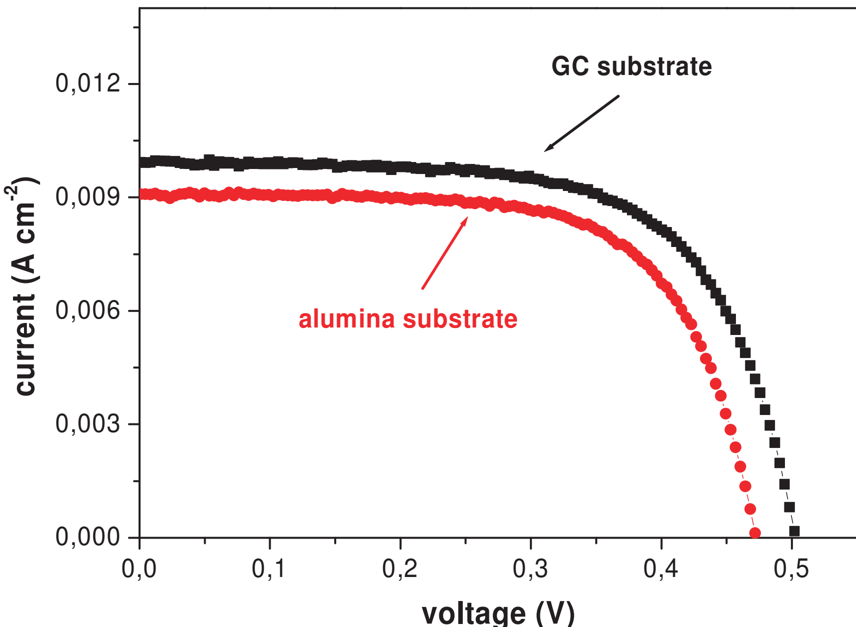


Figure 4.38: Current-voltage (*I-V*) curve of p-type based AIC solar cells made on alumina and glass-ceramic substrates.

Poly-Si solar cell	*on GC*	*on Al_2O_3*
Roughness (nm)	8.2	160
Grain Size (μm) (AIC formed at 500°C)	11.2	6.9
J_{sc} (mA cm^{-2})	9.93	9.06
V_{oc} (mV)	502.0	471.7
FF (%)	65.7	66.97
η (%)	**3.3**	2.9

Tablo 4.6: Solar cell parameters for p-type poly-Si cell on glass-ceramic (GC) and alumina (Al_2O_3) substrates.

The short circuit current enhancement observed for the cell on glass-ceramic substrate is checked by internal quantum efficiency measurements. Figure 4.39 shows the internal quantum efficiency (IQE) of both cells. The IQE of the glass-ceramic used cell is enhanced

compared to that of the alumina used cell mainly at long wavelengths. This enhancement shows the higher absorption quality of glass-ceramic substrates which is convenient to cell performance results. Comparable IQE for both cells at short wavelengths is mainly due to the same emitter and contact formation. The improvement of IQE results, which is due to the higher material quality and higher carrier collection, by using glass-ceramic substrate is also studied in terms of effective diffusion length. Effective diffusion length (L_{eff}) of the minority carriers was deduced using the absorption coefficient (α) and IQE data for the calculation of the effective diffusion length [76]. We obtained an effective diffusion length (L_{eff}) value of 1.2μm for the glass-ceramic used cell while that for alumina based cell is of about 0.9μm. This is consistent with the structural and efficiency results that show improvements when using glass-ceramic substrates.

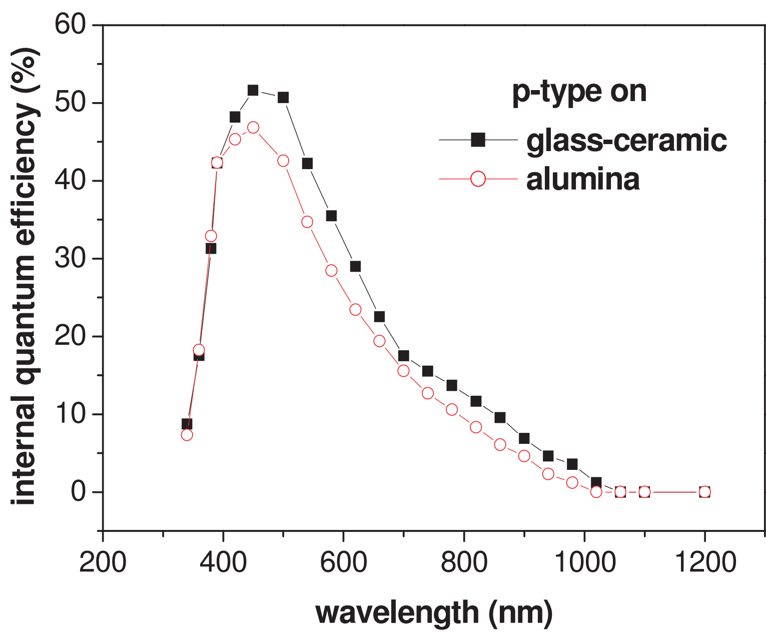


Figure 4.39: Internal quantum efficiency (IQE) as a function of wavelength for p-type poly-Si solar cells on alumina and glass-ceramic substrate.

iii) N-type based polycrystalline silicon solar cells on alumina substrate

We have shown in Chapter 3 that the p-type seed layer can be converted to n-type layer by an overdoping process, making it possible to fabricate efficient (n) poly-/(p) a-Si heterojunction structures, which can offer higher open-circuit voltages compared with our standard (p) poly-/(n) a-Si structure [77]. Furthermore, a higher minority carrier lifetime and a higher tolerance towards metal impurities [78] are also expected in n-type poly-Si. Besides,

the recombination can be controlled by means of a preferential doping along the defects. Hence, n-type heterojunction solar cells can potentially lead to higher efficiencies, as already demonstrated by Sanyo with their HIT^{TM} (Heterojunction with Intrinsic Thin layer) solar cell using n-type high lifetime wafer material [79]. They have achieved efficiency value of 23.0% (V_{oc}= 729mV) using n-type c-Si with HIT emitter. Consequently, using n-type poly-Si cells with HTJ emitter could lead to better photovoltaic performances.

In this part we report on the cell processing of n-type poly-Si solar cells and compare the cell performances of p-type and n-type based AIC polysilicon materials on alumina substrate.

We have prepared p- and n-type polysilicon heterojunction based solar cells on alumina substrate and compared their photovoltaic performances. Illuminated current-voltage (*I-V*) characteristics were measured by using a halogen-lamp-based solar simulator (AM1.5G, $100mWcm^{-2}$, 25°C). The results of I-V measurements for p- and n-type solar cells are reported in Figure 4.40a. As shown in Figure 4.40a, the cell has the following 1-Sun parameters: J_{sc} = $16.8mAcm^{-2}$, V_{oc} = 462mV, FF = 0.645, η = 5.0%. The p-type polysilicon cell shows a slightly higher V_{oc} by about 10mV compared to n-type cell. This can be explained as a result of much less experience yet in optimizing the hydrogenation step and emitter layer formation for n-type poly-Si. On the other hand, the n-type cell exhibits a much higher short circuit current J_{sc} which is almost 2 times more than that of p-type cell. The fill factor (*FF*) is quite comparable for both cases indicating that the aluminium is also a good contact for n-type cell. These cell parameters are reached without doping profile control, optimized emitter, optimized hydrogen passivation nor light trapping, all of which will be improved in our future research. As a result of the current increase, using n-type cell led to an increase in efficiency from 2.9 to 5.0% compared to p-type cell. The efficiency of 5.0% realized in our n-type cell is worldwide the best efficiency so far for n-type poly-Si solar cells based on the AIC approach.

The n-type cell was also characterized by the Suns-V_{oc} tool as shown in Figure 4.40b. This measurement takes the V_{oc} as a function of the light intensity or Suns (1 sun equals $1000W/m^2$) which determines the pseudo-fill factor, pseudo-efficiency and open circuit voltage without the influence of the series resistance [80]. The Suns-V_{oc} curve for n-type cell is compared in Figure 4.40b with the measured illuminated *I-V* curve of the n-type solar cell. Considering these curves, it is precise that the series resistance results the difference between two curves at the knee. Except the knee region, the curves closely follow each other. The measurement of conventional *I-V* curve gives an efficiency of 5.0% with a fill factor of

64.5%. The curve constructed from the Suns-V_{oc} data indicates a pseudo-efficiency of 5.5% with a pseudo-fill factor of 71.6%. This comparison clearly indicates that reduction in series resistance and carrier transport effects improve the cell efficiency from 5.0 to 5.5%.

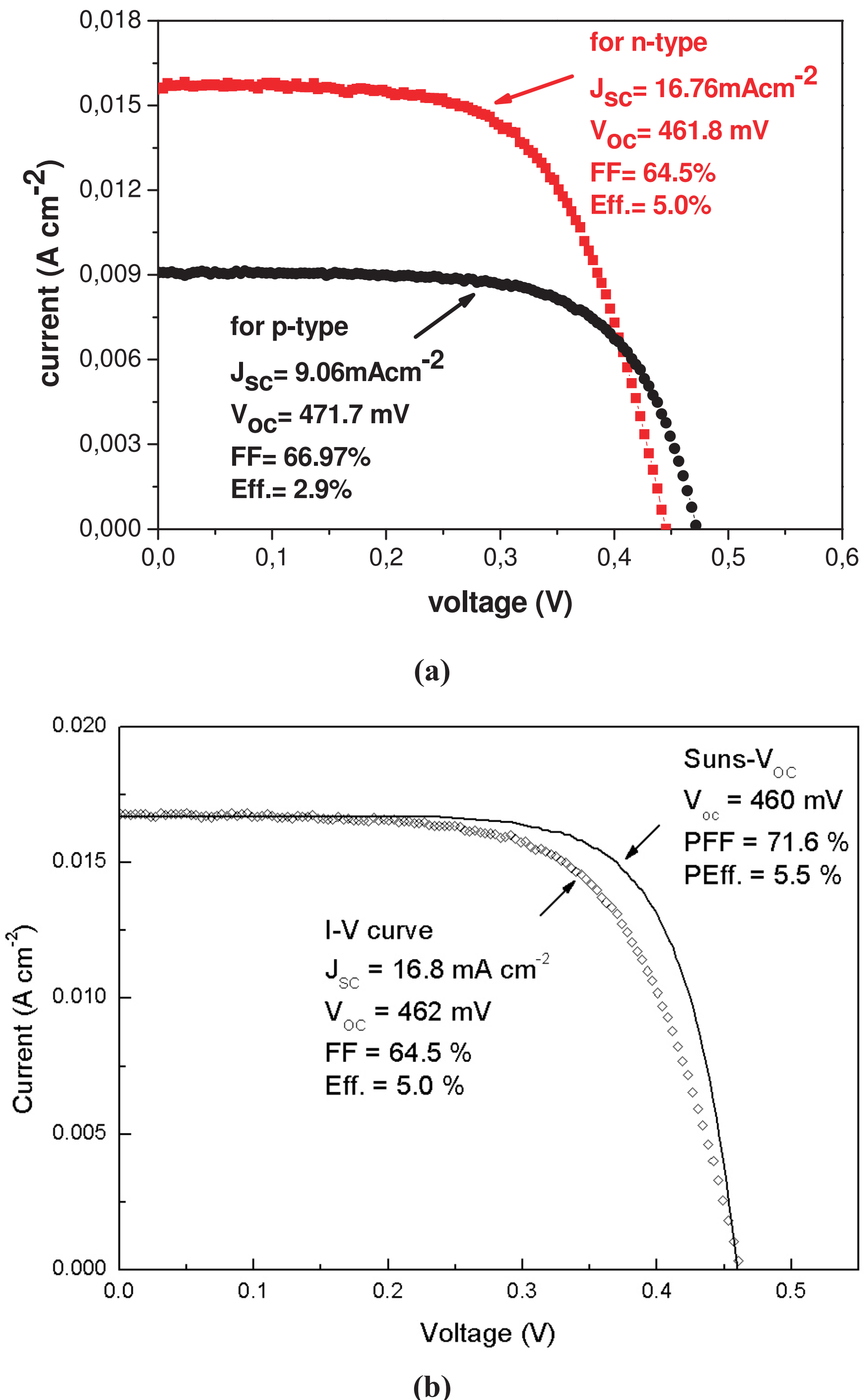


Figure 4.40: (a) Illuminated current-voltage (*I-V*) curves of p- and n-type poly-Si solar cells on alumina substrate, and (b) *I-V* data and Suns-V_{oc} data of the 5.0% n-type solar cell.

The solar cell efficiency values discussed above are for total area measurements. However, calculating the cell efficiency only by using total area is the failure to mask the cell such that only light incident on the reported active area reaches the absorber. This is especially important when the area is small (e.g. 0.25-1cm^2) [81]. For our case, if we consider that the total cell area is 1cm^2 and the interdigitated contact covers the ~8% of total area, the cell results can be expressed as listed in Table 4.7. In this table, the cell efficiency values deduced from *I-V* and Suns-V_{oc} measurements for p- and n-type polysilicon cells are determined by including the total and active areas. It is shown that, the efficiency values of n-type cell by using active area calculation, which excludes the mask shadowing effect, reach up to 5.5% for *I-V* measurement and 6.1% for Suns-V_{oc} measurements.

Cell	*Efficiency (%)*			
	From I-V (total area)	*From I-V (active area)*	*From Suns-V_{oc} (total area)*	*From Suns-V_{oc} (active area)*
N-type	5.0	**5.5**	5.5	**6.1**
P-type	2.9	3.2	2.9	3.2

Tablo 4.7: Cell efficiency results for total and active areas of n-type and p-type solar cells.

The significant current enhancement by using n-type material instead of p-type is studied in terms of spectral response measurements. The spectral response of the n-type HTJ and interdigitated poly-Si cell is presented in Figure 4.41.

Due to the reduced front surface reflection by ITO and the oblique light coupling, a much larger portion of the light gets absorbed near the space-charge region. External and internal quantum efficiency can be analyzed through three different ranges of wavelengths. The weak response (~10-30%) for the wavelengths lower than 450nm corresponds to the current collection in the emitter. The well processed heterojunction emitter that makes a good passivation by intrinsic a-Si can explain this quite high quantum efficiency results. Beyond 450nm, the IQE represents the collection in the space charge region and in the base. Quite large and wide wavelength range located IQE explains the good base layer quality and the possible improvements by hydrogenation and using the n-type material, which can cause the defect passivation at grain boundaries. The effective diffusion length analysis can be done in the wavelength range of 800-950nm (see Appendix B).

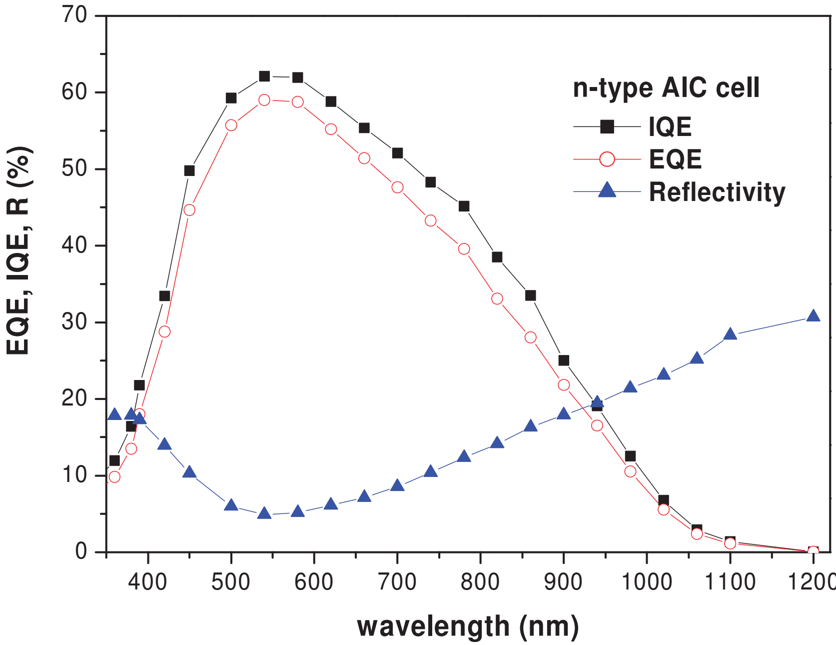


Figure 4.41: Spectral response of the n-type, HTJ emitter, interdigitated contact solar cell. The reflectivity, external (EQE) and internal (IQE) quantum efficiencies are represented as a function of wavelength.

In addition to comparative *I-V* results for p- and n-type cells, a deeper analysis was carried out by measuring the spectral response of these cells. The internal quantum efficiency (IQE) data allow approaching the minority carrier diffusion length in the base as well as providing information on the back surface recombination velocity. However, for thin-film cells it is important to include the emitter properties in the model when analyzing the IQE spectra. Figure 4.42 plots the IQE for the n-type and p-type polysilicon cells made on FOx-coated alumina. It is clearly seen that the spectral response of the n-type cell is much higher than that of p-type cell, over a large part of the spectrum. This is consistent with the deduced J_{sc} values reported above. The current increases from 9.06 to 16.76mA/cm^2 for n-type cell results from a lower reflectance and from an oblique coupling of the light into the cell. Short circuit current of solar cells depends to a large extent on the way that the photogenerated carriers are collected. This can explain the consistency of quite high J_{sc} and IQE results for n-type cell. Additionally, the dominating SCR recombination in our n- and p-type cells is confirmed using spectral response measurements. Using the absorption coefficient (α) and IQE data for the calculation of the effective diffusion length [82], we obtained an effective diffusion length (L_{eff}) value of about 2.6µm for the best n-type heterojunction cell. This value is comparable to the absorbing silicon layer. On the other hand, an effective diffusion value of

0.9µm is calculated for p-type heterojunction cell. The enhanced effective minority carrier diffusion length, L_{eff} is responsible for the improved long wavelength minority-carrier collection efficiency. Additionally, the enhancement in L_{eff} can be attributed to the well known phosphorus gettering process [83] resulting in a significant improvement on IQE curve for n-type cell, especially in long wavelengths, and thereby the enhancement of L_{eff}. Although the structural properties of p-type and n-type based cells are comparable, the cell performances are better for n-type cells. This can be due to better carriers transport and lower grain boundaries and twins electrical activities due to phosphorus.

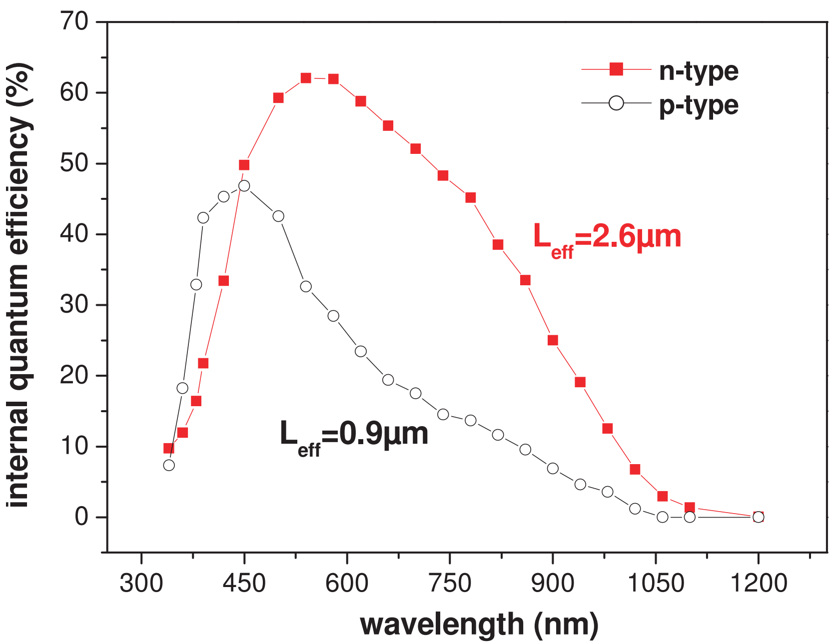


Figure 4.42: Internal quantum efficiency (IQE) curves of p- and n-type poly-Si solar cells on alumina substrate.

In addition to gettering effect of phosphorus, the other important effect on higher cell performance and L_{eff} for n-type can be the effect of drift field on minority carrier collection. The p-type solar cells are of classical type, i.e., fabricated by making a diffusion into a base layer with constant impurity during epitaxial thickening. However, our n-type poly-Si solar cells exhibit a graded phosphorus profile thanks to the out-diffusion of phosphorus from the heavily doped AIC seed layer as modelled in Figure 4.43. This graded phosphorus profile for our n-type poly-Si thin film solar cells gives rise to an electric field [55,84]. Since the electric "drift" field resulting from non-uniform base doping is potentially beneficial to solar cell performance, evaluation of its effect is of practical importance.

Indeed, it has reported that long-wavelength minority carrier-collection efficiency of solar cell with low-minority carrier lifetime can be improved by creating a drift field in the base layer [85,86]. By suitably varying the doping concentration across the base of the cell, an electric field can be formed so that minority carriers will be drift towards the junction and thus, have an enhanced effective diffusion length. It is suggested that in our case the field ranges from lower to higher doping concentrations (i.e. from the epi-layer surface to the AIC seed layer surface). Minority charge carriers (holes) would follow the drift field resulting in an enhanced J_{sc} of the processed solar cell.

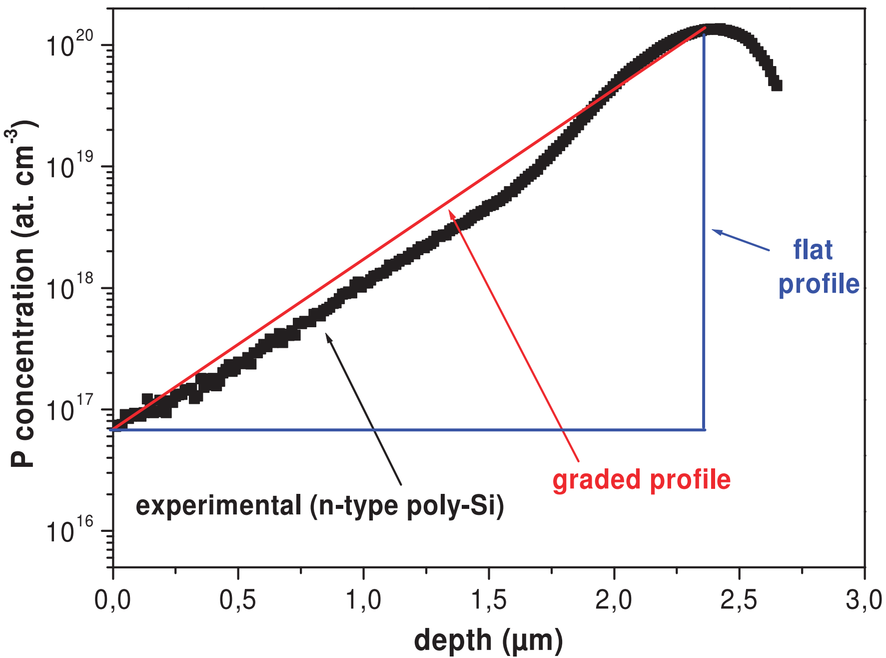


Figure 4.43: Modelling of phosphorus doping profile for n-type polycrystalline silicon formed on AIC seed layer using P509 solution.

Effect of drift-field on minority carrier collection can be studied in terms of L_{eff}. The graded doping profile of our poly-Si thin film as modelled in Figure 4.43 can be approximately expressed by an exponential gradient:

$$N_D(x) = N_D(0)e^{\beta x} \tag{4.6}$$

where $N_D(0)$ is the doping concentration at the back-surface field. Additionally, the electrical field $E(x)$ generated by an arbitrary doping gradient and effective diffusion length are given by [55]:

$$E(x) = \left(\frac{kT}{q}\right)\beta \tag{4.7}$$

$$L_{eff} = L_p(\beta L_p + 1) \tag{4.8}$$

where L_p is the minority carrier diffusion length. As deduced from Equation 4.8, $L_{eff}=L_p$ when there is no graded doping profile. However L_{eff} is higher than L_p if a graded doping profile occurs, i.e. by the presence of electrical drift-effect.

As shown in Figure 4.43, the doping gradient of 1.35×10^{20}cm^{-3} to 8.43×10^{16}cm^{-3} creates a good drift-field in the base. This thin-film doping gradient yields β=3.69µm^{-1}. The value of β calculated using the parameters in Table 4.8 is quite high as well as resulting in higher L_{eff} (~2.6µm for n-type cell).

Parameter	*Value*
Depth of base *x*	2µm
$N_D(0)$	1.35×10^{20}cm^{-3}
$N_D(2)$	8.43×10^{16}cm^{-3}
β	**3.69µm^{-1}**
η (with drift effect)	5.5%

Tablo 4.8: The doping and depth parameters to deduce the β.

The phosphorus doping gradient is not only enhancing the effective minority-carrier diffusion length but also increasing the long wavelength response. The effect of drift-field on IQE is simulated in Figure 4.44 comparing the spectral response of cells with graded and flat doping profiles that are including and excluding the drift-field, respectively. The spectral response is much more improved with drift-field effect, especially at long wavelengths. A large spectral response result with drift-field effect has a quite concordance with the experimental IQE results for n-type solar cell depicted in Figure 4.42. Since the benefit of a drift-field is greatest in poorer quality material, the influence of drift effect is fairly large for n-type polycrystalline solar cells.

As a summary, the drift-field incorporated in the absorber layer assists in minority carrier diffusion toward the junction, and hence in an enhancement in J_{sc}. However, drift fields reduce V_{oc} by the voltage drop across the layer where they act. By this modelling, we can explain the significant increase of J_{sc} from 9.06 to 16.76mA/cm^2 using n-type material and improvement in efficiency η, while V_{oc} has a slight decrease compared to p-type.

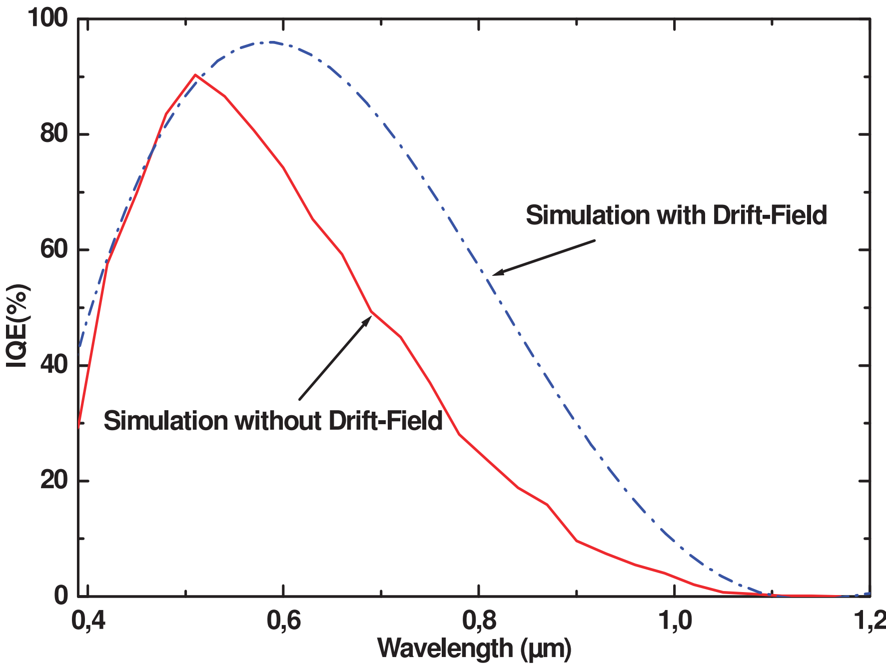


Figure 4.44: Simulation of spectral response of solar cells by including and excluding drift-field effect.

To summarize this section, the first n-type polysilicon solar cells with AIC approach were fabricated using the heterojunction emitter structure and interdigitated contacts. ITO is used as an ARC, resulting in a reduction of front surface reflection and the oblique light coupling. The high base epi-layer quality and the efficient defects reduction by plasma hydrogenation applied to n-type polysilicon give rise to a quite broad and high IQE. The n-type cell exhibits a much higher short circuit current J_{sc} which is almost 2 times more than that of p-type cell of comparable thickness. As a result, the efficiency of 5.5% realized in our n-type cell is worldwide the best efficiency so far for n-type poly-Si solar cells based on the AIC approach while it is limited to 3.2% for p-type cells without texturing. In addition to cell efficiency, the spectral response of the n-type cell is also much higher than that of p-type cell, over a large part of the spectrum, which is coherent with the behaviour of J_{sc}. The improved long wavelength minority-carrier collection efficiency and phosphorus gettering process can explain the high effective diffusion length L_{eff} for n-type cell (~2.6µm). In addition to gettering effect of phosphorus, the other important effect on higher cell performance and L_{eff} for n-type can be the effect of drift field on minority carrier collection due to a graded phosphorus profile (n^+n) thanks to the out-diffusion of phosphorus from the heavily doped AIC seed layer.

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CHAPTER 5: CONCLUSION and OUTLOOK

Thin film polycrystalline silicon solar cells on foreign substrate is a promising alternative to single crystalline silicon solar cells due to its long-term stability, steadily upward efficiency and low-cost fabrication. In this work, aluminium induced crystallization (AIC) process and formation of polysilicon solar cells using AIC seed layer and epitaxy approaches are investigated.

The AIC of amorphous silicon (a-Si) has been used to produce polycrystalline silicon layer (pc-Si or poly-Si) with grains much larger than those achievable either by thermal annealing of a-Si or by direct deposition of pc-Si by Chemical vapor deposition (CVD). In this work, the Si and Al layers, each a few hundreds of nm thick, were generally deposited by PECVD and electron beam evaporation respectively. The initial a-Si was systematically slightly thicker than the initial Al layer in order to form a continuous layer. Importantly, a few nanometer thin AlO_x membrane was formed between the initial Al and a-Si layers prior to Si deposition. This AlO_x inter layer plays a crucial role throughout layer exchange process by remaining in position, separating top and bottom layer and behaving as a membrane that controls the diffusion. The aluminium acts as a catalyst to induce crystallization; and the transformation from amorphous to crystalline silicon occurs at temperatures below the Al/Si system eutectic temperature of 577°C. The growth of the crystalline phase would stop when no more metal is available. We have studied the effects of some crucial parameters on the nucleation kinetics of grains and on the final properties of the grown AIC poly-Si layers. In particular, we have found the following results:

- The thickness of the AlO_x layer has an effect on the surface morphology and crystal quality of the final AIC polysilicon film. Thicker is the oxide layer longer is total duration needed for crystallization. On the other hand, the average grain size tends to enhance by increasing the thickness of AlO_x. Lower nucleation rate and bigger grain size were observed with thicker oxide layer thickness.
- We have identified two parameters of the aluminium layer that controls the nucleation rate of Si, namely the oxygen concentration and the grain size of aluminium. Aluminium layer containing a higher oxygen concentration can include more defects that may cause faster diffusion of grain and thereby resulting in a reduced process time. On the other hand, lower oxygen content in the starting Al film reduces the nucleation rate and causes larger average grain size. Finally, lowering the Al deposition rate increases the Al grain size that gives raise to lower nucleation rate and thereby larger-grain size poly-Si film.

- Glass-ceramic and alumina were chosen as substrates due to their high temperature resistance (≥1000°C) and thermal expansion coefficients matching that of silicon. The investigations showed that the small average grain size and the very broad grains distribution observed for poly-Si formed on SiO_2 coated alumina can be correlated to the quite degree of roughness of the alumina surface (R=160nm) compared to surface roughness of glass-ceramic (R=18.5nm). Increased surface roughness enhances the nucleation rates and results in competing grown grains, and finally in small grains. Polycrystalline silicon layer with quite large grains with an average grain size value of ~26µm can be formed by AIC technique on glass-ceramic substrate.
- The annealing temperature and time are crucial parameters of the Al/Si layers exchange process. The nucleation and crystallization are very fast (i.e. in shorter time) for high process temperatures while they are slower (i.e. the crystallization happens slowly) at lower temperatures. The observed behaviour at high temperatures can be correlated to the lower incubation time. It can be noted that the nucleus density decreases at lower temperatures whereas the grain size increases. The kinetics of the nucleation during AIC can differ with regards to the used substrate due to the different activation energies. We have deduced higher activation energy (1.7eV) of the crystallization process of silicon on glass-ceramic substrate compared to alumina used process (1.4eV). Additionally, it can be concluded that the lower annealing temperature also reduces the nucleation rate, resulting in larger grain size.
- The post thermal treatment of AIC polysilicon layer at high temperatures (≥900°C) was carried out to check the defect annealing, with the hope of an improved poly-Si films quality. We have shown that the thermal annealing has no significant effect in terms of crystallographic or electrical quality of the AIC seed layers. The Hall mobility of $62.5cm^2/Vs$ at hole concentration of $1.19\times10^{18}cm^{-3}$ before post annealing remains almost the same after annealing.
- For most experimental conditions, the resulting polycrystalline silicon layers are quite smooth and continuous. The optimal thermal budget is 475°C for 8h, resulting in polycrystalline silicon with an average grain size more than 100 times its thickness (0.2µm). Additionally, most of the grains are <100> oriented.
- We have shown that the main crystallographic defects present in the continuous AIC polysilicon seed layers are the low-angle grain boundary (LAGB, angle<2°) and the coincident site lattice (CSL) boundaries consisting of twin boundaries of first order (Σ3),

second order (Σ9) and third order (Σ27) while the majority of crystallographic defect is Σ3 independently from substrate choice and exchange annealing temperature.

The AIC process being based on the overall layer exchange of adjacent Si and Al films and transformation of amorphous to polycrystalline Si during thermal annealing, the resulting polycrystalline layer is a p^+ type. Indeed the p^+-type AIC poly-Si film is formed directly due to the presence of Al in poly-Si layer and serves as a back surface field with a carrier concentration of ~$2x10^{18}cm^{-3}$.

We have also investigated the possibility of the formation of n-type polycrystalline silicon by direct doping of the p-type AIC layer from a solid doping source. We have studied the thermal diffusion of phosphorus in p-type seed polysilicon from a spin-on dopant (SOD) solution containing a high concentration of phosphorus atoms. The overdoping of the poly-Si AIC is first analyzed by the four-point probe method. The sheet resistance value is reduced from 2700Ω/sq for the AIC layer to 19.6Ω/sq after phosphorus diffusion at 1000°C for 1h. We have checked the change in doping type and concentration using Hall Effect measurements. The result shows that it is possible to efficiently convert a thin p-type polysilicon AIC layer into a highly doped n^+-type poly-Si thanks to the phosphorus diffusion at high temperature and the appropriate choice of the doping sources.

The AIC poly-Si layers being too thin (~200nm) and too heavily doped ($C \sim 2\times10^{18}cm^{-3}$ for p-type film or $C \sim 6\times10^{20}cm^{-3}$ for n-type film when P509 doped) to serve as a base for solar cells, we have investigated the epitaxial thickening step to form the absorber layer aiming at a thickness of 2-8µm. Since our aim is to fabricate p^+p or n^+n structures on foreign substrate, the highly doped p^+- and n^+-type AIC polysilicon layers can be used as a seed for further growth, as a back surface field for carriers and -more original-, as a doping source for the epitaxial layer during the thickening step. For the fabrication of the epitaxial silicon layer on the poly-Si seed layer we have explored two ways: (i) high-temperature (>700°C) solid phase epitaxy (SPE) of a-Si thick film deposited on oxide-free AIC poly-Si seed layers; and (ii) high-temperature vapor phase epitaxy (VPE) using silicon-chlorine based gases or silane (SiH_4) as silicon precursors.

In SPE technique, recrystallization of the amorphous silicon deposited on the AIC seed layer was performed either by rapid thermal processing (RTP) using lamps or by classical thermal processing (CTP) using conventional resistive heater. We have shown that quite large average grain size (~40µm) and fewer defective poly-Si films were formed using RTP. The enhancement of the grain size and existence of fewer defects after RTP can be explained by a decrease in nucleation or an increase in the grain growth rate as an effect of

low thermal budget of RTA system. The majority of silicon surface are composed of <100>-oriented grains, independently from the furnace type. This was expected for poly-Si films formed by thickening on preferentially <100>-oriented AIC layer. The crystal quality of SPE-Si strongly depends on the annealing conditions for recrystallization, such as annealing tool, temperature and duration. Stress free crystalline silicon can be formed using RTP while silicon with compressive stress was obtained for CTP. During SPE, phosphorus diffuses from the heavily n-type doped AIC layer within the epitaxial layer towards the surface, resulting in a graded n doped region. We have shown that the phosphorus doping profile within the epi-layer depends strongly on the doping source. Lower doped solutions offers much graded profile compared to the heavily doped one. We have also shown that the preferred <100> orientation of the AIC seed layer is conserved after SPE process, as well as the grains size. However, the cracked surface morphology of the silicon surfaces formed by SPE for both type of furnaces is the drawback of this technique for further solar cell processing.

We have also investigated the epitaxial thickening of the AIC layer by VPE performed at high temperatures (>900°C). In contrast to the SPE process, the VPE is a one step process (direct deposition and epitaxy). The resulting average grain sizes are consistent with those of the underlying AIC poly-Si seed layer for both alumina and glass-ceramic used substrates, thanks to the columnar growth during epitaxy. This shows the grain size conservation during the epitaxial thickening of AIC seed layer. However, using glass-ceramic substrate instead of alumina led to a significant enhancement in average grain size of the epitaxial layer as it was the case already for the AIC layer.

For thickening the n-type AIC layers, no intentional doping gas was used during the epitaxy step. In this case, phosphorus exo-diffusion into the epi-layer occurred during the silicon without additional annealing. Thus, n-type poly-Si absorber layers were formed on the AIC layer. In contrast to SPE process, the exo-diffusion of phosphorus from the n^+ type AIC layer occurs during VPE thickening and allowed the formation of graded n^+n structure thanks to the high-temperature epitaxy process. Although smaller grain sizes are found for VPE-Si, cracks free, fully crystallized, continuous poly-Si films and controlled phosphorus diffusion were achieved using VPE technique.

The epitaxial layers formed by VPE were used as an absorbing layer for solar cells fabrication. The epitaxy was followed by plasma hydrogenation and then by heterojunction emitter formation by depositing a stacked undoped and doped amorphous silicon layers. After coating with ITO, the metallic contacts were formed as interdigitated structure.

Thus, p^+pn^+ cell configuration with heterojunction emitter and interdigitated contacts were formed on glass-ceramic and alumina substrates. The smooth-surface glass-ceramic substrates led to poly-Si solar cells with higher V_{oc} values and higher efficiency values than on the rough alumina substrates even coated with SiO_2. Although it should be considered as an approximation, we have deduced an effective diffusion length (L_{eff}) value of 1.2µm for the cells on glass-ceramic compared to 0.9µm for alumina based cell. It can be concluded that using the use of glass-ceramic substrates improves the structural quality and solar cell performance.

We have also prepared for the first n-type based polysilicon solar cells (n^+np^+) with AIC approach on alumina substrate. The heterojunction emitter and interdigitated-contacts were used. These n-type polysilicon cells exhibited a slightly lower V_{oc} by about 10mV compared to p-type based cell. We explained such result as due to much less experience yet in optimizing the hydrogenation step and emitter layer formation for n-type poly-Si. On the other hand, the n-type cell exhibits a much higher short circuit current J_{sc} which is almost 2 times more than that of p-type cell. As a result of this quite high current enhancement, an efficiency of about 5.5% realized in our n-type cells without texturization that should be compared to 3.2% for p-type cells. In addition to cell efficiency, the spectral response of the n-type cell is also much higher than that of p-type cell, over a large part of the spectrum, which is consistent with the behaviour of J_{sc}. We attributed such good performances to improved long wavelength minority-carrier collection efficiency as a result of phosphorus gettering as well as to the drift-field effect induced by the graded phosphorus doping profile within the absorbing layer. Taking the data with caution but for comparison, this lead to an enhancement in L_{eff} for n-type cell (~2.6µm) compared to that of p-type (0.9µm). Analysis of the best n-type based cells with Sun-V_{oc} apparatus, neglecting therefore the contacts resistivity, led to an efficiency value of 6.1%, showing the potential of the n-type polysilicon solar cells without any optimisation of the hydrogenation step, the heterojunction passivation and junction formation, nor the surface texturing. It is considered that this last step is capable to boost the efficiency by a factor a least of 2.

Outlook

There are many investigations that are still needed to complete the present work. They can be summarized as:

- *Texturization of glass-ceramic substrate:* Due to the weak absorption of near-infrared light in crystalline silicon (c-Si), an effective light trapping scheme is essential for poly-Si thin-film solar cells. One effective way to obtain light trapping is to texture the substrate material prior to the deposition of the Si film. As a result of the texturization, light is transmitted obliquely into the Si film, significantly enhancing the optical path length and thus increasing the optical absorption.
- *Optimization of a-Si deposition parameters:* The quality of AIC seed layer is found to have a strong impact on the quality of final polysilicon film. On the other hand, the composition of the amorphous silicon film influences the crystallographic morphology of AIC layer. We have already started some experiments by diluting the silane with hydrogen and much larger grains were obtained. More studies are required to understand the effect of hydrogen on the nucleation rate and also how defective are these layers compared to those prepared in this work.
- *Optimization of Solid Phase Epitaxy (SPE) technique:* We have shown previously that SPE techniques enable to reach large average grain size up to ~40µm. This is a very promising result compared to other techniques. However, due to the problem of cracks in the polysilicon layer, it limited further solar cell fabrication by SPE. Solutions for fewer cracks that should be tested are slow cooling rate after SPE or modifying the SiN_x barrier layer to absorb the mechanical stress.
- *Optimisation of the heterojunction emitter:* Using an intrinsic a-Si:C layer or polymorphous instead of pure a-Si for HTJ emitter may provide a more efficient surface passivation by avoiding the crystallization of the intrinsic layer. This particularly interesting for n-type polysilicon based cells.
- *Plasma texturing of front silicon surface:* To enhance the absorbance within the polysilicon layer, the front surface reflectance of the Si needs to be lowered by texturing the surface. Surface texturing is used to control the reflection by roughening the surface in such a way that the incident light gets more chances to enter the polysilicon layer or used increase the light trapping, thereby a longer effective path length of light.
- *Superstrate configuration for glass-ceramic used cells:* The optical transparency of glass-ceramic is important for superstrate cell configuration, which has several advantages such as no requirement of surface cover glass for encapsulation and interconnection between unit cells in the manufacturing of modules.

APPENDICES

APPENDIX A

A.1 Electron Cyclotron Resonance Plasma Enhanced Chemical Vapor Deposition System (ECR-PECVD)

The a-Si and SiN_x were deposited by electron cyclotron resonance plasma enhanced chemical vapor deposition system (ECR-PECVD, Roth&Rau) in InESS (Strasbourg, France). The ECR-PECVD system is used as a source of plasma that is the combination of electron cyclotron resonance (ECR) and radio frequency (RF). Figure A.1 shows a schema of the RF–ECR plasma system used for our experiments.

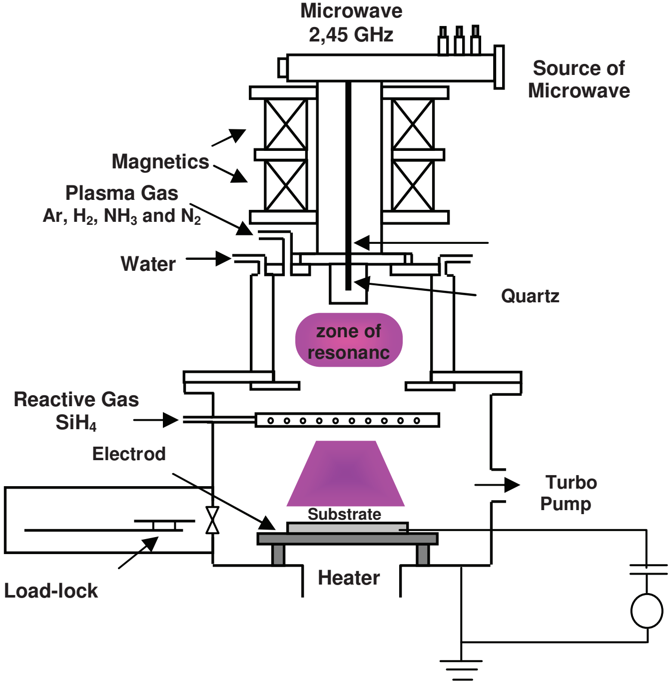

Figure A.1: Schematic of RF–ECR plasma apparatus (Roth&Rau) for a-Si and SiN_x deposition.

In ECR-PECVD system, NH_3, N_2, Ar or H_2 are excited by the 2.45GHz microwave in the resonant chamber, where a magnetic field is applied to maintain the ECR condition. The main chamber is evacuated by a turbo molecular pump to a background pressure of 10^{-7}mbar. The carrier gas radicals are then accelerated in a second chamber where RF plasma is established. The RF bias can be varied from 0 to 800V. The argon gas is introduced into the

''ECR'' chamber and decomposed there while the SiH_4 is decomposed in the ''RF'' chamber. The substrate temperature can be varied in the range of 50 and 500°C. Available gases for our ECR-PECVD system are SiH_4 (72sccm), NH_3 (200sccm), N_2O (100sccm), N_2 (100sccm), Ar (100sccm), H_2 (50sccm).

A.2 Rapid-Thermal Atmospheric Pressure Chemical Vapor Deposition System (RT-APCVD)

During our experiments at the InESS (Strasbourg, France), we used a horizontal cold-wall "JetLight 100" reactor designed and developed by Jipélec (France).

A schematic vertical cross section of the reactor is shown in Figure A.2. The substrates are heated by 12 tungsten halogen lamps from the topside through a double quartz window cooled by oil.

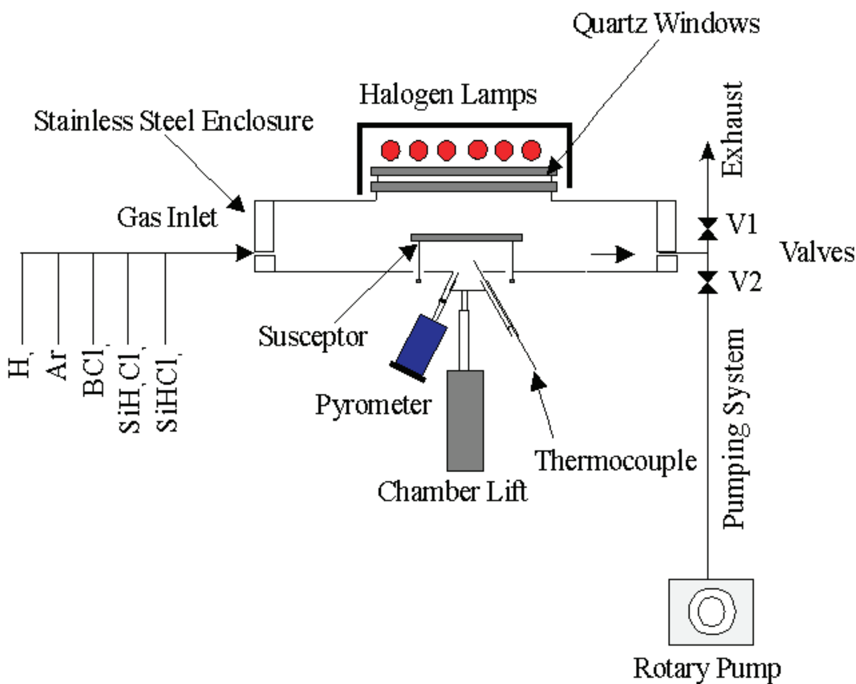

Figure A.2: Schematic representation of RT-APCVD system.

The layers with the thickness of 5 to 50µm can be deposited at pressure atmospheric pyrolytic decomposition of trichlorosilane ($SiHCl_3$) diluted in hydrogen (H_2) with varying concentrations of 1 to 25%. The input hydrogen flow (100-2000sccm) is controlled for the mass flow (1-5g/min) of trichlorosilane.

The in-situ doping of thin films of polycrystalline silicon is obtained by the addition of trichloroborine gas (BCl_3) with concentrations of 1-5% in hydrogen.

A.3 Low Pressure Chemical Vapor Deposition System (LPCVD)

To achieve a low cost final product a commercial available reactor is used in IMEC (Leuven, Belgium). It is named PEO 603 #022 LPCVD (Figure A.3) from ATV Technology GmbH, 85591 Vaterstetten, Germany; and it is used in combination with WinATVnt Version 3.00.0109 operating software. It is able to operate at low pressures till $1x10^{-2}$mbar and a maximum temperature of 1000°C.

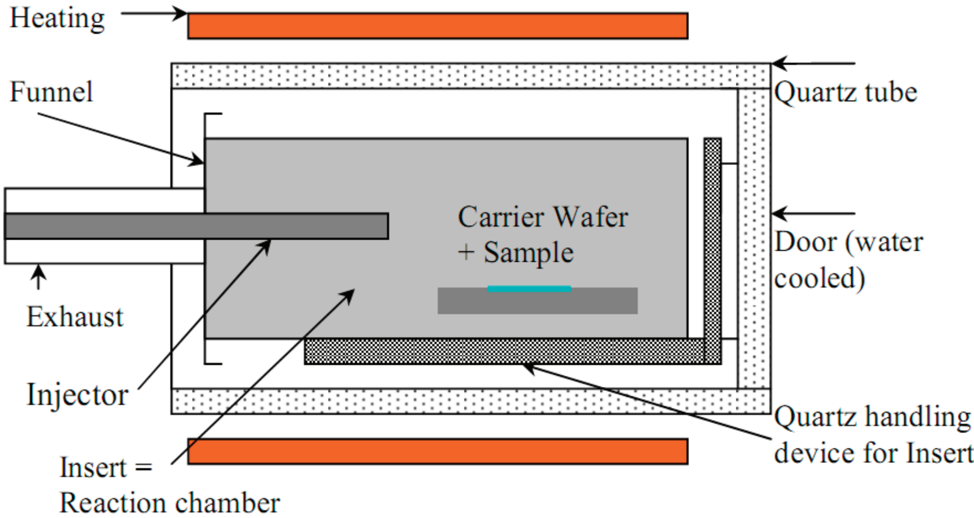

Figure A.3: Schema of assembly of the hot wall LPCVD.

The system consist out of three units; the dosing unit (gas bottles, gas lines, pressure regulators, drop points and Mass flow controllers), the LPCVD device as a hot wall CVD unit and the vacuum pump (and unit for gas recycling or dumping). For all investigations several gas lines like, a silane (SiH_4) line (with maximum flow of 200sccm), a hydrogen (H_2) line (with maximum flow of 5000sccm), a diborane (B_2H_6) line (50ppm) diluted in hydrogen (with maximum flow of 10sccm) and diborane line (1%) diluted in hydrogen (with maximum flow of 200sccm) are available. Furthermore, it is possible to purge all these lines with pure nitrogen (N_2).

APPENDIX B

B.1 Current-Voltage Characteristic

A pn junction solar cell is capable of transform the absorbed energy from incident sunlight into electrical energy. When the free surface of this junction is illuminated, photons whose energy are greater than the width of the band gap E_g (1.124eV for silicon at 300K) can generate electron-hole pairs in the quasi-neutral n (or p) and the transmitter of the base p (or n). A photovoltaic cell behaves as a power generator under illumination where its operation is equivalent to that of an electrical circuit comprising a diode, a current generator (I_{ph}) and a combination of series and parallel resistances (r_s, r_p). Figure B.1a and B1.b illustrate the circuit equivalent model for p-type (p^+pn^+) and n-type (n^+np^+) cells on foreign substrate, respectively. There are various circuit components. If we consider it only in terms of series resistance, there is a contribution of base (r_b) and emitter (r_e) as shown in Figure B.1a and B.1b. Due to the inverse of the cell configuration, the current direction also becomes inverse as shown in the figure.

When a load (or illumination) is present, a potential difference develops between the terminals of the cell. This potential difference generates a current, which acts in the opposite direction to the photocurrent, and the net current is reduced from its short circuit value. This reverse current is usually called the dark current in analogy with the current I_{dark}(V) which flows across the device under an applied voltage, or bias, V in the dark. Most solar cells behave like a diode in the dark. For an ideal diode the dark current density J_{dark}(V) varies as

$$J_{dark}(V) = J_o\left(e^{qV/kT} - 1\right) \tag{B.1}$$

where J_o is the saturation current, k is Boltzmann's constant and T is temperature in Kelvin.

The typical current-voltage characteristic of a solar cell is presented in Figure B.1c. In the case of the simple model for a diode, this $I(V)$ characteristic can be determined by following equations:

$$I = I_{ph} - I_{dark}(V) \tag{B.2}$$

$$I = I_{ph} - \frac{V + IR_s}{R_p} - I_o\left[\exp\left(\frac{q(V + IR_s)}{nkT}\right) - 1\right] \tag{B.3}$$

This can explain the losses by recombination of the minority carriers. These losses can be localised in volume of the quasi-neutrals areas (n, p), on front and back surfaces of the cell or on the level of the space charge region.

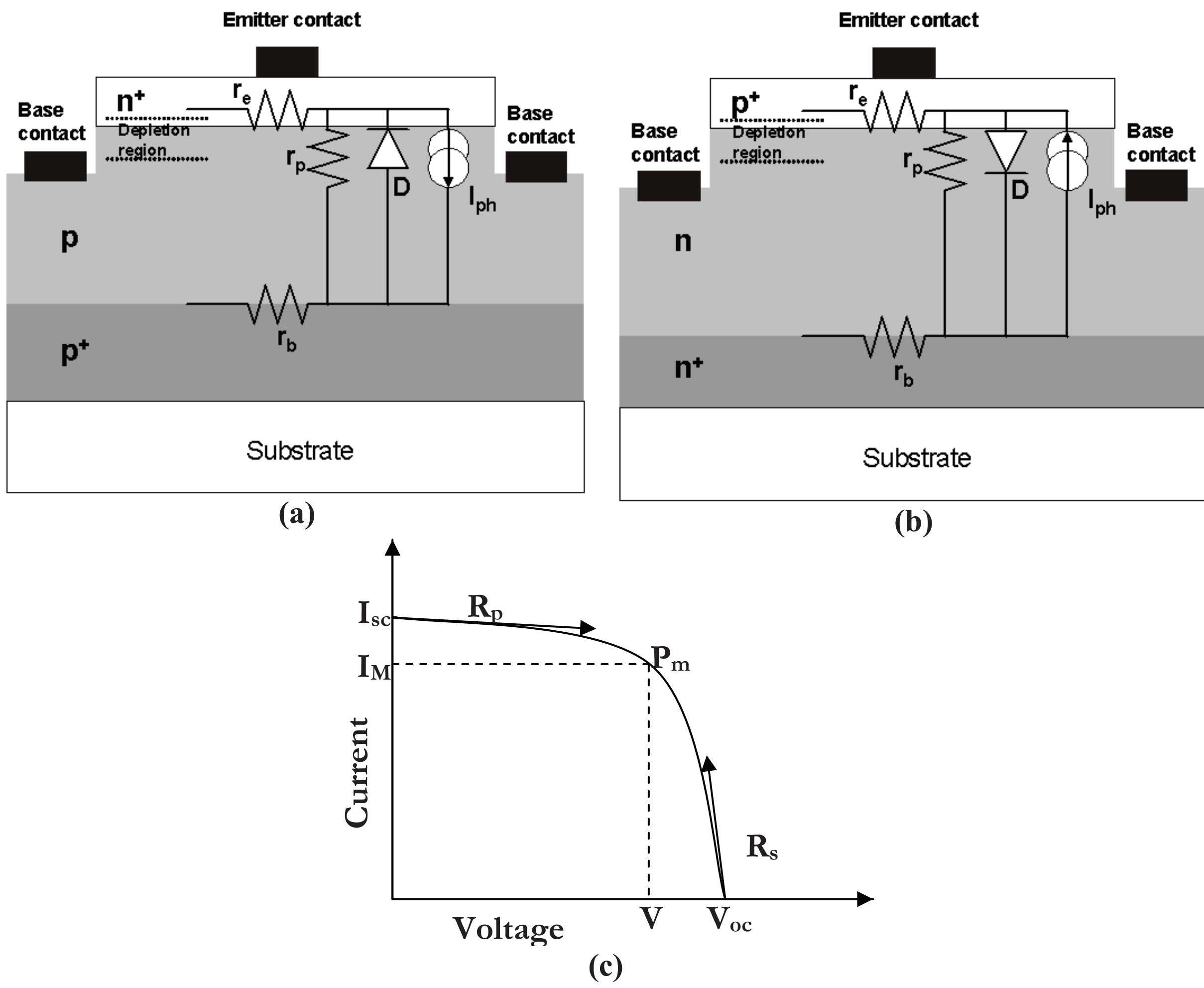

Figure B.1: Equivalent circuit of a diode model for: (a) p-type, and (b) n-type cell configurations. Current-voltage characteristic under illumination is shown in (c).

Among significant parameters of the solar cell that can be extracted from current-voltage curves are the equivalent series and parallel resistances. The value of the series resistance R_s, is typically much lower than the parallel resistance R_p (sometimes referred to as the shunt resistance R_{sh}). For the ideal solar cell, R_s would be zero, and R_p would be infinite. Since, the effect of R_s is negligible near open circuit conditions, the slope of the current-voltage curve in that vicinity is an indicator of the value of R_p. Conversely, since the effect of R_p is negligible near short circuit conditions, the slope of the curve in that vicinity is an indicator of the value of R_s. As a physical meaning, series resistance is primarily due to the resistance of the semiconductor material and that of the metal/semiconductor contacts. In

addition, the physical mechanisms responsible for the appearance of parallel resistance are complex. The value of this resistance interprets the leakage of the carriers through the surface side of the junction and the presence of defects or metal impurities in the junction [1]. To maximize output statement, it is necessary to minimize series resistances and to maximize parallel resistance. The typical values of a good cell silicon are R_s~0.1Ω and R_p>103Ω.

When the contacts are isolated, the potential difference has its maximum value, the open circuit voltage V_{oc}. This is equivalent to the condition when the dark current and short circuit photocurrent exactly cancel out. For the ideal diode,

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{I_{sc}}{I_o} + 1\right) \quad \text{(B.4)}$$

Equation B.4 shows that V_{oc} increases logarithmically with light intensity. It should be noted that voltage is defined, so that the photovoltage occurs in forward bias ($V>0$). Figure B.1c shows that the current-voltage product is positive, and the cell generates power, when the voltage is between 0 and V_{oc}. At $V<0$, the illuminated device acts as a photodetector, consuming power to generate a photocurrent which is light dependent but bias independent. At $V>V_{oc}$, the device again consumes power. This is the regime where light emitting diodes operate.

The rectangle-defined V_{oc} and I_{sc} provide a convenient means for characterizing the maximum power point. The fill factor (FF) is a measure of the squareness of the current-voltage characteristic and is always less than one. It is the ratio of the areas of the two rectangles shown in Figure B.1c or

$$FF = \frac{P_M}{V_{oc} I_{sc}} = \frac{V_M I_M}{V_{oc} I_{sc}} \quad \text{(B.5)}$$

where P_M; V_M and I_M refer to maximum power, the voltage and the current for maximum power, respectively. Arguably, the most important figure of merit for a solar cell is its power conversion efficiency, η, which is defined as

$$\eta = \frac{P_M}{P_s} = \frac{I_M V_M}{P_s} = FF \frac{I_{sc} V_{oc}}{P_s} \quad \text{(B.6)}$$

The solar power, P_s, is determined by the properties of the light spectrum incident upon the solar cell. The four quantities; J_{sc}, V_{oc}, FF and η are the key performance characteristics of a solar cell. All of these should be defined for particular illumination

conditions. The Standard Test Condition (STC) for solar cells is the Air Mass 1.5 spectrum (AM1.5), an incident power density of $1000Wm^{-2}$, and a temperature of 25°C.

B.2 Quantum Efficiency and Spectral Response

It has been a long cherished a goal for people to improve the photo-electric conversion efficiency of a solar cell unendingly. According to the semiconductor theory, the current in a cell always includes the photo-generated current and the dark diode current, with the former being proportional to the incident light intensity and the latter being independent of it. Thus, the conversion efficiency relies on the photogenerated current and the diode property. Quantum efficiency (QE) is the ratio of the number of charge carriers collected by the solar cell to the number of photons of a given energy shining on the solar cell. QE, therefore, relates to the response of a solar cell to the various wavelengths in the spectrum of light shining on the cell. The QE is given as a function of either wavelength or energy. If all the photons of a certain wavelength are absorbed, and we collect the resulting minority carriers (for example, electrons in a p-type material), then the QE at that particular wavelength has a value of one. The QE for most solar cells is reduced because of the effects of recombination, where charge carriers are not able to move into an external circuit. The same mechanisms that affect the collection probability also affect the QE. For example, modifying the front surface can affect carriers generated near the surface. And because high-energy (blue) light is absorbed very close to the surface, considerable recombination at the front surface will affect the "blue" portion of the QE. To enhance the conversion efficiency one has to raise the QE since the photogenerated current strongly relates to the quantum efficiency (QE, the number of electron-hole pairs generated per incident photon). From theoretical aspect, the QE corresponds to the spectral response (SR), which determines the spectral distribution of the short circuit current I_{SC}. By calculating the QE, both SR and the contributions to the I_{SC} of different wavelengths can be determined, helping one to analyze quantum yields from the different cell regions. So, it is very useful to calculate the QE for promoting the performance of a cell. The QE involves EQE and IQE, which stand for external quantum efficiency and internal quantum efficiency, respectively, with the latter defined as the number of minority carriers contributing to the short circuit current divided by the number of photons entering the cell. External Quantum Efficiency (EQE) is the ratio of the number of charge carriers collected by the solar cell to the number of photons of a given energy shining on the solar cell from outside. Internal Quantum Efficiency (IQE) is the ratio of the number of charge carriers

collected by the solar cell to the number of photons of a given energy that shine on the solar cell from outside and are not reflected back by the cell, nor penetrate through. The IQE is always larger than the EQE. A low IQE indicates that the active layer of the solar cell is unable to make good use of the photons. A low EQE can indicate that a lot of the light was reflected. In experiment, the IQE can be obtained through the light reflectance and the SR. The QE spectrum reflects the cell design and the material quality. For a p-n cell the short wavelength response is provided at the front of the cell. Since, carriers generated near the front surface are susceptible to surface recombination, the short wavelength QE is particularly sensitive to the surface recombination velocity. S_n may be reduced by introducing a window layer or pasivating the surface. Long wavelength QE is affected by the back surface quality and the thickness of the cell. The abruptness of the QE edge reflects the form of the absorption. At intermediate wavelengths, carriers are generated in the space charge region (scr). The various contributions to the QE are shown in Figure B.2. As shown in the figure, we can see that for photons with higher energy (λ<0.4μm), the emitter contributes more to the IQE than the base, and the scr do due to a greater absorption for those photons, which leads to a higher generation rate in the region. On the other hand, for photons with smaller energy the absorption coefficients are also smaller, which leads to a higher generation rate in the base and hence more contribution to the IQE from this region. What is of interest is that the total IQE curve doesn't vary monotonously as the wavelengths, but has a peak value around 0.5μm. This is useful for optimally matching a solar cell with the sun spectrum. The overall magnitude of the IQE is affected by the efficiency of light absorption. It may be increased by reducing reflection losses, by increasing the width of the cell or by light trapping techniques.

To reach the response of the cell with respect to the localization of absorption, we can exploit the spectral responses (SR). Therefore, mathematically, dividing the measured cell current $I_{SC}(\lambda)$ by the light intensity $I_{light}(\lambda)$ gives the SR as

$$SR(\lambda) = \frac{I_{SC}(\lambda)}{I_{light}(\lambda)} \tag{B.7}$$

External quantum efficiency gives the fraction of the charge carriers contributing to I_{sc} current compared to the number of the incidental photons for a given wavelength:

$$EQE(\lambda) = \frac{hc}{e\lambda} SR(\lambda) \tag{B.8}$$

with h is the Planck constant, c is the speed of the light in the vacuum and e is the electron charge, λ is the free-space wavelength and hc/e=1239.84V.nm.

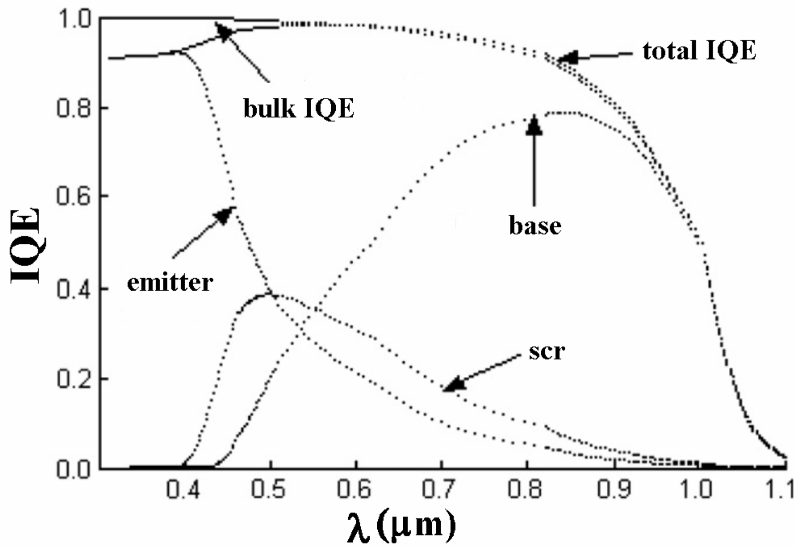

Figure B.2: Contributions of the base, emitter and space charge region (scr) to the IQEs [2].

By taking into account of the losses by total reflectivity ($R(\lambda)$), we can determine the number of the photons interacting with silicon, which defines the notion of internal quantum efficiency IQE:

$$IQE(\lambda) = \frac{EQE(\lambda)}{(1-R(\lambda))} = \frac{1}{(1-R(\lambda))}\frac{hc}{e\lambda}SR(\lambda) \tag{B.9}$$

Internal quantum efficiency is intended to represent the fraction of minority carriers photogenerated in the cell, which are collected under short-circuit conditions, and is the sum of the contributions of emitter (IQE_e), the space charge region (IQE_{scr}) and base (IQE_b). For the thick layers, it is possible to determine the base minority carriers' diffusion length from the measurements of internal quantum efficiency. The absorption of light depends on the wavelength: smaller the wavelength, higher the absorption. Minority carriers generated deep in the base by long wavelength photons have to diffuse a longer distance to the collecting emitter than minority carriers generated by short wavelength photons. As a consequence, the IQE provides information about the diffusion length of the minority charge carriers. For that reason, it is necessary to plot inverse internal quantum efficiency (IQE^{-1}) versus penetration depth (α^{-1}) in the wavelength range of 800 to 950nm. In this area, the contributions of the emitter and space charge region with the current are negligible. The expression of $IQE^{-1} = f(\alpha^{-1})$ usually used in the photovoltaic field in order to determine the diffusion lengths is given by the following [3]:

$$IQE^{-1} \approx 1+\frac{1}{L_{eff}}\alpha^{-1} \text{ with } L_{eff} = L_b \frac{1+S_b \frac{L_n}{D_b}\tanh\left(\frac{X_b}{L_b}\right)}{\frac{S_b}{D_b}+\tanh\left(\frac{X_b}{L_b}\right)} \tag{B.10}$$

where L_{eff} is the effective diffusion length, L_b is the diffusion length of the base minority carriers, S_b is the back surface recombination velocity, X_b is the thickness of the base and D_b is the minority carrier diffusion constant in the base. The conventional method used to determine the diffusion length L_b from the internal quantum efficiency is based on the idea that the latter can be approximated by a simple expression, which is a function of L_b and of the light absorption coefficient (α) only. The validity of this expression is however restricted to cases in which the diffusion lengths L_b significantly lower than X_b (i.e. $L_b<<X_b$), so that the back surface recombination velocity S_b does not have a significant effect and the effective diffusion length L_{eff} becomes close or equal to L_b. In this case, the plot of IQE^{-1} vs α^{-1} is linear for absorption lengths (α^{-1}) greater than the junction depth but shorter than the device thickness. The inverse of this slope is equal to the minority carrier diffusion length in the base region [4]. Thus, the expression of inverse quantum efficiency (Equation B.10) is given by [5]:

$$IQE^{-1} \approx \frac{1}{\alpha(x_j + L_b)} \tag{B.11}$$

where x_j is the junction depth. Finally, we can deduce a slope whose reverse gives an effective diffusion length L_{eff} equal to the sum of (L_b +x_j).

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E-MRS Spring Meeting 2004 (Symposium P: Filled and Nano-Composite Polymer Materials), Strasbourg, France, 2004.

[22] Larysa Fenenko, Petro Smertenko, Sergey Svechnikov, Nikolay Guba, Ludmila Grebinskaja, L. V. Pisarzhevski, Sener Oktik, **Ozge Tuzun**, "Peculiarities of Charge Flow and Charge Effects in Polymer Film Structures", *ICEPOM-5 Conference (Electronic Processes in Organic Materials)*, Kyiv, Ukraine, 2004.

Résumé court : Dans ce travail, nous avons étudié d'abord la croissance du silicium polycristallin (couche germe AIC) sur substrats d'alumine ou vitrocéramiques par le procédé de cristallisation induit par aluminium du silicium amorphe. Les études ont concerné la cinétique de croissance de la couche AIC en fonction de plusieurs paramètres expérimentaux (température, temps, épaisseur du film Si amorphe, teneur en hydrogène,…) et la détermination des défauts de structure inter-grains (joints) et intra-grains (macles). En utilisant des verres céramiques, nous avons pu réaliser des films poly-Si à T<500°C, présentant une taille moyenne de grains cent fois supérieure à son épaisseur (0.2µm d'épaisseur et 26µm en taille de grains), et des grains majoritairement orientés <100>. Nous avons montré que la densité des macles, en particulier Σ3, est réduite en diminuant la température de cristallisation. Nous avons également recherché à réaliser des films tampons de type n par surdopage et évaluer leurs efficacités. En variant les conditions expérimentales, des couches n^+ avec des concentrations de porteurs libres de 10^{19} à $6\times10^{20}cm^{-3}$ et des mobilités de $50\text{-}60cm^2/Vs$ ont pu être réalisées sur des couches de 0.2µm. Nous avons utilisé deux méthodes de croissance de la couche absorbante: l'épitaxie en phase vapeur (VPE) à haute température ou l'épitaxie en phase solide (SPE) par dépôt d'une couche Si amorphe et recuit. Nous avons particulièrement mis en évidence la formation d'une distribution graduelle n^+n très souhaitable pour les composants photovoltaïques. Enfin nous avons réalisé des cellules photovoltaïques sur ces matériaux afin de valider leur potentiel pour la future génération de cellules solaires. Nous avons ainsi réalisé des structures de cellules de configuration p^+pn^+ sur poly-Si de type p mais également des configurations n^+np^+ sur poly-Si de type n. Nous avons mesuré un rendement de l'ordre de 5.5% (6.1% en Sun-V_{oc} et en considérant la surface active), pour les cellules préparées par VPE sur couche tampon n-AIC. Il faut rappeler qu'aucun confinement optique ni architecture spécifique n'a été utilisé. Les caractéristiques impliquant les mesures des différentes grandeurs des cellules et la réponse spectrale, ont permis une analyse fine des régions de pertes de la conversion.

Mots clés : Silicium polycristallin, Couche mince, Cristallisation induite par aluminium, Epitaxie, Cellule photovoltaïque

Short Summary : In this work, we have prepared p- and n-type polycrystalline silicon seed layers by aluminum-induced crystallization (AIC) of a-Si on alumina and glass-ceramic substrates, followed by epitaxial thickening using low pressure chemical vapor deposition (LPCVD); and HIT solar cells (Heterojunction with Intrinsic Thin layer) were then fabricated. Polycrystalline silicon layer with quite large grains with an average grain size value of ~26µm, that is one hundred times more than thickness of AIC layer (0.2µm), can be formed by AIC technique at 475°C on glass-ceramic substrate. The preferred orientation is <100> independently from substrate and exchange annealing temperature. The main crystallographic defect is Σ3 that is reduced by lowering the annealing temperature. We used two methods for the growth of the absorber layer: vapor phase epitaxy (VPE) at high temperature or solid phase epitaxy (SPE) by depositing an amorphous Si layer and following annealing. The grain size conservation for epitaxial layers was observed with that of the underlying AIC poly-Si seed layer. We especially highlighted the formation of a n^+n graded structure, which is very desirable for photovoltaic components. Finally, we have made solar cells on these materials to validate their potential for future generation solar cells. In addition to p-type cell (p^+pn^+), we have prepared for the first time n-type based polysilicon solar cells (n^+np^+) with AIC approach on alumina substrate. An efficiency of about 5.5% realized in our n-type cells without texturization that should be compared to 3.2% for p-type cells. In addition to cell efficiency, the spectral response of the n-type cell is also much wider than that of p-type cell, over a large part of the spectrum. This lead to an enhancement in L_{eff} for n-type cell (~2.6µm) compared to that of p-type (0.9µm). Analysis of the best n-type based cells with Sun-V_{oc} apparatus, neglecting therefore the contacts resistivity, led to an efficiency value of 6.1%, showing the potential of the n-type polysilicon solar cells without any optimisation of the hydrogenation step, the heterojunction passivation and junction formation, nor the surface texturing.

Keywords: Polycrystalline silicon, Thin film, Aluminium induced crystallization, Epitaxy, Solar cells