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Développement de capteurs à pixels résistants aux rayonnements intenses pour la détection de particules chargées.

Development of radiation hardened pixel sensors for charged particle detection.

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Introduction

In order to unravel the mysteries of matter, forces, and the building blocks of our universe, subatomic physics experiments are built all over the world. This PhD thesis aims at contributing to the development of a new type of position sensitive detector composing heavy-ion experiments looking for Quark-Gluon Plasma formation. The detectors concerned are those which allow determining the spatial origin of particles created in the vicinity of the beam-interaction region. To determine the spatial origin of particles created in the collisions, one relies usually on a vertex detector composed of silicon-based pixel sensors. Pixel sensors will in particular equip the Micro Vertex Detector (MVD) of the Compressed Baryonic Matter (CBM) experiment, planed at the FAIR accelerator (GSI/Darmstadt). The specifications of the MVD are particulary demanding: its physics goals require sensors with every low material budget, short readout time, and the radiation tolerance adapted to > 1 Mrad/year (ionizing) and $> 10^{13}$ n_{eq}/cm^2/year (non-ionizing) particle doses.

The CMOS[1] pixel sensors developed at the Institut Pluridisciplinaire Hubert Curien (IPHC) in Strasbourg (France) are considered as particularly interesting technology for the CBM-MVD. These sensors offer an attractive compromise between the most crucial parameters. However, when this PhD thesis started, CMOS pixel sensors were unable to provide the performance which meets the CBM-MVD specifications: the radiation hardness and readout time required improvements. This PhD thesis concentrated on enhancing the radiation tolerance of CMOS sensors to the level needed for the physics program relying on the MVD performance. The studies presented here were ongoing at the IPHC-Strasbourg.

A part of this thesis was also devoted to the Charge-Coupled Devices (CCDs), which were proposed to equip the vertex detectors of the International Linear Collider experiments. This work was a part of the LCFI collaboration[2] R&D program and it was carried out in the Department of Physics of the Lancaster and Liverpool Universities (United Kingdom).

Radiation hardness of Monolithic Active Pixel Sensors

CMOS pixel sensors, called also Monolithic Active Pixel Sensors (MAPS), integrate the sensing elements and the processing electronics on the same substrate. These sensors feature thin sensitive volume, limited to an epitaxial layer (EPI layer), and they can be thinned down to about 50 μm or even less, providing a low material budget. The sensing volume of MAPS that have been studied so far was composed of a low-resistivity silicon, which could not be

[1] CMOS stands for Complementary Metal Oxide Semiconductor
[2] Linear Collider Flavour Identification collaboration

depleted using standard CMOS voltages. Thus, the charge-transport process from the EPI layer to sensing diodes occurred due to thermal diffusion. The signal charge was spread out over several neighboring pixels. As a consequence, the device was too sensitive to non-ionizing radiation to match the CBM specification.

The MAPS that have been developed so far were featuring an analog output, and they were produced to assess the technology detection characteristics. The achieved detection efficiency (ϵ_{det}, Section 4.2.4) for that type of sensors was typically above 99.5%, even after a substantial sensor irradiation. The readout was sequential and rather slow because the analog outputs of these devices were providing information about all pixels without selecting only those with useful signals. Consequently, these devices could not meet the readout time demanding experimental conditions such as those of the CBM experiment.

In order to decrease the readout time, MAPS were organized in columns which were read out in parallel. Moreover, functionalities selecting the pixels containing useful signals and sending information about their position to the outside world were implemented inside the chip data sparsification logic. This selection was performed by a simple column comparator. For the purpose of the column-parallel readout, pixels had to be modified and became more complex than the "classical" ones, without advanced signal processing. This complexity resulted in a potential sensitivity to ionizing radiation.

The main object of this PhD thesis was to study the impact of radiation on such advanced devices and to improve their tolerance to radiation. The studies described in this document were undertaken in two steps. The first one aimed at assessing for the first time the tolerance of MAPS with a column-parallel architecture to radiation and to define the most radiation-tolerant in-pixel architecture. The second step was devoted to the identification of the elements particularly sensitive to ionizing radiation and to a consecutive optimization of the in-pixel architecture. The sensors with column-parallel readout studied in the framework of this thesis were featuring low-resistivity sensitive volume. As a consequence, to achieve the required sensor performance, the architecture optimization was focused on the electronic noise minimization.

Studies carried out in the past showed that the non-ionizing radiation tolerance of MAPS based on a low-resistivity EPI layer depends strongly on a pitch size. It was concluded that the reduction of the pitch size improves the sensor tolerance to non-ionizing radiation. This was in contradiction with the requirements of column-parallel sensors development calling for a pitch large enough to fit the in-pixel-signal-processing electronics. Consequently, it was difficult to provide sensors for applications requiring at the same time high radiation tolerance and short readout time.

This strong imbalance motivated investigations of other solutions which could overcome the existing limitations. The studies presented in this thesis addressed several CMOS processes with features that allow improving the radiation tolerance without reducing the pixel pitch.

Technologies based on EPI layers where the charge transport is enhanced by an internal electric field were of particular interest. The charge transfer in such EPI layers is supposed to be faster and more focalized than the one which undergo a thermal diffusion process. As a consequence, a higher signal on individual pixels, thus also a higher signal over noise ratio, is expected. In addition, a faster charge collection should limit significantly the device sensitivity to radiation-induced traps. Due to these features, MAPS based on an EPI layer with enhanced charge collection should be more radiation tolerant.

Modeling of the radiation effects in the Charge-Coupled Devices

A part of this thesis was also devoted to the radiation tolerance of Charge-Coupled Devices, within the framework of the LCFI project settled in the United Kingdom. The CCDs have been proposed to supply the vertex detector of experiments planned for the International Linear Collider. These devices demonstrated excellent performance regarding spatial resolution (σ_{res}, see Section 4.2.4) and material budget. However, their readout time and radiation hardness, particularly against the non-ionizing radiation, were far from the ones required for upcoming high energy physics experiments.

In order to improve the readout time, the development of the CCDs focused on sensors featuring a column-parallel architecture. One of the key questions was related to the radiation tolerance of this type of devices. Due to the CCD's readout scheme, charges generated by impinging particles have to travel a long way inside the silicon before being transferred to the output buffer. Thus, the charge transfer is very sensitive to bulk damages introduced by non-ionizing radiation. This fact prompted the studies performed within the scope of this work on the Charge Transfer Inefficiency (CTI), which refers to the charge loss during its transfer from the point where it was generated to the CCD output buffer.

The work presented in this thesis addresses the development of the TCAD simulation model to assess the radiation effects in column-parallel CCDs[3].

Thesis layout

The achieved parameters of CMOS sensors were already matching specifications of numerous potential applications demanding a high spatial resolution and a low material budget. However, for the most demanding among of those applications, there was still a gap to bridge in terms of radiation tolerance and readout time. The particularly demanding CBM experiment is emblematic for the necessity to improve the MAPS performance.

This thesis concentrated predominantly on radiation tolerance improvement of CMOS pixel sensors. The document is subdivided into seven chapters.

Chapter 1 aims at explaining the origin of requirements regarding the vertex detector mounted near the target of the CBM experiment. Later in this chapter, the requirements

[3]This work was performed while spending 1.5 years in the Department of Physics of the Lancaster and Liverpool Universities (United Kingdom).

imposed by other CMOS-sensor applications are presented.

Chapter 2 introduces the currently available position sensitive silicon sensors and their features regarding material budget, readout time, σ_{res} and radiation hardness. Some trends in the R&D on silicon sensors are discussed next. The performance of the currently available pixel sensors is compared to the requirements of the high energy physics applications presented in Chapter 1, particulary to the CBM-MVD specifications.

Chapter 3 focuses on interactions of particles with matter and their consequences to particle detection with semiconductor detectors. Later in this chapter, the most important aspects regarding the mechanisms of ionizing and non-ionizing radiation damage creation in electronic devices will be discussed.

Chapter 4 provides complete knowledge related to MAPS: their basic architectures, noise sources, and readout schemes are presented. The pros and cons of this type of sensor are also discussed. This chapter delivers the necessary information related to the MAPS characterization carried out within the scope of this thesis. This chapter discusses as well the influence of ionizing and non-ionizing radiation on the CMOS-sensor performance. The past studies and the major observations regarding the radiation tolerance of MAPS are discussed. The discussion is based on the results obtained with several MIMOSA[4] sensors.

Chapter 5 focuses on the studies related to the radiation tolerance of MAPS with column-parallel architecture. At the beginning, it explains the motivation for the R&D on column-parallel MAPS and introduces briefly the past developments. Next, the first radiation-tolerance assessment of a sensor featuring a column-parallel readout is addressed with several devices based on a standard CMOS 0.35 μm process featuring a low resistivity EPI layer. The studies related to the radiation tolerance of different in-pixel amplifier architectures are presented. Later, the report focuses on the investigation of the in-pixel amplifier elements, expected to be particularly sensitive to ionizing radiation. These studies are addressed with MAPS featuring a column-parallel readout.

Chapter 6 addresses the radiation tolerance of different CMOS processes featuring an EPI layer with enhanced charge collection. First, the radiation tolerance of a BiCMOS technology providing a graded EPI layer is investigated. Secondly, the radiation hardness of sensors based on a high resistivity EPI layer is presented. At the end, a CMOS process equivalent to the currently leading one (AMS[5]-OPTO[6] 0.35-μm) is characterized. The studies on this process were prompted by the fact that, in the near future, this technology is expected to be based on a high resistivity EPI layer.

Chapter 7 concentrates on the modeling of the radiation effects in the Charge-Coupled Devices.

[4]MIMOSA - Minimum Ionizing particle MOS Active pixel sensor.
[5]AMS - **A**ustria**M**icro**S**ystems
[6]The CMOS Opto process option provides enhanced optical sensitivity for embedded photodiodes and high density CMOS camera products.

1 CMOS-sensor applications

1.1 High-energy physics experiments

Since many ages, the human beings have been attracted by questions provoking in their minds a deep understanding of the Universe. The laws governing the particles and their interactions were encapsulated in a quantum field theory called the Standard Model. This model describes our universe made of six types of quarks and six types of leptons, interacting with each other's via three fundamental forces: strong, weak, and electromagnetic.

The Standard Model has been confirmed by numerous high-precision experiments. Nevertheless, it is not yet the complete theory of fundamental interactions: for example it does not account for dark matter and dark energy, and it does not include gravitation.

In order to extend our current understanding of the subatomic world, dedicated experiments are built. They use particle beam of very high energies, and they are composed of several different subsystems to reconstruct the particle properties. Vertex detectors are used to reconstruct, with high precision needed to separate primary and secondary vertices, the particle trajectories close to the interaction point.

Vertex detectors are based on silicon sensors, sensitive to charged particles. Monolithic Active Pixel Sensors developed at IPHC[1] have been proposed for vertex detectors of several high-energy physics experiments: the ongoing STAR [1] experiment upgrade at RHIC, the Compressed Baryonic Matter (CBM) experiment at FAIR [2] (planned for 2017) and the International Linear Collider (ILC) [3] (foreseen after 2020). These sensors have to achieve performance which reflects an ambitious balance between readout time, radiation tolerance, σ_{res} and material budget. These requirements will be illustrated with one of the most demanding case: the CBM experiment. The requirements related to other MAPS applications, including beam telescopes, will be reviewed later in this chapter.

1.1.1 Understanding of the requirements - the CBM experiment as an example

Quarks are confined inside hadrons. However, it is supposed that in special conditions (e.g. those existing in neutron stars or few microseconds after the Big Bang) quarks and gluons are deconfined, and they can move freely in a state of matter called Quark Gluon Plasma (QGP). The CBM experiment aims at creating the QGP by colliding gold ions with a fixed target, also made of gold. The CBM detector is presented in Figure 1.1.

[1] IPHC - Institut Pluridisciplinaire Hubert Curien, Strasbourg, France.

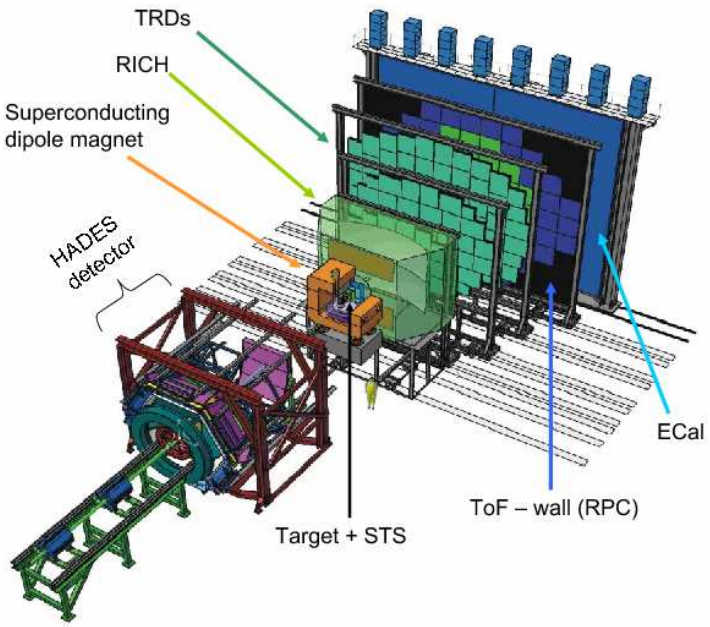


Figure 1.1: The CBM experiment. The picture illustrates the setup optimized with respect to open charm and electron/positron measurements. The first two stations of the Silicon Tracking System (STS) will be equipped with high-granular, fast and radiation-tolerant pixel sensors (figure taken from [4]).

There are several probes proposed for studying the QGP. Among those, the open charm mesons (D^0 and $D^{\pm}$) whose production cross-section could be modified by the presence of the QGP [4]. The open charm mesons cannot be accessed directly by any detector since they decay at a distance of a few hundred microns from the interaction point. Their benchmark hadronic decays $D^0 \rightarrow K^-\pi^+$ and $D^{\pm} \rightarrow K^{\mp}\pi^{\pm}\pi^{\pm}$ can be identified by studying their decay products. The impact parameter of the extrapolated track to the particle production point (see Figure 1.2) is of primary interest. The capability to reconstruct secondary vertices is usually expressed by the resolution on the track impact parameter: σ_{IP}. This resolution has to be adequate in order to distinguish tracks originating either from a primary or a secondary vertex. The σ_{IP} strongly depends on the characteristics (geometry, resolution, material budget) of the vertex detector.

The impact parameter resolution is frequently given by the approximated but compact relationship:

$$\sigma_{IP} = a \oplus \frac{b}{p \cdot sin^{3/2}(\theta)} \tag{1.1}$$

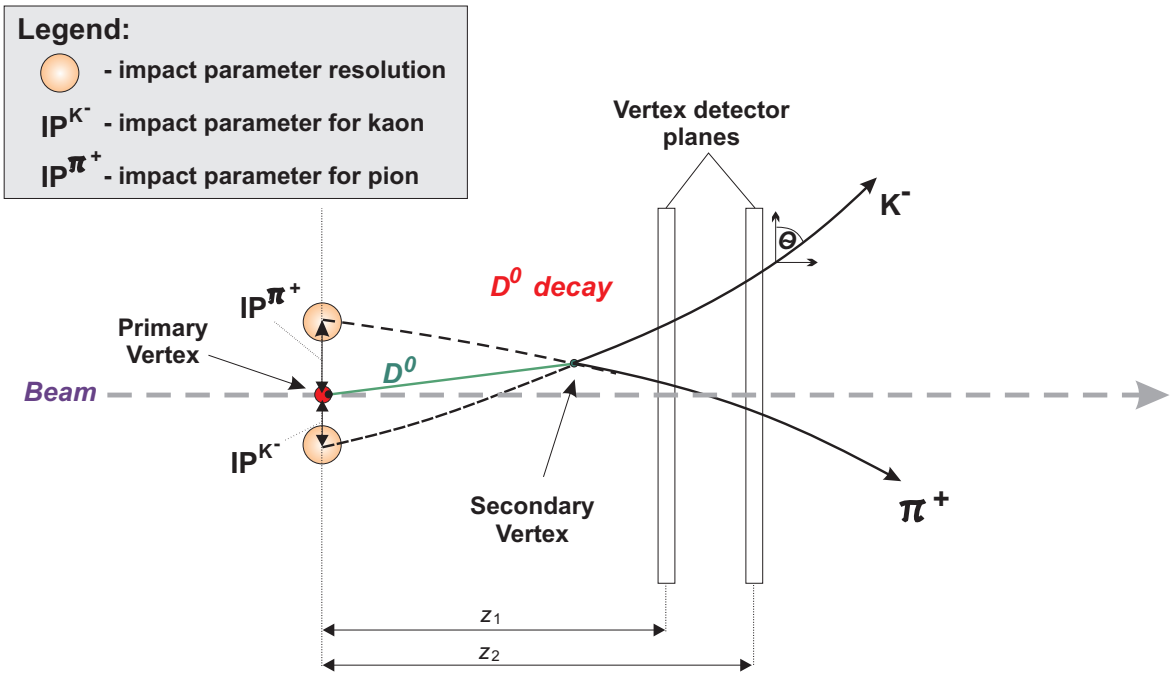


Figure 1.2: The principle of the track reconstruction of a short-lived particle with a 2-station vertex detector. The trajectories of the charged particles are displayed curved due to a magnetic field they traverse. Here, a decay of a D^0 meson to charged kaon and pion. Due to the very short life time of the D^0, the outstanding spatial resolution of the vertex detector is needed to distinguish the primary vertex from the secondary one.

For the simple geometry illustrated in Figure 1.2 the parameter a is defined as:

$$a = \frac{z_1\sigma_2 \oplus z_2\sigma_1}{z_2 - z_1} \tag{1.2}$$

where σ_1 and σ_2 corresponds to the spatial resolution of the reference planes, and z_1 and z_2 are the distances from the interaction point of the first and second plane, respectively.

The parameter b is governed by the multiple scattering (which depends on the thickness x of the sensors that are composing the vertex detector) the momentum p, and the crossing angle θ of the impinging particle:

$$b = z_1 \cdot \frac{q_p \cdot 13.6MeV}{\beta c} \cdot \sqrt{\frac{x}{X_0 sin(\theta)}} \left[1 + 0.038ln\left(\frac{x}{X_0 sin(\theta)}\right)\right] \tag{1.3}$$

where $\beta = \frac{v}{c}$, v is the particle speed, c is the speed of light, q_p is the charge of the particle, and X_0 is the material budget[2].

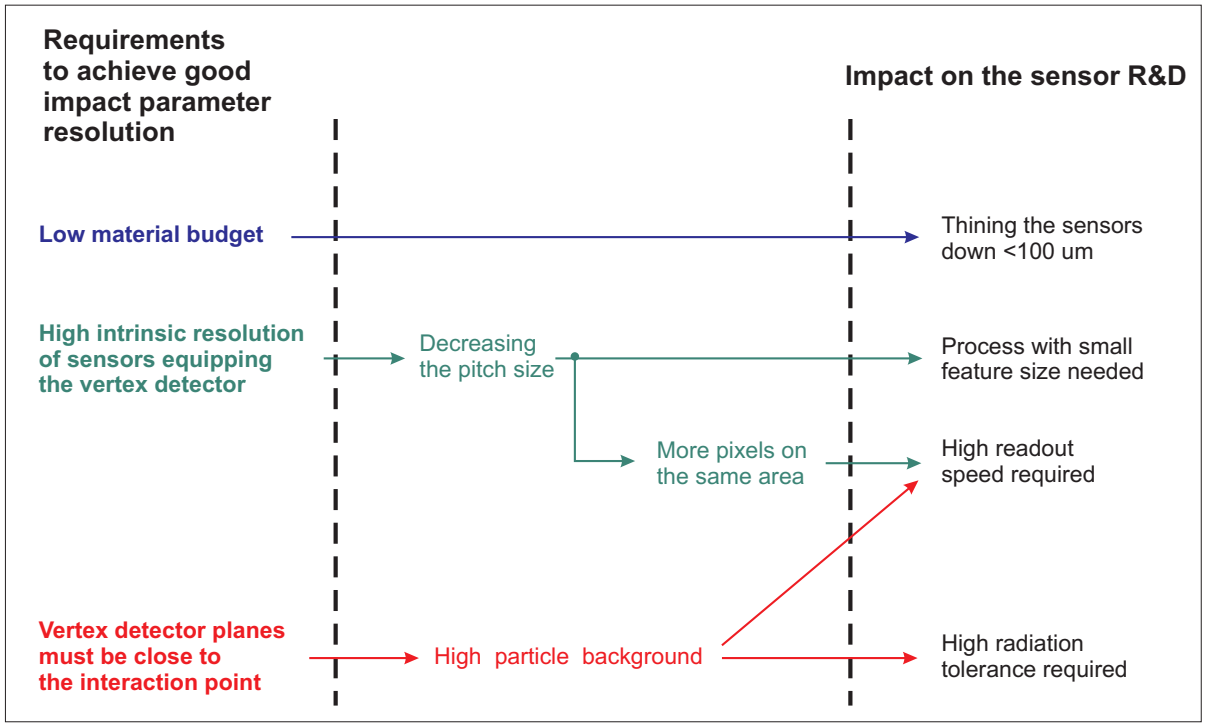


Figure 1.3: The influence of the impact parameter required on the sensor performance. The figure illustrates the trade-off between the small pixel pitch required to achieve high σ_{res}, and the fast readout time calling for pixels with larger areas.

To achieve the required σ_{IP}, the vertex detector must be composed of sensors featuring a

[2]Material budget is related to the thickness and properties of a given material. This thickness is expressed usually in units called radiation length X_0. The latter corresponds to the material thickness within which a high energy electron loses all but $1/e$ of its kinetic energy. X_0 for silicon amounts to 9.36 cm [5].

high intrinsic σ_{res} and a low material budget. Moreover, the first plane should be placed as close as possible to the interaction point. These facts have a direct impact on the silicon detector R&D, as it is illustrated in Figure 1.3. To achieve a low material budget, sensors featuring a thin sensitive volume are preferred[3]. The need for a high σ_{res} leads to the decrease in the pixel pitch. A larger pixel density follows, which translates into an increased readout time and power consumption. The small distance of the vertex detector planes relative to the interaction point results in a large particle background, inducing radiation damage and a high occupancy that the sensors have to cope with.

The CBM experiment requirements.

The MVD of CBM is composed of two circular planes. They will be located at 5 cm and 10 cm downstream of the target and will feature an outer radius of 2.5 cm and 5 cm for the first and for the second plane, respectively. Both planes have circular opening of 0.55 cm radius to let the primary beam pass through.

To meet the physics goals of the CBM experiment, the required σ_{IP} has to be about $\sim$45 µm [6]. This imposes the following requirements on the vertex detector: a material budget on the order of a few 0.1% X_0 per plane and an intrinsic σ_{res} not exceeding 5 µm, both calling for thin and highly granular sensors. With nominal interaction rate of 10^7 Au-Au collisions per second, which ensures a good statistics to meet the physics goals of the CBM experiment, the particle background and radiation levels will become relevant. To cope with the high background, the detector planes will have to ensure the readout time of $\leq$100 ns. Concerning radiation damage, the sensors mounted on the first plane will be exposed to fluences of $\sim 2 \cdot 10^{15}$ $\mathrm{n_{eq}/cm^2}$ and doses of $\sim$340 Mrad [7].

The CBM experiment requirements are extremely ambitious. Presently, there is no technology available that fulfills all of them. For this reason, a less constraining scenario, but still allowing for precise measurements, was proposed. In this scenario, the number of interactions per second is limited to 10^5 [8]. This reduces the non-ionizing radiation fluence and the ionizing radiation dose on the sensors mounted on the innermost layer to about $1 \cdot 10^{13}$ $\mathrm{n_{eq}/cm^2}$ and several Mrad. The required time resolution is about 30 µs. All requirements for pixel sensors equipping the CBM-MVD in this option are shown in Table 1.1.

MAPS[4] are the most promising pixel sensor technology to equip the MVD of the CBM experiment. However, the existing devices cannot meet all of the CBM requirements. Namely, the readout time and radiation hardness are not adequate. This work is a part of the R&D program of the CMOS group from IPHC-Strasbourg and aims at improving the tolerance to radiation of CMOS pixel sensors.

[3] Thin sensitive volume allows for thinning sensors down without performance loss (Chapter 4).

[4] Monolithic Active Pixel Sensors (MAPS). They are the main subject of this thesis and will be described in details in Chapter 4.

Table 1.1: Performance requirements for the sensors composing the CBM Micro Vertex Detector.

CBM-MVD requirements	
Non-ionizing radiation tolerance	$>10^{13}$ n_{eq}/cm^2
Ionizing radiation tolerance	>3 Mrad
σ_{res}	5µm
Material budget per station	$<0.3\% X_0$
Time resolution	30 µs
Power consumption	<2 W/cm^2
Operating temperature	O (-20) °C

1.1.2 Upgrade of the STAR experiment.

The ongoing upgrade of the STAR vertex detector is the first application of CMOS sensors in a high-energy physics experiment. The main goal of the STAR experiment is to search for signatures of the QGP. The gold ions are accelerated at energies up to 250 GeV by the Relativistic Heavy Ion Collider (RHIC) and collide inside the STAR detector shown in Figure 1.4.

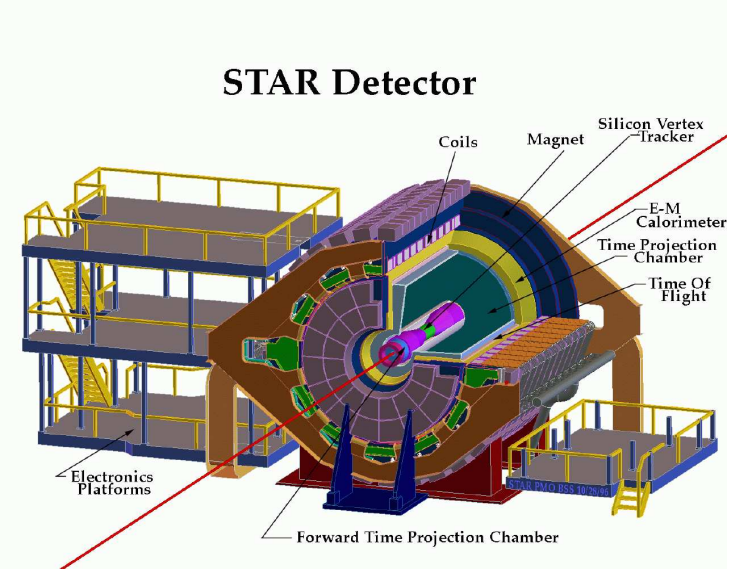


Figure 1.4: The STAR detector [9].

The STAR collaboration plans to extend the current capabilities of the detector. In order to improve the tagging efficiency of short-lived particles such as b- and c-mesons by measuring their displaced vertex, the following impact parameter resolution is needed:

$$\sigma_{IP} \leqslant 13\mu m \oplus \frac{19\mu m}{p \cdot sin^{3/2}(\theta)}[GeV/c] \tag{1.4}$$

This will be achieved by adding two concentric layers of MAPS at distances of 2.5 cm and 8 cm from the collision point [10].

Table 1.2: Specification of the CMOS sensors equipping the STAR pixel detector.

Requirements of the STAR experiment upgrade	
Non-ionizing radiation tolerance	$\sim 3{\cdot}10^{12}$ $\mathrm{n_{eq}/cm^2}$
Ionizing radiation tolerance	$\sim$150 krad
σ_{res}	$< 10\mu$m
Material budget per ladder	$< 0.4\% X_0$
Time resolution	$\leqslant 200\mu$s
Power consumption	$\leqslant 150$ mW/cm^2

The sensor constraints imposed by the physics goals and the running conditions are summarized in Table 1.2. The sensors should withstand 300 krad of integrated dose and a non-ionizing radiation fluence of $1{\cdot}10^{13}$ $\mathrm{n_{eq}/cm^2}$. A further constraint comes from the fact that only an air cooling can be applied to the vertex detector. The working temperature will then be in the range of 20-30 °C. The radiation damage of sensors and the temperature regime where they are expected to operate may imply significant leakage currents, leading to the increase in the electronic noise. Therefore, MAPS dedicated for the STAR experiment upgrade were designed to provide the required performance even in such hard conditions.

1.1.3 The International Linear Collider.

The ILC is a proposed linear accelerator which will collide electrons and positrons at a center of mass energy ranging up to 1 TeV. It will perform detailed investigations of the physics of the Standard Model, and beyond, complementing the coming studies at the Large Hadron Collider (LHC, [11]).

MAPS are promising candidates to equip the vertex detector foreseen for the International Large Detector (ILD), one of the two detector concepts proposed for the accelerator. The two alternative geometries for the ILD vertex detector are shown in Figure 1.5. The concept shown on the left side (technically more ambitious) implies three concentric, double-sided layers with sensors 2 mm apart. The other concept is based on 5 concentric layers of sensors.

The extremely ambitious physics goals require an impact parameter resolution as small as [3, 12]:

$$\sigma_{IP} \leqslant 5\mu m \oplus \frac{10\mu m}{p \cdot sin^{3/2}\theta}[GeV/c] \tag{1.5}$$

Values of σ_{IP} complying with this requirement can be obtained with very granular pixel sensors featuring an intrinsic resolution of 2-3 μm. However, to profit from performance delivered by sensors, the material budget must be limited to ambitious value of few per-mill of

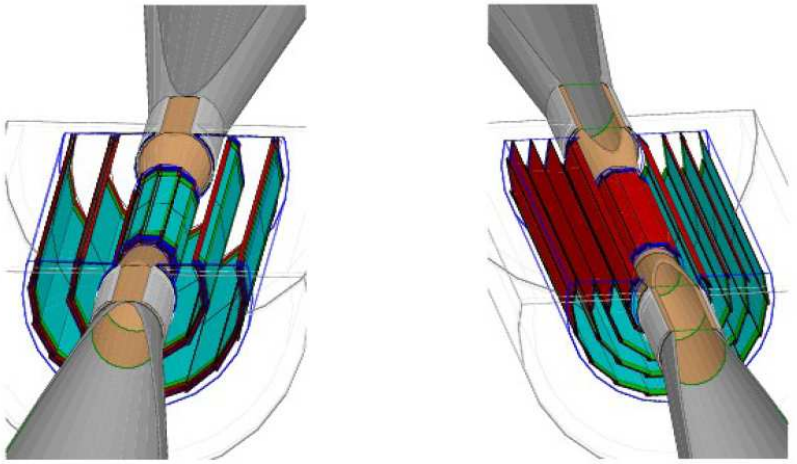


Figure 1.5: The two concepts of the ILD vertex detector developed for the ILC.

X_0. Table 1.3 summarizes the requirements of the sensors proposed to compose the layers of the ILD vertex detector.

Table 1.3: The requirements the ILC experiment regarding pixel sensors equipping the innermost layer of the vertex detector.

ILC requirements	
Non-ionizing radiation tolerance	$O(10^{11})n_{eq}/cm^2$
Ionizing radiation tolerance	$\leqslant O$ (100) krad
σ_{res}	2-3µm
Material budget per ladder	0.1-0.2%X_0
Time resolution	25µs

1.2 Beam telescopes

Most of the particles seen by the vertex detectors in high-energy physics experiments are MIP. It is mandatory to fully characterize the sensors with such particles and measure their properties such as ϵ_{det} or σ_{res}. Figure 1.6 shows a beam telescope, based on MAPS, which is used for that purpose. It allows reconstructing precisely particle trajectories. These trajectories are interpolated at the position of the device under test (DUT) giving the impact position of the impinging particles, to be compared with the DUT response.

1.2.1 TAPI: Télescope À Pixels de l'IPHC.

The R&D on pixel sensors, carried out by the IPHC, aiming for intrinsic σ_{res} in the range of a few microns, entailed the development of a beam telescope which allows for precise measurements of detector performance. Such a telescope was developed at the IPHC in 2006 [13, 14]. Its working name "$TAPI$" originates from French: "**T**élescope **À P**ixels de l'**I**PHC". The artist view of this telescope is sketched in Figure 1.6. This telescope was used to assess the performance of several CMOS sensors MIMOSA-24 and MIMOSA-25 prototypes described later in this thesis.

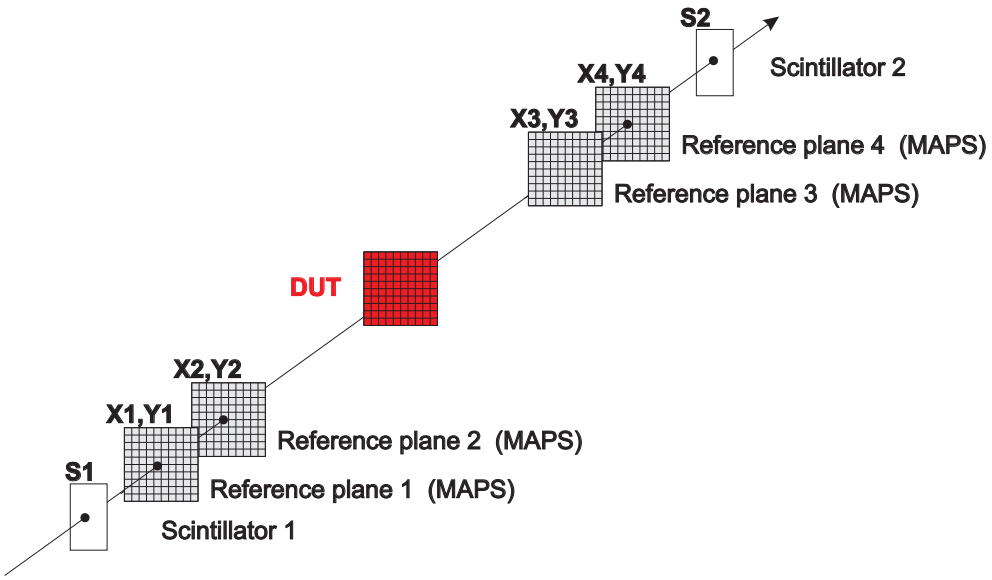


Figure 1.6: Artist view of the beam telescope developed at the IPHC-Strasbourg. The reference planes are based on high precision and low material budget Monolithic Active Pixel Sensors, allowing to achieve a σ_{res} of the telescope of 1µm . Beam telescopes are used during sensor characterization with high-energy particle beam. Measurements are based on the comparison of the particles tracks observed with the device under test and those observed with reference planes.

The reference planes are equipped with MIMOSA-18 sensors. They feature a 10-µm pitch size, 4 subarrays with 256×256 pixels each covering an active area of 5×5 mm^2, and they are read out within 4 ms. In order to reduce the multiple scattering effects, thus to improve the track resolution, the MIMOSA-18 sensors were thinned down to ∼50 µm.

The TAPI telescope incorporates a trigger system, based on the coincidence of two scintillation counters featuring the area smaller than the one of a DUT. The data acquisition is based on digitizer cards developed at the IPHC-Strasbourg. Each card features four input channels digitized with 12-bit, 50 MHz, analog to digital converter. In addition, a temperature stabilization system for the reference planes and DUT is implemented. This allows to operate the sensors over temperature range from -20 to +40 °C (±1 °C).

The performance of the TAPI telescope was assessed during a test beam campaign with high-energy (∼100 GeV) pion beam. An excellent efficiency of the telescope of above 99.9% and a track resolution at the DUT position of 0.95 ± 0.1 µm were observed [13, 14].

1.2.2 The EUDET telescope

Funded by the European Union, the EUDET[5] project [15, 16] aimed to provide an infrastructure to support the detector R&D for the ILC. Within the EUDET JRA1 (Joint Research Activity 1), a high-precision beam telescope has been developed. The CMOS sensors called MIMOSA-26 have been fabricated to equip the reference planes of the telescope. Its main characteristics are stated in Table 1.4.

Table 1.4: The main characteristics of the CMOS sensors with digital and sparsified output used for EUDET telescope.

Sensor:	**MIMOSA-26**
Process	AMS-OPTO
Number of pixels	663552
Pixel pitch	18.4 µm
Active area	21.2×10.6 mm^2
σ_{res}	⩽3.5 µm
Readout mode	column parallel
Output signal	digital and sparsified
Frame readout time	⩽100 µs

The EUDET telescope is sketched in Figure 1.7. It features a track resolution on the DUT surface of ∼1 µm, a readout of 10^4 frames per second, and it can be operated in a 1.2 T magnetic field.

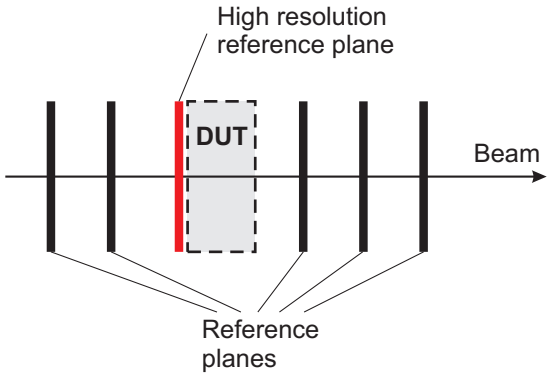


Figure 1.7: Plane configuration for the EUDET beam telescope. The high-resolution plane (red) is placed next to the DUT in order to attenuate multiple-scattering effects on the track reconstruction.

[5] http://www.eudet.org/e13/e21/e727/

1.3 Conclusions and summary

Several applications of silicon pixel sensors were presented and discussed in this chapter. They were selected because the CMOS pixel sensors, being the subject of this PhD thesis, were proposed to be used in these applications. Most of presented applications are calling simultaneously for sensors featuring a low material budget, a short readout time and an excellent spatial resolution. In addition, some of the experiments require sensors featuring an unprecedented radiation tolerance. The prominent example of such a sensor application is the CBM-MVD.

There is a certain trade-off between the required parameters and the sensor development. As it will be shown in Chapter 3, sensors used today (e.g. at LHC) provide a good radiation tolerance and a very short readout time. The same sensors do not offer the resolution and material budget which would satisfy the demands of experiments discussed above. Several sensor technologies, described in the same chapter, are pretended to meet the specifications of even the most demanding applications. Among those, the CMOS pixel sensors technology is the most mature with the strongest potential to provide, in the nearest future, devices with the required performance.

Even today, the CMOS pixel sensors provide a material budget of $0.05\%X_0$ and a spatial resolution of $\leqslant$3 µm, which meet well the requirements of all the applications discussed here. However, their tolerance to radiation and the readout time both require some improvement. This thesis contributed substantially to the R&D program addressed at IPHC-Strasbourg aiming at enhancing of the CMOS sensor performance. This contribution is presented in Chapter 5 and 6 of this thesis.

The three following chapters aim at presenting to the reader an overview of the currently existing sensor technologies used for charged particles detection and at giving complete background to understand processes discussed in the core of this thesis, in Chapters 5 and 6.

2 Particle interactions with matter and radiation damage

The silicon detectors used for vertexing in high-energy physics experiments are constantly exposed to a flux of numerous particles. The reactions occurring when the particles traverse the detector material are at the origin of the signal used to detect them.

Depending on the particle type and its energy, different interactions with the impinged material are observed. For example, charged particles interact with matter mainly through inelastic collisions and they are able to ionize atoms directly through interactions with their shell electrons. On the other hand, the probability of direct interaction with nuclei is small for this type of particles. At the contrary, neutrons do not ionize atoms directly, but instead they feature a high cross-section for interactions with nuclei.

Particles interacting with a sensor material generate also undesirable side effects, called later radiation damage. These side effects are at the origin of signal losses and noise increase, both leading to the degradation of sensor performance.

This chapter aims at describing the basic interactions of particles with matter. It also discusses the signal creation and radiation damage in silicon sensors.

2.1 Heavy charged particle interactions with matter

Two main features characterize the passage of charged particles through matter: the energy loss by the particles in inelastic collisions with the atomic electrons of the material, and the deflection of particles from their original direction due to an elastic scattering from nuclei.

In inelastic collisions, energy is transferred to the atom. If this energy is below the ionization threshold of the atomic electrons, only lattice excitations occur. Otherwise, the atom is ionized. In general, the amount of energy transferred to the material in each collision is small. Depending on the material density, the number of collisions per path unit can be very large and a substantial cumulative energy loss can be observed even in a thin material layer.

All mentioned processes are statistical in nature. Because of a large number of interactions per path length, the fluctuation of the total energy loss is small. The term dE/dx defines the average energy loss per unit of path length. This quantity was first calculated by Bohr and later corrected by Bethe and Bloch. The Bethe-Bloch formula [17, 18] is presented below:

$$-\frac{dE}{dx} = 2\pi N_a r_e^2 m_e c^2 \rho \frac{Z}{A}\frac{z^2}{\beta^2}\left[ln\left(\frac{2m_e\gamma^2 v^2 W_{max}}{I^2}\right) - 2\beta^2 - \delta - 2\frac{C}{Z}\right]\left[\frac{eV}{cm}\right] \tag{2.1}$$

r_e - electron radius = 2.817·10^{-13}cm	ρ - density of absorbing material
m_e - electron mass	z - charge of incident particle in unit of [e]
N_a - Avogadro's number = 6.022·$10^{23}/mol$	β - v/c of the incident particle
I - mean excitation potential	γ - $1/\sqrt{1-\beta^2}$
Z - atomic number of absorbing material	δ - density correction
A - atomic mass of absorbing material	C - shell correction
	W_{max} - maximum energy transfer in a single collision

W_{max} is the maximum kinetic energy which can be transferred to a free electron in a single collision:

$$W_{max} = \frac{2m_e c^2\beta^2\gamma^2}{1 + 2\frac{m_e}{M} + \left(\frac{m_e}{M}\right)^2} \tag{2.2}$$

where M is the mass of the incident particle.

It is worth highlighting the two correction factors C and δ. The first one is the shell correction, which intervenes when the velocity of the impinging particle is comparable or smaller than the orbital velocity of electrons. In such conditions, the electrons cannot be treated as stationary with respect to the impinging particle. The density correction δ accounts for the polarization effect, which is significant in condensed materials.

For practical purposes in high-energy physics, where $M \ggg m_e$, dE/dx in a given material is mostly a function of β and γ, and it does not depend on the mass of the traversing particle.

Figure 2.1 depicts the rate of energy loss as a function of the incident particle momentum for various particles and different mediums. The low-energy range is dominated by the $1/\beta^2$ and the energy loss is relatively high. When the particle velocity is about 96% of the speed of light, the energy loss is minimal. A particle depositing the minimum of energy is known as a Minimum Ionizing Particle (MIP: $\beta\gamma$ typically between 3 and 4). For particles with larger momentum, the relativistic rise of the average energy loss per unit path length is observed. Despite this rise, it is common to treat those particles as a MIP.

In parallel to inelastic collisions causing energy losses, charged particles passing through matter also undergo an elastic Coulomb scattering from nuclei, but with smaller probability. This scattering results in a deflection of the trajectories of the incident particles. As a consequence of numerous scattering, the particles follow a random zigzag path. The probability distribution of the total deflection of the outgoing particle with respect to the incident direction is a function of the particle mass and velocity, as described by the following equation:

$$\frac{d\sigma}{d\Omega} = \frac{q^2 Q 2F(\Theta)}{4p^2\beta^2 sin(\Theta/2)} \tag{2.3}$$

where q is the particle charge, p is the momentum, β is the velocity, Θ is the deflection angle, and

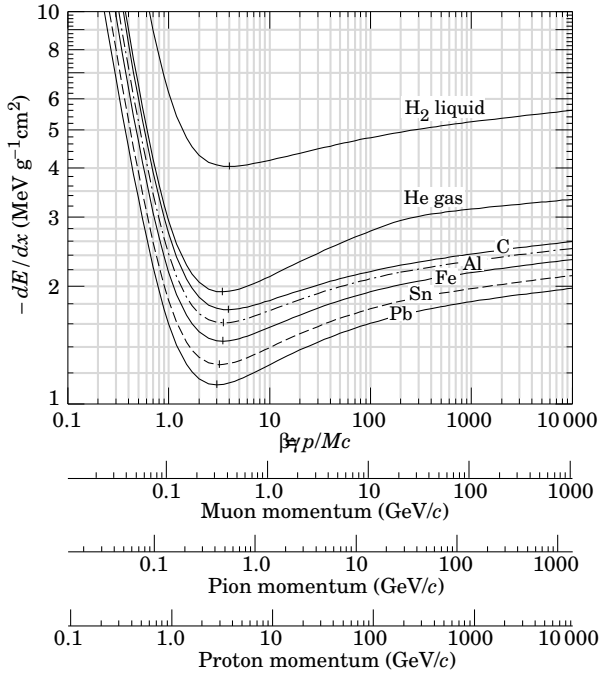


Figure 2.1:
Average energy loss per unit of path length as function of the particle momentum. The x-axis $\beta\gamma = p/Mc$ expresses the fact that the dE/dx does not depend on the mass of traversing particle but it is the function of β and γ.

Q is the nucleus charge. $F(\Theta)$ introduces an additional dependence originating from the spin of the scattered particle. The multiple scattering can be almost neglected for highly energetic and massive particles. In contrary, for electrons, featuring a much lower mass than the nuclei, the multiple scattering is more pronounced.

2.1.1 Energy-loss distribution for charged particles

The Bethe-Bloch formula refers to the mean energy loss per path unit. The actual probability distribution of the energy loss depends on the thickness of the impinged material.

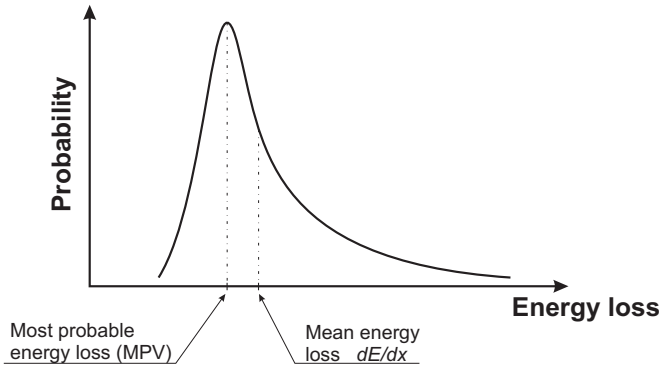


Figure 2.2:
Passage of particles through matter — energy-loss distribution in a thin absorber. In the case of thin absorbers (e.g., silicon detectors), one observes an asymmetric Landau distribution. Due to the high-energy tail of the distribution, the mean value of the distribution is displaced with respect to its most probable value.

For thick absorbers, the number of elementary collisions is large and the energy loss distribution features a Gaussian shape. This originates directly from the statistic Central Limit Theorem which states that the sum of N random variables, all following the same statistical

distribution, approaches the Gaussian distribution when $N \to \infty$.

In the case of thin absorbers, the number of collisions is too small to use the Central Limit Theorem. For silicon sensors (featuring typically a thickness of <500μm), the distribution of the energy loss was calculated by Landau, Symon and Vavilov [19, 20, 21]. Such calculations are difficult due to the possibility of a large energy transfer in a single collision. Such events are rare and they are responsible for the long tail at high energies in the energy loss probability distribution. Consequently, the distribution is asymmetric in shape (follows the Landau distribution), as illustrated in Figure 2.2. The mean energy loss from dE/dx does not correspond to the Most Probable Value (MPV) but is displaced due to the high-energy tail of the energy loss.

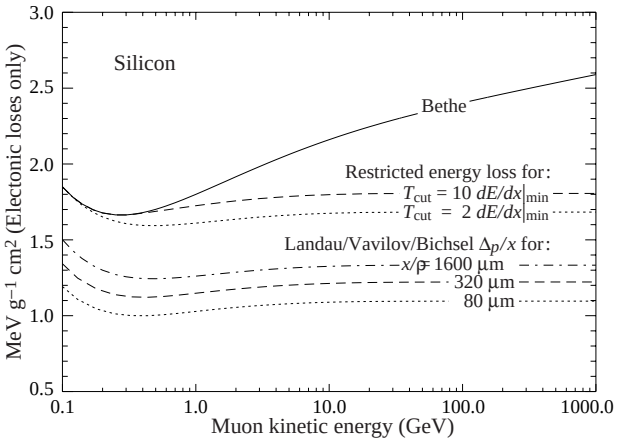


Figure 2.3:
Average energy loss in silicon per unit of path length as a function of the muon kinetic energy.

Figure 2.3 presents the most probable energy loss in silicon for muons calculated from the Bethe-Bloch formula (Equation 2.1) and the one calculated for thin silicon layers by Landau, Vavilov and Bichsel. The energy loss dependence on the particle momentum reaches a plateau for muon momenta above 1 GeV.

2.1.2 Energy loss of electrons and positrons

Since the impinging electrons/positrons feature the same mass as the orbital atomic electrons of the matter they penetrate, an additional energy loss mechanism starts to play a role. This is related to the emission of an electromagnetic-radiation arising from the scattering in the electric field of the nucleus (bremsstrahlung) [17]. Thus, the energy loss per unit of path length is the sum of the energy loss due to inelastic collisions and an electromagnetic radiation emission.

The energy loss due to inelastic collisions described by the Bethe-Bloch formula (Equation 2.1) has to be corrected for electrons and positrons. The first reason is that the impinging electrons have the same masses as the orbital atomic electrons. The second reason is that for electrons the inelastic collisions occur between identical particles. For these reasons, electrons

follows much more tortuous path through the material so they can lose a much larger fraction of energy in a single interaction than heavy charged particles do. More detailed discussion can be found in literature [17, 18].

2.2 Interactions of photons

Photons have neither rest mass nor electric charge. Their interactions with matter are dramatically different from these observed for charged particles. For example, because photons do not have a rest mass neither electric charge, they do not trivially[1] interact with matter through inelastic collision (characteristic for charged particles). Instead, photons interact with matter through the photoelectric effect, the Compton and Rayleigh scattering and the pair production.

The photoelectric effect, illustrated in Figure 2.4 (a), is a process where atomic electrons are emitted from matter as a consequence of absorption of incident photons. The whole energy carried by the absorbed photon is transferred to an atomic electron. Part of this energy is used to break the bindings with the atom and the rest contributes to the electron kinetic energy. The photoelectron appears with an energy given by the following equation:

$$E_e = hv - E_B \tag{2.4}$$

where hv is the photon energy and E_B represents the binding energy of the photoelectron.

The Compton effect is illustrated in Figure 2.4 (b). During the interaction between the incident photon and the atom, a part of the incident energy is spent on breaking the electron binding with the atom. Some of the energy is converted into kinetic energy of the electron and the rest to a photon, which is emitted in a different direction from the original one. The newly created photon possesses an energy expressed by:

$$hv' = \frac{hv}{1 + \frac{hv}{m_0c^2}(1 - cos\theta)} \tag{2.5}$$

where m_0c^2 is the rest-mass energy of the electron and θ is the scattering angle.

If the secondary photon still has enough energy, the process may be repeated. In this scenario, the electron is treated as free or as a loosely bound "free electron".

The Rayleigh scattering is related to photon interactions when no excess energy is transferred to the medium. The absorber atoms are neither excited nor ionized, but the photons are deflected.

In the pair production process, presented in Figure 2.4 (c), the energy of an impinging photon is spent on the creation of an electron-positron pair. This process can occur if the energy of the photon exceeds twice the rest mass of the electron (511 keV). Because of the conservation rules,

[1] Photons with high energy may materialize as a pair of charged fermions, e.g., μ-τ pair. Such events are seldom.

this process is only possible in the presence of an electromagnetic field, for example, the atomic one.

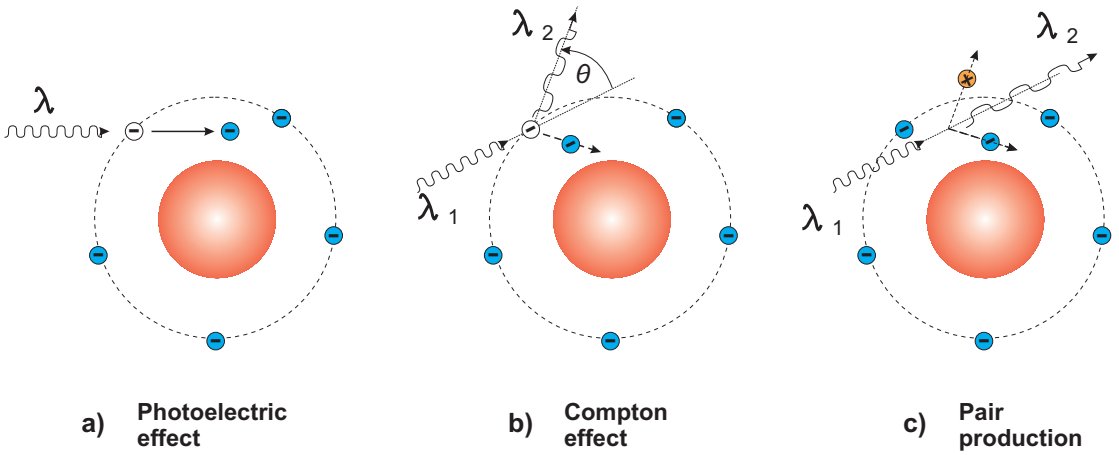


Figure 2.4: Interactions between photons and bound electrons. (a) Photoelectric effect: The photon is absorbed and its energy is used to ionize the electron. (b) Compton effect: The photon is elastically scattered. (c) Pair production: Energy of the photon is used to create an e+/e- pair.

In a given medium, the probability of the photoelectric effect, the Compton scattering and the pair production to occur depends on the incident photon energy. The photoelectric effect and pair production are processes which occur only when the energy of the incident photon exceeds a certain threshold value. Figure 2.5 illustrates the probability of photon interactions for 300 μm thick silicon as a function of the photon energy. The photons with relatively low energies, below 100 keV, interact mainly through the photoelectric effect. In the energy range from 100 keV up to about 10 MeV, the Compton scattering prevails. At energies above 10 MeV, the pair production is the dominant process involved.

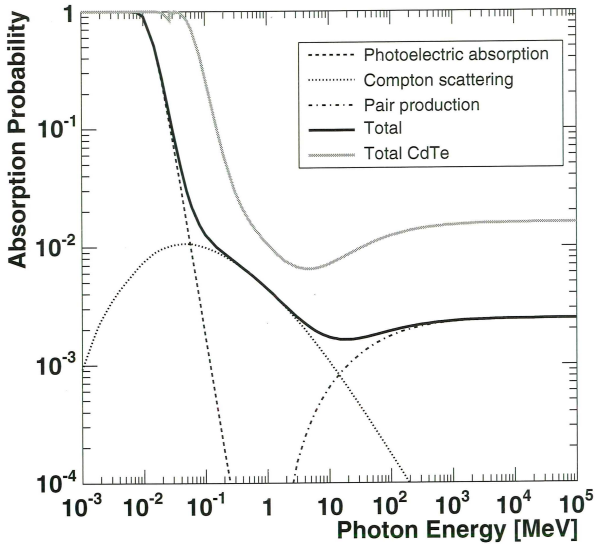


Figure 2.5: Probability for the interaction between a photon and a 300 μm thick silicon detector as function of the photon energy [22].

The photoelectric effect[2] is very important to understand the processes occurring in silicon detectors exposed to the photon radiation used for testing purposes. One of the frequently used sources for semiconductor detector characterization is an $^{55}\mathrm{Fe}$ source, emitting 5.9 keV and 6.49 keV photons. The photons emitted by an $^{55}\mathrm{Fe}$ source mainly interact with the electrons through the photoelectric effect. The ejected electrons have enough energy to ionize silicon atoms and create e-h pairs that are at the origin of a useful signal. A more detailed discussion related to the use of an $^{55}\mathrm{Fe}$ source for a sensor characterization is presented in Section 4.2.3.1.

2.3 Neutron interactions with matter

Since photons and neutrons do not carry any electric charge, they cannot interact with matter directly through the Coulomb force [23]. Neutrons undergo interactions with nuclei of an absorbing material. Depending on their energy, neutrons are either absorbed with a subsequent emission of radiation, or they are scattered by a nuclei.

For the low-energy neutrons (less than 100 keV), the reactions such as (n,α), (n,p) and (n,fission) prevail. An example of the (n,α) reaction is the interaction of a slow neutron with a boron nucleus, where a lithium nucleus with an energy of 0.84 MeV and an α particle with an energy of 1.47 MeV are created [24].

The elastic scattering from nuclei is the dominant process of energy loss for the neutrons in the MeV region [17]. In such a collision, a fraction of the kinetic energy of the neutron is transferred to the nucleus and the total kinetic energy is conserved. The impinging neutron is scattered and the nucleus is recoiled [25].

The neutrons featuring an energy above 1 MeV interact with matter by inelastic scattering. In this process, the recoil of nuclei is accompanied by gamma radiation.

2.4 Principles of particle detection with semiconductor detectors

A simplified cross-section of a silicon based charged particles sensor is illustrated in Figure 2.6. The top layer contains an insulating material (e.g., a silicon oxide SiO_2) and metal traces providing the connections between micro-circuitries, which are implemented near the $Si - SiO_2$ interface. The middle layer is the detector sensitive volume, while the bottom one is the detector bulk. An impinging particle crossing such a detector interacts with its matter according to the laws presented in the previous sections. Among all these effects, two are of great importance. The first one is the ionization, and the second one is related to the recoil of nuclei mostly due to the elastic scattering.

The electron-hole pair production due to ionization is beneficial in sensitive volume since it leads to the useful signal creation. The charge carriers are drifted towards the collecting implants (forming the reverse biased p-n junction with the detector sensitive volume), where

[2]The Auger effect, which competes with the photoelectric effect, is not considered here for the sake of simplicity.

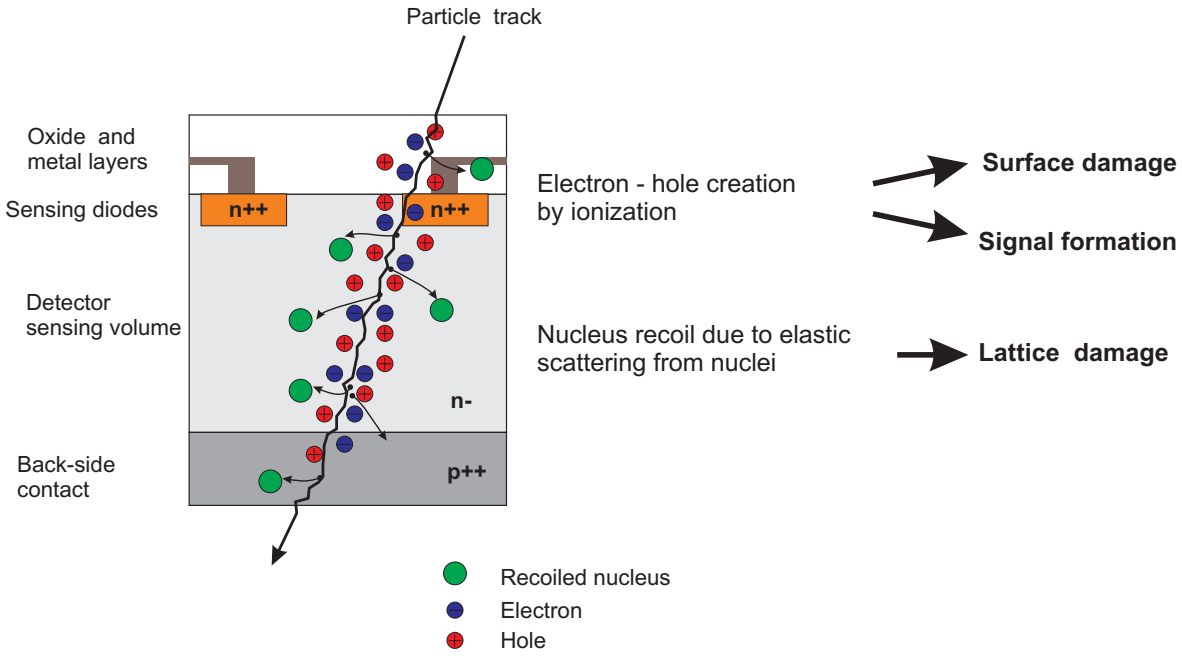


Figure 2.6: Consequences of particle interactions with a detector material. The figure depicts a simplified cross-sectional view of a silicon detector. Ionizing radiation passing through the oxide layers leads to a positive charge buildup, changing the electronic device parameters as a consequence. The same radiation interacting with sensitive volume leads to a signal creation. The non-ionizing radiation passing through the sensor displaces atoms from their positions in a lattice. This type of radiation is especially destructive for sensitive volume, where (by introducing traps) it leads to charge signal losses.

they are converted to a voltage, and then read out as a useful signal. On the other hand, the same process is responsible for undesirable effects occurring in the oxide layers and $Si - SiO_2$ interface. The recoil of nuclei from their positions in the silicon lattice leads to the damage in the detector material and, consequently, to signal losses. The presented effects and their consequences to the silicon detectors will be described in details in the following section.

2.4.1 Signal formation in silicon detectors

When ionizing particles traverse the detector medium, the electron-hole pairs are created along their tracks. The amount of those electron-hole pairs can be expressed as :

$$N_{e-h} = \frac{E_{absorbed}}{E_{ep}} \tag{2.6}$$

where $E_{absorbed}$ is the energy absorbed by the detector sensitive volume, E_{ep} stands for the energy required for the creation of an electron-hole pair. This energy is proportional to the material band gap and in the case of silicon amounts to 3.6 eV [26].

As presented in Section 2.1.1, the energy loss distribution for thin absorbers is asymmetric. This distribution was studied extensively by Hans Bichsel [27] as a function of a detector thickness, material type, impinging particle type and energy. These analytical calculations agreed with the experimental data over a very large range of particle energies, variety of particles and detector thicknesses (from 32 μm up to 3000 μm). Considering the MPV of the energy loss distribution calculated by Bichsel ($E_{absorbed}$) and the energy needed for the e-h pair creation, it can be concluded that for a thin detector (∼300 μm) approximately 80 e-h pairs are created by a MIP per each μm.

2.4.2 Radiation damage in silicon detectors

2.4.2.1 Ionizing damage

The ionizing damages in the silicon detectors are related to the accumulation of holes at the $Si - SiO_2$ interface. This phenomenon and its consequences are discussed in the following.

Figure 2.7(a) shows the electrons and holes generated by an impinging particle. The energy required to produce electron-hole pairs in silicon oxide layers amounts to about 17 eV [28]. The number of generated electron-hole pairs depends strongly on the particle type and energy, and also on the medium thickness.

Electrons and holes generated by an incident particle in the SiO_2 (insulator) layer undergo recombination. The fraction of holes escaping this recombination (fractional hole yield) is determined by the magnitude of the electric field applied through the oxide and by the initial density of electron-hole pairs produced. A stronger electric field separates the electrons from the holes more rapidly than a weak electric field, and the fractional hole yield is high. A higher electron-hole pairs density imposes consequently a higher probability of their recombination.

Because of a high mobility, the electrons which do not undergo recombination with holes are swept out of the oxide very rapidly. Instead, the holes which escape this recombination are transported through the oxide, see Figure 2.7(b). The transport of holes in the oxide is based on stochastic movements described in [29, 30]. This transport is activated by an electric field or a temperature increase, and features a very dispersive nature. The holes may travel through a typical gate oxide for several seconds at room temperature before reaching the $Si - SiO_2$ interface. In the case of lower temperatures, thousands of seconds may be needed.

When propagating from the generation point to the $Si - SiO_2$ interface, the holes may be trapped in oxide defects (E' centers) [31, 32, 33, 34] and retained for a long time. An E' center is a trivalent silicon defect associated with an oxygen vacancy in the oxide structure. In the case of MOS transistors with a positively biased gate, such trapping occurs in a thin region (5-20 nm) starting from the $Si - SiO_2$ interface toward the metal gate. The holes trapped in the oxide are relatively stable and undergo a long term annealing process. This annealing can extend from hours to years, depending on the temperature and the applied field.

Ionizing radiation is also responsible for the buildup of traps at the $Si - SiO_2$ interface. Those traps are called Pb centers [35, 36] and they are identified as defects composed of a trivalent silicon at the $Si - SiO_2$ interface with a dangling bond perpendicular to the interface. The mechanism through which the radiation creates these traps is not precisely known. There are several models which explain this phenomenon [32, 37, 38, 39, 40, 41, 42]. They will not be discussed here.

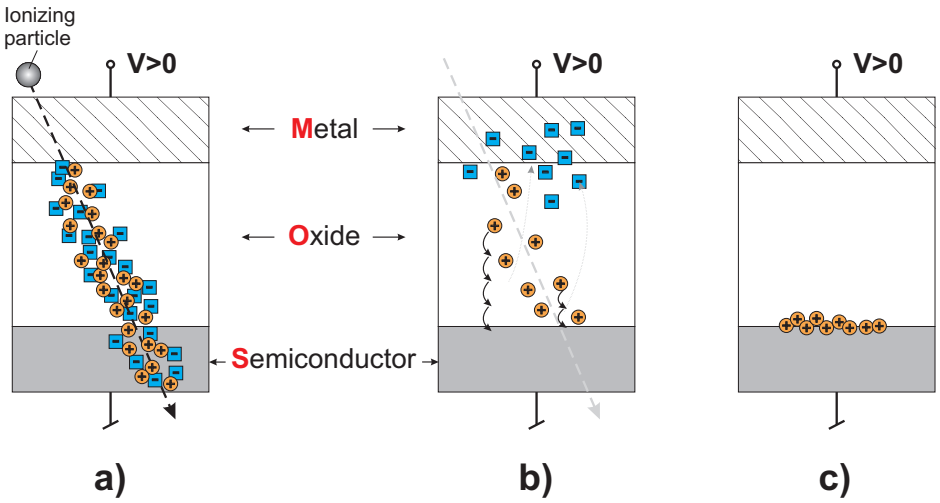


Figure 2.7: Creation of ionizing damage. (a) Electron-hole pairs are created in the $Si0_2$. (b) Electrons and holes drift in the oxide in the presence of an electric field. (c) Holes are trapped at the $Si - SiO_2$ interface.

The above described mechanism explains the ionizing-damage creation at the single particle level. When integrating the passage of many particles, cumulative effects appear.

The accumulation of a net positive charge in the oxide has negative consequences on the

electronic devices. In MOS devices, such charges are responsible for threshold voltage shifts and generation of leakage currents between transistor drain and source. Moreover, radiation-induced traps at the $Si - SiO_2$ interface are responsible for the increase in the low-frequency flicker noise (1/f noise). Sensing diodes suffer as well from the accumulation of ionizing doses. The increase in the leakage current is seen to be the major degradation when a CMOS sensor is operated in a radiation environment. A more detailed discussion related to ionizing radiation effects on this type of sensors will be presented in Chapter 4.

The standard unit for ionizing radiation doses is the Gray (Gy) [J/kg]. It represents the amount of radiation required to deposit 1 Joule of energy in 1 kilogram of any kind of matter. For the purpose of the work described in this document, the radiation dose is referred to the Si material. The "rad" (radioactivity absorbed dose) is the corresponding traditional unit, which is 0.01 J deposited per kg (1 Gy = 100 rad).

2.4.2.2 Non-ionizing damage

The non-ionizing damage is caused predominantly by interactions of particles with atomic nuclei (elastic scattering) and reflects the removal of atoms from their places in the crystal lattice. The probability of displacing a silicon atom from its location in the lattice depends strongly on the type and energy of the radiation.

In the case of silicon, an energy of about 25 eV is needed to remove an atom from the crystal lattice [43]. Electrons need to carry a minimal energy of about 260 keV in order to create such an atom recoil [44]. As neutrons and protons feature larger masses than electrons, they need a lower energy, about 190 eV, to remove an atom from its position. Photons with energy exceeding 260 keV may also contribute indirectly to a lattice damage [45]. In this case, the damage is produced by secondary Compton electrons with an energy exceeding 260 keV. The recoiled silicon atoms may also contribute to the lattice damage by removing further atoms which will create clusters of defects. The clusters are created predominantly by neutrons and protons, while for electrons point defects prevail.

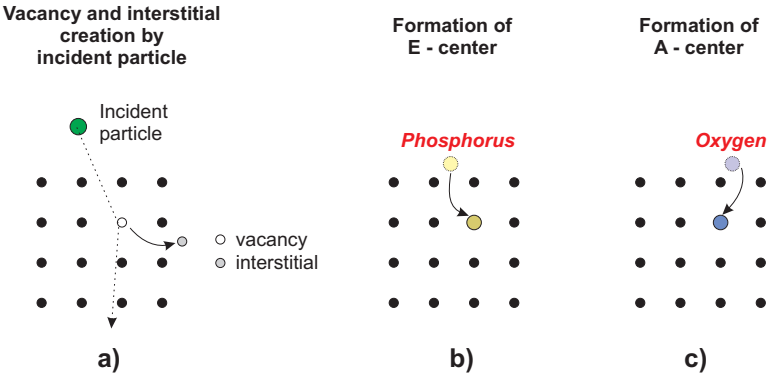


Figure 2.8: Creation of: (a) A vacancy and an interstitial; (b) The E-center corresponding to the phosphorus-vacancy pair; (c) The A-center formed by the oxide-vacancy pair.

The consequence of the atom displacement is the creation of a so-called Frankel pair. The latter is composed of a vacancy and an interstitial. This mechanism is depicted in Figure 2.8.

The vacancy corresponds to an empty space left by the recoiled atom in the lattice while the interstitial corresponds to the presence of a recoiled atom in an interstitial position. Point defects tend to migrate through the silicon lattice even at room temperature. They can eventually recombine, decreasing the effective number of defects (annealing). During such a movement, the primary defects may combine with silicon impurities like oxygen, boron or phosphorus, and form stable defects. For example, phosphorus is added in order to create n-type silicon. When a vacancy recombines with phosphorus, a new complex called E-center is created (see Figure 2.8(b)). In parallel, the phosphorus ion does not fulfill its original role of donor anymore. This process is called donor removal. Oxygen can be introduced in the silicon wafer during the crystal growing stage to limit the donor removal phenomenon. The combination of vacancy and oxygen, which competes with the recombination of vacancy with phosphorus, leads to the creation of a so-called A-center.

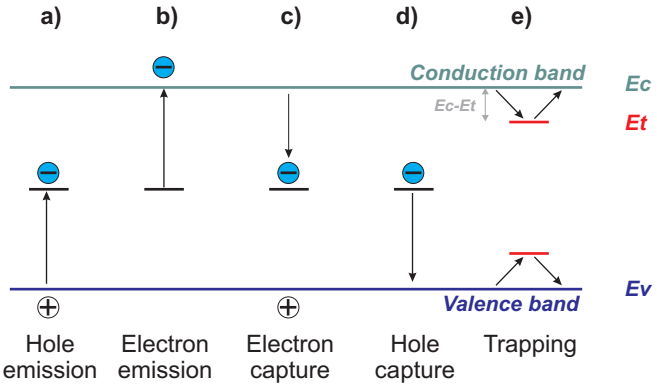


Figure 2.9: Emission and capture processes through intermediate states induced by non-ionizing radiation. The emission of holes (a) and electrons (b) in the detector sensitive volume leads to the creation of additional charge carriers (leakage current). Electrons or holes may also be captured (c) and (d), resulting in a decrease in the current in the conduction band. Stable defects also act as trapping centers able to capture electrons or holes and re-emit them with some delay (e).

The stable defects are electrically active and form intermediate states between the valence and conduction bands. This means that they are able to capture or emit electrons or holes. Figure 2.9 illustrates the emission and capture processes through intermediate states. The emission of electrons (Figure 2.9 a) and holes (Figure 2.9 b) in the detector sensitive volume leads to the creation of additional charge carriers (leakage current). Electrons or holes may also be captured (Figure 2.9 c and d), resulting in a decrease in the current flow in the conduction band. Stable defects also act as trapping centers able to capture electrons or holes and re-emit them with some delay, as illustrated in Figure 2.9 e).

According to the Shockley-Read-Hall theory [46, 47], the rate of change in the trap occupancy is given by the following equation:

$$\frac{dn_t}{dt} = \frac{N_t - n_t}{\tau_c} - \frac{n_t}{\tau_e} \tag{2.7}$$

where N_t stands for the total trap density, n_t for the density of trapped electrons, τ_c and τ_e are the time constants for electron capture and emission respectively. Both time constants can be calculated using the Shockley-Read-Hall theory, which considers a defect at an energy E_t

below the bottom of the conduction band, E_c, and gives:

$$\tau_c = \frac{1}{\sigma_e v_{th} n_s} \tag{2.8}$$

$$\tau_e = \frac{1}{\sigma_e \chi_e v_{th} N_c} \exp\left(\frac{E_c - E_t}{k_B T}\right) \tag{2.9}$$

where: σ_e is the electron capture cross-section, χ_e stands for the entropy change factor by electron emission, v_{th} refers to the electron thermal velocity, N_c corresponds to the density of states in the conduction band, k_B is the Boltzmann constant, T is the absolute temperature and n_s is the corresponding density of signal electrons.

The presence of the radiation-induced trapping centers has a strong impact on the transfer of the signal-charge carriers inside the detector volume. Due to a very short capture time constant, usually in the nano-seconds range, the signal charges are trapped quickly by the lattice defects. Instead, the emission time constant can vary from nano-seconds at high temperatures, to minutes or hours for low temperatures.

Traps also act as generation centers, creating electron flow from the valence to the conduction band. This flow occurs when electrons are firstly moved from the valence band to intermediate energy levels inside the forbidden band, and then move from the trap energy levels to the conduction band. This effect increases the leakage current and it is strongly visible at high temperatures because of the electron thermal excitation. At cryogenic temperatures, the emission time constant is so long that the traps, once filled, become inactive. The leakage current is also suppressed. In the intermediate temperature range, the charge carriers are released faster but too late to contribute to the useful signal. In this temperature regime, a signal decrease and high leakage current are frequently observed in sensors exposed to non-ionizing radiation.

NIEL scaling

For the purpose of a normalization of radiation damage, the NIEL (Non-Ionizing Energy Loss) scaling hypothesis was introduced. According to the NIEL scaling, any particle fluence can be reduced to an equivalent 1 MeV neutron fluence producing the same bulk damage in a specific semiconductor. The scaling is based on the hypothesis that the generation of bulk damage is due to non-ionizing energy transfers to the lattice. The displacement damage is described by the function D(E), which depends on a particle type and energy. The displacement damage for 1 MeV neutrons is set according to the ASTM[3] standard as a normalizing value: D(1 MeV neutron)= $95MeV \cdot mb$. On the basis of the NIEL scaling, the damage caused by any particle with an energy E can then be described as D(E)/D(1 MeV neutron). Figure 2.10 shows D(E) for different particles. The D(E) values are originating from different measurements

[3]ASTM - American Society of Testing Materials (www.astm.org).

performed on irradiated n-type silicon detectors. For some energy ranges, only numerical calculations are available. The complete discussion related to the data used for the creation of Figure 2.10 can be found in [48, 49].

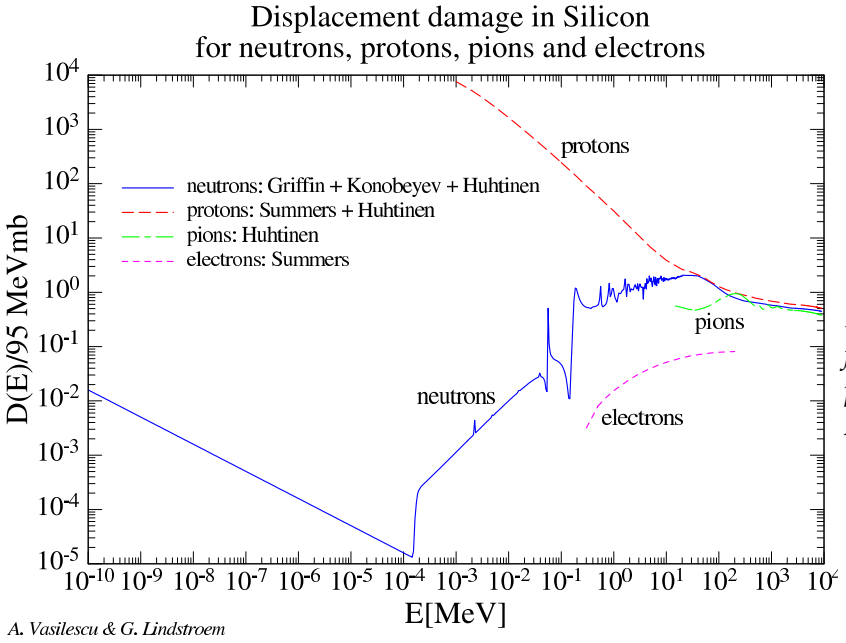


Figure 2.10: Displacement damage as a function of energy of different particles plotted relatively to 1 MeV neutrons [50].

The NIEL hypothesis has some limitations. For example, the NIEL scaling does not apply in the case of detectors based on Oxygenated silicon (DOFZ), tested in the framework of the ROSE collaboration. For those sensors, the observed changes in the effective doping due to the donor removal process were less pronounced in samples irradiated with protons and pions (both scaled with NIEL to 1 MeV neutrons) than for the ones exposed to neutrons. This effect is known as the "p-n-puzzle" and has its origin in different primary interactions with a sensor material. A detailed explanation of this phenomenon can be found in the relevant literature, for example in [51]. In the range of up to 1 MeV, neutrons interact with silicon predominantly by an elastic scattering, thus, the recoiled silicon atoms feature relatively high energies. As a consequence, clusters of defects are produced. Instead, protons interact predominantly by Coulomb scattering resulting in low-energy recoils producing point like defects. Finally, due to the cluster formation, larger number of defects disturbing the signal collection was produced in neutron irradiated samples.

This document covers the radiation tolerance studies related to CMOS pixel sensors. Those devices are based on p-type silicon. One may wonder if the NIEL scaling hypothesis can be applied for p-type silicon. The density of intrinsic silicon amounts to $5{\cdot}10^{22}$atoms/cm^3. For p-type doping, Boron atoms with a density in the range of 10^{13}-10^{14}atoms/cm^3 for the EPI layer and 10^{19}atoms/cm^3 for the substrate is used. This is from 3 up to 9 orders of magnitude lower than for intrinsic silicon. Therefore, in a first approximation, interactions of neutrons

with impurity atoms are rare. Moreover, regarding lattice defect production in both p-type and n-type silicon, the double vacancy defects prevails [52]. As the NIEL scaling hypothesis is based on non-ionizing energy loss during interactions with silicon atoms, it should also be valid for any type of silicon.

It could be expected that depending on the nature of the interactions, one may observe violations of the NIEL scaling also for p-type sensors. An illustrative example of such violation will be discussed in Section 4.2.5.2.

2.5 Conclusions and summary

This section presented the basic aspects of interactions of particles with matter. Among all the possible interactions, two effects are of great importance: ionization and displacement of atoms.

The ionization leads to the signal creation in the detector sensitive volume and simultaneously creates undesirable effects in the oxide layers. The defects introduced by radiation at the $Si - SiO_2$ interface are at the origin of the electronic noise and leakage current increase. The buildup positive charge affects a performance (e.g. the threshold voltage) of MOS transistors.

The displacement of atoms from their lattice results in the production of active states in the silicon material. These states introduced in the detector sensitive volume disturb the signal collection. They are also the source of the leakage current and noise increase. Consequently, due to an insufficient signal and high noise, the sensors are losing their performance.

Many factors impact the sensor tolerance to radiation: the material used for charged particle detection, the presence of an electric field in sensitive volume, and last but not least the technology used for the sensor manufacturing. Several different sensor technologies are discussed in the next chapter to present the accomplished and the ongoing R&D on the charge sensitive devices.

3 Position sensitive particle detectors

The R&D on the silicon-based charged particle sensors is ongoing to meet the requirements of future applications. Some of these devices, like the strip sensors or the Hybrid Active Pixel Sensors (HAPS), are being used at the Large Hadron Collider (LHC) experiments [11]. Some others are developed to fulfill the requirements of the upcoming upgrade of the LHC: the super LHC (sLHC). These developments are mostly focused on improving the sensor tolerance to radiation. The sensors dedicated for the LHC and its upgrade feature a good tolerance to radiation and fast readout, but they are thick, and their spatial resolution is insufficient to meet the requirements of future experiments like the CBM, ILC or the STAR experiment upgrade. These experiments call for sensors which are fast, granular, tolerant to radiation, and featuring a very low material budget. To fulfill these conditions, several sensor technologies are under development: the CCDs (Charge-Coupled Devices), ISIS (In-Situ storage Image Sensor), DEPleted Field Effect Transistor (DEPFET), SOI (Silicon On Insulator), and CMOS pixel sensors.

The following chapter aims at presenting the main features of all aforementioned sensor technologies, except of the CMOS devices, which are discussed separately in Chapter 4.

3.1 Strip detectors

The simplest position sensitive devices are those based on segmented diodes. The strip sensors are a good example. They have been widely used for tracking in many high-energy physics experiments in the past twenty years. The simplest strip sensors are based on a $\sim$300-μm thick, depleted n-type silicon substrate, where p-type-silicon strips are implemented. The readout circuits are located aside the sensitive area. The strip sensors provide a one-dimensional (1D) position information. To achieve a two-dimensional (2D) information, two strip sensors rotated by some angle with respect to each other may be used.

A more sophisticated 2D sensor, with strips on both sides, is shown in Figure 3.1. In this example, the n+ -silicon strips are tilted by 90 degrees with respect to the p+ -type strips. Such sensors provide 2D position information, but they are more complicated to handle than single sided sensors [53].

Due to a relatively thick sensitive volume, typically $\sim$300 μm , the strip sensors feature a large signal, in excess of 20.000 e^- for a MIP. Such a signal magnitude is needed due to the high noise of these devices, which is dominated by the strip capacitance (typically in the range of 1 pF/cm). The latter translates into the electronic noise of about 1000-2000 e^-, depending on

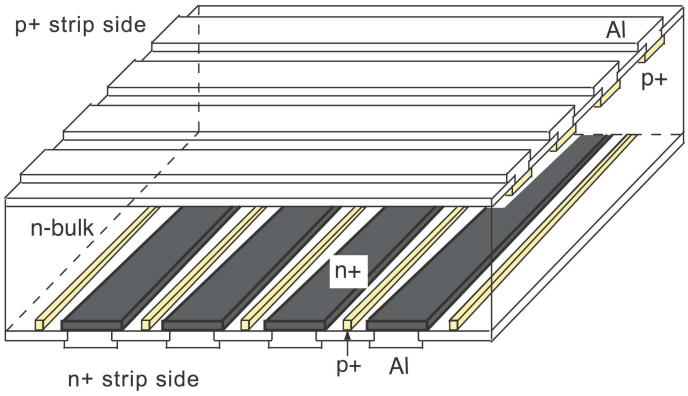


Figure 3.1:
Concept of a double-sided strip sensor [54]. The p-type strips are implemented on one side, while on the other side n+ type strips oriented orthogonally are used. Such sensors provide 2D position information; however, they are more complicated to handle than single sided strip sensors.

the detector dimensions.

The strip sensors need not more than 10 ns for charge collection. Their readout time depends predominantly on the Front-end Electronics (FE). For example, the readout time of strip sensors installed at the LHC experiments is of ∼25 ns.

Concerning the radiation hardness, the strip sensors developed for the LHC experiments withstand non-ionizing radiation fluences as large as $2{\cdot}10^{14}\ \mathrm{n_{eq}/cm^2}$ [55, 56, 57]. This high tolerance was achieved by selecting carefully the sensor parameters, for example, by implementing them on the fully-depleted substrate (For more detailed discussion see the reference [58].). Moreover, to suppress a significant rise in the radiation-induced bulk leakage current, the strip sensors require moderate cooling.

By the mean of dedicated readout electronics, the strip sensors feature also a satisfactory ionizing radiation tolerance. For example, the ATLAS strip detector readout electronics provides satisfactory performance even after irradiation up to 60 Mrad [55].

The σ_{res} of strip sensors depends on the strip to strip pitch. A resolution as low as 10 μm can be achieved with a pitch of 80 μm [59].

The strip sensors feature also several weaknesses. The relatively thick sensitive volume of these sensors leads to a substantial material budget of about $0.3\%X_0$. Furthermore, when several particles cross the sensors simultaneously, ambiguities in the association of the two coordinates to reconstruct 2D hits (see Figure 3.2) arise. They are limiting the applications of the strip sensors to low-particle-rate regions.

The strip sensors feature low production costs and a reduced number of channels (with benefits for the power consumption and data acquisition) with respect to the pixel sensors. For these reasons, they were frequently used for the external layers of tracking detectors. Strip sensors will also be installed at the Silicon Tracking System (STS) of the CBM experiment.

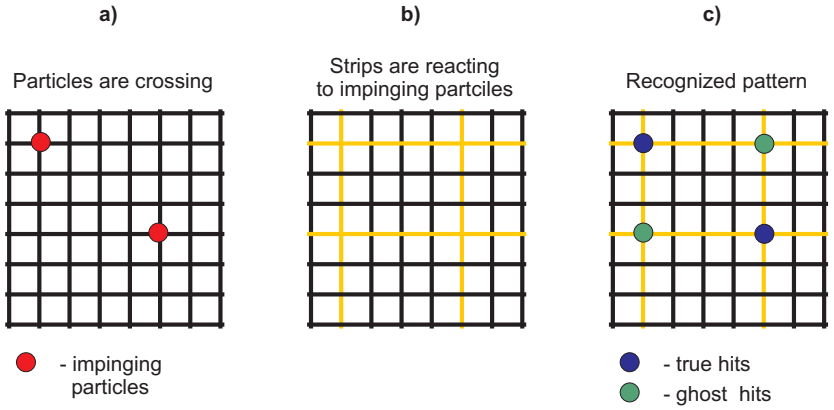


Figure 3.2: Pattern ambiguities in 2D strip sensors. (a) This figure depicts the case when two charged particles (shown in red) are crossing the strip sensor. (b) In this example, the signal left by the particles is observed for four strips. (c) During the analysis, it cannot be distinguish whether the particles were originally crossing places marked with blue points (row 2 column 2 and row 5 column 6) or those marked with yellow ones.

3.2 Hybrid Active Pixel Sensors

3.2.1 The classical approach

The classical approach for the Hybrid Active Pixel Sensors (HAPS) presented here is based on the sensors used for the vertex detector of the ATLAS experiment [60] at the LHC.

Figure 3.3 shows an ATLAS pixel module which is composed of three main parts connected together. The first one is the sensitive volume producing analog signals (”sensor”). This part is connected using a bump-bonding technique [61] to the front-end electronics circuitry (”FEs”) that performs the signal processing. The third part contains the Module Controller Chip (”MCC”) that ensures the communication with the outside world (e.g., data transmission via optical links or setting of the sensor parameters).

The sensitive volume of the ATLAS HAPS is based on oxygenated and fully depleted silicon. The choice of this material was motivated by its high non-ionizing radiation tolerance [62]. The sensor active area is 16.4×60.8 mm^2 in size and it hosts 47232 pixels. Each pixel has a size of 50×400 µm^2 and features a fast charge preamplifier with current feedback.

The front-end electronics was fabricated in the IBM 0.25-µm process. The small feature size allows implementing numerous functionalities, like for instance a preliminary selection of useful data. The information about the pixels containing a useful signal is transferred to the module controller (MCC). The latter ensures, among others, the event building. The data from the MCC are transferred to optical transmitters and sent to the outside world. The readout time provided by the FE electronics of the ATLAS modules allows to sample the pixel outputs every 25 ns[1].

[1]This is not a hard limit for the readout electronics. The readout time was adjusted to the time space between two consecutive beam spills.

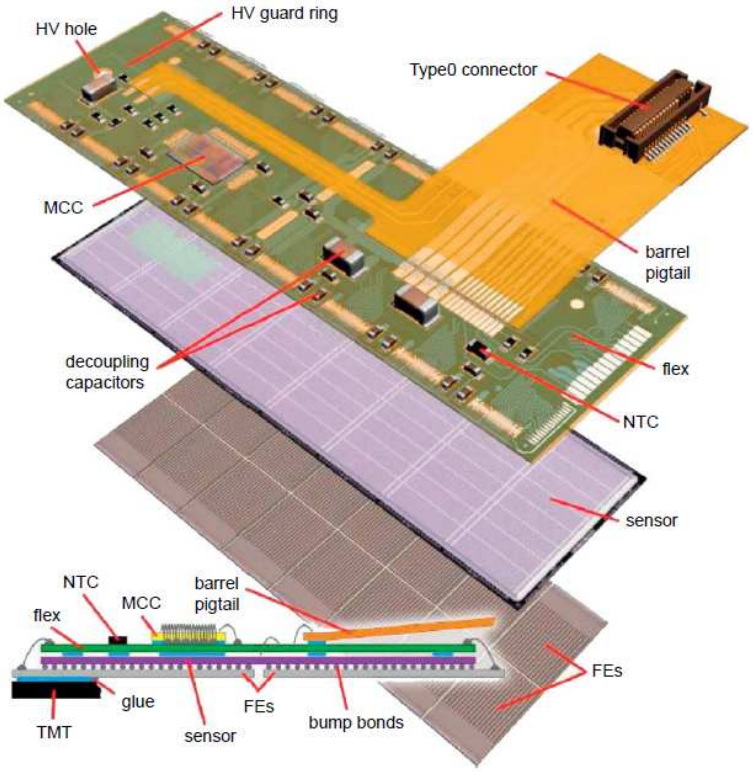


Figure 3.3:
Hybrid pixel sensor. This figure shows the HAPS equipping the ATLAS experiment. The ATLAS pixel module is composed of 3 layers containing: front end electronics (bottom), sensitive volume (middle), control unit and data transfer unit (top). The whole module features a material budget of $1.5\%\ X_0$. *Figure taken from [60].*

The performance of the ATLAS modules was reported in numerous publications, for example, in [63, 64, 65]. The ATLAS sensors were irradiated with a 24 GeV proton beam up to fluences of about $2{\cdot}10^{15} p/cm^2$. This corresponds roughly to $1.1{\cdot}10^{15}\ \mathrm{n_{eq}/cm^2}$ and to 50 Mrad. Since the ATLAS modules feature 300-µm thick sensitive volume, their σ_{res} is influenced by several parameters: strength of a magnetic field, incident angle of impinging particles, and radiation level. The σ_{res} measured for the ATLAS modules before irradiation in the shortest pixel dimension (50µm) varies from 6 to 10 (± 0.6) µm.

The ϵ_{det} was observed to be above 99.9% before sensor irradiation. It dropped down to $97.8 \pm 0.7\%$ for proton irradiated samples ($2{\cdot}10^{15} p/cm^2$). Despite the accumulation of such a substantial radiation, the ATLAS pixel modules were still able to meet the requirements of the experiment.

For these sensors, their very short readout time and robustness to radiation environment are not accompanied by a low material budget. The latter is reflecting a relatively large thickness of the full module, composed of two bump-bonded slices of silicon and a small PCB[2] on the top. This translates into a material budget of about $1.5\%\ X_0$. As a consequence, the HAPS could not be used for high-energy physics experiments where a low material budget is of the highest priority.

The potential increase in the LHC nominal luminosity by one order of magnitude (sLHC

[2]PCB stands for Printed Circuit Board.

project $L = 10^{35}/cm^2s$) will increase also the fluence of non-ionizing radiation to which the HAPS will be exposed to about $1{\cdot}10^{16}$ $\mathrm{n_{eq}/cm^2}$. To withstand such a fluence, two R&D programs on HAPS are investigating different approaches. The first one is using silicon-based sensors featuring a transversal charge collection. The second one utilizes sensors based on diamond material. Sensor prototypes fabricated using these techniques will be discussed in the next sections.

3.2.2 Hybrid sensors with transversal charge collection ("3D sensors")

The traps introduced by non-ionizing radiation (see Chapter 2) reduce the mean free path of the charges generated by the impinging particles. For example, after $1{\cdot}10^{15}$ $\mathrm{n_{eq}/cm^2}$ the mean free path for electrons amounts to approximately 150 μm [66]. This is shorter than the standard sensitive-volume thickness, typically in the range of 300-500 μm. The charges generated far from the collecting diodes cannot reach them and, consequently, they cannot contribute to the signal. This reduces the Signal over Noise Ratio (SNR) and hence degrades the sensor performance. To cope with this effect, sensors featuring column-shaped electrodes penetrating the sensitive volume perpendicularly to the surface were introduced ("3D-sensors") [67]. Since the distance between electrodes is very short (typically ∼70 μm), all the signal charge is available even after the detector has been irradiated with $\geqslant 10^{15}$ $\mathrm{n_{eq}/cm^2}$. Figure 3.4 illustrates the difference between the charge collection in the planar/standard (left) and 3D-sensor (right).

Due to the reduced distance between electrodes, only a few tens of volts are sufficient to fully deplete the sensitive volume, compared to hundreds of volts for the planar sensors. This is another prominent advantage of the 3D-sensors.

The sensitive volume of the 3D-sensors is organized in pixels, as illustrated in Figure 3.5. The pixels and the bias electrodes are etched in the 300 μm silicon bulk [68, 69], and filled later with poly-silicon. The poly-silicon is additionally doped with n-type or p-type material. The electrodes are arranged in 50×400 μm^{2}pixels (3 collecting electrodes are connected together). In the example shown here, the distance between two n-type electrodes belonging to a single pixel is 130 μm, while the distance from p-type to n-type collecting electrodes amounts to 50 μm. A proper biasing of the p-type and n-type electrodes ensures the sensitive-volume depletion and a signal transfer towards the n-type columns. Such sensitive volume is next bump bonded to the front-end electronics used previously with the standard ATLAS modules (see Section 3.2.1).

The first beam tests[3] performed to assess the performance of the 3D-sensors [70, 68, 69, 71, 72] indicated: a σ_{res} comparable to the planar devices (6 to 10 μm in the shortest pixel dimension); a ϵ_{det} of $99.9 \pm 0.1\%$ for 15 ° inclined tracks and $95.9 \pm 0.1\%$ for perpendicularly-incident tracks (due to dead areas corresponding to the regions occupied by the n/p-type electrodes). The low ϵ_{det} for the perpendicularly incident tracks may become a weak point of the 3D-sensors (depends on the application).

[3]The sensor parameters were measured at the temperature of -20 °C which corresponds to the temperature range expected at the experiment (⩽ -20 °C).

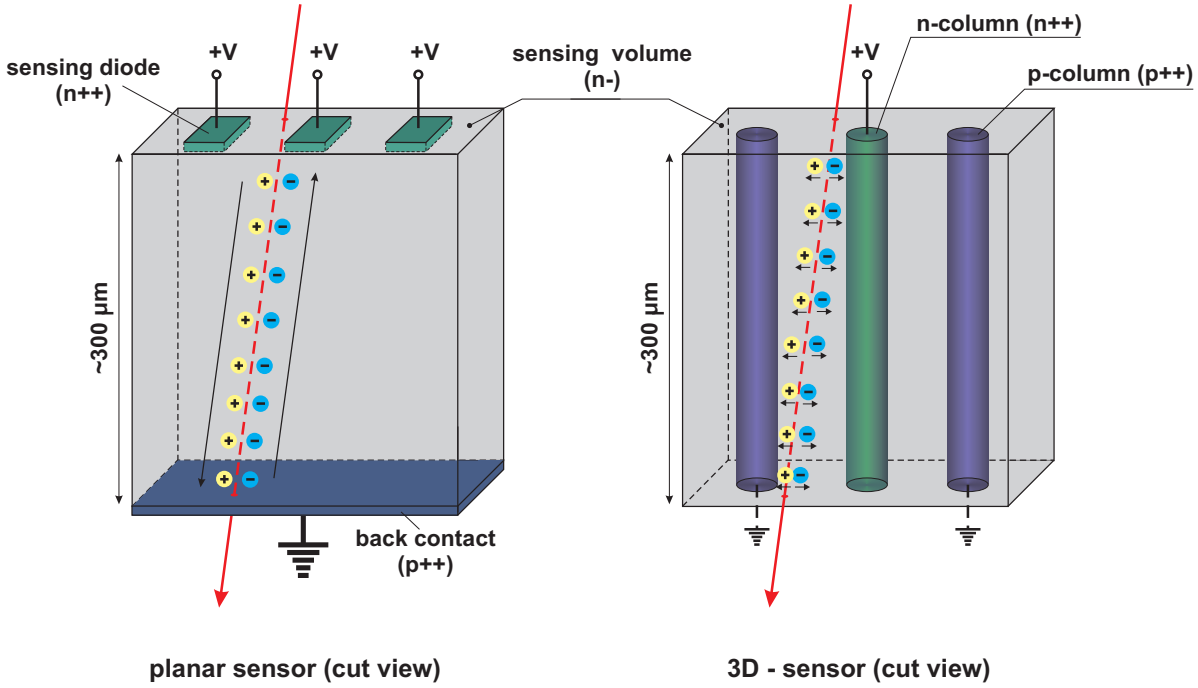


Figure 3.4: Charge collection in the planar and 3D sensors. In the planar sensor (left), the charge generated in the sensitive volume is transported towards the sensing diodes. After exposure to a substantial fluence of non-ionizing radiation, the mean free path for electrons amounts to about 150 µm , which is shorter than the thickness of conventional active volumes (300-500 µm). Charge carriers generated far from the sensing diodes cannot reach them and thus cannot contribute to the signal. This results in a reduction of the SNR and hence in the degradation of the detector performance. The "3D-sensors" (right) feature column-shaped electrodes penetrating the sensitive volume perpendicularly to the surface. The distance between electrodes is typically ∼70 µm. Since the distance between the charge collecting implants is shorter than the mean free path for electrons in irradiated silicon, the charge is not lost even after substantial detector irradiation.

The non-ionizing radiation tolerance was assessed with the 3D-sensors irradiated up to $\sim 1 \cdot 10^{16}$ $\mathrm{n_{eq}/cm^2}$. Despite the significant decrease in the charge collection, the signal was still double than the one observed for the planar sensors [68] irradiated up to the same fluences. The amount of charge collected by a single pixel of the 3D-sensor allowed achieving a SNR of 38 after sensor irradiation up to $8.8 \cdot 10^{15}$ $\mathrm{n_{eq}/cm^2}$ [69].

The 3D-sensors introduce an excellent idea for improving the non-ionizing radiation tolerance. So far, they are still in the development phase in order to fulfill the sLHC requirements regarding the radiation hardness. For this application, the constraints on the material budget are less severe than for the CBM and ILC experiments. The currently existing 3D-sensors are based on approximately 300 µm-thick sensing volume[4] which makes them not attractive for experiments that are particularly demanding in terms of material budget. In

[4]The bump-bonded readout electronics and data-transmitters should be accounted for a total material budget.

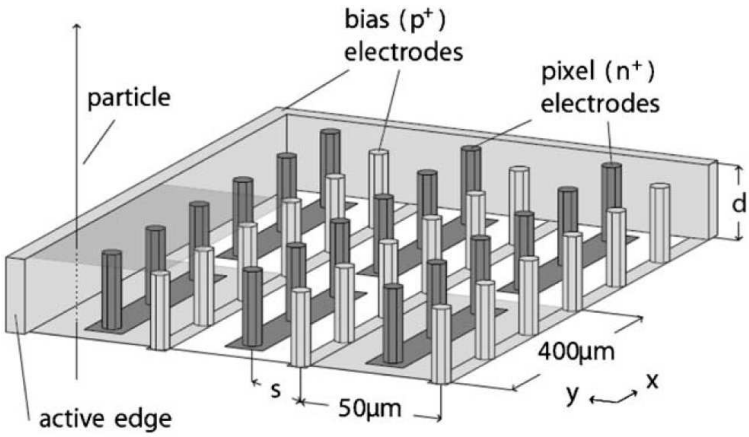


Figure 3.5:
This figure illustrates the organization of the sensitive volume of the 3D-sensors (figure taken from [53]). The electrodes are arranged in 50×400 µm² pixels (3 collecting electrodes are connected together). The distance between two n-type electrodes belonging to a single pixel is 130 µm, while the distance from p-type to n-type collecting electrodes amounts to 50 µm. The idea of the lateral charge collection is considered as a possible option for the ATLAS experiment sensor upgrade for the sLHC.

addition, industry still has difficulties in making an homogeneous "large" scale production of this type of sensors.

3.2.3 Diamond-based hybrid sensors

Since many years, diamond has been the object of several R&D programs aiming to improve the tolerance of sensors to radiation. In fact, except the most natural blue diamond, which behaves as a semiconductor due to substitutional boron impurities replacing the carbon atoms, diamond is a good electrical insulator. An n-type diamond can be obtained by phosphorus doping during a Chemical Vapor Deposition (so-called CVD Diamond) and can be used for particle detection.

The bandgap of 5.5 eV of the CVD diamond leads to a higher energy (13.1 eV) for the electron-hole pair creation with respect to 3.6 eV required for silicon [70]. This is beneficial since the thermal noise creation is significantly suppressed, but it is a disadvantage in terms of signal generation. The higher band gap translates into a smaller bulk leakage current, but also into smaller signals (32 e-h pairs/µm for diamond with respect to about 80 e-h pairs/µm for silicon) generated by impinging particles. The radiation length of diamond (12.2 cm) is larger than the one of silicon (9.4 cm). However, due to the very small leakage current, thus very small shot-noise contribution, the SNR per $0.1\%\ X_0$ of diamond-based sensors is in the same order as of silicon-based devices [70].

Diamond has also potential to provide particle sensors that are more tolerant to radiation than those based on silicon. The radiation hardness of diamond and silicon materials was extensively studied in [73]. Authors claim the two following facts that cause the diamond to be more tolerant to non-ionizing radiation than silicon:

- The averaged energy to create a lattice displacement is larger for diamond (37-47 eV) than for silicon (15-20 eV).

- Most of the damage induced in the sensor material during interactions with particles are not caused by the primary particles, but by the recoil and nuclear fragments from the first atom hit (e.g., primary knock-on atom). Low energy particles are created by the nuclear fragments from inelastic collisions or the nuclear recoils from either elastic or inelastic scattering. For silicon with an atomic number of 28 many nuclear recoils can be created, which cause a large amount of NIEL (see Section 2.4.2.2). In the case of diamond, most of the secondary particles are the light He nuclei, which cause a relatively small amount of NIEL. This is the basic reason why diamond is an order of magnitude more radiation hard at high energies.

The small relative dielectric constant for diamond (ϵ_r=5.3, to be compared with 11.9 for silicon) results in a smaller input capacitance for the amplifier. This reduces the contribution of both the 1/f and the thermal noise.

Diamond is also an excellent thermal conductor. This feature could possibly be used to provide an efficient heat evacuation.

The precursors of diamond sensors were based on the ATLAS pixel modules, where the standard silicon sensitive volume was exchanged with diamond. Such devices were exposed to non-ionizing radiation fluence in the range of $1{\cdot}10^{16}$ $\mathrm{n_{eq}/cm^2}$ and tested with high-energy pion beam [74, 75, 76]. These sensor prototypes [74, 75] featured an extraordinary radiation tolerance against non-ionizing radiation. The devices exposed to $1.8 \cdot 10^{16} p/cm^2$ (24 GeV protons) still exhibited satisfactory performance required for efficient particle detection. At this fluence, a quarter of its original pulse height was observed, resulting into a SNR of 18 ± 6 at a field of 1 V/μm. Increasing the voltage to 2 V/μm improves the SNR up to 24 [74].

3.3 Classical Charge-Coupled Devices

The Charge-Coupled Devices (CCDs) are well-known from their imaging applications. These sensors were also used in the past for particle tracking in the vertex detector of the ACCMOR and SLD experiments [77]. The CCDs feature a good σ_{res} of less than 2 μm, reflecting their small pitch size. Since they are based on a <20-μm thick sensitive volume, they can be thinned down without any signal losses to a thickness of about 50 μm, corresponding to the material budget of about $0.05\%\ X_0$. Due to those features, CCDs were proposed to equip the vertex detector of the ILC experiment [3].

A simplified CCD matrix is sketched in Figure 3.6(a). The pixel array is organized in so-called vertical registers, separated from each other by "channel stoppers". A single pixel is featuring three transfer gates: P1, P2, P3, as shown in Figure 3.6(b). They control the

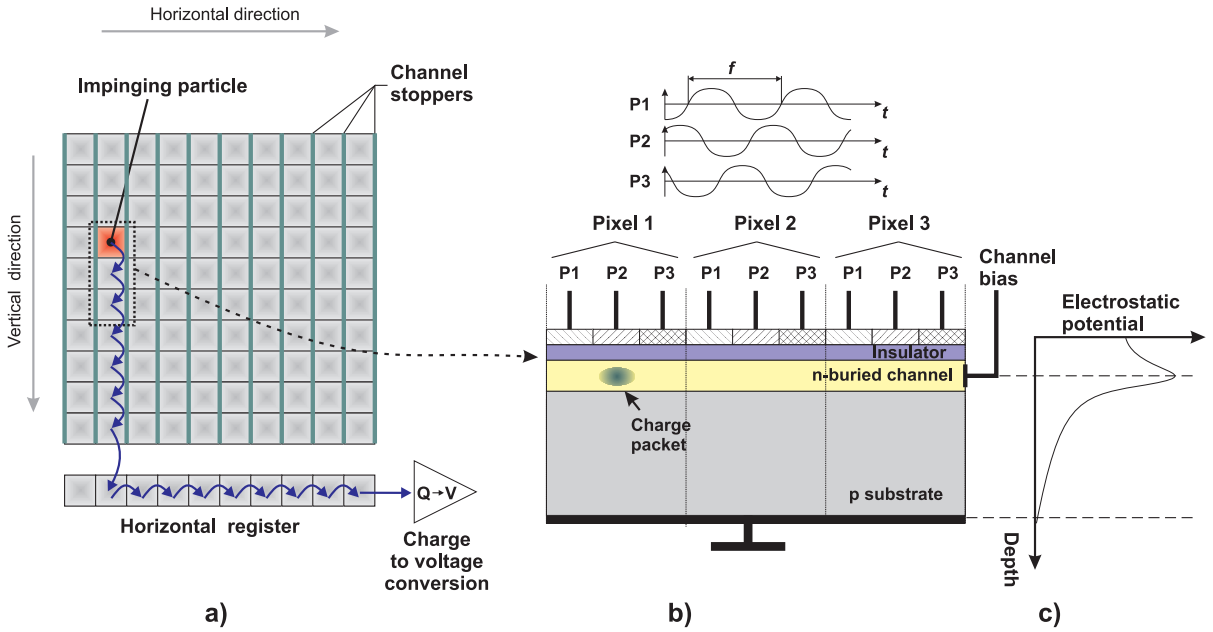


Figure 3.6: Charge-Coupled Devices: (a) A simplified CCD-sensor pixel array organized in vertical registers, separated from each other by "channel stoppers". (b) A cross-sectional view of 3 adjacent pixels of the n-buried-channel CCD: A single pixel is featuring three transfer gates P1, P2, P3 that control the charge transfer (vertical direction) towards a horizontal register. This register moves the charge packets towards the output, where the charge to voltage conversion is performed. (c) The electrostatic potential through the CCD: At the channel level, the electrostatic potential has a maximum.

charge transfer (vertical direction) towards a horizontal register. This register moves the charge packets towards the output, where the charge to voltage conversion is performed. A cross-sectional view of 3 adjacent pixels of the CCD is shown in Figure 3.6(b). The device presented is the n-buried channel CCD, where the charge transfer occurs in the n-type-silicon layer located underneath the transfer gates. At this level, the electrostatic potential has its maximum sketched in Figure 3.6(c). The charge is transferred inside the CCD channel due to the sinusoidal modulation of the electric field inside. The field is controlled by means of the clock pulses applied periodically to the transfer gates. The clock pulses feature the same amplitudes, but they are shifted in phase[5] by 120 °.

The signal charge has to cross a long way before arriving to the charge to voltage converter. This feature leads to significant charge losses after sensor irradiation, resulting in a moderate non-ionizing radiation tolerance (up to $\sim 1 \cdot 10^{10}$ $\mathrm{n_{eq}/cm^2}$) [78]. Noticeable effects are also observed after sensor exposure to ionizing radiation [79]. The flat-band-voltage shifts are as large as 7V/100 krad. The latter can be controlled by applying an external voltage (e.g., by external DACs), controlled by a dedicated chip. However, such compensation would have to be done on-line, with potential additional complications. The voltage control might be

[5] 3-phase CCD. In the case of 2-phase devices, the clock signals are in opposite phases.

implemented in the case of a vertex detector working in a uniform radiation environment (e.g., an experiment at the ILC). The implementation of this approach seems difficult for sensors working in an environment with non-uniform radiation levels. For this reason CCDs are not suitable for composing the CBM-MVD planes, where ionizing doses are expected to vary from tens of krad to few Mrad for the outer layers and central part, respectively. In such a case, the flat-band-voltage shifts should be tuned separately for each sensor, which is hard to afford.

Another weak point of the currently available CCD is their long readout time. These devices are read out in a rolling shutter mode. Their readout time depends on the sensor size (number of pixels) and it is mainly limited by the maximum frequency of signals applied to the transfer gates. This weakness prompted the R&D on Column Parallel CCD (CP-CCD) working at a 50-MHz clock frequency and aiming to fulfill the time resolution requirements of the ILC (see next section).

3.4 In-Situ storage Image Sensors

Simultaneously to the column-parallel CCDs, the CCD/CMOS-based sensors called ISIS (In-Situ storage Image Sensor) have been developed. They provide an alternative approach for the readout, with the timing of the ILC experiment in mind. Every 200 ms, the ILC will deliver 2820 e^+e^- bunches organized in $\sim$1 ms trains. The time gap between two trains is 200 ms. During this period, sensors are not impinged by particles. In order to keep the occupancy at an acceptable level for an efficient track reconstruction, the innermost layers of the vertex detector have to be read out at least 20-50 times during each train. Since this task is very challenging for the CCDs, innovative sensors with in-situ charge storage were introduced. The main idea of these sensors is to store the signal charges generated during single train collisions and to read out the signal during the 200 ms period between two consecutive bunch trains.

The ISIS are the devices based on the dedicated process that implements additional features inside a CMOS-like sensor (see Section 4.1.1). The concept of ISIS is presented in Figure 3.7. The readout circuits are insulated from the sensitive volume by means of a p+ -type silicon shielding layer. In the ISIS, the signal charge is generated by impinging particles in a high-resistivity EPI layer. The latter is partially depleted in the nearest surrounding of a deep n-type silicon implant called "a photogate". The charge generated in the EPI layer is reflected by the p+ type silicon shielding layer until it arrives to the photodiode. The signal charges are transferred from the photogate to the internal memory implemented in each pixel as a 20-cells long CCD register. The amount of memory cells was prompted by the necessity to keep the occupancy of the innermost layers of the vertex detector at a level of 1% or below. The memory cells are read out during the 200 ms quiet period. Since the raw charge is stored inside the pixels during beam spills and only converted into signal when there is no beam, ISIS is insensitive to the potentially intense electromagnetic waves produced by the electron-positron beam buckets circulating in the beam pipe. On the contrary, sensors with continuous charge-

to-signal conversion (i.e. MAPS) are sensitive to these parasitic waves.

The charge transfer in the ISIS occurs along the 20-cells-long CCD registers. As a consequence, the signal losses during the long transfers of the charge packets from the generation point to the output buffers should be strictly limited. For this reason, the ISISs should be more radiation-tolerant than their classical predecessors. The pixels implemented in the ISISs should feature a 20-µm pitch to ensure the required σ_{res}. Reduction of material budget by thinning the ISISs to 20-50 µm is planned for the future.

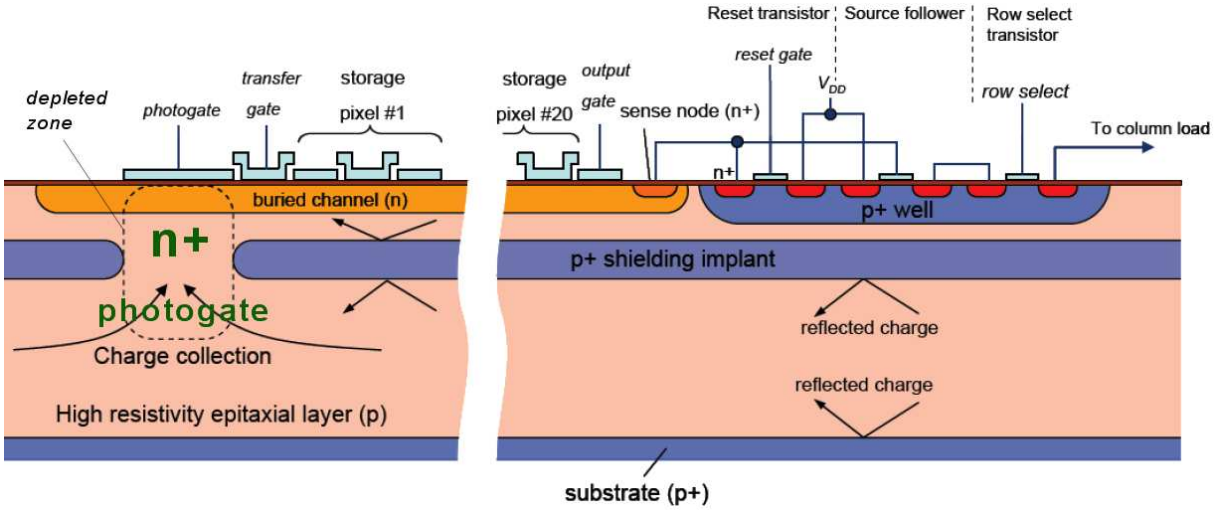


Figure 3.7: ISIS1 prototype cross-section [80]. This figure presents the principle of operation of the ISIS sensor. The charge generated by an impinging particle is transferred in the partially-depleted sensitive volume towards the photogate and it is stored in a burred CCD register. Next, the charge is converted to voltage by an in-pixel electronics (enclosed in p-well) and transferred towards the pixel output.

The first ISIS sensor was called ISIS1 and it aimed at validating the concept. The ISIS1 was based on a 50-µm-thick EPI layer and featured a matrix composed of 256 pixels of size 40×160 µm^2. There were only 5 memory cells implemented inside each pixel. The sensors were tested before irradiation with a 6-GeV electron beam [81]. A σ_{res} of 9.4 ± 0.1 µm was measured for the shortest pixel dimension. The ϵ_{det} did not exceed 35%. This poor efficiency is most likely a consequence of the asymmetric and large pixel pitch [82]. It can be also related to a not fully depleted EPI layer. As the EPI layer in the first ISIS prototype was 50-µm-thick, it cannot be excluded that the charges generated in the undepleted regions diffused thermally and were spread out between many neighboring pixels, resulting in a SNR too low for an efficient particle detection. It is also likely that due to large distances between sensing diodes, signal charges recombined in the sensing volume before being collected.

In terms of the readout, the ISIS concept seems to be well adapted to the running conditions of the ILC. Concluding, the ISIS represents an interesting and innovative idea to accommodate two sensor technologies into a single charge-sensitive device. However, before these sensors could compete with other devices, more R&D is required.

3.5 DEPFET sensors

The concept of the DEPFET pixel architecture was proposed in the late 80's by Kemmer and Lutz [83]. A simplified view of the DEPFET pixel cell is shown in Figure 3.8. The basic principle of the concept consists in a MOS transistor integrated onto the sensor substrate. The sensitive volume of the DEPFET sensor is fully depleted, using a p+ back contact. By means of a sidewall depletion and additional n- implant, the electrostatic potential reaches its maximum about 1 μm underneath the MOS transistor structure. There, a so-called internal gate is located. The charges generated by an impinging particle in the sensor volume drift towards the internal gate due to the electric field. The accumulation of the signal charge under the MOS gate changes the potential of the internal gate. This modulates the current flow through the MOS transistor channel.

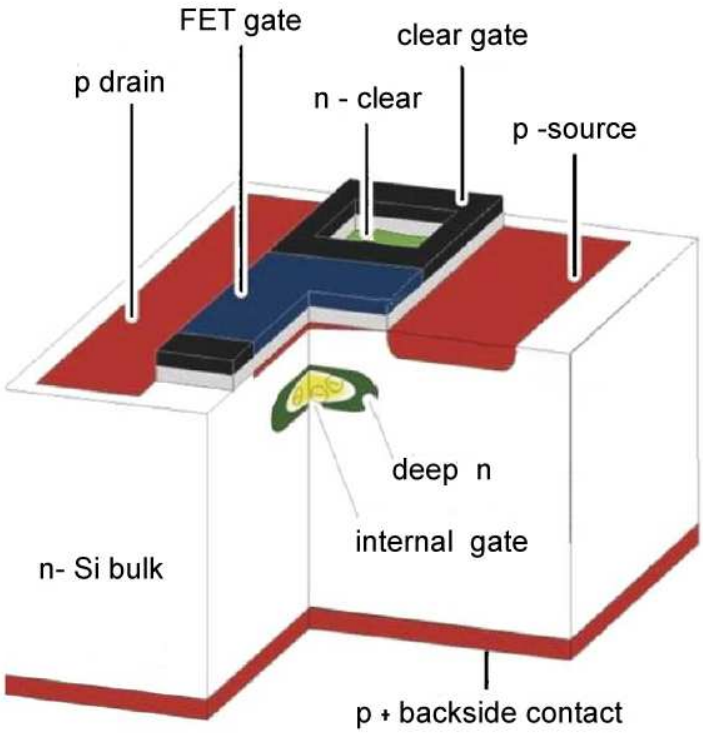


Figure 3.8:
This figure shows the principle of operation of the DEPFET sensor [84]. A MOS transistor is integrated onto the fully depleted sensor substrate. The electrostatic potential underneath the MOS transistor structure is formed in a way to reach its maximum at about a 1 μm depth. By means of the electric field, the charges generated by an impinging particle in the sensor volume are accumulated under the MOS gate. This changes the potential of the internal gate and consequently modulates the current flow through the MOS transistor channel.

Most of the time, a DEPFET cell is in the OFF state where the MOS transistor consumes almost no power. Even in this state, the proper bias is applied to deplete the sensor substrate so that the signal charges are collected underneath the MOS gate. During the readout cycle (ON state), a voltage above the MOS threshold is applied to the "FET gate". The transistor is then switched ON and its source to drain current is composed of a pedestal current due to both: the "FET gate" voltage, and the signal current. The latter is proportional to the charge collected inside the internal gate. Then, the signal charge is removed from the internal gate by means of a voltage applied to the "clear gate". The drain to source current is then measured again and considered as the pedestal current. The signal is obtained by subtracting the currents measured

in both readout cycles. Next, the "FET gate" is set back and the MOS transistor is in the OFF state again.

In order to operate the DEPFET-sensor matrix, two dedicated ASICs are needed. To achieve the readout time required for the ILC vertex detectors, both devices work at a frequency of 50 MHz. The first ASIC is responsible for the proper steering of the "FET gate" and "clear gate". The second one reads out the current signals from all columns in parallel. The currently manufactured DEPFET sensors are based on a 1.2-μm process and feature complex readout architecture requiring additional surface for implementation. This results in the areas insensitive to impinging particles and can be considered as a drawback.

The results published in [85] showed that the DEPFET sensors feature an electronic noise of about 50 e^-. However, the data obtained during beam tests [86] suggested an electronic noise of about 225 e^-.

The DEPFET sensors are typically based on 450-μm thick, high-resistivity and fully-depleted substrates. As a consequence, the signals generated by impinging particles in the sensitive volume are large. Signals in the range of 32500 e^- were registered [86] considering 3×3 pixels clusters, resulting in a SNR of approximately 140 for sensors before irradiation.

The σ_{res} of the DEPFET-sensor prototypes with pixel sizes between 22 and 36 μm amounted to 3-4 μm.

It is claimed that the DEPFET sensors may be thinned down to about ∼50 μm using a process described in [87]. However, this possibility has not been demonstrated yet.

The tolerance of the DEPFET sensors to ionizing radiation was assessed up to about 1 Mrad [88]. The MOS-threshold-voltage shifts of about -4 V and -6 V were observed for devices irradiated in OFF and ON state, respectively. As this shift can be compensated by means of an external voltage, irradiated devices were considered as still operational. However, such a threshold voltage compensation results in many complications, as it was explained already in Section 3.3.

By virtue of the depleted sensitive volume, the DEPFET sensors should provide a relatively high non-ionizing radiation tolerance. No significant deterioration of the sensor performance was observed after irradiation with protons ($3 \cdot 10^{12} p/cm^2$) and neutrons ($2{\cdot}10^{11}$ $\mathrm{n_{eq}/cm^2}$). Taking into account the charge transfer to the internal gate by means of an electric field, one may suppose that the DEPFET sensors will feature a good non-ionizing radiation tolerance. The studies related to the assessment of the sensor performance at higher non-ionizing-radiation fluences are ongoing [89].

At a first glance, the proven and claimed DEPFET performance leads to the conclusion that those devices seem to have a good potential for vertexing for the ILC experiments. Some of the drawbacks, like for example large threshold voltage shifts after sensor irradiation, may become difficult to handle in real experiments. DEPFET sensors are therefore most likely not well suited for the vertex detectors where a non-uniform irradiation is expected across the surface (e.g., the CBM experiment).

3.6 Silicon On Insulator sensors

The Silicon On Insulator (SOI) technology allows to design monolithic pixel sensors for radiation detection with many advantages with respect to devices fabricated in a standard bulk CMOS processes. The SOI implementation of microcircuits is performed on a thin silicon layer which is electrically insulated from the sensitive volume by means of a buried oxide (BOX). The insulation of the microcircuits from the sensitive volume allows using both type of transistors (PMOS and NMOS). This is a significant advantage over sensors implemented in standard CMOS processes, for example, MAPS described in Section 4.1.1. The proof of principle was addressed within the SUCIMA Collaboration [90], using a 3 μm process from IET, Poland [91, 92, 93].

There are several methods to insulate the sensitive volume from the electronics placed on the surface. One of the most interesting and particularly suited for particle detection is called the wafer bonding, as presented in Figure 3.9. The buried oxide is grown on the surface of a first wafer "A" (see Figure 3.9(a)). Then, a second wafer "B" is combined with the first one, as shown in Figure 3.9(b). The wafer "A" is then partially removed by plasma-associated chemical etching, Figure 3.9(c). The microcircuitry is implemented in the thin remaining slice from wafer "A". A cross-sectional view of the simplified SOI pixel cell is depicted in Figure 3.9(d). Other methods for isolating the integrated microcircuits from the substrate may be found in [94, 95, 96].

Besides the separation of the microcircuits from the sensitive volume, the SOI technology allows to mix wafers with different parameters. One may imagine a device featuring high-resistivity sensitive volume ensuring a fast signal charge transfer and a good radiation tolerance combined with another silicon slice, optimized for microcircuits [94].

As the transistors are separated from the sensitive volume, the SOI technology allows leakage currents on the orders of magnitude lower than those observed for devices implemented in bulk silicon to be achieved.

The devices implemented in the SOI technology feature two weak points. The first one is related to a coupling between the microcircuits and the bulk, the so-called back-gate effect. The name is related to the fact that the area under the transistor acts as a back gate which potentially affects the threshold voltage and the leakage current of the transistor. The second drawback of the SOI technology is its radiation softness. Due to the thick buried oxide separating the sensitive volume from the readout electronics, these devices may be particularly sensitive to ionizing radiation. It has indeed been observed that the SOI technology suffers from an accumulation of positive charges in the buried oxides, which leads to a coupling between the transistors and the sensitive volume [96]. As a consequence, the transistor threshold voltages are strongly modified by irradiation. Differences of a few hundreds of mV after a dose of a few hundreds of krad were observed [95]. Such large threshold-voltage shifts cannot be tolerated since they change dramatically the performance of the implemented microcircuits.

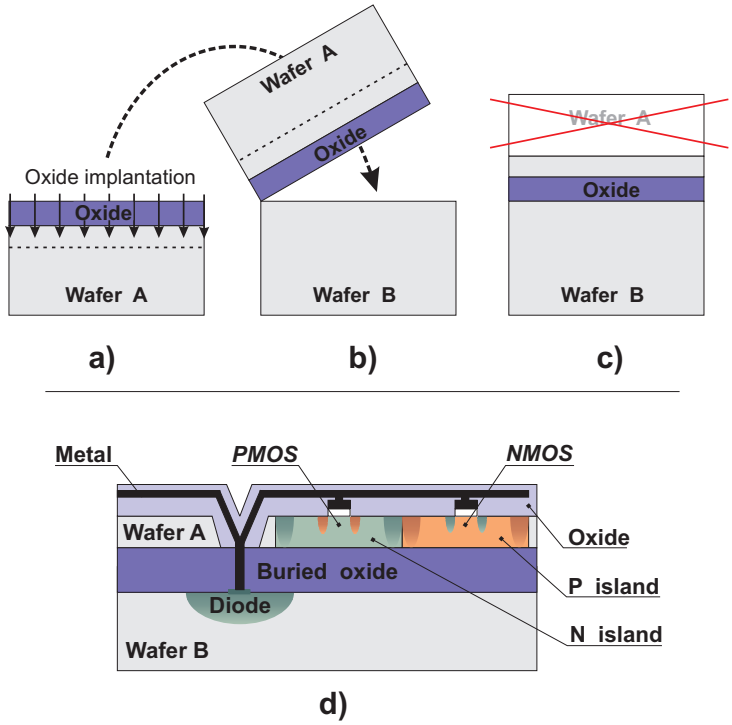


Figure 3.9: The concept of the SOI technology is based on insulation of the processing electronics from the sensitive volume by means of an insulation layer (buried oxide). This figure presents the wafer processing in the SOI process: (a) oxide implantation, (b) wafer bonding, (c) wafer etching and (d) simplified cross-section of the pixel implemented in this technology. Since the SOI process allows to mix wafers with different parameters, the sensitive volume and readout microcircuits can be optimized separately.

One possible solution could be to implement under the BOX a deep p-type dopants through the top Si layer which would then create a buried p-well (BPW) [97, 98]. Due to this operation, the back gate effect was observed to be suppressed or significantly limited also after sensor irradiation of up to 400 krad. However, after integration of larger doses, the transistors became not operational.

Due to these weak points, the implementation of SOI processes for particle detector purposes is still in the development phase.

3.7 Conclusions and summary

As it was discussed in Chapter 1, the requirements for the MVD of the CBM experiment are very severe: a readout time of ∼30 µs, σ_{res} of ∼5 µm, and tolerance to radiation of $>1{\cdot}10^{13}$ $\mathrm{n_{eq}/cm^2}$ and >3 Mrad. Considering all the sensors discussed in this chapter, only some of them have the potential to meet some of these requirements.

The HAPS, despite of their excellent radiation hardness and a short readout time, have to be

excluded as they feature a low σ_{res} and large material budget.

On the contrary, the CCDs feature a high σ_{res} and a low material budget, but they suffer from a low tolerance to radiation and long readout time.

Due to their construction and readout scheme, the ISIS cannot be considered as universal sensors for each application. Moreover, their performance has not been yet fully established. So far, they feature a modest σ_{res}, and their time resolution and tolerance to radiation are not precisely known.

The DEPFET sensors can potentially provide a good σ_{res}. Since they are based on a depleted substrate, also a reasonable non-ionizing radiation tolerance is expected. They probably can be thinned down to 50 µm or less, ensuring a material budget in the range of 0.05%. However, most of those features have never been demonstrated. The DEPFET sensors suffer from threshold voltage shifts after exposure to ionizing radiation. Those shifts may be difficult to handle at doses higher than 1 Mrad, and particularly in the case when the sensor surface is not uniformly irradiated. The feature size of 1.2 µm used for the DEPFET sensors brings another limitation. Due to the fact that the gate-oxide thickness for processes with such a feature size is large, the implemented devices are intrinsically radiation-soft. In addition, the implementation of a fast readout occupying a small area is not affordable.

The sensors implemented in the SOI technology may provide excellent non-ionizing radiation tolerance because they are based on a depleted substrate. This process has also a good potential for production of highly-granular and thin sensors. So far, the devices implemented in the SOI processes suffer from ionizing-radiation effects, particularly present in thick buried-oxide layers. The back-gate effect, significantly enhanced by ionizing radiation, results in transistors no longer operational. This effect is already pronounced even after sensor irradiation up to a few hundreds of krad.

Among the sensor technologies presented here, there is not a single one which could meet all the requirements of the upcoming high-energy physics experiments calling simultaneously for an excellent resolution, extremely low material budget, fast readout and high tolerance to radiation. This concerns also the CMOS pixel sensors, studied in this thesis work. However, as the CMOS sensors are fabricated using commercial processes, their development is very fast and relatively inexpensive. They offer an interesting compromise between a material budget, readout time and tolerance to radiation. These sensors are currently the most promising candidates to equip the CBM-MVD.

The CMOS pixel sensors are the subject of the three upcoming chapters. Chapter 4 intends to introduce in details this sensor technology. The basic architectures of the CMOS sensors will be presented. Also, the tools and measurement methods used in this thesis work to study the sensor parameters and to evaluate their tolerance to radiation are discussed. Chapter 5 and 6 present the studies addressed within the scope of this thesis aiming at enhancing the radiation tolerance of the CMOS sensors to the level required for the physics program of the

CBM experiment.

4 CMOS pixel sensors and status of their radiation hardness

To reconstruct particle trajectories with a high precision, high-energy physics experiments call for vertex detectors with an excellent impact parameter resolution. Such a resolution can only be achieved by equipping the vertex detector planes with pixel sensors featuring a high-granularity and low material budget. The vertex detector planes are placed close to the interaction point which translates into a high particle background. To cope with this background, the sensors must feature a short readout time (to reduce occupancy) and high tolerance to radiation. As it was discussed in Chapter 3, currently there is no sensor technology which could satisfy the needs of the upcoming high-energy physics experiments.

CMOS pixel sensors have a potential to satisfy these requirements in the near future. Several experiments are already interested in using CMOS sensors for their vertex detectors or for their upgrade. It is worth mentioning that the STAR-HFT is currently upgrading the vertex detector with CMOS sensors. The CBM experiment planned for 2015 also aims at using these devices. The ALICE experiment at the LHC is considering an upgrade of its vertex detector with CMOS sensors too.

This chapter discusses the principle of operation of MAPS regarding the signal creation and its transport from the EPI layer to the sensing diodes. The two basic in-pixel architectures used for test purposes and a basic sensor readout scheme will be presented.

The methodology for basic CMOS-sensor-parameter measurements such as electronic noise, leakage current and ϵ_{det}, required for radiation-tolerance assessment will be presented. The particle sources used for testing purposes and those employed for sensors irradiation will be described.

At the end of this chapter, the most important results obtained during radiation-tolerance studies carried out in the past at the IPHC will be presented.

4.1 CMOS pixel sensor – the device

4.1.1 Principle of operation

MAPS are implemented in standard CMOS processes. A particularly attractive advantage of these sensors is to integrate the sensitive elements and the processing electronics on the same substrate. The sensitive volume of these sensors is a p-type EPI layer (p-EPI), which is typically

10-20 μm thick. Figure 4.1(a) depicts the cross-sectional view of a CMOS-sensor pixel cell.

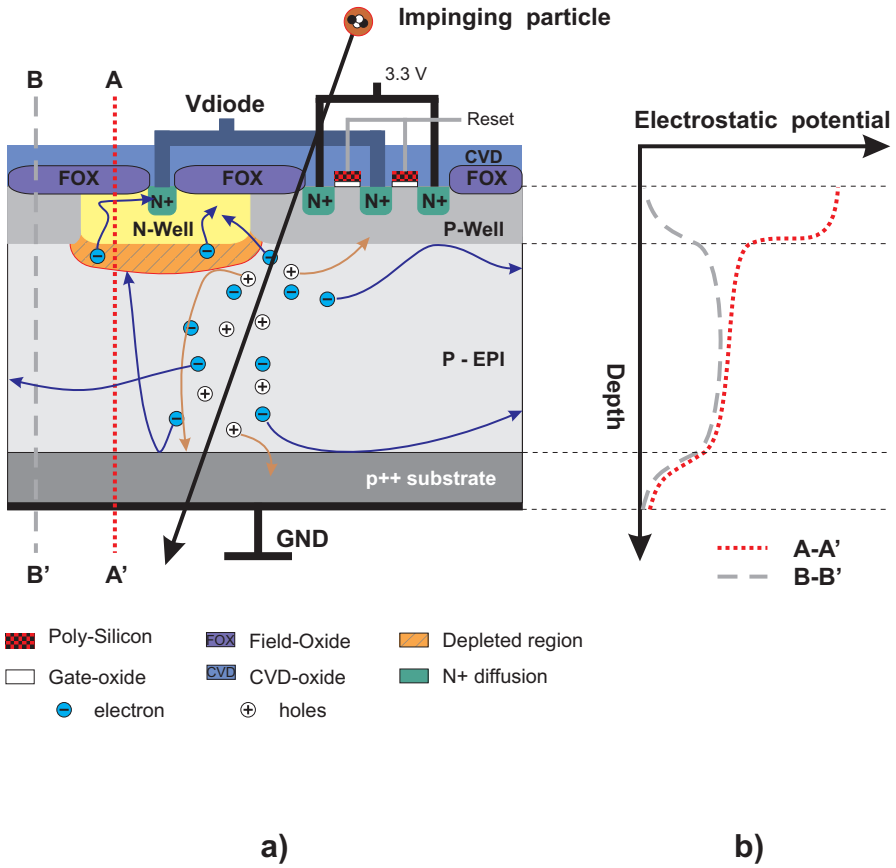


Figure 4.1: Figure (a) presents the cross-sectional view of a Monolithic Active Pixel Sensor showing the basic sensing element (N-Well) and the reset transistor, both implemented on the same substrate. The charge generated by an impinging particle is diffused thermally inside the EPI layer towards the sensing element. Figure (b) presents the electrostatic potential through the sensor volume in two points marked as A-A' (red dotted line) and B-B' (gray dashed line).

When incident particles cross the detector volume, e-h pairs are generated along their paths. As there is no electric field apart of a shallow (<1-μm) depleted region underneath the n-wells, the electrons created in the sensitive volume are thermally diffused in all directions. They are reflected back to the EPI layer by the p-EPI – p++ and the p-well – p-EPI interfaces. The diffusion continues until the electrons are intercepted by the regularly implanted collecting n-wells[1], where the electrostatic potential reaches its maximum (see Figure 4.1(b)). Within the n-wells, the electron charge is converted into a voltage on the sensing-diode capacitance. This voltage is transferred to a source-follower implemented in each pixel, and it is read out.

[1]Some electrons recombine in the crystal. The typical path for this to happen is on the order of 100 μm.

4.1.2 Pros and cons of CMOS pixel sensors

Since the creation of a useful signal occurs in CMOS sensors in a very thin EPI layer (typically 10-20 μm), the thick substrate does not participate in the charged particles detection. Therefore, most of the substrate can be removed without sensor performance loss and sensors can be thinned down to about 30-50 μm or even less. Thinned down MAPS expose a relatively low material budget of $\leqslant 0.05\% X_0$ (50 μm silicon) to traversing particles. Another prominent feature of CMOS sensors is their high granularity. The typical pixel pitch of MAPS is in the range of 10-20 μm. This allows achieving a σ_{res} of $\sim$1 μm. Due to the fact that those devices accommodate on the same substrate signal processing electronics, they usually do not require any external readout controllers. CMOS sensors feature excellent detection performance. Typically, a ϵ_{det} above 99.5% for an Average Fake Hit Rate (referred by FH_{rate} in Section 4.2.4.3) below 10^{-4}. The radiation hardness of those devices was assessed to be of 1 Mrad and $1{\cdot}10^{13}$ $\mathrm{n_{eq}/cm^2}$ [7]. More detailed information about the status of radiation tolerance of MAPS is given in Section 4.3. Moreover, the production costs of MAPS is low and the time needed for development is short (multi-project run schedule).

There are also disadvantages of CMOS sensors. One of them is the thin sensitive volume which translates into small signal amplitudes, typically 800-1200 $\mathrm{e^-}$ for a MIP. The sensitive volume of MAPS fabricated in standard processes is almost undepleted. Consequently, the signal collection in the EPI layer occurs due to thermal diffusion. The typical time needed for the charge collection from $\sim$15-μm-thick EPI layer is $\sim$100 ns [99], which sets a theoretical limit for a maximum readout time of those devices. Since there is no electric field inside the sensitive volume that could focus the charge movement in a particular direction, the charge generated by impinging particles is spread over several pixels. Only a small fraction of the initial charge (typically 20-25%) is stored in the seed pixel. Consequently, the SNR governing the sensor performance, do not typically exceed 30. The undepleted sensitive volume has another drawback: an increased probability for the signal charges to interact with the radiation-induced traps. This feature is reflected by a moderate tolerance of MAPS to non-ionizing radiation.

Furthermore, the implementation of electronic microcircuits inside the pixels is limited since only NMOS transistors can be used in the sensitive area. In a typical CMOS process, the PMOS transistors are implemented into additional n-wells. In the case of CMOS sensors, these n-wells would not be insulated from the EPI layer and they would participate in the charge collection. This feature prevents the implementation of PMOS-based amplifiers featuring a high gain. As a consequence, the signal amplification and its separation from the electronic noise can be realized only to some extent, as it is presented in Chapter 5. The CMOS process[2] currently used for MAPS fabrication imposes several additional limitations. One of them is the feature size which restricts the number of transistors that can be accommodated inside a pixel.

[2]The 0.35-μm process from AustriaMicroSystems (AMS).

Another one is the ionizing radiation tolerance. The larger the feature size, the thicker the gate oxide, which impacts the sensor tolerance to this type of radiation. Moreover, in the AMS 0.35-µm process, sensor design is limited to 4 metal layers, which imposes a certain readout organization.

Most of those obstacles can be overcome by implementing the sensors in CMOS processes with smaller feature size than 0.35 µm. These processes provide more metal layers for interconnections. Since they feature a thinner gate oxide, they are intrinsically more tolerant to ionizing radiation. Some of them also provide deep p-wells that can be used to insulate the n-wells hosting the PMOS transistors from the sensing diodes. These deep p-wells provide an opportunity to accommodate both types of MOS transistors in a single sensor without the risk of charge losses. Such processes became recently available for the CMOS sensors implementation and they will be explored at the IPHC-Strasbourg in near future.

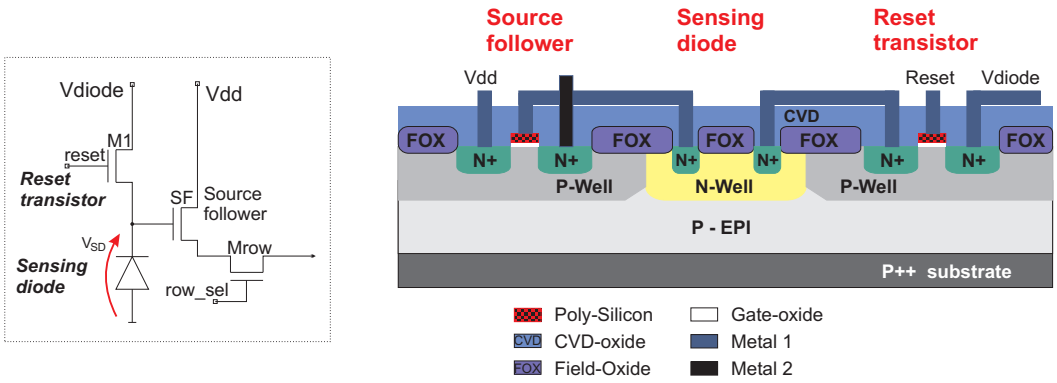
4.1.3 Basic in-pixel architectures implemented in CMOS pixel sensors

In the following section, the two simplest and frequently used in-pixel architectures are presented. Historically, the principle of operation of MAPS was demonstrated with sensors featuring a simple "three transistor" in-pixel architecture, as sketched in Figure 4.2(a). This architecture is named "three transistor" (3T) since it is based on three transistors required for pixel operation. In this architecture, a sensing diode is connected with a reset transistor ($M1$) and a source follower (SF). To compensate the sensing-diode voltage decay caused by the leakage current, the sensing diode is periodically connected to the reference potential ($Vdiode$). This is done by the means of the reset transistor and it is schematically sketched in Figure 4.2(b). The phase when the reset transistor is closed by applying a steering signal to its gate is called a "reset phase". The next phase corresponds to the integration of the signal (integration phase).

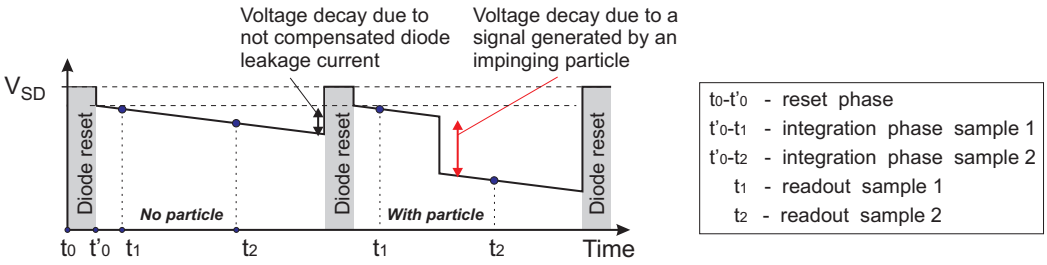
For the purpose of the Correlated Double Sampling (CDS) discussed in detail in Section 4.2.1, the diode voltage is read out twice between two consecutive reset pulses. The two samples are then subtracted from each other to identify a useful signal. The first read out occurs just after a reset and the second one after a time called "integration time", which is usually equivalent to the time needed for full sensor readout. Even in the absence of signal from particles crossing the detector, the result of this subtraction can be different from zero. This difference is usually called "offset", and it can be used for the sensing-diode-leakage-current assessment. The offset varies from one pixel to another, reflecting the diode-leakage-current fluctuations originating from non-uniformities of the fabrication process.

The 3T architecture was implemented in most of the sensors studied in this thesis because it is adequate for sensor characterization purposes. Particularly, the 3T architecture allows for measurements of the sensing-diode leakage current.

The 3T architecture features a "dead time" during which the pixel is insensitive to impinging particles. Depending on the readout and reset organization inside the sensor, this dead time can reach up to 50%.



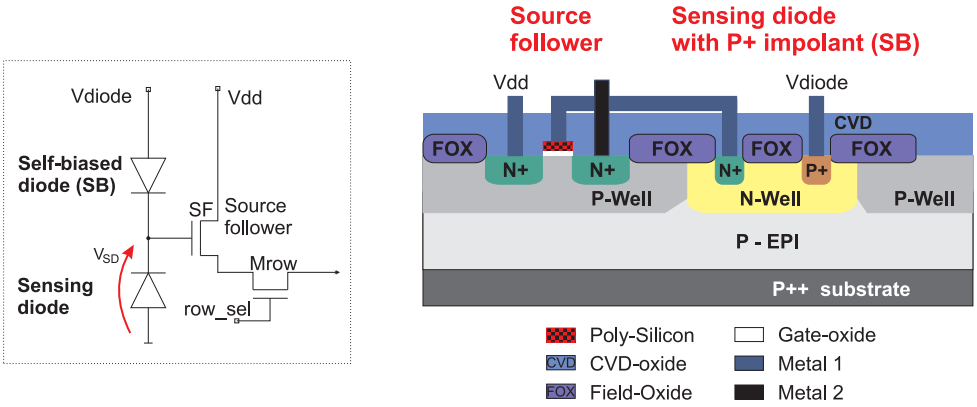
(a) Schematic (left) and cross-sectional view (right) of the 3T pixel architecture.



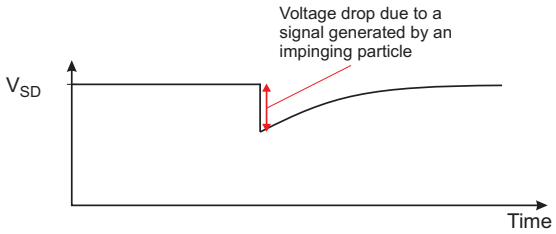
(b) Pixel timing.

Figure 4.2: Figure (a) presents the schematic view of the 3 transistor (3T) pixel cell (left) and its cross-sectional view (right), including: the sensing diode, the source follower and the reset transistor. The time diagram of the 3T architecture is shown in (b).

The second basic and frequently used in-pixel architecture is called "self-biased" (SB). This solution is based on two transistors and one diode polarized in the forward direction. The SB architecture is presented in Figure 4.3. This idea originated from CMOS-sensor imaging applications, where devices capable of operating with a high-dynamic range of input signals are required. Those devices feature a logarithmic response to a photocurrent. Such a response was achieved with a MOS transistor connected to the sensing diode and operating in the weak inversion region [100, 101, 102]. In the logarithmic pixel proposed for particle tracking, the charge collecting diode is reverse-biased, while a forward-bias is applied for the other diode.



(a) Schematic (left) and cross-sectional view (right) of the SB pixel architecture.



(b) Pixel timing.

Figure 4.3: Figure (a) presents the schematic view of the SB pixel cell (left) and its cross-sectional view (right), including: the sensing, the forward-biased diodes and the source-follower transistor. The time diagram of the SB architecture is shown in (b).

The SB architecture can be modeled as an *RC* circuit, composed of the dynamic resistance[3] of the forward-biased diode and of the reverse-biased junction capacitance of the sensing diode. At the equilibrium, the sensing diode voltage does not change, and amounts approximately to $V_{diode} - R \cdot I_{leakage}$ (see Figure 4.3(a) for V_{diode} meaning). The equilibrium state can be described as follows:

[3]For the calculations presented here, it will be assumed that R is constant.

$$\frac{Q_{equilib}}{C_{diode}} + R \cdot I_{leakage} = V_{diode} \tag{4.1}$$

When the sensing diode collects the charge deposited by an impinging particle, the voltage of this diode decreases, as depicted in Figure 4.3(b). A slow recovery of the sensing diode voltage level occurs to reach the equilibrium state again. The charge Q delivered by an impinging particle is slowly removed by the current I. The non-equilibrium state can be described as:

$$\begin{aligned}\frac{Q_{equilib} + Q(t)}{C_{diode}} + R \cdot (I_{leakage} + I(t)) = \frac{Q_{equilib}}{C_{diode}} + \frac{Q(t)}{C_{diode}} + R \cdot I_{leakage} + R \cdot I(t) \\ = V_{diode}\end{aligned} \tag{4.2}$$

By comparing the two expressions for V_{diode} given by Equations (4.1) and (4.2), it can be concluded that:

$$\frac{Q(t)}{C_{diode}} + R \cdot \frac{dQ(t)}{dt} = 0 \tag{4.3}$$

The solution of such an equation is:

$$Q(t) = Q_0 \cdot exp(-\frac{t}{\tau}) \tag{4.4}$$

where $\tau = R \cdot C_{diode}$ is the recharge time constant. The time constant is strongly dependent on the sensing-diode properties. At equilibrium, the forward-biased diode conducts only the leakage current from the sensing diode. This current is usually small, in the range of 1 fA, and the diode dynamic resistance R is very high. As a consequence, the recharge time constant typically reaches several milliseconds.

If the sensing-diode leakage current increases, the current flow through the forward-biased diode also increases. This results in a decrease in the recharge time constant τ. This decrease, in parallel with a long integration time, may lead to reduction of the signal amplitude.

The SB architecture features several advantages with respect to the 3T one. One of them is the fact that it does not need applying a periodical reset to compensate the sensing diode voltage drop. Consequently, there is no dead time and the readout scheme of such an architecture can be simplified. As the reset transistor is not used here, there is more space to implement the in-pixel electronics. Also, the Fixed Pattern Noise (FPN)[4] originating from the reset-transistor non-uniformities is eliminated. On the other hand, due to constant biasing, the SB architecture does not allow for leakage-current measurements that are possible with the 3T architecture.

[4]This type of noise will be discussed in Section 4.1.4.2.

4.1.4 Noise and its sources in CMOS pixel sensors

4.1.4.1 Temporal noise

The term "temporal noise" is used to describe temporal fluctuations of the values of the pixel output voltage when its input is constant. This type of noise is particularly important for MAPS. These sensors feature a relatively small active volume where the impinging particle generates a limited amount of signal electrons. Since the signal amplitude is low, the temporal noise is the major player influencing the SNR, which governs the sensor performance. The temporal noise analysis in MAPS is complicated since it requires considering the non-stationary character of the device and of the noise sources. Such an analysis can be found in [103]. Several components of the temporal noise can be distinguished: thermal noise, shot noise and $1/f$ (flicker) noise.

The **thermal noise** (also called Johnson–Nyquist noise) is the electronic noise originating from the thermal agitation of the charge carriers (usually the electrons) inside an electrical conductor (e.g., resistor) at equilibrium, which happens regardless of the applied voltage. The thermal noise is approximately a white noise, which means that its power spectral density is nearly constant throughout the frequency spectrum. The mean square of the noise voltage value is proportional to the conducting resistance of the medium, temperature and bandwidth taken for measurements.

The **shot noise** in electronic circuits is due to the quantized nature of the electric charge. It consists of random fluctuations of the electric current. The current flow is not continuous, but results from the motion of charged particles. At the microscopic level, the current varies in an unpredictable way and this unpredictable variation is called noise.

The **1/f noise** (also called flicker noise) is the noise featuring a power spectral density inversely proportional to the frequency. In the CMOS sensors, the $1/f$ noise is originating predominantly from MOS transistors. There are two different theories explaining the physical origin of the $1/f$ noise in MOSFETs. In the carrier number fluctuation theory proposed by McWhorter [104], the flicker noise is attributed to the random trapping and de-trapping process of charges in the oxide traps near the $Si - SiO_2$ interface. The charge fluctuations result in variations of the surface potential which in turn modulates the channel carrier density. The mobility fluctuation theory, proposed by Hooge [105], considers the source of the flicker noise to be due to the fluctuations in the mobility of the free charge carriers. The most recent theories assume that the $1/f$ noise is caused by the summation of Random Telegraph Signals (RTS - discussed in Section 4.1.4.3) originating from many individual traps located in the gate oxide.

For the purpose of this thesis, the noise sources in the 3T pixel cell will be investigated. The noise analysis will be performed separately for the three states of the pixel operation: reset, integration, and pixel readout.

Noise during the reset phase: During the sensor operation, the diode voltage has to be

periodically reset to remove the collected charge or to compensate the sensing-diode leakage current. During the reset phase, the gate of the reset transistor $M1$ is set to the potential of the power supply (*Vdd*). The reset transistor starts to conduct the current and the fluctuations of its flow result in a shot noise. Depending on the sensing diode voltage, the transistor is saturated during a short time period and then goes to the subthreshold region for the rest of the reset phase (for low diode voltages). For low diode voltages, the reset transistor is not saturated during the reset. In the case of very long reset-time, greater than the set-time, the steady state is achieved. However, the reset-time is usually very short (a few tens of nanoseconds) in real sensor applications and the steady-state is not reached. In this case, the mean square value of the reset noise is given by the following Equation [106]:

$$\overline{V^2}_{reset} = \frac{1}{2}\frac{k \cdot T}{C_{diode}} \tag{4.5}$$

where *k* is the Boltzman constant, T is the absolute temperature, and C_{diode} is the sensing-diode parasitic capacitance.

The reset-noise contribution expressed in equivalent charge units can reach a few tens of electrons, while a signal charge generated by an impinging particle amounts typically to a few hundreds of electrons. One can notice that the reset-noise contribution is significant. This noise is reduced efficiently by the CDS operation discussed in Section 4.2.1.

Noise during the integration phase: After a pixel reset, the diode integrates the signal charge. During this integration, the main contribution to the temporal noise comes from the shot noise, which is a consequence of the diode leakage current. The mean square value of the temporal noise during the reset phase is given by:

$$\overline{V^2}_{integration} = \frac{q \cdot I_{leakage}}{C^2_{diode}} \cdot t_{integration} \tag{4.6}$$

where *q* is the electric charge, $I_{leakage}$ is the sensing-diode leakage current, C_{diode} is the sensing-diode parasitic capacitance, and $t_{integration}$ is the integration time.

The equivalent noise charge (ENC) can be estimated from the following equation:

$$ENC[e^-] = \sqrt{\frac{I_{leakage} \cdot t_{integration}}{q}} \tag{4.7}$$

The typical value of the diode leakage current before irradiation is on the order of a few fA at room temperature. The value of 1 fA is used here for simplicity. For an integration time of 100 µs, the shot-noise contribution during the integration time is $\sim$1 e^-. One can conclude that in such conditions, the contribution of the shot noise due to the diode dark current is negligible in comparison to the signal charge. After sensor irradiation, for example, up to 1 Mrad, the leakage current of the sensing diode may increase to a few hundreds of fA. Considering a

leakage current of 100 fA after irradiation, the shot-noise contribution during an integration time of 100 µs is approximately 8 e^-. The temporal noise of ∼25 e^- can be expected for an integration time on the order of a millisecond. The leakage-current increase subsequent to the ionizing-irradiation dose may translate into a substantial SNR deterioration. The reduction in the temporal-noise contribution can be achieved by decreasing the integration time, or by reducing the leakage current. An efficient suppression of the leakage current is obtained by cooling the sensors.

Noise during the read out phase: During the readout phase, the main contribution to the temporal noise originates from the source follower SF, the access transistor M_{row} and other transistors composing the readout chain (e.g., M_{col} and M_{cur} shown in Figure 4.7(a)). The electronic components ensuring the signal amplification and its transfer from the chip to the readout system also contribute to this noise category. The temporal noise during the readout phase can be reduced by optimizing the sensor design, for example, by a careful selection of transistor parameters (e.g., a transistor channel transconductance g_m, an output drain conductance of a transistor g_{ds}) and of the load capacitance (C_{load}) value (see Section 4.2.2.1).

The 1/f-noise contribution originates mainly from the reset transistor and the source follower. For submicron n-channel MOSFET, the equivalent $1/f$ noise power spectral density of the drain current is described by the following equation:

$$S_{Id}(f) = \frac{g_m^2 q^2 kTN_t}{2C_{ox}^2 WL\gamma f} \tag{4.8}$$

where g_m is the transistor channel transconductance, C_{ox} is the gate-oxide capacitance, q is the electron charge, N_t is the trap density, k is the Boltzman constant, T is the absolute temperature, W and L are the transistor width and length, respectively, γ is the tunneling constant and f is the frequency.

4.1.4.2 Fixed Pattern Noise (FPN)

The sensing-diode-output-voltage pedestal varies from one pixel to another. The standard deviation of the pedestal distribution is called Fixed Pattern Noise. The FPN originates from the accuracy and the reproducibility of the CMOS fabrication processes. They are limited due to mask production mismatches, doping concentration variations, or a contamination during fabrication. For example, identically designed MOSFET transistors may exhibit different threshold voltages, different gain or different transistor channel width to length ratio (W/L) after fabrication.

4.1.4.3 Random Telegraph Signal (RTS)

The RTS is a multi-bistable current waveform reassembling seen in many devices including bipolar transistors, MOSFETs, JFETs, diodes and many others. As this document is dedicated

to CMOS sensors, the RTS originating from MOSFETs and the detector bulk will be addressed here.

The RTS is seen in CMOS sensors as a modulation of the sensing-diode leakage current or of the transistor drain current. The modulation of the sensing-diode leakage current is due to lattice defects acting as generation-recombination centers. In the case of MOS transistors, the RTS originates from traps located near to the $Si - SiO_2$ interface.

The leakage current of a diode or transistor observed in some period of time is presented in Figure 4.4. The pixel showed on the top of the figure exhibits the RTS whereas the one at the bottom does not. The times t_1 and t_2 correspond to the time when the two samples required for the CDS operation are taken. In the case of RTS, the CDS operation may result in a signal equal to the difference between two current levels (A_{RTS}), which actually cannot be distinguished from a signal generated by an impinging particle. For a sensor with data sparsification discussed in Chapter 5, the RTS may introduce substantial data load to the readout chain and consequently it may impact on the particle-tracking performance.

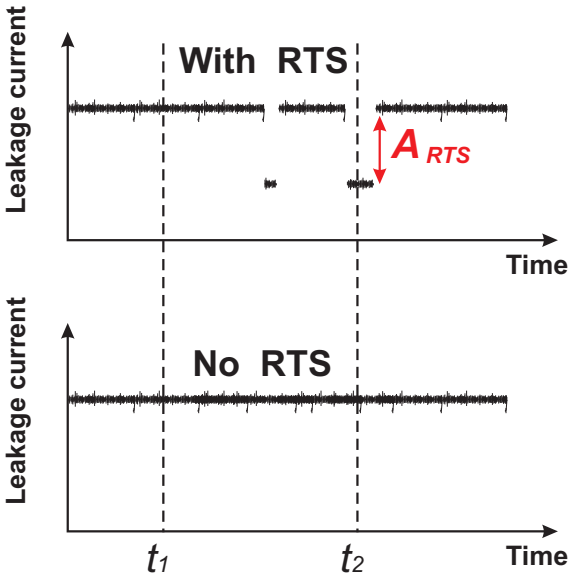


Figure 4.4:
Illustration of standard and RTS pixels. A simplified representation of a pixel output voltage featuring RTS signals (top). When 2 samples taken at the times t_1 and t_2 are subtracted from each other for correlated double sampling purposes, it results in some voltage drop at the output node and can be considered as a real signal. The figure at the bottom represents a pixel output without RTS signals.

The RTS has been studied with numerous CMOS sensors and CCDs [107, 108, 109, 110, 111, 112]. Despite the same origin of the RTS (related to traps), the impact on the sensor performance was strongly dependent on the process quality and sensor characteristics such as: biasing, readout architecture, readout time, temperature, and radiation levels. The RTS in submicron MOSFETs were observed to disappear after exposure to ionizing radiation and it turned into 1/f noise increase. For CMOS sensors, an increase in the number of the RTS pixels was not observed after exposing to ionizing radiation. Instead, a large number of the RTS pixels was observed after exposing sensors to non-ionizing radiation [107].

The correlation between irradiation and RTS noise has not been studied in this document.

4.2 Tools and measurement methods

4.2.1 Correlated Double Sampling

The CDS is a frequently used technique to reduce the influence of low-frequency noise components (e.g., the reset noise) and to extract the signal from the data. For the CDS, two consecutive signal samples are used. This technique is used differently in the case of the 3T and the SB architectures. Both cases will be described hereafter.

In the case of the 3T architecture, the two consecutive signal samples for the purpose of CDS are read out in the following manner. First, there is a "reset phase" when all the sensing diodes are connected to the reference voltage V_{SD} (see Figure 4.5). Due to the charge injection from the reset transistor, the sensing diodes are set to the V_{rst} voltage when the reset phase is over. Then, all the pixels are read out one by one in a rolling shutter mode. When the last pixel is accessed, the read out begins from the first pixel. However, this time the access to the first pixel is not followed by the reset phase. When the whole pixel matrix is read out again, the sensor is re-set. Consequently, each pixel is accessed twice between two reset phases.

Figure 4.5(a) displays the time diagram for the CDS technique for two cases: (left) when there is no signal from an impinging particle, and (right) when a signal is present. The two signal samples are taken at time t_1 (the first sample after reset) and t_2 (second sample). The charge integrated on the diode capacitance at time t_1 contains several components: $Qrst$, $Qleak_1$ and $Qnoise_1$. The $Qrst$ component represents mainly the charge injected from the reset transistor, kTC noise and low-frequency pick-up noise. The $Qleak_1$ corresponds to the sensing-diode leakage current. The temporal noise is represented by $Qnoise_1$. The charge integrated on the sensing diode at times t_1 and t_2 is in Figure 4.5(b), and the result of the CDS operation is presented in Figure 4.5(c).

Figure 4.5 depicts also the time diagram for the CDS operation in the case when the signal from impinging particle is present. Different symbols t'_1 and t'_2 (corresponding to time t_1 and t_2) are used to distinguish those two cases.

At the time t_1 (t'_1), the diode capacitance contains the following charge components:

$$Q_{t1} = Qrst + Qleak_1 + Qnoise_1 \tag{4.9}$$

and

$$Q'_{t1} = Q'rst + Q'leak_1 + Q'noise_1 \tag{4.10}$$

The second access to the pixel occurs at the time t_2 (t'_2). If there is no signal generated by an impinging particle, the charge integrated in the sensing diode is given by:

$$Q_{t2} = Qrst + Qleak_2 + Qnoise_2 \tag{4.11}$$

but when the signal is present:

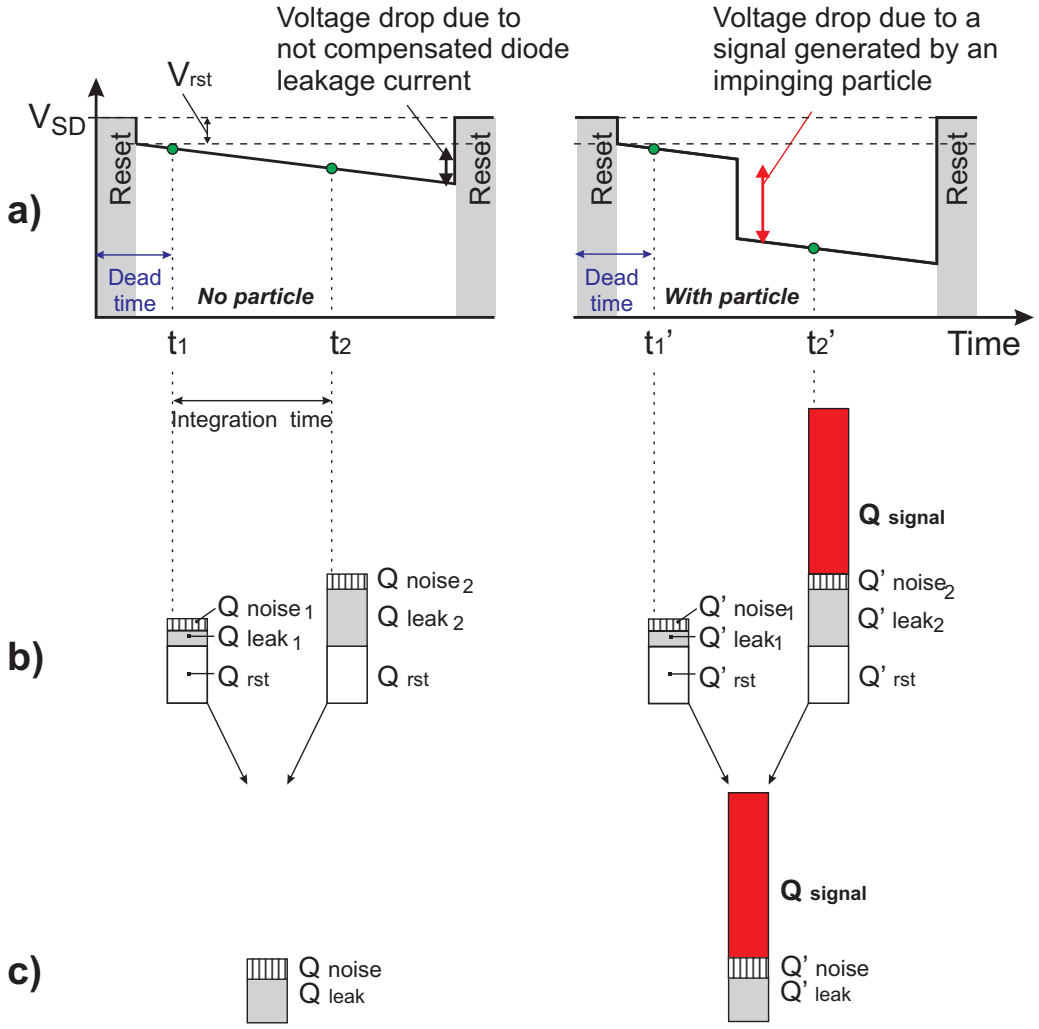


Figure 4.5: Correlated Double Sampling operation – 3T pixel example. (a) Time diagram for two cases: without impinging particle (left) and with impinging particle (right); (b) Bars represent the charge components integrated on the diode capacitance; (c) Result of the CDS operation.

$$Q'_{t2} = Q'rst + Q'leak_2 + Q'noise_2 + Qsignal \tag{4.12}$$

where $Qsignal$ corresponds to the charge generated by the impinging particle.

The two samples taken at time t_1 (t'_1) and t_2 (t'_2) are correlated. Consequently, the component $Qrst$ ($Q'rst$ respectively), for example originating from the charge injection from the reset transistor, is removed by subtraction of the two samples. The result of this subtraction presented in Figure 4.5(c) is given by the following equation:

$$\begin{aligned} Q^{CDS}_{NoParticle} &= Qrst + Qleak_2 + Qnoise_2 - (Qrst + Qleak_1 + Qnoise_1) \\ &= Qleak + Qnoise \end{aligned} \tag{4.13}$$

$$\begin{aligned} Q^{CDS}_{WithParticle} &= Q'rst + Q'leak_2 + Q'noise_2 + Qsignal - (Q'rst + Q'leak_1 + Q'noise_1) \\ &= Q'leak + Qsignal + Q'noise \end{aligned} \tag{4.14}$$

The frequency response of the CDS circuit was studied by several authors [113, 114]. The CDS is acting as a high-pass filter with a corner frequency corresponding to $1/t_{int}$ (t_{int} is an integration time). The studies indicated that the low-frequency noise is efficiently reduced by the CDS but it is not completely filtered. Moreover, those unfiltered components may contribute to the tail of the pixel-noise distribution. The filtering efficiency depends on the integration time and initial power spectral density of the low-frequency noise. Shorter integration times lead to a better rejection of low-frequency signals. The filtering is less effective in the case wherein a significant low-frequency noise was initially present.

The temporal noise components taken at the times t_1 (t'_1) and t_2 (t'_2) are not correlated, hence they are added quadratically:

$$Qnoise = \sqrt{Qnoise_1^2 + Qnoise_2^2} \tag{4.15}$$

$$Q'noise = \sqrt{Q'noise_1^2 + Q'noise_2^2} \tag{4.16}$$

It is worth to notice that in this readout scheme, the 3T pixels feature a dead time. This time corresponds to the time between the start of the pixel reset and the first access to the pixel after the reset. If impinging particles cross the pixel during this dead time, they will not be seen as $Qsignal$ will be present in both samples. The CDS performed on those samples will cancel the $Qsignal$ contribution.

In the case of the SB architecture, there is no reset needed and this architecture does not feature a dead time. The output of each sensing diode is periodically sampled (period equal to the integration time) and the CDS is performed for two consecutive signal samples. Figure 4.6 illustrates the sensing diode voltage in the SB pixel architecture as a function of time. The time when the pixel is accessed is indicated by the green dots. At the bottom of the same figure, the result of CDS operation is indicated using gray columns. When the pixel is in equilibrium, the CDS operation gives ”0”. This reflects the fact that the leakage current of the sensing diode is constantly compensated by the forward-biased diode. The presence of an impinging particle results in a decrease in the sensing diode voltage (V_{SD}). This corresponds to the highest value of a signal after the CDS operation. Then, the result of the CDS operation decreases because the charge generated by an impinging particle is constantly compensated by the means of the forward-biased diode.

For sensor characterization purposes, the signal samples taken at the times t_1 and t_2 are

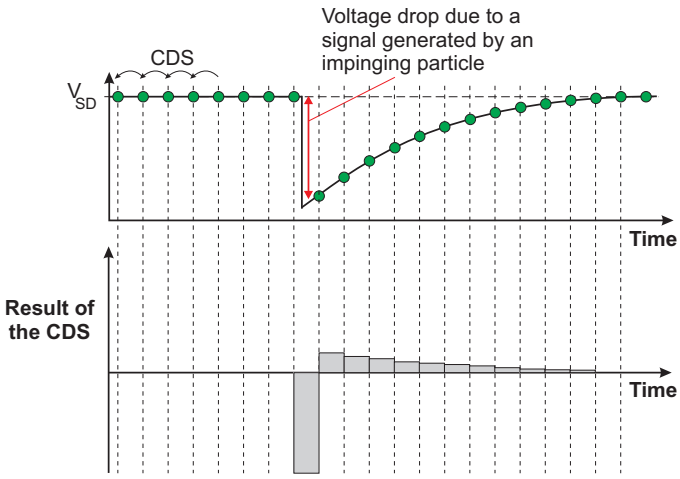


Figure 4.6: CDS operation for the SB pixel: time diagram of the sensing diode voltage (top); results of the CDS operation (bottom).

initially stored in the PC and then the CDS is performed off-line using analysis software. The column-parallel MAPS studied in Chapter 5 feature the CDS circuits implemented inside each pixel.

4.2.2 Measurements – sensor readout and setup

4.2.2.1 Basic readout architecture

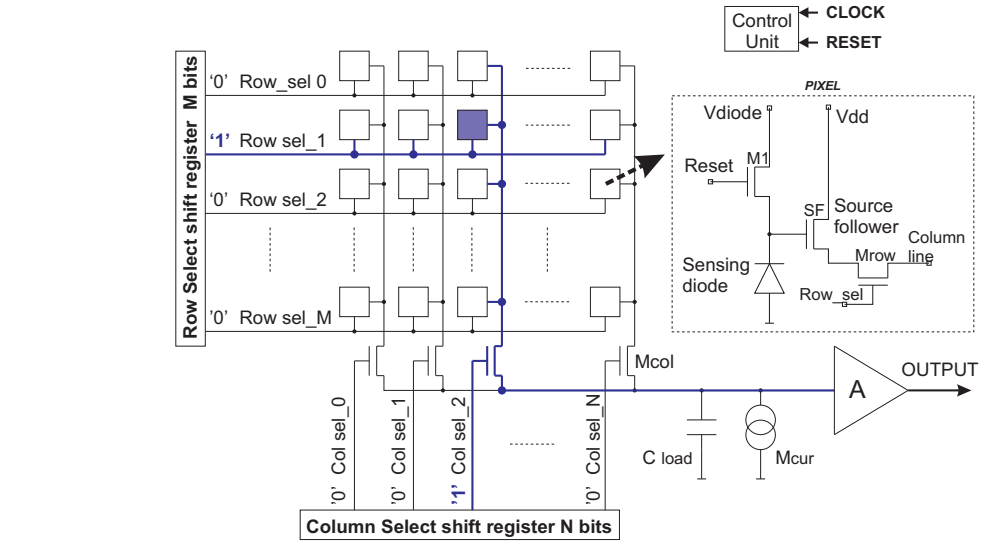
CMOS sensors consist of thousands of individual pixels regularly distributed over the silicon surface. They form an "array of pixels". The array is usually read out by accessing the individual pixels sequentially. Such a readout scheme is presented in Figure 4.7.

In order to perform the CDS operation, the pixel array is read out twice. The first read out occurs just after the reset phase and the second one after the integration time. This time is inversely proportional to the frequency of the externally delivered clock signal, and it is directly proportional to the number of pixels as defined by the following expression:

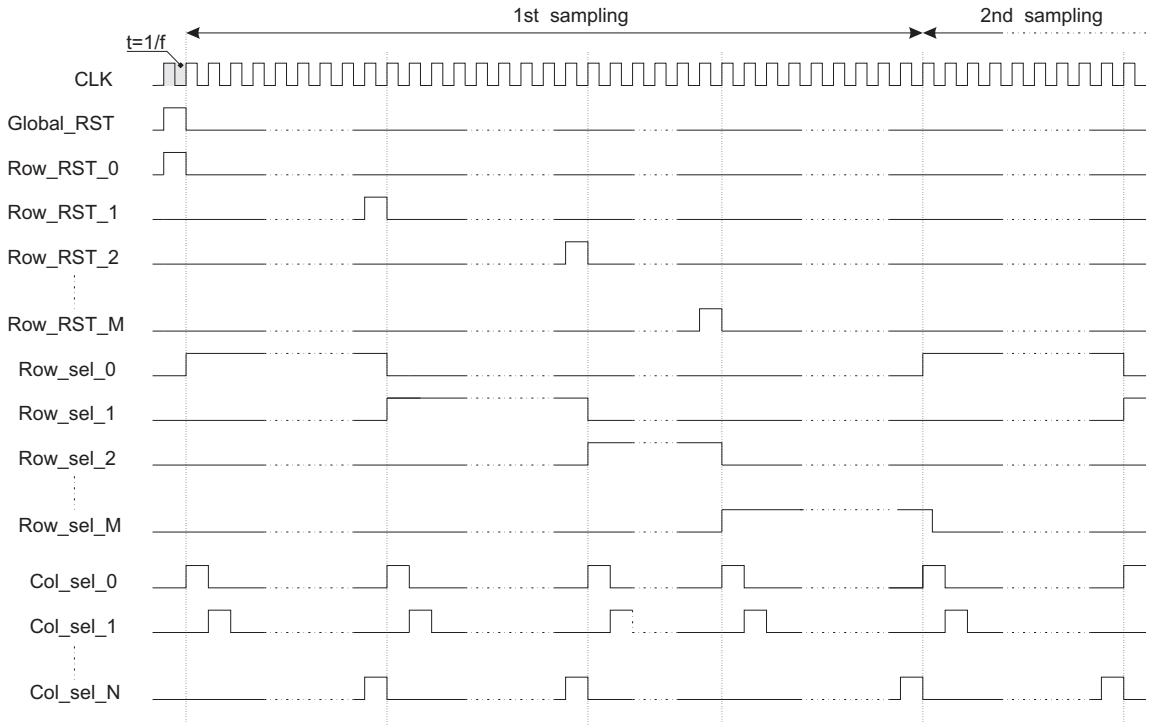
$$t_{integration} = N_{px} \cdot \frac{n}{f} \tag{4.17}$$

where N_{px} is the number of pixels in the array, f is the external clock frequency, and n is the number of clock cycles needed to read out a single pixel (typically n=1).

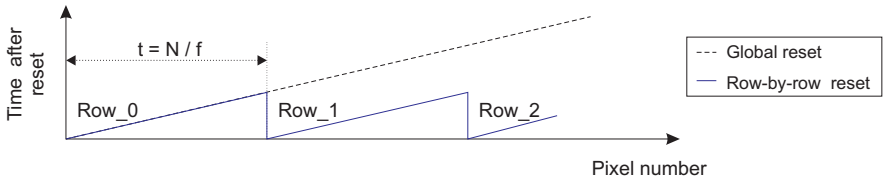
In the case of the 3T pixel architecture, two different modes of resetting the pixels can be applied. They are illustrated in Figure 4.7(c). The first one is called "row-by-row reset". In this mode, the row of pixels is selected by the "row select" register and the reset signal is delivered to all the pixels belonging to the selected row. Then, the pixels are addressed individually by means of the "column select" register, and the signal values from these pixels are read out one by one. After that, the next row is selected and the same cycle is repeated until the whole matrix is read out. During the first read out, the reference values of the individual pixels are recorded.



(a) Simplified sensor architecture.



(b) Readout scheme.



(c) Time after reset as a function of the pixel index.

Figure 4.7: CMOS pixel sensor: concept of the sequential readout.

After that, the second read out of the full matrix occurs without resetting the sensing diodes.

The second reset mode is called a "global reset". Here, the reset signal is delivered to the full array of pixels simultaneously. After the global reset, the matrix is read out twice and the cycle is repeated.

Both reset modes have their advantages and disadvantages. The global reset mode is easier to implement but it introduces significant non-uniformities between the pixels read out at first and those read out at last. Indeed, even if the time between two consecutive accesses to the same pixel is constant, the first pixel is read out just after the reset while the last is read out after the time t_{GR} from the reset:

$$t_{GR} = M \cdot N \cdot \frac{n}{f} \tag{4.18}$$

where M is the number of rows and N is the number of columns, f is a readout clock frequency and n is the number of readout clocks needed to read out a single pixel.

As a consequence, the pixels from the beginning of the matrix and these from its end are read out in different conditions. The row-by-row reset is more complicated to implement but it ensures a more uniform distribution of the time slot between the reset and the readout. In this case, the first pixel of each row is read out just after the sensing diode reset. Instead, the last pixel from each row is accessed after the time t_{RBR} from the row reset:

$$t_{RBR} = N \cdot \frac{n}{f} \tag{4.19}$$

where N is the number of pixels in a row, f is a readout clock frequency and n is the number of readout clocks needed to read out a single pixel.

In the case of SB architectures, all the complications related to the periodical reset of the diode voltage do not exist. The pixel array is read out periodically and two consecutive samples are taken for the CDS.

In some cases, the output amplifier A presented in Figure 4.7(a) is build-in the chip and shared by all the pixels. The purpose of this device is to amplify a signal in the early stage of the data processing. This results in a better separation of the signal from the noise.

4.2.2.2 Measurement setup

The typical readout chain for studying the MAPS consists of: a motherboard, auxiliary board and data-acquisition board connected to a computer. Such a readout chain is sketched in Figure 4.8, and is described in detail in [115].

The motherboard has several functionalities. It provides a mechanical support for the Device Under Test (DUT) that is glued to the surface of the motherboard and then wire-bonded to dedicated pads. The motherboard also provides the power supply for the DUT,

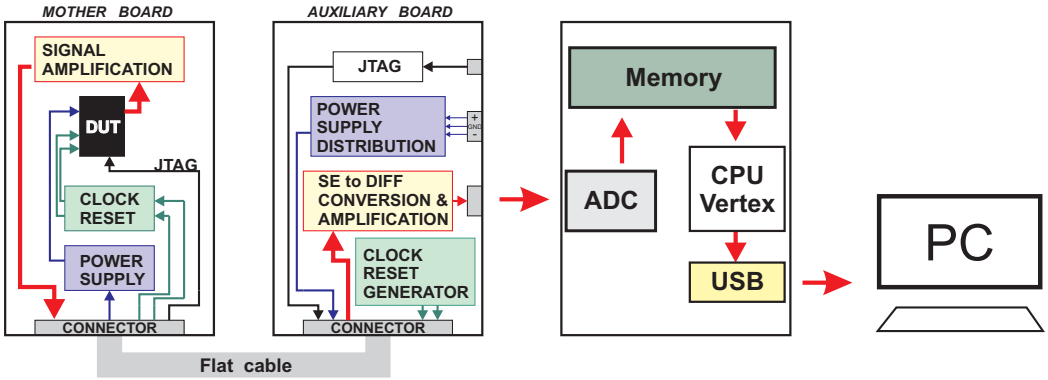


Figure 4.8: A typical setup configuration used for studying the CMOS-sensor performance. The motherboard provides a mechanical support for the device under test, a power supply, a signal amplification, and a slow-control signals. The auxiliary board distributes the power-supply signals and steering signals, and provides further signal amplification and conversion. The data-acquisition board provides the analog to digital conversion and performs data transfer to the PC.

and transmits the steering signals (clock, reset, JTAG[5]) from the auxiliary board and houses a signal amplification.

The auxiliary board generates the clock and the reset signals. If required, it allows transmitting these signals from the outside world, for example, from a pattern generator. It also provides the stabilized voltage that after filtration on the motherboard, is applied to the DUT.

The signal from the DUT that is pre-amplified on the motherboard is further amplified on the auxiliary board. Besides amplification, the signal is converted from single ended to differential. As the distance from the auxiliary board to the data-acquisition board is usually long (from 1m up to several tens of meters), a differential transmission of the signal is required to minimize the signal degradation. The differential transmission occurs via coaxial cables identical to those used for Ethernet networks.

The data-acquisition board is equipped with an Analog to Digital Converter (ADC) co-operating with an FPGA[6] device (internal CPU) and memory banks. The analog signals from auxiliary board are converted into digital representation and kept in the on-board memory. The memory content is then sent to the PC via a USB port.

In order to ensure a proper separation between analog and digital power supplies and between analog and digital signals, a multi-layer PCB is used for both motherboard and auxiliary board.

[5]JTAG - is a communication protocol defined by the IEEE-1149.1 standard. In the CMOS sensors, JTAG is used to program the internal registers responsible for sensor operations. This extends the sensor testability.
[6]FPGA stands for Field Programmable Gate Array.

4.2.2.3 The dark chamber

Because the CMOS sensors are light-sensitive, the accurate assessment of their parameters has to be performed in the darkness. The motherboards are therefore placed inside a specially prepared box called the "dark chamber".

Besides light protection, the dark chamber has other important functionalities. Because the chamber is made of metal, it acts as a Faraday cage. There is a copper or an aluminum plate mounted inside the dark chamber. This plate has two functions: it ensures a mechanical support for the motherboard and provides cooling. The heat transfer between the cooling plate and the motherboard is realized via a special heat-conductive material which also ensures the electrical insulation between both elements. The dark chamber was connected to a cooling system capable of controlling the DUT temperature in the range of -20 °C to +40 °C with a precision of about ± 1 °C.

The temperature of the DUT was measured by a platinum resistance thermometer (PT-100) located on the opposite side of the motherboard, just in front of the DUT. The temperature difference between the sensor and the PT-100 was estimated using MAPS with an integrated temperature sensor. For temperatures above 0 °C, the temperature measured by the PT-100 had an offset of +1 °C with respect to the one measured on the DUT. An offset of approximately $+2$ °C was observed for lower temperatures.

Since the MAPS with the integrated temperature sensor used here for calibration were featuring relatively high power consumption, the temperature differences between the sensor and the PT-100 probe were observed. This difference should be marginal in the case of sensors with low power consumption. Overall, the calibration of the PT-100 readings allowed to measure the sensors at stable and well controlled temperature.

Although not stated explicitly, the temperature values given in this document stand for the sensor temperatures.

4.2.2.4 System automation

Studying the performance of CMOS sensors requires very often a complex set of measurements that is repeated for all the tested devices. For example, in order to assess the radiation tolerance of an investigated CMOS process, several sensor samples are used. Each of them needs to be characterized at several different temperatures (e.g., -10 °C, 0 °C, +10 °C, +20 °C, +40 °C) and with several different integration times (about seven values). To assess precisely the sensor performance, the characterization has to be carried out with and without a radioactive source, for example, an $^{55}\mathrm{Fe}$ source.

The standard system available in the laboratory (described in [115]) required frequent interactions with the operator. All the settings regarding the clock frequency applied to the DUT, temperature control, sensor exposition to the radioactive source, had to be done manually. The amount of tests addressed within the scope of this PhD studies prompted the

automation of some of the tasks.

The automation of the measurements covered: the automatic control and stabilization of the sensor temperature, the clock frequency settings, and the sensor exposition to an $^{55}\mathrm{Fe}$ source. Finally, the operator was needed only in order to change the sensors inside the dark chamber and to start the automatic measurement procedure.

4.2.3 Observables measured in the laboratory conditions

The observables addressed in this thesis can be divided in two groups. The first group contains the parameters measured in the laboratory: temporal noise and FPN, charge collection efficiency (CCE), leakage current and pixel parasitic capacitance C_{px}. The laboratory tests are usually not time restricted. They allow for precise and extensive studies of sensor behavior in different running conditions, for example, in terms of temperature or integration time.

The second group of parameters is used to describe the sensor response to MIP expected in real experimental conditions. Tests with these particles have to be carried out using a high-energy particle beam, for example, the pion beam from the CERN-SPS. The access to a high-energy beam is strongly time restricted and extensive studies cannot usually be performed. The parameters describing the sensor performance measured with MIP are discussed in Section 4.2.4.

In order to achieve reliable measurements, a sensor calibration with a well known radioactive source has to be done. In this thesis work an $^{55}\mathrm{Fe}$ source was used. The calibration procedure is described in the following section.

4.2.3.1 Sensor calibration with an $^{55}\mathrm{Fe}$ source

The analog information from the sensor is converted during the read out into a digital sample by the means of the ADC discussed in Section 4.2.2.2. The signal generated by impinging particles, the equivalent noise charge, or the leakage current are expressed in unit of electrons. In order to find the conversion factor between the ADC units and number of electrons, a calibration procedure is needed. This procedure allows comparing results between sensors featuring different gains of the readout chain. The calibration is usually performed with a radioactive isotope that has a well-known spectrum. The commonly used source is an $^{55}\mathrm{Fe}$, emitting X-Rays with the following energies: $K_\alpha = 5.9keV$ and $K_\beta = 6.49keV$ [5]. The K_α peak corresponds to 24.4% of the $^{55}\mathrm{Fe}$ decays while K_β to 2.86% only.

The $^{55}\mathrm{Fe}$-photon interaction with a silicon material leads to the creation of e-h pairs. These interactions are point-like and generate e-h pairs in a limited distance ($\sim$1 µm) from the interaction point. Therefore, one can distinguish several peaks in the typical $^{55}\mathrm{Fe}$ spectrum illustrated in Figure 4.9. This spectrum was observed for the seed pixel: the one containing the highest charge in the pixel cluster. The origin of the peaks visible in the spectrum is explained hereafter:

- The left most peak is due to the electronic noise.
- The signal electrons generated in the EPI layer are thermally distributed in all directions. As a consequence of the electron reflection from the p-/p++ junction between bulk and EPI layer, the electrons cannot escape from the EPI layer. Due to the charge spread, several diodes collect the available charges. The middle peak, located at approximately 70 ADC counts, corresponds to the signal charge originating from the EPI layer and observed for the seed pixel. It is called "signal peak".
- The two peaks located next to each other on the right side correspond to the signal generated inside the small depleted volume underneath the sensing diode. In this case, the whole generated charge is collected by the sensing diode and transferred to the output. The most populated peak among those two corresponds to the 5.9 keV photons of the ^{55}Fe source and it is called the "calibration peak". This peak is used to convert the ADC units into electrons.

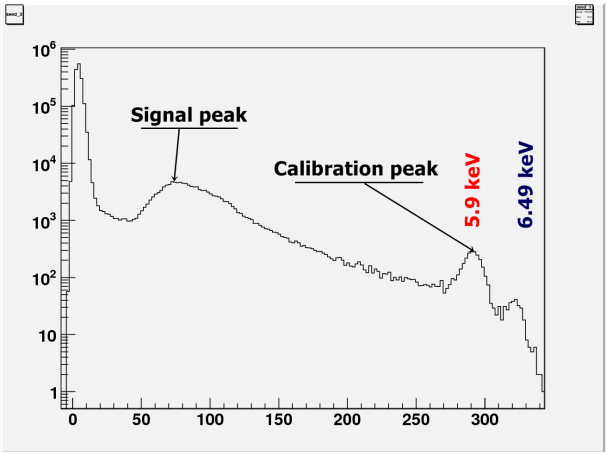


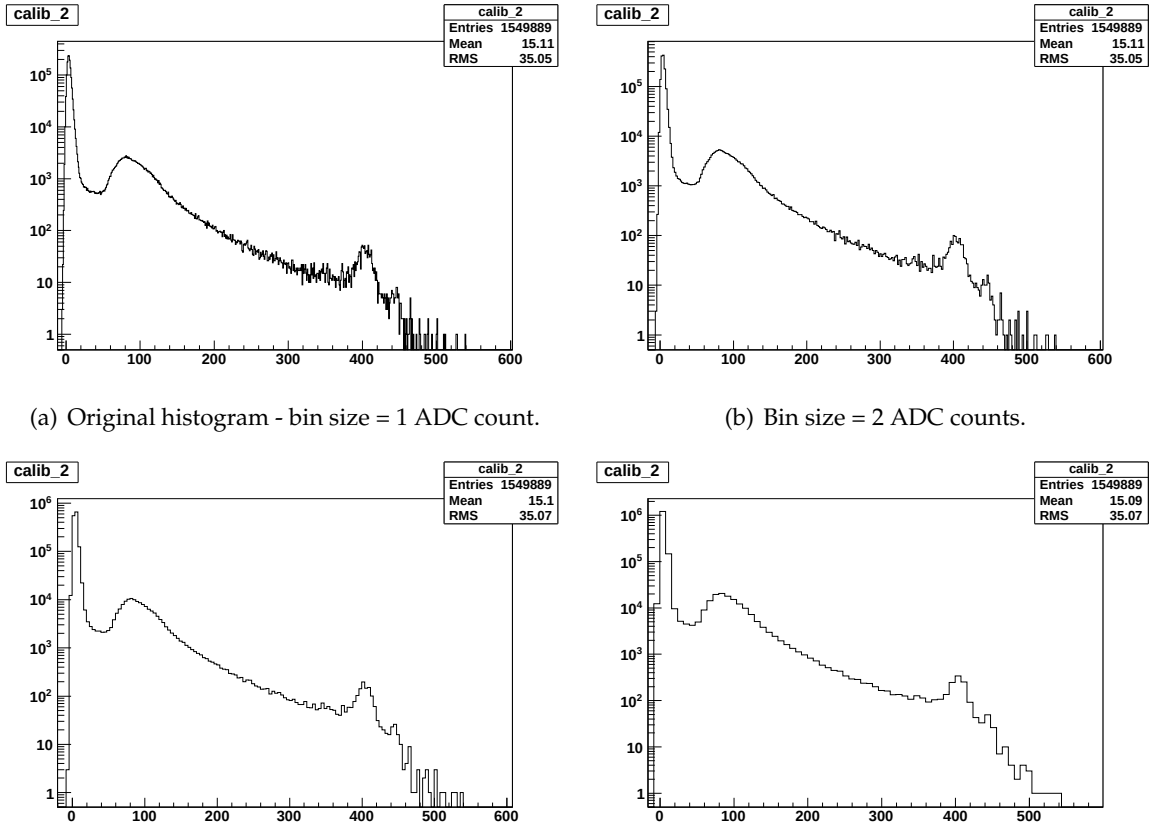
Figure 4.9:
A typical ^{55}Fe spectrum observed with a CMOS pixel sensor.
Signal peak: originates from an ^{55}Fe photon interactions occurring inside the EPI layer. In this example this peak is located at about 70 ADC counts.
Calibration peak: originates form an ^{55}Fe K_α photon interactions occurring inside the small depleted volume underneath the sensing diode where the whole generated charge is collected by the sensing diode. The calibration peak (here around 290 ADC units) is used to convert the ADC units into electrons.

In general, the signal electrons generated inside the detector bulk or highly p-doped-silicon regions recombine and do not contribute to the signal. There may be exceptions, for example, when a high-energy γ ray is produced in this domain and penetrates the EPI layer. The contribution of such cases to the signal charge is marginal.

The calibration procedure is accomplished by comparing the calibration-peak position [ADC units] with the associated electron charge [e^-]. The latter is well defined and corresponds to the charge collected in the depleted region under the sensing diode. As an energy of 3.6 eV is needed to generate an e-h pair in silicon, the 5.9 keV photons from the ^{55}Fe source will then generate approximately 1640 e-h pairs. The calibration peak then corresponds to $\sim$1640 e^-. Assuming a linear response of the readout chain, the output signal expressed in ADC units

can be translated into electrons. In the case of the histogram from Figure 4.9, the 5.9 keV peak corresponds to ∼290 ADC counts. The ratio between the charge associated with the calibration peak and its corresponding value in ADC units will be referred as the calibration factor (f_{calib}).

For the purpose of the measurements presented in this document, a precision for the calibration peak position on the order of a few percent is sufficient. For example, one of the most frequently measured parameter is the electronic noise, usually in the range of 10 e^- before sensor irradiation. Thus, a precision of 0.5 e^- ($\sim 5\%$) is sufficient to compare two noise values.



(a) Original histogram - bin size = 1 ADC count.

(b) Bin size = 2 ADC counts.

(c) Bin size = 4 ADC counts.

(d) Bin size = 8 ADC counts.

Figure 4.10: Example of a re-binning of histograms. The bin size is varied from 1 ADC/bin (see panel a) to 8 ADC/bin (see panel d). In the original (not re-binned) histogram, 1 ADC unit corresponds to one bin. During the re-binning process, the content of two or more neighboring bins is merged. The value of the new histogram bin is a sum of those bins. A single bin of the newly created histogram corresponds to 2 (figure b),4 (figure c),8 (figure d),16... ADC units.

Several methods featuring such a precision can be applied to find the position of the calibration peak [4]. In this work, the one based on changing the histogram binning (re-binning) is proposed. The use of this method is motivated by the fact that it substantially

reduces the time needed for the analysis of a large number of histograms, still keeping a satisfactory precision of $\leqslant 1\%$. In the example shown in Figure 4.10, 1 ADC unit corresponds to one bin (see Figure 4.10(a)) for the original (not re-binned) histogram. Then, the histogram is re-binned. In this procedure, the two consecutive histogram bins are merged. The value of the new histogram bin is a sum of two consecutive histogram bins, and then every bin of the newly created histogram corresponds to 2 ADC units (see Figure 4.10(b)). The histogram is still chopped and one cannot precisely identify the calibration peak. Another change of the histogram bin size is performed. Now, one bin corresponds to 4 ADC units of the original histogram (see Figure 4.10(c)). The re-binning procedure is continued until the maximum of the calibration peak can be defined without any ambiguity. In the next steps, the histogram bin corresponds to 8, 16,... ADC units. Finally, the histogram features a smooth shape in the region of interest and the calibration peak position can be found (see Figure 4.10(d)). In the example illustrated in Figure 4.10, the peak position was identified for the bin size corresponding to 8 ADC counts. The uncertainty of such calibration peak estimation is governed by the bin size according to the following equation:

$$\sigma_{fit} = \frac{\frac{binH}{\sqrt{12}}}{CP_{max}} \cdot 100\% \tag{4.20}$$

where CP_{max} is the peak position (MPV) given by the fit, and $binH$ is the histogram bin size which allows identifying the maximum of the calibration peak.

In the example discussed here, the calibration peak position was estimated to be at 400 ADC counts. The bin size of 8 ADC counts used for this estimation translates into the uncertainty of the calibration peak position below 1% that is sufficient for the purpose of this thesis work.

4.2.3.2 Charge Collection Efficiency

The Charge Collection Efficiency (CCE) is the ratio between the charge collected by the sensing diode (or diodes) and the total charge generated by an impinging particle. For the purpose of this work, the CCE was measured with the $^{55}\mathrm{Fe}$ source. The CCE is calculated directly from the histogram, presented for example in Figure 4.9, as the ratio between the signal and calibration peak. The CCE reflects roughly the sensor bulk properties that may vary due to a different EPI-layer thickness (different charge spread), diode size and geometry or radiation level.

4.2.3.3 Pixel capacitance measurements

The charge generated by an impinging particle is converted on the pixel capacitance into voltage. Then it is amplified and sampled by the ADC unit. The pixel capacitance C_{px} is mainly composed of the sensing-diode and reset-transistor parasitic capacitances. This capacitance determines the amplitude of the diode output voltage signal according to the

following equation:

$$V_{signal} = \frac{Q_{signal}}{C_{px}} \tag{4.21}$$

where Q_{signal} is the charge stored on the sensing diode. A small value of the C_{px} is mandatory to achieve a reasonable signal amplitude.

In order to estimate C_{px}, the gain of the readout chain has to be measured. This gain is defined as the ratio:

$$RO_{gain} = \frac{\Delta Vdiode}{\Delta ADC} \tag{4.22}$$

where ΔADC is the ADC channel variations induced by a sensing-diode-voltage variation (ΔVdiode).

For example, in the 3T pixel architecture (presented in Figure 4.2) the RO_{gain} is measured as follows. The reset transistor is permanently closed and the diode voltage is set directly by the $Vdiode$ voltage. The latter is next regulated in some range, usually from 0V up to 3.3V for 0.35 µm processes. The corresponding variation of the diode output voltage is read out and recorded in ADC units. Figure 4.11 presents an example result of readout channel gain measurements. The RO_{gain} is found as the slope of the curve ADC=f(Vdiode).

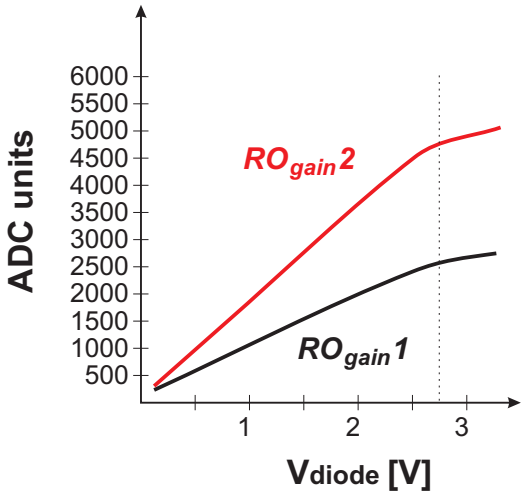


Figure 4.11:
Example results of the readout channel gain measurements. Red line corresponds to the channel with the higher gain. The channel with the smaller gain is indicated by the black curve.

In order to estimate the pixel capacitance, the following equation is used:

$$C_{px} = \frac{Q \cdot q}{V} \tag{4.23}$$

where Q is the collected charge in electrons, V is the corresponding voltage, and q is the electron charge. The value of the collected charge Q in the sensing diode is obtained from the calibration peak (1640 e^-). The voltage V can be derived from the following equation:

$$V = RO_{gain} \cdot ADC_{5.9keV} \tag{4.24}$$

where $ADC_{5.9keV}$ is the calibration peak value expressed in ADC channels. Then,

$$C_{px} = \frac{Q \cdot q}{RO_{gain} \cdot ADC_{5.9keV}} \tag{4.25}$$

The above described method for indirect parasitic-pixel-capacitance measurements gives the precision of ≤ 1 fF, which is sufficient for the CMOS sensor characterization addressed in this thesis work.

4.2.3.4 Leakage current and noise calculations

Measurements of the leakage current are possible for pixels with the 3T architecture described at the beginning of this chapter. For this purpose, a sensor composed of P pixels is read out N times. During each read out, the two samples required for the CDS operation are recorded.

After CDS (see Section 4.2.1), the charge integrated on the sensing diode capacitance is given by the equation similar to Equation 4.13:

$$Q^{px}_{pixel}(n) = Q^{px}_{noise}(n) + Q^{px}_{leakage}(n) \tag{4.26}$$

The index px corresponds to the pixel serial number that ranges from 1 to P. The index n corresponds to the number of the read out varying from 1 to N.

In order to calculate the average leakage current and temporal noise over the pixel matrix, the operation illustrated in Figure 4.12 is performed. The distribution composed of N samples of Q_{pixel} is plotted for each pixel. Figures 4.12(a)(b)(c) represent the distribution for pixel 1, pixel 2 and pixel P, respectively. The $\overline{Q}^{px}_{pixel}$ is the mean charge due to the leakage current integrated over the integration time while σ^{px}_{pixel} is its standard deviation, which gives the information about the temporal noise associated with the given pixel.

The leakage current and noise are the properties of an individual pixel. Since a real sensor is composed of thousands of individual pixels, it is more useful to measure the mean value of the leakage current distribution over the pixel matrix. In addition, the dispersion of the leakage current around the mean value is also convenient information to characterize non-uniformities over the pixel matrix. In order to calculate the mean value of the leakage current over the matrix, the mean values of $\overline{Q}^{px}_{pixel}$ for P pixels are stored in a separate histogram shown in Figure 4.12(d). The mean value of the distribution is used to calculate the average charge due to the leakage current according to the following equation:

$$\overline{I}_{leakage} = \frac{\bar{Q}_{leakage}[e^-] \cdot q}{t_{integration}} = f_{calib} \cdot \frac{\bar{Q}_{leakage}[ADCunits] \cdot q}{t_{integration}} \tag{4.27}$$

where f_{calib} is the calibration factor presented in Section 4.2.3.1, $t_{integration}$ is the integration time, q is the electron charge and $\bar{Q}_{leakage}[ADCunits]$ is the mean leakage current charge

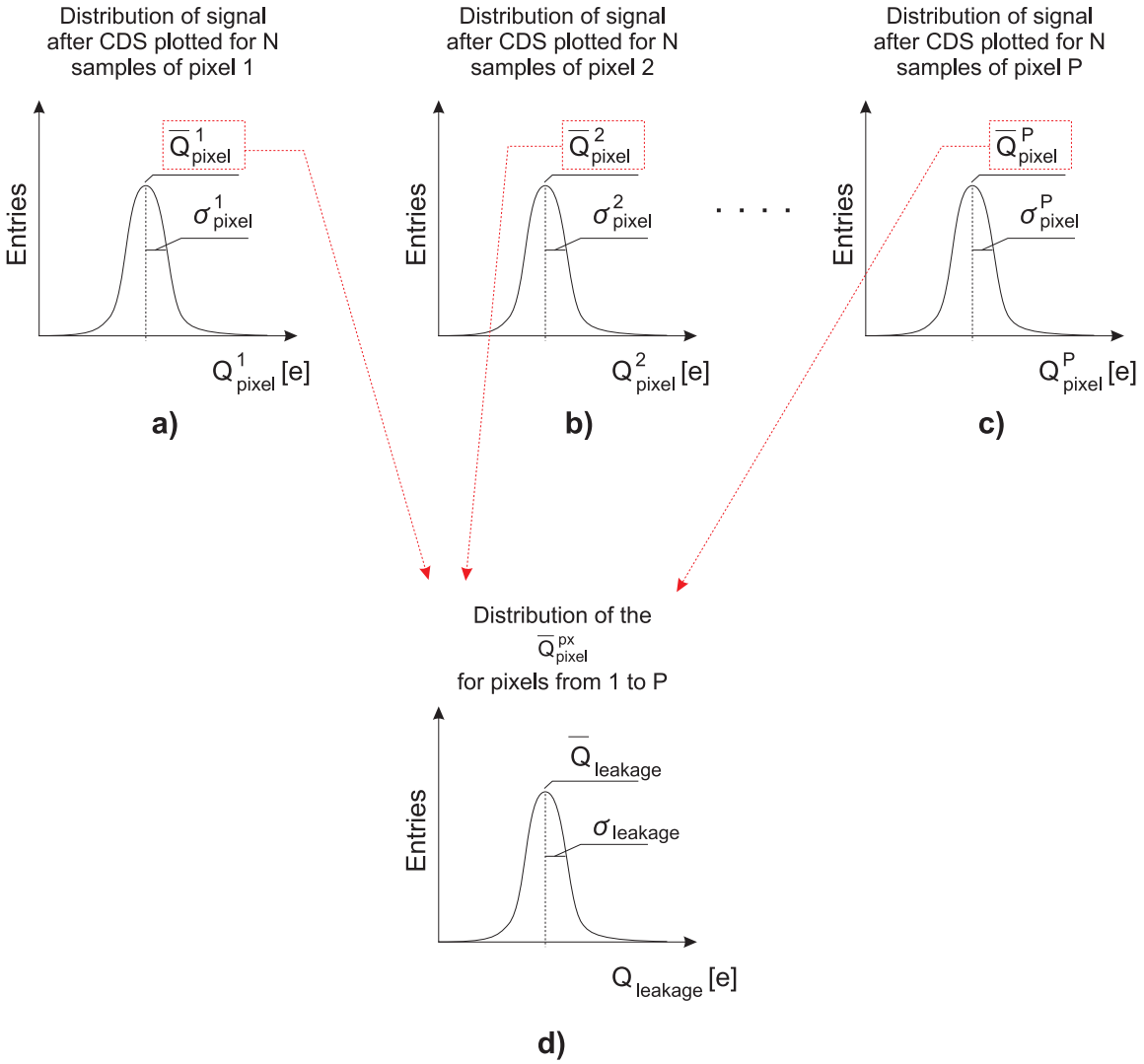


Figure 4.12: Calculations of the average leakage current. N samples of charge corresponding to P pixel leakage currents are stored in histograms for pixel 1 (figure a), 2 (figure b) and P (figure c). Next, the charge mean value corresponding to the leakage current of the individual pixels is stored in the output histogram (d). This histogram gives the information about the mean value of the charge corresponding to the leakage current over the full matrix $\overline{Q}_{leakage}$ and its standard deviation $\sigma_{leakage}$.

expressed in ADC units.

Both the mean value [7] and standard deviation of the distribution are used in this document for a graphical representation of the results. The points displayed in the graphs correspond to

[7] The uncertainties on the mean value of the leakage current stand for the standard deviation of their distributions divided by $\sqrt{P}$, where P stands for the number of investigated pixels.

the mean value of the leakage current distribution. The error bars shown in the graphs carry the information about the standard deviation of the leakage-current distribution. The uncertainties on the mean value of the leakage current are not given in the plots. They usually do not exceed a few percent of the measured value.

Actually, $Q^{px}_{noise}(n)$ is composed of a common mode noise (CMN) component $Q^{px}_{cmn}(n)$ and temporal noise component $Q^{px}_{temporal}(n)$. Thus, $Q^{px}_{pixel}(n)$ can be written now as follows:

$$Q^{px}_{pixel}(n) = Q^{px}_{temporal}(n) + Q^{px}_{cmn}(n) + Q^{px}_{leakage}(n) \tag{4.28}$$

The common mode noise (CMN) is observed as a simultaneous change of many adjacent pixel outputs and it originates from a pick-up noise. This type of noise contains all the contributions that are not correlated in time but instead the correlation exists between the pixels. It is postulated that the mean value of the CMN over the time is zero.

In order to calculate the mean temporal noise over the matrix, the CMN must be rejected first. The CMN does not affect the mean value of the pixel leakage current (which is by definition constant for a given pixel), thus:

$$Q^{px}_{leakage}(n) = \overline{Q}^{px}_{leakage} \tag{4.29}$$

and Equation 4.28 can be rewritten as:

$$Q^{px}_{temporal}(n) + Q^{px}_{cmn}(n) = Q^{px}_{pixel}(n) - \overline{Q}^{px}_{leakage} \tag{4.30}$$

In order to insulate the common mode, one has to calculate the mean value over the pixels:

$$\frac{1}{P}\sum_{n=1}^{P} Q^{px}_{temporal}(n) + \frac{1}{P}\sum_{n=1}^{P} Q^{px}_{cmn}(n) = \frac{1}{P}\sum_{n=1}^{P}(Q^{px}_{pixel}(n) - \overline{Q}^{px}_{leakage}) \tag{4.31}$$

Since:

$$\frac{1}{P}\sum_{n=1}^{P} Q^{px}_{temporal}(n) = 0 \tag{4.32}$$

the CMN can be expressed as:

$$\overline{Q}_{cmn}(n) = \frac{1}{P}\sum_{n=1}^{P}(Q^{px}_{pixel}(n) - \overline{Q}^{px}_{leakage}) \tag{4.33}$$

Thus:

$$Q^{px}_{pixel}(n) = Q^{px}_{temporal}(n) + \overline{Q}_{cmn}(n) + \overline{Q}^{px}_{leakage} \tag{4.34}$$

Examples of distributions $Q^{px}_{pixel}(n)$ composed of N samples for the pixels 1,2 and P are shown in Figure 4.13.

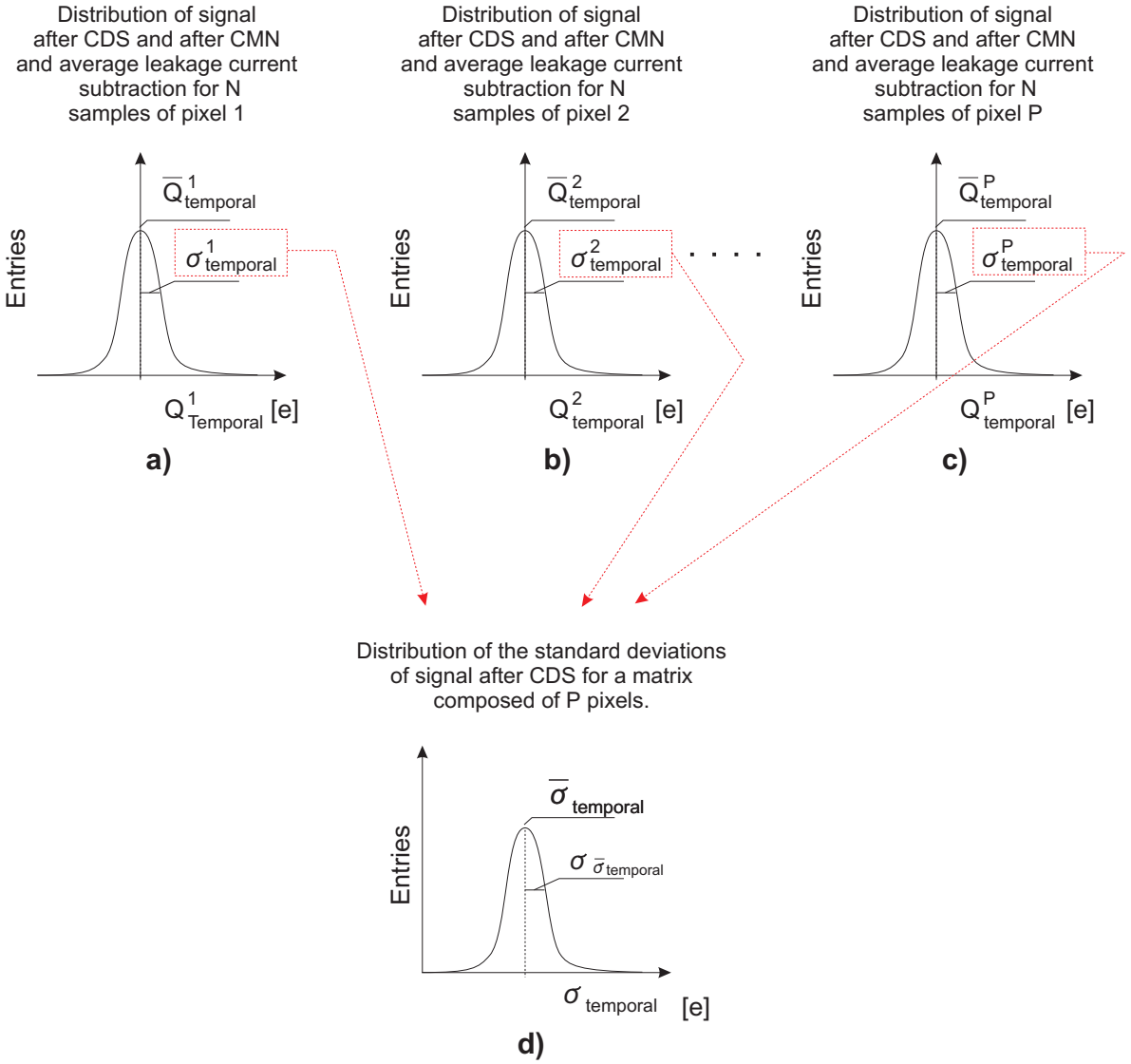


Figure 4.13: Calculations of the temporal noise. The distributions of CDS-signal after CMN and average leakage current rejection are stored in P histograms. The histograms for pixel 1, 2 and P are shown in figure (a), (b), and (c), respectively. Next, the standard deviation of each distribution is collected in the output histogram (figure d). The mean value of the output histogram corresponds to the temporal noise $\overline{\sigma}_{temporal}$ and the standard deviation indicates the dispersion of the noise of the individual pixels.

The standard deviation of each distribution stands for the temporal noise of a given pixel. In order to calculate the mean value of temporal noise over the whole matrix, the standard deviations of $Q^{px}_{pixel}(n)$ distributions for all the P pixels are stored in a separate histogram shown in Figure 4.13(d). The mean value of this distribution corresponds to the mean temporal noise

according to the equation:

$$\overline{noise}_{mean} = \overline{\sigma}_{temporal} \cdot f_{calib} \tag{4.35}$$

In order to illustrate the noise in figures, the same convention as for the leakage current presentation is used. The uncertainties on the mean value of the electronic noise are not given in the plots. They do not exceed a few percent of the measured value.

4.2.4 Observables measured with Minimum Ionizing Particles

This section will introduce the second group of observables which require dedicated tests with a high-energy pion beam.

The MAPS detect the passage of particles in high-energy physics experiments. The particles of interest usually feature an energy that is high enough to treat them as a MIP. It is then useful to study the response of sensors to this type of particles. Such studies are performed to evaluate sensor characteristics regarding: signal collection, ϵ_{det}, σ_{res} or FH_{rate}.

4.2.4.1 Detection efficiency – ϵ_{det}

The ϵ_{det} is studied with the beam telescope presented already in Section 1.2. The ϵ_{det} is the ratio between the number of particles detected with the DUT and the number of tracks reconstructed with the beam telescope.

The ϵ_{det} is governed by the SNR. For pixels featuring a small SNR, the signals generated by a MIP cannot be distinguished from the noise. Such pixels become blind to particles and contribute to the degradation of the ϵ_{det}. In the case of a sensor before irradiation, the SNR is usually high enough to ensure the ϵ_{det} close to 100%. After irradiation, the signal degradation and the noise rise lead to the decrease in the SNR. Therefore, the ϵ_{det} is studied as a function of non-ionizing and ionizing radiation. In this studies, the ambitioned ϵ_{det} value was $\geqslant 99\%$. This value was set as a threshold below which the sensors were treated as not operational. This requirement is quite drastic and in most of the cases the ϵ_{det} of 98-99$\%$ is satisfactory.

4.2.4.2 Spatial resolution – σ_{res}

The σ_{res} is strongly governed by the pixel pitch and the charge sharing inside the sensitive volume. If one does not account for any charge sharing (binary resolution), the resolution defined by the pixel pitch can be given by the following equation:

$$\sigma_{res} = \frac{pixelpitch}{\sqrt{12}} \tag{4.36}$$

Thus, a sensor featuring a pixel pitch of 20 µm provides in the worst case a σ_{res} of ∼5.8 µm. Since the charge sharing exists in CMOS sensors, the algorithms calculating the σ_{res} take into

account this phenomenon. Finally, the place where a particle crosses a sensor is identified with a better precision.

4.2.4.3 The average fake hit rate – FH_{rate}

The FH_{rate} is defined as the average number of fake hits per pixel per readout. A fake hit is caused by an excessive pixel noise being at the signal level, and therefore treated as a signal originating from an impinging particle.

Since the tracking algorithms cannot distinguish between true and fake hits, the latter are at the origin of ambiguities during the extrapolation of particle tracks.

It is important to limit the number of fake hits produced by the pixel sensors but there is no hard limit related to the acceptable FH_{rate} that is simultaneously valid for all CMOS-sensor applications (discussed in Chapter 1 of this document). The number of fake hits that can still be accepted by the tracking algorithms depends on how precisely the algorithm can define the region of interest where it looks for hit candidates on the pixel sensor stations[8]. For example, in the case of the STAR experiment, a FH_{rate} of 10^{-4} is an acceptable limit. For the CBM experiment this quantity is unknown so far. The threshold value corresponding to the STAR experiment will be used in this thesis to judge the sensor performance.

4.2.4.4 Adequacy of a $^{106}\mathrm{Ru}$ source for the sensor characterization

The tests with a high-energy particle beam reflect the interactions ongoing between a sensor and particles in real high-energy physics experiments. Since the access to the beam lines for test purposes is very restricted, there was a strong interest in particle sources that allow assessing some of the most important CMOS-sensor parameters in the laboratory conditions. For this reason the adequacy of a $^{106}\mathrm{Ru}$ source was investigated.

The Ruthenium 106 ($^{106}\mathrm{Ru}$) is the radioactive isotope of the naturally occurring Ruthenium. The $^{106}\mathrm{Ru}$ decays to ^{106}Rh and then, by 5 different beta emission, to Pd^{106}, which is stable. During this decay, electrons with an energy spectrum shown in Figure 4.14 [116] are emitted. The energy range of the $^{106}\mathrm{Ru}$ electrons corresponds to the minimum energy loss per unit of path length and therefore they can be treated as MIP.

In the case of tests with a $^{106}\mathrm{Ru}$ source, the charge collected by a sensor was 10-20$\%$ larger than the one observed during tests with high-energy pion beam. Table 4.1 compares the charge collected[9] in a single pixel during tests with a $^{106}\mathrm{Ru}$ source and high-energy pion beam. During tests with a high-energy particle beam usually $\sim$120 GeV pions are used. For a thin silicon sensor, the average energy loss per unit of path length reaches a plateau at a pion kinetic energy of a few GeV. Therefore, 120 GeV pions impinging a silicon detector lose approximately the

[8] A larger number of fake hits is acceptable in the case where the algorithm looks for hits in a more precise region of interest.

[9] The table contains the charge collected with different pixels of the MIMOSA-25 sensor prototype based on a high-resistivity EPI layer. This sensor and its radiation-tolerance assessment will be presented in Section 6.2.

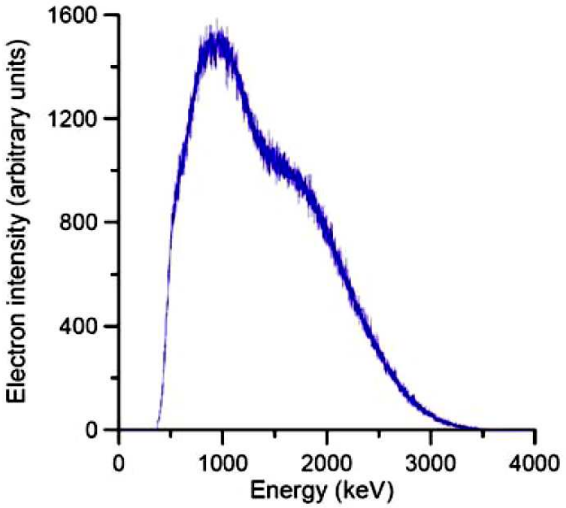


Figure 4.14:
Spectrum of the electrons emitted by a ^{106}Ru source [116].

same energy per unit of path length. For a ^{106}Ru electrons entering the silicon detector, the average energy loss per unit of path length is close to a MIP ($\beta\gamma$ =3.5). The dE/dx for ^{106}Ru electrons rises rapidly when they are crossing the sensor material. Consequently, the ^{106}Ru electrons lose more energy traversing through the same silicon sensor than the high-energy pions. This higher energy loss is converted into a larger amount of electron-hole pairs created, thus to a larger signal.

A ^{106}Ru seems to be a proper particle source for a rough assessment of the charge collection properties of sensors, for example, SNR calculations. However, due to a larger multiple scattering, the ^{106}Ru source cannot be used for ϵ_{det} or σ_{res} measurements.

Table 4.1: Most probable signal charge in the seed pixels of hit clusters generated by beta rays from a Ru-106 source and by 120-GeV/c pions. The results are expressed in units of electrons and shown as function of pixel type and radiation dose. (Results observed for the MIMOSA-25 prototype studied in Section 6.2.)

MIMOSA-25 diode	non-irradiated	$1.3{\cdot}10^{13}$ n_{eq}/cm^2	$3{\cdot}10^{13}$ n_{eq}/cm^2
Ruthenium source			
$3T_{4\times4}$	548 ± 8	453 ± 5	429 ± 5
$SB_{5\times6.5}$	671 ± 7	572 ± 5	548 ± 6
$3T_{5\times6.5}$	675 ± 7	586 ± 6	547 ± 7
120 GeV/c pions			
$3T_{4\times4}$	462 ± 5	391 ± 26	331 ± 10
$SB_{5\times6.5}$	588 ± 2	428.2 ± 8	402 ± 3
$3T_{5\times6.5}$	623 ± 4	475 ± 18	430 ± 6

4.2.5 Sensor irradiation facilities used for this work

The particle detectors used for tracking in high-energy physics experiments may be mounted very close to the interaction points where they are exposed to a significant amount of particles. Depending on the particle type and energy, some of the particles crossing the detector volume create ionizing effects in the oxide layers. Some others induce non-ionizing defects in silicon lattices. Some particles, for example charged pions, generate both ionizing and non-ionizing effects in the detector material. At the stage of laboratory tests, it is important to assess the sensor performance in conditions as close as possible to those expected in a real experiment. This can be done by irradiation of samples with X-Rays and neutrons, responsible for ionizing and non-ionizing damages in silicon detectors respectively. In order to study independently the effects induced by ionizing and non-ionizing radiation, MAPS being within the scope of this thesis were exposed separately to both types of radiation. The necessary information related to X-Rays and neutron sources used in this work are given hereafter.

4.2.5.1 Ionizing radiation source used in this work

Since many years people have been studying the influence of ionizing radiation on different materials and tissues, see for instance [117, 118, 119, 120]. One of the key issues for such studies is to deliver experimentally the same dose as the one expected to be accumulated by the tested object in its running conditions. The studies on the radiation hardness of the space craft electronics, which is supposed to survive on Earth orbits for several years, is an illustrative example. During such studies, an expected dose is delivered to the samples in laboratory conditions within a shorter time (usually several hours) than the one needed for the accumulation of the same dose in the real operation environment. This motivated the development of irradiation tools capable of providing the expected ionizing doses within a short time. One of them is the X-Ray wafer probe "Seifert Rp149", described in [121, 122, 123]. Such a device was also used for the irradiation of the sensors studied in this thesis. The main features of the "Seifert Rp149" are:

- Two tubes available, with Tungsten (peak energy at 10 keV) and Molybdenum (peak energy at 19 keV) targets.
- Precision of the delivered dose within 20 $\%$ [124].
- Beryllium window to seal the tube, with a thickness of 0.25 mm.
- Aluminum filter - with a thickness of 0.15 mm.
- Dose rate variability between 10 and 800 rad/s.
- Diameter of the X-ray beam up to about 1 cm in standard usage conditions.
- Laser pointer which allows aligning a DUT with the X-ray beam center.

- Possibility of inserting a monochromator to obtain an nearly mono-energetic X-ray beam.

Figure 4.15 shows the dose spectrum of X-Rays generated by Seifert Rp149. This spectrum is narrow and concentrated about 10 keV. X-Rays in such an energy range are supposed to create only ionizing effects in silicon devices.

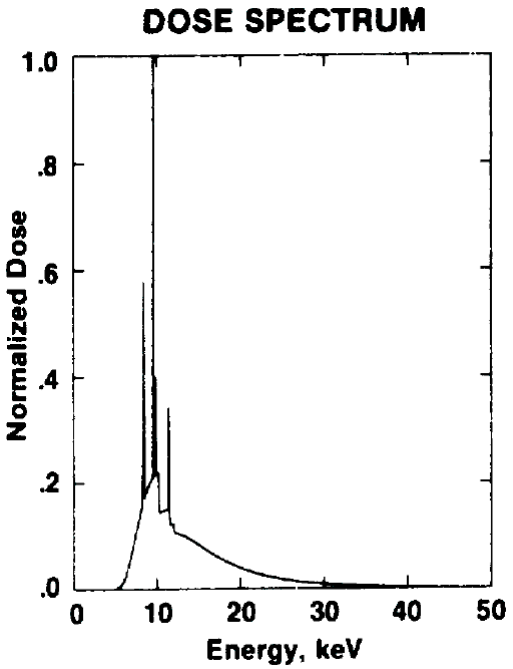


Figure 4.15:
Dose spectrums of the X-Rays from the Seifert Rp149 facility used for the sensor irradiation [123].

As it was mentioned in Section 2.4.2, the ionizing radiation leads to accumulation of a net positive charge at the $Si - SiO_2$ interface. The amount of this charge depends on the fractional hole yield, determined by the magnitude of the electric field applied through the oxide and the initial density of electron-hole pairs produced. Therefore, during exposure to ionizing radiation, the devices should be powered and read out with their nominal conditions. The sensors studied within the scope of this thesis were operating with their nominal parameters during irradiation.

The dose rate influence on the device performance after irradiation (dose rate effect) was widely studied in the past [125, 126, 127, 128, 129]. In the case of high dose rates, the density of created electron-hole pairs in the oxide is large, and the probability of electron-hole recombination is also large. As a consequence, a limited number holes arrive at the $Si - SiO_2$ interface. On the other hand, such a device is exposed to a given dose in a relatively short time, thus radiation-induced effects have almost no time to anneal. When the dose rates are low, the probability of electron-hole recombination is also low. Consequently, a large fraction of holes arrives at the $Si - SiO_2$ interface. At low dose rates, the irradiated devices are exposed to a given dose in a relatively long time and the probability of some of the radiation-induced effects to anneal is high during the irradiation process itself. In the literature cited just above, there is no agreement whether the dose rate has a strong impact on a sensor performance observed

after irradiation. The dose rate seems to influence devices implemented in some of the CMOS processes while in the case other processes no correspondence is observed. The dose-rate-related effects may also be expected in MAPS, however, they were not addressed in this thesis. For the studies described in this document, it was important to irradiate the sensors under exactly the same conditions and compare their main parameters. Therefore, all the devices studied in this thesis work were irradiated at the conditions listed below:

- X-Ray energy peak at 10 keV, tube with Tungsten.
- Dose rate: $\sim$42 rad/s.
- Distance between a DUT and X-Ray tube: 8 cm.
- Dimensions of the X-ray beam: 20$\times$11 mm^2 (ellipsoid).
- DUT temperature: 25-30 ^{o}C.

4.2.5.2 Non-ionizing radiation sources used in this work

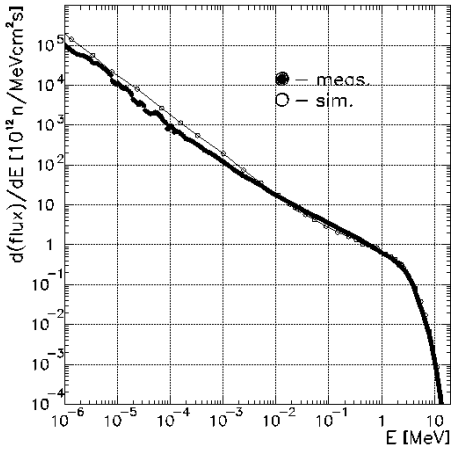
The neutrons and other particles with energies high enough to remove silicon atoms from their crystal lattice position are responsible for non-ionizing damages. The number of such particles crossing an area of 1 cm^2 of the medium within a given time period is called "fluence". It is common to refer the non-ionizing damages caused by different particles to those caused by 1-MeV neutrons. Therefore, the term "fluence" used later in this thesis will be related to the 1-MeV neutron equivalent fluence.

There are several facilities in Europe offering exposures of devices to non-ionizing radiation. Some of them, like the Ljubljana reactor [130] or the FRM II reactor from Munich [131], provide neutrons. Since neutrons in principle do not cause ionizing damage, they were chosen to irradiate samples dedicated to studies of non-ionizing-radiation effects in MAPS.

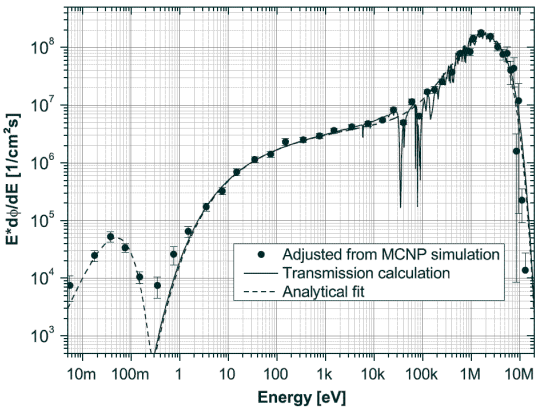
Figure 4.16 presents the energy spectra of neutrons originating from both afore mentioned irradiation facilities. The FRM II facility delivers neutrons with energies close to 1 MeV, while neutrons from the Ljubljana reactor are predominantly at energies well below 1 MeV. Unfortunately, each neutron irradiation is accompanied with simultaneous exposure to ionizing radiation. In the case of the Ljubljana reactor, the associated dose is in the range of 100 krad per each $1{\cdot}10^{13}$ $\mathrm{n_{eq}/cm^2}$ of neutron fluence. The ionizing radiation is better filtered in the case of the FRM II reactor. Since this thesis aimed at investigating the non-ionizing damages up to several 10^{13} $\mathrm{n_{eq}/cm^2}$, the neutron source providing the best filtering of the ionizing radiation background was used.

The spectra of both the Ljubljana and the Munich neutron sources were normalized, according to the NIEL scaling, to the corresponding 1-MeV neutron fluence. In the case of the Ljubljana reactor, the neutrons with energies below 100 eV were excluded from NIEL calculations. Following Figure 2.10 in Section 2.4.2.2, the displacement damage caused by

these low-energy neutrons was assumed to be significant. The NIEL calculations carried out in Munich accounted for the whole energy spectrum.



(a) Energy spectrum of neutrons from the Ljubljana reactor (Slovenia) [130].



(b) Energy spectrum of neutrons from the MedApp facility at the research reactor FRM II in Munich (Germany) [131].

Figure 4.16: Energy spectrum of the neutron sources used for sensor irradiation.

The past studies on MAPS radiation tolerance, for example presented in [4], were carried-out when the FRM II facility was not yet available. The same author studied later the consequences of neutron irradiation with both mentioned facilities. The conclusion was that the sensors irradiated at FRM II were by a factor of 2 less damaged than the ones irradiated in Ljubljana. The observed behavior would have originated from the difference in energy spectra in these two facilities. In the case of Ljubljana reactor, more low-energy neutrons were delivered to samples to achieve a given fluence than in the case of the FRM II reactor. Accounting for the NIEL scaling hypothesis discussed in Section 2.4.2.2, the non-ionizing energy loss in the sensitive volume should be equal for both neutron sources. The NIEL calculations for both sources did not account for nuclear reactions of low-energy neutrons, for example, with Boron atoms used for the p-type doping of the sensitive volume of the sensors. Due to those nuclear reactions, discussed already in Sections 2.4.2.2 and 2.3, particles with an energy sufficient to induce atom displacements are created. Those particles might be responsible for the larger damage observed for the sensors irradiated with the Ljubljana reactor where the majority of the neutrons feature energies below 100 eV.

It is worth highlighting here that the past studies on the radiation tolerance of MAPS were based on sensors irradiated with low-energy neutrons from Ljubljana. The sensors being within the scope of this thesis were instead irradiated with the FRM II in Munich.

A difficulty arises when irradiating the sensors with neutrons. The irradiation has to be carried out for sensors not yet bonded to the motherboards. This constraint originates from the fact that the motherboard would become radioactive if it is exposed to neutrons. As

a consequence, the characterization of the sensors dedicated to studying the non-ionizing radiation effects is impossible before irradiation. On the other hand, as the sensors are not biased during their irradiation, the radiation damage caused by the ionizing radiation background is less significant than for sensors running with nominal conditions.

4.3 Radiation effects in CMOS pixel sensors and current radiation tolerance status

4.3.1 Ionizing radiation effects in CMOS pixel sensors

4.3.1.1 Parasitic path creation

The ionizing-radiation effects introduced in Section 2.4.2 and related to the accumulation of a net positive charge in the Si-SiO_2 interface are present in the MAPS. This section aims at introducing an impact of ionizing radiation on the performance of this type of sensors.

The built-up positive charge at the Si-SiO_2 interface leads to shifts in the transistor threshold voltages. The CMOS sensors use only NMOS transistors in the active area. For this type of transistors, the threshold-voltage shift (V_t) is negative. This means that the voltage needed to switch the NMOS transistor ON becomes smaller as a consequence of the integrated dose. A detailed discussion about the shift of V_t is presented in [132]. The V_t shift is proportional to the thickness of the gate oxide and also to the integrated dose. The gate-oxide thickness is process dependent and it scales down with the technology feature size [133]. As a consequence, the transistors implemented in submicron technologies are intrinsically more resistant to ionizing radiation. Therefore, there is a strong interest to implement MAPS in processes featuring smaller feature size than 0.35 μm.

Apart from threshold voltage shifts, there are other effects induced by ionizing radiation. The basic NMOS transistor layout is sketched in Figure 4.17. It consists of two $N+$ regions called "drain" and "source". The latter are separated by a polysilicon gate. The silicon substrate is insulated from the gate by a thin gate oxide. The region below the gate is the transistor channel. The whole structure is surrounded by a thick field oxide (FOX), which is used to insulate the transistor from the metal layers and other devices. In fact, when an $N+$ type material is implemented, a small and not precisely known diffusion occurs over the region defined by the mask. This undesirable diffusion is illustrated in Figure 4.17(a) as the diffused N type region. The transistor gate has to be extended to insulate effectively drain from source. This situation is depicted in Figure 4.17(b). Since the transistor gate overhangs the thick field oxide, the two parasitic transistors are formed. Before irradiation, either parasitic transistors do not conduct any current or this current is much lower than the one passing through the channel region. After irradiation, the positive charge buildup in the oxide layers is responsible for a threshold voltage shift in both intrinsic and parasitic transistors. As the gate oxide is much

thinner (typically below 10 nm) than the field oxide (400-1000 nm), the magnitude of the V_t shift is more pronounced in the parasitic transistors. Consequently, the global flow of the leakage current through the parasitic transistors increases and it becomes significant with respect to the current passing the channel region.

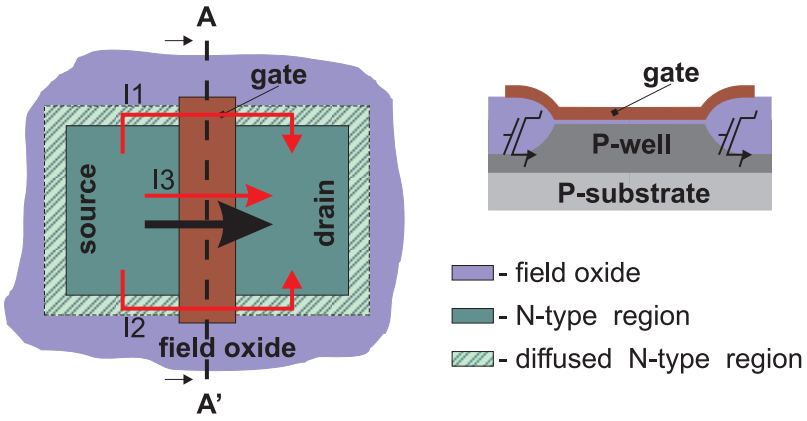


Figure 4.17: Figure illustrates the consequences of the ionizing damage in an NMOS transistor: the formation of two parasitic lateral transistors. The green "N-type region" corresponds to the CMOS process mask area used during the diffusion of the N-type silicon. The green dashed "diffused-N-type region" indicates that the N-type silicon diffuses slightly around the region limited by the CMOS-process masks. Due to this lateral diffusion, the transistor gate has to be extended (brown) in order to insulate the transistor drain from the source. Consequently, on each side of the extended gate, two parasitic transistors are built. They are shown in AA' cut of an NMOS transistor shown on the right. Because those parasitic transistors feature a thick oxide under the gate, they are more sensitive to ionizing radiation. "I1" and "I2" illustrate the current flow after irradiation of the two lateral transistors. I3 corresponds to the increase in the current flow through the transistor drain. The black arrow corresponds to the drain current before irradiation.

The well-known approach to suppress leakage paths is the use of MOS transistors featuring a so-called enclosed geometry. They are also called Enclosed-Layout Transistors (ELT). An example of ELT is sketched in Figure 4.18, as proposed in [134]. In such a configuration, the transistor drain is enclosed by the poly-silicon gate, thus by the thin gate-oxide. The transistor source region is placed outside and surrounded with a guard-ring, insulating the transistor from the outside world (bottom of Figure 4.18). The formation of a parasitic field transistor between the drain and source is automatically excluded.

4.3.1.2 Increase in the sensing-diode leakage current

Ionizing radiation also influences the performance of the sensing diodes. The increase in the sensing-diode leakage current is seen to be the major degradation when an active pixel sensor is operated in a radiation environment. As it is known from the previous discussion, the ionizing

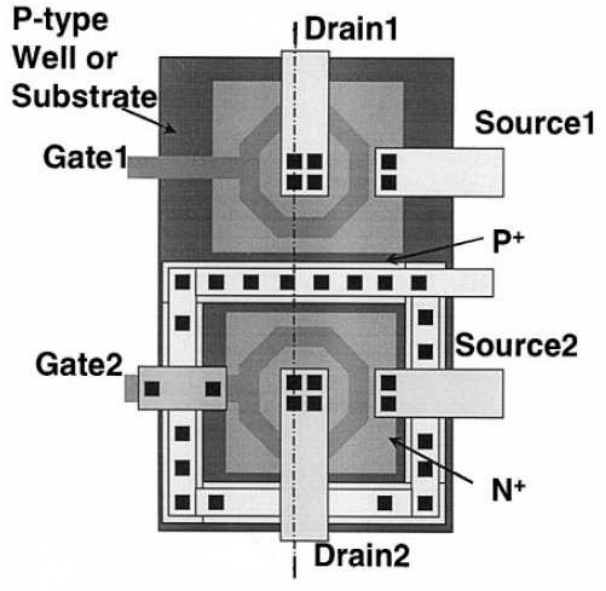


Figure 4.18:
A transistor with enclosed-layout geometry [134]. This layout prevents the formation of parasitic field-effect transistors between the drain and source.

radiation-induced interface states are responsible for an increase in the charge generation at the $Si - SiO_2$ interface and they are at the origin of an increase in the leakage current.

Figure 4.19(a) presents a cross-sectional view of a part of a MAPS pixel cell before exposure to ionizing radiation. The sensing diode and the reset transistor are shown. The sensing diode is the $N - well$—$P - EPI$ junction with an $n+$ contact implemented inside. This basic solution is called ”standard diode”. The reset transistor (and other in-pixel transistors not presented here) is a typical NMOS transistor implemented inside a P-Well. In this thesis, the name ”standard transistor” will be used for all the transistors implemented in the same way as the reset transistor depicted in Figure 4.19(a).

Figure 4.19(b) shows the cross-sectional view of the same pixel part after exposure to ionizing radiation. The positive charge buildup at the Si-SiO_2 interface is shown. The arrows correspond to the possible paths for the leakage current induced by ionizing radiation. This current leads to several undesirable effects resulting in the degradation of the MAPS performance. The latter was extensively studied in the past at the IPHC-Strasbourg and reported in [4].

These studies also addressed the possible methods for radiation hardening of the MAPS implemented in standard CMOS processes. Improvements in the radiation tolerance were achieved by implementing the so-called ”radiation-tolerant diode” and by means of the reset (and other) transistor featuring an enclosed geometry (Figure 4.18). An improved ionizing radiation tolerance was achieved by surrounding the N-well with a thin gate oxide (Figure 4.19(c)). In this oxide, the accumulation of a positive charge is significantly limited due to the reduced oxide thickness. Such a gate surrounding the diode reduces, if not prevents, the path creation for the leakage current. This translates into reduced shot-noise contribution originating from the leakage current.

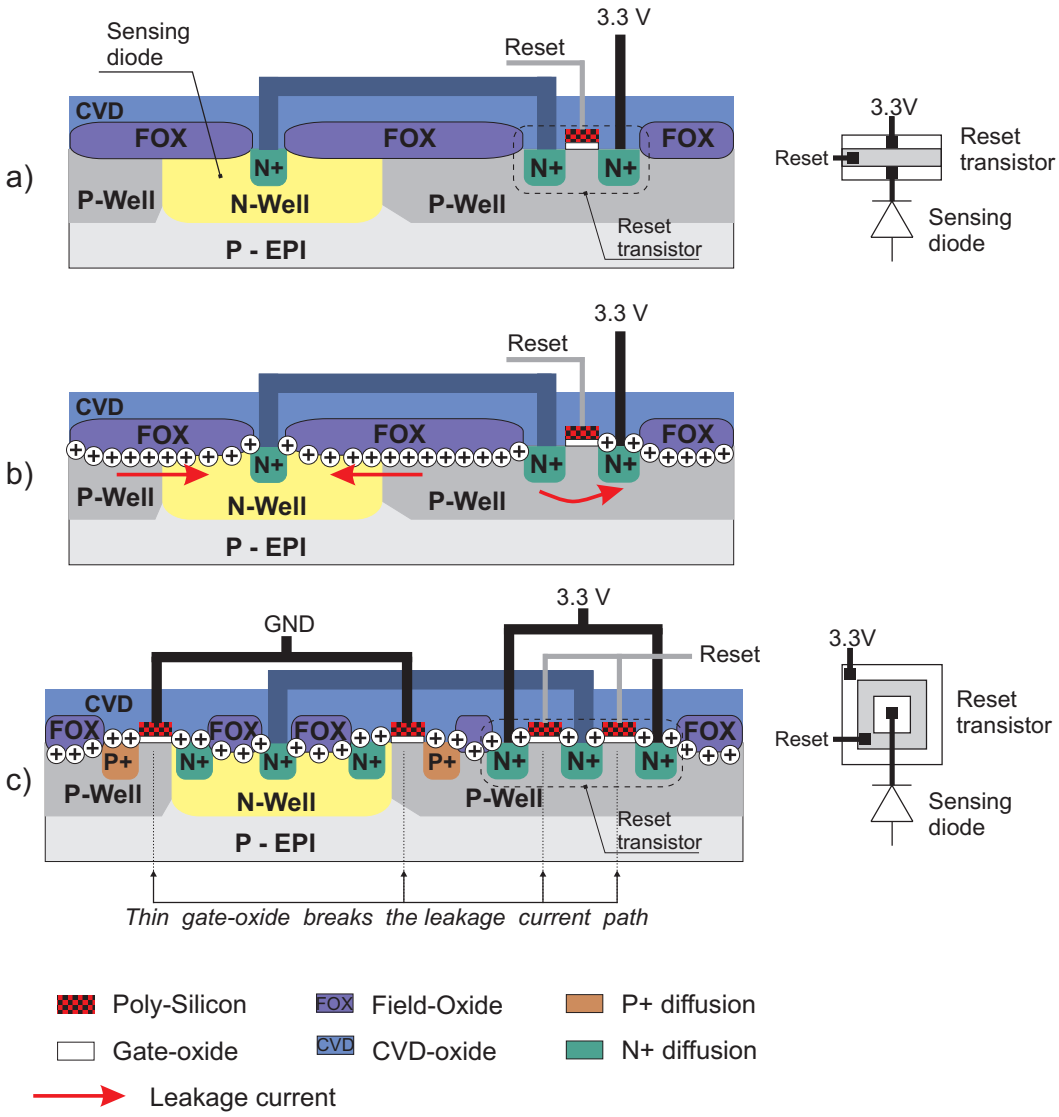


Figure 4.19: Ionizing radiation effects in CMOS sensors. (a) non-irradiated pixel, (b) irradiated pixel with charge losses due to radiation-induced leakage current, (c) irradiated radiation-tolerant diode design made in AMS-OPTO technology (MIMOSA-15)

4.3.1.3 Noise increase

The main consequence of the ionizing radiation is an increase in the leakage current of the sensing diode and accompanying transistors, and also a built-up of traps at the Si-SiO_2 interface. The increased density of traps at the Si-SiO_2 interface translates into a rise in the 1/f noise, which reduces the SNR and consequently degrades the sensor performance.

The studies on the 1/f noise in MOS devices have been carried out for many years. Some examples of such studies can be found in [135, 136, 137, 138]. These studies showed that there is a certain compromise among the 1/f noise, technology scaling, and minimum transistor

dimensions allowing the low noise to be achieved. The 1/f noise depends on the number of traps in the gate oxide N_t. This feature is driven mainly by the process quality and feature size (gate-oxide thickness) in addition to the radiation level. In submicron processes, the gate oxide is thin and the number of traps N_t is small. Therefore, the 1/f noise is comparatively low. Since the flicker noise is inversely proportional to the transistor-channel size (W·L), transistors with a very low feature size should be avoided to obtain analog circuits with a low 1/f noise.

4.3.2 Ionizing-radiation-tolerance status of CMOS sensors developed at the IPHC-Strasbourg (2007)

The performance of MAPS featuring standard and radiation-tolerant diodes was widely studied in the past. For completeness of this document, the main observations and conclusions of the past studies are given hereafter.

Figure 4.20 displays the leakage currents observed for radiation-tolerant diode of the MIMOSA-15 prototype. This sensor was implemented in the AMS-OPTO 0.35-µm process. MIMOSA-15 was based on the 3T-architecture discussed in Section 4.1.3) and had a sequential readout (see Section 4.2.2.1). This sensor was irradiated up to 1 Mrad and characterized over the temperature range from -20 °C to $+40$ °C (coolant temperature). The leakage current measured at room temperature before sensor irradiation amounted to about 10 fA. An order of magnitude higher leakage current was observed after sensor irradiation up to 1 Mrad. The irradiated and unirradiated sensors were next cooled down to -20 °C. In both the cases, the leakage current was observed to decrease to a few fA or below. It was concluded that the temporal (shot) noise component originating from the leakage current can be efficiently reduced by the means of cooling.

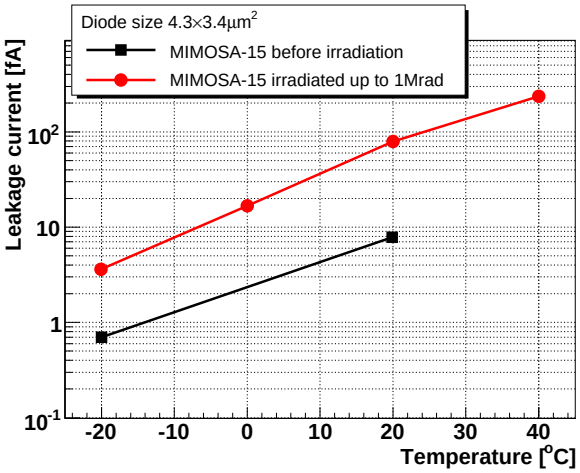


Figure 4.20:
The leakage current of the radiation-tolerant diodes implemented in the MIMOSA-15 prototype as a function of temperature. The results were observed before (black) and after (red) sensor irradiation. The temperature shown corresponds to the coolant temperature.

Leakage current of the radiation-tolerant diodes implemented in the MIMOSA-15 prototype as a function of temperature. The results were observed before (black) and after (red) sensor irradiation. The temperature shown corresponds to the coolant temperature.

The performance of the radiation-tolerant diodes implemented with MIMOSA-15 was studied with 5 GeV electron beam at DESY. The sensors were irradiated up to 1 Mrad and cooled down to -20 °C. In these conditions, the sensors were observed to provide a satisfactory SNR of 19.4 $\pm$ 0.2 (MPV). This resulted in an excellent ϵ_{det} exceeding 99.9% [4]. One may conclude from these results that the established tolerance of MAPS to ionizing radiation reached 1 Mrad at the temperature of -20 °C, and this value seemed to be not a hard limit.

Figure 4.21 displays the temporal noise as a function of the integration time measured with the MIMOSA-11 prototype. The latter featured the SB architecture (see Section 4.1.3) and a sequential readout (discussed in Section 4.2.2.1). The measurements were performed in a temperature ranging from -25^oC up to $+40^oC$ (coolant temperature), before and after sensor irradiation up to 1 Mrad. Figure 4.21 collects only part of the results which are shown for radiation-soft and radiation-tolerant diodes.

A strong dependency of the temporal noise on the integration time and on the temperature was noticed for both diode types after exposure to ionizing radiation. However, the temporal noise measured with radiation-tolerant diodes was much below the values observed for radiation-soft diodes studied under the same conditions. This is a consequence of a limited leakage current due to the radiation-tolerant diode layout. One can also notice that shortening the integration time or lowering the temperature was very effective. It allowed recovering the temporal-noise values observed before sensor irradiation.

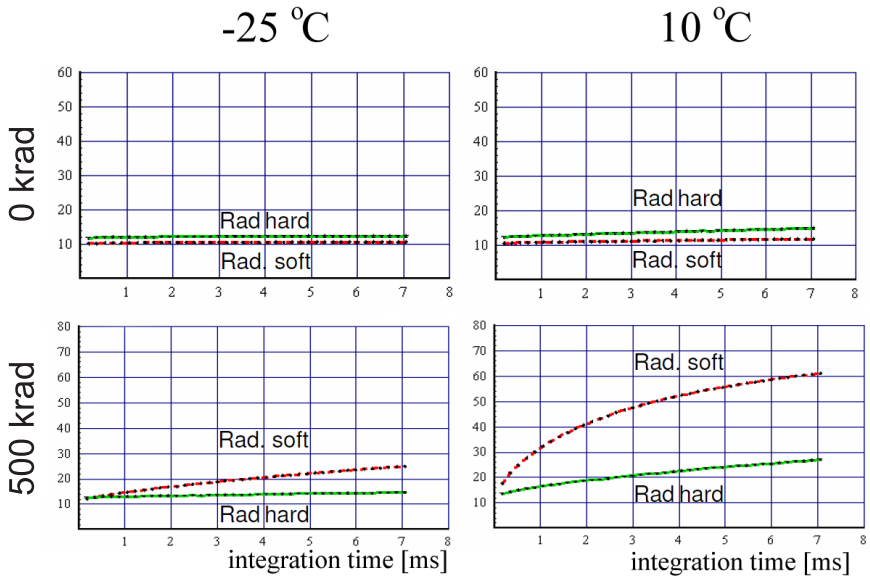


Figure 4.21: Ionizing radiation effects – temporal noise as a function of the temperature and integrated dose for MIMOSA-11 (figure taken from [4]).

Consequently, cooling the sensors and running them with a short integration time should be

considered in applications where a substantial ionizing radiation background is expected. This concerns particularly the CBM-MVD where the ionizing dose exceeding Mrad is anticipated.

4.3.3 Non-ionizing radiation effects

The prominent consequences of non-ionizing radiation are bulk damages that induce a decrease in the life-time of signal electrons. After sensor exposure to non-ionizing radiation, the lifetime reaches a level wherein a significant fraction of the signal charges may recombine before being collected by the sensing diodes. Such a deterioration of the charge-collection process leads to a decrease in the SNR, and consequently to a degradation in the sensor performance. In order to overcome these limitations, one may try reducing the distance the signal charges have to travel before being collected.

In the case of MAPS, two approaches are possible. The first one is related to the decrease in the sensor pitch which leads to a reduction in the distance between the sensing diodes. This solution is illustrated in Figure 4.22(b) and it should be compared with Figure 4.22(a) where the cross-section of a part of a sensor without any geometry modifications is displayed.

The pitch influence was a subject of the past studies performed on the MAPS radiation hardness. The main results were presented in [4, 139, 7]. Figure 4.23, taken from [7], shows how the non-ionizing radiation tolerance varies with the pitch size. The sensors with a SNR high enough to provide a ϵ_{det} above 95% were considered as operational. This observation leads to the conclusion that shortening the pitch size by a factor of 2 (20 µm$\rightarrow$ 10 µm) improves the non-ionizing radiation tolerance by about more than one order of magnitude. The tolerance assessed with the sensor featuring the smallest pitch size (MIMOSA-18) amounted to $\geqslant 10^{13}\ \mathrm{n_{eq}/cm^2}$ [140]. Therefore, the MIMOSA-18 prototype became the most robust to neutron irradiation among CMOS sensors based on a standard EPI layer.

The second approach concentrates on a reduction in the EPI-layer thickness, as sketched in Figure 4.22(c). This approach reduces the charge spread in the EPI layer and in addition the signal charges are generated closer to the sensing diodes. The signal electrons traversing the EPI layer towards the sensor substrate are also reflected within shorter distances. The studies on the influence of the EPI layer thickness on the CCE were undertaken and reported in [4, 139, 141]. The main observations derived from those studies were that a CCE increases for the sensors with a thinner EPI layer; however, an EPI layer thinner than 10 µm leads to the decrease in the signal generated by impinging particles. Consequently, the SNR governing the sensor performance decreases. It appears that the optimal thickness of the EPI layer is in the range 10 - 20 μm.

From the above facts, it became evident that the tolerance of the MAPS to non-ionizing radiation could be improved even by an order of magnitude by reducing the pixel pitch and keeping the EPI layer thickness in the optimum range of 10-20 µm. However, this approach has a serious limitation. The decrease in the pixel pitch leads to an increase in the number of

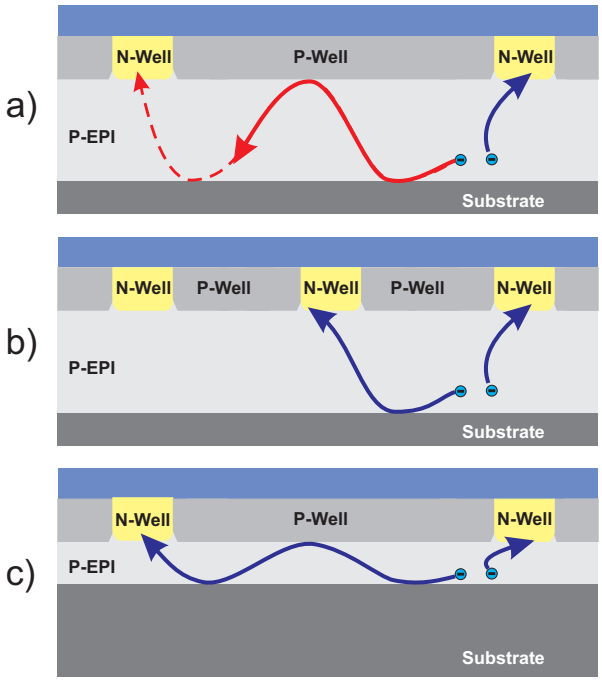


Figure 4.22:
Impact of the pixel pitch and the thickness of the EPI layer on the tolerance of CMOS sensors to non-ionizing radiation. Figure (a) presents the assumed initial situation. Figure (b) presents the sensor with a reduced pixel pitch. For the sensor shown in (c), a thinner EPI-layer is used. Both modifications reduce an average diffusion path between the generation point of the signal electrons and the collection diodes. Consequently, the probability that signal electrons are trapped is reduced and the sensors become more tolerant to non-ionizing radiation.

pixels occupying the same area. Consequently, a longer time is needed to read out a sensor and also the power consumption of the sensor increases.

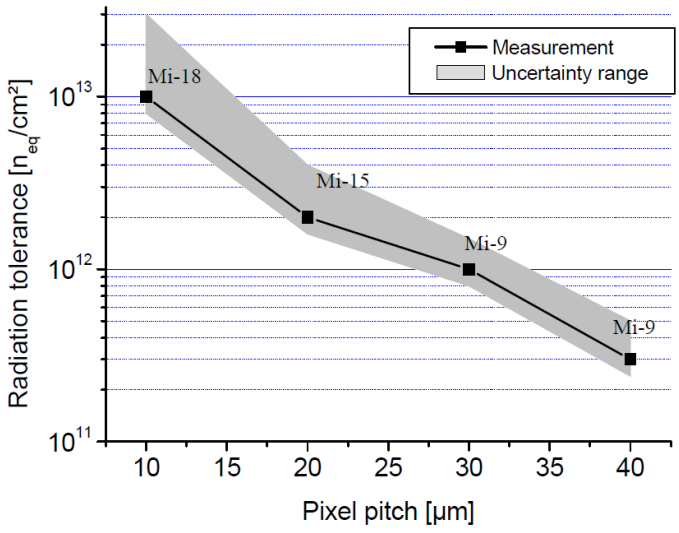


Figure 4.23:
Non-ionizing radiation effects: radiation tolerance as a function of the pixel pitch. Figure taken from [7]

4.4 Conclusions and summary

This chapter addressed the principle of operation of the MAPS and their basic architectures regarding the pixel design (3T and SB) and serial readout organization that allows achieving a readout time on the order of several milliseconds. The major quantities describing the sensor performance and basic methods used for these studies were described.

The past studies discussed in this chapter showed that the sensor performance is degraded after exposure to ionizing radiation due to an increase in the electronic noise. It was concluded that the sensing diode is the in-pixel element that is particularly sensitive to ionizing radiation. The sensing-diode-leakage-current increase from fA before irradiation up to several pA after irradiation was observed. This increased leakage current is at the origin of the significant rise in the temporal noise. Moreover, non-uniformities in the diode leakage current are observed. They translate into an FPN increase.

Transistors also suffer from ionizing radiation effects. The latter are responsible for a preoccupying rise in the temporal noise and FPN in those devices.

The past studies showed that the diode leakage current (i.e., its contribution to the temporal noise) can be efficiently suppressed by the means of a so-called "radiation-tolerant diode". It was also demonstrated that cooling the sensors down to temperatures of about -20 °C allows to recover the leakage current observed before irradiation. As a consequence, even after integration of 1 Mrad of ionizing dose, the performance of the cooled down sensors remained almost unaffected. One may thus conclude that the tolerance of the past sensors to ionizing radiation is above 1 Mrad. Since the high ionizing radiation tolerance was achieved with devices kept at negative temperatures, cooling should be considered in the applications where a substantial amount of ionizing radiation is expected, for example in the CBM-MVD.

The influence of non-ionizing radiation on the MAPS performance was also studied in the past. The tolerance to this kind of particles was observed to improve with decreased pixel pitch. The sensors featuring a pitch size of 10 µm and irradiated up to $1{\cdot}10^{13}$ $\mathrm{n_{eq}/cm^2}$ were still operational. This was not the case for the devices with a pixel pitch of 20 µm. They were able to withstand a fluence of $2{\cdot}10^{12}$ $\mathrm{n_{eq}/cm^2}$. The decrease in the pixel pitch has also disadvantages. It leads to an increase in the number of pixels occupying the same area, thus to increase in the readout time and power consumption.

The aim of R&D on the MAPS is to provide sensors which fulfill the requirements of the applications described in Chapter 1. The case of the CBM experiment, calling for a readout time of 30 µs or less and a radiation tolerance of $>$ 3 Mrad and $> 1{\cdot}10^{13}$ $\mathrm{n_{eq}/cm^2}$, is currently the most demanding one. In order to improve the readout time, the MAPS architecture has been changed from the serial to the column-parallel and the data sparsification has been implemented the inside sensors. In order to allow for a data sparsification, additional micro-circuits were implemented inside the pixels. The pitch size was increased to fit the required in-pixel electronics. This led to a compromise between the pixel pitch needed to achieve the required readout time, and the one ensuring the aimed non-ionizing radiation tolerance. Therefore, the R&D program of the IPHC-Strasbourg focused on investigation of commercially available technologies with special features, for example, a depleted EPI layer. Such a sensitive volume has a potential for further increase in the tolerance of CMOS pixel sensors to non-ionizing radiation without the need for decreasing the pixel pitch.

This thesis became a part of this R&D and it covered the studies related to radiation tolerance.

The results of these studies are gathered in next two chapters. Chapter 5 will firstly introduce the principle of operation of the column-parallel CMOS sensors with data sparsification and then focus on studying the radiation tolerance of those devices. Chapter 6 will focus on the studies undertaken to discover new radiation-tolerant processes for MAPS implementation.

5 Radiation tolerance of CMOS pixel sensors with a column-parallel readout

Several prototypes of CMOS pixel sensors with a sequential analog readout were widely studied in the past. Those devices were equipped with pixels featuring a very simple architecture (SB, 3T). Their readout time was strongly dependent on the number of pixels, number of outputs and the maximum achievable readout frequency. For example, to read out sequentially a single output matrix composed of $\sim$1 million pixels, about 40 ms are needed assuming a readout clock frequency of 50 MHz. One can partially overcome this limitation by dividing the pixel matrix into several submatrices equipped with separate outputs being read out in parallel. For practical reasons, such subdivision of a pixel matrix is also limited and typically allows the readout time to be improved by one order of magnitude. The practical limit seems to be approximately 1 ms.

The CBM experiment requires pixel sensors with a time resolution of $\sim$30 μs or less. The fact that such a time resolution was not achievable with sequential readout prompted the R&D on sensors with column-parallel architecture, providing in-parallel data filtering and restricting the readout to only those pixels which collected some signal charge.

This thesis work aims at studying for the first time the radiation tolerance of CMOS sensors with column-parallel architecture. This chapter will present the results of these studies.

5.1 The need for the column-parallel architecture

In order to speed up the readout, MAPS can be organized in N columns read out in parallel. This approach reduces the integration time by a factor of N with respect to a fully sequential readout. Because of multiple analog outputs, the amount of data produced by such sensors may easily become too large to be handled efficiently. To overcome this obstacle, a logic which selects and sends only information related to the pixels with signal above a certain threshold was implemented in the sensor. The simplified schematic of the sensor architecture containing both the column-parallel readout and the data sparsification block is shown in Figure 5.1. The sensing part contains the n-well diode and a front-end signal processing circuity (amplification and sensing-diode noise suppression). The amplified signal samples are compared with a fixed threshold. This operation is performed by the column-level discriminators [142, 143]. The necessary information about pixels with a signal above a defined threshold is obtained through a data sparsification logic, which selects them and provides their position (address)

to the outside world. Sensors based on this architecture are currently being developed at the IPHC Strasbourg. The development is organized in two parallel streams. One addresses the fast sensing part with the column-parallel readout architecture. The other stream covers the sparsification logic.

For the purpose of the column-parallel readout, the signal processing microcircuits need to be implemented inside each pixel. As a consequence, the pixels have become more complex than the "classical" ones which feature no signal processing. Such a complexity was expected to influence the robustness of the column-parallel MAPS to ionizing radiation. This prompted the studies on the radiation hardness of the column-parallel sensors. The main results will be presented later in this chapter.

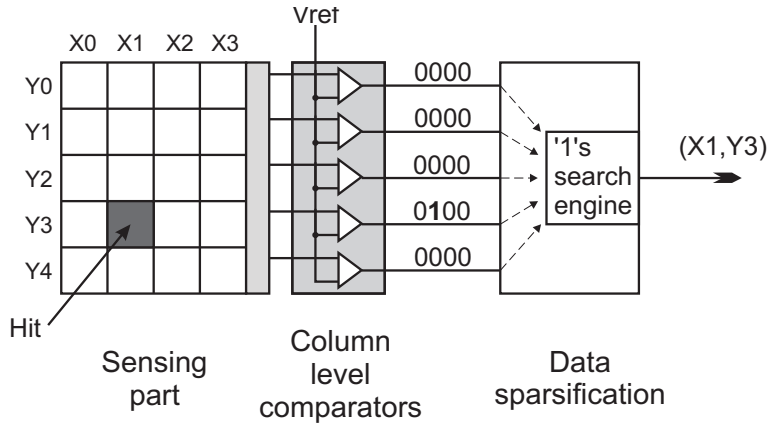


Figure 5.1: Schematic view of the sensor equipped with a column-parallel readout and data sparsification. The sensing part contains pixels equipped with an n-well diode and signal amplification. The column discriminators compare samples with a common threshold. The data spasification logic sends information about pixels with signal above threshold to the outside world.

5.2 Towards a fast column-parallel architecture with FPN noise removal and in-pixel signal processing

In order to combine the fast column-parallel readout and data sparsification, some modifications to the ordinary CMOS pixels (presented in Section 4.1.3) are needed. The signal charge produced by impinging particles is on the order of 800 - 1600 e^- (for a 10 - 20-µm-thick EPI layer). Typically, about 20 - 30% of this charge is collected by the seed pixel. For a sensing-diode size of 4.3×3.4 μm^2, the MPV of the charge collected by the seed pixel is indeed about 200 - 300 electrons. Assuming 8 - 10 fF for the diode capacitance and including the other parasitic capacitances, for example, the capacitance of the source follower, the signal is in the range of 3.5 - 4.5 mV. Moreover, the diode output voltage has some offset which varies from one diode to another (FPN, see Section 4.1.4.2). In order to select pixels delivering a

signal above a certain magnitude, the signal samples have to be compared with a discriminator threshold voltage. To accommodate the small pixel pitch, the comparators are moved outside the pixel area. A single comparator is therefore used for each column. As the magnitude of the FPN may be in the same range as the signal generated by an impinging particle [142], the signal selection with the column discriminator may become ineffective. To overcome this problem, the signal amplification and the FPN reduction have to be integrated in each pixel. In parallel, the temporal noise, having its origin in the sensing-diode shot noise and in the in-pixel circuitry (transistor thermal, shot, and 1/f noise), has to be kept as low as possible.

The best choice for in-pixel signal amplification would be to use a PMOS transistor as an amplifier load [1]. However, the implementation of PMOS transistors in a CMOS process based on a p-type substrate (suitable for MAPS) would demand the implementation of an additional n-well. The latter would compete with the sensing diode in the charge collection process and subsequently reduce the available signal. To avoid this, the in-pixel amplifier has to be based on an n-channel transistor. The implementation of n-type amplifiers with high gain inside the pixel is challenging, mainly due to space constraints.

The development of the fast column-parallel CMOS sensors with in-pixel signal processing was started several years ago. Those devices were implemented in different CMOS technologies. For testing purposes, they contained columns with digital and analog outputs. The digital ones were ended with discriminators and delivered a binary output. They were used for chip characterization with a high-energy pion beam. Columns without discriminators provided an analog output allowing for pixel characterization. Table 5.1 contains the list of sensor prototypes with fast architecture and presents their main performance characteristics.

5.2.1 The first prototype of the CMOS sensor with the column-parallel architecture – MIMOSA-6

The first step towards the construction of the high-performance sensor integrating the column-parallel readout was made in 2003 with the sensor prototype called MIMOSA-6 [144, 143]. This chip contained 30×128 pixels featuring various sensing diodes (4.0×3.7 μm^2 and 5.0×4.7 μm^2) and various amplification schemes (with and without a clamping capacitor). MIMOSA-6 was designed for the purpose of verifying the overall functionality of the column-parallel architecture and its different building blocks. The performance of the amplifiers and the functionality of the CDS implemented in the pixel were the points of interest.

The simplified in-pixel architecture without a clamping capacitor[2] is sketched in Figure 5.2. The in-pixel architecture was designed to have two storage capacitors (Cs1,Cs2), needed for the CDS operation. After a diode reset, the signal from the sensing diode was amplified by the in-

[1] PMOS transistors would allow the design of an in-pixel amplifier with a higher gain than with only NMOS transistors.

[2] The architecture with a clamping capacitor will not be discussed here.

Table 5.1: Main features of the column-parallel CMOS sensors developed at IPHC-Strasbourg.

Prototype name	Technology	EPI thickness [μm]	Pixel pitch [μm]	Columns	Temporal noise/FPN [e^-] [a]	Comments
MIMOSA-6	MIETEC 0.35 μm	4	28	24 digital 6 analog	15/120	Not optimized for the FPN
MIMOSA-8	TSMC 0.25 μm	7	25	24 digital 8 analog	18/6	Low SNR mainly due to thin EPI layer.
MIMOSA-16	AMS-OPTO 0.35 μm	14	25	24 digital 8 analog	15/7	Not optimized diode size and in-pixel architecture.
MIMOSA-22/22bis/22ter	AMS-OPTO 0.35 μm	14	18.4	128 digital 8 analog	12/4	Used for in-pixel architecture optimization and radiation-tolerance assessment. **Within the scope of this thesis work.**

[a] Both types of noise observed for sensors before irradiation.

pixel amplifier (A) and memorized in the storage capacitor Cs1. After a time corresponding to the integration time, the diode voltage was sampled a second time, amplified, and memorized in the storage capacitor Cs2. Next, both signal values stored in Cs1 and Cs2 were passed through the source followers SF1 and SF2 to the column-level comparator block shared by all the pixels from the same column. There, the difference between the two signal samples was computed and compared with the comparator reference voltage (Vcomp). This operation was performed for all the pixel outputs connected sequentially to the comparator front-end. Moreover, in order to limit the power consumption, the in-pixel amplifier was switched on only during the short period of time covering the clock pulses needed to read out the pixel.

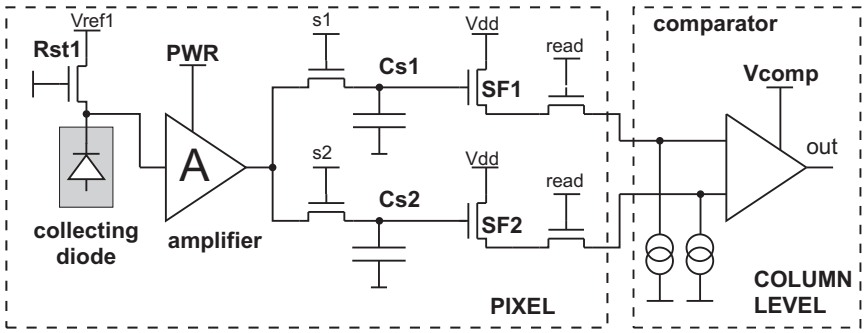


Figure 5.2: Simplified schematic of the first sensor prototype – MIMOSA-6 – with the column-parallel architecture. The pixel and the column-level elements are surrounded by dashed lines.

Tests with this device showed that the CDS functionality was implemented successfully inside the pixels and that the discriminator design goals were met. The chip was extensively studied in the laboratory. The temporal noise, measured with the analog outputs, was on the order of $\sim 15\,e^-$ [143]. However, an unexpectedly high FPN, in excess of $120\,e^-$ [143], was observed. The source of this FPN was assigned to non-uniformities between the storage capacitors (Cs1 and Cs2) and between the source followers (SF1 and SF2) [144, 143]. Despite this high FPN, MIMOSA-6 validated the possibility of in-pixel sampling and storing signals from two different time slots. The excessive FPN noise observed for MIMOSA-6 prompted more extensive studies dedicated to in-pixel architectures equipped with a "clamping" capacitor. This step was at the origin of the MIMOSA-8 prototype discussed hereafter.

5.2.2 The architecture towards FPN noise reduction – MIMOSA-8 prototype

The sensor prototype MIMOSA-8 [145, 146] was fabricated using the standard CMOS TSMC 0.25-μm process with an EPI-layer thickness of about 7 μm. In general, the TSMC process exhibited a lower dispersion between transistors than the process used for the production of MIMOSA-6. MIMOSA-8 contained 4 subarrays, each with pixels featuring sensing diodes of different dimensions: $1.2\times1.2\ \mu m^2$, $1.7\times1.7\ \mu m^2$, $2.4\times2.4\ \mu m^2$ (architecture with a reset transistor), and $4.1\times2.5\ \mu m^2$ (architecture with a self-biased diode). The pixels were organized in a 25-μm pitch matrix with 32 columns and 128 rows. MIMOSA-8 was equipped with 24 pixel columns connected individually to a discriminator. The eight remaining columns provided analog information allowing for the pixel characterization.

Following the technique presented in the reference [147], the in-pixel architecture of the MIMOSA-8 sensor was optimized (see Figure 5.3) to achieve a lower FPN and to reduce the diode reset noise. This new in-pixel architecture was proposed in [148] and widely studied in [142, 149, 150, 151], proving its performance and functionality as needed for later data sparsification implementation. The optimization of the sensor architecture regarding FPN was related to the reduction of the non-uniformities of the storage capacitors (Cs1,Cs2) and of the source followers (SF1,SF2), shown in Figure 5.2. Instead of the two storage capacitors, a single, serially connected clamping capacitor (MOSCAP) was used to reduce the diode reset noise (see Figure 5.3). Also, the two source followers were replaced by only one. The two storage capacitances were moved to the column-level microcircuitry. Following the previous prototype idea for limiting the power consumption, the in-pixel amplifier was switched on only during the period dedicated to the pixel readout. The details related to the MIMOSA-8 architecture are discussed in details in Appendix A.1.

The FPN and the temporal noise were measured in the laboratory with the eight analog outputs. A temporal noise value not exceeding $\sim 20\,e^-$ was observed in the worst case, pertaining to the $2.4\times2.4\ \mu m^2$ diode. The FPN of $\sim 6\,e^-$ was the same for all pixels featuring the 3T-base architecture. Pixels based on the SB architecture exhibited the FPN of $\sim 4\,e^-$ [149]. The latter was a factor of 30 smaller than the FPN obtained for MIMOSA-6. Thus, the architecture

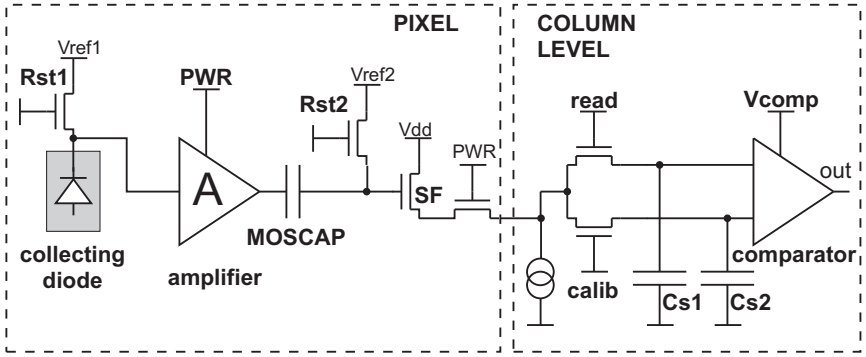


Figure 5.3: Simplified schematic of the improved column-parallel architecture implemented in MIMOSA-8. This architecture features a single source follower (SF) and a clamping capacitor (MOSCAP). The capacitors Cs1 and Cs2 were moved outside the pixel (column level) and became common for the whole column of pixels.

of MIMOSA-8 became the baseline for the next prototypes.

The sensor performance was also assessed with a high-energy pion beam. The ϵ_{det}, derived from discriminated data collected with a beam telescope [152], was $99.3 \pm 0.1\%$ for a discriminator threshold slightly above 3 times the noise [146]. The relatively thin ($\sim$7 µm) EPI layer of MIMOSA-8 translated into a relatively low signal charge generated by an impinging particle crossing the sensor. As a consequence, the SNR observed was below 10 [141]. Since the SNR was poor, the discriminator threshold voltage could not be set optimally to efficiently filter excessive noise signals. Consequently, these noise signals were treated as true hits and the sensor manifested a significant FH_{rate} of above 10^{-3}. The σ_{res} was governed by the pixel pitch and amounted to $\sim$7-8 µm.

In order to improve the detector performance, the implementation of a new device on a substrate based on a thicker EPI layer was necessary. One of the processes offering such a feature was the 0.35-µm AMS-OPTO CMOS process. The MIMOSA-8 architecture was translated into this technology and the new prototype, called MIMOSA-16, was produced.

5.2.3 Improvement of the charge collection efficiency - MIMOSA-16

The MIMOSA-16 prototype was a nearly exact translation of the MIMOSA-8 design from TSMC to the 0.35-µm AMS-OPTO CMOS process. MIMOSA-16 was implemented using wafers with an EPI-layer thicknesses of 14 µm and 20 µm. Due to the thicker EPI layer, an improvement of the SNR was expected with respect to MIMOSA-8. The sensor was divided into 4 submatrices (32 rows each) which hosted pixels with different sensing-diode sizes: 1.7×1.7 µm^2(standard version), 2.4×2.4 µm^2 (standard and radiation-tolerant version), and 4.5×4.5 µm^2 (standard version). The pixels containing the largest sensing diodes were connected to a new version of the in-pixel amplifier with an enhanced gain and a negative feedback loop. The pitch size for this sensor was 25 µm.

The performance of MIMOSA-16 was assessed with a high-energy particle beam. The readout was running at a clock frequency of 100 MHz, translating into 51 µs of integration time. The measured temporal noise of the subarray equipped with 4.5×4.5 µm^2 diodes was ∼15 e$^-$. The measured SNR was in the range of 16-17 (Most Probable Value of the Landau fit). The σ_{res} was about 5 µm. The ϵ_{det} was measured for all the matrices. The results are shown in Figure 5.4. The influence of the diode size on the ϵ_{det} was clearly present. Regarding the ϵ_{det}, only the pixels with the largest sensing diodes gave satisfactory results. This was attributed to the poorer CCE of the smaller-sized sensing diodes. The poor CCE was attributed to an n-well screening effect by the other implants (e.g., p+, p-well), which was more pronounced for the 0.35-µm AMS-OPTO CMOS process than for the TSMC process used for MIMOSA-8. Such implants located next to the sensing diode were suspected to prevent the minority charge carriers from reaching the n-wells. However, for pixels with the largest sensing diodes, where the screening effect was less pronounced, the SNR was observed to be high enough for efficient particle detection.

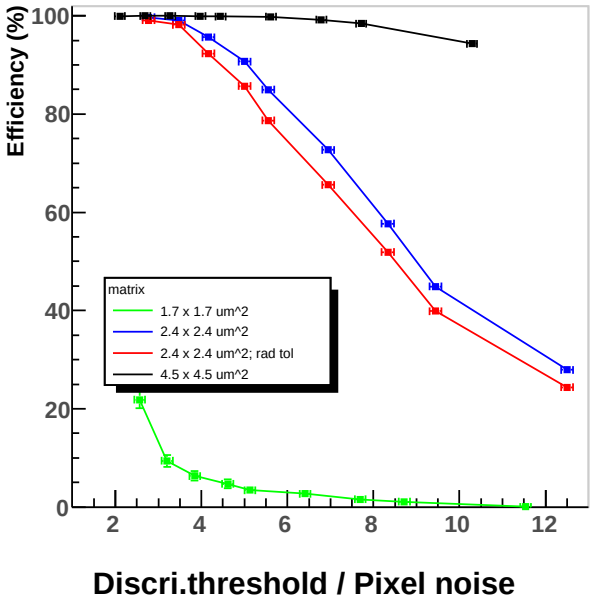


Figure 5.4: The ϵ_{det} assessed with the digital part of the MIMOSA-16 prototype as a function of the discriminator threshold voltage. The observed performance depends significantly on the sensing-diode size. Only the largest diode of 4.5×4.5 µm^2 achieves the required detection efficiency of above 99% for a relatively wide threshold voltage range.

The ϵ_{det} for the matrix with the largest diodes was above $99.9\% \pm 0.1\%$ for a discriminator threshold voltage of 4 mV, where the FH$_{rate}$ of about $2{\cdot}10^{-4}$ was observed. Increasing the discriminator threshold voltage to 6 mV did not affected the ϵ_{det}, but it reduced the FH$_{rate}$ to a value $\sim 10^{-5}$ [141]. One major outcome of this prototype was to prove that a very high ϵ_{det} for a MIP was achieved for discriminator threshold values high enough to keep a very low FH$_{rate}$.

Despite the satisfactory performance achieved with the MIMOSA-16 matrices equipped with

the largest diodes, the pitch size of 25 μm was too large to ensure the required σ_{res} and non-ionizing radiation tolerance. Also, the size of the sensing diode was yet not optimized. Indeed, the largest sensing diodes featured the best charge collection, thus SNR, but they also had the largest parasitic capacitance. This capacitance resulted in a high temporal noise of $\sim$15 e^- (compared with typical value of 10-12 e^-). In order to reach the targeted performance, all the features implemented in the MIMOSA-16 pixels were translated into a smaller pixel pitch and a smaller diode size. The new device was named MIMOSA-22. The main features of this sensor will be discussed hereafter.

5.3 First radiation-tolerance assessment for a large-scale CMOS sensor with in-pixel signal processing

The simplified block diagram of the analog and the digital parts of the MIMOSA-22 sensor is shown in Figure 5.5. Each pixel integrated a sensing diode with a size of $\sim$15 μm^2, a signal amplifier, and CDS circuitry. All elements were enclosed in an area of 18.4×18.4 μm^2, which defined the pixel pitch. The chip hosted 136 columns with 576 pixels each. Of those columns, 128 ended with a discriminator and were used to measure the ϵ_{det}, FH_{rate}, and σ_{res} with the full discrimination chain. Eight more columns without a discriminator were implemented to allow access to the analog signals; these were used to estimate the CCE and electronic noise.

The MIMOSA-22 prototype was equipped with the JTAG (IEEE 1149.1 Rev. 1999) communication standard [153]. The control interface based on JTAG allowed the internal registers of the sensor to be accessed. The internal registers were used to define, for example, the sensor bias or to control the digital to analog converters. All parameters related to the pixel readout sequence, including the control of the discriminators, were also accessible via the JTAG interface. More details related to the communication with MIMOSA-22 can be found in [154].

In the search for the optimum design, several alternative in-pixel amplifier architectures were studied. The tolerance of these architectures to ionizing radiation was addressed for the first time within this thesis work.

5.3.1 Performance tests of the in-pixel amplifier architectures

A substantial signal amplification in an early stage of the signal processing chain, namely inside pixels, is highly desirable since it alleviates the impact of the noise introduced by the next stages (chip periphery). It is also needed for efficient signal discrimination with column comparators, as already mentioned in Section 5.2. The performance of the amplifier, for example, stable gain and low noise, should remain inappreciably affected by temperature variations and irradiation. The power consumption can be limited by using the amplifier in switched mode and operating the amplifier only when the pixel is read out. This adds complexity to the design. In order to find the optimum in-pixel amplifier architecture, several

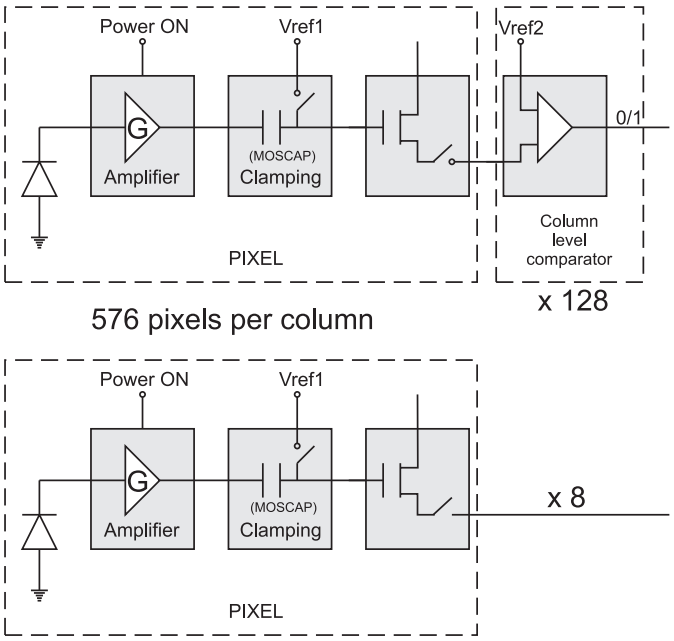


Figure 5.5:
Simplified sensor architecture of the MIMOSA-22 prototype. Top: Schematic of a column ended with a discriminator. Bottom: Schematic of a column with analog output. The 128 columns with discriminator and the 8 columns with analog output are integrated into the chip.

options were studied with MIMOSA-22. They are depicted in Figure 5.6.

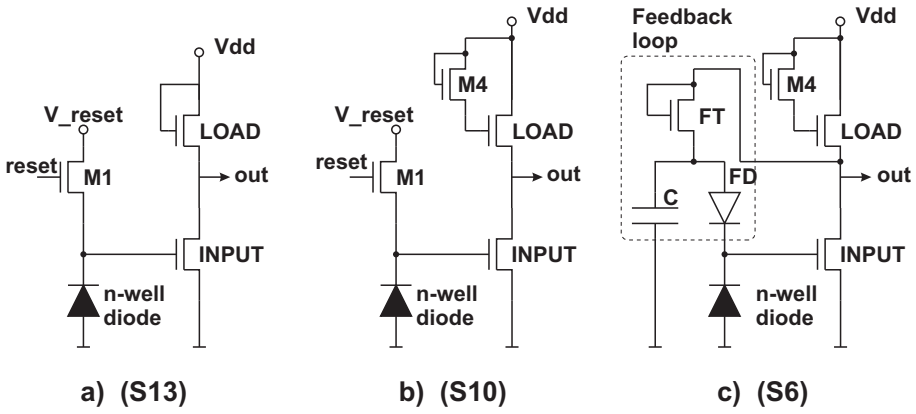


Figure 5.6: The three in-pixel amplifier architectures studied with MIMOSA-22:
a) Common-Source amplifier.
b) Common-Source amplifier with improved gain.
c) Common-Source amplifier with improved gain and feedback loop.

The basic architecture, called S13, is based on a common-source (CS) amplifier stage and depicted in Figure 5.6(a). Its gain is defined by the properties of both the input and the load transistors. The relationship between the amplifier small-signal gain and the transistor properties is given by [155]:

$$\frac{V_{out}}{V_{in}} = \frac{g_{m_{IN}}}{g_{m_{LOAD}} + g_{mb_{LOAD}} + g_{ds_{IN}} + g_{ds_{LOAD}}} \tag{5.1}$$

where: $g_{m_{IN}}$ and $g_{m_{LOAD}}$ stand for transistor transconductances; $g_{ds_{IN}}$ and $g_{ds_{LOAD}}$ are the output conductances of the transistor channels; $g_{mb_{LOAD}}$ refers to the body-effect transconductance of the load transistor; the indices $_{LOAD}$ and $_{IN}$ are related to the load and input transistors of the CS amplifier stage.

A higher AC gain was achieved with the architecture S10 by decoupling the gate of the load transistor with one additional NMOS transistor (M4), as shown in Figure 5.6(b). Simulations [99] showed that the AC gain of this architecture was improved with respect to S13, but the DC operating point and the DC gain were unchanged. The small-signal gain of architecture S10 is given by the following relation [155]:

$$\frac{V_{out}}{V_{in}} = \frac{g_{m_{IN}}}{g_{mb_{LOAD}} + g_{ds_{IN}} + g_{ds_{LOAD}}} \tag{5.2}$$

Another approach proposed for the in-pixel amplifier architecture is depicted in Figure 5.6(c). The presented architecture (S6) is based on a CS amplifier equipped with a negative feedback loop. The feedback is formed by a low-pass filter with a very large time constant defined by the capacitance (C) and the transconductance of the feedback transistor (FT). From the DC analysis point of view, the pixel output voltage of this architecture is defined by resistor divider composed of the load transistor, feedback-loop transistor, forward-biased diode, and sensing diode:

$$V_{out} = V_{GS_{INPUT}} + V_{FB} + V_{DS_{FT}} = V_{DD} - V_{DS_{LOAD}} \tag{5.3}$$

For small-signal analysis the circuit is a feedback-loop amplifier with the AC gain given by Equation 5.2.

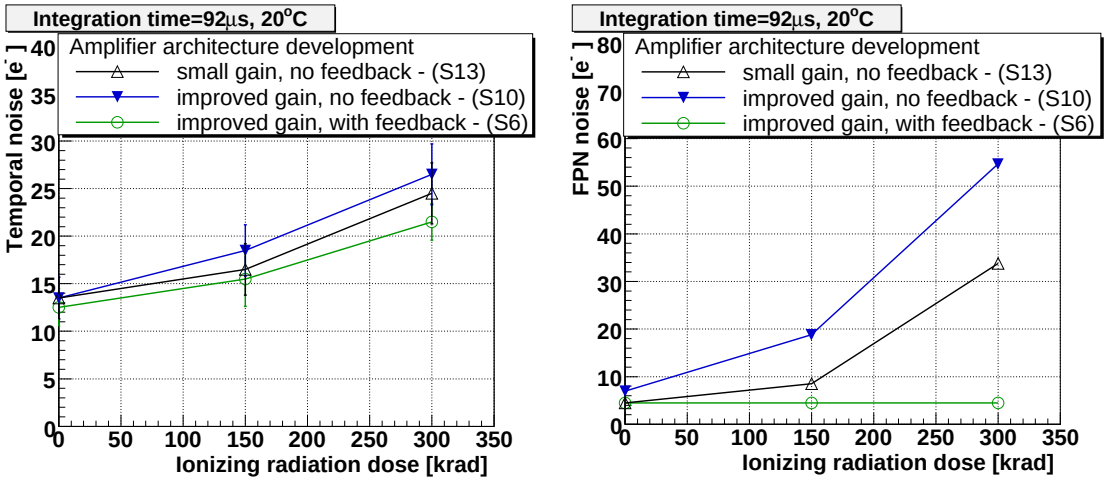
In order to increase the ionizing radiation tolerance, the radiation-tolerant version of the sensing diode (see Section 4.3.1.2) was used. The performance of different in-pixel architectures was tested in the laboratory as well as with a high-energy particle beam. The results of those tests will be discussed next.

5.3.2 Ionizing-radiation tolerance of MIMOSA-22 – laboratory tests and results

Several samples of MIMOSA-22 were irradiated to 150 krad and 300 krad. The temporal noise and the FPN of the investigated in-pixel amplifier architectures were the main points of interest. The measurements of both observables were done using the eight columns providing analog signals. The tests were performed at 20 °C with an ^{55}Fe source (Section 4.2.3.1). The performance of the in-pixel amplifiers was characterized at a nominal clock frequency of 100 MHz, which corresponds to an integration time of $\sim$92 μs.

The temporal noise and FPN values as functions of the ionizing dose are presented in Figure 5.7. The temporal noise and FPN were similar for all the investigated architectures before irradiation.

After irradiation, the architecture (S6) with the negative feedback loop was observed to exhibit the best performance. This architecture featured the smallest temporal-noise increase



(a) Temporal noise (b) FPN

Figure 5.7: The temporal noise (a) and the FPN (b) as functions of ionizing dose measured for MIMOSA-22 featuring in-pixel architectures with (S6) and without (S10, S13) a feedback loop. Measurements were performed at the nominal sensor integration time of ∼92 μs and at temperature of +20 °C.

and the FPN remaining unchanged (see Figure 5.7(b)). The unchanged FPN observed for the submatrix S6 with respect to the submatrices S10 and S13 may be attributed to the different in-pixel architecture, in particular to the presence of the feedback loop.

Guided by the unaltered FPN after irradiation, the pixel design based on the amplifier with a negative feedback loop was retained as a baseline for future sensors with column-level signal discrimination.

5.3.3 Ionizing-radiation tolerance of MIMOSA-22 – beam test results

The response of MIMOSA-22 to a MIP was studied with a high-energy particle beam. The studies addressed the sensors before irradiation as well as after irradiation to 150 and 300 krad. The beam telescope, introduced in Section 1.2, was used for the reconstruction of the impinging particle tracks. The measurements were performed with 92 μs of integration time and at a coolant temperature of 20 °C. This section will present the most important results.

Table 5.2: The most probable values of the SNR for the three amplifier architectures studied with MIMOSA-22 before irradiation. The statistical uncertainties of the measurements are shown.

Subarray	S6	S10	S13
SNR	17.6 ± 0.2	16.5 ± 0.3	16.0 ± 0.3

Data from the eight analog columns of non-irradiated MIMOSA-22 were used to estimate the SNR of the investigated subarrays. The most probable values of this parameter are presented in

Table 5.2 [156]. Within the uncertainties shown here, the most probable values of SNR observed for the investigated architectures are the same.

Figure 5.8 shows the results of ϵ_{det} and FH_{rate} for non-irradiated MIMOSA-22 chips. A satisfactory ϵ_{det} for all matrices was achieved for a relatively large discriminator threshold equivalent to up to six times the pixel noise. This threshold value allowed for FH_{rate} below 10^{-4}.

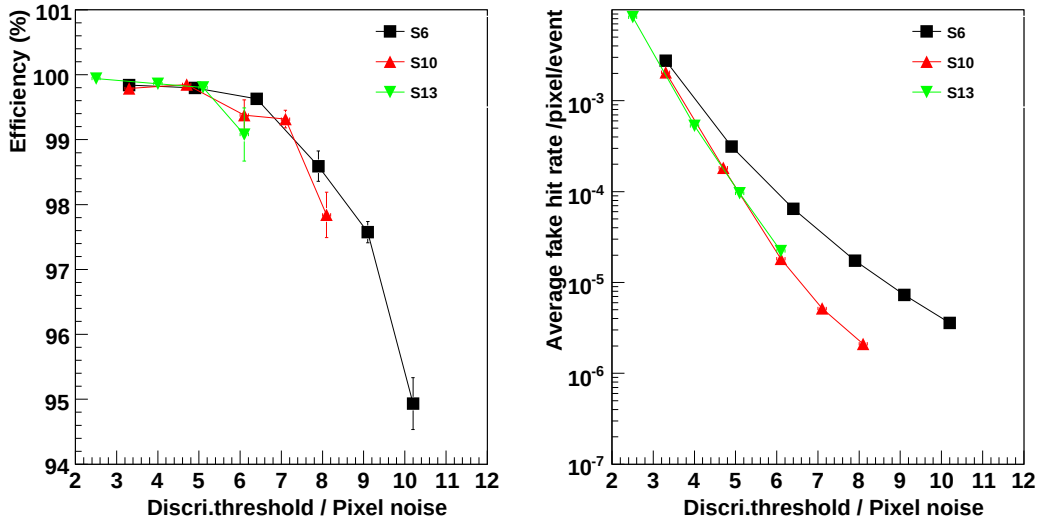


Figure 5.8: The results from the studies of MIMOSA-22 with the 120 GeV/c pion beam. The left panel of the figure displays the ϵ_{det} of three different pixel architectures as function of the discriminator threshold. The right panel shows the FH_{rate}. In order to compare the performance of architectures featuring different gains, the x-axis was converted from [mV] to discriminator threshold voltage [e^-] / electronic noise [e^-]. The measurements were performed with 92 μs of integration time and at a coolant temperature of 20 °C.

Despite the highest SNR observed among the investigated submatrices, the S6 architecture exhibited the highest FH_{rate} for the same equivalent discriminator threshold. For example, for a threshold value equal to six times the temporal noise, the FH_{rate} observed with architecture S6 was approximately a factor of five higher than the one obtained with architectures S10 and S13. The observed differences could be attributed to the fact that different groups of pixels were used for assessing the FH_{rate} than were used for the SNR measurements. In the case of the FH_{rate} assessment, the 128 columns featuring the discriminators were read out. In contrary, the SNR measurements were based on the eight analog columns.

Despite the relatively large FH_{rate}, the S6 architecture was considered as particularly interesting for future sensor development. This is because its FPN remained unchanged after irradiation.

The three investigated in-pixel amplifier architectures were also studied with minimum ionizing particles after exposure to ionizing radiation. A substantial FH_{rate} increase and a

Table 5.3: Test results with a high-energy pion beam for the S6 subarray of MIMOSA-22. The measurements were performed with 92 µs of integration time and at a coolant temperature of 20 °C. The statistical uncertainties of the measurements are shown.

Irradiation	Threshold [mV]	SNR cut	ϵ_{det} [%]	σ_{res} [µm]	FH_{rate}
non-irradiated	3.0	6.2	99.79 ± 0.06	3.9 ± 0.1	$5.8 \pm 0.1\ 10^{-5}$
	4.3	8.3	99.02 ± 0.11	3.9 ± 0.1	$9 \pm 1\ 10^{-6}$
	5.4	10	97.25 ± 0.20	3.5 ± 0.1	$6 \pm 1\ 10^{-6}$
150 krad	1.7	3.3	99.89 ± 0.04	4.0 ± 0.1	$1.60 \pm 0.01\ 10^{-3}$
	3.0	4.8	99.66 ± 0.07	4.1 ± 0.1	$8.1 \pm 0.1\ 10^{-5}$
	4.3	6.2	98.50 ± 0.15	4.2 ± 0.1	$6 \pm 1\ 10^{-6}$
300 krad	3.0	4.5	99.42 ± 0.09	4.3 ± 0.1	$1.50 \pm 0.01\ 10^{-4}$
	5.3	6.8	95.38 ± 0.25	3.8 ± 0.1	$5 \pm 1\ 10^{-6}$

ϵ_{det} drop were observed for the in-pixel architectures without the feedback loop (S10 and S13), even for relatively low discriminator threshold voltages. This drop was attributed to the significant FPN increase[3] after irradiation already observed in the laboratory and discussed in Section 5.3.2. In contrary, the performance of the in-pixel architecture featuring the feedback loop was only moderately degraded.

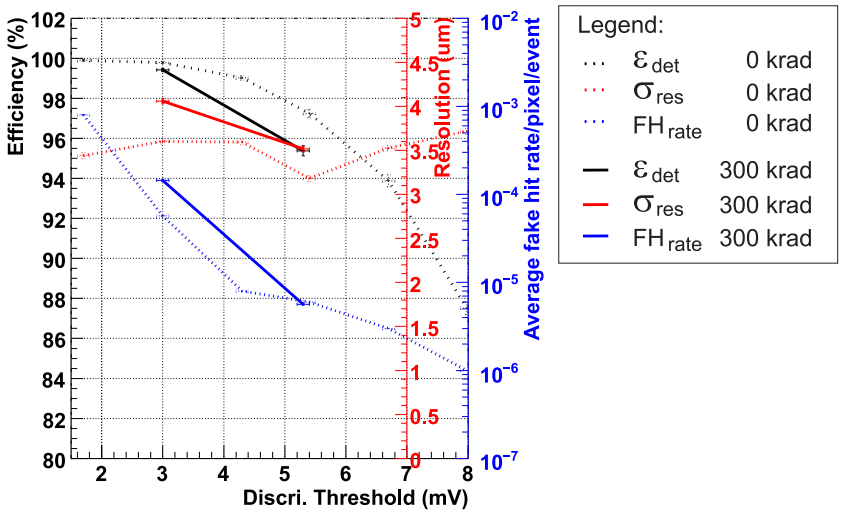


Figure 5.9: The performance of subarray S6 of MIMOSA-22 as a function of discriminator threshold voltage. The parameters were assessed with a high-energy particle beam before and after sensor exposure to 300 krad. The measurements were performed with an integration time of 92 µs and at a coolant temperature of +20 °C.

Table 5.3 lists the main parameters measured for architecture S6 (containing a feedback loop)

[3]Due to a large FPN after irradiation, a fraction of pixels is above the threshold even for a high threshold voltages. This fraction of pixels contributes to the FH_{rate}.

before and after sensor irradiation: ϵ_{det}, σ_{res}, and FH_{rate}. These parameters are also depicted in Figure 5.9 as functions of the discriminator threshold voltage. The σ_{res} observed for the S6 architecture (digital outputs used) amounted to $\sim$3.5-4.0 µm for sensor before and after irradiation. This meets the requirements of the sensor application in the CBM-MVD.

In order to judge whether the sensors were operational after irradiation or not, the criterion described in Section 4.2.4 was used. One can notice that a $\mathrm{FH}_{rate} \leqslant 10^{-4}$ and $\epsilon_{det} \geqslant 99\%$ is possible for MIMOSA-22 irradiated to 150 krad, while after irradiation of up to 300 krad, the performance starts to be at the edge of acceptance.

The observed drop in sensor performance was attributed to the temporal noise increase after irradiation. However, previous studies of the radiation tolerance of MAPS without in-pixel signal processing (but with exactly the same design of the sensing diode) showed a lower temporal noise after the same ionizing dose (see Section 4.3.2). Consequently, the currently observed increase in the temporal noise could not be attributed to the sensing diode but to the in-pixel amplifier. This observation triggered the studies aiming at unraveling the possible sources of the excessive temporal noise. These studies were undertaken with an upgraded MIMOSA-22 sensor called MIMOSA-22bis.

5.4 Improvement in the radiation hardness of an in-pixel amplifier with a negative feedback loop – MIMOSA-22bis

The studies made with the MIMOSA-22 prototype showed that the design of the in-pixel amplifier architecture had a significant influence on the FPN, which remained unchanged after ionizing irradiation only for the architecture with the feedback loop. However, another problem related to an unexpected rise in the temporal noise component arose.

The temporal noise increase after irradiation was suspected to originate from the in-pixel elements (feedback loop as well as input and load transistors). The difficulties arise since the influence of the particular in-pixel elements cannot be simulated based on the SPICE models delivered by the CMOS technology provider. Those models are usually created for devices working in a different operation regimes than the elements used in the MAPS pixels. For some elements (e.g., ELT, irradiated transistors), such SPICE models are not available.

To determine which in-pixel elements are particularly sensitive to ionizing radiation, another approach was used. The properties of some of the elements were changed systematically. Those changes were implemented in a new version of the sensor called MIMOSA-22bis which was next studied under different conditions regarding the radiation level, temperature, and integration time.

5.4.1 Tested subarrays – MIMOSA-22bis

The aim of designing MIMOSA-22bis was to explore the influence of the following elements on the pixel performance after irradiation:

- the feedback transistor type (standard and enclosed geometry) and size (W/L)
- the input-transistor and the load-transistor geometry
- the sensing-diode size

Table 5.4 summarizes the characteristics of the feedback transistors implemented in each subarray of MIMOSA-22bis. The ELT was implemented in the feedback loop of the in-pixel amplifier of two subarrays which differ in sensing-diode size (4.3×3.4 μm^2 and 3.1×3.65 μm^2). The submatrix S5 containing the "standard" feedback transistor was an exact copy of subarray S6, tested previously with MIMOSA-22. It was implemented to allow a direct comparison of the performance of in-pixel-amplifiers hosting either the standard transistor or ELT in the feedback loops. The layouts of the pixel cells (with larger diodes) for the subarrays S4 (feedback ELT) and S5 (standard feedback) of MIMOSA-22bis are shown in Figure 5.10.

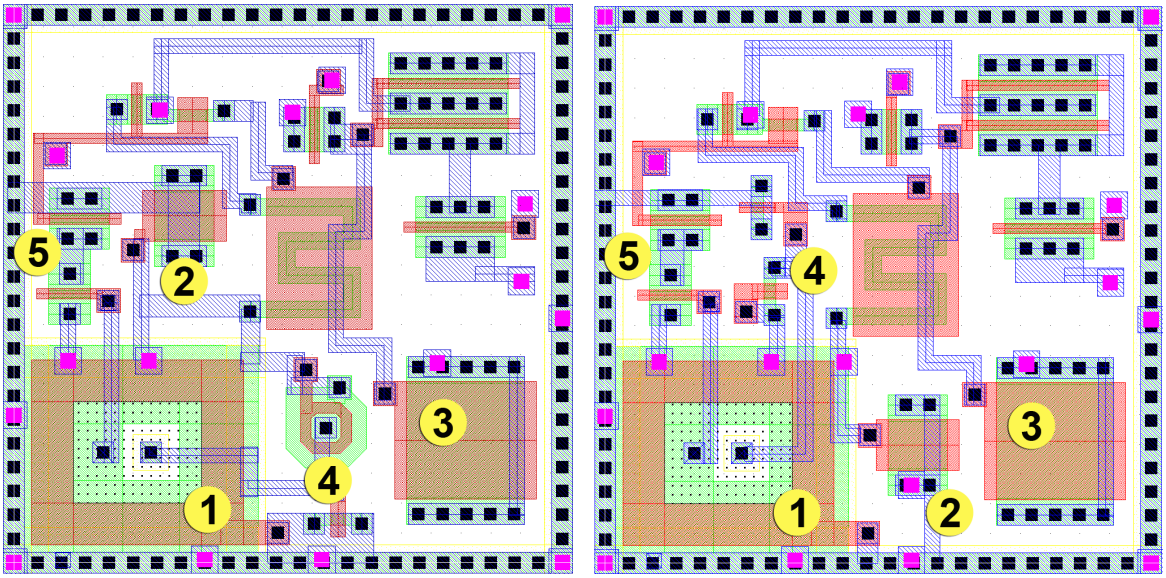
In order to investigate the behavior of the subarray equipped with feedback ELT and to verify the sensing-diode influence on the temporal noise, 3 subarrays with smaller (3.1×3.65 μm^2) diodes were implemented. Figure 5.11 shows the pixel layouts of the subarrays equipped with smaller diodes.

Finally, the influence of the load-transistor and the input-transistor geometry (W/L) on the amplifier noise performance after irradiation was addressed with MIMOSA-22bis.

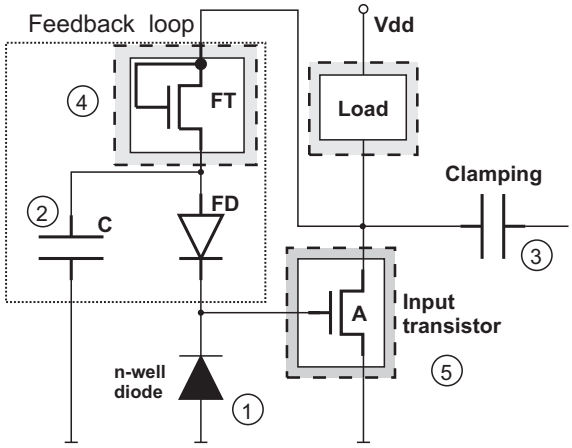
5.4.2 Beam-test results of improved in-pixel amplifier architectures – larger diodes

MIMOSA-22bis test matrices, which contain pixels equipped with diodes of size 4.3×3.4 μm^2 as listed in Table 5.4, were tested with a high-energy particle beam. The tests were performed with non-irradiated devices as well as with some others exposed to 150 krad and 300 krad. The studies were performed at nominal integration time of ∼92 µs, achieved with a 100-MHz readout clock frequency, and at a stabilized coolant temperature of 20 °C. The main focus was to compare the performance between the subarrays containing either the "standard" (S5) or the ELT (S4) transistor in the feedback loop.

Figure 5.12 graphically depicts the main results: the ϵ_{det} and the FH_{rate} for subarrays S5 and S4 measured with non-irradiated sensors as well as with those exposed to 150 krad and 300 krad. The same results are also listed in Table 5.5. To better understand the impact of ionizing radiation on the detector performance, gray and blue backgrounds were introduced to the figures. The gray region corresponds to the discriminator threshold voltages where ϵ_{det} was below the required value of 99%. The blue region corresponds to the discriminator threshold



(a) ELT (S4). (b) "Standard" (S5).

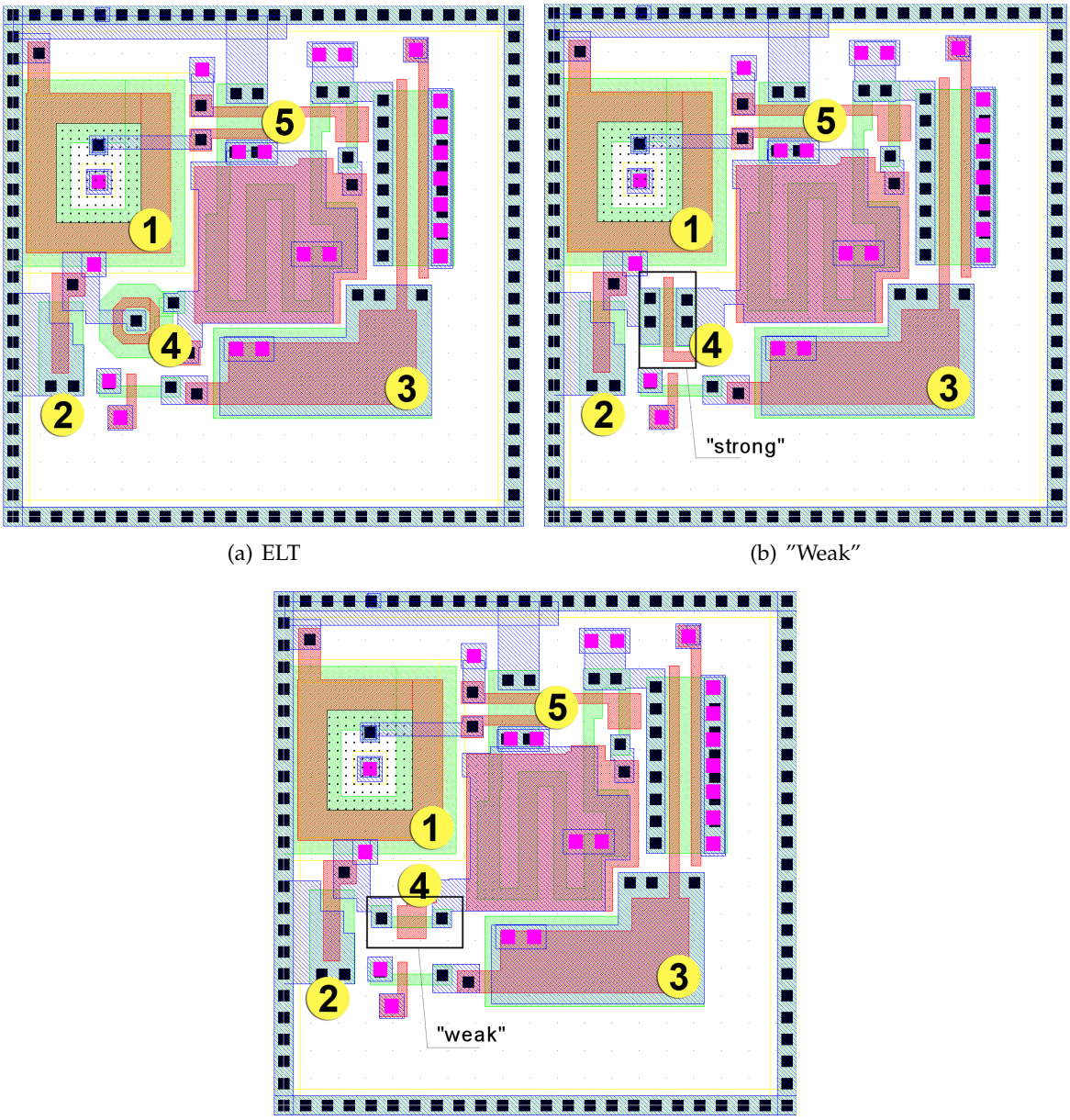


(c) Addressed in-pixel elements.

Figure 5.10: Layouts of MIMOSA-22bis pixels; (a) pixel (S4) with the ELT feedback transistor; (b) pixel (S5) with the "standard" feedback transistor. (1) sensing diode, (2) feedback low-pass-filter capacitor, (3) clamping capacitor, (4) feedback transistor, and (5) in-pixel amplifier; (c) schematical representation of the in-pixel elements studied with MIMOSA-22bis.

Table 5.4: Feedback transistors used in the test architectures implemented in MIMOSA-22bis.

Diode	Feedback trans.	Trans. dimensions
4.3×3.4 μm^2	ELT (S4)	W=4.4 µm, L=0.35 µm
4.3×3.4 μm^2	"standard" (S5)	W=0.4 µm, L=0.50 µm
3.1×3.65 μm^2	ELT	W=4.4 µm, L=0.35 µm
3.1×3.65 μm^2	"Weak"	W=0.4 µm, L=1.05 µm
3.1×3.65 μm^2	"Strong"	W=2.1 µm, L=0.35 µm



(a) ELT (b) "Weak"

(c) "Strong"

Figure 5.11: Layouts of MIMOSA-22bis pixels with different feedback transistor types and geometry. (a) pixel with the ELT feedback transistor, (b) pixel with the "Weak" feedback transistor, (c) pixel with the "Strong" feedback transistor. (1) sensing diode, (2) feedback low-pass-filter capacitor, (3) clamping capacitor, (4) feedback transistor, and (5) in-pixel amplifier.

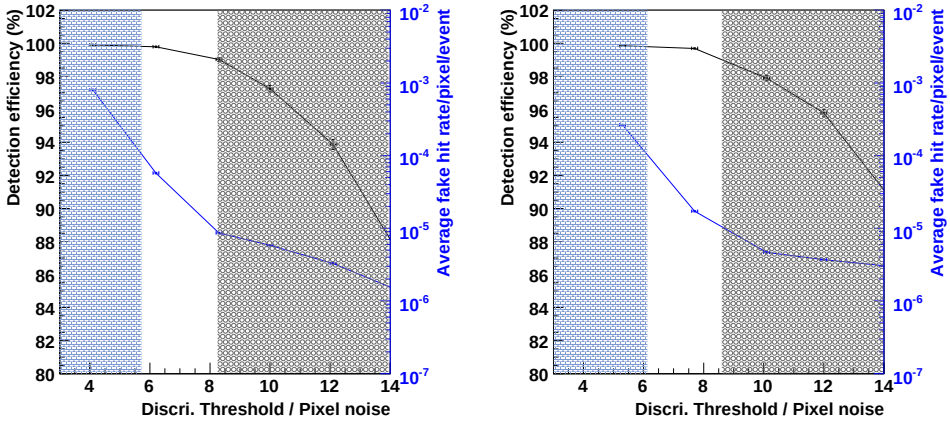
voltages where the FH_{rate} was above 10^{-4}. The empty region (white) between the gray and blue regions shows the useful range of the discriminator threshold values.

One can notice that both investigated submatrices (with the standard transistor or the ELT in the feedback loop) performed similarly and satisfactorily before irradiation for threshold values amounting to about six to eight times the pixel temporal noise. The similar performance was observed after irradiation to 150 krad, but with a narrowed range of threshold values. After 300 krad, the required performance could no longer be achieved with the submatrix featuring a standard feedback transistor. Instead, for the architecture hosting the ELT (S4), a ϵ_{det} of 99.05 ± 0.13 % was measured with a FH_{rate} of $4.3 \pm 0.5\, 10^{-5}$ for a discriminator threshold of 5.5 times the pixel noise. For this subarray, there is probably still some narrow range of threshold values where the required performance can be achieved. The width of this region is not well-known as the subarray S4 was not characterized with thresholds where the FH_{rate} $\sim 10^{-4}$ was reached.

Table 5.5: Results from the tests with a high-energy pion beam for the two investigated subarrays of MIMOSA-22bis: standard (S5) and ELT (S4). The ϵ_{det}, σ_{res}, and FH_{rate} were measured as functions of the discriminator threshold voltage and the irradiation dose. The uncertainties shown here are statistical.

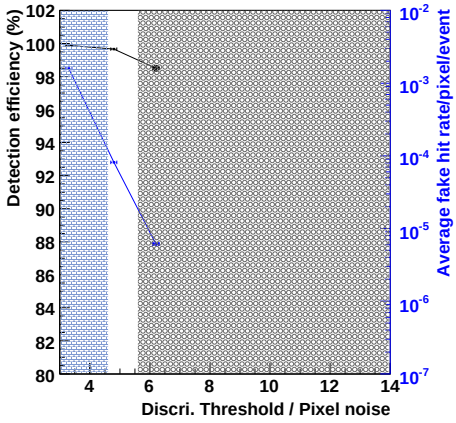
Subarray name and radiation level	Threshold [mV]	ϵ_{det} [%]	σ_{res} [µm]	FH_{rate}	SNR cut
"standard"	3.0	99.79 ± 0.06	3.9 ± 0.1	$5.8 \pm 0.1 \cdot 10^{-5}$	6.2
0 krad	4.3	99.02 ± 0.11	3.9 ± 0.1	$9 \pm 1 \cdot 10^{-6}$	8.3
	5.4	97.25 ± 0.20	3.5 ± 0.1	$6 \pm 1 \cdot 10^{-6}$	10
"standard"	3.0	99.66 ± 0.07	4.1 ± 0.1	$8.1 \pm 0.1 \cdot 10^{-5}$	4.8
150 krad	4.3	98.50 ± 0.15	4.2 ± 0.1	$6 \pm 1 \cdot 10^{-6}$	6.2
"standard"	3.0	99.42 ± 0.09	4.3 ± 0.1	$1.40 \pm 0.01 \cdot 10^{-4}$	4.5
300 krad	5.3	95.38 ± 0.25	3.8 ± 0.1	$6 \pm 1 \cdot 10^{-6}$	6.8
ELT	3.0	99.69 ± 0.06	3.3 ± 0.1	$1.7 \pm 0.1 \cdot 10^{-5}$	7.7
0 krad	4.3	97.88 ± 0.16	3.6 ± 0.1	$5 \pm 1 \cdot 10^{-6}$	10.1
	5.4	95.78 ± 0.22	3.6 ± 0.1	$4 \pm 1 \cdot 10^{-6}$	12.0
ELT	3.0	99.48 ± 0.07	3.9 ± 0.1	$2.9 \pm 0.1 \cdot 10^{-5}$	5.3
150 krad	4.3	97.37 ± 0.17	4.0 ± 0.1	$5 \pm 1 \cdot 10^{-6}$	6.5
ELT	3.0	99.05 ± 0.13	3.5 ± 0.1	$4.3 \pm 0.5 \cdot 10^{-5}$	5.5
300 krad	5.3	92.44 ± 0.33	3.8 ± 0.1	$4 \pm 1 \cdot 10^{-6}$	8.1

Summarizing, one can conclude that the performance of the pixels equipped with the feedback-ELT is better than those equipped with a standard feedback-loop transistor, especially

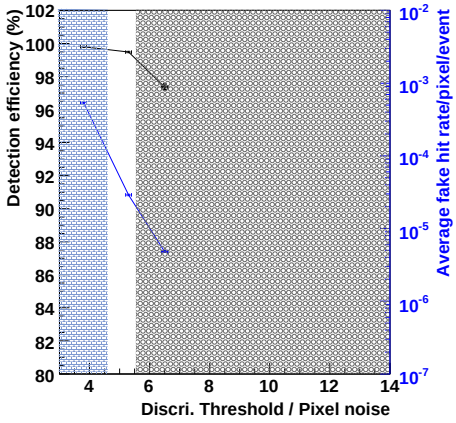


(a) S5 (standard) - before irradiation

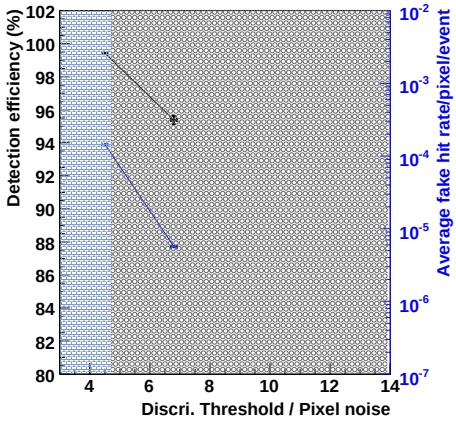
(b) S4 (ELT) - before irradiation



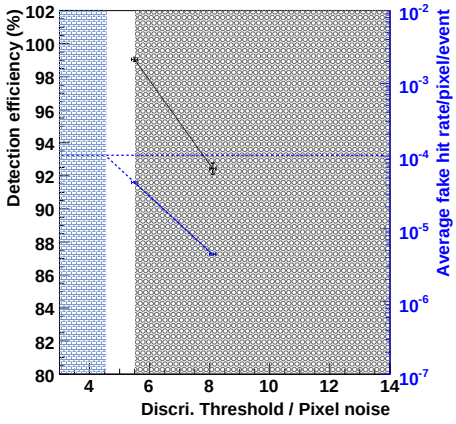
(c) S5 (standard) - 150 kRad



(d) S4 (ELT) - 150 kRad



(e) S5 (standard) - 300 kRad



(f) S4 (ELT) - 300 kRad

Figure 5.12: Degradation of the performance after irradiation for MIMOSA-22bis architectures S5 (standard) and S4 (ELT). The gray region corresponds to the discriminator threshold voltages where a ϵ_{det} was below the required 99%. The blue region corresponds to the discriminator threshold voltages where the FH_{rate} was above the target upper limit of 10^{-4}. The empty region (white) in between shows the useful range of the discriminator threshold values.

after exposure to ionizing radiation. However, the performance improvement achieved by means of the feedback ELT was modest and a radiation tolerance up to 1 Mrad could not be achieved due to excessive temporal noise. To understand the sources of this noise, extended tests conducted in the laboratory. They will be described hereafter.

5.4.3 Motivation for extended tests

The better performance of the architectures featuring an ELT in the feedback-loop was established by tests with a high-energy pion beam. The beam tests covered a very narrow range of conditions with regard to the sensor temperature, integration time, and radiation dose. As a consequence, it was difficult to identify the sources of the excessive temporal noise which degraded the sensor performance after irradiation. Further studies were therefore undertaken in the laboratory with an $^{55}\mathrm{Fe}$ source. The following aspects were addressed:

- The influence of the feedback transistor geometry and type on the temporal noise.
- The dependence of the temporal noise on the load-transistor and input-transistor geometry.
- The noise at different operating conditions characteristic for various CMOS sensor applications: temperature, radiation level, and integration time.

Sensors were studied over a temperature range of -10 °C up to +40 °C and after exposure to different ionizing doses from 150 krad up to 1 Mrad (300 krad and 500 krad were intermediate values). The negative temperature range and the highest ionizing doses are representative of the CBM-experiment running conditions while higher temperatures and lower ionizing doses are the running conditions expected for the STAR experiment. Moreover, lowering the temperature was already known as a very efficient means of recovering an acceptable performance for the irradiated devices without in-pixel signal processing (see Section 4.3.2). It seemed natural to verify whether the performance of the irradiated sensors with in-pixel signal processing, in particular regarding the temporal noise, could also be recovered to the level before irradiation.

The performance of MIMOSA-22bis was also tested using different integration times. These studies were necessary because the column-parallel MIMOSA sensors are being developed to satisfy the needs of several applications. For example, an upgrade of the STAR vertex detector requires sensors with a readout time of $\leqslant 200$ µs, while for the CBM-MVD, 30 µs is required.

The following section will discuss the results obtained during extensive laboratory studies addressing the MIMOSA-22bis sensor prototype. These results will also be compared with results of the former prototype (MIMOSA-11 - implemented in the same technology as MIMOSA-22bis) which did not feature the advanced in-pixel signal processing [4].

5.4.4 MIMOSA-22bis — laboratory test results — the influence of the feedback-transistor type on the radiation tolerance

The main parameter studied was the temporal noise. Figure 5.13 shows the dependence of the temporal noise of architectures S4 (feedback ELT) and S5 (standard feedback) on the ionizing-radiation dose. The data presented here were measured at +20 °C and with a sensor integration time of 92 µs.

The observed temporal noise was nearly the same[4] for both subarrays up to about 300 kRad. At higher doses, the difference in the noise performance between architectures S4 and S5 became more pronounced. The subarray based on a feedback ELT exhibited a lower temporal noise than the one based on a "standard" transistor. For example, after 1 Mrad, the difference observed was $\sim 12 \pm 1e^-$.

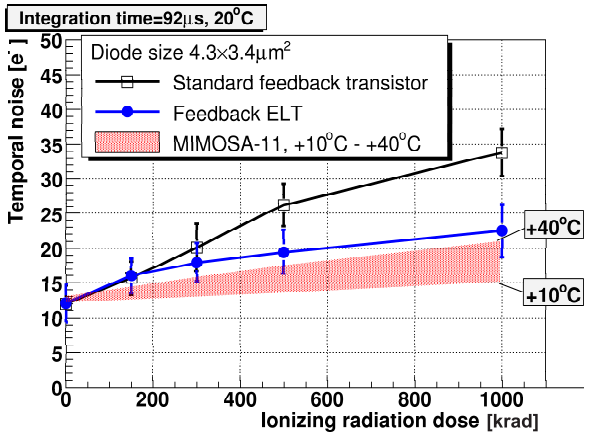


Figure 5.13: Temporal noise of MIMOSA-22bis observed for subarrays S4 (feedback ELT) and S5 (standard feedback) each as functions of ionizing dose. The data obtained at +20 °C and at an integration time 92 µs. The red shaded area corresponds to the temporal noise values measured for the MIMOSA-11 prototype, which did not feature in-pixel signal processing (the integration time was 180 µs). The uncertainties shown here represent the temporal noise distribution over the pixel array. The noise values presented in this graph were measured with a precision of $\pm 0.9e^-$ in the worst case (standard feedback transistor at 1 Mrad).

Figure 5.13 compares the temporal noise of MIMOSA-22bis and MIMOSA-11 (red shaded region). In the case of MIMOSA-11, the noise was measured at +10 °C and +40 °C (coolant temperature), with an integration time of 180 µs. The temporal noise before irradiation was observed to be nearly the same for both the MIMOSA-11 and MIMOSA-22bis pixels. However, starting from 150 krad, the noise measured for MIMOSA-22bis was systematically higher than

[4] A slightly different performance of the architectures S4 and S5 when irradiated up to 300 kRad was observed during tests with a high-energy particle beam (see Section 5.4.2). During tests with MIP, the performance of the subarray S4 was better than that of S5. This observation may be explained by the fact that during the beam tests, sensors were kept at a temperature several degrees higher than during the laboratory tests. The higher operating temperature most likely causes differences in the noise of S4 and S5 to appear while they were marginal during the laboratory tests ongoing at room temperature.

the one measured for MIMOSA-11, despite the latter having an integration time that is twice as long. After the pixels were irradiated up to 1 Mrad, the temporal noise measured for MIMOSA-11 did not exceed 21 e^-, even at a temperature of +40 °C. Instead, a noise of about 22 e^- was observed at +20 °C for MIMOSA-22bis subarray S4 (feedback ELT) and about 34 e^- for subarray S5 (standard feedback transistor). Despite the improvement achieved by using the transistor with an enclosed topology, pixels with signal processing still seem to be more sensitive to ionizing radiation.

The previous studies (see Section 4.3) showed that by cooling sensors to temperatures below 0 °C, the noise performance of the irradiated sensors featuring simple in-pixel architectures was efficiently recovered to the value observed before irradiation. This observation is important for the CMOS sensor applications involving cooling and featuring a high-ionizing-particle background, in particular the CBM experiment, where ionizing radiation exceeding 1 Mrad is expected. Therefore, the temporal noise of MIMOSA-22bis was studied for higher doses in the regime of negative sensor temperatures.

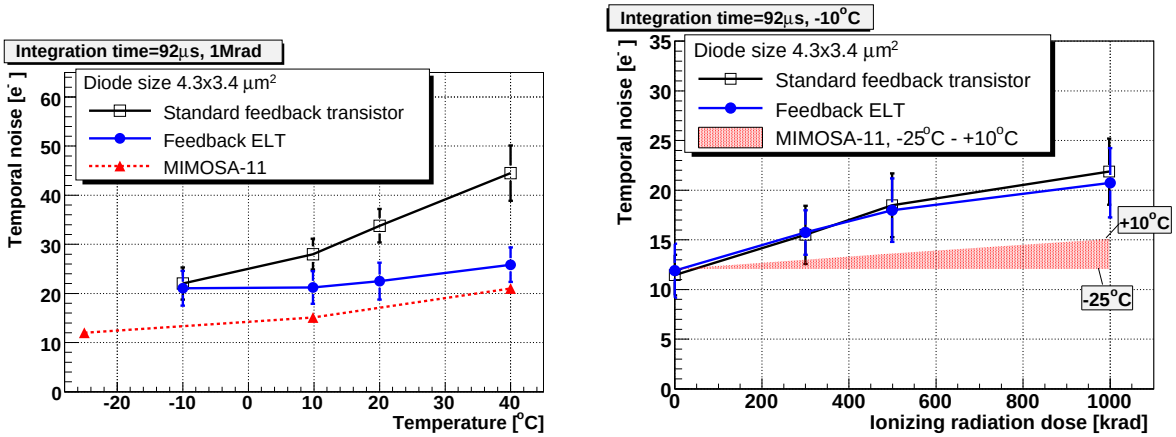


Figure 5.14: MIMOSA-22bis – variation of the temporal noise with temperature after irradiation to 1 Mrad (left); Temporal noise as a function of the integrated dose, observed at a constant temperature of -10 °C (right); Dashed line and shaded region correspond to the data measured for MIMOSA-11, i.e., the sensor without advanced in-pixel signal processing (the integration time is 180 μs in this case). The uncertainties shown here represent the temporal noise distribution over the pixel array.

Figure 5.14 (left) shows the influence of the temperature on the sensor noise performance. The measurements were performed with MIMOSA-22bis running with an integration time of 92 μs and irradiated up to 1 Mrad. The same figure shows the temporal-noise values observed for MIMOSA-11 irradiated to 1 Mrad and tested with an integration time of 180 μs (red dashed line). One can observe that the temporal noise decreased with increasing temperature for all architectures. Cooling the sensor down to decrease the temporal noise was most efficient in the case of pixels equipped with the "standard" transistor in the feedback-loop. For pixels with the feedback ELT (S4), only a modest improvement was observed. Moreover, the temporal noise

of the architecture S4 seemed to reach a plateau at approximately +10 °C: The same temporal noise of $\sim$21 $\pm$ 0.7 e^- was observed at +10 °C and -10 °C. Another interesting observation was made at -10 °C: At this temperature, the temporal noises of architectures S4 and S5 were almost identical.

Figure 5.14 (right) shows the temporal noise measured at -10 °C and an integration time of 92 µs as a function of the ionizing dose. As can be seen, at each investigated dose, the noise performance of architectures S4 and S5 was the same. Moreover, the temporal noise had a tendency to rise significantly with the integrated dose, even at a temperature of - 10 °C, where the shot-noise contribution originating from the leakage currents (e.g., sensing diode, FB diode, and transistors), was significantly suppressed. A difference of approximately 10.2 ± 0.9 e^- between unirradiated sensors and the one exposed to 1 Mrad was observed. The same tendency was not found for MIMOSA-11, which featured a "simple" in-pixel architecture (see red region). The temporal noise for MIMOSA-11 did not increase after irradiation up to 1 Mrad for sensors cooled down to -25 °C and only moderately increased from $\sim$10$\pm$0.5 e^- to 15$\pm$0.6 e^- was found at +10 °C.

The variation of the temporal noise with integration time was also studied with the architectures S4 and S5. Figure 5.15 depicts the results measured for MIMOSA-22bis irradiated up to 150 krad and 1 Mrad. In general, shortening the integration time reduced the temporal noise measured for both of the investigated subarrays. At the ionizing radiation doses and integration times expected in the STAR experiment (150 krad, $\leqslant$200 µs), the performance of the subarrays S4 and S5 is approximately the same (see Figure 5.15(a)). At higher doses, the differences in the noise performance between architectures S4 and S5 are more pronounced. Figure 5.15(b)) shows the temporal noise of both architectures after sensor irradiation to 1 Mrad. It is clear that at this integrated dose, the use of the ELT in the feedback is beneficial. However, despite the ELT in a feedback, even a very short integration time does not allow the temporal noise to be reduced below 20 e^-. This observation is in agreement with previous observations indicating the noise plateau at approximately $\sim$21 e^- for this radiation level.

Summarizing, there are several important observations regarding the performance of irradiated sensors with in-pixel signal processing:

- **At temperatures above 0 °C, the architecture with the feedback ELT features lower temporal noise after irradiation than the architecture with the standard transistor.** In this temperature range, the leakage current is not suppressed and it contributes to the shot noise, thus contributes to the total temporal noise observed here. Limiting the discussion to the feedback loop, several elements are the origin of the shot noise: the sensing diode, the FB diode, and the feedback transistor. To simplify, one may assume that the contributions to the shot noise from the sensing and FB diodes are the same, since those elements are the same in the case of both investigated submatrices (with a standard transistor or a ELT in the feedback loop). Due to the enclosed geometry, the

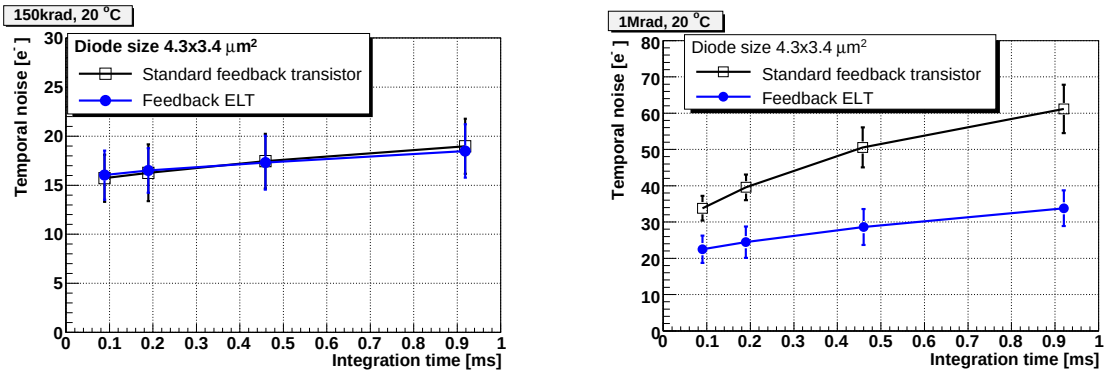


Figure 5.15: Temporal noise as a function of integration time for standard and enclosed-layout feedback transistors. Measured at +20 °C after the accumulation of the ionizing dose.
Left: after irradiation up to 150 krad.
Right: after irradiation up to 1 Mrad.

feedback transistor used in the architecture S4 is less sensitive to ionizing radiation and by definition, it does not have a lateral transistor, which is a weak point in standard designs. Since the leakage current between the drain[5] and source of enclosed-layout transistor is limited, the shot-noise contribution of this transistor to the temporal noise is less significant than the noise contributed by the standard transistor used in the architecture S5.

- **At a temperature of -10 °C, the temporal noise becomes independent of the transistor type used in the feedback loop.** In this temperature range, the leakage current is significantly suppressed. Consequently, the contribution of the shot noise originating from any leakage current is insignificant. The contributions from other noise sources independent of the transistor type used in the feedback loop become dominant.

- **At negative temperatures, the temporal noise of the pixels with integrated amplification and CDS is significantly larger than the noise from pixels with simple in-pixel architectures (MIMOSA-11).** Even by cooling the sensor down to negative temperatures, the temporal noise cannot be recovered to the values observed before irradiation as is possible with the sensors with simple in-pixel architectures. This observation suggests that in the in-pixel architectures with signal processing, there is some radiation-induced noise source which does not manifest itself as strongly in simple in-pixel architectures. The source of this noise remains unknown.

Overall, at the temperatures above -10 °C, the presence of the ELT in the feedback loop yields to a lower temporal noise after sensor irradiation. Implementation of this transistor type in the

[5]The feedback transistor is in a diode configuration and therefore its drain and gate are shorted.

feedback loop seems to be a good choice to improve the sensor performance if efficient cooling cannot be supplied.

5.4.5 Tests on subarrays with smaller diodes - tests of the influence of feedback-transistor type and geometry on the noise performance

The contribution of the feedback-transistor type and geometry to the temporal-noise increase after irradiation was assessed under the same conditions as mentioned in the previous section. The temporal noise of the subarrays containing smaller diodes (listed in Table 5.4) was investigated for ionizing doses of up to 1 Mrad. The results are depicted in Figure 5.16. The noise increase for the design utilizing the ELT in the feedback loop is reduced if compared to the noise observed for the architectures called ”weak” and ”strong”, which feature the standard transistor in the feedback loop. There is also a clear dependence of temporal noise on the geometry of the feedback transistor. The highest temporal noise was observed for an architecture where the ”strong” transistor was implemented in the feedback loop. This transistor has a very short but wide channel. It cannot be excluded that for the same threshold voltage, the lateral parasitic transistors accompanying the ”strong” transistor conduct more leakage current after irradiation than the parasitic transistors of the ”weak” transistor. In such a case, the larger leakage current of the ”strong” transistor translates into the larger shot noise, which contributes to the total temporal noise observed for these pixels.

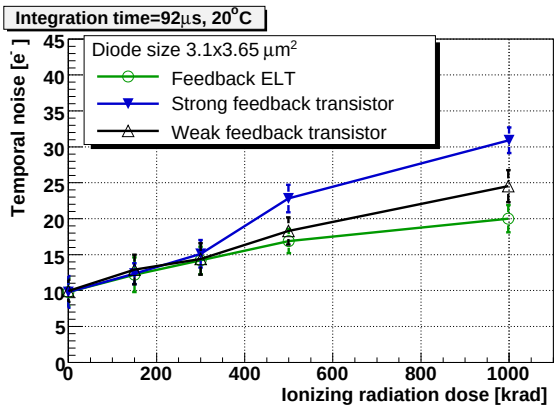


Figure 5.16: Temporal noise as a function of ionizing dose for the three investigated feedback transistors (”weak”,”strong”, and ELT) implemented in MIMOSA-22bis. Data were taken at +20 °C with an integration time of 92 μs.

5.4.6 The influence of the input-transistor and load-transistor geometry on the in-pixel amplifier performance after irradiation

The noise performance of an amplifier depends on its operation point. Due to radiation effects, which modify the transistor threshold voltage, the operation point may change in an unfavorable way. The noise performance of an irradiated amplifier may be improved by compensating the amplifier bias point. This can be achieved by modifying the DC potential transferred to the input transistor via the feedback loop. Such a modification can be done by changing the initial value of the transconductances for the load and the input transistors,

thus changing the current flowing through them. The influence of the geometry (W/L) of both transistors on the amplifier noise performance after irradiation was addressed within MIMOSA-22bis.

Table 5.6 presents the variations of the tested in-pixel architectures. All these architectures originated from the "BASE" architecture which has the following size parameters for the investigated transistors: the load transistor W/L=0.6 µm/22.5 µm, the input transistor W/L=1.85 µm/0.35 µm, and the feedback transistor W/L=0.4 µm/1.5 µm. Next, one (or more) of the investigated transistors was changed with respect to the "BASE" architecture. For example, the architecture called "ITS" (Input Transistor Strong) featured feedback and output transistors the same as the "BASE" architecture, while the input transistor was changed to a so-called "strong" (with W/L=2.8 µm/0.35 µm). The architecture called "FELT_ITW_LTS" (Feedback ELT, Input Transistor Weak, Load Transistor Strong) featured feedback-loop transistor as well as load transistor and input transistor changed with respect to the "BASE" architecture according to the dimensions W/L given in Table 5.6.

Table 5.6: The input, load, and feedback transistors transconductance modification.

Name used	Description	Transistor dimension W/L [μm]
BASE	Basic architecture. Except the sensing-diode size (here 3.1×3.65 µm^2), this architecture is equivalent to the one with the "standard" feedback transistor described before.	Input 1.85/0.35 Load 0.6/22.5 Feedback 0.4/1.5
ITS	Input Transistor Strong	2.8/0.35
ITW	Input Transistor Weak	1.05/0.35
LTS	Load Transistor Strong	0.6/18.5
LTW	Load Transistor Weak	0.4/22.5
FELT	Feedback Enclosed-Layout Transistor	4.4 / 0.35
Variations tested [a]	ITS, ITW, FELT_ITS, FELT_ITW, LTS, LTW, FELT_LTS, FELT_LTW, ITS_LTS, ITS_LTW, ITW_LTS, ITW_LTW, FELT_ITS_LTS, FELT_ITS_LTW, FELT_ITW_LTS, FELT_ITW_LTW	

[a] For example, ITS → means that in this test architecture, the input transistor was changed from base to ITS version (ITS - Input Transistor Strong) and the other transistors (the load and the feedback) are the same as in BASE architecture. FELT_ITS → corresponds to the architecture with a Feedback Enclosed-Layout Transistor (FELT) and an input transistor is ITS.

The performance of all amplifiers listed in Table 5.6 was investigated at room temperature after sensor irradiation to 1 MRad. Figure 5.17 shows the mean values of the temporal noises. To enhance the differences in the performance of the studied in-pixel architecture variations,

the presented results were obtained for a relatively long integration time of ∼0.92 ms (10 times the nominal integration time of the sensor).

One can observe that the temporal noise depends mainly on the type of transistor used in the feedback loop. All architectures hosting the ELT in the feedback loop had a lower noise than those each equipped with a standard transistor. The best observed performance was achieved with the strong input transistor and strong load transistor. In contrast, the worst results were observed for the architectures with input and load transistors called "weak". The differences observed for an integration time of 0.92 ms were almost nonapparent when the sensor was later run at an integration time corresponding to its nominal frequency, namely, 92 µs. Under these conditions, the input-transistor and the load-transistor geometries had only a marginal effect on the pixel performance after irradiation.

The performance after irradiation of the in-pixel architectures with signal processing was indeed improved by implementing the ELT in the feedback loop. However, more development is needed to meet the radiation-tolerance requirements of the most demanding experiments (e.g., the CBM experiment). For ionizing doses exceeding 300 krad, the noise level of current sensors with column-parallel readout architecture is still too high for efficient particle detection. Since the modifications of the input and load transistors did not bring any visible advantage, further improvement must thus come from other components besides the feedback, load, and input transistors.

5.4.7 Further improvements towards a better ionizing radiation tolerance – MIMOSA-22ter

A new prototype named MIMOSA-22ter (depicted in Figure 5.18) addresses several aspects related to the influence of the in-pixel circuit elements on the overall sensor performance. The first aspect is related to the efficiency of parasitic-signal filtering by the feedback capacitance (C). Another aspect addresses the tolerance to radiation of the forward-biased diode (FD). Finally, the amplifier (A) and the clamping capacitance (Clamping) influences on the temporal noise were further investigated. All the mentioned aspects addressed with MIMOSA-22ter are briefly described in the following text.

If the excessive temporal noise originates from poorly filtered parasitic signals approaching the amplifier input, an improvement after irradiation is expected from the design with an increased feedback capacitance (C). Increasing this capacitance will indeed increase the low-pass filter time constant. Moreover, there might be a noise contribution originating from the fact that the in-pixel amplifier is switched on only during the short period of time needed to read out the pixel. The increase in the feedback loop capacitance could lead to the more efficient filtering of the noise related to the power supply fluctuations.

On the other hand, too large feedback capacitance brings the risk that a memory effect will be enhanced by a larger time constant of the low-pass filter. Also, the implementation of a capacitance that is, for example, one order of magnitude larger than the one used in MIMOSA-

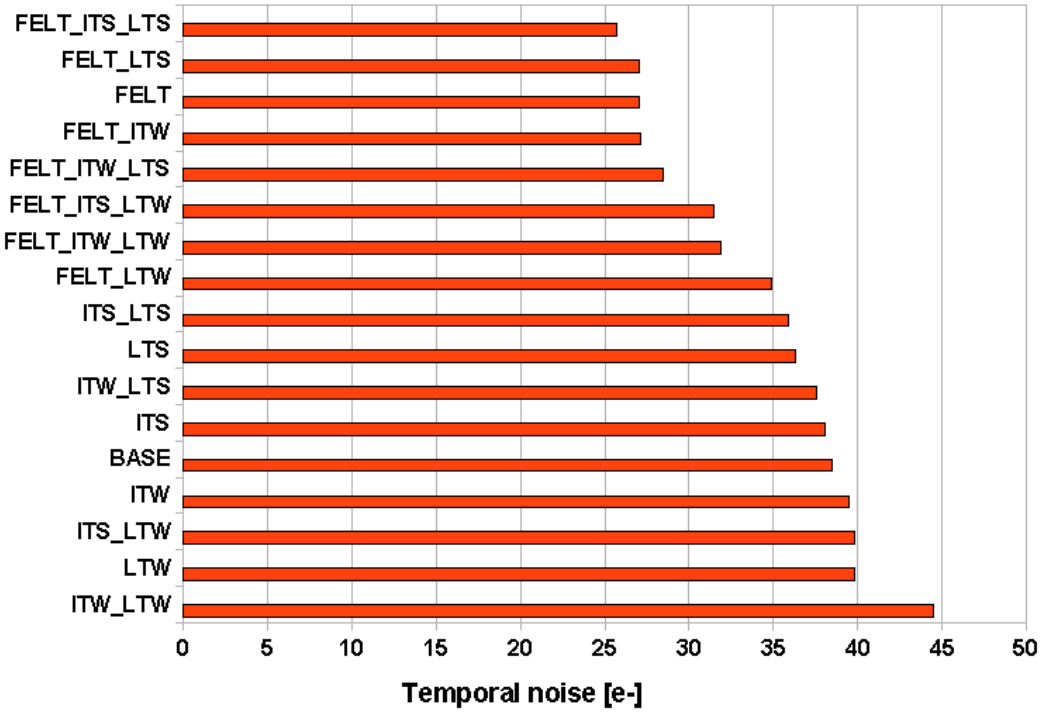


Figure 5.17: Influence of the geometry of the input transistor and load transistor on the amplifier performance after irradiation to 1 Mrad. Data taken at room temperature and at an integration time of ∼920 µs. These operating conditions were chosen to enhance any possible differences in the architecture performance. The meaning of all abbreviations can be found in Table 5.6.

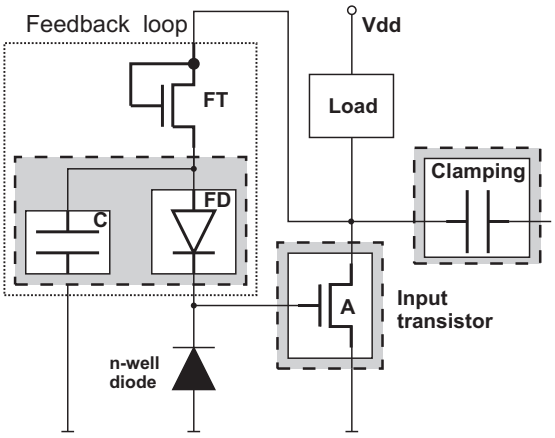


Figure 5.18: Diagram of the in-pixel elements investigated with the MIMOSA-22ter prototype.

22 is not really beneficial since it would call for too pixel pitch.

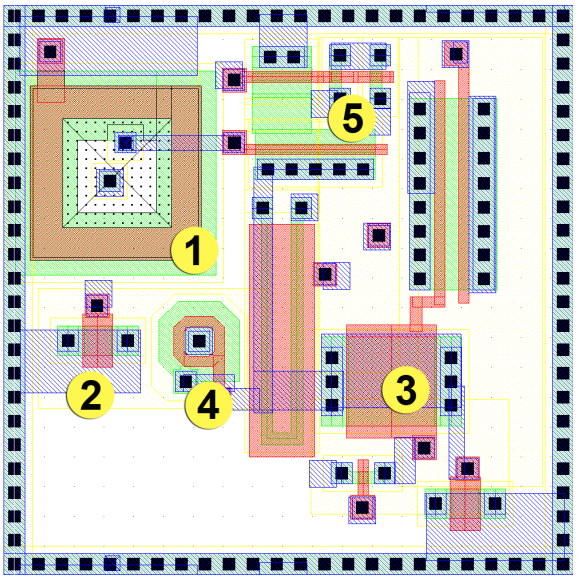
Therefore, to verify the influence of the feedback capacitance on the noise performance, a feedback capacitor of ∼20 fF was implemented. This capacitance is approximately three times as large as that of the previously implemented in MIMOSA-22/22bis. MIMOSA-22ter is also hosts pixels with ∼7 fF feedback capacitance for comparison. Figure 5.19 shows pixel layouts equipped with ∼7 fF feedback capacitance (a) and ∼20 fF (c) (compare the elements labeled (2)).

The excessive temporal noise mentioned previously may also originate from components not related to the amplifier input circuitry. In this case, the noise contribution would be added after signal amplification. To ensure a better separation between the signal and noise, an amplifier (A) with a higher gain could be implemented. The simplest solution which could be applied, regarding the limited space inside the pixel consists of equipping an already tested in-pixel amplifier with an additional transistor to build a cascode amplifier. Such a solution was implemented within MIMOSA-22ter, where the mentioned cascode amplifier has an AC gain ∼2 times larger than the common-source amplifier used previously in MIMOSA-22/22bis. The layouts of pixels with a common-source amplifier and a cascode amplifier are shown in Figure 5.19 (a) and (b), respectively.

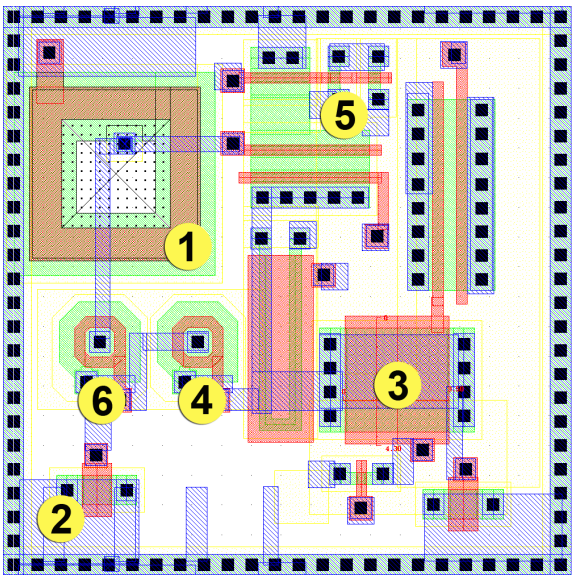
Attention was also given to the forward-biased diode, ensuring a constant bias for the sensing diode and compensating its leakage current, as shown in Figure 5.20(a). This diode is usually made of the high-doped p-type-silicon implant on the top of the n-well diode, as shown in Figure 5.20(b). The functionality of this diode could be also provided by an ELT working in a diode configuration. In order to maximize the radiation tolerance, such a transistor should be implemented so that its inner part is connected to the sensing diode. Its gate an outside part should be shorted together and connected to the feedback transistors, as illustrated in Figure 5.20(c).

The clamping capacitor adds kTC noise to the output signal (see Appendix A.1). In order to check whether the clamping capacitor (Clamping) shown in Figure 5.18, could have an impact on temporal noise, three subarrays with different clamping capacitors were implemented within MIMOSA-22ter. The reference architecture, which is identical to the one implemented in MIMOSA-22bis ("weak" - see Section 5.4), contains a clamping capacitance of ∼100 fF. Two other submatrices contain a clamping capacitance with the following values: ∼40 fF and ∼60 fF. The differences in the pixel layouts equipped with 40 fF and 60 fF clamping capacitors are shown in Figure 5.19 a) and c). The use of smaller clamping capacitances brings a risk of an increased FPN.

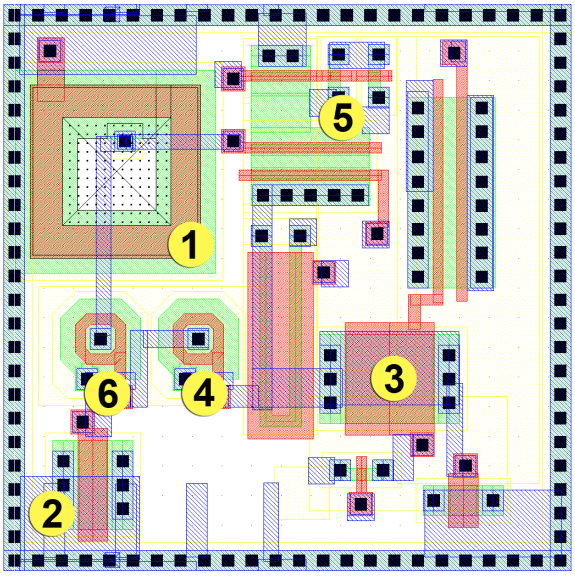
The architecture of the MIMOSA-22ter prototype, including the in-pixel amplifier equipped with a negative feedback loop, was based on the previously presented MIMOSA-22 (see also Figure 5.6 in Section 5.3). The new prototype was fabricated in the fall of 2009. The influence on the temporal noise of the in-pixel elements addressed with MIMOSA-22ter was studied after exposing the device to ionizing radiation. Those studies are not within the scope of this thesis



(a) Standard (MIMOSA-22/22bis) feedback filter capacitor ∼7 fF, clamping capacitor ∼40 fF, common-source amplifier.



(b) Standard (MIMOSA-22/22bis) feedback filter capacitor ∼7 fF, clamping capacitor ∼60 fF, cascode amplifier.



(c) Enlarged feedback filter capacitor ∼20 fF, clamping capacitor ∼40 fF, cascode amplifier, ELT working in the forward-biased diode configuration.

Figure 5.19: Pixel layouts of the MIMOSA-22ter prototype. (1) Sensing diode, (2) feedback low-pass filter capacitor, (3) clamping capacitor, (4) feedback transistor, (5) in-pixel amplifier, and (6) ELT working in the forward-biased diode configuration.

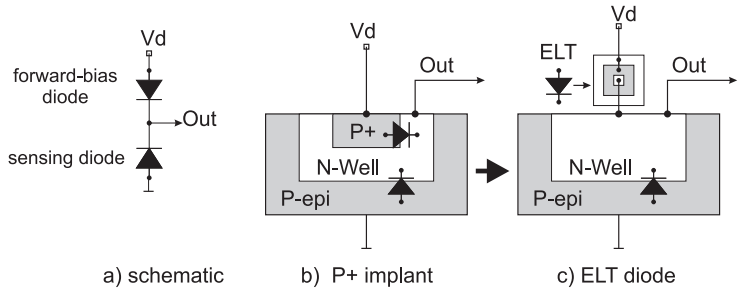


Figure 5.20: Two possible implementations of the SB pixel: (a) schematic of a simplified in-pixel architecture, (b) forward-biased diode p+/n-well, (c) the use of ELT in a diode configuration.

work and they will not be described here in detail. However, some of the observations are worth to mentioning here for completeness [99].

Several samples of the new prototype were irradiated up to 300 krad and studied under the same conditions as MIMOSA-22/22bis. The excessive temporal noise observed for the two previous MIMOSA-22-like prototypes was also observed for all irradiated MIMOSA-22ter samples. The results suggest that the modification of the clamping and feedback capacitances in a small range around their default values, does not give any visible advantage neither before nor after irradiation. The same conclusions were made for the forward-biased diode whether implemented as a p+ implant or as a transistor working in diode configuration.

As expected, some improvement was achieved with the architectures featuring the in-pixel amplifier implemented in a cascode configuration. Despite the larger thermal noise and increased FPN (see Section 4.1.4.2), this type of architecture exhibited the best SNR before and after irradiation. However, the implementation of the cascode amplifier did not improve significantly the sensor ionizing radiation tolerance.

Summarizing, the ionizing-radiation tolerance of sensors with in-pixel signal processing was not improved with MIMOSA-22ter to the required level. The sensor is still too sensitive to ionizing radiation, resulting in an excessive temporal noise. The origin of this noise has not yet been determined, even though the influence of all in-pixel elements was studied carefully.

Further studies should focus on reconsidering several details of the in-pixel architecture, including the steering and clock signals, the layout, and so on. One should keep in mind that the MIMOSA-22-like sensors feature a readout allowing the samples subtraction of two sample signals to remove low-frequency components.[6] However, the level of correlation between the two samples is not precisely known. This level of correlation should also be the subject of further investigations.

Another aspect worth addressing in the future concerns the 1/f noise, never studied for the CMOS sensors developed at the IPHC-Strasbourg. This low-frequency noise component should be suppressed, at least to some extent, by the CDS. However, the efficiency of this suppression depends on the initial value of the noise. The CDS behaves like a high-pass filter,

[6] Frequency below $1/t_{integr}$.

with an illustrative frequency response shown in Figure 5.21 (blue line). The CDS filter has a cut-off frequency fc equal to 1 over an integration time ($fc = 1/T_{integration}$). In the same figure, hypothetical 1/f-noise frequency spectra are shown for two cases: before (black) and after (red) irradiation[7]. One can observe that the 1/f-noise frequency spectrum changes its amplitude and slope in such a way that this type of noise is no longer filtered efficiently by the CDS high-pass filter. It cannot be excluded that this type of noise, originating from multiple sources of investigated in-pixel architectures, might significantly impact the sensor performance after irradiation.

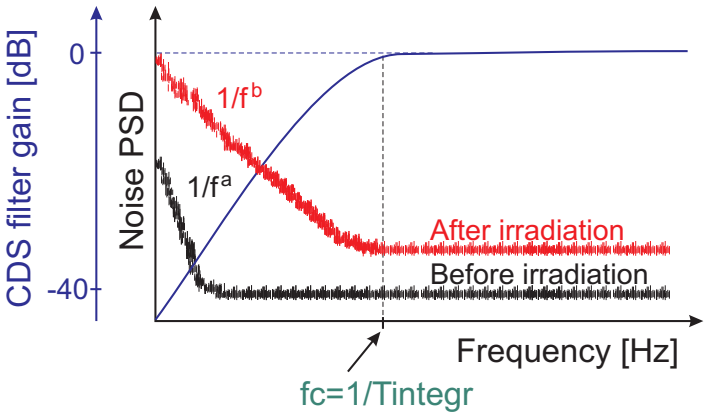


Figure 5.21: 1/f-noise frequency spectrum before (black) and after (red) irradiation compared with the frequency response of the CDS, acting as a high-pass filter (blue) with a cutoff frequency of fc=1/Tintegr. The amplitude of the 1/f noise as well as the 1/f slope may change significantly after irradiation. Therefore, some of 1/f components may not be sufficiently suppressed by the CDS operation and contribute to the temporal noise.

5.5 First large-scale chip with a column-parallel architecture and data sparsification – MIMOSA-26

The first full-scale sensor with zero-suppressed binary output, MIMOSA-26, was developed in the framework of the EUDET project [15]. This sensor was intended for incorporation in a high-resolution beam telescope. MIMOSA-26 will also serve as a baseline for the vertex detectors of several experiments, for example, the STAR Heavy Flavor Tracker upgrade and the CBM-MVD (prototyping phase).

The upstream part of the signal detection used in MIMOSA-26 has already been validated with the two sensor prototypes described previously: MIMOSA-22 and MIMOSA-22bis. The testability of the MIMOSA-26 architecture is better than that of the MIMOSA-22-like sensors. The on-chip programmable bias, voltage references, and the selection of the test mode are set via a JTAG controller. Each pixel of MIMOSA-26 can be read out in analog and digital mode. The analog mode allows accessing the analog signals applied to the discriminator inputs. The

[7] This hypothetical 1/f noise frequency spectrum and the CDS filter frequency response were plotted based on literature, e.g., [135, 136].

second mode allows reading out a discriminated information. The discriminator outputs are later connected to a zero suppression logic.

The data sparsification in MIMOSA-26 is implemented as follows: The analog signal from the pixels is converted to 0/1 code by means of discriminators at the end of each column. An impinging particle manifests itself as a cluster of neighboring pixels with a signal above the discriminator threshold level. Figure 5.22 presents a digital matrix frame with some hits inside. A group of consecutive pixels inside a row which are above the threshold value, are encoded as a so-called *state*. Each state consists of the 10-bit address and the 2-bit binary code. The 10-bit address stands for the column in which the first pixel belongs (marked as black). The 2-bit binary code tells how many pixels with a signal above the threshold immediately follow the "first" pixel.

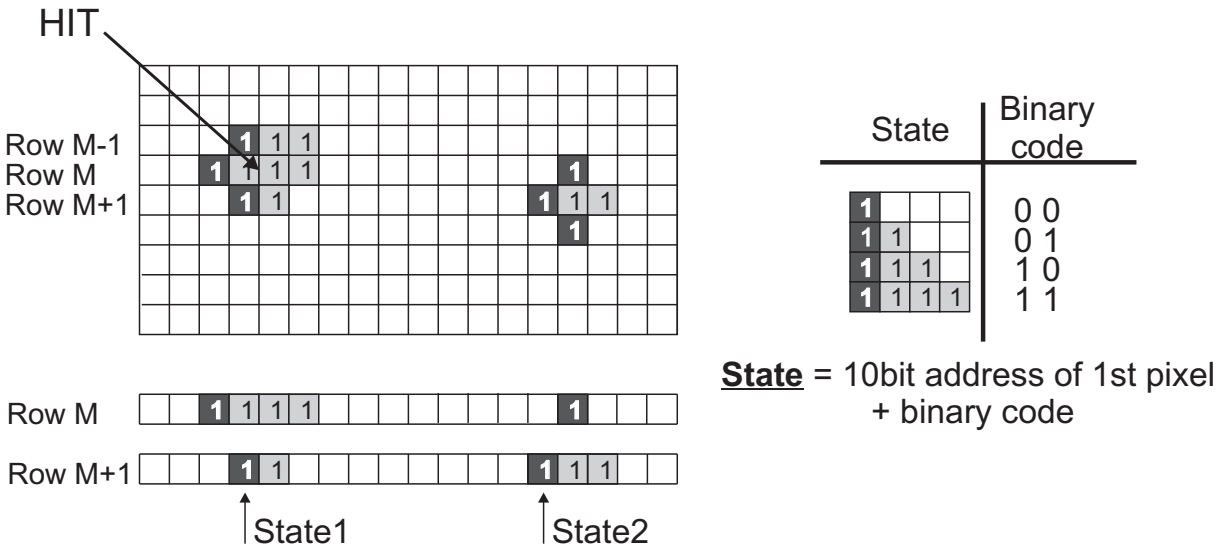


Figure 5.22: Simplified illustration of the data sparsification implemented in MIMOSA-26. This figure presents a digital matrix frame with some hits inside. An impinging particle manifests itself as a cluster of neighboring pixels with a signal above the discriminator threshold level ("1"). A group of consecutive pixels inside a row which are above the threshold value are encoded as a so-called state. Each state consists of the 10-bit address and the 2-bit binary code. The 10-bit address stands for the column in which the first pixel belongs (marked as black). The 2-bit binary code tells how many pixels with a signal above the threshold immediately follow the "first" pixel.

The zero-suppression logic is based on a Priority Look Ahead (PLA) algorithm which allows pixels above the threshold in a given row to be found. The data sparsification logic and the algorithm were validated with the SUZE-01 prototype chip fabricated in the AMS C25B4C3 CMOS 0.35-µm technology. More details about the PLA and SUZE-01 can be found in [157].

The first MIMOSA-26 prototypes arrived from the foundry in February 2009. Extensive tests were performed in the laboratory and with a high-energy pion beam. The performance observed for MIMOSA-26 was almost identical to the performance of MIMOSA-22 and

MIMOSA-22bis, presented earlier in this chapter. Table 5.7 summarizes the performance parameters achieved.

Table 5.7: Performance of MIMOSA-26.

Sensor external dimensions	21.2×10.6 μm^2
Number of pixels	∼660 000
Readout time	$\leqslant$ 100 µs
Power consumption	∼300 mW/cm^2
Non-ionizing radiation tolerance	few 10^{12} n_{eq}/cm^2
Ionizing radiation tolerance	∼300 kRad
Pixel pitch	18.4 µm
Single point resolution	∼3 µm
Material budget per sensor	0.05 $\%X_0$

5.6 Conclusions and summary

This chapter presented the radiation tolerance studies carried out with CMOS sensors featuring the column-parallel architecture, fabricated in a 0.35-µm process.

The ionizing-radiation tolerance of sensors with signal processing circuitry inside the pixel was assessed for the first time for MIMOSA-22. Three types of in-pixel amplifier architectures were investigated. The FPN was observed to remain unchanged after sensor irradiation up to several hundreds of krad, but only for the architectures featuring a negative feedback loop. This architecture was found to perform best.

The performance of sensors exposed to ionizing radiation was observed to start degrading significantly after 300 krad. Above this dose, the ϵ_{det} above 99%, and FH_{rate} below 10^{-4} were difficult to achieve. The ionizing radiation tolerance was found to be limited by an excessive temporal noise. Based on previous studies, the increase in the temporal noise could not be attributed to an increase in the sensing-diode leakage current. The studies conducted to discover the potential sources of this noise concentrated on the in-pixel signal processing microcircuitry.

In order to determine the origin of this excessive noise, two different sensor prototypes were fabricated: MIMOSA-22bis and MIMOSA-22ter. MIMOSA-22bis addressed the influence of the feedback, input, and load transistors on the sensor performance after irradiation. MIMOSA-22ter investigated the properties of pixels with a modified amplifier, forward-biased diode, clamping and feedback capacitors.

Studies investigating the role of feedback transistor characteristics on the amplifier-noise performance were conducted to determine which components are particularly sensitive to ionizing radiation. Among the different variants considered for the feedback transistor, the use of the ELT was the most beneficial, especially for the highest doses, temperatures, and

integration times considered. The tolerance of this architecture to radiation was assessed up to 300 kRad. This value meets the requirements of the STAR experiment upgrade, the ILC experiment, and the EUDET telescope. However, this tolerance is still below the level required by the most demanding application, the CBM experiment.

Extensive studies addressing MIMOSA-22bis and MIMOSA-22ter found that all the in-pixel amplifier elements considered except the feedback transistor have a second-order effect on the noise performance after sensor irradiation. For all the sensors tested, the temporal noise was too high for the highest doses considered. Even today, the source of this noise is not well understood. Currently, the performance of the column-parallel CMOS sensors is limited by an SNR that is too low for ionizing doses exceeding 300 krad.

Studies carried out with various in-pixel architectures exposed to different ionizing radiation doses also showed that the temporal noise cannot be reduced efficiently by cooling. The temporal noise observed at 0 °C was only slightly lower than the one found at room temperature, and moreover, it reached a plateau at ∼+10 °C, where further cooling was no longer effective. This excessive temporal noise does not originate from leakage currents (shot noise) but from more complex in-pixel electronics.

There are still some aspects regarding the in-pixel architecture which have not yet been addressed. For example, due to space constraints, not all transistors implemented inside the pixels were ELTs. The 1/f-noise influence has not yet been studied. Also, due to space limitations, the in-pixel transistors were not protected by guard rings.

The 0.35-µm feature size of the process used for fabricating the column-parallel sensors studied in this chapter seems to be a factor that limits their ionizing radiation tolerance. The CMOS processes with smaller feature size are definitely more attractive for future MAPS development targeting higher tolerances to ionizing radiation and shorter readout times. These processes utilize more metal layers, allowing the improvement of interconnections. The parasitic capacitances of lines are smaller and allow for running the sensor with higher clock and steering signal frequencies. Moreover, processes with smaller feature size utilize thinner gate oxides, for example, reduced from ∼7 nm for the 0.35-µm process to about 4 nm for 0.18-µm technology. Due to this thinner gate oxide, the accumulation of net positive charge introduced by ionizing radiation is significantly suppressed and radiation-induced effects become less pronounced. Therefore, devices implemented in such technologies become significantly more tolerant to ionizing radiation. Moreover, a smaller feature size alleviates the space constraints and allows implementing more ELTs (each surrounded with a guard ring) inside the pixel. Summarizing, changing the fabrication process for the CMOS sensors will have a strong impact on their ionizing radiation tolerance.

The sensors investigated in this chapter are based on an EPI layer where the charge is transferred towards the sensing diodes by a thermal-diffusion process. Thus, the charge sharing between the neighboring pixels is relatively large, and finally, only a modest fraction of

the charge generated by an impinging particle is available on the seed pixel. As the excessive noise cannot be overcome, an improvement in the SNR could be achieved by increasing the signal available in the individual pixel. This can be done by using substrates with special features enhancing the charge collection. CMOS sensors based on such substrates were studied within the scope of this work. Those studies are reported in the following chapter.

6 Radiation-tolerance assessment of the different CMOS processes

The CBM experiment requirements regarding the sensors equipping the MVD are very demanding. The sensors should simultaneously provide a readout time of ∼30 µs, a tolerance to radiation of ⩾1 Mrad and few $10^{13}\ \mathrm{n_{eq}/cm^2}$, as well as a σ_{res} of 5 µm. To meet the requirements regarding the readout time, the architecture of the MAPS was changed to include the column-parallel readout with data sparsification. This operation increased the complexity of the in-pixel architecture. Consequently, the column-parallel sensors were less tolerant to ionizing radiation than the simple devices based on the 3T or the SB architecture (This is discussed in Section 5.3.2).

A good example of a sensor with improved readout time is MIMOSA-26, presented in Section 5.5. This sensor features 1024 columns and 576 rows, an 18.4-µm pixel pitch, and a 100-µs readout time. It will be used to equip the CBM-MVD prototype planned for 2012. The tolerance of this sensor to ionizing radiation was assessed to be ∼300 krad at room temperature[1]. This tolerance seems to be the limit that can be achieved with column-parallel MAPS implemented in the currently established AMS 0.35-µm process. The gate oxide of the 0.35-µm process is relatively thick compared to the one in technologies with smaller feature size. This makes the devices implemented in the AMS process intrinsically less tolerant to ionizing radiation. Moreover, due to the bigger feature size of the AMS process, standard radiation protection techniques cannot be used. There is not enough area in the pixel to implement proper guard-rings and to exchange the standard MOS transistors with ELTs.

It is natural for the development of MAPS to go towards processes with smaller feature size. This will most likely result in improved ionizing radiation tolerance, significantly increasing the probability of reaching the tolerance level required by the experiment. The readout time is predicted to decrease by 10-15% due to the lower parasitic capacitances present in processes with smaller feature sizes. Further readout time improvements that allow the CBM-MVD requirements to be met, can be achieved by reducing the column length of the sensor.

The change of the CMOS fabrication process to one with a smaller feature size will not automatically solve the problem of an insufficient non-ionizing radiation tolerance. In the currently available AMS 0.35-µm process, the baseline technology for MAPS development, this

[1]MIMOSA-26 features the in-pixel architecture of MIMOSA-22. The tolerance of this architecture to ionizing radiation was investigated in Chapter 5. For sensors with column parallel architectures, the tolerance to this kind of particles cannot be increased by cooling the sensors down.

tolerance depends predominantly on the pixel pitch. Sensors featuring pixel pitches of 10 μm or 20 μm achieved radiation tolerances of $1{\cdot}10^{13}\ \mathrm{n_{eq}/cm^2}$ and $2{\cdot}10^{12}\ \mathrm{n_{eq}/cm^2}$, respectively. Therefore, one can expect sensors like MIMOSA-26, featuring a pixel pitch of 18.4 μm, to withstand no more than a few $10^{12}\ \mathrm{n_{eq}/cm^2}$. The pixel pitch in the case of column parallel sensors cannot simply be reduced in order to achieve better radiation tolerance. There are at least several reasons for this:

- There would be no space in the pixels with reduced pitch to accommodate signal processing microcircuits.
- Reducing the pixel pitch is not practical because it would lead to an increase in the integration time. For example, reducing the pixel pitch from 20 μm to 10 μm and preserving the same column length (e.g., 1 cm) increases the integration time by a factor of 2.
- More pixels means more power consumption, which requires a very efficient cooling system to dissipate the heat. Such cooling would introduce an additional material budget to the experiment.

Since reducing the pixel pitch will not bring any rational benefits in the long term, another way to improve the non-ionizing tolerance had to be found. The main limitation of MAPS in terms of non-ionizing tolerance is the undepleted sensitive volume. The charge transfer from the bulk to the sensing implants occurs predominantly due to thermal diffusion. Therefore, the aim of this thesis is to investigate specific features of CMOS technologies that could offer different charge-transport mechanisms of a charge transport, for example, like the mechanism existing in the fully depleted HAPS discussed in Chapter 3.2. The latter involves charge transport inside a built-in electric field, which has the following advantage. The charge spread is limited because the charge movement is not stochastic but is mostly focused in a certain direction instead. Consequently, signal electrons do not migrate through a substantial amount of sensitive volume and the probability that they will interact with radiation-induced traps decreases. The above mentioned mechanisms lead to an increase in the signal charge collected by a seed pixel, thus, to an increase in the SNR, which predominantly governs sensor performance.

Unfortunately, depleting the sensitive volume of MAPS based on a low-resistivity EPI layer is impossible. Due to certain technological limits, the diode voltage cannot be increased above a few volts for standard CMOS processes. The other option would be to use a high-resistivity substrate. In this case, an N-well—p-EPI junction is formed between high-doped n-well and low-doped p-EPI. Such an EPI layer could most likely be partially depleted even at standard CMOS voltages. However, when I started this thesis work, the high-resistivity substrate was not available in CMOS processes.

A similar charge-transport-enhancement effect due to an electric field could be obtained by implementing a graded doping into the EPI layer. This graded doping profile leads to

the formation of an electric potential that could drag electrons more efficiently towards the sensing diodes. This postulate was proven by a simulation performed with ISE-TCAD [158]. The graded EPI used in this thesis research was manufactured by a commercial vendor[2] using a 0.25-µm BiCMOS[3] process. Studies aiming to unravel the potential of this technology for particle tracking will be discussed in this chapter.

With time, the need for industry to improve the performance of photo-detecting elements initiated the development of CMOS processes with a feature particularly interesting for MAPS development – a high-resistivity EPI layer. One of the first available technologies capable of producing such an EPI layer was the 0.6-µm XFAB CMOS process with a so-called PIN option[4] [159]. Despite its large feature size, this technology was found to be very promising for improving the tolerance of MAPS to non-ionizing radiation. The first MAPS featuring depleted sensitive volume were manufactured during the course of this thesis. Studies on the first prototype of such sensors, called later MIMOSA-25, will be discussed in this chapter after discussing the BiCMOS technology.

Finally, in the near future, a high-resistivity EPI layer should be available for 0.35-µm technology provided by XFAB[5]. Due to its smaller feature size, this process would allow more elements to be fitted on the same surface. Consequently, the sensors with column-parallel readout, like the MIMOSA-26 sensors, could be reproduced with a new technology based on depleted sensitive volume. Unfortunately, this process was not yet available during the time when this thesis work was being conducted. To verify whether the currently existing XFAB 0.35-µm line (despite its low-resistivity epitaxial layer) can provide the parameters required for particle tracking, it was relevant to study the performance and the radiation tolerance of this process. This chapter will present studies performed with the sensor prototype MIMOSA-24, manufactured in the XFAB 0.35-µm process. The performance of this sensor will be compared to that observed for sensors featuring similar in-pixel architectures but implemented in the AMS 0.35-µm technology.

In the following sections, systematic studies on the radiation tolerance of all technologies mentioned above are presented. Table 6.1 summarizes their main features.

[2]The vendor name may not officially appear in this document.

[3]BiCMOS is an evolved semiconductor technology that integrates two formerly separate semiconductor technologies - that of the analog bipolar junction transistor and the technology of the digital CMOS transistor - in a single integrated circuit device.

[4]The PIN option allows the design of so-called "PIN" diodes. The abbreviation "PIN" is related to the diode construction. The diode is formed as a p-n junction with intrinsic silicon between p- and n- doped regions. In the investigated XFAB 0.6-µm CMOS process, the p- region is formed by the highly doped substrate (p+). The region of intrinsic silicon corresponds to the low-doped (high-resistivity) EPI layer (p-). The n- region is implemented as an n-well diode (n+). Finally, the PIN diode is composed of p+ p- n+ materials.

[5]Such a statement was made during a discussion with the vendor.

Table 6.1: The three CMOS processes investigated in order to improve the radiation hardness.

Process	Vendor	EPI thickness	EPI resistivity	Prototype
0.25-µm BiCMOS	— [a]	∼9 µm	graded	MIMOSA-21bis
0.6-µm CMOS [b]	XFAB	∼15 µm	∼1 kΩ·cm	MIMOSA-25
0.35-µm CMOS	XFAB	∼14 µm	∼10 Ω·cm	MIMOSA-24

[a] The vendor name may not officially appear in this document.
[b] The official name of this process: the XFAB 0.6-µm CMOS process with PIN option.

6.1 Radiation tolerance of the 0.25-µm BiCMOS process with a graded EPI layer

The need for new technologies suitable for MAPS production triggered investigations regarding the BiCMOS process [160] with a feature size of 0.25 µm. The interesting aspect of this technology is the non-uniform doping profile of the EPI layer. The dopant concentration gradually increases from the wafer surface to the substrate. This doping profile is called "graded". This non-uniform doping concentration is expected to result in the internal buildup of an electric field in the EPI layer. Consequently, the charge collection in the EPI layer should be enhanced. This would be very beneficial during sensor exposure to non-ionizing radiation. The traps created inside the EPI by non-ionizing radiation have a certain probability of trapping the signal electrons. This probability decreases as the signal charge velocity increases. As the latter is expected to be increased by the graded EPI profile, the trapping probability should decrease and more signal electrons are expected to reach the collecting diodes. The sensors should become more robust to non-ionizing radiation.

The BiCMOS technology uses additional process steps related to the implementation of bipolar transistors. The cross-section of a device implemented in this process is shown in Figure 6.1. Deep n- (or p-) type implants forming the collector, emitter, and base of a bipolar transistor, are achieved in the BiCMOS process by ion implantation, or by using buried layers. In the case of the investigated BiCMOS process, the second option is applied. Such deep implants are also interesting for MAPS development. The n-type-buried layer located underneath the n-well, may increase the depth of the collecting diode, thereby improve the charge collection. On the other hand, such a deep implantation of the sensing element may lead to an increase in the parasitic capacitances of the sensing diodes. Together with the implantation of the n-type-buried layers, the p-type-buried layers are also implemented. There is a risk that the p-type-buried layers may screen the sensing diodes and limit, or even prevent, the charge collection from the sensitive volume.

The potential of the BiCMOS process based on a graded EPI layer was studied with the sensor prototype called MIMOSA-21. Studies related to this sensor are discussed in the following.

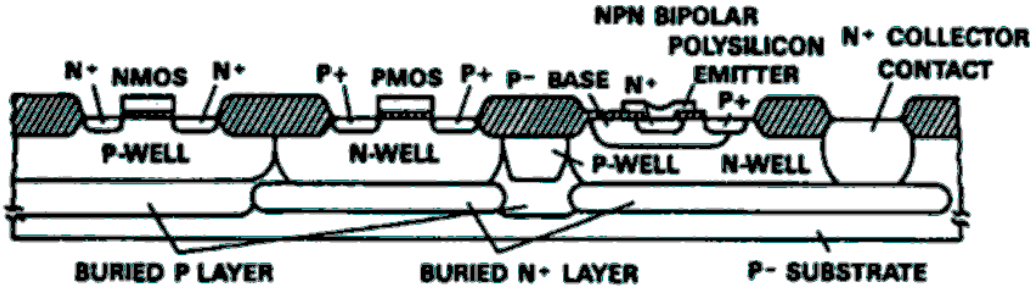


Figure 6.1: Cross-sectional view of the BiCMOS process (from [160]).

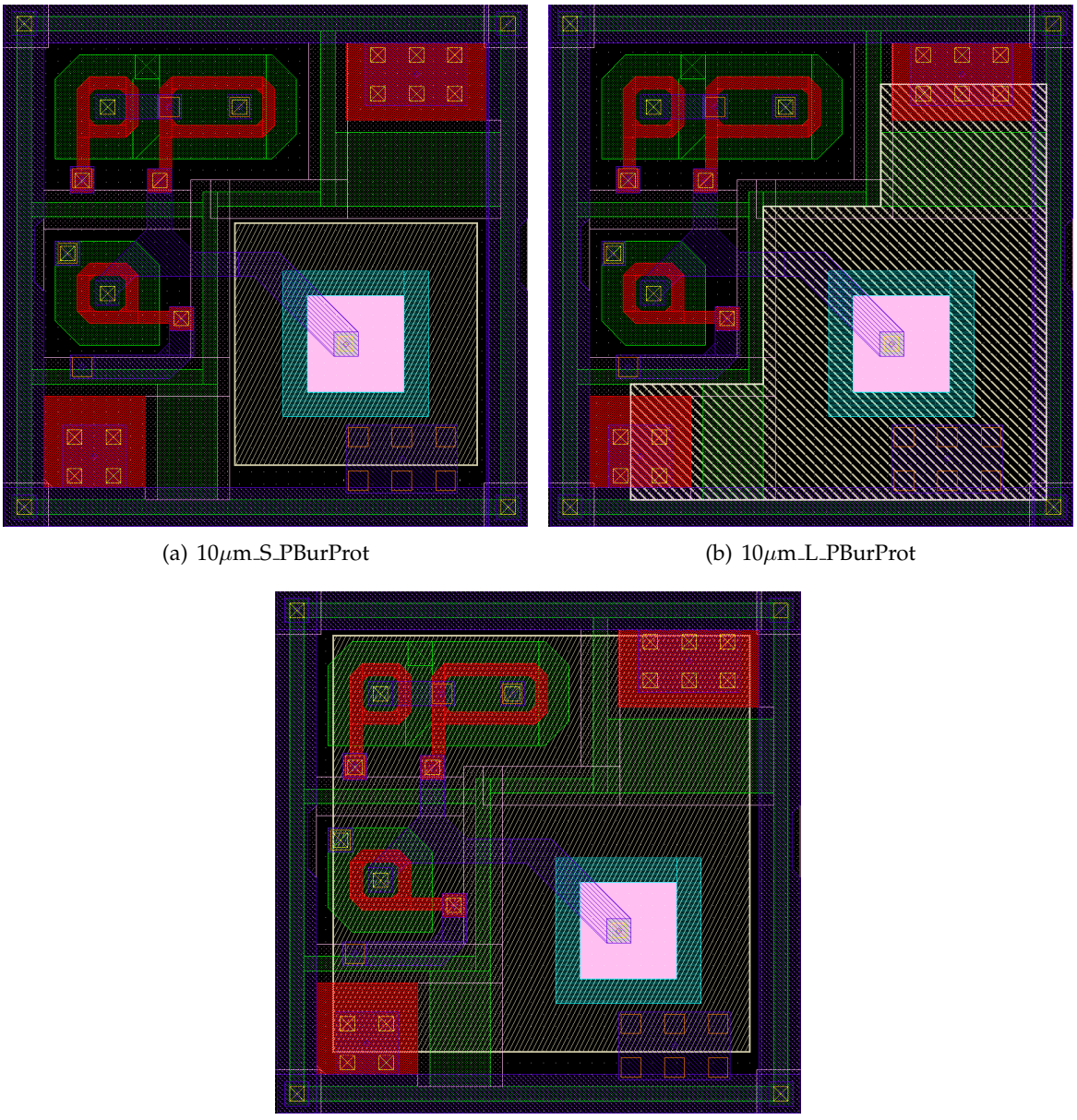
6.1.1 The sensor prototype based on a graded EPI layer – MIMOSA-21bis

The MIMOSA-21bis sensor was produced in two versions: A and B. The A version features standard (non-radiation-tolerant) diodes of 2×2 μm^2 in size. This version made it possible to investigate the influence of the p-type-buried regions on the charge collection. The p-type-buried-layer extent was controlled (i.e., limited) during the design process by the so-called p-type-buried-layer exclusion[6]. MIMOSA-21bis A had three different sizes of the p-type-buried-layer exclusion, as shown in Figure 6.2. The pixels named *10μm_PBurProt_S* had the smallest (4×4 μm^2) p-type-buried-layer exclusion, and the p-type-buried layer was implemented relatively close to the sensing diodes (Figure 6.2(a)). The p-type-buried-layer exclusion covering the full pixel area, except the transistors, was explored with *10μm_PBurProt_L* pixels (Figure 6.2(b)). Next, the p-type-buried-layer-exclusion zone was extended further to nearly the full pixel size in the *10μm_PBurProt_XL* pixels (Figure 6.2(c)).

The MIMOSA-21bis B sensor was designed with the goal of exploring different versions of the sensing diodes and increasing the ionizing radiation tolerance. For example, the *10μm_S_PBurProt_A* pixel is composed of a radiation-tolerant diode similar to the ones already implemented in the AMS 0.35-μm process (see 4.3). Table 6.2 summarizes the main features of both MIMOSA-21bis versions.

Due to the design constraints related to the MIMOSA-21bis readout, the maximum operating frequency for this sensors was 1.25 MHz. Both MIMOSA-21bis versions contained two matrices with different pitch sizes of 10 μm and 20 μm. There were 24576 pixels for each of the subarrays with a 10-μm pitch size. The subarrays with a pitch size of 20 μm contained 6144 pixels. Despite the different number of pixels, the integration time of ∼20 ms was kept equal for both subarrays.

[6]In the areas not covered by the "p-type-buried-layer exclusion", the p-type-buried silicon (p++) was implemented.



(a) 10μm_S_PBurProt

(b) 10μm_L_PBurProt

(c) 10μm_XL_PBurProt

Figure 6.2: Three pixels implemented in MIMOSA-21bis A in order to explore the influence of a p-type-buried silicon layer surrounding the sensing diodes. The p-type-buried silicon is everywhere except areas enclosed by the white line. (Color code: red–polysilicon; blue–metal; green–diffusion; light-pink rectangular shape–sensing diode).

Table 6.2: Description of pixels implemented in the A and B versions of MIMOSA-21bis.

Chip	Pixel design name	Pitch [μm]	Diode size [μm^2]
MIMOSA-21bis A (standard diodes)	10μm_S_PBurProt	10	2×2
	10μm_L_PBurProt	10	
	10μm_XL_PBurProt	10	
	20μm_L_PBurProt	20	
	20μm_XL_PBurProt	20	
MIMOSA-21bis B (radiation-tolerant diodes)	10μm_L_PBurProt_A	10	2.6×2.6
	10μm_L_PBurProt_B	10	3×3
	10μm_L_PBurProt_C	10	3×3
	10μm_L_PBurProt_D	10	3×3
	20μm_L_PBurProt_A	20	2.6×2.6
	20μm_L_PBurProt_E	20	2.6×2.6
	20μm_L_PBurProt_F	20	2.6×2.6

6.1.2 Sensor calibration with an ^{55}Fe source

In the first step of the BiCMOS process investigation, the basic sensor parameters (the parasitic pixel capacitance, the leakage current, and the temporal noise) were studied. The measurements were performed at 20 ^{o}C and a 1.25-MHz clock frequency, resulting in an integration time of 20 ms.

Table 6.3 shows the measured values of the pixel capacitances, temporal noise, and leakage currents for both MIMOSA-21bis A and B versions. The values of the parasitic capacitances measured for the sensing diodes implemented in MIMOSA-21bis A were nearly the same. This reflects the fact that all the pixels implemented in MIMOSA-21bis A had identical sensing diodes. Instead, the leakage current seems to depend on the pitch size and the p-buried exclusion area (see Figure 6.2). An investigation of the designs with the same pitch size showed that the highest leakage current was observed for the pixel with the largest p-type-buried-layer exclusion (XL). The lowest leakage current was observed in the case of the smallest p-type-buried-layer exclusion. The temporal noise was also pitch-size and p-type-buried-area dependent. This reflected the leakage-current variations.

The MIMOSA-21bis B prototype was composed of different versions of sensing diodes, designed to be tolerant to ionizing radiation. Due to their layout, those diodes were expected to have increased parasitic capacitances. The capacitance measurements were especially important for this sensor. A successfully implemented radiation-tolerant diode may happen to have a large capacitance. In such a case, the electron charge would be converted into a voltage signal of very small amplitude. This would lead to a poor SNR, one of the main parameters governing a sensor performance. Indeed, measurements showed that the radiation-tolerant

diodes implemented in MIMOSA-21bis B demonstrated larger capacitances than the standard versions. However, the measured values were in an acceptable range (<20 fF).

The leakage current and temporal noise measured with MIMOSA-21bis B pixels varied according to the pitch size and sensing diode design. Neglecting those variations, one may conclude that the leakage currents and parasitic capacitances measured with MIMOSA-21bis were in the same range as already observed for MAPS implemented in other technologies (e.g., the AMS-OPTO 0.35 μm). Instead, the temporal noise, in the range from ∼12 e^- to ∼19 e^-, was higher than observed for previous sensors implemented in the AMS technology (see Section 4.3.2). This high temporal noise measured with MIMOSA-21bis can be explained by the relatively long integration time of 20 ms. This time is at least one order of magnitude longer than the one from the past measurements, for example, those performed with the AMS sensors described in Section 4.3.

Table 6.3: Parasitic capacitances of pixels, temporal noise, and leakage current measured with MIMOSA-21bis A and B prototypes before irradiation. The precision of the capacitance measurements was estimated to be ≤1 fF. The statistical uncertainties of the temporal noise and leakage current mean value shown in the table do not exceed 1%.

Chip	Design name	Capacitance [fF]	Temporal noise [e^-]	Leakage current [fA]
MIMOSA-21bis A (standard diodes)	10μm_S_PBurProt	7.2	12.0	1.5
	10μm_L_PBurProt	7.1	14.3	2.5
	10μm_XL_PBurProt	7.1	14.9	3.0
	20μm_L_PBurProt	7.1	18.1	5.0
	20μm_XL_PBurProt	7.0	18.9	5.8
MIMOSA-21bis B (radiation-tolerant diodes)	10μm_l_PBurProt_A	16.7	18.9	0.4
	10μm_L_PBurProt_B	13.2	16.2	1.5
	10μm_L_PBurProt_C	13.2	15.3	0.6
	10μm_L_PBurProt_D	11.2	15.0	0.8
	20μm_L_PBurProt_A	16.6	17.4	0.5
	20μm_L_PBurProt_E	16.9	19.1	0.8
	20μm_L_PBurProt_F	10.6	15.1	1.1

6.1.3 Ionizing radiation tolerance

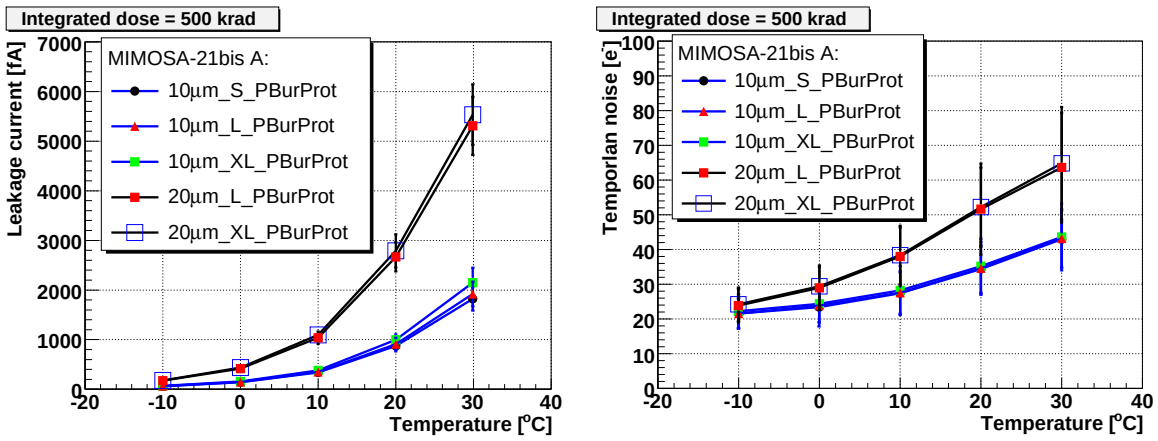
Several MIMOSA-21bis A and B sensors were irradiated up to 500 krad. Due to a very high leakage current, the sensing diode voltage decay was much faster than the integration time. Characterizing the sensor without shortening the integration time was impossible. A shorter integration time was achieved by changing the sensor readout mode. A dedicated pattern supplied by a pattern generator was applied to switch from the sequential to the column readout mode. The integration time was then reduced to ∼247 μs. In order to verify the sensor parameters' dependence on the temperature, the devices were measured in a wide temperature

range, from -10 ^{o}C up to +30 ^{o}C.

Figure 6.3(a) displays the leakage current measured with MIMOSA-21bis A. The values measured for the standard 2×2 μm^2 diodes were very large, on the order of 1-3 pA at +20 ^{o}C. Such large leakage-current values for relatively small sensing diodes had never been previously observed after irradiation with past sensors implemented in the AMS 0.35-µm process. Also, a very strong and unexpected dependence on the pitch size was found.

A similar leakage current of approximately 1 pA was observed at room temperature with all MIMOSA-21 A pixels with the pitch size of 10 µm. The leakage currents measured for the pixels with the pitch of 20 µm amounted to approximately 3 pA under the same conditions. It is worth mentioning that the ratio between the leakage currents observed for pixels with a pitch of 20 µm or 10 µm was ∼3 over the full temperature range studied here. Based on the sensor layout, it was possible to calculate the area where the thick oxide was implemented. This evaluation was done in order to determine whether the excessive leakage current originates from the thick-oxide regions. For the 10-µm pitch, the thick-oxide area amounted to ∼100 μm^2 , while for the 20-µm pitch, it covered ∼290 μm^2. The thick-oxide-area ratio is therefore ∼2.9, which is very close to the leakage-current ratio calculated above. Most likely, the defects induced by ionizing radiation in the thick oxide are responsible for the observed leakage-current increase.

Also after irradiation, the temporal noise (see Figure 6.3(b)) reflected the leakage-current variation with temperature (Figure 6.3(a)), confirming that the main contribution to the total noise originated from the shot noise of the leakage current.



(a) (b)

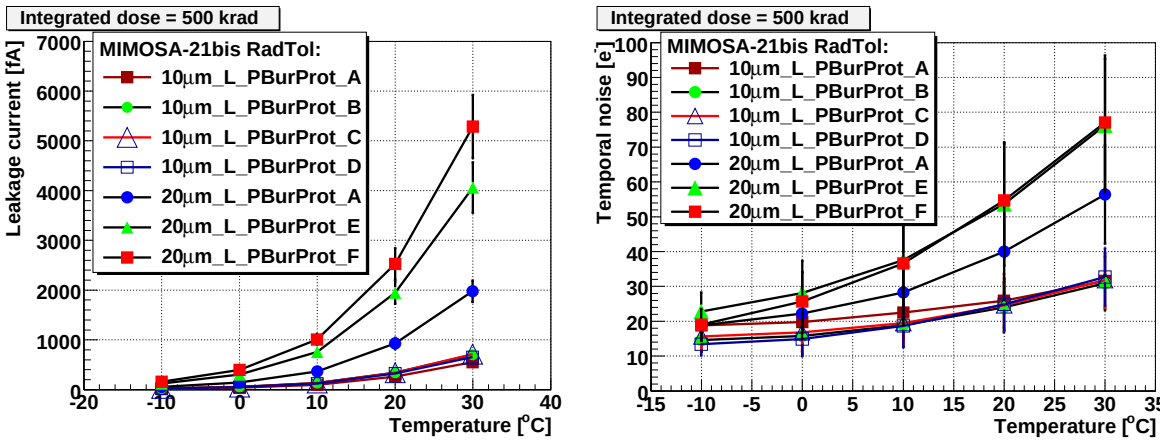
Figure 6.3: MIMOSA-21bis A: (a) Leakage current and (b) temporal noise as a function of temperature after sensor irradiation up to 500 krad. The uncertainties displayed take the leakage current and noise dispersion into account. The uncertainties of the mean values of both observables do not exceed 1%.

MIMOSA-21bis B was measured under the same conditions as MIMOSA-21bis A. Figure 6.4(a) shows the leakage-current variation with temperature. One can observe that

the leakage current is also pitch dependent in the case of the radiation-tolerant version of MIMOSA-21bis. This observation may be explained, as previously done for MIMOSA-21bis A, by the area of the thick oxide occupying the pixel. However, in this case, the same calculations are more difficult due to the variety of radiation-tolerant diode designs implemented in MIMOSA-21bis B.

Among all the designs implemented in MIMOSA-21bis B, the *10µm_L_PBurProt_A* and *20µm_L_PBurProt_A* pixels were equipped with the replica of the radiation-tolerant diode already implemented in previous devices based on the AMS process, such as the MIMOSA-15 featuring a 20-µm pitch and 4.3×3.4 µm^2 diodes (see also Section 4.3.2). To compare the radiation hardness of both processes, the *20µm_L_PBurProt_A* pixels were chosen for further study because they feature the same pitch size as some of the AMS-based designs. The measured leakage current for the *20µm_L_PBurProt_A* pixels implemented in the BiCMOS process was (∼900 fA) at +20 °C. However, the leakage current observed for the radiation-tolerant diodes implemented in the AMS 0.35-µm process and irradiated up to 1 Mrad was ∼100 fA. The reader is referred to Figure 4.20 in Section 4.3.2 for a comparison. The investigated BiCMOS process was found to be not tolerant to ionizing radiation.

The MIMOSA-21 B temporal noise (presented in Figure 6.4(b)) reflected the leakage-current change, as was observed in the case of MIMOSA-21bis A. Despite the relatively short integration time of ∼247 µs, noise above 30 e$^-$ was observed at room temperature after irradiation up to 500 krad. Such a high temporal noise does not allow this technology to be used for sensors dedicated to particle tracking.



(a) (b)

Figure 6.4: MIMOSA-21bis B: (a) Leakage current and (b) temporal noise as a function of temperature after sensor irradiation of up to 500 krad. The uncertainties displayed take the leakage current and noise dispersion into account. The uncertainties of the mean values of both observables do not exceed 1%.

6.1.4 The charge collection properties after neutron irradiation

Since MIMOSA-21bis A contained the pixels featuring a different p-type-buried-layer exclusion (see Section 6.1.1), it was chosen for studying the CCE and its dependence on the p-type-buried-silicon areas. The measurements were done at +20 °C for a nominal readout clock frequency of 1.25 MHz, translating into an integration time of 20 ms.

Table 6.4 contains the CCE values measured with MIMOSA-21bis A before and after irradiation to $6{\cdot}10^{12}\ \mathrm{n_{eq}/cm^2}$ and $1.3{\cdot}10^{13}\ \mathrm{n_{eq}/cm^2}$. The same table presents the estimated charge collected by the seed pixel. This charge was estimated taking into account the CCE measured with an $^{55}\mathrm{Fe}$ source and assuming that a MIP will generate $\sim$720 e^- crossing the 9-µm-thick EPI layer[7]. For example, if the CCE = 25.1%, the estimated charge collected by the seed pixel is equal to 720 $\mathrm{e^-} \times 25.1\% \approx 247e^-$. The last two columns of Table 6.4 present the temporal noise and estimated SNR (in this case, the ratio between the estimated charge and the mean value of the temporal noise). The temporal noise and the charge collected by the seed pixel of the MIMOSA-15 prototype are given in the same table for comparison. The reader should keep in mind that in case of MIMOSA-15, the collected charge value was not estimated by simple calculation but measured with high-energy pion beam.

The CCE was observed to significantly depend on the p-type-buried-layer-exclusion area (see Figure 6.2). The CCE could not be measured with the pixels featuring the smallest p-type-buried-layer exclusion (*10µm_S_PBurProt* with p-type-buried silicon implemented relatively close to the sensing diodes). Instead, the CCE was measurable for pixels with larger p-type-buried-silicon exclusions, amounting to $8.8 \pm 0.4\%$ and $17.1 \pm 0.9\%$ for *10µm_L_PBurProt* and *10µm_XL_PBurProt* pixels, respectively. Moreover, the CCE was observed to decrease with reduced pixel pitch ($34.3 \pm 1.6\%$ for *20µm_XL_PBurProt* and $17.1 \pm 0.9\%$ for *10µm_XL_PBurProt*). The opposite tendency was observed for the previous sensors implemented in the AMS process [4].

Since the worst CCE was noticed for the diodes featuring the smallest p-type-buried-silicon exclusion and the smallest pitch size, there was evidence that the p-type-buried silicon may have screened the sensing diode, resulting in the poor CCE for such pixels. This possible screening effect is sketched in Figure 6.5. In the case of the poorest CCE (see Figure 6.5(a)), the p-type-buried silicon is not only located below the p-wells, but it is likely to extend underneath the n-wells. This spread may reach several micrometers and essentially close the area around the collecting diode. As a consequence, the charge collection from the EPI layer would not be observed. In the case of a larger pitch, Figure 6.5 (b), or larger p-type-buried-layer exclusion (Figure 6.2(c)), the sensing diodes are no longer isolated from the EPI layer.

Before concluding with a comparison between the BiCMOS and the AMS, it should be mentioned that the characterization of MIMOSA-21bis was not performed systematically up to the end. In particular, it would be worthwhile to characterize sensors under different conditions (temperature, radiation doses) and with high-energy pion beam, to study the

[7] This value was officially specified by the vendor.

Table 6.4: Estimation of the charge expected in the seed pixel for the MIMOSA-21bis A prototype.

Irradiation	Design name	CCE seed [%]	Estimated charge [a] [e^-]	Noise [e^-]	Estimated SNR
non-irradiated	10μm_S_PBurProt	—	—	12.0	—
	10μm_L_PBurProt	8.8 ± 0.4	64	14.3	4.4
	10μm_XL_PBurProt	17.1 ± 0.9	123	14.9	8.3
	20μm_L_PBurProt	25.1 ± 1.1	181	18.1	10
	20μm_XL_PBurProt	34.3 ± 1.6	247	18.9	13
MIMOSA-15 [b]	20-µm pitch , 4.3×3.4 µm^2 diode	∼22	253.7 ± 0.6	—	27.8 ± 0.5
$6{\cdot}10^{12}$ n_{eq}/cm^2	10μm_S_PBurProt	—	—	14.2	—
	10μm_L_PBurProt	6.18 ± 0.3	44	16.3	2.7
	10μm_XL_PBurProt	12.5 ± 0.6	90	16.9	5.3
	20μm_L_PBurProt	12.8 ± 0.6	92	20.1	4.6
	20μm_XL_PBurProt	20.4 ± 1.0	147	20.9	7
MIMOSA-15 $2.1{\cdot}10^{12}$ n_{eq}/cm^2	20-µm pitch , 4.3×3.4 µm^2 diode	—	134.4 ± 0.2	—	14.7 ± 0.3
$1.3{\cdot}10^{13}$ n_{eq}/cm^2	10μm_S_PBurProt	—	—	18.2	—
	10μm_L_PBurProt	7.2 ± 0.4	52	20.8	2.5
	10μm_XL_PBurProt	11.2 ± 0.5	81	20.6	3.9
	20μm_L_PBurProt	10.8 ± 0.5	78	27.8	2.8
	20μm_XL_PBurProt	16.7 ± 0.7	120	24.5	4.9

[a] The charge was estimated taking into account the CCE measured with an ^{55}Fe source and assuming that a MIP will generate ∼720 e^- crossing the 9-µm-thick sensor EPI layer (value specified by the vendor).
[b] For MIMOSA-15, the signal charge collected by the seed pixel was measured for a MIP.

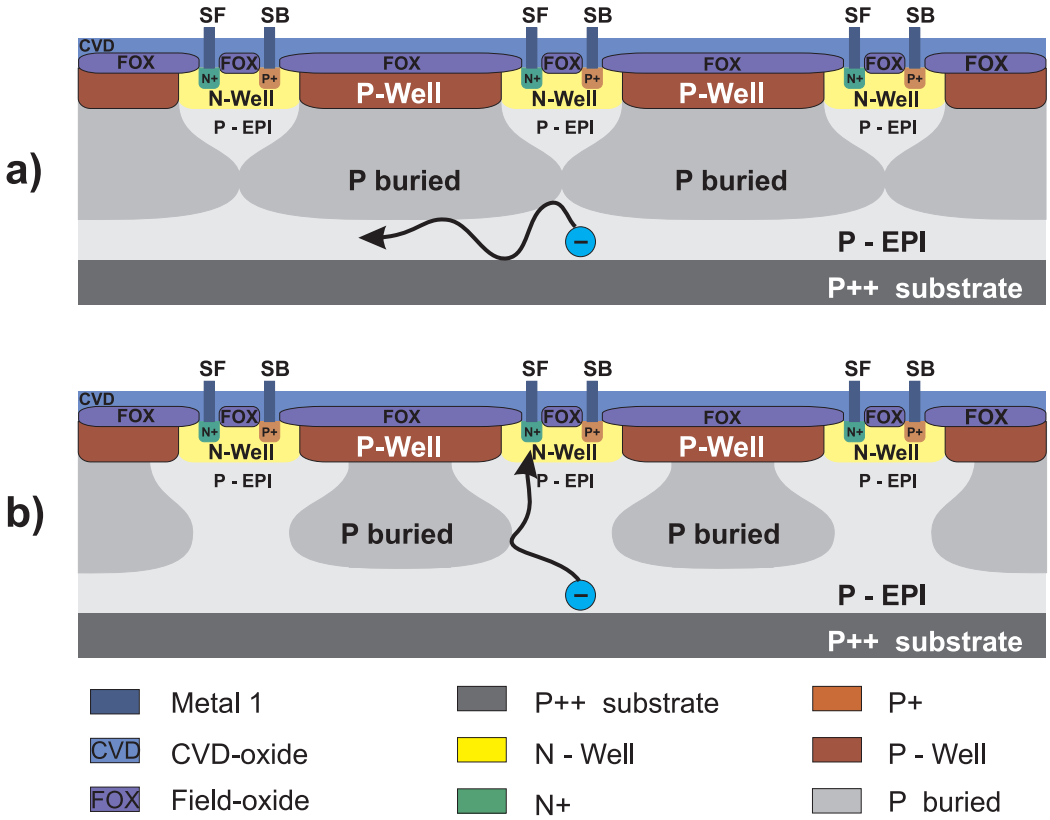


Figure 6.5: Vertical cut of the MIMOSA-21bis A prototype illustrating the influence of the p-type-buried-silicon exclusion on the charge collection. Exact doping profiles for this BiCMOS process are unknown, e.g., the depth of p-wells or p-type-buried-silicon implants; therefore, the picture may not be to scale.
(a) Small p-type-buried-silicon exclusion – the p-type-buried silicon is not only located below the p-wells, but is likely to extend underneath the n-wells. This spread may reach several micrometers and essentially close the area around the collecting diode, resulting in poor CCE.
(b) Large p-type-buried-silicon exclusion – the sensing diodes are no longer isolated from the EPI layer.

sensor response to MIP. This would allow for better comparison between the investigated BiCMOS process and the AMS process. Such tests were abandoned because the ionizing radiation tolerance of the sensors implemented in the BiCMOS process was not considered to be sufficient for particle tracking. As a consequence, the performance comparison of the CCE of devices implemented in the BiCMOS and in the AMS processes is very limited if restricted to the CCE measurements. Concluding on the potential of the BiCMOS technology over the AMS process is difficult on the basis of the available sensors. The latter have different basic parameters. For example, the thicknesses of the EPI layers are different (9 µm in the case of the BiCMOS process and 15 µm - 20 µm for the AMS technology[8]), which results in different CCE (see the discussion in Section 4.3.3).

6.1.5 Conclusions

The performance of the BiCMOS process based on a graded EPI layer with enhanced charge collection was studied with MIMOSA-21bis. Before irradiation, all devices exhibited similar properties in terms of leakage current and sensing-diode parasitic capacitances as previous sensors fabricated with CMOS processes based on a standard, low-resistivity EPI layer. The CCE measured for the sensors when $^{55}\mathrm{Fe}$ was used as a radiation source was strongly disturbed by the screening effect; this disturbance depended mainly on the size of the p-type-buried-silicon-exclusion area and the pixel pitch.

After exposure to ionizing radiation, the leakage current was observed to increase significantly above typical values obtained with previous sensors. In addition, the leakage-current increase was strongly dependent on the pitch size. Such behavior had never been observed before. This very high leakage current translated into a high temporal noise. The poor performance measured of these sensors after irradiation suggests that the BiCMOS process studied here was not tolerant enough to this type of particles.

Due to the poor ionizing radiation tolerance of the process, the MIMOSA-21bis prototypes were not studied with high-energy particle beam, and the tolerance of this BiCMOS process to non-ionizing radiation was not assessed.

6.2 Performance of sensors based on a high-resistivity epitaxial layer – MIMOSA-25

As discussed in the previous section, the BiCMOS process based on a graded substrate cannot be used for particle tracking due to its poor ionizing radiation tolerance. This fact prompted studies oriented towards other commercially available processes, with special features likely to increase the non-ionizing radiation tolerance. This chapter reports on the

[8]The effective thickness assessed with high-energy pion beam was a few micrometers below the value specified by the vendor. As the real thickness of the graded EPI was not measured, the values given here correspond to those specified by the vendor.

studies carried out with sensor prototypes implemented in the 0.6-µm XFAB process based on a high-resistivity EPI layer.

6.2.1 Substrate properties

The standard CMOS technologies use a low-resistivity substrate of ∼1 Ω·cm, on top of which an ∼10-20-µm-thick EPI layer with a resistivity of ∼10 Ω·cm is implemented. Figure 6.6 (left) shows a typical doping profile of a standard CMOS process. As displayed in Figure 6.6 (right), at standard CMOS voltage (here 3.8 V), the depletion depth of the EPI layer located underneath the n-well diode reaches only a fraction of micrometer. As there is almost no electric field in most of the EPI layer, the signal electrons are predominantly collected through thermal diffusion. The results of simulations made with ISE-TCAD package [158] showed that for a typical EPI layer thickness of ∼14-15 µm, the charge collection time of thermally diffused electrons is approximately 100 ns [99].

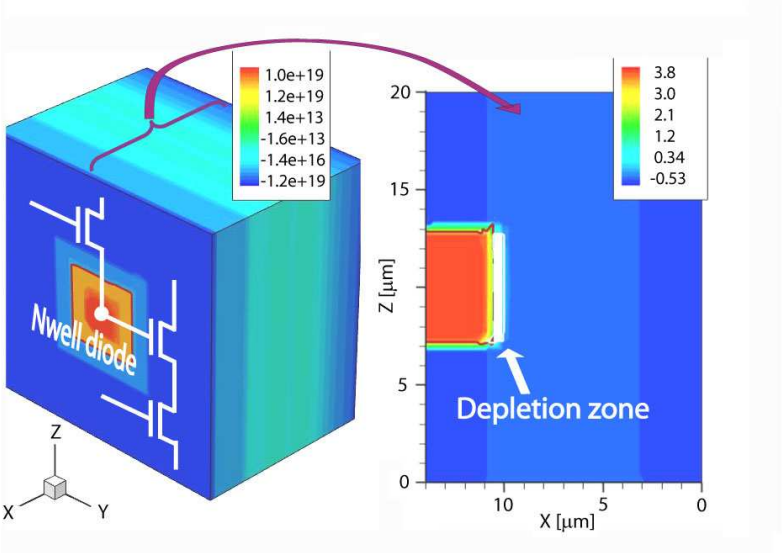


Figure 6.6:
Left: CMOS sensor pixel cell based on a low-resistivity EPI layer; the color scale represents the doping concentration [cm^{-3}].
Right: Potential [V] through the volume. Depleted zone <1 µm.

The first CMOS process offering a high-resistivity EPI became available for MAPS implementation in 2008. It was a 0.6-µm process with so-called PIN option and was offered by XFAB. Due to the low doping of the epitaxial layer (typically 10^{12}cm^{-3}, which translates into a resistivity of ∼1 kΩ·cm), the depleted zone of the n-well (n+) – p-EPI (p–) junction extends underneath the highly doped n-well (typically 10^{17}-10^{18}cm^{-3}) by several micrometers. Due to an electric field existing in the depleted region, the charge transfer is expected to be faster and more oriented towards the n-wells. These expectations were confirmed by a simulation made with the ISE-TCAD package. The simulation results showed that, indeed, the depleted zone inside the high-resistivity EPI layer can be significantly extended (as shown in Figure 6.7). The time needed for the charge collection in the high-resistivity EPI layer is ∼10 ns [99]. This is about 10 times faster than for a standard, low-resistivity EPI layer. The fast signal collection indicates a substantial reduction of the mean free path for the electrons before reaching a

sensing diode. It is expected that this reduced mean free path will translate into a higher non-ionizing radiation tolerance. The remaining questions are:

- How much can this tolerance be improved ?
- What is the tolerance of this technology to ionizing radiation ?

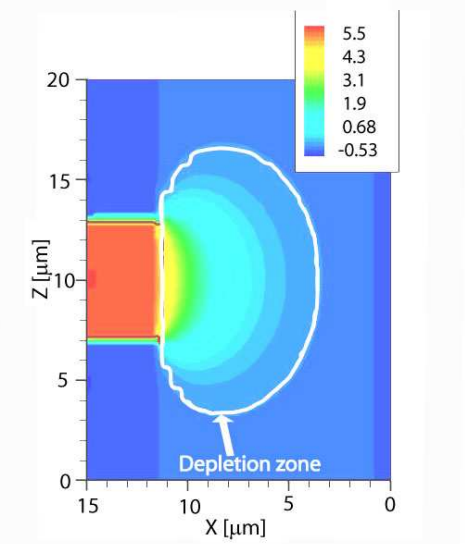


Figure 6.7:
CMOS sensors based on a high-resistivity EPI layer: potential [V] calculated using ISE TCAD. Reverse biasing of n-well – p-EPI junction at 5.5V results in a depleted zone extended by several µm towards the sensitive volume.

6.2.2 Design of the MIMOSA-25 prototype based on the XFAB 0.6-µm high-resistivity EPI layer

To study the potential of the CMOS process based on the high-resistivity EPI layer offered by XFAB, the first sensor prototype named MIMOSA-25 was manufactured. The strategy was to equip this sensor with pixels whose performance could be easily compared with performance of the similar architectures already manufactured in the AMS 0.35-µm technology. Therefore, the two basic pixel architectures were implemented: the 3T and the SB (see Section 4.1.3). In order to verify whether the implementation of radiation-tolerant sensing diodes is possible with the XFAB process, the two mentioned pixel architectures were equipped with the radiation-tolerant version of the sensing diode. The pixels hosting the standard and the radiation-tolerant versions of the sensing diode were implemented in two separate MIMOSA-25 sensors: MIMOSA-25$_{STD}$ and MIMOSA-25$_{RadTol}$, respectively. Some details related to the implementation of the two versions of MIMOSA-25 are shown in Figure 6.8 and they will be discussed in the following.

The basic 3T architectures implemented in MIMOSA-25 were equipped with a sensing diode of 4×4 µm^2. This size was the minimum compatible with the design rules. At the same time, these diodes featured an area close to the one implemented in the past in the AMS 0.35-µm process (usually 4.3×3.4 µm^2). In addition, an enclosed-layout transistor was used to reset the

diode voltage. Its inner part was connected to the sensing diode. This solution was used for the first time in reference [4] to improve the ionizing radiation tolerance.

Due to the design rules, the minimum n-well size available in case of the SB diode amounted to 5×6.5 μm^2. The 3T architecture was therefore also implemented with a 5×6.5 μm^2 diode in order to allow for a comparison.

To increase the ionizing radiation tolerance, the aforementioned pixel architectures were equipped with the radiation-tolerant version of the sensing diodes. The pixel layout was intended to duplicate the radiation-tolerant diodes already implemented in the AMS process, where the thick oxide surrounding the sensing diode is replaced by an ∼10-nm-gate oxide (see Figure 4.19 in Section 4.3). The design of the radiation-tolerant diodes requires the violation of some design rules. This procedure was well established for the AMS 0.35-µm technology. However, due to the different design rules of the XFAB process, the AMS approach could not be applied. As a consequence, the thin gate oxide surrounding the n-well diode did not extend up to the n-well – p-EPI boundary, as in the case of the AMS (see Section 4.3). Figure 6.9 displays drawings illustrating the difference in sensing diode implementation between the standard and the radiation-tolerant versions of MIMOSA-25.

Both sensors, MIMOSA-25$_{STD}$ and MIMOSA-25$_{RadTol}$, had a sequential analog readout without any sophisticated data processing inside or outside the pixel area. However, this readout was different from the one frequently used in the past which was presented in Section 4.2.2.1. More details may be found in Appendix A.4. The readout of MIMOSA-25 permits an integration time of 77 µs.

6.2.3 Non-ionizing radiation tolerance assessment of MIMOSA-25

In order to study the performance of the sensors based on the high-resistivity EPI layer, particularly their non-ionizing radiation tolerance, several MIMOSA-25 prototypes were irradiated up to 1.3·10^{13} $\mathrm{n_{eq}/cm^2}$ and 3·10^{13} $\mathrm{n_{eq}/cm^2}$. The performance of the samples was assessed with an $^{55}\mathrm{Fe}$ source before and after sensor irradiation with neutrons. Later, the charge collection properties of the high-resistivity EPI layer were studied with a $^{106}\mathrm{Ru}$ source and with high-energy pion beam.

6.2.3.1 Temporal noise before and after neutron irradiation

The temporal noise of MIMOSA-25$_{STD}$ and MIMOSA-25$_{RadTol}$ was studied before and after irradiation with neutrons. In general, the temporal noise measured for MIMOSA-25$_{RadTol}$ was similar to the temporal noise measured for MIMOSA-25$_{STD}$ and the observed small difference was compatible with chip to chip variations.

This noise, observed for MIMOSA-25$_{RadTol}$ before and after irradiation to 3·10^{13} $\mathrm{n_{eq}/cm^2}$, is displayed in Table 6.5. The values presented are comparable to the ones observed in the past with other sensors featuring similar sensing diodes (see Section 4.3.2 for comparison). The

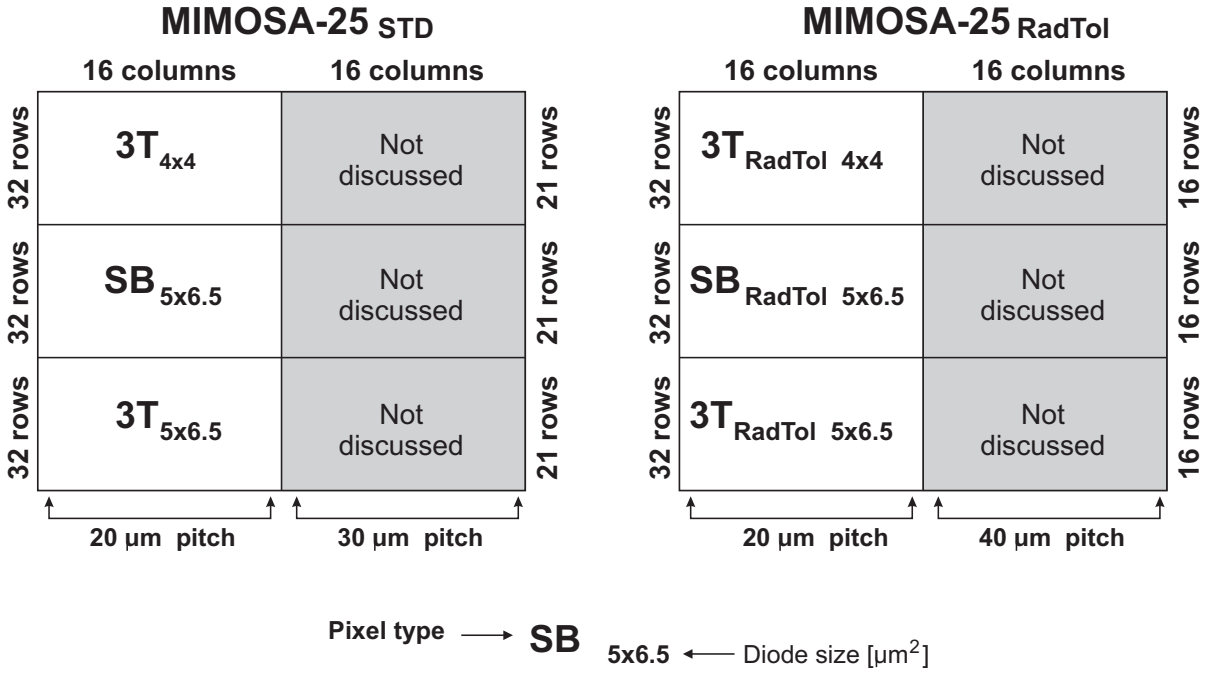


Figure 6.8: The two versions of MIMOSA-25.
Left: MIMOSA-25$_{STD}$ design with standard diodes implemented inside pixels featuring a pitch size of 20 µm and 30 µm.
Right: MIMOSA-25$_{RadTol}$ design with radiation-tolerant diodes implemented inside pixels featuring a pitch size of 20 µm and 40 µm.

slightly larger values of the temporal noise observed after irradiation could be attributed to an increase in the bulk current or to surface effects induced by ionizing radiation accompanying the neutrons[9]. The observed noise increase after irradiation to $3{\cdot}10^{13}\ \mathrm{n_{eq}/cm^2}$ should be compared with the simultaneous signal decrease attributed to the sensor bulk damage. The properties of MIMOSA-25 prototypes regarding charge collection are described in the following section.

Table 6.5: Temporal noise of MIMOSA-25$_{RadTol}$ before and after neutron irradiation, measured at a temperature of +20 °C. Typical uncertainties do not exceed 0.5 e$^-$.

MIMOSA-25$_{RadTol}$	Before irradiation	$3{\cdot}10^{13}\ \mathrm{n_{eq}/cm^2}$
Pixel	Noise [e$^-$]	Noise [e$^-$]
$3T_{4\times4}$	10.8	14.7
$SB_{5\times6.5}$	12.2	16.2
$3T_{5\times6.5}$	13.8	18.9

[9]The neutron irradiation process is also accompanied by a flux of low-energy photons. This flux results in the accumulation of an ionizing dose in addition to the neutron fluence. The ionizing dose usually reaches values below 100 krad per $1{\cdot}10^{13}\ \mathrm{n_{eq}/cm^2}$ (for more information see Section 4.2.5). Due to the expected ionizing radiation, attention was given to the MIMOSA-25$_{RadTol}$ sensors, which were expected to be more robust to the mentioned type of radiation.

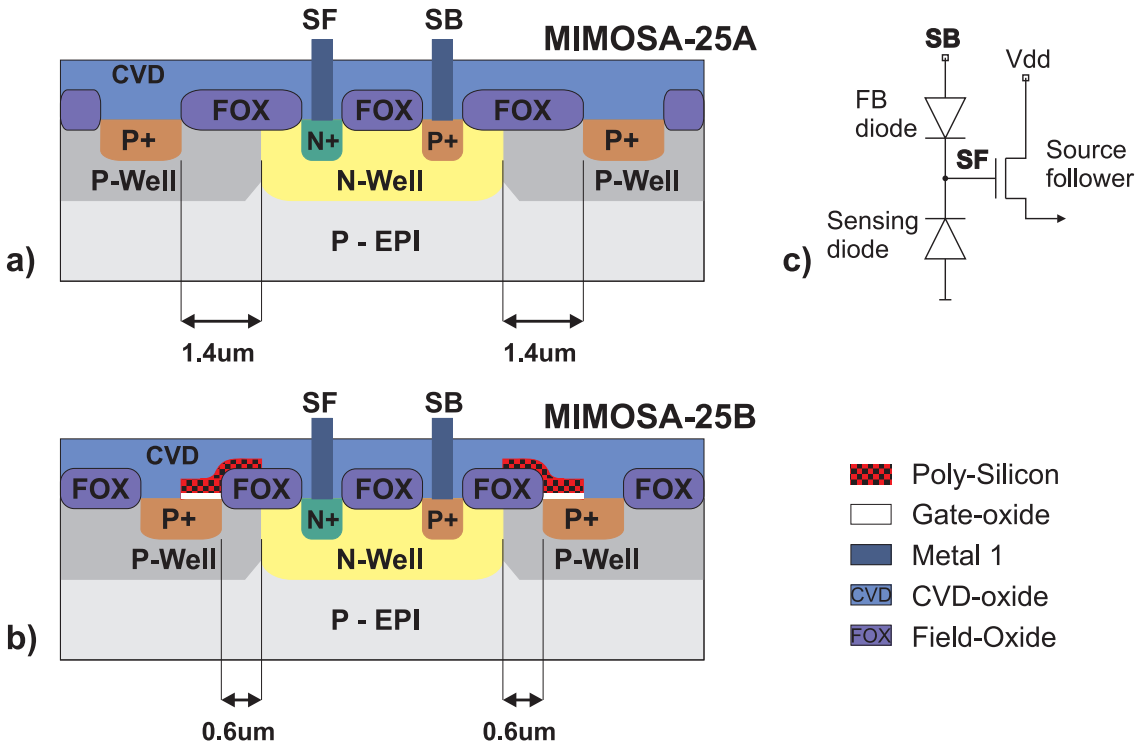


Figure 6.9: MIMOSA-25 SB diode versions: (a) standard version, (b) radiation-tolerant diode surrounded by a thin gate-oxide ring (white), (c) simplified pixel schematic.

6.2.3.2 Charge collection properties of the high-resistivity EPI layer studied in the laboratory.

The sensor response to MIP was studied in the laboratory with a $^{106}\mathrm{Ru}$ source emitting electrons (see Section 4.2.4). The distribution of the charge collected by the seed pixel was measured for several MIMOSA-25$_{RadTol}$ samples. This distribution is shown in Figure 6.10 for the three different sensing diodes implemented in MIMOSA-25$_{RadTol}$. Two peaks are visible: one at very low values of the charge (located below 200 e^-), corresponding to temporal noise, and another peak typical of a Landau distribution, extending to the highest charge values, expressing the collected signal charge.

Two peaks are visible: the one at very low values of the charge and the one extending up to the highest charge values. The first one, located below $\sim$200 e^-, corresponds to the temporal noise. The second one, typical of a Landau distribution, expresses the collected signal charge.

The MPV of the Landau distribution was used to evaluate the charge-collection properties of the sensors. The MPVs of the charge collected by the seed pixel are presented in Table 6.6. The statistical uncertainty of the MPV was assessed to be approximately 1%. The measurements show that the charge collected by the seed pixel depends strongly on the diode size. The $3T_{4\times4}$ diode collected $\sim$20% less charge than the $3T_{5\times6.5}$. The charge collected with each of

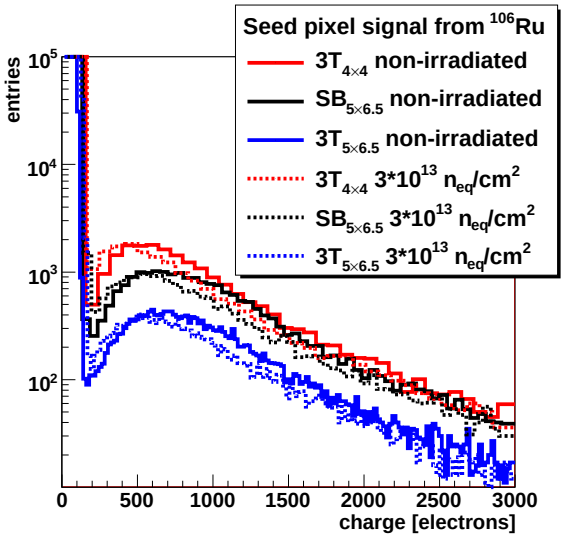


Figure 6.10:

The distribution of the signal charge from a ^{106}Ru source collected by the seed pixel of MIMOSA-25$_{RadTol}$ for three investigated matrices. Dashed lines correspond to the signal charge distribution obtained with sensors before irradiation. Solid lines represent the charge distribution after sensor irradiation to 3·10^{13}n$_{eq}$/cm^2. The measurements were performed at room temperature.

Table 6.6: The collected charge MPV [e$^-$] in the seed pixel assessed with MIMOSA-25$_{RadTol}$ before irradiation. Results from tests with a ^{106}Ru source performed at room temperature.

MIMOSA-25 submatrix	Collected charge
$3T_{4\times4}$	548 ± 8
$SB_{5\times6.5}$	671 ± 7
$3T_{5\times6.5}$	675 ± 7

the two largest diodes ($SB_{5\times6.5}$ and $3T_{5\times6.5}$) was similar to the other. The observed difference in charge collection between the smaller diode and the larger diode suggested that the EPI layer underneath the sensing diode was not fully depleted. This was expected from the T-CAD simulations presented earlier in Figure 6.7. In the case of a fully-depleted sensor, one could expect rather insignificant differences related to the sensing-diode size.

Figure 6.11 shows the charge collected for various pixel multiplicities inside a cluster for different sensor prototypes: MIMOSA-9[10], MIMOSA-18[11] and MIMOSA-25. The MIMOSA-9, and the MIMOSA-18 prototypes were implemented in the 0.35-µm AMS process based on a standard EPI layer. MIMOSA-9 has a pixel pitch of 20 µm. Due to its pixel pitch of 10 µm, MIMOSA-18 was the sensor most tolerant to non-ionizing radiation among those based on standard EPI layer. Moreover, both MIMOSA-9 and MIMOSA-18 implemented sensing diodes with a size similar to the one implemented in the MIMOSA-25 prototype. The results presented

[10]MIMOSA-9 — 4.3×3.4 µm^2 sensing diode, 20-µm pitch size, T=-20 °C, integration time ∼1.6 ms.
[11]MIMOSA-18 — 4.3×3.4 µm^2 sensing diode, 10-µm pitch size, T=-20 °C, integration time ∼3 ms.

in Figure 6.11 were observed before exposing the sensors to non-ionizing radiation. The value "1" corresponds to the seed pixel. In the case of MIMOSA-25, a ^{106}Ru source was used during the measurements. Data related to MIMOSA-9 and MIMOSA-18 were derived from tests with high-energy pion beam[12].

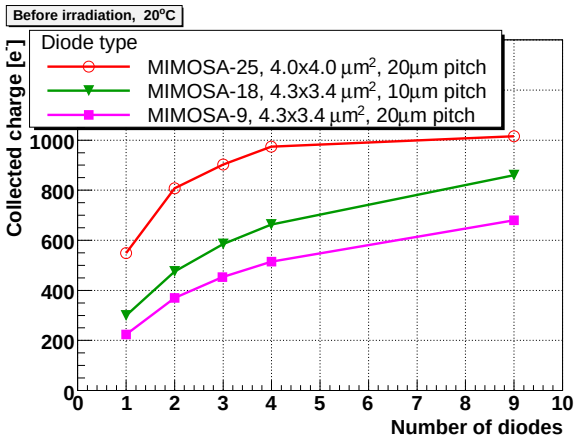


Figure 6.11:
Comparison of the collected charge as a function of the cluster size for MIMOSA-25 and for older devices based on the standard EPI layers (0.35-µm AMS process) – MIMOSA-9 (4.3×3.4 µm² sensing diode, 20-µm pitch size), and MIMOSA-18 (4.3×3.4 µm² sensing diode, 10-µm pitch size). Measurements performed at −20°C for MIMOSA-9 and MIMOSA-18, and at room temperature for MIMOSA-25.

One can observe that in the case of the sensor based on a high-resistivity EPI layer, the charge collected by the seed pixel is about twice as large as in the case of a standard EPI layer (MIMOSA-9 and MIMOSA-18). This originates directly from the different charge collection processes acting in both types of EPI layers. In the case of standard sensors, the charge collection proceeds through thermal diffusion, leading to a sizeable charge spread among neighboring pixels. As depicted in Figure 6.11, the cluster size composed of 9 pixels is not large enough to collect all of the signal charge generated inside the EPI layer. The charge spread is much more limited in MIMOSA-25 due to its partially depleted EPI layer. For this sensor, almost all of the charge is already stored in clusters composed of 4 pixels. The observed behavior follows the expectations.

6.2.3.3 Charge collection properties of a high-resistivity EPI layer measured with high-energy pion beam.

The MIMOSA-25 prototypes were tested before and after irradiation to $1.3{\cdot}10^{13}$ $\mathrm{n_{eq}/cm^2}$ and $3{\cdot}10^{13}$ $\mathrm{n_{eq}/cm^2}$ with 120-GeV pion beam. A constant sensor temperatures of +20 °C was applied. The studies with high-energy pion beam were prompted by the following needs:

- to compare the response of sensors exposed to a ^{106}Ru source and to high-energy particle beam

[12] As shown later in this document, the charge collected by a seed pixel during tests with a ^{106}Ru source is 10-20% larger than the one observed with high-energy particle beam.

- to measure the ϵ_{det}, which is difficult with a $^{106}\mathrm{Ru}$ source due to multiple scattering
- to compare performance with past sensors that were measured under similar conditions

Table 6.7: The MPV of charge [e^-] collected by the seed pixel as measured with MIMOSA-25$_{RadTol}$, MIMOSA-15, and MIMOSA-18, before and after irradiation.

MIMOSA-25 (+20°C)	Before irradiation	1.3·10^{13} $\mathrm{n_{eq}/cm^2}$	3·10^{13} $\mathrm{n_{eq}/cm^2}$
$3T_{4\times4}$	462 ± 5	391 ± 26	331 ± 10
$SB_{5\times6.5}$	588 ± 2	428 ± 8	402 ± 3
$3T_{5\times6.5}$	623 ± 4	475 ± 18	430 ± 6
MIMOSA-15 (−20°C)	Before irradiation	4.7·10^{11} $\mathrm{n_{eq}/cm^2}$	2.1·10^{12} $\mathrm{n_{eq}/cm^2}$
20-µm pitch, 4.3×3.4 µm^2 diodes	∼215	∼204	∼134
MIMOSA-18 (−20°C)	Before irradiation	6·10^{12} $\mathrm{n_{eq}/cm^2}$	1·10^{13} $\mathrm{n_{eq}/cm^2}$
10-µm pitch, 4.3×3.4 µm^2 diodes	∼300	∼230	∼200

Table 6.7 depicts the MPV of the charge accumulated in the seed pixels for the different diode designs, before and after irradiation with 1-MeV neutrons. These values are compared to the ones obtained in the past with MIMOSA-15[13] and MIMOSA-18. Both sensors featured a sensing diode of 4.3×3.4 µm^2, which was similar to the 4×4 µm^2 diode used in the MIMOSA-25 prototypes. The main difference between MIMOSA-15 and MIMOSA-18 is the pitch size. The later was 20 µm for MIMOSA-15 and 10 µm for MIMOSA-18. Observations show that the signal collected by the seed pixel of MIMOSA-25 is about 55% larger than in the case of MIMOSA-18 and is more than double compared to the signal observed for MIMOSA-15 (the same pitch/diode size as MIMOSA-25).

Due to the sizeable signal available on the seed pixel and due to the relatively small temporal noise measured with MIMOSA-25 (see Table 6.5), the SNR increased significantly. The MPV of the SNR measured with MIMOSA-25 before and after irradiation are shown in Table 6.8 and Figure 6.12. The latter also contain data obtained in the past with sensors based on a standard EPI layer, MIMOSA-15, and MIMOSA-18. In addition, the ϵ_{det} achieved at a given SNR with both, MIMOSA-15 and MIMOSA-18 are given in brackets in Table 6.8.

One can notice that, before sensor irradiation, the SNR[14] observed for MIMOSA-25 (4×4 µm^2 diode) was about twice the value measured for MIMOSA-15 and MIMOSA-18. After irradiation up to 2.1·10^{12} $\mathrm{n_{eq}/cm^2}$, the SNR of MIMOSA-15 (with the same pitch as MIMOSA-25) decreased to about 15. A noticeable improvement of MAPS non-ionizing radiation tolerance was observed for MIMOSA-18, which features a smaller pixel pitch of 10 µm. A SNR that did not allow for efficient particle tracking was observed for this sensor after irradiation up to 1·10^{13} $\mathrm{n_{eq}/cm^2}$. Comparatively, the SNR of MIMOSA-25 dropped from ∼60 to ∼30 once the sensor was irradiated with 3·10^{13} $\mathrm{n_{eq}/cm^2}$. Despite this striking drop, the

[13]MIMOSA-15 — 4.3×3.4 µm^2 sensing diode, 20-µm pitch size, T= -20 °C, integration time ∼700 µs.

[14]Observations from past studies indicate that sensors featuring a SNR below 15 (MPV) did not provide a ϵ_{det} above 99.5% [4]. Thus a SNR∼15 seems to be the hard limit.

SNR remained in a range where the ϵ_{det} was measured to be $\sim$100%.

Table 6.8: The MPV of the SNR measured with high-energy pion beam with MIMOSA-25$_{RadTol}$ before and after irradiation. The results obtained with sensors based on a standard EPI layer, MIMOSA-15 and MIMOSA-18, are given here for comparison. Numbers in parenthesis correspond to the ϵ_{det} achieved at a given SNR.

MIMOSA-25 (+20 °C)	Before irradiation	$1.3{\cdot}10^{13}$ n_{eq}/cm^2	$3{\cdot}10^{13}$ n_{eq}/cm^2
$3T_{4\times4}$	61 ± 1	30.0 ± 1	27.5 ± 0.5
$SB_{5\times6.5}$	69.9 ± 0.9	30.8 ± 0.6	28.3 ± 0.2
$3T_{5\times6.5}$	59.6 ± 0.7	31.3 ± 0.7	28.0 ± 0.2
MIMOSA-15 (-20 °C) 20-µm pitch	Before irradiation 27.8 ± 0.5 (100%)	$4.7{\cdot}10^{11}$ n_{eq}/cm^2 21.8 ± 0.5 (99.9%)	$2.1{\cdot}10^{12}$ n_{eq}/cm^2 14.7 ± 0.3 (99.3%)
MIMOSA-18 (-20 °C) 10-µm pitch	Before irradiation 28.5 ± 0.2 (99.93%)	$6{\cdot}10^{12}$ n_{eq}/cm^2 20.4 ± 0.2 (99.85%)	$1{\cdot}10^{13}$ n_{eq}/cm^2 14.7 ± 0.2 (99.5%)

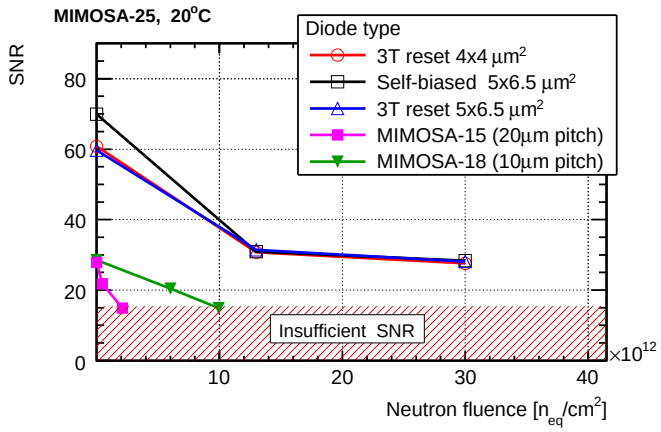


Figure 6.12: Comparison of SNR as a function of non-ionizing radiation fluence for sensors based on the high-resistivity EPI layer – MIMOSA-25 – and those based on standard EPI layer – MIMOSA-15 and MIMOSA-18. Results from tests with high-energy particle beam from the CERN-SPS, performed at $+20°C$ for MIMOSA-25 and at $-20°C$ for MIMOSA-15 and MIMOSA-18.

The results presented in this section indicate clearly that a high-resistivity EPI layer enhances the charge collection. As a consequence, a much larger signal is available in the seed pixels. This translates directly into a higher SNR than for sensors based on standard EPI layer. The studies performed with the MIMOSA-25 prototype based on a high-resistivity EPI layer showed that the non-ionizing radiation tolerance of $3{\cdot}10^{13}$ n_{eq}/cm^2 can be achieved with sensors featuring a 20-µm pitch and $\sim$16 µm^2 sensing diodes.

6.2.4 MIMOSA-25 ionizing radiation tolerance – laboratory tests and results

The encouraging non-ionizing radiation tolerance of MIMOSA-25 was shown and discussed in the previous subsection. In this subsection, the studies related to the assessment of the ionizing radiation tolerance will be reported.

The main parameters studied were the leakage current and temporal noise. These studies were performed with both MIMOSA-25 versions: with (MIMOSA-25$_{RadTol}$) and without

radiation-tolerant diodes (MIMOSA-25$_{STD}$).

Several MIMOSA-25$_{STD}$ and MIMOSA-25$_{RadTol}$ sensors were irradiated up to 150 krad and 500 krad. The sensors were characterized before and after irradiation, at a constant temperature of 20 ^{0}C and a clock frequency of 2.5 MHz, corresponding to an integration time of ∼77 µs .

6.2.4.1 Leakage current measurements

The leakage current was measured only for the pixels in the 3T configuration: MIMOSA-25$_{STD}$ and MIMOSA-25$_{RadTol}$. The evolution of this parameter was studied as a function of the integrated dose, as shown in Figure 6.13. The measured leakage currents of the 3T$_{RadTol\ 4\times4}$ and the 3T$_{RadTol\ 5\times6.5}$ were observed to be approximately one order of magnitude lower than those observed for the standard versions of the same diodes (3T$_{4\times4}$ and 3T$_{5\times6.5}$). This was a good indication that the implementation of the radiation-tolerant diodes in the XFAB 0.6-µm process was successful.

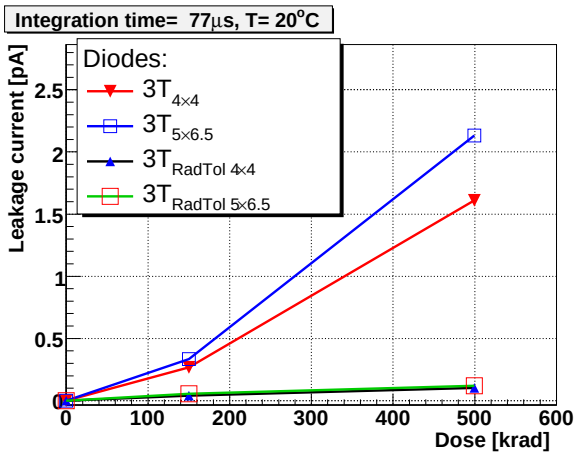


Figure 6.13:
Leakage current of different MIMOSA-25 diodes as a function of ionizing dose, observed at a temperature of +20°C.

6.2.4.2 Temporal noise measurements

Figure 6.14 depicts the temporal noise measured as a function of the integrated dose for both types of diodes (non-radiation and radiation tolerant diode). In general, the temporal noise variation with the dose was observed to reflect the sensing-diode leakage currents presented in Figure 6.13. The lowest temporal noise of 13 e$^-$ was observed for the radiation-tolerant diode 3T$_{RadTol\ 4\times4}$ after sensor irradiation to 500 krad. For the sensing diode featuring the same size as 3T$_{RadTol\ 4\times4}$ but implemented without any protection against ionizing radiation effects (3T$_{4\times4}$), the temporal noise amounted to ∼40 e$^-$.

Some comments follow on the trend of the temporal noise with increasing dose observed for the pixels equipped with SB diodes. The temporal noise of the SB$_{5\times6.5}$ pixel was the smallest in MIMOSA-25$_{STD}$ before irradiation, while it was the largest one after irradiation. The same

trend was noticed for MIMOSA-25$_{RadTol}$ pixels. Accounting for the same size of the sensing diode equipping SB and 3T pixels, one could roughly assume that the leakage current of the sensing diode for both pixel configurations should not be significantly different. Therefore, the shot-noise contribution originating from the sensing-diode leakage current should be at least comparable for both architectures. However, in the case of the SB pixel, the sensing diode leakage current is continuously compensated; therefore, there is constant current flow through the forward-biased diode. This current is quantitatively the same as the leakage current of the sensing diode. Consequently, one may expect the shot-noise contribution (see discussion in Section 4) to the total noise from both the sensing diode and the forward-biased diode. This contribution is approximately equal to: $\sim\sqrt{2}\sigma_{I_{leakage}}$, where $\sigma_{I_{leakage}}$ is the shot noise due to the leakage current of the sensing diode. Before sensor irradiation, when the leakage current is low, the noise of the SB pixel is smaller than that of the 3T pixel due to different pixel parasitic capacitance, which is larger for the 3T pixel. After irradiation, when the leakage current starts to be significant, the shot-noise contribution prevails, which is clearly seen for the SB pixel where the shot-noise contribution is multiplied by $\sqrt{2}$.

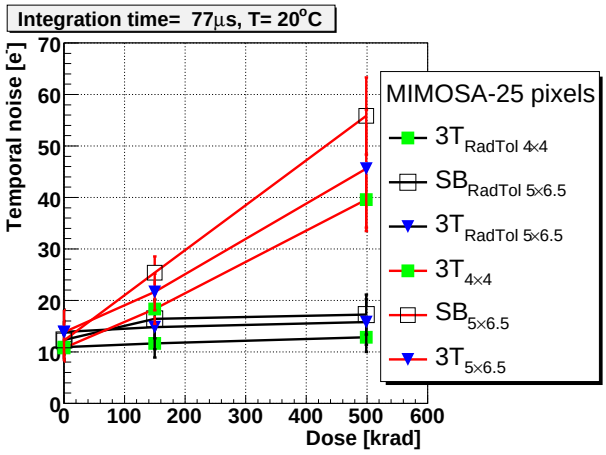


Figure 6.14: The temporal noise measured for the different sensing diodes implemented in the MIMOSA-25 sensors at a temperature of +20 °C. Please note that the uncertainties displayed here refer to the temporal noise dispersion. The statistical uncertainties of the mean values of the measured observable do not exceed 1%.

6.2.5 Conclusions

The industrial need to improve photo detectors embedded in a CMOS chip motivated the original use of a high-resistivity EPI layer. This layer can be depleted at a standard CMOS voltage, which opens up new perspectives for MAPS. This was the main motivation for MIMOSA-25, which has been recently built and extensively tested.

An important advantage of the depleted EPI layer is a faster charge-collection time, which translates into a more efficient charge collection. Results show that the charge collected by the seed pixels of MIMOSA-25 was ∼55% greater than in sensors with an undepleted EPI layer, while the thermal noise remained essentially unchanged. This translated into a high SNR, which was a factor of two larger than that observed for previous sensors featuring a standard

EPI layer. After the sensor was irradiated to $3{\cdot}10^{13}$ $\mathrm{n_{eq}/cm^2}$, the SNR decreased but was still at a level of 30 at room temperature. This value corresponds to the best SNR achieved before irradiation with sensors based on a standard EPI. The high SNR translates into a ϵ_{det} close to 100%, which was observed during tests with high-energy particle beam. The high SNR that is still present after irradiation to $3{\cdot}10^{13}$ $\mathrm{n_{eq}/cm^2}$ will most likely allow a similar ϵ_{det} to be achieved even after irradiation to $1{\cdot}10^{14}$ $\mathrm{n_{eq}/cm^2}$ at room temperature.

Another important aspect of MIMOSA-25 is the successful implementation of the radiation-tolerant diodes in the new technology. The measured leakage current for this type of pixel amounted to ∼100 fA after 500 krad. The temporal noise was estimated at room temperature with sensors running at a maximum clock frequency, corresponding to ∼77 µs of integration time. Depending on the diode type and size, the temporal noise was found to be in a range between 15 and 50 e^-, predominantly reflecting the diode leakage currents. The lowest noise value was observed for the $3T_{RadTol\ 4\times4}$ diode.

The SNR that was still high after neutron irradiation and the still low temporal noise of about $15e^-$ observed after 500 krad suggest that this sensor would most likely meet the CBM-experiment-radiation-tolerance requirements, which amount to $O(10^{13})n_{eq}/cm^2$ and to O(1)Mrad.

6.3 Radiation-tolerance of the XFAB 0.35-µm process with a standard EPI layer

The studies presented in Section 6.2 explored, for the first time, the capacity of a CMOS process based on a high-resistivity EPI layer for particle tracking. Improved non-ionizing radiation tolerance, by at least one order of magnitude with respect to sensors based on standard EPI layer, was observed. Unfortunately, highly granular sensors featuring fast, column-parallel architecture (see Section 5) with sparsified output could not be implemented in this technology. This is due to the feature size (0.6 µm) which was too large to accommodate signal processing microcircuitry in the pixel pitch of ∼20 µm needed to achieve the required σ_{res}. The space constraints could simply vanish by implementing CMOS sensors in technologies offering both a small feature size and a high-resistivity EPI layer for preserving the improved radiation hardness. The XFAB company claimed the availability, in the near future, of the currently established 0.35-µm CMOS process but based on an EPI layer with a resistivity of 500 Ω·cm – 2 kΩ·cm. Despite the standard EPI, the sensor prototype MIMOSA-24 was manufactured in the XFAB 0.35-µm process. The main motivation was to discover the pros and cons of this technology, for example, its ionizing radiation tolerance.

The following chapter will focus on the comparison of the basic features of the XFAB 0.35-µm process (e.g., temporal noise, leakage current, radiation hardness) with respect to the already known performance of sensors implemented in the AMS 0.35-µm technology.

6.3.1 The first prototype in the XFAB 0.35-μm technology – MIMOSA-24

Table 6.9 summarizes the salient features of the XFAB process investigated in this section, compared to those of the 0.35-μm AMS-OPTO technology, which is currently the baseline for the development of MIMOSA sensors.

Table 6.9: Comparison of the most relevant XFAB and AMS-OPTO-0.35-μm process parameters.

Process	**AMS**	**XFAB**
Process parameter	min. / typ. / max.	min. / typ. / max.
Minimum transistor channel width	0.35 μm	0.35 μm
Gate oxide thickness	7.1 / 7.6 / 8.1 nm	6.7 / 7.7 / 8.8 nm
Field oxide thickness	260 / 290 / 320 nm	280 / 330 / 370 nm
Area junction capacitance	0.08 fF/μm^2	0.11 / 0.12 / 0.13 fF/μm^2
Sidewall junction capacitance	0.51 fF/μm	0.27 / 0.36 / 0.45 fF/μm
Poly-DIFF capacitance	4.26 / 4.45 / 4.86 fF/μm^2	4.1 / 4.6 / 5.3 fF/μm^2
Substrate thickness	710 / 740 μm	725 μm
Substrate resistivity	14 / 19 / 25 Ω·cm	10 / 15 / 20 Ω·cm
EPI thickness	14 or 20 μm	15 μm
EPI resistivity	10 Ω·cm	6.8 / 8 / 9.2 Ω·cm
N-well depth	3.5 μm	1.1 μm
No. of meatal layers	4	4

The MIMOSA-24 prototype aimed at reproducing, to some extent, the MIMOSA-9 sensor implemented in the AMS 0.35-μm process and extensively studied in the past. The replication focused mainly on the sensing-diode size and type, pitch size, and in-pixel architecture. The array of MIMOSA-24 was divided in four parts, each part equipped with its own analogue output. Each subarray additionally featured a so-called "test row". The test rows contain pixels where the output signal is not provided by the sensing diode. Instead, the sensing diode is bypassed, and the signal comes from the reset transistors, as shown in Figure 6.15. When *Reset* is active, the *Vdiode* voltage is propagated directly to the source-follower input gate. The purpose of this test row is to simplify the process of calibrating the gain of each output.

In addition, each of the four subarrays mentioned was divided in two parts containing different pixel designs. In summary, eight different subarrays were implemented inside the sensor. Table 6.10 and Figure 6.16 contain details related to these subarrays. The implemented diodes featured sizes of 4.3×3.4, 5.0×5.0, or 6.0×6.0 μm^2. The pixels were enclosed in a pitch size of either 20 μm or 30 μm.

In order to verify whether the implementation of radiation-tolerant sensing diodes is possible with the XFAB 0.35-μm process, two types of the radiation-tolerant version of the sensing diode were implemented. They were named RadTol$_{AMS-like}$ and RadTol$_{ELT}$. The design of the RadTol$_{AMS-like}$ diode was meant to be as close as possible to the radiation-tolerant diode

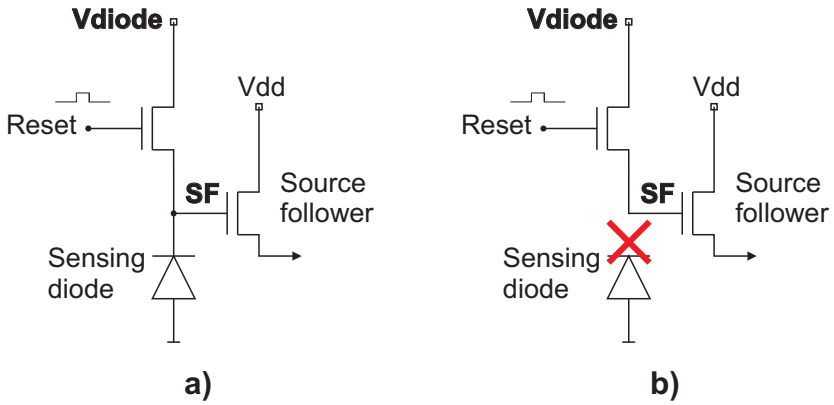


Figure 6.15: MIMOSA-24: (a) the standard pixel cell, (b) the pixel cell implemented in the test rows.

Table 6.10: MIMOSA-24 – description of implemented subarrays.

Matrix	Diode size [μm^2]	Pitch [μm]	Subarray size [pixels]	Architecture	$C_{parasitic}$ [a]
0	4.3×3.4	20	31×64	SB	7.4
1	6.0×6.0	20	32×64	SB	13.0
2	4.3×3.4	20	31×64	3T	7.4
3	6.0×6.0	20	32×64	3T	13.0
4	4.3×3.4	20	31×64	RadTol$_{ELT}$, 3T	7.4
5	4.3×3.4	20	32×64	RadTol$_{AMS}$, 3T	7.4
6	4.3×3.4	30	15×32	3T	7.4
7	5.0×5.0	30	16×32	3T	10.2

[a] The parasitic capacitance of the sensing diodes was calculated using the area junction capacitance and sidewall junction capacitance specified by the vendor (see Table 6.9). The calculations do not take into account contributions from reset (3T architecture), source-follower transistors, nor from the forward-biased diode (SB architecture). Those capacitances extracted during design phase with Cadence software were on the order of several fF.

design developed with the AMS technology (see Section 4.3 for more details). The idea of the AMS design was to break the path for the leakage current induced by ionizing radiation. This was realized in the AMS process by implementing the thin oxide around the sensing diode. This step required the violation of some design rules. However, due to the different design rules, such a diode could not be reproduced with the XFAB process. The radiation-tolerant diode implemented in the XFAB technology is shown in Figure 6.18(b). The thin gate oxide surrounding the n-well diode does not extend up to the n-well – p-well boundary, as was the case in the AMS designs (Figure 6.17). There is a 0.4-μm gap between the n-well and the gate oxide which does not exist in the AMS radiation-tolerant diode. Consequently, in the RadTol$_{AMS-like}$ diode, just as in the standard diode shown in Figure 6.18(a), the field oxide covers the n-well—p-well boundary. This could prove to be a weakness of all diodes

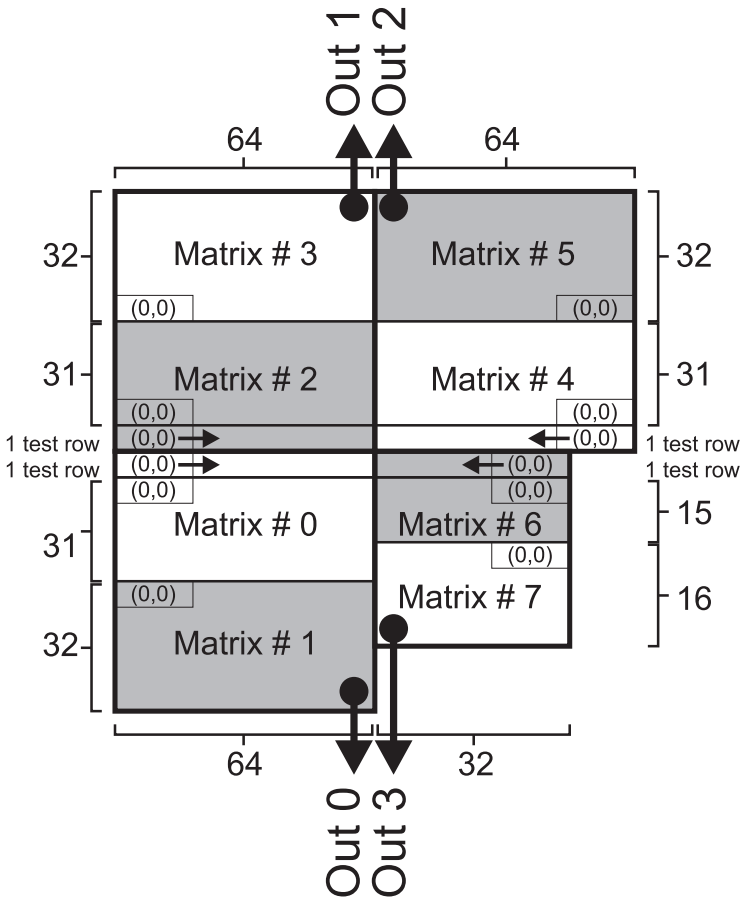


Figure 6.16: MIMOSA-24 – subarray implementation.

implemented in the MIMOSA-24 prototype.

The second radiation-tolerant diode, shown in Figure 6.18(c), was named RadTol$_{ELT}$. It exploited the ELT to implement the thin gate oxide around the sensing diode. In this case, the sensing diode is built inside a region enclosed by the n-channel ELT. The thin gate oxide of this transistor is used to break the path for the radiation-induced leakage current. Also in this case, the thin oxide does not cover the n-well – p-well boundary and is placed at a distance of 1.2 µm from the sensing diode.

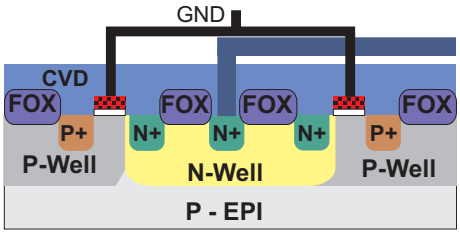
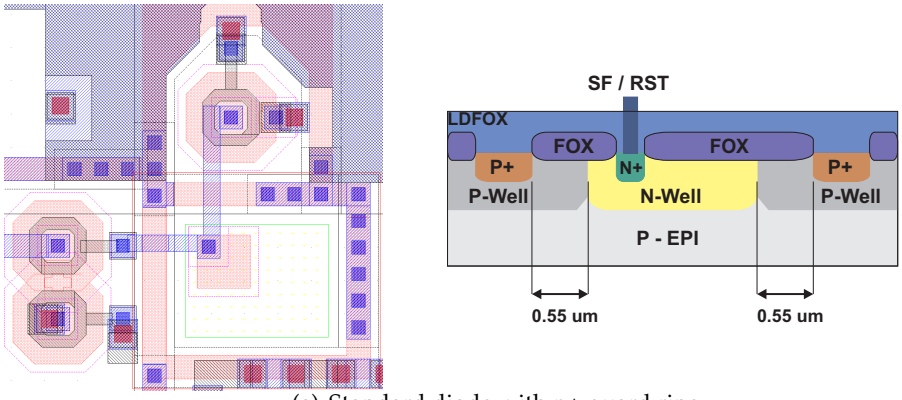
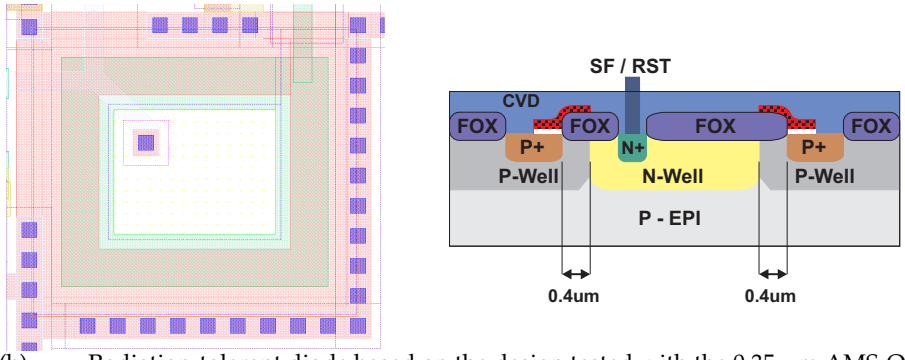


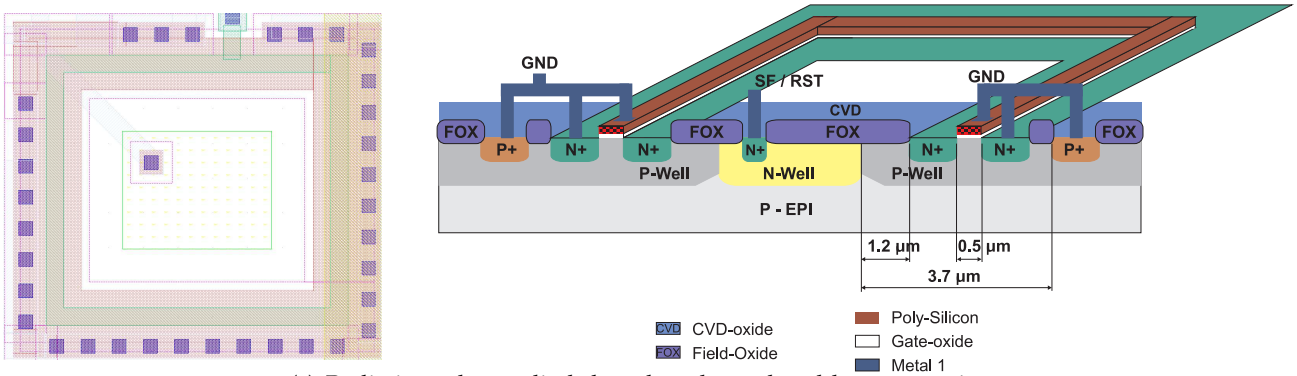
Figure 6.17: Cross-sectional view of the radiation-tolerant diode design implemented in the AMS technology.



(a) Standard diode with p+ guard ring.



(b) Radiation-tolerant diode based on the design tested with the 0.35-µm AMS-OPTO technology.



(c) Radiation-tolerant diode based on the enclosed-layout transistor.

Figure 6.18: Cross-sectional view of the different sensing diodes implemented in the MIMOSA-24 prototype.

Table 6.11: MIMOSA-24 – measured pixel capacitances. Uncertainties of $\leqslant$1%.

Diode type	Diode size	Pitch [µm]	Capacitance [fF]
SB	4.3×3.4 µm^2	20	13.0
SB	6.0×6.0 µm^2	20	18.2
3T	4.3×3.4 µm^2	20	15.0
3T	6.0×6.0 µm^2	20	18.5
3T RadTol$_{ELT}$	4.3×3.4 µm^2	20	14.9
3T RadTol$_{AMS}$	4.3×3.4 µm^2	20	14.3
3T	4.3×3.4 µm^2	30	15.8
3T	5.0×5.0 µm^2	30	17.0

6.3.2 Sensor gain calibration and pixel capacitance measurements

The sensor calibration procedure followed the one described in Section 4.2.3.1. In addition, the four test rows of MIMOSA-24 were used to measure the gain of the readout chain (see Section 4.2.3.3).

This gain was used to calculate the sensing-diode capacitance, according to the Equation 4.25 presented in Section 4.2.3.1. The measured values of the capacitances are presented in Table 6.11.

The presented values include the contributions to the pixel parasitic capacitance from all possible sources, mainly from the sensing diode, the reset transistor, a forward-biased diode, and the source follower. The measured values are in agreement with expectation. They are also in the range of parasitic pixel capacitances observed for similar sensing diodes implemented in the AMS-OPTO 0.35-µm process. The results suggest that pixels implemented in the XFAB process should have charge to voltage conversion factors (such as the voltage signals available at the pixel outputs) similar to those observed for the AMS pixels.

6.3.3 Leakage current and temporal noise measurements before irradiation

The leakage current before sensor irradiation was studied in a wide temperature range, that is from 0 °C to +40 °C. All the values were measured for sensors working with a readout clock frequency of 25 MHz, corresponding to an integration time of 164 µs. The *Vdiode* voltage was set to 2.1 V, which was in the middle of the operating range. Due to the in-pixel architecture, the leakage current was measured only for the 3T pixels.

Figure 6.19 depicts the temperature dependence of the leakage current. The results indicate that the leakage current before sensor irradiation is very low, $\sim$2 fA, and not sensitive to temperature.

The leakage currents measured before sensor irradiation for selected MIMOSA-24 pixel designs are presented in Table 6.12. The values of the leakage currents measured for the pixels implemented in the AMS-OPTO process featuring the same architecture and diode size are

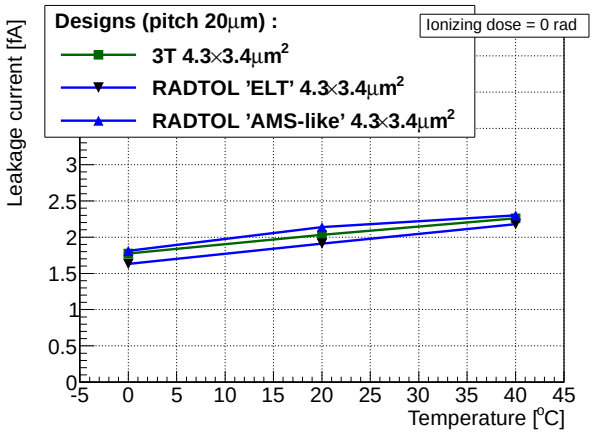


Figure 6.19: MIMOSA-24-sensor leakage current before irradiation as a function of the temperature.

given for comparison in the same table. One may observe that both processes exhibit small leakage currents of below 10 fA, resulting in a low contribution to the temporal noise.

Table 6.12: Comparison of the leakage currents measured at a temperature of +20 °C with sensing diodes implemented in the AMS (MIMOSA-15) and the XFAB (MIMOSA-24) 0.35-μm processes. All investigated diodes were 4.3×3.4 μm² in size.

Technology	Leakage current [fA] non-irradiated
AMS standard	<5 fA
XFAB Standard	1-3
AMS RadTol	6-9
XFAB RadTol$_{ELT}$	1-3
XFAB RadTol$_{AMS-like}$	1-3

Figure 6.20 presents the temporal-noise dependence on temperature for MIMOSA-24 sensors before irradiation. The temporal noise of MIMOSA-24 was almost stable in the whole investigated temperature range, but it was greater than the noise observed for similar architectures implemented in the AMS technology (typically 10-12e$^-$) [4]. The observed temporal noise did not originate from the sensing-diode shot noise but was instead dominated by the in-pixel electronics and the readout chain. The calculations performed for the 3T pixel featuring the 4.3×3.4 μm^2 sensing diode assessed the contribution from the leakage-current shot noise[15] to be in the range of 1.5 e$^-$.

Additional simulations performed with Spice[16] estimated the noise contribution from the in-pixel electronics and amplifiers used for the readout. The contribution from the processing electronics was assessed to be in the range of 13 e$^-$. Approximately 40% of this temporal noise

[15] Estimated using equation 4.7 for a leakage current of 2fA and an integration time of 164 μs.

[16] The Spice simulations of the in-pixel source-follower temporal noise were based on the standard transistor-noise models delivered by XFAB. In order to simulate the noise contribution originating from the components included on the motherboard, the models delivered by vendors were used.

was related to the source followers implemented inside the MIMOSA-24 pixels. The remainder was assigned to the motherboard components. After summing up all the contributions quadratically, the temporal noise amounted to about 15 e^-. A similar value was also measured with this sensor at a temperature of +20 °C (see also Figure 6.20).

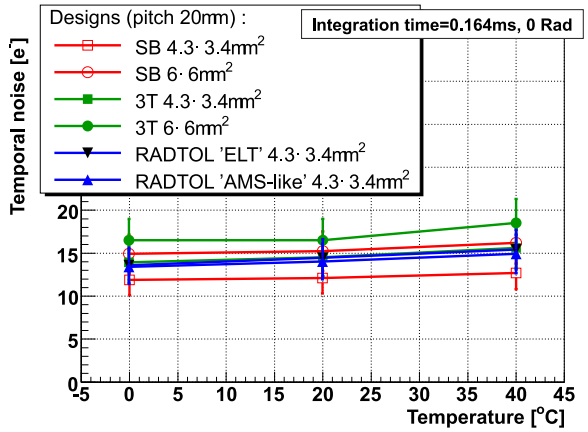


Figure 6.20:
Temporal noise as a function of temperature for the MIMOSA-24 sensor before irradiation. The uncertainties displayed refer to the temporal noise dispersion. Statistical uncertainties of the mean values of the measured observable do not exceed 1%.

The larger temporal noise observed for MIMOSA-24 can be explained by the relatively large temporal-noise contribution originating from the in-pixel source follower and the motherboard components as shown previously. This contribution was much lower in the case of the AMS prototypes. The reduction of this noise is closely connected to a better knowledge of the technology. This is an important aspect of the learning phase of the XFAB process, which started with the MIMOSA-24 prototype.

The temporal noise measured with the SB pixels was about 2e^- lower than with the 3T configuration. Those additional 2e^- should be attributed to the different parasitic capacitances, thus to the different charge-to-voltage conversion factors for both designs. In both cases, the contribution of the sensing diode to the pixel capacitance is the same. However, in the case of pixels in the 3T configuration, the reset transistor features a higher parasitic-capacitance contribution than the forward-biased diode.

6.3.4 Charge collection performance observed before irradiation

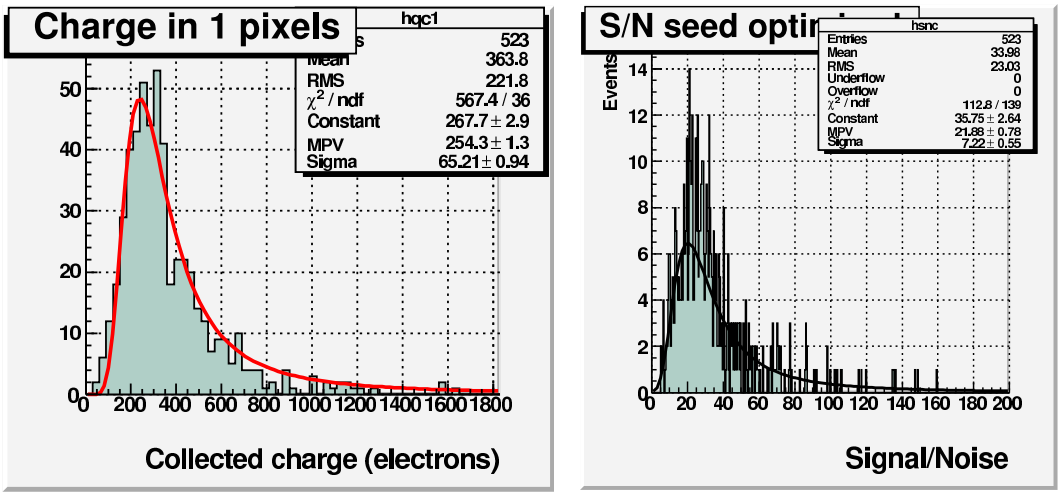
The CCE was studied at a maximum readout frequency of 25 MHz, translating to an integration time of 164 μs. The sensors were kept at a stable temperature of +20 ^{o}C.

The CCE estimated for sensors implemented in the 0.35-µm XFAB and AMS-OPTO processes are shown in Table 6.13. In the case of the AMS process, the data are related to the MIMOSA-9 and MIMOSA-22 prototypes, both featuring the same sensing diode (4.3×3.4 µm^2) as MIMOSA-24. The CCE observed with the MIMOSA-24 SB pixel before irradiation amounts to 20.8 $\pm$ 0.6 % for the seed pixel. This value compares well with the CCE obtained for the sensors implemented in the AMS 0.35-µm process: MIMOSA-9 and MIMOSA-22.

Table 6.13: Comparison of the CCE observed with pixels before irradiation from different MIMOSA prototypes, based on either the AMS or the XFAB technologies.

Prototype	Vendor	Diode size / type / pitch[µm]	Seed	3×3 cluster	5×5 cluster
MIMOSA-9	AMS	4.3×3.4 μm^2 / SB / 20	21.9 ± 0.7	70.2 ± 0.9	80.2 ± 1.0
MIMOSA-22	AMS	4.3×3.4 μm^2 / SB / 18.4	22.6 ± 0.7	75.4 ± 1.0	85.9 ± 1.1
MIMOSA-24	XFAB	4.3×3.4 μm^2 / SB / 20	20.8 ± 0.6	70.2 ± 1.0	80.3 ± 1.1

The MIMOSA-24 performance was also studied with high-energy particle beam. The following parameters were measured: the charge collected by the seed pixel, the SNR, and the ϵ_{det}. Figure 6.21 presents the distribution of the signal collected by the seed pixel (a) and the SNR distribution (b). The results of the tests performed with high-energy pion beam on pixels featuring 4.3×3.4 µm^2 sensing diodes are shown in Table 6.14. The same table contains values measured in the past with the AMS sensors featuring the same in-pixel architecture (SB) and sensing-diode size, MIMOSA-9 and MIMOSA-15.



(a) Signal distribution

(b) SNR distribution

Figure 6.21: Signal and SNR distributions observed for the MIMOSA-24 prototype before irradiation.

The value of the charge collected by the seed pixel of MIMOSA-24 was observed to be slightly lower than the one measured with the AMS sensors. This result is consistent with the one obtained in the laboratory using an ^{55}Fe source.

All the sensors compared in Table 6.14 had different SNR values, reflecting predominantly their different temporal noise. The lowest SNR was observed for the XFAB design but as already explained in Section 6.3.3, the noise properties of the MIMOSA-24 sensor and its motherboard were not optimized. Despite this relatively high temporal noise, the observed value of the SNR was still high enough (∼22) to achieve a ϵ_{det} close to 100%.

Table 6.14: Parameters measured during tests with high-energy pion beam: MPV of charge [e^-] collected by the seed pixel, corresponding SNR (MPV), and ϵ_{det}. All parameters assessed before sensor irradiation and at room temperature.

Prototype	Signal [e^-]	SNR	Efficiency[%][a]
MIMOSA-24	254.3 ± 0.9	21.9 ± 0.79	$\sim$100
MIMOSA-9	224.5 ± 1.6	25.3 ± 0.2	$\sim$100
MIMOSA-15	253.7 ± 0.6	27.8 ± 0.5	$\sim$100

[a]The uncertainty on the ϵ_{det} is typically on the order of a few 0.1 %.

6.3.5 Ionizing radiation tolerance

Another aim of the MIMOSA-24 implementation was characterizing the radiation tolerance of the 0.35-µm XFAB process and comparing it with the one observed for the AMS 0.35-µm process. In order to investigate the radiation tolerance of the XFAB 0.35 µm process, laboratory tests determining the leakage current and noise were carried out before and after sensor irradiation[17]. The tests were launched at various temperatures and integration times.

Several parameters can be examined to compare the performance obtained with different technologies. For example, the noise level, as a prevailing parameter for the ϵ_{det}, should have priority in the investigation. However, the temporal noise measured at the end of the readout chain is a convolution of components originating from various sources. These sources are located in the sensor itself as well as in the accompanying readout electronics, such as the motherboard. The temporal noise contribution from the sensor originates from the in-pixel electronics, mainly from the sensing diode (shot noise) and the source follower (see Section 4.1.4.1). All the previously mentioned temporal noise contributions may vary from one sensor to the next, especially for those implemented in different processes. The differences observed between sensors cannot be simply attributed to a well-defined origin, at least quantitatively, by measuring the noise of different sensors and under various conditions. Since it is well-known that ionizing radiation will mainly impact the diode leakage current, which can be measured with a precision of about 1 fA, the measurements of the latter should be preferred over noise assessment.

The leakage-current measurements deliver additional information that allows for a better comparison of the tolerance to radiation between different processes. The knowledge gained about the leakage current allows the noise originating from the microcircuitry to be distinguished from the noise coming from the sensing-diode leakage current itself. At the first order, the leakage-current measurements are independent of the in-pixel electronics (e.g., source follower), motherboard, and other associated devices. Since the leakage current is strongly temperature dependent, the comparison of the performance between two different processes is only meaningful if the leakage current is studied at the same temperature.

[17]Several samples of the MIMOSA-24 sensor were irradiated to different ionizing doses of 150 krad, 500 krad, and 1 Mrad.

6.3.5.1 Leakage-current measurements after irradiation.

The leakage-current dependence on the ionizing dose was studied in the same temperature range (from 0 °C to +40 °C) as for the sensor samples before irradiation. The other conditions, such as the integration time (164 µs) and *Vdiode* voltage (2.1 V), were conserved.

Table 6.15 shows the leakage currents measured after 1 Mrad at +20 °C. To compare the radiation hardness of the XFAB 0.35-µm process with the AMS-OPTO 0.35-µm process, the values of the leakage currents measured under the same conditions with the AMS sensors (featuring the same architecture and diode size) are given in the same table. One can observe that even the standard pixels implemented in the XFAB process features a better radiation tolerance than the radiation-tolerant pixels from the AMS-OPTO technology. For example, the leakage current of ∼36 fA measured with the XFAB standard 3T pixels is about half of the one observed with the radiation-tolerant pixels implemented in the AMS-OPTO process.

Table 6.15: Comparison of the leakage currents measured at 20 °C with sensing diodes implemented in the AMS (MIMOSA-15) and the XFAB (MIMOSA-24) 0.35-µm processes. All investigated diodes featured a size of 4.3×3.4 µm^2. Statistical uncertainties of the mean values of the measured observable do not exceed 1%.

Technology	Leakage current [fA] 1 Mrad
AMS standard	>500 fA
XFAB Standard	35.8
AMS RadTol	78.8
XFAB RadTol$_{ELT}$	44.5
XFAB RadTol$_{AMS}$	62.3

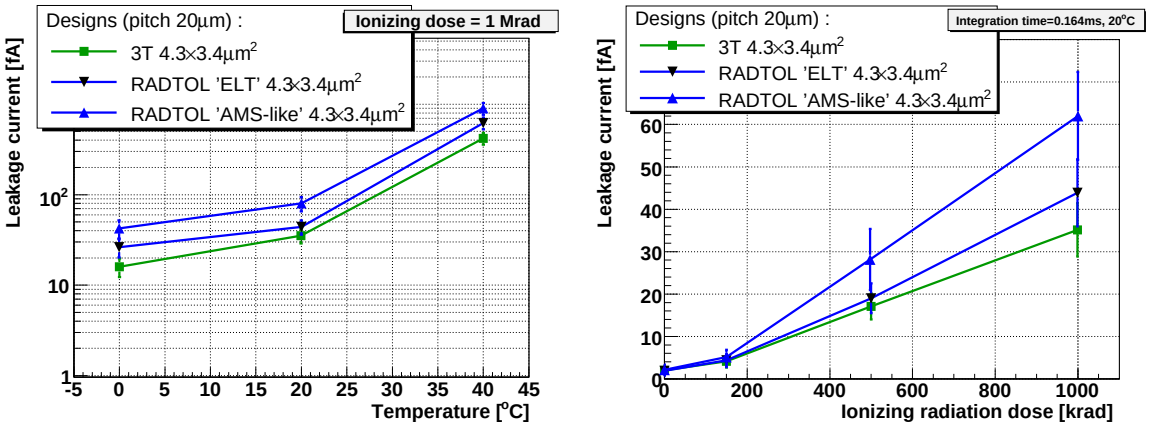
Instead, the radiation-tolerant diodes implemented in the XFAB process featured a leakage current that was higher than the one measured with standard diodes. One can conclude that the implementation of the radiation-tolerant diodes in the XFAB 0.35-µm technology was not successful. The radiation-tolerant XFAB diodes were implemented in a different way than those made previously in the AMS process, but nevertheless, the thin gate oxide surrounded the sensing diode. The origin of this phenomenon is not yet understood well.

This observation becomes even more puzzling if one recalls the results presented in Section 6.2.4.1, related to the leakage-current comparison of the radiation-tolerant and non-radiation-tolerant pixels implemented in the MIMOSA-25 prototype (XFAB 0.6-µm process). The MIMOSA-25 radiation-tolerant diode was identical to the RadTol$_{AMS}$ design of MIMOSA-24; however, in the case of the 0.6-µm process, the observed performance was as expected.

To exclude any possible mistake linked to the irradiation procedure, some additional MIMOSA-24 prototypes were irradiated under the same conditions and with the same integrated doses. The irradiated sensors were characterized in a similar way with regard to integration time and temperature range. The leakage currents measured for samples originating from two different irradiation runs were the same taking into account the

uncertainty on the delivered dose of about 20%.

The leakage current was also measured as a function of the temperature and the integrated dose. The results are depicted in Figures 6.22(a) and 6.22(b). Figure 6.22(a) shows the temperature dependence of the leakage current for the device irradiated up to 1 Mrad. The measurements agreed with the expectations. For example, the leakage current measured with the standard 3T pixels was observed to increase from ∼15 fA at 0 °C to ∼400 fA at 40 °C. The leakage current was observed to increase linearly with the integrated ionizing dose. The same tendency was already observed for CMOS sensors by several authors and reported in [161, 162, 163, 164].



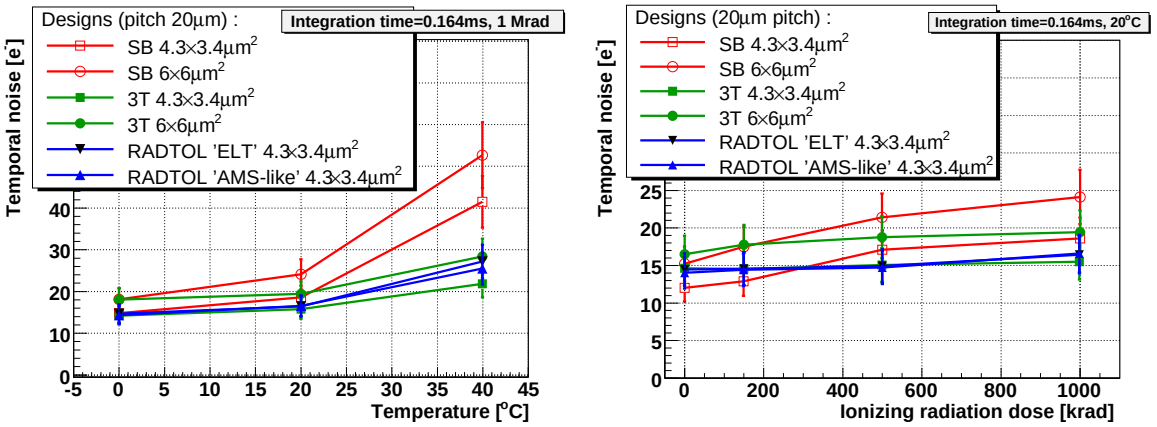
(a) (b)

Figure 6.22: MIMOSA-24 – laboratory test results: (a) Leakage current as a function of temperature for the sensors exposed up to 1 Mrad. (b) Leakage current measured at a constant temperature of +20 °C as a function of integrated dose. The uncertainties shown refer to the leakage-current dispersion. Statistical uncertainties of the mean values of the measured observable do not exceed 1%.

6.3.5.2 Temporal-noise measurement after irradiation

Figure 6.23 presents the temporal-noise dependence on the temperature (a) and integrated dose (b) for sensors after irradiation of up to 1 Mrad. The changes of the temporal noise with temperature reflected the variation of the sensing diode leakage current presented previously in Figure 6.22(a). This observation was valid for all the pixels implemented inside MIMOSA-24 featuring the 3T architecture. For a temperature above 20 °C, the temporal-noise increase measured for all pixels was not significant, about 2 e^- larger than the one observed for sensors before irradiation. However, at a temperature of 40 °C, the temporal noise increased significantly to ∼23 e^- for pixels featuring a standard diode and the 3T architecture.

The most significant increase in the temporal noise was observed for pixels featuring the



(a) (b)

Figure 6.23: MIMOSA-24 – laboratory test results: (a) Temporal noise as a function of temperature for the sensors irradiated up to 1 MRad. (b) Temporal noise as a function of integrated dose at a constant temperature of +20 °C. Please note that the uncertainties shown here refer to the temporal noise dispersion. Statistical uncertainties of the mean values of the measured observable do not exceed 1%.

SB architecture. The temporal noise measured for this architecture at 20 °C before sensor irradiation was the lowest among all the implemented pixels. However, after irradiation above 300 krad, the temporal noise started to be systematically higher than for 3T pixels, finally amounting to 18 e^- at +20 °C for 4.3×3.4 μm^2 diodes after 1 Mrad. The same tendency was already noted in the case of MIMOSA-25 and explained in Section 6.2.4.2.

6.3.6 Non-ionizing-radiation-tolerance assessment

The tolerance of the 0.35-µm XFAB process to non-ionizing radiation was determined by irradiating MIMOSA-24 prototypes up to $3{\cdot}10^{12}$ n_{eq}/cm^2 and $1.3{\cdot}10^{13}$ n_{eq}/cm^2. For the sake of comparison, the neutron fluences were similar to those already used in the past for the irradiation of sensors implemented in the 0.35-µm AMS process.

The CCE was estimated and compared with the results obtained in the past with sensors fabricated in the AMS processes. The results are shown in Table 6.16 for a fluence of $3{\cdot}10^{12}$ n_{eq}/cm^2. In the case of the AMS process, the data are related to the MIMOSA-22 prototypes, featuring the same pixel architecture (SB) and sensing-diode size (4.3×3.4 μm^2) as MIMOSA-24 but a slightly different pitch of 18.4 µm. The CCE of the pixels implemented in the XFAB process was observed to be systematically lower after irradiation than for the pixels implemented in the AMS process.

Among the possible explanations of this phenomenon, the most probable one points towards differences in the pitch size and the EPI-layer thickness. After irradiation, the lifetime of the diffusing charge carriers is strongly reduced due to the defects in the silicon lattice. As observed

Table 6.16: Comparison of the CCE after irradiation to 3·10^{12} n_{eq}/cm^2 of sensors manufactured in the 0.35-µm AMS-OPTO and XFAB processes. In both cases, the SB-pixel architecture featuring a 4.3×3.4 µm^2 sensing diode was studied.

Vendor	Prototype	Pitch[µm]	Seed [%]	3×3 cluster [%]	5×5 cluster [%]
AMS	MIMOSA-22	18.4	19.1 ± 0.7	60.1 ± 1.0	66.2 ± 1.1
XFAB	MIMOSA-24	20	16.6 ± 0.6	48.5 ± 0.8	53.4 ± 0.9

in the past and mentioned in Section 4.3.3, increasing the distance between sensing diodes from 10 µm to 20 µm significantly reduced the charge available in the seed pixels. Consequently, the non-ionizing radiation tolerance was reduced by a factor of five. The 1.6-µm difference in the pitch size between MIMOSA-24 and MIMOSA-22 may lead to a different CCE than observed here.

On the other hand, a thicker EPI layer results in an increase in the average distance the charge carriers have to travel before being captured by a sensing diode. As a consequence, the signal electrons have a higher probability of being trapped in lattice defects, which translates into greater charge losses. The EPI-layer thickness provided by both the AMS and the XFAB process specifications is comparable. However, past observations regarding the AMS sensors have shown that the presumed ∼14-µm thickness of an EPI layer given by the vendor was different from the one assessed with high-energy pion beam, which indicated a 11-µm thickness. Due to limitations of the acquisition system used during the tests with high-energy pion beam, this cross-check could not be performed with MIMOSA-24.

The performance of the irradiated MIMOSA-24 sensors was also studied with high-energy particle beam. The MPVs of both the signal collected by the seed pixel and the SNR distribution measured after irradiation up to 3·10^{12} n_{eq}/cm^2 are given in Table 6.17. In order to compare the results measured with MIMOSA-24 to those obtained with previous MAPS prototypes implemented in the AMS process, the same parameters are also given for MIMOSA-9 and MIMOSA-15. Any comparison of performance between those three sensors should be done very carefully because they were measured under slightly different conditions. MIMOSA-24 was measured at room temperature while the AMS sensors were measured at a temperature of -20 °C. The integration time was also different for all three sensors: 164 µs for MIMOSA-24, 700 µs for MIMOSA-15 and 1.6 ms for MIMOSA-9.

If one considers the amount of charge collected by the seed pixels of the three investigated sensors, the largest charge is stored in the MIMOSA-24 diodes. This can be explained by the different facilities used to irradiate MIMOSA-24 and MIMOSA-9/MIMOSA-15: MIMOSA-24 was irradiated in Munich with ∼1MeV neutrons, while in the case of the AMS sensors, irradiation took place in the nuclear reactor in Ljubljana, where cold neutrons prevailed. More details about possible differences in radiation damage due to irradiation in different facilities can be found in Section 4.2.5.2 of this document. Recalling that sensors irradiated with cold

Table 6.17: The MPV of the collected charge [e^-] in the seed pixel and the corresponding SNR. Both parameters were assessed after the irradiation of MIMOSA-24 with neutrons. The table also shows these observables for MIMOSA-9 and MIMOSA-15, together with the ionizing doses at which those observables were measured. MIMOSA-24 was studied with an integration time of 164 μs and a temperature of +20 °C. MIMOSA-9 and MIMOSA-15 were studied at +20°C with different integration times: 1.6 ms and 700 μs, respectively. The sensors all feature the same pixel pitch of 20 μm.

Prototype	Signal [e^-]	SNR	Efficiency[%]	Temperature	$t_{integration}$ [ms]
MIMOSA-24	$3{\cdot}10^{12}$ n_{eq}/cm^2				
	180.2 ± 0.9	13.72 ± 0.46	94.8 ± 3.2	+20 °C	0.164
MIMOSA-9	$1{\cdot}10^{12}$ n_{eq}/cm^2				
	154.8 ± 0.1	19.76 ± 0.16	99.7 ± 0.4	-20 °C	1.6
MIMOSA-15	$2.1{\cdot}10^{12}$ n_{eq}/cm^2				
	134.4 ± 0.2	14.7 ± 0.3	99.32 ± 0.5	-20 °C	0.7

neutrons seemed to be more affected than the ones irradiated with fast neutrons could also explain any differences in charge collection between the three sensors compared here.

Despite the larger charge collected by the seed pixel, MIMOSA-24 exhibits the worst SNR of ∼13.7, translating to a low[18] ϵ_{det} with respect to requirements. In the case of MIMOSA-9, which exhibits the lowest charge collected by the seed pixel, the SNR was larger (14.7). The low SNR observed for MIMOSA-24 is most likely due to the influence of the source follower and the motherboard components, resulting in a temporal noise for this sensor that was a few electrons larger than the one observed for the AMS devices. This larger noise could easily translate into the SNR differences discussed here.

In the end, any straightforward performance comparison of neutron-irradiated AMS and XFAB sensors is difficult. One could assume that the temporal noise will be optimized for future sensors implemented in the XFAB process. Therefore, it is possible that due to the larger charge collected with MIMOSA-24 pixels, the SNR of sensors fabricated in the XFAB process will be larger than the one observed for the AMS sensors. Consequently, the higher SNR would most likely allow slightly better non-ionizing radiation tolerance to be achieved.

6.3.7 Conclusions on the XFAB 0.35-μm process

The studies performed with the MIMOSA-24 prototype allowed for the first assessment of the detection performance of the 0.35-μm XFAB CMOS process. The performance observed before sensor irradiation (e.g.,regarding pixel capacitances or the leakage current) was equivalent to that observed in the past with sensors implemented in the 0.35-μm AMS process. The temporal noise measured for the XFAB designs was slightly higher than the one observed for the AMS pixels. This was attributed to the sensor design, which was not yet optimized for this process examined for particle tracking for the first time.

[18]The goal is to achieve a ϵ_{det} of ≥99%.

The ionizing radiation tolerance was assessed with sensors irradiated up to 1 Mrad. The leakage current of the MIMOSA-24 standard diodes was in the range of the leakage current measured with radiation-tolerant diodes implemented in the AMS technology. Unfortunately, the radiation-tolerant diodes implemented in MIMOSA-24 were not reproduced correctly. They exhibited a slightly larger leakage current than the standard diodes. Any future developments based on the XFAB technology should therefore concentrate on a better reproduction of the radiation-tolerant diodes, which should limit the leakage current measured after ionizing irradiation.

The non-ionizing radiation tolerance was assessed with sensors irradiated up to $3{\cdot}10^{12}$ $\mathrm{n_{eq}/cm^2}$. The results indicate that the charge collection performance measured with the MIMOSA-24 prototypes before and after irradiation was slightly better than that obtained in the past with sensor prototypes implemented in the AMS-OPTO 0.35-µm technology. However, due to the higher temporal noise observed for the XFAB sensors, the SNR after irradiation did not allow better non-ionizing radiation tolerance to be achieved than that observed for similar AMS sensors (2-3$\cdot10^{12}$ $\mathrm{n_{eq}/cm^2}$).

In summary, the satisfactory ionizing radiation tolerance observed for current XFAB sensors combined with the high-resistivity EPI layer of the future 0.35-µm XFAB process makes this technology attractive for further MAPS development.

6.4 Conclusions and summary

To reduce the readout time and allow for data sparsification, the sensors were organized in columns which are read out in parallel. The pixels became more complex and they required more space for implementation. The larger pitch needed to fit the in-pixel electronics contradicted with the small pitch required to achieve a good non-ionizing radiation tolerance. Therefore, there was a strong interest in improving the non-ionizing radiation tolerance without needing to decrease the pixel pitch. The main objective was to exchange the charge-collection process, which limits the tolerance of the currently established process, for MAPS implementation. The currently established process utilizes a low-resistivity EPI layer where the electrons generated by impinging particles are thermally diffused towards the collecting implants. The aim of this thesis was to investigate CMOS processes where charge collection is enhanced by an electric field.

The first investigated technology, BiCMOS 0.25 µm, offered an enhanced charge collection due to a graded EPI layer, resulting in an internal electric field builtup. However, the benefits of this technology regarding the enhanced charge collection unfortunately cannot be used as the process is not tolerant to ionizing radiation.

The second process studied was the XFAB 0.6 µm, utilizing a high-resistivity EPI layer. As the layer was partially depleted, the charge spread between the neighboring pixels was limited. Moreover, the charge collection was much faster than in the case of undepleted EPI layers. As

a consequence, a much higher charge was collected by a single pixel than in the case of pixels implemented in standard processes based on low-resistivity EPI layers. This was reflected immediately in an increase in the non-ionizing radiation tolerance. These results suggest that the radiation hardness of MAPS featuring a high-resistivity EPI can be increased even beyond $3{\cdot}10^{13}$ $\mathrm{n_{eq}/cm^2}$. However, due to a large feature size, the XFAB 0.6-µm process cannot be used to implement MAPS with in-pixel signal processing. The pixel size would become too large with respect to the requirements of the σ_{res}.

These excellent results, combined with the likelihood that this technology would be soon accessible with a feature size of 0.35 µm, triggered studies of the XFAB 0.35-µm process (still restricted to a standard epitaxial layer), which is similar to the AMS-OPTO process used previously. The tolerance of the XFAB 0.35-µm process to non-ionizing radiation was found to be similar to that obtained with the AMS technology. The XFAB 0.35-µm process was observed to be more tolerant to ionizing radiation than the AMS 0.35-µm process: the leakage current observed at room temperature with the XFAB pixels was a factor of two smaller than for radiation-tolerant AMS pixels.

The breakthrough in the development of radiation-tolerant CMOS sensors was achieved with sensors based on a high-resistivity EPI layer. The non-ionizing radiation tolerance of $3{\cdot}10^{13}$ $\mathrm{n_{eq}/cm^2}$ was demonstrated at room temperature with sensors featuring a pitch size of 20 µm. This achievement triggered a new generation of CMOS pixel sensors dedicated to particle tracking which relies on a high-resistivity EPI layer. It also shows that the development of CMOS sensors is on a good track to meet the requirements of the CBM experiment.

Further studies will focus on reproducing some of the sensors, for example, the one with data sparsification (see Section 5.5), in technologies offering such high-resistivity EPI layers. The first steps towards reproducing sensors by utilizing the AMS 0.35-µm process featuring a high-resistivity ($\sim$400 $\Omega{\cdot}$cm) epitaxial layer have been recently undertaken at the IPHC-Strasbourg.

7 Modeling of the radiation effects in the Charge-Coupled Devices

A part of this thesis was devoted to studying the radiation tolerance of Charge-Coupled Devices. The CCDs have been proposed to supply the vertex detector of experiments planned for the International Linear Collider [3]. The studies were addressed within the framework of the LCFI collaboration settled in the United Kingdom. The collaboration is pursuing an ambitious research program to develop a pixel-based vertex detector for the ILC. The CCDs have been used for many years as vertex detectors in high energy physics experiments, for example, the NA-32 experiment [165]. These sensors have demonstrated excellent performance in terms of the σ_{res} and material budget. The work presented in this chapter addresses the development of the TCAD simulation model for assessing influence of radiation-induced effects on the charge transfer in CCDs.

7.1 Confrontation of the CCD performance with the ILC experiment requirements

An important requirement of a vertex detector is to remain tolerant to radiation for its anticipated lifetime. CCDs suffer from both surface and bulk radiation damages. However, when considering the charge transfer losses in buried channel of the CCD, only effects introduced into the detector bulk are important. As discussed in Section 2.4.2.2, the lattice defects introduced during particle interactions with a detector material create energy levels between the conduction and valence bands. Those defects, called also traps, are able to capture electrons and emit them back to the conduction band after a certain time. This leads to the signal charge losses during its transfer from the interaction point to the output buffers and to a subsequent decrease in signal-over-noise ratio governing the sensor performance.

In the investigated CCDs, the charge is generated in a thin EPI layer and drifts towards an n-buried channel where it forms charge packets. The charge movement is enhanced by an electric field, which reaches its maximum in the channel.

In the CCD channel, the movement of electrons towards the output buffer is forced by periodical changes of clock pulses delivered to the transfer gates. The signal packets have to travel long distances, sometimes several centimeters, before they reach the output buffer and therefore a greater amount of traps interacts with signal packets.

The Charge Transfer Inefficiency (CTI) is the fractional loss of charge after transfer across one pixel. An initial charge Q_0 after being transported across m pixels is reduced to:

$$Q_m = Q_0(1 - \mathrm{CTI})^m \tag{7.1}$$

For CCDs devices containing many pixels, CTI values around 10^{-5} are not negligible.

The CTI depends on many parameters which can be divided in two groups. The first group reflects radiation damage in the detector bulk: trap energy levels, trap capture cross-sections and concentration. The second group covers the operating conditions, for example, readout frequency or temperature. Variations of the CTI with the readout frequency and its strong temperature dependence were published by several authors [166, 167, 78, 168, 169].

The beam structure of the ILC has significant implications for the design and readout of CCD sensors as possible candidates for the vertex detector. In order to keep occupancy below 1%, the vertex detector has to be read out several times during a single bunch train. To meet this requirement, a fast readout of the CCDs composing the vertex detector is necessary. CCDs with a sequential readout are simply not fast enough. This motivated the R&D towards CCD with a column-parallel architecture.

Figure 7.1 shows schematically the organization of a sequential and a column-parallel CCD. The time t_p needed to read out a sequential CCD is significantly longer than the readout time t_p of a column-parallel architecture:

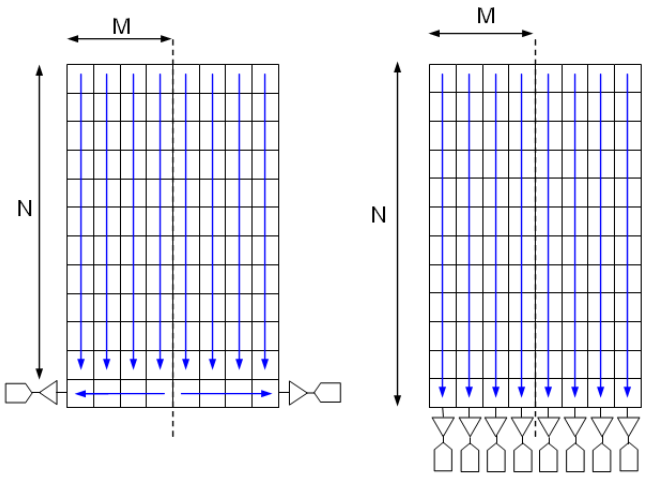


Figure 7.1: Readout organization of Charge-Coupled Devices: standard readout (left) and column-parallel readout (right).

$$t_s = \frac{N \cdot M}{f_{out}} \tag{7.2}$$

$$t_p = \frac{N}{f_{out}} \tag{7.3}$$

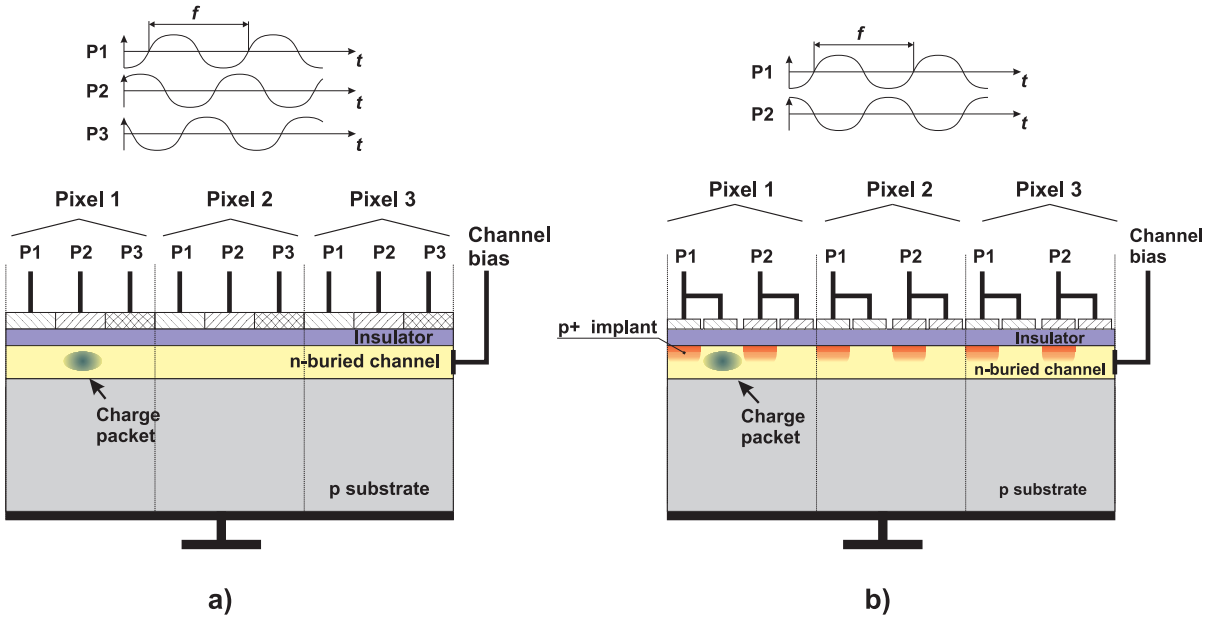


Figure 7.2: Implementation of the 3-phase and 2-phase CCD: (a) In the 3-phase CCD the pixel is defined by the three signal gates P1,P2 and P3. Sinusoidal signals are applied to the gates to move the charge towards the next pixel. The control signals are shifted in phase by 120°; (b) In the case of a 2-phase CCD, the pixel is defined by gates P1 and P2. The two control signals are in the opposite phases. The p+ implants introduce the potential barriers to keep charges under the pixel without a need of applying signals to the gates.

where f_{out} is the readout frequency, M and N correspond to the number of columns and rows, respectively.

The change in the CCD sensor from the serial to the parallel architecture was followed by modifications of the physical structure of the device. The new CCD architecture, called 2-phase CCD, was based on a p-substrate with a ∼20-µm EPI layer, which determines the sensor's sensitive volume. Figure 7.2 compares the "old" 3-phase CCD architecture (a) and the 2-phase one (b). The 2-phase CCD features a non-uniform channel doping with p-type implants, used to form the potential barriers for charge separation. Those p-type implants define also the pixel pitch in the vertical direction. As a consequence, electrons are stored in the potential wells under the part of the gate structure next to the implant, even when the clock pulses are disconnected. This feature, accompanied by a reduced number of steering signals (clock pulses P1 and P2) needed for the charge transfer, decreases the power consumption of the device. The charge transfer from one gate to another is carried out by means of only two periodic clock pulses, P1 and P2. Both pulses have the same amplitude but opposite phase.

7.2 Charge transfer losses in 2-phase CCD devices

The charge transfer losses in the 2-phase CCD have two main origins. The first one is related to insufficient amplitude of the control signals. The seconds comes from interactions of signal electrons with radiation-induced bulk defects. Both origins will be discussed in the following sections.

7.2.1 Insufficient gate voltage

In the biased 2-phase CCD sensor, the signal electrons are stored in the potential wells under the part of the gate structure next to the p-implants. In order to transfer a signal-charge packet from one gate to the next one, the two, phase-shifted, sinusoidal clock signals are applied. As a consequence, a non-uniform electrostatic potential between these gates is formed. Electrons drift to the gate with a higher potential. If the electrostatic potential applied to the gates is smaller than the potential barrier induced by the p-implant, the charge is not transferred. However, above a certain voltage, the transfer is fully efficient. To find the minimum gate voltage which allows achieving an efficient charge transfer, TCAD simulations and laboratory tests were performed within the scope of this thesis. They will be described in the following.

7.2.2 Bulk radiation damage

A presence of defects introduced by radiation has a strong influence on the charge transfer losses in a CCD channel. During a CCD readout, charge is transferred from pixel to pixel along a CCD column. In this process, radiation-induced bulk defects can trap part of the charge and release it with some delay. As a consequence, a rise in the CTI is observed. In the trapping process, electrons are captured from the signal packet and each captured electron fills a trap. This occurs with a time constant τ_c (see Equation 2.8 in Section 2.4.2.2). The electron emission process is described by the emission of captured electrons from filled traps back to the conduction band, and into a following signal packet with the time constant τ_e. The latter is an exponential function of temperature and a defect energy level.

At low temperatures, the emission time constant τ_e can be very large, on the order of seconds. For a typical clock frequencies used for CCD readout, the time needed for the charge transfer through a single pixel is on the order of nanoseconds. In the case of a large τ_e, the electron traps remain filled for a time much longer than the one needed for the charge transfer through a pixel. Consequently, further trapping of the signal electrons is not possible and the CTI becomes small at low temperatures.

For the device working at high temperatures, the emission time constant decreases and become even shorter than the time needed for the charge transfer through a pixel. In such conditions, the signal electrons are trapped and emitted back immediately to the conduction band. The trapped electrons may therefore join the same signal packet and be transferred to the next pixel. Consequently, the CTI for devices working at high temperatures decreases.

When the emission time constant is comparable to the time needed for the charge transfer from one pixel to another, the highest CTI values are observed.

The probability of capturing the signal electrons by radiation-induced defects is also a function of the charge transfer velocity through the CCD channel. For example, in the case of charge transfer with lower frequency of the clock pulses, the velocity of the charge packets in the channel decreases. Thus traps have more time to interact with signal carriers and the charge transfer loses are more pronounced. One may expect the opposite behavior (faster charge transfers) to be observed for higher clock frequencies.

7.3 Simulation model

In order to predict charge transfer efficiency in an irradiated CCD, a simplified model of the device was implemented in the TCAD software[1]. The simulations carried out within the research program of the LCFI collaboration aimed at reproducing the behavior of the 2-phase CCD with column-parallel readout, called CPC-1. It was planned to compare simulation results with test results from an irradiated CPC-1 sensor. Data from such tests could also be used for final model tuning. The CPC-1 was manufactured by "E2V Technologies" and featured 20×20 μm^2 pixels organized in a matrix with dimensions of 400×750 pixels. The following sections will discuss the sensor specifications used for numerical simulations.

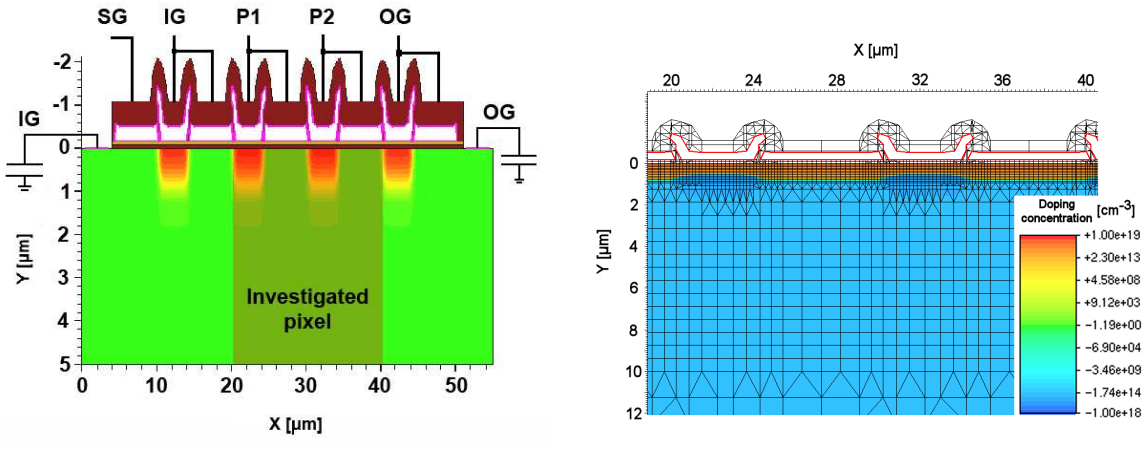
7.3.1 Device specification in ISE-TCAD

Among several important constrains related to device simulations in the TCAD software, one of them seems to have a special importance: the calculation time. The latter can vary from single hours to weeks or months, depending on the available hardware, the required precision and the simulated device structure. The simulation of the full 3D model of the CPC-1 sensor would require a very long time (accounting for the hardware used). This motivated the development of a less complicated 2D model, which is shown in Figure 7.3(a) and discussed in the following.

The simulated device features the n-type-buried channel with additional p-type-silicon implants implemented inside. Following the real CPC-1 sensor, the model is based on a p-type, 20 μm thick EPI layer. As the active volume of the CPC-1 is determined by the EPI layer, the p+ substrate is not implemented in the model. The gates are made of PolySilicon with a Silicon Nitride (Si_3N_4) layer beneath, and they are surrounded by silicon dioxide (SiO_2).

The simplified TCAD model of the CPC-1 sensor features a single pixel placed underneath the P1 and P2 transfer gates. In order to bias the simulated device, a DC voltage is applied between the input drain (ID), the output drain (OD), and the substrate. Other gates are used to emulate the charge transfer process along the buried channel. The applied voltages as well as

[1]The ISE-TCAD package (version 7.5) [158], and the DESSIS program (Device Simulation for Smart Integrated Systems) were used for this purpose.



(a) (b)

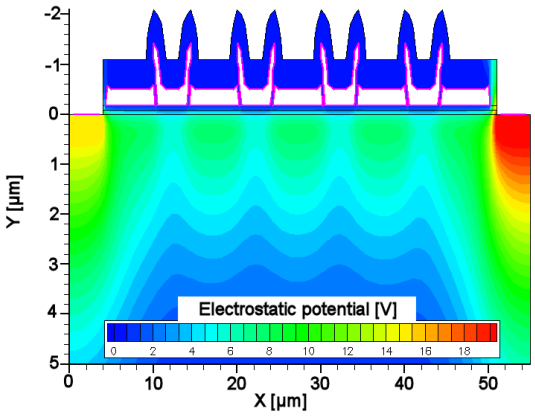
Figure 7.3: Figure (a) shows a simplified 2D TCAD model of the 2-phase CP-CCD used in simulations. P1 and P2 form one pixel. IG and OG are the input and output gates, respectively. Figure (b) presents the mesh and the doping profile used for simulations. The positive dopant concentration corresponds to the n-type silicon (the 1µm n-buried channel) while the negative dopant concentration represents the p-type silicon (EPI layer).

the doping profiles (see Figure 7.3(b)) are selected to achieve the same electrostatic conditions as they are in the real CCD device.

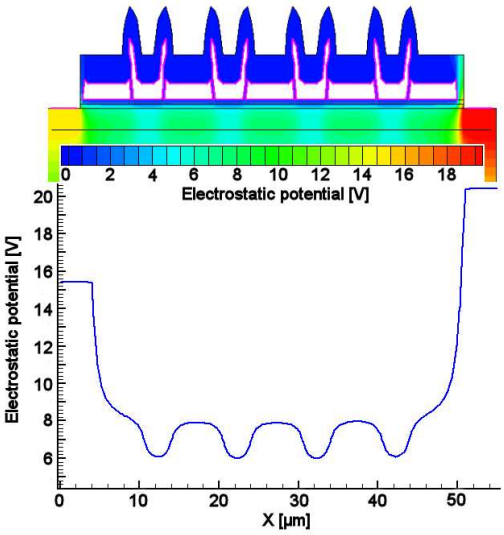
Figure 7.4(a) shows the electrostatic potential distribution in the simulated 2D model of the CCD and Figure 7.4(b) depicts the electrostatic potential along the channel at the depth of 0.35 µm. The potential barrier between p+ implants and n-type-buried channel amounted to ∼1.9V. The signal charge is transferred through the channel at 0.35 µm below Si-SiO_2 interface, where the electrostatic potential has its maximum, as shown in Figure 7.4(c). The signal electron packets are stored under the gates between the p-type-silicon implants, as depicted in Figure 7.4(d).

An impinging particle is introduced in the simulated the 2D CCD sensor with a dedicated TCAD command[2], which gives possibility to control the number of injected e-h pairs. In reality, the impinging particle generates in silicon approximately 80 e-h pairs along 1 µm track. In the 20 µm thick active volume of the modeled CCD sensor, the number of generated electrons amounts to around 1600 e^-. The real pixel of the investigated CPC-1 has dimensions of 20×16 μm^2. The mentioned 16 µm corresponds to the pixel width in the third, not simulated dimension. The 2D model used in this work assumes that the size of the third dimension is equal to 1 µm. Assuming a uniform distribution of the signal charge inside the pixel active volume, the signal of 1600 e^- is scaled by the factor of 16. The latter represents the difference in the third dimension between the 2D and the 3D model. As a consequence, the charge of 100 e^- is introduced to the 1 µm-thick simulated slice of the CCD. This number of electrons is used for

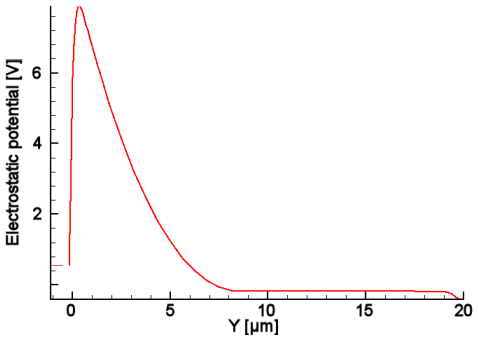
[2] "HeavyIon" command.



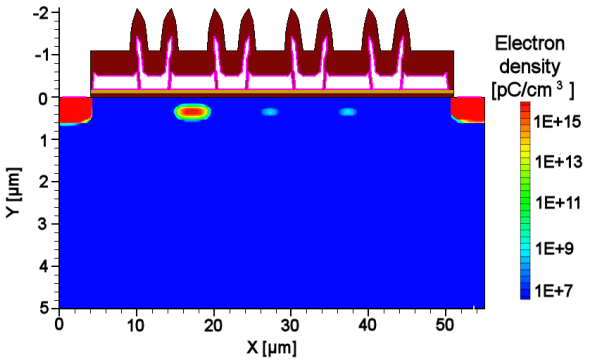
(a) Electrostatic potential.



(b) Electrostatic potential in the 2–phase CP-CCD along the channel at 0.35 µm below the Si-SiO_2 interface.



(c) Electrostatic potential under the gate as a function of the depth.



(d) Charge packets are stored in the device under the gates where the potential has a local maxima.

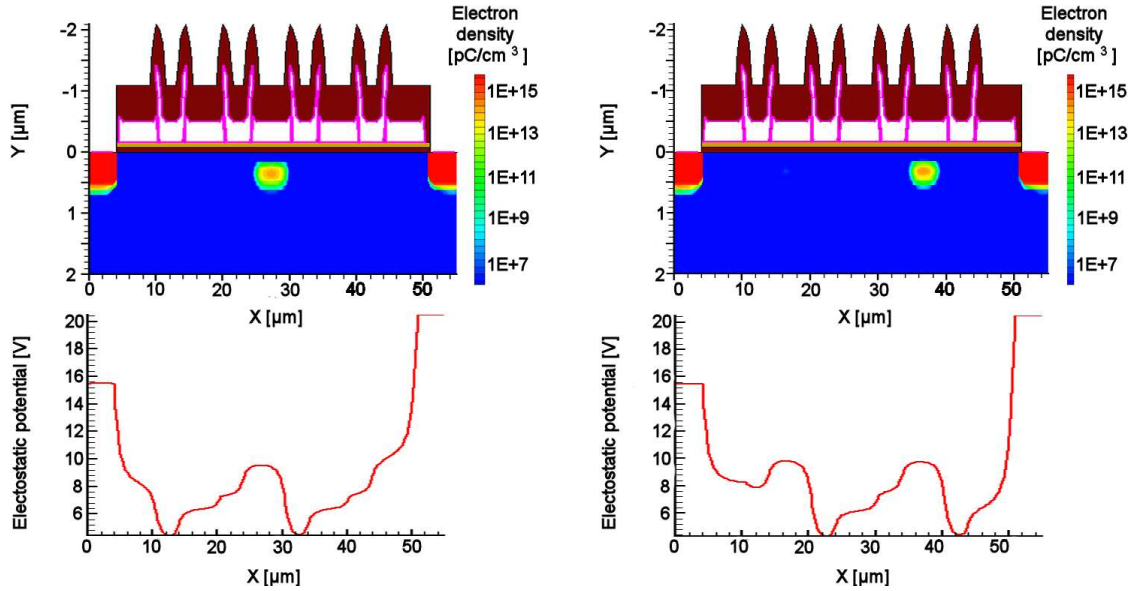
Figure 7.4: Main properties of the simplified 2D simulation model of the CCD pixel.

simulations and is injected under the IGB gate (see Figure 7.3(a)). Subsequently, a sinusoidal clock voltage is applied to the gates and the charge is transferred from left to right towards the output gate (OG). This situation is shown in Figure 7.5(a) and Figure 7.5(b).

7.3.2 CTI and its extraction from ISE-TCAD simulation

The definition of the CTI used during TCAD simulations is given by the following equation:

$$CTI = \frac{e_T - e_B}{e_S} \tag{7.4}$$



(a) Situation at the time t_0, when P1 and P2 clock amplitudes reach their maximum (P1) and minimum (P2) values.

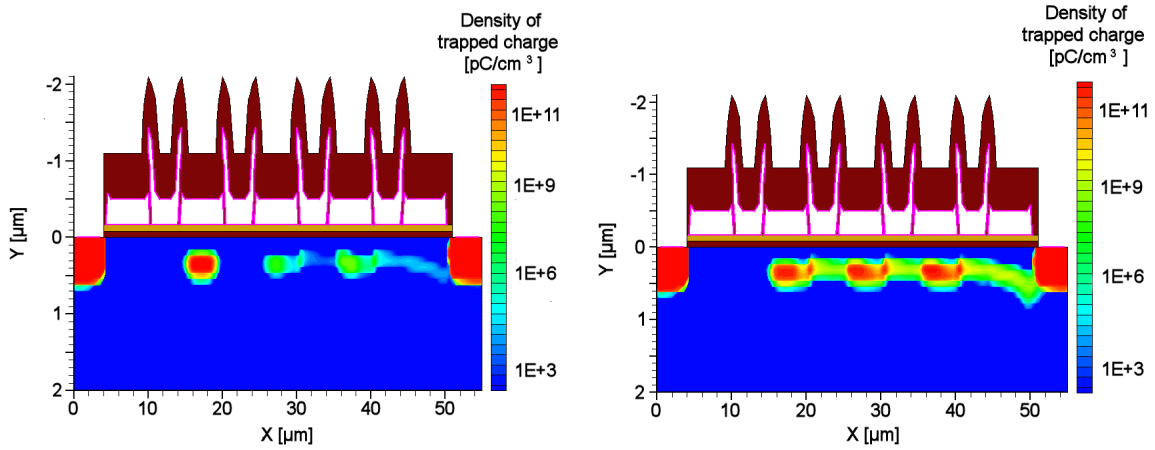
(b) Situation at the time, when pulses P1 and P2 are in opposite phases with respect to the phases they had at the time t_0.

Figure 7.5: Simulation of the charge transfer along the CCD channel. Electron density (top). Potential along the channel (bottom). The charge is transferred from the left to the right side of the simulated device.

where: e_S is the electron signal packet density before transfer (amount of signal electrons), e_B stands for the density of the trapped electron charge prior to signal packet transfer (number of trapped electrons in the previous transfer), and e_T corresponds to the density of trapped electrons just after the transfer of the charge packet (amount of electrons trapped during the current transfer).

Some comments are necessary for better understanding the importance of the background charge density (e_B in the Equation 7.4). One may consider two consecutive charge transfers through the investigated pixel. During such transfers, some amount of electrons from the charge packet will be trapped by silicon defects. The trapped electrons may or may not be released by traps before the next signal packet arrives. These traps which contain electrons from the previous transfer cannot trap more carriers. As the e_T stands for total density of the trapped charge and the e_B gives the density of trapped carriers before the charge transfer, the difference between e_T and e_B provides the density of trapped carriers during the current transfer. The latter compared to the density of the charge arriving to the investigated pixels defines the CTI for this pixel.

Figure 7.6(a) presents the trapped-charge density just before the transfer of the charge packet through the investigated pixel. The same density just after the transfer is shown in Figure 7.6(b). The simulations were carried out for 10 MHz clock frequency, temperature of 150 K and for the



(a) Charge trapped under the investigated pixel before the charge transfer.

(b) Charge trapped under the investigated pixel after the charge transfer.

Figure 7.6: Simulation of the charge transfer through an irradiated 2-phase CCD. Simulation for 0.17eV traps.

defects with energy level of 0.17 eV below the bottom of the conduction band (see the next section for more details).

7.3.3 Estimation of the trap density in the CCD channel

Previous studies covering the radiation effects in the CCD sensors produced by E2V Technologies were described in [170, 167]. These studies indicated that in the low-oxygen-content silicon, as the one used for n-buried CCD channel, the major contribution to the CTI originated from the A-center, and the E-center. These defects are located at the energies of 0.17 eV (A-center) and 0.44 eV (E-center) below the bottom of the conduction band and they are both considered within the scope of this document. They will be referred simply as the 0.17 eV and 0.44 eV traps.

In order to determine the trap densities to be used for simulations, the particle fluxes expected for the three inner detector concepts for the ILC experiment were used, as shown in Table 7.1. The main expected background arises from e^+e^- pairs with an average energy of 10 MeV and from neutrons (knocked out of nuclei by synchrotron radiation).

Table 7.1: Simulated background results for three different detector concepts. The values are hits per square centimeter per e^+e^- bunch crossing. SiD is the Silicon Detector Concept, LDC is the Large Detector Concept and GLD is the Global Linear collider Detector.

Simulator	SiD	LDC	GLD
CAIN/Jupiter	2.9	3.5	0.5
GuineaPig	2.3	3.0	2.0

Table 7.2: Trap concentrations C and electron capture cross-sections σ used in the TCAD simulations.

Defect energy level $E_t - E_c$ (eV)	Defect type	Trap concentration C (/cm^3)	cross section σ (/cm^2) [167]
0.17	Acceptor	$1{\cdot}10^{11}$	$1{\cdot}10^{-14}$
0.44	Acceptor	$1{\cdot}10^{11}$	$4{\cdot}10^{-15}$

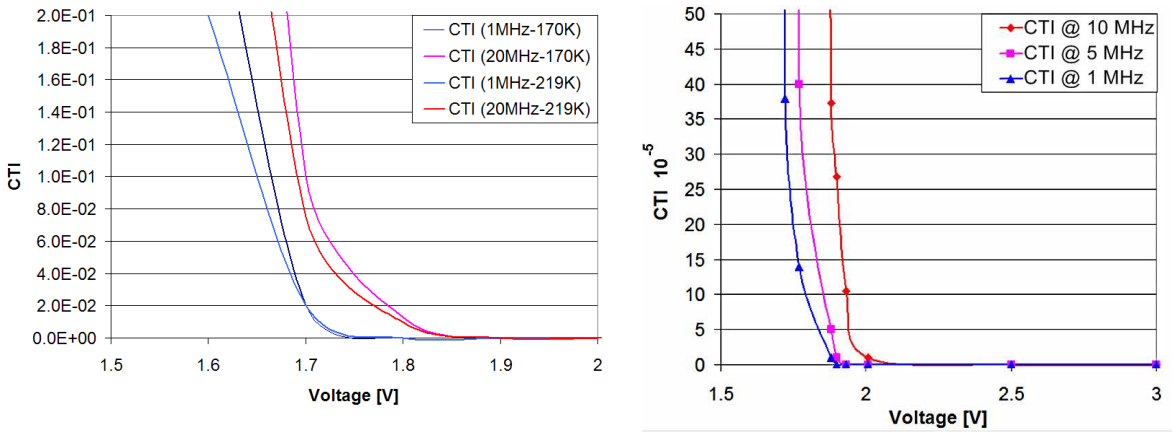
Using the Large Detector Concept (LDC), where the innermost layer of the vertex detector is located at 15 mm from the interaction point, one can estimate an e^+e^- flux to be approximately 3.5 hits/cm^2/bunch crossing. This translates into the yearly fluence of $\sim 1.5{\cdot}10^{12}$ e/cm^2 or, according to the NIEL scaling, to $1{\cdot}10^{11}$ $\mathrm{n_{eq}/cm^2}$. The two independent studies estimated the expected neutron fluence at the innermost layer of the LDC to be 10^{10} n/cm^2/year [171] and $1.6{\cdot}10^{10}$ n_{eq}/cm^2/year [172]. No safety factors were applied to the expected fluences.

The knowledge of the expected particle fluences at the innermost vertex detector layer opens an opportunity for calculations of the introduced trap densities for both A and E centers. These calculations were carried out based on the so called defect introduction rate. The latter is a coefficient which multiplied by the particle fluence provides the density of traps required for TCAD simulations. The defect introduction rate depends on a particle type and a sensor material. Some values of introduction rates for n-type silicon exposed to 1 MeV neutrons and 10 MeV electron fluence can be found in the literature [173, 174, 175, 176, 177, 178, 179, 180, 170]. Considering the expected fluence of $1{\cdot}10^{11}$ $\mathrm{n_{eq}/cm^2}$ at the innermost layer of the ILC vertex detector, the trap densities were estimated to be in the range of 10^{11}–10^{12}/cm^2. Since the precise number could not be found, it was decided to use the trap concentration of 10^{11}/cm^2 for both investigated defects. Additional simulations related to the influence of the trap concentration on the CTI were performed. They are discussed in Section 7.5.2.

7.4 Influence of the clock amplitude and frequency on the charge transfer

The CTI can be created not only by signal trapped by radiation-induced effects in the CCD channel but also by applying an insufficient clock voltage to the CCD gates. This section will present the TCAD simulations of the voltage-induced CTI. To distinguish between the effects caused by radiation and those induced by the insufficient gate voltage, the trapping was disabled during these simulations.

The 2D CPC-1 sensor model described previously in this chapter, was used for simulations of this phenomenon. The charge equivalent to 100 e^- was injected under the input gate (IG) (see Figure 7.3(a)). Next, the sinusoidal signals with different amplitudes were applied to transfer the charge packet from the IG gate to the P1 gate. The number of not transferred signal electrons was extracted. This procedure was then repeated for different clock frequencies (1MHz and



(a) TCAD simulation

(b) Measured at RAL with the CPC1

Figure 7.7: CTI as a function of clock amplitude.

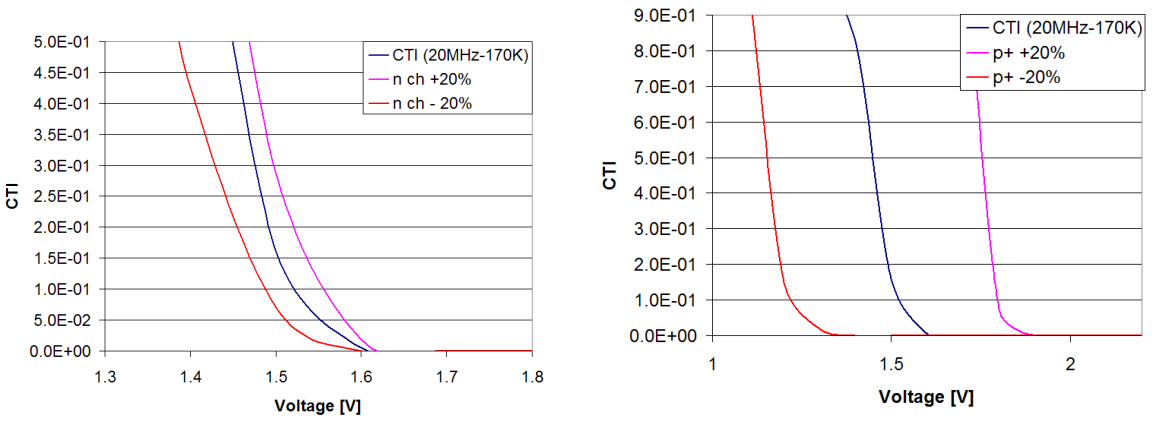
20MHz) and voltages (from 1.4 V to 2.3 V, with a step of 0.1 V). Results of the simulations are shown in Figure 7.7(a).

The simulations identified the threshold voltage (V_{CTI}) below which the CTI was observed to rise. Observations at 20 MHz clock frequency indicated the CTI increase for the clock amplitudes below 1.8 V. For the lower clock frequency, 1 MHz, the rise in the CTI was observed for voltages below 1.7 V.

In order to compare simulation results with data originating from real CPC-1 sensor, stand-alone tests at Rutherford Appleton Laboratory (RAL) were performed. Figure 7.7(b) presents experimental results obtained with the CPC-1 sensor. Similar results were already presented in [181].

The measured and the simulated CTI were observed to rise for the clock voltage amplitude below 1.9 V. The changes of V_{CTI} with the clock frequency were visible for both the simulated model and the real device. In the case of RAL measurements, the V_{CTI} was decreasing for larger clock frequencies. For example, in the case of 10 MHz clock frequency, the V_{CTI} threshold was $\sim$1.9 V, while V_{CTI}=1.7 V was observed at 1 MHz.

To verify the possibility of adjusting the simulated sensor behavior to the real one, the response of the CPC-1 sensor model to changes in doping concentration for p+ inter-gate implant and the n-buried channel was studied in a dedicated set of simulations. The variations of dopant concentration for both mentioned regions amounted to about $\pm 20\%$. As the voltage needed for charge transfer has to be larger than the potential barrier between p+ implants and n-channel, a significant influence of their doping concentration on the V_{CTI} was expected. Figures 7.8(a) and 7.8(b) show that changes in the doping levels had a noticeable influence on the clock voltage value where CTI starts to increase. Values of V_{CTI} agree with these observed at RAL for the real CPC-1.



(a) (b)

Figure 7.8: CTI as a function of clock amplitude: (a) For different p+ implant doping concentrations; (b) For various n-channel doping concentrations. The blue curves in both figures correspond to the nominal doping profiles.

The simulations presented above prove that the 2D TCAD model reflects to some extent the behavior of the real sensor. The model response to variations in amplitude and frequency of steering signal as well as to the changes in doping profiles was correct.

7.5 Dependence of the CTI on the temperature and readout-clock frequency – TCAD simulations

7.5.1 Model parameters

This section will present the TCAD simulations of the radiation-induced CTI. To distinguish between the effects caused by radiation and those induced by the insufficient gate voltage, the voltage for searing clock signals was set significantly above the critical limit and the trapping was enabled during simulations. Simulations of the CTI dependence on temperature and clock frequency were carried out for traps with energy levels at 0.17 eV and 0.44 eV below the bottom of the conduction band.

For further understanding, one should recall the process of the signal charge transfer through a randomly chosen pixel in the CCD device. At a time t_n, a charge packet (n) is transferred through that pixel and remains stored under the pixel for approximately one clock period. The charge transfer occurs in the temperature range where traps are active. The number of trapped electrons depends on the charge packet transfer velocity and capture time constant τ_e. Such trapped electrons stay captured for a time which depends on the emission time constant τ_c. At the time t_{n+1} the next charge packet (n+1) is transferred and again some electrons are trapped. The number of trapped electrons depends on the number of all traps and traps already filled

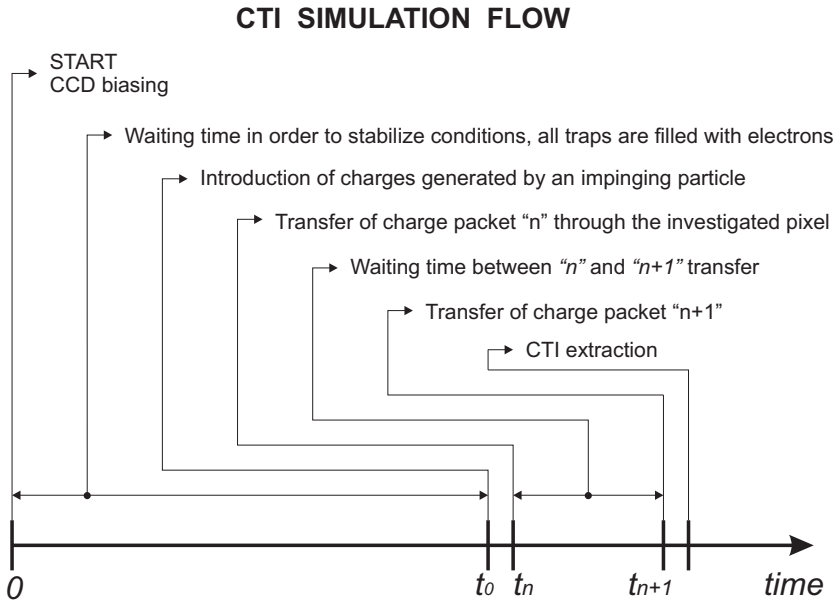


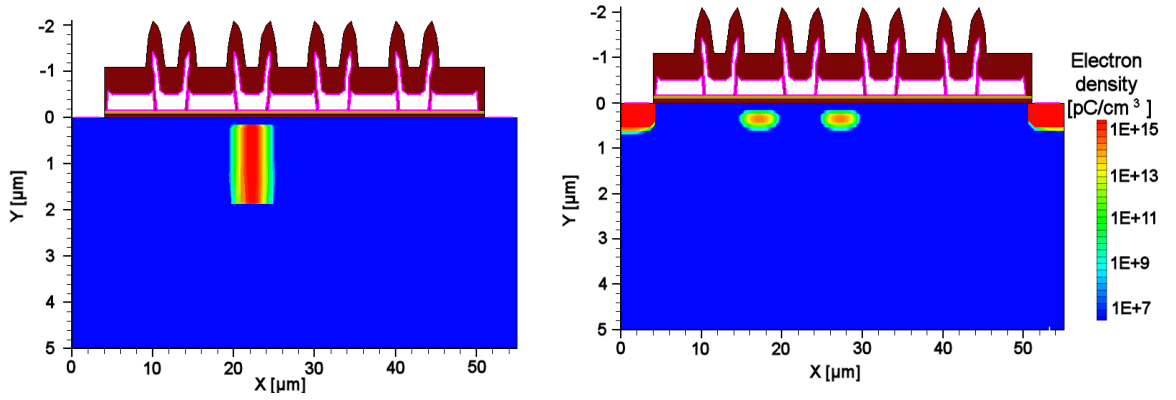
Figure 7.9: The CTI simulation flow in TCAD.

with electrons from the previous charge packet. The CTI is determined for the (*n+1*) packet as the ratio of charge trapped during the (*n+1*) transfer to the total amount of charge arriving to the pixel. For example, during the transfer of the packet *n* through the investigated pixel, 3 electrons were trapped. There was a charge Q_{n+1} of 100 electrons in the packet *n+1* arriving to the investigated pixel. During the transfer of the packet *n+1*, 4 electrons were trapped but in the same time, 2 of the previously trapped electrons (from packet *n*) were released and joined the packet *n+1*. Therefore, the number of electrons in the packet *n+1* decreased after the transfer through the pixel to $Q'_{n+1}e^- = Q_{n+1} - 4e^- + 2e^-$.

To reproduce correctly the charge transfer process ongoing in the real device, several charge packets should be implemented in the simulations. However, the TCAD simulations have their limitations and for example, one cannot introduce several charge packets originating from several particles impinging the detector. The command responsible for e-h pair generation can be used in TCAD only once per simulation run[3].

In order to overcome these complications, the CTI simulations in TCAD were carried out according to the scheme presented in Figure 7.9. At the beginning, the device was powered and the traps were filled with electrons by the dedicated command available in the simulator. This operation implements approximately the conditions existing in the device after several charge transfers. The traps remained filled till the moment t_0, when the charge packet was introduced into the device. From this moment traps were allowed to interact in the way described by physics laws with the signal electrons. Thus, they could emit an electron or capture it from the charge packet.

[3]The recent versions of TCAD package allows for multiple use of "HeavyIon" command.



(a) Introduction of charges by the means of "HeavyIon" TCAD command. Charge is introduced exactly under the left p+ implant of gate P1.

(b) By the mean of p+ implant, the introduced charge is split into two equal pieces and stored under gates in IG and P1.

Figure 7.10: Simulation of an influence of previous charge transfer on the CTI.

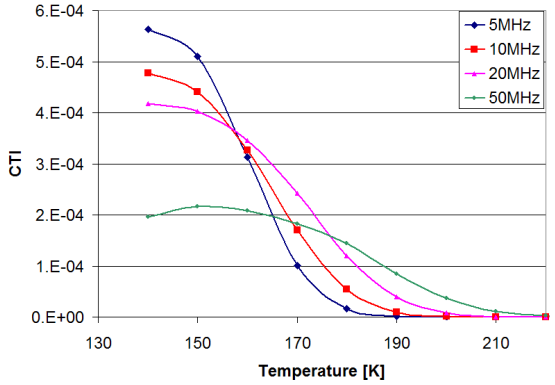
Next, the e-h charge was generated exactly under the the p+ -implant center of the gate P1, see Figure 7.10(a). Due to the symmetry of the 2D model used for simulations, the e-h pairs were split by an electric field and stored with equal amount under the IG and the P1 gates (see Figure 7.3(a) and Figure 7.10(b)). The electron packet localized on the right hand side was used to simulate signal approaching the investigated pixel in time t_n. The electron packet from the left was transferred next and was used to simulate the electrons reaching the pixel in time t_{n+1}.

7.5.2 Simulation results

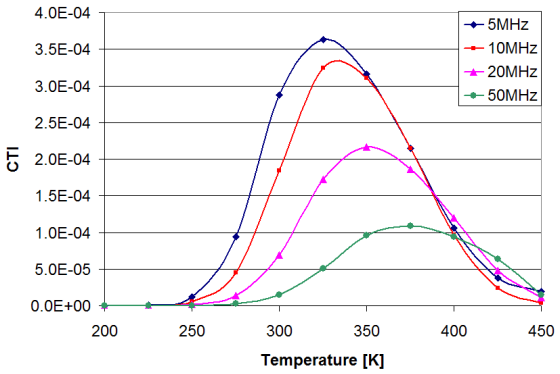
Using the method described above, the CTI dependence on temperature was simulated for the 0.17 eV and 0.44 eV traps. The simulations were carried out for a wide temperature range from 140 K up to 440 K. Different clock frequencies from 5 MHz to 50 MHz were also taken into account.

Obtained results for 0.17 eV traps and different frequencies are shown in Figure 7.11(a) while for 0.44 eV traps they are displayed in Figure 7.11(b). The combined effect is illustrated at the bottom of the same figure.

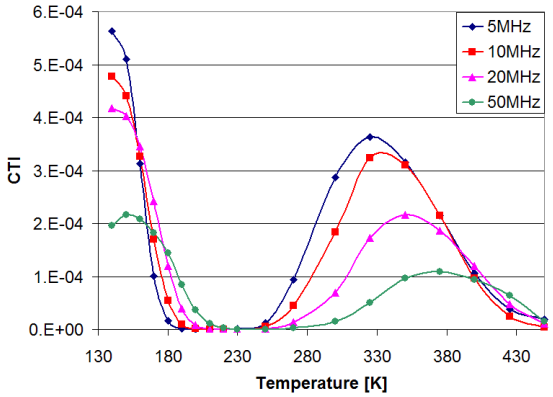
The CTI behavior for both investigated traps agreed with the expectations. The CTI values obtained in the case of the transfer with a lower readout frequency were higher as expected. This reflected the fact that in this case the electron packet stays longer under the investigated pixel and therefore the probability of capturing an electron increases. The temperature range where the CTI peaks are visible is strongly dependent on the readout frequency and it moves towards higher temperatures for a faster readout frequency. The shift of the peak position was related to the charge transfer velocity, as expected.



(a) Et= 0.17 eV



(b) Et= 0.44 eV



(c) Combined results of 0.17 eV and 0.44 eV traps

Figure 7.11: The simulated CTI as a function of temperature for four different clock frequencies: (a) for 0.17 eV traps, (b) for 0.44 eV traps, (c) combined effects originating from both investigated trap energy levels.

To address difficulties with assessing the correct trap densities introduced by particle fluences expected at the ILC, additional simulations were carried out. In these simulations, the CTI was studied as a function of different trap densities. The latter was varied from $10^{10}/cm^2$ to $10^{12}/cm^2$. The temperature and the clock frequency were kept constant. Results are shown in Figure 7.12. The CTI was observed to be a linear function of the trap concentration for the range studied here. This feature will simplify the final tuning of the simulation model according to future CTI measurements with irradiated CPC-1 sensors.

The simulations results can be used to estimate the performance of CCDs in various conditions regarding radiation level, readout speed and temperature. To present how the outcome of the TCAD simulation of the CPC-1 model can be used, the following example is discussed:

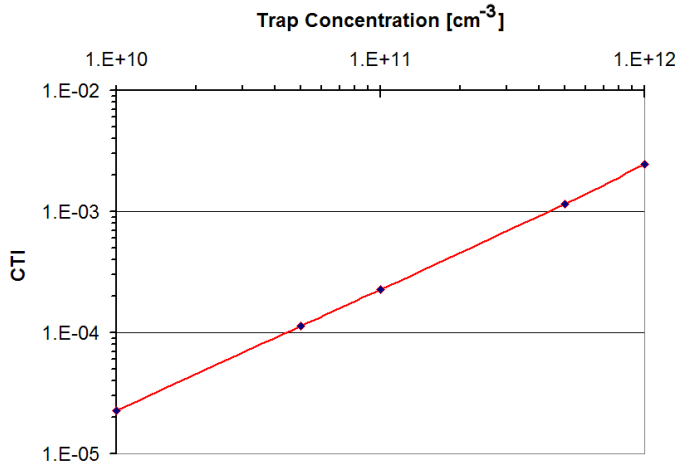


Figure 7.12: Simulated CTI as a function of trap concentration. Simulations for 20 MHz, 0.17 eV traps and at 160 K.

- Realistic CCD dimensions: 2×2 cm^2. Consequently the CCD array is composed of 1 million of pixels (1000×1000). Pixel pitch of 20 μm. EPI layer thickness of 20 μm.
- Generated charge: 1600 e-h pairs generated in 20 μm thick EPI layer of CCD. Due to charge sharing about 50% of the initial charge is collected by a single pixel.
- In the case of serial readout, the charge will travel over 1000 (vertical register) + 1000 (horizontal register) pixels (the worst case) before arriving to the output node.
- In the case of column-parallel readout, the charge will travel over 1000 (vertical register) pixels (the worst case) before arriving to the output node.
- CTI of 10^{-4} simulated at room temperature, for clock frequency of 50 MHz and for a device exposed to $10^{11} n_{eq}/cm^2$
- Realistic noise of around 6 electrons before sensor irradiation [182] (CCD for SNAP Satellite), but for the column-parallel CCD produced for the LCFI collaboration the noise before irradiation was in the range of 15-60 electrons [167, 181]. Noise of 15 electrons is assumed for calculations.
- Required SNR $>$ 15. SNR of 15 is the critical value for CMOS pixel sensors. Below this SNR value, these sensors start to lose their performance. To compare CMOS sensors and CCD sensors, both based on sensitive volumes with similar thicknesses, value of SNR=15 is considered as mandatory for efficient particle detection.

Using Equation 7.1, one can calculate the charge than can be accessed at the output gate for both investigated CCD architectures: with a serial and with a column-parallel readout.

In the case of serial readout, where charge has to travel 2000 pixels, Equation 7.1 (where Q_0 is 800 electrons) can be written as following:

$$Q_{2000} = Q_0(1 - 10^{-4})^{2000} \approx 100e^- \longrightarrow SNR = 6.7 \tag{7.5}$$

In the case of column-parallel readout, where charge has to travel 1000 pixels, Equation 7.1 (where Q_0 is 800 electrons) can be written as following:

$$Q_{1000} = Q_0(1 - 10^{-4})^{1000} \approx 300e^- \longrightarrow SNR = 20.0 \tag{7.6}$$

Knowing the number of charges arriving to the output gate and assuming that one could build the CCD featuring the noise of 15 e^- after irradiation, it could be concluded that only the device with column-parallel architecture will meet the afore mentioned requirements. Currently, the knowledge about the CCD for ILC is insufficient to predict whether the particular CCD will meet certain requirements or not. Simulations presented here should be accompanied with the extensive studies of the data taken with real CCDs. Such studies would allow creating a data base related to sensor behavior (CTI generated, noise, detection efficiency) in different conditions regarding clock frequency, temperature and radiation level. Those results should be next confronted with the simulated CTI values in order to tune the TCAD model.

First steps towards such studies were undertaken within the framework of this thesis. The stand-alone test setup was prepared at Liverpool University. Detailed description of the setup and information about preliminary data taken with 2-phase CCD can be found in [183]. However, the studies with irradiated sensors could not be continued because the project was stopped due to insufficient funding.

7.6 Summary and conclusions

Simulations of the CTI using a 2D model of the 2-phase CCD were performed during this PhD thesis work. The CTI was studied as a function of the clock voltage and the trap density.

Regarding the minimum voltage necessary for efficient charge transfers, the results obtained with simulations were coherent to those measured with a real device.

The simulation results of CTI induced by radiation effects agreed with the expectations. The CTI variations with clock frequency and temperature were consistent with the assumed charge-transfer mechanism, and similar to those presented in literature. The absolute CTI values obtained with the TCAD simulation model may however differ from these which could have been observed in the real device. There are several reasons for this. For example, the trap concentration used for simulation purposes could have been under or over estimated. Also, in the real device, the sinusoidal signals applied to the CCD gates to control the charge transfer will not be sinusoidal. This is the consequence of parasitic capacitances of the signal distribution lines. Moreover, tests at low temperatures are very demanding. In fact, the

components such as amplifiers, used to build the co-operating PCBs are not the ones dedicated to work in extremely low temperatures. Finally, one may expect also traps with energies not considered in this work.

The simulations shown in this chapter may become a useful tool for assessing the tolerance of the CCDs to radiation. However, the presented results need to be confronted with the CTI values obtained with real CCDs exposed to different non-ionizing radiation fluences. The simulation model presented in this work needs to be tuned to the results obtained with real sensors.

Summary

Achievements of this PhD thesis

The work underlying this thesis on the radiation tolerance of CMOS Monolithic Active Pixel Sensors addresses an aspect of increasing importance as the range of sensor applications expands. The CMOS sensors have been proposed as the sensor technology for the vertex detector of the Compressed Baryonic Matter experiment. In this vertex detector, the sensors will be exposed to radiation of a few $10^{13}\ \mathrm{n_{eq}/cm^2}$ and several Mrad. Moreover, in order to keep the occupancy of the sensors composing the vertex detector reasonably low, a sensor readout time on the order of tens of microseconds is mandatory.

To achieve the required readout time, the sensor pixel array was organized in parallel columns, at the same time providing data filtering and restricting the readout to pixels which had collected the signal charge. For this purpose, the in-pixel architecture was complemented with amplification and correlated-double-sampling circuitry. Consequently, these pixels became more complex and therefore potentially more sensitive to ionizing radiation than the simple architectures of earlier sensors. The development of these fast column-parallel CMOS pixel sensors in a 0.35-μm CMOS process also imposes a minimal pixel pitch of 16-18 μm. This allows the in-pixel-signal-processing electronics to be fitted and provides the required spatial resolution.

On the other hand, studies carried out in the past with CMOS pixel sensors based on undepleted sensitive volume showed that the non-ionizing radiation tolerance can be enhanced up to a few $10^{13}\ \mathrm{n_{eq}/cm^2}$ by reducing the pixel pitch to 10 μm. Though the pixel pitch may be reduced by implementing the column-parallel sensors in processes with a smaller feature size, other limitations occur: the growth in the number of pixels per column increases the readout time, and the growth in the number of columns increases the power consumption.

Therefore, the study of column-parallel CMOS pixel sensors tolerance to ionizing radiation ought to be pursued while simultaneously improving their non-ionizing radiation tolerance without squeezing the pixel pitch. These aspects became the main focus of the research and development presented in this document.

This thesis work studied for the first time the radiation tolerance of column-parallel CMOS pixel sensors. The work aimed at identifying which in-pixel architectures are the most robust to ionizing radiation. The studies also addressed the question of whether the performance of irradiated column-parallel sensors can be improved by optimizing the design or by cooling the

devices down.

Among all the implemented in-pixel architectures, the one featuring a feedback loop exhibited the lowest pixel to pixel output signal dispersions, which remained unchanged after exposure to ionizing radiation. Since the column-parallel sensors utilize a single comparator for a whole column of pixels, such low dispersion between them is mandatory to ensure the proper comparison of signals with a reference value. The architecture equipped with a feedback loop is therefore particularly promising for further CMOS-sensor implementations.

As expected, the sensors with advanced in-pixel signal processing were more sensitive to ionizing radiation than the sensors based on simple 3T or SB architectures. The performance of sensors exposed to ionizing radiation was observed to start significantly degrading after 300 krad, a dose for which the detection efficiency and fake hit rate were difficult to maintain above 99% and below 10^{-4}, respectively. The performance degradation at this modest ionizing dose was attributed to the rise in the temporal noise, which was beyond the level observed for sensors featuring simple in-pixel architectures.

To determine which factors would reduce the sensor sensitivity to ionizing radiation, studies investigating the impact of different in-pixel elements on the temporal noise after irradiation were performed. The studies showed that the performance of the column-parallel sensors can be improved by implementing an enclosed-layout transistor in the feedback loop and a cascode amplifier that features a higher gain than the common source configuration used previously. Nevertheless, the performance improvement was modest: the noise excess observed after irradiation up to 300 krad was still nearly as high as before. The outcome of these studies is that the temporal noise increase following ionizing radiation cannot be controlled either by standard radiation protection techniques with the 0.35-μm fabrication process used or by the optimization of individual in-pixel elements.

The studies carried out with various in-pixel architectures exposed to different ionizing radiation doses also showed that the temporal noise cannot be reduced efficiently by cooling. The temporal noise observed at 0 °C was only slightly lower than the one measured at room temperature, reaching a plateau at ∼0 °C where further cooling was no longer effective. This shows that this excessive temporal noise does not originate from a diode leakage current, but rather from more complex in-pixel electronics.

Currently, the column-parallel CMOS pixel sensors fabricated in the 0.35-μm AMS process feature a radiation tolerance of ∼300 krad at room temperature. More robust sensors could be most likely achieved by replacing all the standard transistors with their enclosed-layout versions and surrounding them with guard rings. However, to provide such protection and simultaneously accommodate all in-pixel microcircuitry in small pixels which provide the required spatial resolution and non-ionizing radiation tolerance requires the use of processes with a smaller feature size than 0.35 μm. Such processes are also intrinsically more tolerant to ionizing radiation because of reduced gate-oxide thickness.

This PhD thesis addressed the investigation of different CMOS processes where charge collection in the sensitive volume proceeds (at least partially) through a built-in electric field. The latter can be achieved by sensor depletion or by implementing a graded doping profile in the EPI layer. Depleted sensitive volume already exists in the Hybrid Active Pixel Sensors or strip detectors, allowing the devices to tolerate non-ionizing radiation at a level well beyond the one required for the CBM experiment. This approach has been so far hampered by the EPI layers of standard CMOS processes which feature high and uniform doping. However, this obstacle has vanished recently since new CMOS processes with an epitaxial layer featuring graded doping or high resistivity have now become available.

The potential of CMOS processes based on a gradually doped EPI layer was studied with a 0.25-μm BiCMOS technology. This process was found to be intolerant to ionizing radiation. Therefore, the characterization of this technology was not performed systematically up to the end, and consequently, the influence of the graded EPI layer on the sensor tolerance to non-ionizing radiation was not evaluated.

The breakthrough in the development of radiation-tolerant CMOS pixel sensors was achieved with sensors based on a high-resistivity (1 kΩ·cm) EPI layer implemented in the 0.6-μm XFAB process. Sensors based on this type of EPI layer were observed to feature a signal on the seed pixel at least twice as large as the signal from sensors based on an undepleted epitaxial layer. This substantial signal enhancement translated into a high signal-over-noise ratio and allowed a satisfactory detection efficiency of $\sim$100% at room temperature to be achieved even for sensors featuring a pixel pitch of 20 μm and irradiated with $3{\cdot}10^{13}$ $\mathrm{n_{eq}/cm^2}$. The tolerance to non-ionizing particles of sensors based on a high-resistivity EPI layer was thus observed to be at least one order of magnitude higher than of those featuring the same pixel pitch but based on a standard epitaxy. This achievement triggered a new generation of CMOS pixel sensors dedicated to particle tracking which rely on a high-resistivity EPI layer. It also shows that the development of CMOS pixel sensors is on track to meet the requirements of the CBM experiment.

These excellent results combined with the likelihood that this technology will soon be accessible with a feature size of 0.35 μm triggered studies of the standard-epitaxial-layer XFAB 0.35-μm process, which is similar to the AMS-OPTO process used previously. The tolerance of the XFAB 0.35-μm process to non-ionizing radiation was found to be similar to the one obtained with the AMS technology. However, observations indicate that the XFAB process tends to be more tolerant to ionizing radiation than the AMS process: the leakage current observed at room temperature for the XFAB pixels was a factor of two smaller than that for the radiation-tolerant AMS pixels.

In parallel to the studies related to CMOS pixel sensors, another study devoted to the radiation tolerance of CCDs was undertaken during this thesis work. CCD sensors also provide a high granularity and a low material budget, which make them attractive for particle tracking.

However, despite the depleted sensitive volume, CCD sensors suffer significantly from non-ionizing radiation effects. A TCAD-based simulation model capable of predicting the influence of radiation-induced effects on the charge transfer in column-parallel CCDs was established within the framework of this thesis. The charge transfer was studied for the specific case of a vertex detector of the International Linear Collider, where the radiation level is lower than in the case of the CBM experiment. The charge losses were modeled for various parameters like temperature, trap energy level and concentration as well as clock frequency. The results obtained from the model agree with the theoretical expectations. However, the model results could not be compared with experimental data because insufficient funding prematurely ended the project.

Ongoing studies related to the radiation tolerance of CMOS pixel sensors

After the end of this PhD thesis, the radiation tolerance studies were pursued with the AMS 0.35-µm process featuring a high-resistivity (∼400 Ω·cm) epitaxial layer, which became available in 2009/2010.

One of the sensors reproduced with the new process was MIMOSA-26, which features a column-parallel readout, a pixel pitch of 18.4 µm, and an integration time of 100 µs. This sensor was irradiated up to $3{\cdot}10^{13}$ $\mathrm{n_{eq}/cm^2}$ and exhibited satisfactory detection performance at 0 °C when exposed to a high-energy particle beam. Table 8.1 summarizes the achieved parameters.

Table 8.1: The performance achieved with the column-parallel CMOS sensor (MIMOSA-26) based on a high-resistivity EPI layer.

Number of pixels	∼ 660000
Readout time	⩽ 100 µs
Power consumption	∼300 mW/cm^2
Non-ionizing radiation tolerance	⩾$3{\cdot}10^{13}$ $\mathrm{n_{eq}/cm^2}$
Ionizing radiation tolerance	∼300 krad
Single point resolution	∼3 µm
Material budget per sensor	0.05%X_0

Another device reproduced with the new AMS process featuring the high-resistivity EPI layer is the analog-output sensor MIMOSA-18. Due to its pixel pitch of 10 µm, its original (standard EPI) version featured a radiation tolerance of at least 10^{13} $\mathrm{n_{eq}/cm^2}$ at -20 °C (cooling liquid temperature). The reproduced sensor, called MIMOSA-18 AHR, was irradiated with neutrons up to $3{\cdot}10^{14}$ $\mathrm{n_{eq}/cm^2}$ and characterized with $^{55}\mathrm{Fe}$ and $^{106}\mathrm{Ru}$ sources at IKF-Frankfurt, Germany. The first measurements performed at -34 °C (sensor temperature) indicated that the signal collected by the seed pixel is only mildly degraded (Figure 8.1). One may conclude that the radiation tolerance of MIMOSA-18 AHR is ⩾$3{\cdot}10^{14}$ $\mathrm{n_{eq}/cm^2}$ at sufficiently low temperature. This preliminary result needs to be confirmed during tests with a high-energy particle beam. This outstanding radiation tolerance obtained with a strongly cooled sensor is of particular

interest for the CBM experiment, where the sensors composing the MVD will be cooled down below -20 °C.

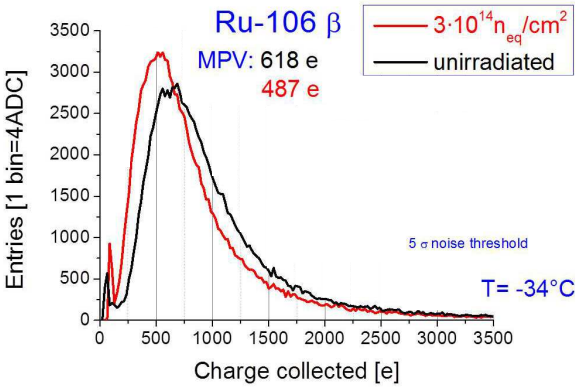


Figure 8.1:
Charge collected by the seed pixels measured for MIMOSA-18 AHR (fabricated with a high-resistivity EPI layer) before (black) and after (red) irradiation to a fluence of $3{\cdot}10^{14}$ $\mathrm{n_{eq}/cm^2}$ *[184].*

Future plans regarding CMOS pixel sensor development

In the coming years, the development of CMOS pixel sensors will be based on a new 0.18-µm CMOS process, which features an EPI layer with 1-5 kΩ·cm resistivity. Therefore, sensors fabricated in this process are expected to be more tolerant to non-ionizing radiation than the ones discussed in this thesis. The deep p-wells existing in the new process may be used to insulate the n-wells of PMOS transistors from the sensing diodes. Therefore, the new process will allow the use of PMOS transistors within the sensing area and, consequently, implement them inside in-pixel amplifiers to enhance their gain. The six metal layers in the 0.18-µm CMOS process will allow the interconnections between the sub-blocks composing the sensor to be optimized. Due to the gate oxide, which is thinner than that of 0.35-µm technologies, the new process is expected to be intrinsically more tolerant to ionizing radiation. It therefore cannot be excluded that one could avoid implementing enclosed-layout transistors inside more complex in-pixel architectures and still achieve the required tolerance.

The development of CMOS pixel sensors in the new process will be spread over several steps. In the first step, planned for the end of 2011, the process parameters will be examined with a prototype sensor featuring an analog output and simple in-pixel architectures. In this phase, the basic building blocks of the column-parallel sensors will be explored. In the next steps, the development will focus on implementing the column-parallel architectures. Here, optimization of the in-pixel signal processing (including 2-bit analog to digital conversion), data sparsification, and readout time may be addressed.

Within a few years, the radiation tolerance of the column-parallel CMOS pixel sensors implemented in the new process is expected to reach several Mrad and $\sim 10^{14}$ $\mathrm{n_{eq}/cm^2}$, and the readout speed will be improved to 20-40 µs. The spatial resolution of the new devices is expected to be at a level of 3-6 µm and their power consumption should not exceed 200-300 $\mathrm{mW/cm^2}$. All these parameters will meet the requirements of the CBM Micro Vertex

Detector.

A Appendices

A.1 Readout scheme of CMOS sensors with column-parallel architecture.

The typical readout scheme of CMOS sensors with serial readout (e.g., the 3T pixel) relays on periodical access to the pixels as discussed in Section 4.2.2.1. To perform the CDS operation (see Section 4.2.1), two consecutive samples of signal are used. The first sample is taken after a reset, the second one after a time during which the signal is integrated (integration time).

To speed up the readout, the simple in-pixel architecture was replaced by novel architecture named "clamping pixel" which allows for a massive parallel readout concept. This approach accelerates the readout time of the sensor by a factor equal to the number of (parallel processed) columns of the pixel array.

The functionality of the CDS procedure can be understood from the timing diagram shown in Figure A.1 and the pixel readout cycle presented in Figure A.2.

A simplified schematics of the clamping pixel of MIMOSA-22/22bis/26, which performs this analog data processing, is shown in Figure A.2. The central element of the pixel is a preamplifier, which amplifies the voltage applied to the parasitic capacitance of the sensing diode. The output of this preamplifier is AC-coupled to a clamping node. The potential of the latter is fixed prior to each readout cycle. Once the potential of the clamping node is set, the pixel integrates the signal charge, which modifies the potential of the node. The latter is sensed by means of a source follower (SF) and sent to the discrimination block aside the pixel matrix.

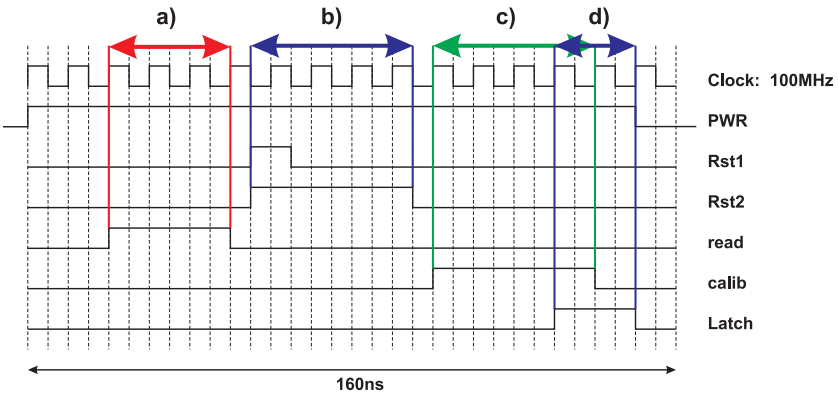


Figure A.1: Readout scheme of the column-parallel CMOS sensor: time diagram. The phases a), b), c) and d) are described in Figure A.2.

The four steps of the readout scheme are the following (see Figure A.1 for the time diagram):

- Figure A.2(a): the cycle starts with switching-on the power supply of the pixel: the signal

PWR state shown in Figure A.1 changes from logical 0 to 1. Next, the potential of the pixel after the integration time is read out. By closing the ”read” switch, this potential is passed into the storage capacitor Cs1 located at the end of the column;

- Figure A.2(b): the diode voltage and potential of the clamping node are reset by closing the switches Rst1 and Rst2;
- Figure A.2(c): the ”calib”-switch is closed in order to store the Vref2 potential as the reference voltage into the second capacitor Cs2;
- Figure A.2(d): the voltage stored in the ”calib”-capacitor Cs2 is subtracted from the one stored in the ”read”-capacitor. Provided the reset potential is arbitrary but well reproducible, the output of this procedure is a pedestal corrected CDS-signal, which is computed during the readout of the individual pixel. This signal is compared with the fixed (and common for all the pixels) threshold voltage Vrefc.

The integration time is the time between the two consecutive accesses to the same pixel, e.g., between the two rising edges of the ”read” signal as shown in Figure A.3.

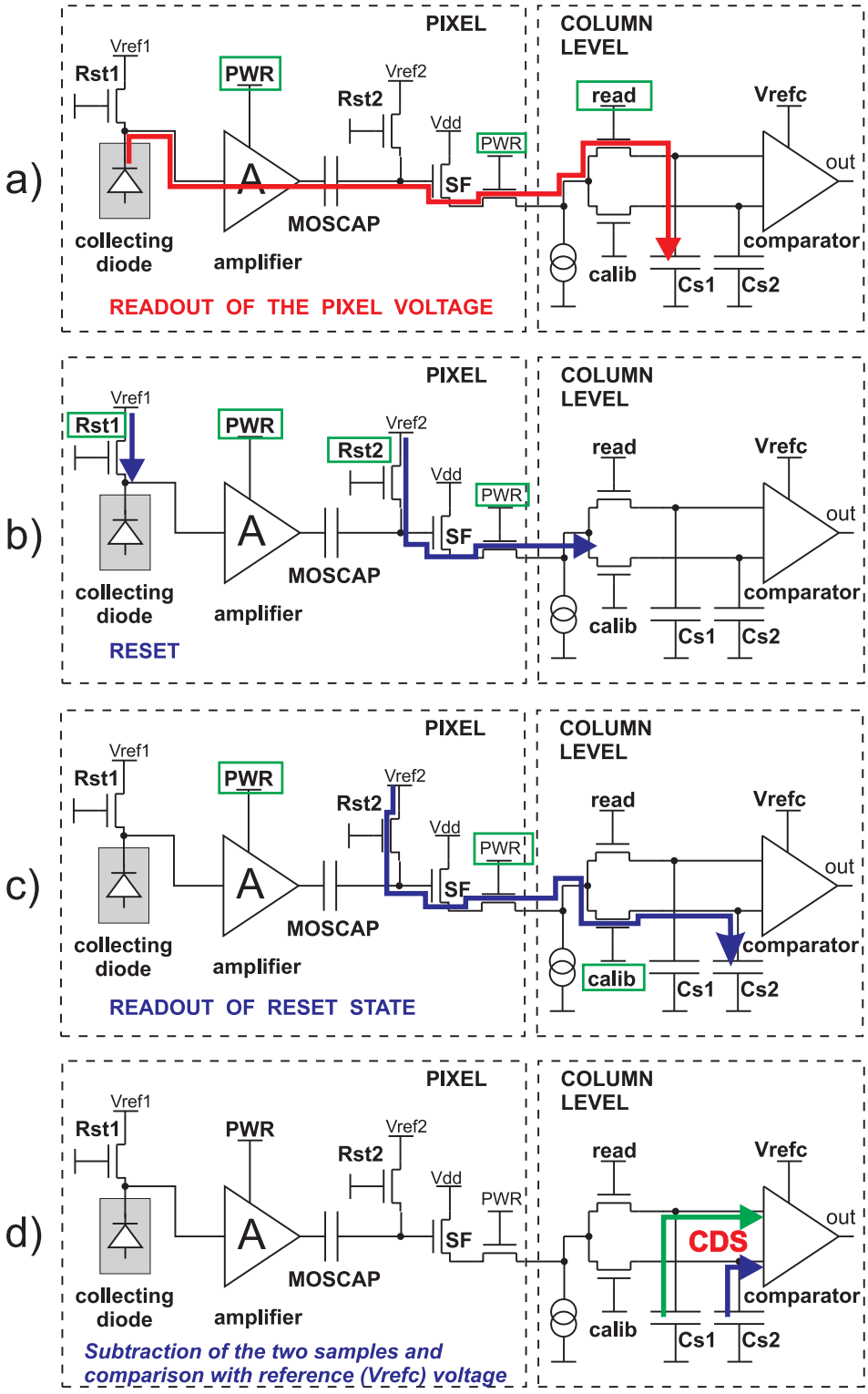


Figure A.2: Readout scheme of the column-parallel CMOS sensor: (a) "read" = 1: the signal integrated in the pixel is read out and memorized in the capacitor Cs1; (b) "Reset": Rst1 = 1 and Rst2 = 1: a fixed voltage is delivered to the sensing diode and source follower; (c) "calib" = 1: the reset voltage level is memorized in the capacitor Cs2; (d) "Latch" = 1: the signal samples memorized in the capacitors Cs1 and Cs2 are subtracted. The result of this subtraction is compared with the reference voltage Vrefc. A logical "1" or "0" is present at the comparator output depending on the result of the comparison.

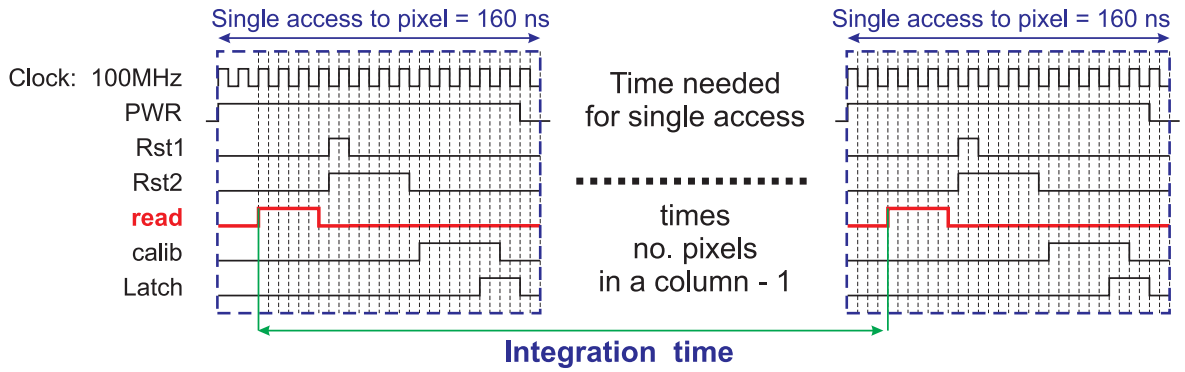


Figure A.3: Readout scheme of the column-parallel CMOS sensor: integration time.

A.2 Test matrices implemented in the MIMOSA-22ter prototype

Table A.1: MIMOSA-22ter test sub-matrices.

Name	Amplifier	Feedback trans.	FB diode [a]	Filter C	clamping C	comments
S1	cascode	standard	ELT	∼20 fF	∼40 fF	
S2	cascode	ELT	ELT	∼20 fF	∼40 fF	
S3	cascode	standard	ELT	∼7 fF	∼40 fF	
S4	cascode	ELT	ELT	∼7 fF	∼40 fF	tight p+ diode guardring [b]
S5	cascode	ELT	ELT	∼7 fF	∼40 fF	
S6	cascode	standard	p+ implant to n-well	∼7 fF	∼40 fF	
S7	cascode	standard	p+ implant to n-well	∼20 fF	∼40 fF	
S8	cascode	ELT	p+ implant to n-well	∼20 fF	∼40 fF	
S9	cascode	ELT	p+ implant to n-well	∼7 fF	∼40 fF	
S10	cascode	ELT	p+ implant to n-well	∼7 fF	∼40 fF	tight p+ diode guardring
S11	cascode	ELT	p+ implant to n-well	∼20 fF	∼60 fF	
S12	cascode	ELT	p+ implant to n-well	∼7 fF	∼60 fF	
S13	CS [c]	ELT	p+ implant to n-well	∼7 fF	∼87 fF	MIMOSA-22bis (S2) reference [d]
S14	CS	standard	p+ implant to n-well	∼7 fF	∼40 fF	
S15	CS	ELT	p+ implant to n-well	∼7 fF	∼40 fF	
S16	Cascode	ELT	ELT	∼7 fF	∼60 fF	
S17	CS	standard	ELT	∼7 fF	∼40 fF	
S18	CS	ELT	ELT	∼7 fF	∼40 fF	

[a] FB diode - Forwardly Biased diode.
[b] The p+ guard-ring to suppress the leakage current after irradiation.
[c] CS - Common Source amplifier.
[d] clamping capacitance - ∼87 fF.

A.3 MOS capacitor

Most of the VLSI circuits need to use passive elements such as capacitors or resistors. One of the commonly used techniques for implementation of capacitors inside a VLSI process is to use a MOS transistor. Such an example is shown in Figure A.4

The transistor source and drain are connected together forming one of the capacitor plates. The gate is used as the second capacitor plate. The capacitor is thus formed between the gate poly-silicon and bulk just underneath. The latter are separated by the gate oxide which is a dielectric.

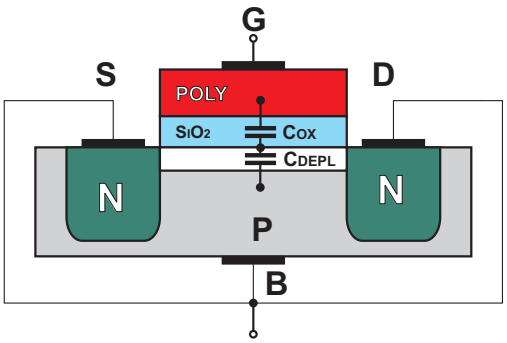


Figure A.4: MOS capacitor.

The capacitor formed in this way has a capacitance given by:

$$C = (\frac{1}{C_{ox}} + \frac{1}{C_{DEPL}})^{-1} \tag{A.1}$$

C_{ox} depends on the transistor gate size as it is presented below:

$$C_{ox} = \frac{\epsilon_0 \epsilon_{Si} W L}{t_{ox}} \tag{A.2}$$

where ϵ_0 it the dielectric constant of vacuum, ϵ_{Si} is the dielectric constant of silicon, W is the transistor channel width, L is the transistor channel length and t_{ox} is the thickness of the gate oxide.

The value of this capacitance per unit of area can be found in the technology specification data sheets.

The C_{DEPL} component is given by:

$$C_{DEPL} = \frac{\epsilon_0 \epsilon_{Si}}{C_{ox}} \sqrt{1 + \frac{2 \mid V_{GB} - V_{FB} \mid C_{ox}^2}{\epsilon_0 \epsilon_{Si} N_B}} - 1 \tag{A.3}$$

where N_B is the bulk doping concentration, V_{GB} is the voltage applied to the capacitor plates, V_{FB} is the flat band voltage.

The values of the capacitance, related to the clamping and feedback capacitors, presented in this section correspond to C_{ox}. They were calculated assuming a typical value of the

POLY1–DIFF capacitance of 4.54 fF/μm^2 taken from [187][1]. The capacitance component C_{DEPL} was not taken into account.

[1]The minimum value of the POLY1–DIFF capacitance given by the vendor is 4.26 fF/μm^2 and the maximum is 4.86 fF/μm^2.

A.4 MIMOSA-25 readout scheme

The readout scheme of MIMOSA-25 is organized in a not conventional way: one analogue output is used to read out 2 columns. The first readout cycle is followed by setting the internal counters to (0,0) position as shown in Figure A.5(right). Then, eight columns corresponding to one half of the chip are read out in parallel. The readout is continued for the second part of the device as shown by the arrows in the same sketch. In order to perform the correlated double sampling, each matrix is read out twice. The readout clock frequency for MIMOSA-25 is 2.5 MHz, which corresponded to the integration time of $\sim$77 μs.

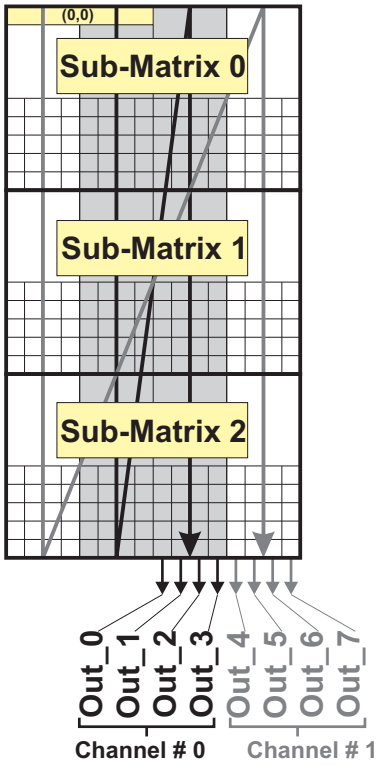


Figure A.5:
Readout scheme of the MIMOSA-25 sensor prototype: the point (0,0) indicates the location of the first pixels which is read out. The arrows provide the direction of the readout. The middle part of the matrix (gray) is connected to Channel 0 while the outer part (white) to Channel 1

Bibliography

[1] J. Adams et al. "Experimental and theoretical challenges in the search for the quark gluon plasma: The STAR collaboration's critical assessment of the evidence from RHIC collisions". *Nuclear Physics*, A757:102–183, 2005.

[2] CBM Collaboration. "Letter of Intent for the Compressed Baryonic Matter experiment", 02 2004. `https://www.gsi.de/documents/DOC-2004-Jan-116.html`.

[3] G. Aarons et al. "International Linear Collider Reference Design". *ILC-REPORT-2007-1, DESY-07-046*, 2007.

[4] M. Deveaux. *"Development of fast and radiation hard Monolithic Active Pixel Sensors (MAPS) optimized for open charm meson detection with the CBM - vertex detector"*. PhD thesis, University of Frankfurt/Main and of Strasbourg, 2008.

[5] C. Amsler et al. "Review of Particle Physics". *Physics Letters B*, 667:1–6, 2008.

[6] M. Deveaux. "A revision of the concept of the CBM-MVD". Presented at the CBM collaboration meeting, Goethe University Frankfurt/Main, Germany, 2008.

[7] M. Deveaux et al. "Design consideration for the Micro Vertex Detector of the Compressed Baryonic Matter experiment". PoS VERTEX2008:028,2008: arXiv:0906.1301v1.

[8] J.M. Heuser et al. "Requirements for the Silicon Tracking System of CBM at FAIR". *Nucl. Instr. & Meth. in Phys. Res. A*, 568:258–262, 2006.

[9] M. Szeleźniak. *"Development of pixel detectors with integrated microcircuits for the Vertex Detector in the STAR experiment at the RHIC collider"*. PhD thesis, University of Strasbourg, 2008.

[10] H.H. Wieman et al. "STAR PIXEL detector mechanical design". *Journal of Instrumentation*, 4:P05015, 2009.

[11] O.S. Bruning et al. *"LHC Design Report. Report No.: CERN-2004-003-V-1"*, volume 1. CERN, Geneva, 2004.

[12] J. Mnich. "Detectors for a linear collider". *Nucl. Instr. & Meth. in Phys. Res. A*, 581:48–56, 2007.

[13] W. Dulinski et al. "Beam Telescope for Medium Energy Particles based on Thin, Submicron Precision MAPS". *IEEE Nuclear Scince Sypmposium*, Conference Record:995–1002, 2007.

[14] W. Dulinski. "TAPI: High Precision Beam Telescope based on MIMOSA-18 Monolithic Pixel Sensor and TNT2 Data Acquisition Boards". *EUDET-Memo-2008-22*, 2008.

[15] T. Haas. "A pixel telescope for detector R&D for an International Linear Collider". *Nucl. Instr. & Meth. in Phys. Res. A*, 569:53–56, 2006.

[16] P. Roloff. "The EUDET high resolution pixel telescope". *Nucl. Instr. & Meth. in Phys. Res. A*, 604:265–268, 2009.

[17] W.R. Leo. *"Techniques for Nuclear and Particle Physics Experiments: A how-to approach"*. Springer-Verlog, 1994.

[18] B. Rossi. *"High Energy Particles"*. Prentice-Hall Inc., Englewood Cliffs N.J., 1952.

[19] L. Landau. "On the energy loss of fast particles by ionization". *Journal of Physics-USRR*, 8:201–205, 1944.

[20] K.R. Symon. *"Fluctuations in Energy Loss by High Energy Charged Particles in Passing Through Matter"*. PhD thesis, Harvard University, Cambridge, 1948.

[21] P.V. Vavilov. "Ionization losses of high energy heavy particleses". *Soviet Physics-JETP*, 5:749–751, 1957.

[22] T. Rohe L. Rossi, P. Fisher and N. Wermes. *"Pixel Detectors from Fundamentals to Applications"*. Springer, first edition, 2006.

[23] A. Das and T. Ferbel. *"Introduction to nuclear and particle physics"*. World Scientific Publishing Co. Pte. Ltd., second edition, 2004.

[24] G. F. Knoll. *"Radiation Detection and Measurement"*. John Wiley and Sons, second edition, 1989.

[25] M.M. El Baradei, W. Burkart, and M. F. L'Annunziata. *"Handbook of Radioactivity Analysis"*. Academic Press, second edition, 2003.

[26] A. Owens and A. Peacock. "Compound semiconductor radiation detectors". *Nucl. Instr. & Meth. in Phys. Res. A*, 531:18–37, 2004.

[27] H. Bichsel. "Straggling in thin silicon detectors". *Reviews of Modern Physics*, 60:663–699, 1988.

[28] J.M. Benedetto and H.E. Boesch. "The relationship between Co^{60} and 10 keV X-ray damage in MOS devices". *IEEE Trans. on Nucl. Science*, 33:1318–1323, 1986.

[29] H.E. Boesch et al. "Hole transport and charge relaxation in irradiated SiO_2 MOS capacitors". *IEEE Trans. on Nucl. Science*, 22:2163–2167, 1975.

[30] H.E. Boesch et al. "Hole transport and recovery characteristics of SiO_2 gate insulators". *IEEE Trans. on Nucl. Science*, 23:1506–1512, 1976.

[31] T.R. Oldahem and F.B.McLean. "Total Ionizing Dose Effects in MOS Oxides and Devices". *IEEE Trans. on Nucl. Science*, 50:483–499, 2003.

[32] P.M. Lenahan and P.V. Dressendorfer. "Hole traps and trivalent silicon centers in metal/oxide/silicon devices". *Journal of Applied Physics*, 55:3495–3499, 1984.

[33] P.M. Lenahan and P.V. Dressendorfer. "Molecular Hydrogen, E' Center Hole Trap, and Radiation Induced Interface Traps in MOS Devices". *IEEE Trans. on Nucl. Science*, 40:1335–1340, 1993.

[34] P.J. Grunthaner F.J. Grunthaner and J. Maserjian. "Radiation-Induced Defects in $Si0_2$ as Determined With XPS". *IEEE Trans. on Nucl. Science*, 29:1462–1466, 1982.

[35] Y.Y. Kim and J. Park. "Dominant Radiation-Induced Point Defects at the Silicon/Silicon Dixide Interface". *Journal of the Korean Physical Society*, 24:246–249, 1991.

[36] E.H. Poindexter et al. "Electronic traps and Pb centers at the $Si - SiO_2$ Interface: Band-gap energy distribution". *Journal of Applied Physics*, 56:2844–2849, 1984.

[37] P.J. Caplan et al. "ESR Centers, Interface States, and Oxide Fixed Charge in Thermally Oxidized Silicon Wafers". *Journal of Applied Physics*, 50:5847–5854, 1979.

[38] E.H. Poindexter et al. "Interface States and Electron Spin Resonance Centers in Thermally Oxidized (111) and (100) Silicon Wafers". *Journal of Applied Physics*, 52:879–884, 1981.

[39] S.K. Lai. "Interface Trap Generation in Silicon Dioxide When Electrons Are Captured by Trapped Holes". *Journal of Applied Physics*, 54:2540–2546, 1983.

[40] D.L. Griscom. "Diffusion of Radiolytic Molecular Hydrogen as a Mechanism for the Post-irradiation Buildup of Interface States in SiO_2-on-Si Structures". *Journal of Applied Physics*, 58:2524–2533, 1985.

[41] F.B. McLean. "A Framework For Understanding Radiation-Induced Interface States In SiO_2 MOS Structures". *IEEE Trans. on Nucl. Science*, 27:1651–1657, 1980.

[42] C.T. Sah. "Origin Of Interface States And Oxide Charges Generated By Ionizing Radiation". *IEEE Trans. on Nucl. Science*, 23:1563–1568, 1976.

[43] G. Lindstrom et al. "Radiation hardness of silicon detectors – a challenge from high-energy physics". *Nucl. Instr. & Meth. in Phys. Res. A*, 426:1–15, 1999.

[44] L. Rossi, P. Fischer, T. Rohe, and N. Warmes. *"Pixel Detectors"*. Springer, 2006.

[45] H. Spieler. *"Semiconductor Detectors Systems"*. Oxford University Press, second edition, 2006.

[46] W. Shockley and W.T. Read. "Statistics of the Recombinations of Holes and Electrons". *Phys. Rev.*, 87:835–842, 1952.

[47] R.N. Hall. "Electron-Hole Recombination in Germanium". *Phys. Rev.*, 87:387, 1952.

[48] T. Angelescu and A. Vasilescu. "Comparative radiation hardness results obtained from various neutron sources and the NIEL problem". *Nucl. Instr. & Meth. in Phys. Res. A*, 374:85–90, 1996.

[49] A. Vasilescu and G. Lindstrom. "Notes on the fluence normalisation based on the NIEL scaling hypothesis". *ROSE collaboration note: ROSE/TN/2000-02*, 2000.

[50] A. Vasilescu and G. Lindstroem. "Displacement damage in silicon, on-line compilation". http://sesam.desy.de/members/gunnar/Si-dfuncs.html.

[51] G. Lindstrom. "Radiation damage in silicon detectors". *Nucl. Instr. & Meth. in Phys. Res. A*, 512:30–43, 2003.

[52] E. Simeon et al. "Effective generation-recombination parameters in high-energy proton irradiated silicon diodes". *Applied Physics Letters*, 69:1–3, 1996.

[53] Hans-Günther Moser. "Silicon detector systems in high energy physics". *Progress in Particle and Nuclear Physics*, 63:186–237, 2009.

[54] S. Takeda et al. "Double-sided silicon strip detector for x-ray imaging". SPIE Newsroom, 2008.

[55] P.K. Teng et al. "Radiation hardness and lifetime studies of the VCSELs for the ATLAS SemiConductor Tracker". *Nucl. Instr. & Meth. in Phys. Res. A*, 497:294 – 304, 2003.

[56] *"ATLAS: technical proposal for a general-purpose pp experiment at the Large Hadron Collider at CERN. Report No.: CERN-LHCC-94-43 ; LHCC-P-2"*. LHC Tech. Proposal. CERN, Geneva, 1994.

[57] C. Lacasta et al. "The ATLAS semiconductor tracker end-cap module". *Nucl. Instr. & Meth. in Phys. Res. A*, 575:353–389, 2007.

[58] F. Hartmann. *"Evolution of Silicon Sensor Technology in Particle Physics"*, volume 1. Springer-Verlag, Berlin-Heidelberg, 2009.

[59] Y. Unno et al. "Beamtest of non-irradiated and irradiated ATLAS SCT microstrip modules at KEK". *Nuclear Science Symposium Conference Record, 2001 IEEE*, 2:638–645, 2001.

[60] T. Sluka et al. "ATLAS pixel detector commissioning". *Nucl. Instr. & Meth. in Phys. Res. A*, 607:27–30, 2009.

[61] E. Cabruja et al. "Bonding techniques for hybrid active pixel sensors (HAPS)". *Nucl. Instr. & Meth. in Phys. Res. A*, 574:392–400, 2007.

[62] G. Casse. "Overview of the recent activities of the RD50 collaboration on radiation hardening of semiconductor detectors for the sLHC". *Nucl. Instr. & Meth. in Phys. Res. A*, 596:54–60, 2009.

[63] T. Lari. "Radiation tolerance studies of silicon pixel detectors". *Nucl. Instr. & Meth. in Phys. Res. A*, 560:93–97, 2006.

[64] A. Andreazza. "Test beam performance of the ATLAS Pixel Detector modules". *Nucl. Instr. & Meth. in Phys. Res. A*, 565:23–29, 2006.

[65] C. Troncon et al. "A measurement of Lorentz angle and spatial resolution of radiation hard silicon pixel sensors". *Nucl. Instr. & Meth. in Phys. Res. A*, 481:204–221, 2002.

[66] A. Kok et al. "3D sensors - state of the art.". *Nucl. Instr. & Meth. in Phys. Res. A*, 560:127–130, 2006.

[67] S.I. Parker et al. "3D - A proposed new architecture for solid-state radiation detectors". *Nucl. Instr. & Meth. in Phys. Res. A*, 395:328–343, 1997.

[68] C. Da Viá et al. "Radiation hardness properties of full-3D active edge silicon sensors". *Nucl. Instr. & Meth. in Phys. Res. A*, 587:243–249, 2008.

[69] C. Da Viá et al. "3D active edge silicon sensors with different electrode configurations: radiation hardness and noise performance". *Nucl. Instr. & Meth. in Phys. Res. A*, 604:505–511, 2009.

[70] N. Wermes. "Pixel detectors for charged particles". *Nucl. Instr. & Meth. in Phys. Res. A*, 604:370–379, 2009.

[71] M.Mathes et al. "Test Beam Characterization of 3D Silicon pixel Detectors". *IEEE Trans. on Nucl. Science*, 35:3731–3735, 2008.

[72] A. Micelli et al. "3D-FBK pixel sensors: Recent beam tests results with irradiated devices". *Nucl. Instr. & Meth. in Phys. Res. A*, 650:150–157, 2011.

[73] Wim de Boer et al. "Radiation hardness of diamond and silicon sensors compared". *Physica Status Solidi (A)*, 244:3004–3010, 2007.

[74] Velthuis J.J. et al. "Radiation hard diamond pixel detectors". *Nucl. Instr. & Meth. in Phys. Res. A*, 591:221–223, 2008.

[75] P. Bergonzo et al. "CVD diamond for radiation detection devices". *Diamond and related materials*, 10:631–638, 2001.

[76] H. Kagan et al. "Radiation hard diamond sensors for future tracking applications". *Nucl. Instr. & Meth. in Phys. Res. A*, 565:278–283, 2006.

[77] C.J.C. Damerell. "CCD-based vertex detector". *Nucl. Instr. & Meth. in Phys. Res. A*, 541:178–188, 2005.

[78] N.B. Sinev and others. "Investigation of radiation damage effects in neutron irradiated CCD". *Nucl. Instr. & Meth. in Phys. Res. A*, 549:117 – 121, 2005.

[79] K.D. Stefanov et al. "A study of the radiation hardness of a two-phase CCD sensor". *Nucl. Instr. & Meth. in Phys. Res. A*, 453:136–140, 2000.

[80] J.J. Velthuis. "ISIS1 beam test using the EUDET telescope". *EUDET-Memo-2008-36*, 2008.

[81] D. Cussans et al. "Results from the ISIS1 detector". *Nucl. Instr. & Meth. in Phys. Res. A*, 604:393–396, 2009.

[82] J.J. Velthuis et al. "First results of the ISIS1 beam test". *Nucl. Instr. & Meth. in Phys. Res. A*, 599:161–166, 2009.

[83] J. Kemmer and G. Lutz. "New structures for position sensitive detectors". *Nucl. Instr. & Meth. in Phys. Res. A*, 273:588–598, 1988.

[84] C. Sandow et al. "Clear-performance of linear DEPFET devices". *Nucl. Instr. & Meth. in Phys. Res. A*, 568:176–180, 2006.

[85] S. Rummel et al. "Intrinsic properties of DEPFET active pixel sensors". *Journal of Instrumentation*, 4(03):P03003, 2009.

[86] R. Kohrs et al. "First test beam results on DEPFET pixels for the ILC". *Nucl. Instr. & Meth. in Phys. Res. A*, 565:172–177, 2006.

[87] L. Andricek et al. "Processing of ultra-thin silicon for future e^+e^- linear collider experiments". *IEEE Transactions on Consumer Electronics*, 51:1117–1120, 2004.

[88] L. Andricek et al. "The MOS-type DEPFET pixel sensor for the ILC environment". *Nucl. Instr. & Meth. in Phys. Res. A*, 565:165–171, 2006.

[89] L. Andricek and S. Rummel. "The DEPFET active pixel sensor for vertexing at ILC and super KEKB". *Nucl. Instr. & Meth. in Phys. Res. A*, 623:189–191, 2010.

[90] M. Caccia et al. "The SUCIMA project: A status report on high granularity dosimetry and proton beam monitoring". *Nucl. Instr. & Meth. in Phys. Res. A*, 560:153–157, 2006.

[91] W. Kucewicz et al. "Monolithic active pixel detector realized in silicon on insulator technology". *Nucl. Instr. & Meth. in Phys. Res. A*, 535:398–403, 2004.

[92] J. Marczewski et al. "Monolithic silicon pixel detectors in SOI technology". *Nucl. Instr. & Meth. in Phys. Res. A*, 549:112–116, 2005.

[93] H. Manka et al. "Prototypes of large-scale SOI monolithic active pixel sensors". *Nucl. Instr. & Meth. in Phys. Res. A*, 560:31–35, 2006.

[94] S. Cristoloveanu. "Introduction to Silicon On Insulator Materials and Devices". *Microelectronic Engineering*, 39:145–154, 1997.

[95] K. Hara et al. "Radiation Resistance of SOI Pixel Devices Fabricated with OKI 0.15μm FD-SOI Technology". *IEEE Nuclear Science Symposium Conference Record*, 4-5:1369–1374, 2008.

[96] J.R. Schwank et al. "Radiation Effects in SOI Technologies". *IEEE Trans. on Nucl. Science*, 50:522–538, 2003.

[97] Y. Arai et al. "Development of SOI pixel process technology". *Nucl. Instr. & Meth. in Phys. Res. A*, 636:S31–S36, 2011.

[98] M. Kochiyama et al. "Radiation effects in silicon-on-insulator transistors with back-gate control method fabricated with OKI Semiconductor 0.20 μm FD-SOI technology". *Nucl. Instr. & Meth. in Phys. Res. A*, 636:S62–S67, 2011.

[99] A. Dorokhov. Development of in-pixel amplifiers for column parallel MAPS. Private communication.

[100] D. Joseph and S. Collins. "Modeling, calibration, and correction of nonlinear illumination-dependent fixed pattern noise in logarithmic CMOS image sensors". *IEEE Transactions on Instrumentation and Measurement*, 51:996–1001, 2002.

[101] Ch. Ying-Chieh et al. "Low-cost logarithmic CMOS image sensing by nonlinear analog-to-digital conversion". *IEEE Transactions on Consumer Electronics*, 51:1212–1217, 2005.

[102] E. Cabruja et al. "Review of CMOS image sensors". *Microelectronics Journal*, 37:433–451, 2006.

[103] H.Tian. *"Noise analysis in CMOS image sensors"*. PhD thesis, Standfort University, USA., 2000.

[104] R.H. Kingston and A.L. McWhorter. "Relaxation Time of Surface States on Germanium". *Phys. Rev.*, 103:534–540, 1956.

[105] F.N. Hooge. "1/f noise sources". *IEEE Trans. on Electron Devices*, 41:1926–1935, 1994.

[106] H. Tian et al. "Analysis of temporal noise in CMOS photodiode active pixel sensor". *IEEE Transactions on Electron Devices*, 36:92–101, 2001.

[107] M. Deveaux et al. "Random telegraph signal in monolithic active pixel sensors". pages 3098–3105, 2009. Presented at 2008 IEEE Nuclear Science Symposium (NSS) and Medical Imaging Conference (MIC) and 16th International Workshop on Room-Temperature Semiconductor X-Ray and Gamma-Ray Detectors (RTSD), Dresden, Germany, 18-25 Oct 2008.

[108] G.R. Hopkinson. "Radiation effects in a CMOS active pixel sensor". *IEEE Transactions Nuclear Science*, 47:2480–2484, 2000.

[109] G.R. Hopkinson et al. "Random Telegraph signals in proton Irradiated CCDs and APS". *IEEE Transactions on Nuclear Science*, 55:2197–2204, 2008.

[110] J. Bogaerts et al. "Random telegraph signals in a radiation-hardened CMOS active pixel sensor". *IEEE Transactions Nuclear Science*, 49:249–257, 2000.

[111] V. Goiffon et al. "Multilevel RTS in Proton Irradiated SMOS Image Sensors Manufactured in a Deep Submicron technology". *IEEE Transactions on Nuclear Science*, 56:2132–2141, 2009.

[112] H. Muto et al. "Random Telegraph Signals in Small MOSFET's after X-ray Irradiation". *IEEE Transactions on Nuclear Science*, 38:1116–1125, 1991.

[113] P. Martin-Gonthier and P. Morgan. "Low-Frequency Noise Impact on CMOS Image Sensors". *Proceedings 24th Conference on Design of Circuits and Integrated Systems - DCIS09, 18-20 Nov 2009, Zaragoza, Spain*.

[114] C. Leyris et al. "Response of Correlated Double Sampling CMOS Imager Circuit to Random Telegraph Signal Noise". *IEEE Proceedings of the 6th International Caribbean Conference on Devices, Circuits and Systems, Mexico*, pages 109 – 114, 2006.

[115] G. Claus et al. "A Portable System For Monolithic Active Pixel Sensor Characterization". *IEEE Transactions on Electron Devices*, 3:1512–1516, 2004.

[116] G. Garcia et al. "Energy deposition model based on electron scattering cross section data from water molecules". *Journal of Physics: Conference Series*, 133, 2008.

[117] A. Krokosz et al. "Study of the effect of dose-rate on radiation-induced damage to human erythrocytes". *Radiation Physics and Chemistry*, 75:98–105, 2006.

[118] R. Frischknecht et al. "Human health damages due to ionising radiation in life cycle impact assessment". *Environmental Impact Assessment Review*, 20:159–189, 2000.

[119] B.W. Glickman et al. "Radiation risk estimation in human populations: Lessons from the radiological accident in Brazil". *Mutation Research/Fundamental and Molecular Mechanisms of Mutagenesis*, 373:207–214, 1997.

[120] Z. Goldberg et al. "Effects of low-dose ionizing radiation on gene expression in human skin biopsies". *International Journal of Radiation Oncology, Biology and Physics*, 58:567–574, 2004.

[121] F. Faccio. CERN/MIC group X-ray irradiation system. http://proj-xraymic.web.cern.ch.

[122] D. Bisello et al. "X-ray radiation source for total dose radiation studies". *Radiation Physics and Chemistry*, 71:713–715, 2004.

[123] L.J. Palkuti and J.J. LePage. "X-Ray Wafer Probe for Total Dose Testing". *IEEE Transactions on Nuclear Science*, 29:1832–1837, 1982.

[124] F. Faccio. - in charge of X-Ray gun at CERN. Private communication .

[125] D.K. Nichols. "A Review of Dose Rate Dependent Effects of Total Ionizing Dose (TID) Irradiations". *IEEE Trans. on Nucl. Science*, 27:1016–1024, 1980.

[126] D.G. Cleveland. "Dose Rate Effects in MOS Microcircuits". *IEEE Trans. on Nucl. Science*, 31:1348–1353, 1984.

[127] R.E. Sharp and S.L. Pater Cleveland. "The influence of dose rate on total dose radiation effects on MOSFETs". *Proceedings of 6th Europen Conference on Radiation and its Effects on Components and Systems*, pages 488–493, 2001.

[128] A.L. Bogorad et al. "Total Ionizing Dose and Dose Rate Effects in Candidate Spacecraft Electronic Devices". *Proceedings of Radiation Effects Data Workshop*, pages 124–130, 2008.

[129] M. Ullan. "Ionizing Damage on ATLAS-STC Front-End Electronics Considering Low Dose Rate Efeects". *IEEE Trans. on Nucl. Science*, 49:1106–1111, 2002.

[130] A. Gorisek. - in charge of neutron irradiation in Ljubljana - private communication.

[131] H. Breitkreutz et al. "Spectral fluence rates of the fast reactor neutron beam MedApp at FRM II". *Nucl. Instr. & Meth. in Phys. Res. A*, 593:466–471, 2008.

[132] J. Bogaerts. *"Radiation-induced degradation effects in CMOS Active Pixel Sensors and design of a radiation tolerant image sensor"*. PhD thesis, Katholieke Universiteit Leuven, Belgium, April 2002.

[133] H.L. Hughes and J.M. Benedetto. "Radiation effects and hardening of MOS technology: devices and circuits". *IEEE Trans. on Nucl. Science*, 50:500–521, 2003.

[134] W. Snoeys et al. "Layout techniques to enhance the radiation tolerance of standard CMOS technologies demonstrated on a pixel detector readout chip". *Nucl. Instr. & Meth. in Phys. Res. A*, 439:349–360, 2000.

[135] D.M. Fleetwood et al. "1/f Noise and Radiation Effects in MOS Devices". *IEEE Trans. on Nucl. Science*, 41:1953–1964, 1994.

[136] H.D. Xiong et al. "Temperature Dependence and Irradiation Response of 1/f Noise in MOSFETs". *IEEE Trans. on Nucl. Science*, 49:2718–2723, 2002.

[137] C. Jakobson et al. "1/F Noise in CMOS Transistors for Analog Applications from Subtreshold to Saturation". *Solid State Electronics*, 42:1807–1817, 1998.

[138] K.W. Chew et al. "Impact of technology scaling on the 1/f noise in thin and thick gate oxide deep submicron NMOS transistors". *IEEE Proceedings - Circuits, Devices and Systems*, 151:415–421, 2004.

[139] M. Deveaux et al. "Charge collection properties of Monolithic Active Pixel Sensors (MAPS) irradiated with non-ionizing radiation". *Nucl. Instr. & Meth. in Phys. Res. A*, 583:134–138, 2007.

[140] A. Besson et al. "Achievements of CMOS Pixel Sensors for the CBM Micro-Vertex Detector". Scientific Report 2007, Fair-Experiments-05, http://www.gsi.de/informationen/wti/library/scientificreport2007/.

[141] Y. Degerli et al. "Development of Binary Readout CMOS Monolithic Sensors for MIP Tracking". *IEEE Trans. on Nucl. Science*, 56:354–363, 2009.

[142] Y. Degerli. "Design of fundamental building blocks for fast binary readout CMOS sensors used in high-energy physics experiments". *Nucl. Instr. & Meth. in Phys. Res. A*, 602:461–466, 2009.

[143] G. Deptuch et al. "Monolithic Active Pixel Sensors with in-pixel double sampling operation and column-level discrimination". *IEEE Trans. on Nucl. Science*, 51:2313–2321, 2004.

[144] G. Deptuch et al. "Monolithic Active Pixel Sensors with on-pixel amplification and double sampling". *Nucl. Instr. & Meth. in Phys. Res. A*, 512:299–309, 2003.

[145] M. Szelezniak et al. "Application-specific architectures of CMOS monolithic active pixel sensors". *Nucl. Instr. & Meth. in Phys. Res. A*, 568:185–190, 2006.

[146] M. Winter. "Development of swift and slim CMOS sensors for a vertex detector at the International Linear Collider". *ILC Vertex Detector review ALCPG-07; American Linear Collider Physics Group.*, 2007.

[147] R. Merrill. "Intra-pixel reset noise cancellation.". *Proceedings of IEEE Workshop on Charge Coupled Devices and Advanced Image Sensors, Lake Tahoe, The United States*, pages 153–156, 2001.

[148] Y. Degerli. "Monolithic active pixels with in-pixel amplification and reset noise suppression for charged particle detection in a 0.25μm digital CMOS process". *DAPNIA preprint no.: DAPNIA-04-184*, 2003.

[149] Y. Degerli et al. "A fast monolithic active pixel sensor with pixel-level reset noise suppression and binary output for charged particle detection". *IEEE Trans. on Nucl. Science*, 52:3186–3193, 2005.

[150] Y. Degerli et al. "Performance of a fast binary readout CMOS active pixel sensor chip designed for charged particle detection". *IEEE Trans. on Nucl. Science*, 53:3949–3955, 2004.

[151] Y. Degerli et al. "Low-power Autozeroed highspeed comparator for the readout chain of a CMOS monolitjic active pixel sensors based vertex detectors". *IEEE Trans. on Nucl. Science*, 50:1709–1717, 2003.

[152] C. Colledani et al. "A submicron precision silicon telescope for beam test purposes". *Nucl. Instr. & Meth. in Phys. Res. A*, 372:379–384, 1996.

[153] IEEE Standards 1149.1-2001 (R2008). "IEEE Standard Test Access Port and Boundary-Scan Architecture". ISBN 0-7381-2944-5 SH94949.

[154] IPHC internal note. "MIMOSA-22 user manual".

[155] A. Dorokhov. "Design and Characterisation of a Fast Architecture Providing Zero Suppressed Digital Output Integrated in a High Resolution CMOS Pixel Sensor for the STAR Vertex Detector and the EUDET Beam Telescope". *Presented at TWEPP conference, Prague, Czech Republic*, 2007.

[156] M. Winter et al. "JRA-1 Beam Telescope Towards the Final Pixel Sensor". *EUDET-Memo-2008-51*, 2008.

[157] M. Winter et al. "JRA-1 Milestone: SDC Prototype 2 Ready". *EUDET-Memo-2007-55*, 2007.

[158] Synopsys Inc. Process and Device Simulation Tools.

[159] M. Förtsch et al. "Integrated PIN Photodiodes in High-Performance BiCMOS Technology". *Presented at Electron Devices Meeting, IEDM '02. Digest. International*, 2002.

[160] A.R. Alvarez. *"BiCMOS Technology and Applications."*. Springer, second edition, 1993.

[161] B.R. Hancock and G.A. Soli. "Total dose testing of a CMOS charged particle spectrometer". *IEEE Trans. on Nucl. Science*, 44:1957–1964, 1997.

[162] E.S. Eid et al. "Design and characterization of ionizing radiation-tolerant CMOS APSimage sensors up to 30 Mrd (Si) total dose". *IEEE Trans. on Nucl. Science*, 48:1796–1806, 2001.

[163] J. Bogaerts et al. "Total dose and displacement damage effects in a radiation-hardened CMOS APS". *IEEE Trans. on Nucl. Science*, 50:84–90, 2003.

[164] V. Goiffon et al. "Ionization versus displacement damage effects in proton irradiated CMOS sensors manufactured in deep submicron process". *Nucl. Instr. & Meth. in Phys. Res. A*, 610:225–229, 2009.

[165] M. Turala. "Silicon tracking detectors–historical overview". *Nucl. Instr. & Meth. in Phys. Res. A*, 541(1-2):1–14, 2005.

[166] J.R. Janesick. *"Scientific Charge-Coupled Device"*. SPIE Press, 2001.

[167] K. Stefanov. *"Radiation damage effects in CCD sensors for tracking applications in high energy physics"*. PhD thesis, Saga University (Japan), 2001.

[168] J.E. Brau and N.B. Sinev. Operation of a CCD particle detector in the presence of bulk neutron damage. *IEEE Trans. Nucl. Sci.*, 47:1898–1901, 2000.

[169] A. Sopczak. LCFI charge transfer inefficiency studies for CCD vertex detectors. Prepared for 9th ICATPP Conference on Astroparticle, Particle, Space Physics, Detectors and Medical Physics Applications, Villa Erba, Como, Italy, 17-21 Oct 2005.

[170] M.S. Robbins. "The Radiation Damage Performance of Marconi CCD". Marconi Technical Note S&C 906/424 2000 (unpublished).

[171] T. Maruyama. "Neutron background at the ILC". Private communication, Stanford Linear Accelerator Center (SLAC), 2006.

[172] A. Vogel. "Neutron background at the ILC.". Private communication, (DESY Hamburg), 2006.

[173] M.S. Robbins and others. "Quality control and monitoring of radiation damage in charge coupled devices at the Stanford Linear Collider". *IEEE Trans. Nucl. Sci.*, 40:1561–1566, 1993.

[174] M.S. Robbins and others. "Degradation of the charge transfer efficiency of a buried channel charge coupled device due to radiation damage by a beta source". *Proceedings of the First European Conference on Radiation and its Effects on Devices and Systems, RADECS 91.*, pages 327–332, 1991.

[175] J.W. Walker and C.T. Sah. "Properties of 1.0-MeV-Electron-Irradiated Defect Centers in Silicon". *Phys. Rev. B*, 7:4587–4605, 1973.

[176] G.K. Wertheim. "Electron-Bombardment Damage in Silicon". *Phys. Rev. B*, 110:1272–1279, 1958.

[177] M. Suezawa. "Formation of defect complexes by electron-irradiation of hydrogenated crystalline silicon". *Phys. Rev. B*, 63, 2000.

[178] N.S. Saks. "Investigation of Bulk Electron Traps Created by Fast Neutron Irradiation in a Buried N-Channel CCD". *IEEE Trans. Nucl. Sci.*, 24:2153–2157, 1977.

[179] J.R. Srour et al. "Transient and Permanent Effects of Neutron Bombardment on a Commercially Available N-Buried-Channel CCD". *IEEE Trans. Nucl. Sci.*, 27:1402–1410, 1980.

[180] E. Fretwurst et al. "Neutron induced defects in silicon detectors characterized by DLTS and TSC methods". *Nucl. Instr. & Meth. in Phys. Res. A*, 377:258 – 264, 1996.

[181] K.D. Stefanov. "CCD-based vertex detector for the future linear collider". *Nucl. Instr. & Meth. in Phys. Res. A*, 549:93–98, 2005.

[182] K. Dawson et al. "Radiation Tolerance of Fully-Depleted P-Channel CCDs Designed for the SNAP Satellite". *IEEE Trans. Nucl. Sci.*, 55:1725–1735, 2008.

[183] A. Sopczak et al. "Comparison of Measurements of Charge Transfer Inefficiencies in a CCD With High-Speed Column Parallel Readout". *IEEE Trans. on Nucl. Science*, 57:854–859, 2010.

[184] D. Doering. private communication – D.Doering is the PhD student in charge of MAPS radiation tolerance assesment at IKF-Frankfurt - Germany.

[185] M.H. White et al. "Characterization of surface channel CCD image arrays at low light levels". *IEEE Journal of Solid-State Circuits*, 9:1–12, 1974.

[186] R.W. Brodersen and S.P. Emmons. "Noise in buried channel charge-coupled devices". *IEEE Transactions on Electron Devices*, 23:215–223, 1976.

[187] Austria Microsystms. "0.35 μm CMOS C35 Design Rules". Document: ENG-183.

RESUME :

Les capteurs CMOS sont développés depuis une décennie en vue d'équiper les détecteurs de vertex des expériences de physique des particules à venir, avec les avantages d'un faible budget de matière et de bas coûts de production. Les caractéristiques recherchées sont un temps de lecture court, une granularité élevée et une bonne radiorésistance. Cette thèse est principalement consacrée à l'optimisation de ce dernier point. Pour diminuer le temps de cycle vers les 10 microsecondes, la lecture des pixels en parallèle dans chaque colonne a été implémentée, associée à une logique de suppression d'information des pixels sans signal. Les pixels sont devenus plus complexes et plus sensibles aux rayonnements ionisants. L'optimisation de l'architecture des pixels, par des techniques standard de durcissement aux rayonnements, a porté la limite à 300 krad (quelques Mrad attendus) pour le procédé de fabrication à 0,35-µm utilisé jusque-là. L'amélioration de la tenue aux rayonnements ionisants passe par l'utilisation de technologies de taille inférieure à 0,35-µm, naturellement plus radio-résistantes. Ceci facilitant de plus l'intégration de tous les composants dans un pixel.

Un autre aspect abordé dans cette thèse concerne la tolérance aux rayonnements non ionisants. Différentes technologies CMOS améliorant la collecte de charges ont été testées. L'utilisation d'une couche de détection de haute résistivité a porté la tenue à ces rayonnements à $3 \cdot 10^{13}$ n_{eq}/cm^2, conforme à l'objectif fixé. Ce résultat marque une étape importante pour les capteurs CMOS qui devraient rapidement satisfaire le cahier des charges d'expériences particulièrement contraignantes telles que CBM par exemple.

ABSTRACT :

CMOS Pixel Sensors are being developed since a few years to equip vertex detectors for future high-energy physics experiments with the crucial advantages of a low material budget and low production costs. The features simultaneously required are a short readout time, high granularity and high tolerance to radiation. This thesis mainly focuses on the radiation tolerance studies. To achieve the targeted readout time (tens of microseconds), the sensor pixel readout was organized in parallel columns restricting in addition the readout to pixels that had collected the signal charge. The pixels became then more complex, and consequently more sensitive to radiation. Different in-pixel architectures were studied and it was concluded that the tolerance to ionizing radiation was limited to 300 krad with the 0.35-µm fabrication process currently used, while the targeted value was several Mrad. Improving this situation calls for implementation of the sensors in processes with a smaller feature size which naturally improve the radiation tolerance while simultaneously accommodate all the in-pixel microcircuitry in small pixels.

Another aspect addressed in this thesis was the tolerance to non ionizing radiation, with a targeted value of $>10^{13}$ n_{eq}/cm^2. Different CMOS technologies featuring an enhanced signal collection were therefore investigated. It was demonstrated that this tolerance could be improved to $3 \cdot 10^{13}$ n_{eq}/cm^2 by the means of a high-resistivity epitaxial layer. This achievement triggered a new age of the CMOS pixel sensors and showed that their development is on a good track to meet the requirements of the particularly demanding CBM experiment.