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par

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Développement de Capteurs à Pixel CMOS pour un Détecteur de Vertex Adapté au Collisionneur ILC

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THESIS

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by

Yunan FU

Development of CMOS Pixel Sensors for a Vertex Detector Suited to the ILC

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There is no royal road to science, and only those who do not dread the fatiguing climb of its steep paths have a chance of gaining its luminous summits.

—-Karl Heinrich Marx

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Strasbourg, 2012

Introduction

A large fraction of the world wide particle physics community elaborates its future on an e+ e- collider called International Linear Collider (ILC), which is expected to start providing beams for physics beyond 2020. The ILC offers experimental conditions which allow for very high precision measurements, provided the experiments installed around the beam interaction regions exhibit a sensitivity allowing to take advantage of these favorable conditions.

Existing detection technologies, such as those used at the Large Hardon Collider (LHC), are often inadequate for this purpose. The case is particularly striking for the vertex detector, which requires developing a new generation of sensors, which would be much more granular and thin than those in use, while allowing to cope with the intense beam related background particles which swamp the inner layer of the detector.

Several pixel technologies are being developed since many years to comply with the required specifications. CMOS pixel sensors (CPS)[1] are well suited for this type of application, where the running conditions are still not as demanding as those imposed at hadron colliders such as the LHC. The fact that the running conditions are milder allows privileging the specifications imposed by the physics goals, and fosters developing a sensor design allowing for the fastest readout speed and highest radiation tolerance not affecting the physics driven performances.

CPS are being developed at IPHC since more than a decade for this purpose, motivated by the necessary readout speed and power consumption improvements, the radiation tolerance being a lesser issue despite the ambition to run at room temperature.

The readout speed achieved up to now complies with the requirements expressed in the Letter of Intent (LoI) of the International Large Detector (ILD) detector concept, adapted to the first phase of the ILC project (characterized by a collision energy of up to 500 GeV). It is not suited to the higher particle rate expected at the energies foreseen

[1]CMOS pixel sensors are also called CMOS Monolithic Active Pixel Sensors (MAPS).

for the second phase of the collider running (up to about 1 TeV). A higher readout speed than the one achieved today would also allow feeling more comfortable in case the beam background turns out to be much higher than expected.

The goal for this second phase is to reach a readout time below 10 μs while keeping the spatial resolution below 3 μm . Speed and resolution are strongly correlated parameters: in the column parallel readout architecture on which present sensors are based, a small pixel pitch, as required by the ambitioned resolution, translates into a large number of pixels to be read out (serially) in each column, at the expense of the readout speed and, possibly, of the power consumption.

3D integration technologies (3DIT) provide a way to mitigate this hampering correlation between speed and resolution, since they allow to staple layers of readout circuitry on top of the sensing layer, which results in a drastic increase of the functionalities located in (the shadow of) each pixel. A multi-layer structure allows for a higher spatial resolution because more and more transistors may be integrated vertically in a relatively small pixel. Moreover, bringing the components of the sensor closer to each other translates in a faster readout, owing to the reduction in the average length of the inner-connecting wires. Vertical integration also opens up the possibility of combining different technologies best suited to each of the sensor main functionalities (signal sensing, analog and digital signal processing and transmission). 3D-CPS are thus expected to overcome most of the limitations of 2D-CPS, and are therefore suspected to offer new perspectives for the innermost layer of the ILC vertex detector. This thesis was motivated by these perspectives.

Besides emerging 3D integration techniques, a double-sided ladder[2] concept based on 2D-CPS is another way to alleviate, though in a lesser extent, the conflict between speed and resolution. This approach consists in equipping each side of the ladders composing the detector with sensors optimized for different, but complementary, functionalities: spatial resolution on one side and time resolution on the other. The two functionalities are combined for traversing particles by correlating their impacts reconstructed on each ladder side.

While the concept is based on the position resolution delivered by state-of-the-art sensors (based on square pixels), the time resolution requires steps ahead. A part of this thesis is devoted to the design of 2D-CPS with novel in-pixel amplifiers and pixel-level discriminators for this purpose, relying on elongated pixels. Sensors made of both types

[2]Called PLUME ladder (Pixelated Ladder with Ultra-low Material Embedding).

of pixels were fabricated in a multi-well CMOS technology, which allows for in-pixel full CMOS capability without degradation of the detection efficiency. These 2D-CPS with significant in-pixel processing capability are important forerunners of those fully complying with the targeted requirements.

Micro-circuit designs developed within the thesis

Several micro-circuits were designed within the framework of the thesis, adapted to the evolution of the sensors developed by the PICSEL group of IPHC. Some main features of these sensors are summarized below. The development of CPS for charged particle tracking was started at IPHC in the late nineties. In these devices, the sensor volume and electronics share the same substrate, and in-pixel signal processing can be performed. The charge is generated in the sensing layer and reaches the electrodes by thermal diffusion in the CMOS technologies with a low-resistivity epitaxial layer. This scheme allows for a high granularity with resolution down to $\sim$ 1-2 μm at very low noise. The question was raised on how the other driving parameters of the innermost layer of the ILC vertex detector, i.e. the sensor readout speed and power consumption, can be accommodated.

In order to obtain a high readout speed, the pixel columns of a pixel array are read out in parallel by sweeping the array with a row-wise rolling shutter (e.g. MIMOSA-26 sensors). A singularity of CPS is that their integration time corresponds to the readout time of the whole pixel array. Although MIMOSA-26 sensors have made a big progress in terms of integration time reduction (it amounts to $\sim$ 100 μs), the column parallel architecture becomes a bottleneck to improve the readout speed for a large-scale pixel array. The global frame readout time is actually limited by the sizable number of rows (typically several hundreds to about one thousand) and the row processing time (typically 200 ns). A pixelated double-sided ladder equipped with two types of 2D-CPS is a first step against this bottleneck. This approach is also advantageous in terms of power consumption.

The required spatial resolution can be achieved with square pixels of $\sim$ 16 μm pitch. A shortening of the readout time may be obtained with an elongated pixel pitch in the column readout direction. By correlating the two hits on both faces of the ladder generated by a traversing particle, the latter gets assigned a spatial resolution of $\sim$ 3 μm together with a time resolution of below 10 μs .

To obtain the ambitioned single point resolution, a $\lesssim 16$ μm pitch pixel with a novel in-pixel amplifier was designed. Theory, circuit simulation and measurement of implemented structure indicate that this advantageous **multi-stage in-pixel amplifier** can potentially provide a better signal-to-noise ratio (SNR) performance than a single-stage amplifier, currently used in present 2D-CPS.

To reach the targeted time resolution, a 16 μm $\times$ 80 μm pitch pixel with a pixel-level discriminator was developed. This **digital pixel sensor architecture** allows digitizing the signal charge within each pixel. Moreover, the readout gets substantially accelerated, as compared to the conventional methodology in which the signal is accumulated on a large parasitic capacitor at each column end. In addition, a relatively large current is required to drive the parasitic capacitor and to maintain a satisfactory signal-to-noise ratio of the analog outputs used in the conventional designs, which translates into extra power consumption. The in-pixel digital outputs make the new approach amenable to development of low-power 2D-CPS, for it eliminates the analog readout bottlenecks. This approach was addressed extensively in this thesis. Its fast readout speed, integration capabilities and low power operation represent a substantial progress w.r.t. existing 2D-CPS approaches.

The next important topic of the thesis concerns 3D-CPS. An important part of the work was devoted to the achievement of low noise, fast, sensors as required for the ILC vertex detector, while keeping the power consumption at an affordable level. Two alternative readout approaches are being investigated: one, called delayed readout, where the signals are stored in the sensors during the bunch train interval and read out during the beam-less period (adapted to the beam time structure of the ILC), and another, called continuous readout, where the sensors continuously transfer the measured signals for readout. In this thesis, these two complementary readout strategies were explored in parallel in order to evaluate and compare their potential and benefits.

The delayed readout approach is motivated by power savings. It consists in implementing a circuitry which accumulates the hits from each pixel during the complete collider train, and to read it out in between consecutive trains using a very low-frequency clock. **3D-CPS with delayed readout**: A 2-tier sensor featuring a 12 μm pitch pixel array, which incorporates in-pixel signal discrimination and time-stamping, was developed in the framework of the thesis. The pixel cell of the bottom (analog) layer includes an n-well/p-substrate diode, a shaper and a threshold discriminator, whose output is

vertically interconnected to the digital pixel on the top tier. Each digital pixel has the capability for storing double hits and the 5-bit time stamps of the relevant first hit.

Another **3D-CPS with continuous readout** (i.e. parallel rolling shutter readout) was designed, developed and tested in this thesis. By taking advantages of 3DIT, the parallel continuous readout architecture overcomes many limitations imposed by conventional rolling shutter readout. The entire pixel array could be split into several sub-arrays. Each sub-array is organized independently in a rolling shutter mode and all sub-arrays are read out in parallel. The global frame readout time is therefore reduced to the time of rolling the shutter across the exposable sensitive area of each sub-array. Moreover, with the reduced parasitic capacitors between analog and digital sections, it is possible to place a considerable amount of small pixels with a power saving feature. The power consumption estimation also shows that this readout architecture has the potential to comply with the power dissipation constraints set for the ILD vertex detector, despite the consumption increase consecutive to the parallelized readout.

In this 3D-CPS, the pixel of the analog tier consists of a diode, a first amplification stage, a first double sampling circuitry and a discriminator. The discriminator output is vertically connected to the digital pixel for performing zero suppression. As a first step towards verifying the functionalities of the pixels, the in-pixel discriminator and zero-suppressing readout circuit have been realized[3] in a 0.13 μm CMOS technology. An alternative approach is also proposed, where a 3-bit pixel-level Analog-to Digital Converter (ADC) is integrated in each pixel for improving the spatial resolution provided by a 20 μm pitch pixel initially equipped with a 1-bit discriminator. Power dissipation concern leads to the investigation of a single-slope ADC, those design includes a diode, a comparator and 3-bit memory in each pixel. The pixel-level ADCs operating in the parallel rolling shutter mode could maintain high frame rate and required spatial resolution.

Thesis layout

This thesis is organized in two parts. The first part, spanning from chapter 1 to 2, is dedicated to the topic of 2D-CPS. Chapter 1 gives a description of the requirements of the innermost layer of an ILC vertex detector, and of different types of CPS. Chapter 2 introduces a light double-sided ladder equipped with 2D-CPS. It is considered as a possible solution to meet the specified requirements. In order to obtain a high signal-

[3] The pixel pitch is 20 μm pitch.

to-noise ratio of the pixel, a novel pixel structure based on multi-stage amplification is presented. We discuss the results of the characterization of an implemented pixel employing this novel offset compensated amplifier.

The second part of this thesis, which consists of chapter 3, 4 and 5, covers the topic of 3D-CPS. A design of 3D-CPS with delayed readout is presented in chapter 3. Chapter 4 introduces novel pixel topologies of 3D-CPS featuring parallel continuous readout. The analysis of the pixel circuits, test results of the proposed pixel-level discriminator and zero-suppressing readout are presented. Chapter 5 describes an alternative pixel architecture (using a 3-bit pixel-level ADC) for a high spatial resolution. The characterization of the pixel-level ADC is also discussed in the same chapter.

The main outcome of the PhD are summarized and discussed at the end of the document, complemented with an outlook providing proposals on the most promising ways to pursue the development of the different approaches addressed in the thesis.

Chapter 1

CMOS pixel sensors for the ILC vertex detector

1.1 Scientific motivation for the ILC

The Large Hadron Collider (LHC), the world's most powerful particle accelerator, started its physics programme with first collisions at CERN. The LHC is a proton-proton collider and has provided 3.5 TeV per beam up to now, i.e. the collision energy amounts to 7 TeV. By 2014, it will reach 14 TeV. The International Linear Collider (ILC) will collide electrons and positrons at energies of initially 500 GeV, upgradeable to 1 TeV at least. Together with the LHC, it will offer mutually supporting views of the new physics world at the TeV-scale.

The ILC has an ambitious physics program, which will extend and complement that of the LHC. It can provide a wealth of information on Standard Model physics and on yet unresolved questions it triggers [1]. Based on experiments and discoveries over the last decades, physicists believe that the TeV-scale will yield evidence for new forms of matter and possibly even extra dimensions of space. The new matter is expected to rely on a Higgs boson and may, for instance, include an extended family of elementary super particles. These discoveries will continue telling us about the nature of the Universe and how the laws of physics came to be.

The ILC scheme calls for two detectors, called International Large Detector (ILD) and Silicon Detector (SiD) [2]. The two detector designs for the ILC are now being elaborated by the ILD and SiD groups towards the Detailed Baseline Design Report (DBD), their layouts are shown in Figure 1.1. These two detector concepts take different approaches for the cost-performance optimization.

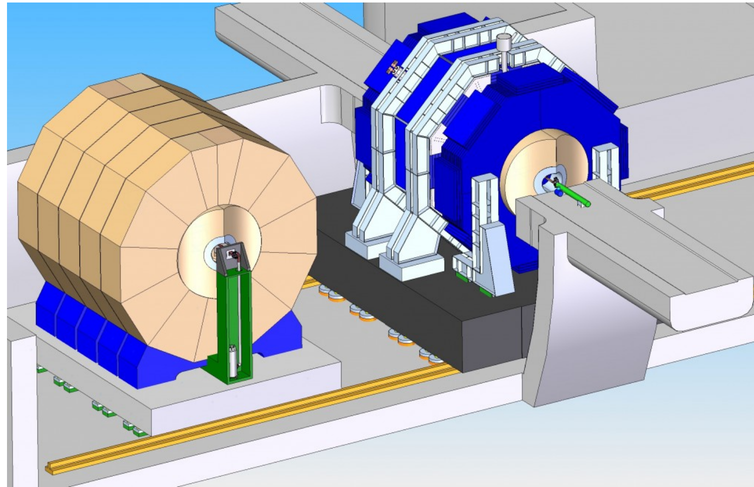


Figure 1.1: Two detectors in the detector hall. ILD (left) is offline, and SiD (right) is shown in the beamline.

While the SiD apparatus relies on a central tracker composed of silicon strips, the ILD design is based on a Time Projection Chambre (TPC). Material budget considerations impose the SiD main tracker to be composed of 5 layers only, which imposes the vertex detector to provide track seeding. With its gaseous detection medium, the ILD main tracker is much less constrained in terms of material budget and provides more than 200 impacts for fully traversing particles. This improved situation alleviates the requirements on the vertex detector readout time, which is not supposed to play a central role in track seeding. The SiD, on the other hand, is more compact than ILD, a difference which benefits to the overall cost, driven by the dimensions of the calorimetres, as well as to the achievable experimental field (5 T against 3.5 T for ILD).

Two alternative vertex detector (VTX) geometries are being considered within the ILD concept [3]. Both geometries are purely cylindrical. The first geometry (called VTX-DL) features 3 double-sided layers, where each layer is equipped with two, $\lesssim 2$ mm apart, arrays of sensors. The second geometry (called VTX-SL) features 5 single-sided layers equipped with one layer of sensors only. Both geometries are shown in Figure 1.2. The double-sided layer option allows spatial correlations between hits generated by the same particle in the two sensor layers equipping a ladder. It is expected to provide better rejection of beamstrahlung background (low momentum < 300 MeV/c) [3] and to provide additional pointing accuracy. The VTX-DL presents however a more challenging goal because of the limited experience in double-sided ladders compared to in single-sided ones. Selected main geometrical parameters of the two VTXs are listed in Table 1.1.

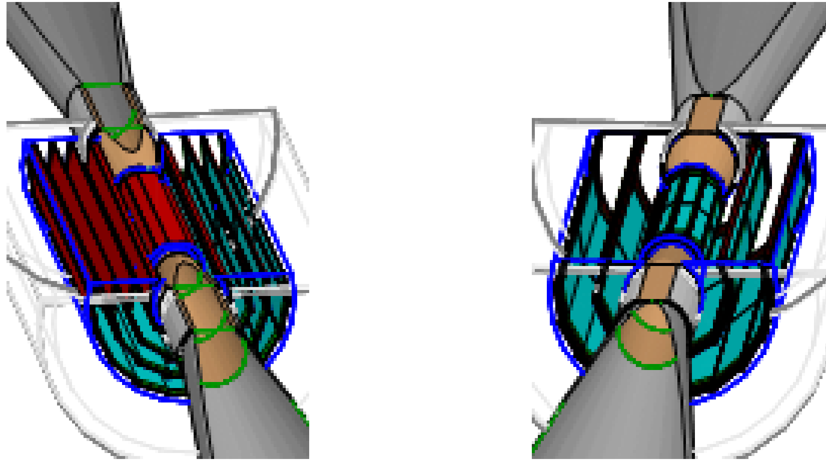


Figure 1.2: Vertex detector geometries of the two design options: (left) 5 single-sided layers (VTX-SL), (right) 3 double-sided layers (VTX-DL).

All vertexing system designs under consideration include a pixelated vertex detector, which surrounds as close as possible the Interaction Point (IP) for accurate measurements of charged particle impact parameters. This creates a major technical challenge because of the rapidly increasing beam-related background when approaching the IP. The sensor technology best adapted to the high background environment is not yet defined. It would be difficult for well established technologies to meet simultaneously all requirements, defined by the physics goals (granularity, material budget) and those imposed by the running conditions (readout speed and radiation dose). Several alternative pixel technologies are therefore being considered and developed [4, 5, 6], among which CPS are one of the most promising candidates. This thesis focuses on developing innovative CPS

Table 1.1: Radius and ladder length for each layer of the two vertex detector geometries.

	radius[mm]		ladder length [mm]	
geometry	VTX-SL	VTX-DL	VTX-SL	VTX-DL
layer1	15	16/18	125	125
layer2	26	37/39	250	250
layer3	37	58/60	250	250
layer4	48		250	
layer5	60		250	

to satisfy the requirements of the innermost layer of an ILC vertex detector, taking the ILD concept as a reference.

1.2 Requirements for CMOS pixel sensors

The small pixel pitch desired for a high spatial resolution requires a large number of pixels per surface unit, which translates into a high power consumption and/or a slow readout speed. The granularity and readout speed drive the power dissipation, which also impacts more or less severely the material budget, depending on the type of cooling system required. It is therefore unavoidable that the sensor R&D concentrates on a balance between those conflicting requirements. The latter is summarized in the coming sub-section.

1.2.1 Requirements from the physics goals

The ILC vertex detectors will provide the central tool for flavour identification based on the displaced vertex of weakly decaying particles. Beauty- and charm-tagging, or even more sophisticated methods such as separated identification of quark and anti-quark jets will be addressed [3]. One of the key detector parameters is the track impact parameter resolution (σ_{ip}), which can be parametrized for a set of cylindrical detector layers as [3]:

$$\sigma_{ip} = a \oplus b/p \cdot \sin^{3/2}\theta \tag{1.1}$$

Where the constant a reflects the single point resolution and the geometrical stability of the detectors, the parameter b represents the resolution degradation due to multiple scattering, which varies with the incident particle momentum p and the track polar angle θ measured with respect to the beam direction. a and b are required to be below 5 μm and 10 μm$\cdot$ GeV/c, respectively. The innermost layer has a radius of 15/16 mm and intercepts all particles produced with a polar angle such that $|\cos\theta| \leq 0.97$. Monte-Carlo studies show that to achieve these specifications:

- The spatial resolution should be $\lesssim 3$ μm.
- The distance between the first measured point of tracks and the IP should be less than ~ 20 mm.
- The material budget should be limited to only a few per mill of radiation length.

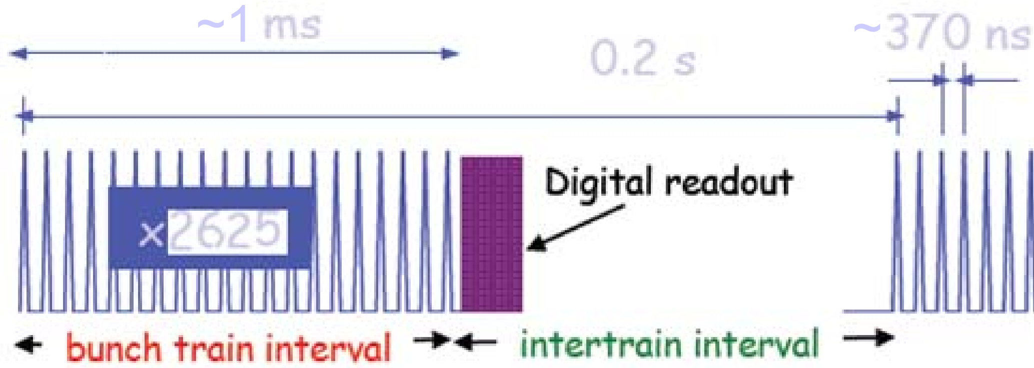


Figure 1.3: The schematic of the bunch timing of the ILC.

- The length of the sensor ladder should typically be about $\sim$ 125 mm.

1.2.2 Requirements from the running conditions

1.2.2.1 Readout speed

The time structure of the ILC bunch train has been described in the Reference Design Report (RDR) [7]. As shown in Figure 1.3, the beam is divided into bunch trains of $\sim$ 1 ms length, containing 2625 bunches with a period of 200 ms. In order to establish a better and more cost-effective baseline, the 2009 Strawman Basline option (SB2009) [8] was proposed, with some major modifications to the design of the ILC. It benefits from a lower beam-power parameter set, obtained with a twice smaller number of bunches per pulse ($\sim$ 1312), as compared to the nominal RDR parameter set.

The hit rate is highest in the innermost layer and is governed by beam-related background. The latter is essentially due to incoherent e^+ e^- pairs produced through beamstrahlung processes. Their rate was estimated with Monte-Carlo simulations, which predict 5.3/4.4 $\pm$ 0.5 hits/cm^2 per bunch crossing at 15/16 mm radius [9]. Extensive background simulations have also been performed with the latest beam geometry. They lead to similar rate values. The latter translate in demanding readout speed requirements in order to keep the occupancy at an affordable level ($\lesssim$ few %) [9].

The acceptable time resolution indicated in the LoI of the ILD is 25-50 μs, for the foreseen running conditions at a collision energy of up to $\sim$ 500 GeV. This time is shorter for the SiD vertex detector, where it is more alike a few μs in order to be able to achieve standalone tracking in the vertex detector. In this thesis, a time resolution well below 10 μs is a target value for both ILD and SiD vertex detectors. In the case of ILD, the

Table 1.2: The requirements of the sensors for the innermost layer of the ILD vertex detector. The values address a collision energy $\lesssim$ 500 GeV, except for the time resolution, which is also provided for 1 TeV.

Radiation tolerance to non-ionizing particles	$O(10^{11}) n_{eq}/cm^2$
Radiation tolerance to ionizing particles	$\sim$ 150 kRad/per year
Spatial resolution	2-3 μm
Material budget per ladder	0.2-0.3% Xo
Time resolution (center-of-mass energy of 500 GeV)	$\lesssim$ 25-50 μs
Time resolution (center-of-mass energy of 1 TeV)	$<$ 10 μs

targeted readout time is intended for the running condition at a collision energy near 1 TeV or above, where the beam related background is expected to be a couple of times higher than at 500 GeV as a consequence of the higher luminosity.

1.2.2.2 Radiation tolerance

From the simulations, the annual ionising dose was calculated to be in the order of 50 kRad per year at 15 mm radius. To account for the limited accuracy of the simulated beamstrahlung rate, it is multiplied by a safety factor of 3 to derive the sensor specification. At least 2 years of operation were assumed before replacing the sensors. Overall, an ionising radiation tolerance of 300 kRad is required for a 2 year life time [10]. The corresponding non-ionising radiation tolerance amounts to $\lesssim 1{\times}10^{11}\ n_{eq}/cm^2$. Table 1.2 summarizes the requirements of the sensors equipping the innermost layer of the ILD vertex detector.

1.2.3 Power consumption considerations

In order to address the challenging issue of power consumption, two alternative readout strategies are being investigated based on the ILC time structure: continuous readout and delayed readout. In the former readout approach, the sensors are read out continuously and the hits are allocated to the time slot which coincides with the time needed to read all pixels (called frame readout time). The other strategy is the delayed readout, where the hits are stored in the sensors during the whole train duration and read out during the beam-less period separating two consecutive trains.

For the continuous readout approach, power consumption estimates were performed

at IPHC, based on fabricated sensors and accounting for power cycling. It was assumed that the beam time structure can be used to reduce the sensor power consumption during a large fraction of the inter-train time by about two orders of magnitude. It is also estimated that a transient time ($\lesssim$ 4 ms) is needed before and after the train to switch on and off all sensors in a well controlled way. With a rather conservative duty cycle of 2% (while the machine duty cycle is $\sim$ 0.5%), the average power consumption would amount to a few tens of watts only (e.g. about 10 W for CPS) [3]. Such values are compatible with modest cooling by air flow, which does not require introducing additional material in the VTX fiducial volume.

Power consumption may in principle even be more mitigated with the delayed readout approach, because it allows for a very low readout clock frequency. This approach has as an important consequence to avoid the effect of the Lorentz forces on the ladders generated by power cycling in the experimental magnetic filed. If the electronic signal is read out only after the end of the train, immunity against EMI may also be reinforced [3]. In order to compare and evaluate the potential and benefits of those two different readout architectures, they will be both developed in this thesis.

1.3 R&D on CMOS pixel sensors adapted to the ILC vertex detector

1.3.1 Principle of standard CMOS pixel sensors

The cross-section of a typical CPS device is illustrated in Figure 1.4. The active volume of the sensor is a lightly doped and undepleted epitaxial (EPI) layer. This layer is common in many modern CMOS processes featuring twin wells, where it is grown on a highly doped substrate. The doping level of the p-well is typically three orders of magnitude higher than the EPI layer, translating into potential barriers at the region boundaries. The substrate is also made of highly doped, crystalline silicon with a typical thickness of several hundreds of microns. Minimum ionizing particles (MIP) produce excess carriers in the EPI layer at a rate of $\sim$ 80 electron-hole pairs per micron. The thickness of the detecting volume is limited to $\sim$ 10-20 μm. Most of the signal charge electrons are reflected back to the EPI layer by the p-EPI/p++substrate and the p-well/p-EPI interface, while the electrons created in the substrate are quickly recombined.

The total signal charge of CPS amounts therefore to several hundred electron-hole

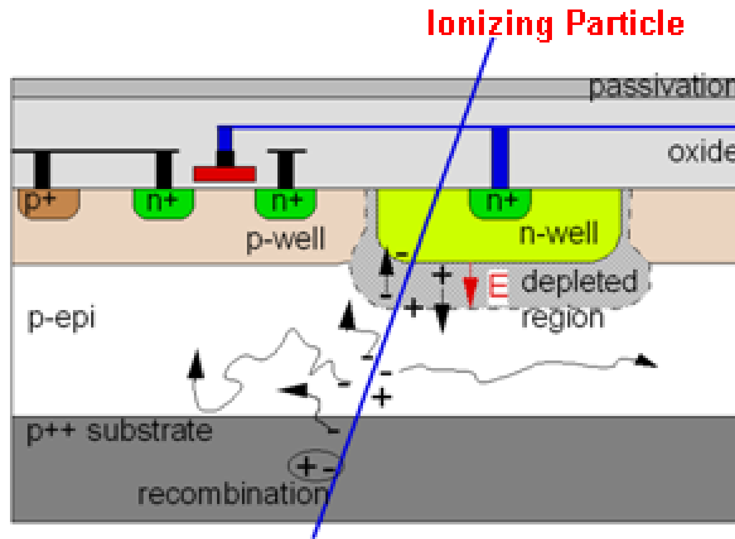


Figure 1.4: Schematic cross-section of a typical CMOS sensor.

pairs. Since the charge is shared between several neighboring pixels, the number of charge carriers collected in the seed pixel[1] is typically 20-50% of the total deposited charge, depending on the EPI layer resistivity, on its thickness and on the pixel pitch and sensing node dimensions.

CPS are a fully monolithic device, where the readout electronics is fully integrated with the sensors on a single chip. Each pixel in such a sensor contains a sensing diode accompanied by electronics needed for reading out the signal. This feature allows for a high chip integration, which alleviates the overall detector cost and allows for very compact systems.

1.3.2 Why considering CMOS pixel sensors for the ILC?

In the last years, several new sensors have been developed for the ILC, CPS for particle detectors being one of them. This technology has many advantages and potential for an application at the ILC as compared to Hybrid Pixel Sensors (HPS), today's most advanced technology [11]. The HPS are mainly built from two different chips: a sensor chip and a readout electronics chip bonded by a bulky metal bump [12], as shown in Figure 1.5. This metal bump is a source of complication, of multiple scattering and of granularity limitations.

[1]The seed pixel of a signal cluster is defined as the one collecting the largest fraction of the total cluster charge.

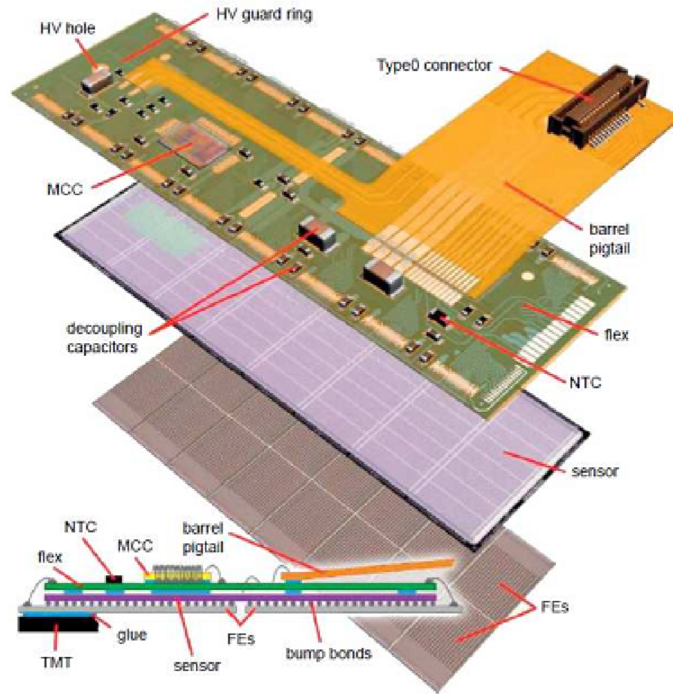


Figure 1.5: Sketch of the composition of a complete ATLAS module, including sensor and FE-chip connected by bump bonds, a hybrid kapton foil and the module control chip.

The ATLAS[2] pixel detector made of HPS is the innermost tracking system of the ATLAS experiment at the LHC. The spatial resolution measured with ATLAS modules (a pixel dimension of 50 μm $\times$ 400 μm) before irradiation is $\lesssim$ 10 μm along the 50 μm pixel pitch. The charge sharing is less effective in the orthogonal z-coordinate (400 μm pitch), where the spatial resolution is about 115 μm [13]. A full ATLAS module featuring a relatively large thickness consists of two bump-bonded slices of silicon and a module controller chip on the top. It translates into a material budget of about 1.5% Xo[3] [13]. As a consequence, HPS have been limited so far by the achievable material budget and poor granularity for the ILC vertex detector. On the other hand, CPS show a significant advantage over these two parameters, at the expense however of the readout speed and radiation tolerance, which are much less demanding at the ILC than at the LHC.

[2]The ATLAS acronym stands for A Toroidal Lhc ApparatuS, but it is also a reminder of the unprecedented size of this detector.

[3]Xo stands for the radiation length.

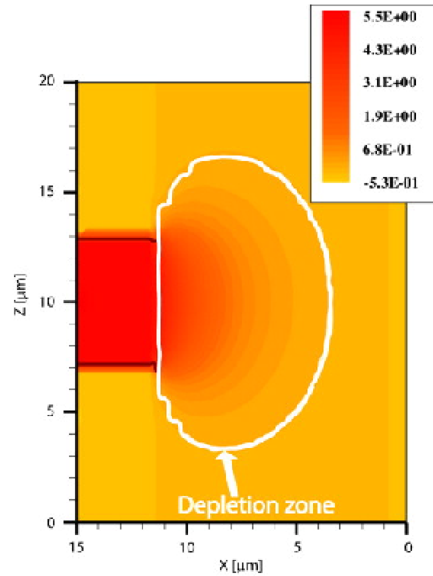


Figure 1.6: CPS based on a high resistivity EPI layer: potential [V] calculated using the ISE-TCAD package [14]. Reverse biasing of n-well/p-EPI junction at 5.5 V results in a depleted zone extending over several μm inside the sensitive volume.

1.3.3 Potential of CMOS pixel sensors

CMOS sensor technology has long been desired in many fields and being became mature. Their industrial manufacturing relies on procedures optimized for commercial items, which may be far from those needed for charged particle detection. With the rapid development of commercial processes, some remarkable progresses have been made in the right direction and the real potential of CPS has being approached.

1.3.3.1 Full charge collection by drift in a depleted EPI layer

Modern CMOS technologies are often built over very thin EPI layers (a few microns) to minimize noise coupling or crosstalk. The number of excess carriers produced by a MIP is proportional to the thickness of the EPI layer, and thus this thin EPI layer results in a very limited signal. This point is one of serious concern in traditional CPS.

The charge collection mechanism in the EPI layer can be another limiting aspect of the standard CMOS technologies, because the latter suffer from small and incomplete signal charge collected by thermal diffusion rather than by a drift. A promising way of improving this mechanism is to manufacture CPS with a high resistivity EPI layer, featuring an EPI layer which is at least partially depleted.

Due to the electric field existing in the depleted region, the charge collection is

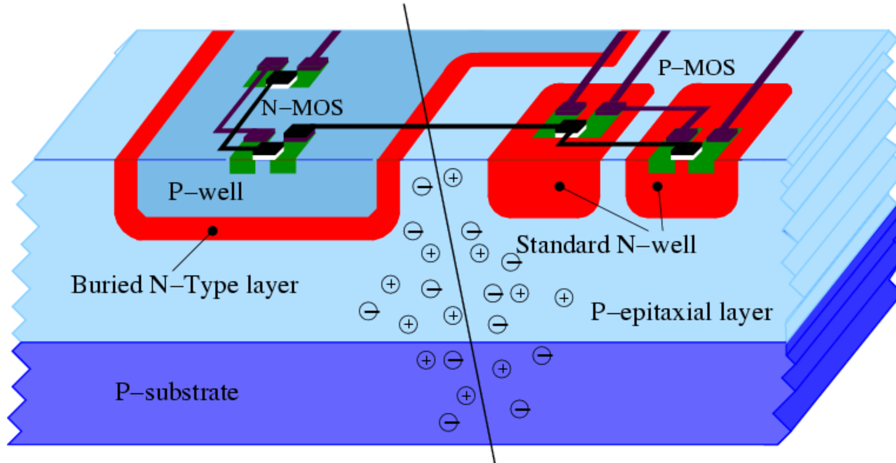


Figure 1.7: Schematic cross-section of a typical CMOS wafer with the deep n-well.

expected to be faster. The features of this kind of technology have been simulated by using ISE-TCAD [14]. The simulation results showed that the depleted zone inside an EPI layer had a significant extension, as shown in Figure 1.6. It therefore enhances the pixel SNR value and the sensor radiation tolerance with respect to the performance achieved with a low resistivity EPI layer.

In order to explore this kind of CMOS process, one of the prototype chips (called MIMOSA-25)[4] was fabricated in a commercially available XFAB-0.6 CMOS process, featuring a high resistivity EPI layer of ∼1k Ω·cm [15]. The test results of MIMOSA-25 showed that the charge collected in seed pixels is at least twice larger than that of the sensors with a low resistivity EPI layer, resulting into a high SNR of up to ∼ 50. A SNR of ∼ 35 has been achieved with chips exposed to a fluence of $\sim 3{\times}10^{13}\ n_{eq}/cm^2$. This is to be compared with the measurements performed with the MIMOSA-15 prototype, fabricated with a low resistivity EPI layer, which exhibited a SNR value as low as ∼ 15 after an exposure to a substantially smaller fluence of $\sim 0.2{\times}10^{13}\ n_{eq}/cm^2$ [15].

1.3.3.2 Full CMOS electronics in the active area

Deep n-well CMOS pixel sensors The implementation of CMOS circuitry in the active area is impractical for traditional CPS. In order to overcome this limitation, a deep n-well of a triple-well commercial CMOS process may be used as charge collecting

[4]MIMOSA stands for Minimum Ionizing particle MOS Active pixel sensors. More than a decade has past since MIMOSA-1 was designed as the first CMOS pixel sensor dedicated to charged particle tracking. Thirty-two different MIMOSA prototype chips have been designed and fabricated at IPHC since 1999.

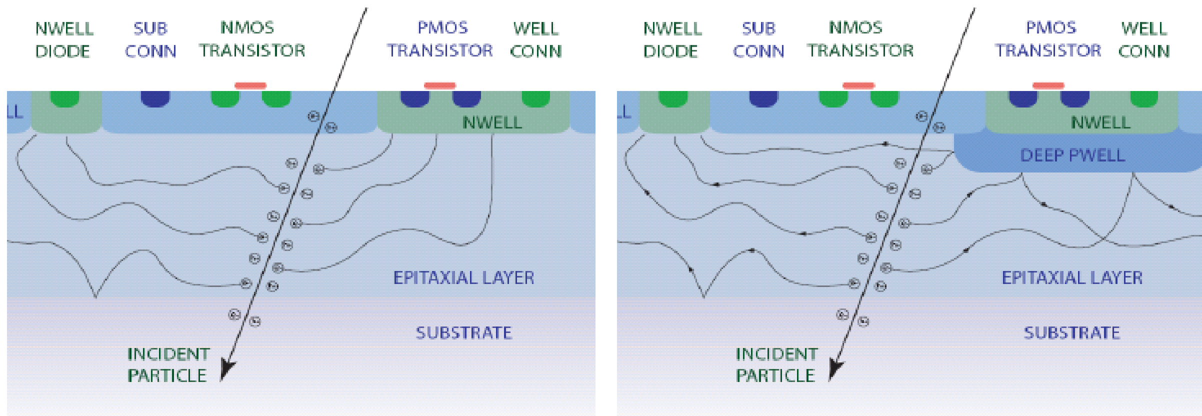


Figure 1.8: A CPS without a deep p-well implant (left) and with a deep p-well implant (right).

electrode, while the PMOS transistors are implemented in an n-well which is geometrically smaller and less deep than the charge collecting deep n-well. Figure 1.7 shows a concept of using a buried n-type layer as the charge collection diode. This approach may take full advantage of the properties of a CMOS technology, taking into account the limited area of PMOS transistors.

This approach was followed in [16]. Several prototype chips (called the APSEL series) have been designed and fabricated in the STMicroelectronics 130 nm CMOS technology. For the first "ILC-class" prototype (named SDR0 chip), a design of CMOS deep n-well sensors with a 25 μm pixel pitch provides a 5-bit time stamping[5], corresponding to a time resolution of $\sim$ 30 μs. Each pixel dissipates $\sim$ 5 μW static power. The limited charge collection efficiency is a main drawback of this deep n-well device, due to parasitic charge collection in the additional n-wells containing PMOS transistors. One of the prototype chips called APSEL4D has been characterized as an example. Beam test results of APSEL4D show that the hit detection efficiency could not be sufficient (up to 92% taking into account a reasonable $\sim$ 450 e^- threshold settings [16]). Therefore, this kind of the sensor still needs to demonstrate its ability to build a working detector, in particular when considering the performance of charge collection efficiency [17].

Deep p-well CMOS pixel sensors A new Jazz-Tower 0.18 μm CMOS technology with a quadruple-well (deep p-well) offers another opportunity of using PMOS transistors in the active area [18]. A deep p-well is introduced underneath the n-wells containing

[5] A time stamping is a sequence of characters, denoting the time at which a certain hit occurred. This data is usually presented in a consistent format, allowing for easy comparison of two different records and tracking progress over time.

the PMOS transistors, which isolates the n-wells from the EPI layer and prevents them from acting as the sensing diodes. This then ensures that all charge is being collected by the sensing diode and maximizes charge collection efficiency (nearly 100%) [19]. This is illustrated in Figure 1.8.

A prototyping sensor (called TPAC1.0 chip) designed by the CMOS sensor design group in Rutherford Appleton Laboratory has demonstrated its feasibility for nearly 100% collection efficiency [20]. The pixel of TPAC1.0 sensors has a pitch of 50 μm, it comprises a preamplifier, a shaper and a comparator. The static power consumption for each pixel is $\sim$ 12 μW.

Another design called “Chronopixel”[6] is also expected to implement a deep p-well over most of the pixel area in the near future. An important feature of this design is the possibility of putting a time stamping on each hit (up to two hits) with sufficient precision (i.e. a 14-bit time stamping) in a relatively small pixel. The second prototype will be designed for a 25 μm pixel with binary readout in TSMC 90 nm technology. This small pixel with 14-bit time stamping capability will be developed as a good candidate of the ILC vertex detectors, but this has to be demonstrated [21].

High voltage CMOS pixel sensors Still another approach was followed, using as a high voltage triple-well CMOS technology. The main motivation of this approach is to avoid relying on the limited number of CMOS processes featuring an adequate (thick, resistive) EPI layer. As a consequence, very deep sub-micron processes ($<$0.18 μm) can be used, which do almost never provide an EPI layer. This opens up the possibility of integrating a substantial amount of transistors in small pixels. A drawback is however that one needs using a high voltage option of the process used, and more power may be consumed. The novel sensor is based on two main ideas: the first idea is to use the deep n-well as the signal collection electrode. The second idea is to implement both types of transistors inside the deep n-well, which is also the substrate of PMOS transistors [22], as shown in Figure 1.9.

In order to verify the performance of high voltage CPS, one of the pixel sensors with a 21 μm pixel pitch was designed in a 0.35 μm high voltage CMOS technology. Test beam measurements have been performed. The measured MIP cluster signals are $\sim$ 2200 e^- , spatial resolution $\sim$ 7μm , SNR of 12.3 and detection efficiency more than 85% [23]. To test the radiation tolerance, several chips have been irradiated with neutrons up to $\sim 10^{14}$

[6] The design was developed by Sarnoff company, the detailed pixel circuits are not open to the public.

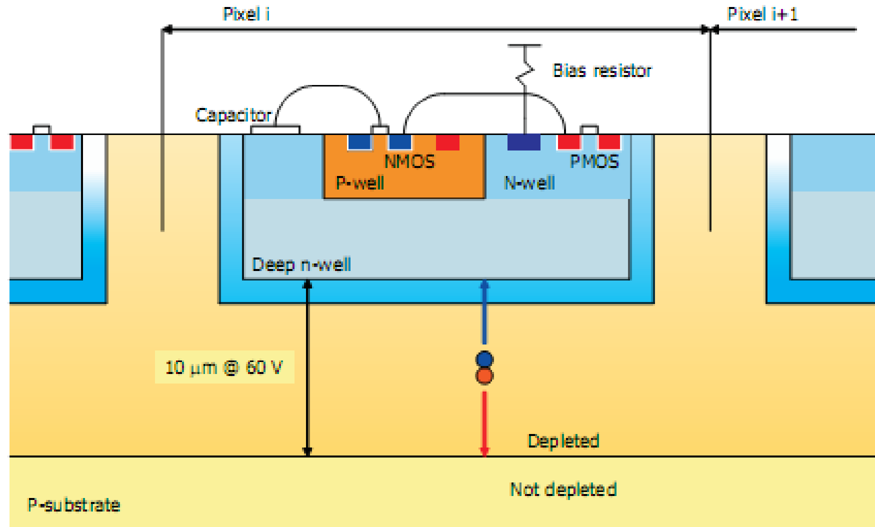


Figure 1.9: Schematic cross-section of a typical CMOS wafer in the high voltage technology.

n_{eq}/cm^2. Before irradiation the equivalent noise charge (ENC) was 70 e^- , immediately after irradiation 300 e^- and after three days of annealing at room temperature it went to 130 e^- . More R&D is still required to validate this technological approach, aiming in particular at better SNR and spatial resolution performance.

1.3.3.3 3D Integrated CMOS pixel sensors

3D integration is defined as the integration of thinned and bonded silicon integrated micro-circuits with vertical interconnects between the different layers. It is particularly suited to CPS, for it could integrate different CMOS manufacturing processes, each optimized for a given sequence of the charge generation and signal processing chain. In this case, vertical integration of two (or more) CMOS layers makes it possible to separate the analog front-end section from the digital readout section, with the widest advantages. The designs in this thesis therefore focus on the development of 3D integrated CPS. Their advantages will be discussed in more detail in chapter 3.

In order to demonstrate the feasibility of 3D-CPS for the ILC vertex detector, a 3D-chip named VIP1 has been designed by the Fermi Laboratory using the MIT Lincoln Laboratory 0.18 μm process [24]. The analog pixel including an analog front-end and the digital pixel including a 5-bit time stamping latch are vertically integrated within a 20 μm pitch. The test results showed that the VIP1 chip works with full functionality. However, the fabrication yield was very poor and it was concluded that such a 3D process is not optimal for mixed-mode signal circuitry that includes high precision and low noise

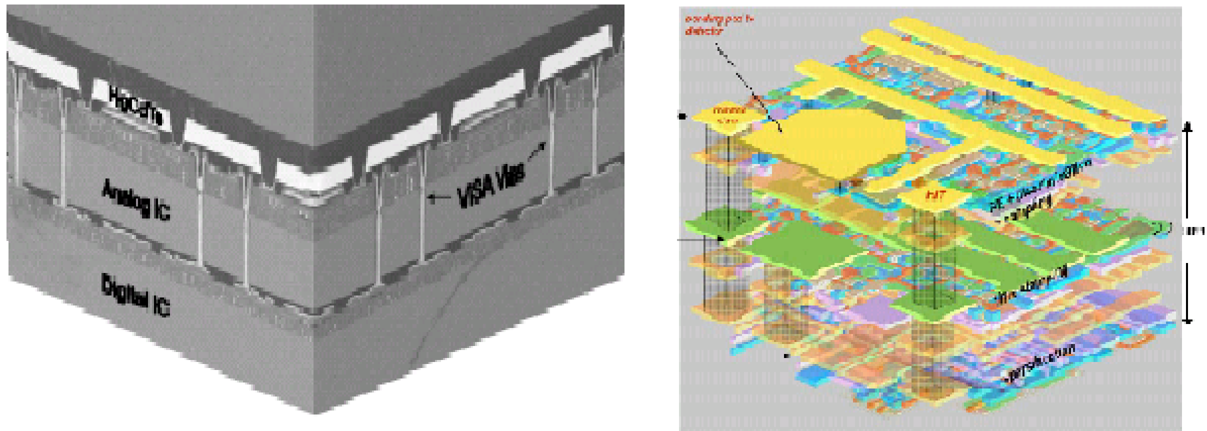


Figure 1.10: Sketch of the 3D-integration technique, integrating several electronic layers (left) and Fermi-Lab 3D design with 3 tiers for different electronic tasks (right).

parts [25].

After VIP1, the focus at Fermi Lab shifted to a commercial CMOS process (i.e. Chartered-3D Tezzaron technology, to be introduced in chapter 3) for possible higher yield. A 24 μm pitch 3D-CPS (called VIP2) has been developed with a 8-bit time stamping, corresponding to a time resolution of $\sim$ 4 μs. Each pixel dissipates $\sim$ 10 μW static operation power [26].

1.4 Conclusion

In order to fully exploit the advantageous running conditions of the ILC and achieve the high precision physics program it allows for, a vertex detector of unprecedented performance is mandatory.

Its specifications are governed by the spatial resolution (i.e. $< 3\ \mu m$) and the material budget (50 μm thin sensors, low power consumption), and compromise the read-out speed and the radiation tolerance to a certain extent. Hybrid Pixel Sensors, which are well established and widely used at the LHC, are thus not suited to this application. CPS are intrinsically significantly better adapted to it.

Several variants of CPS using 2D technologies have been developed so far for charged particle tracking. Despite the appealing results obtained, it is clear that their ultimate performance do not allow exploiting fully the real potential of the technology, mainly because the fabrication parameters are dictated by industrial interests featuring modest overlap with those of subatomic physics experiments. This reality hampers the possibility

of using 2D-CPS for the most demanding running conditions at the ILC such as those foreseen at its highest collision energy.

3D integration technologies seem to be the most promising way to turn around the limitations of 2D-CPS, since they allow combining different CMOS technologies in a single, stapled, multi-tier chip. Each tier can then be optimized for its dedicated functionalities. It is the main purpose of this thesis to explore this possibility using two different readout approaches.

Before exposing the work performed for this purpose, the thesis addresses the question of improving the 2D approach, which exploits the concept of double-sided ladder. The next chapter summarizes design developments realized to improve the signal-to-noise ratio of 2D-CPS.

Chapter 2

Offset compensated in-pixel amplifiers for CMOS pixel sensors

In the previous chapter, different types of CPS were presented, their essential advantages have been explained. The state of the art technology is an optimized 2D-CPS, based on a continuous readout (or called rolling shutter readout) [27]. It makes use of rolling shutter operation, in-pixel amplification, correlated double sampling (CDS) and column-level discrimination. MIMOSA-26 is the first full scale sensor based on this architecture. It was designed and fabricated in 2008. Based on its first performance assessment, a pixelated double-sided ladder equipped with MIMOSA-26 sensors has next been proposed to study the system integration aspects relevant for the ILD vertex detector (see section 2.1).

MIMOSA-26 was manufactured in a 0.35 μm technology, which was not supposed to be used for final sensors. This technology limits CPS to read out in a short integration time of $\sim$ a few μs . However, it is particularly needed to cope with the beam related a high beamstrahlung background, when the ILC will be running around 1 TeV collision energy. In order to realize this goal, many R & D on CPS are being exploited. Many advanced CMOS technologies with smaller feature sizes (e.g. 0.18 μm Jazz-Tower CMOS process) are expected to provide several improvements with respect to the aforementioned 0.35 μm CMOS technology, e.g.:

- Due to smaller parasitic capacitors of metal lines, the readout speed can be increased
- An enlarged number of metal layers is provided (e.g. 6-7 metal layers are available in a 0.18 μm Jazz-Tower CMOS technology)
- The total power consumption usually decreases with lower power supply voltage used in these processes

- Because of the thinner gate oxide, transistors will be less perturated by intense ionising radiation

- The higher degree of integration allows for increased in-pixel functionality implementation

In addition, the shrinking of the feature size of CMOS transistors is an obvious outcome of the evolution of microelectronics. This is exploited in the design of new pixel systems, where advanced functionalities can be implemented in each pixel to provide a higher SNR and to handle a higher hit rate. Therefore, this chapter is motivated by investigating a novel pixel structure, which was designed as a promising solution to the integration of high density circuitry in a small pixel. The proposed CPS were designed and fabricated in a 0.13 μm CMOS process. As compared to MIMOSA-26 pixel structure, a two-stage amplifier instead of a single-stage amplifier was designed for achieving a higher SNR. Even so, a 12 μm pixel pitch is $\sim$ 1.5 times smaller than that of MIMOSA-26 sensors, the proposed CPS may be considered for very small pixel pitch in the inner layers of future vertex detectors.

This chapter is organized as follows: section 2.1 provides an introduction to a pixelated double-sided ladder based on MIMOSA-26 sensors. Section 2.2 introduces the pixel design of MIMOSA-26. In section 2.3, we discuss the main noise sources in CPS. In order to improve the SNR, we proposed a new pixel structure with noise reduction and multi-stage amplification techniques. Section 2.5 covers the aspects of designing and characterizing such a novel CPS.

2.1 Ultra-light pixelated ladders for an ILC vertex detector

The large energy of beam bunches causes a large background of e+ e- pairs produced by beamstrahlung radiation. It forces to build a light weight, high precision inner detector system in order to accurately measure prosperities. A reduction of the detector thickness is highly desirable because it minimizes the amount of multiple scattering experienced by traversing particles. A mechanical support structure of the sensor and electrical cables will add extra material, the system integration is therefore a crucial issue. Although MIMOSA-26 has already shown very promising performance as a single sensor, the con-

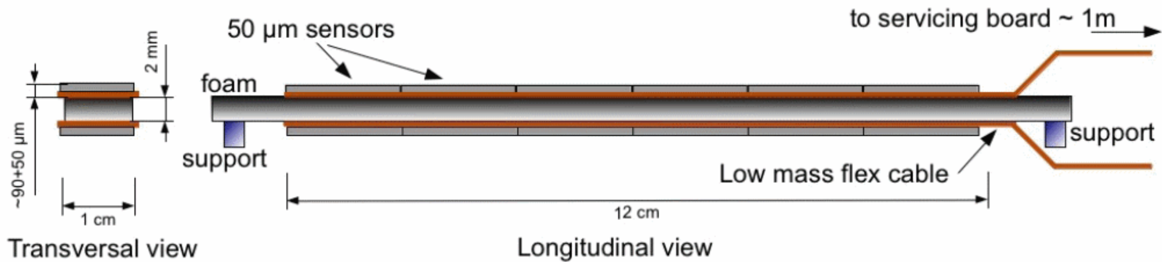


Figure 2.1: Design of the exploratory ladder of the PLUME project.

struction of a functional full vertex detector equipped with a large number of sensors is another challenge.

The PLUME [1] collaboration aims to prototype an ultra-light detector for matching the geometry required by the inner layer of the ILD vertex detector, as described in chapter 1. This collaboration gathers four laboratories [2] to design, fabricate and evaluate the prototypes of the double-sided pixellated ladder. It features a sensitive length of 12.5 cm, a thickness of 2 mm and a material budget around 0.3% of X_o, as a proof of principle for the ILC Detector Baseline Document [28]. The ladder design follows an approach: two flex cables are glued on each side of a support, made of low density silicon carbide foam, as shown in Figure 2.1.

According to the initial assumption of the ladder architecture, the requirements of the ILD vertex detector should be reached. As a first step, the goal of the PLUME project is to construct the double-sided ladder equipped with 6 MIMOSA-26 sensors on each side and to assess their performance. Six MIMOSA-26 sensors with total area of $\sim 12 \times 1$ cm^2 are butted together and glued on the kapton-metal flex cable, on which they are wire bonded. The latter is connected to a servicing board located $\sim$ 1 m away. Before describing the double-sided pixelated ladder, the overall performance of MIMOSA-26 is presented in the following subsection.

2.1.1 Full-scale sensor with binary readout architecture

MIMOSA-26 (see Figure 2.2) is the first full-scale sensor with binary output architecture realized for charged particle tracking. The pixel matrix consists of 1152 columns and 576 rows. Each pixel, featuring a pitch of 18.4 μm, incorporates a diode, an amplifier with CDS and a source follower (SF). The rolling shutter mode, used to read it out, is

[1]Standing for Pixelated Ladder with Ultra-Low Material Embedding
[2]DESY-Hamburg, IPHC-Strasbourg, Universities of Bristol and Oxford

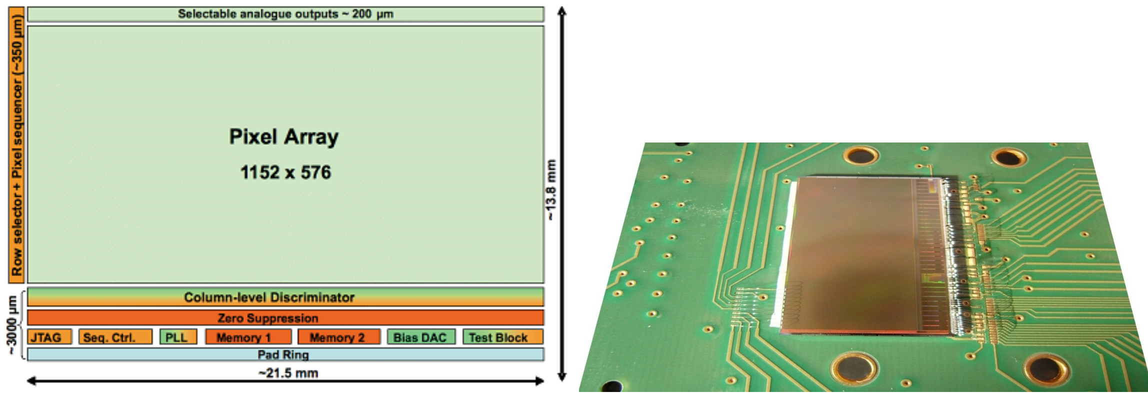


Figure 2.2: Schematic view of MIMOSA-26 displaying the different functional blocks (left) and photograph of the MIMOSA-26 sensor mounted on its interface board (right).

steered through a row selector located on the left side of the pixel matrix. All 576 rows in a column are multiplexed onto a discriminator at end of the column, all 1152 discriminators are read out in parallel. The total active area of the chip is $\sim 224\ mm^2$, the whole pixel matrix is read out in $\sim 100\ \mu$s, and the average power dissipation is ~ 280 mW$/cm^2$ [27].

The discriminated signals are processed by a zero-suppressing[3] readout circuit at the periphery of the matrix. In order to reduce the discriminator offset dispersion, the sensor was subdivided into 4 groups of 288 columns. The distribution of noise over a quarter of the pixel array (288 columns) with its associated discriminators is shown in Figure 2.3.

The total temporal noise[4] of the pixel array associated with discriminators is in the range 0.6-0.7 mV, corresponding to about the equivalent noise charge (ENC)[5] of 12 e^- . The total fixed pattern noise (FPN), caused mainly by the dispersion of discriminator thresholds, is about 0.3-0.4 mV, corresponding to about the ENC of 6 e^- .

Six MIMOSA-26 sensors have been assembled as a beam telescope and characterized with 120 GeV/c pion beams at the CERN-SPS. The detection efficiency in case of a low resistivity EPI layer is $\sim 99.5\pm0.1\%$ up to a threshold value of discriminators ~ 4 mV,

[3] Zero suppression is the removal of zeros from all outputs of discriminators. This can be done for data compression.

[4] The predominant components of electronic noise are divided into two categories: temporal noise and FPN. The latter, also called non-uniformity noise, is due to the spatial variation of output values consecutive to the mismatches of devices. The temporal noise refers to the time-dependent fluctuations; it is primarily due to the diode shot noise, and to the amplifier thermal and flicker noise. The specific impact of these noise sources of pixels will be analyzed in subsection 2.3.

[5] The total temporal noise is usually equivalent to noise charge of pixels; the ENC of 12 e^- includes the pixel temporal noise and that of column-level discriminators.

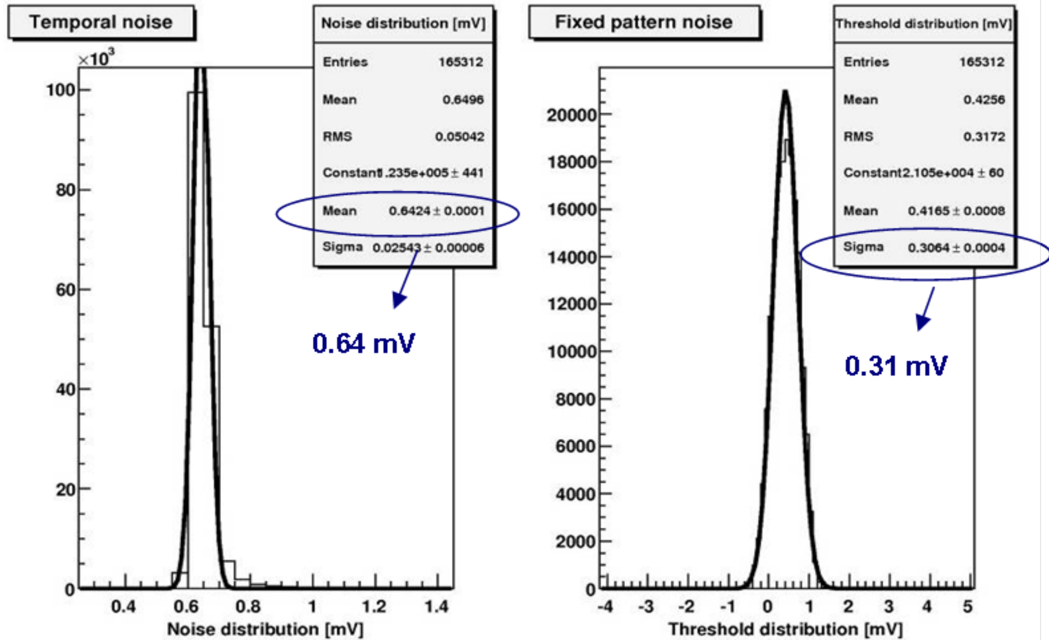


Figure 2.3: MIMOSA-26 noise distributions over a quarter of the sensitive surface (group of 288 columns) as measured at a 80 MHz clock frequency: temporal noise (left) and FPN (right).

corresponding to ∼6 times the noise standard deviation, with a fake rate[6] below 10^{-4}. A spatial resolution close to 3.5 μm was observed with a low resistivity EPI layer [29].

The MIMOSA-26 sensor is a starting point for the development of future micro-vertex detectors. It has reached the necessary prototyping maturity for real scale applications, including the innermost layer of the ILD vertex detector.

2.1.2 PLUME ladder concept

As mentioned above, the main feature of the PLUME ladder concept is a double-sided layout, which consists of two sensor layers separated by a support structure [30]. In this double-sided ladder, the same traversing particle generates a hit information on both sides of the ladder. As illustrated on Figure 2.4, the concept may be used to equip the ladder with different sensors on each side, one providing a high spatial resolution and one optimized for a high readout speed:

- One side can be equipped with squared pixels of 16-17 μm pitch providing a high spatial resolution of < 3 μm. The minimum integration time of MIMOSA-26 sensors

[6] The fake hit rate is defined as the probability for one pixel in one event to deliver a noise fluctuation above the discriminator threshold.

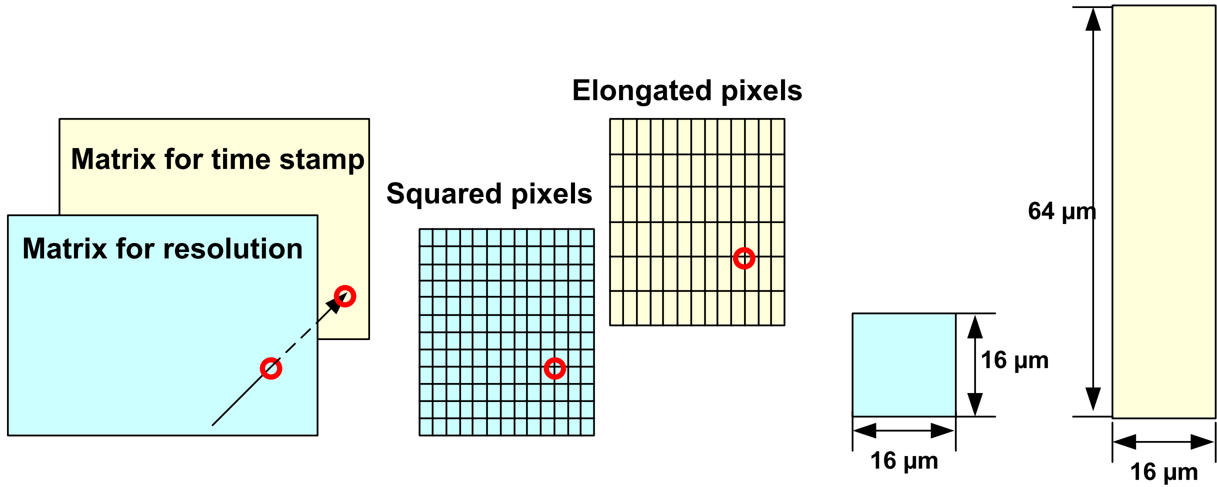


Figure 2.4: The placement of squared and elongated pixels equipped on a double-sided layer (left), and the pitches required for both squared and elongated pixels (right).

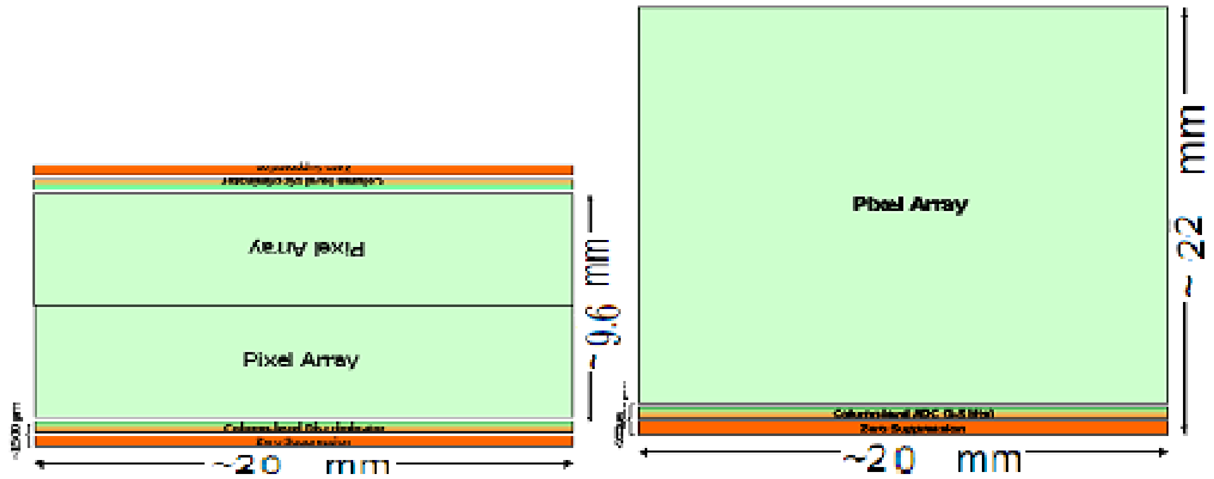


Figure 2.5: The double-sided readout architecture derived from MIMOSA-26 is to equip in the innermost layer (left), and the extension of MIMOSA-26 prepared for the outer layer (right).

is $\sim 100\ \mu$s . Based on the double-sided readout (i.e. the columns of MIMOSA-26 are split in halves and are read out in parallel on each side, as shown in Figure 2.5), the frame readout time would be reduced by a factor of ~ 2. Further improvements down to $\lesssim 40\ \mu$s are expected by moving to a new CMOS technology with smaller feature size 0.18 μm.

- On the other side, the pixels will be elongated in the column direction. The pitch will be increased by a factor of 4-5 with respect to the square pixel[7]. With the same sensitive area as the former side, the integration time can be improved to $\lesssim$

[7]The elongated pixel pitch is 16 μm $\times$ 64 μm or 16 μm $\times$ 80 μm.

10 μs due to the reduction of the number of rows in the readout direction. As a consequence of the increased sensing diode spacing, the spatial resolution will be 6-7 μm in both directions with staggered diodes.

2.2 Topology and analysis of MIMOSA-26 pixels

2.2.1 MIMOSA-26 pixel architecture

2.2.1.1 In-pixel amplifier used in MIMOSA-26

An all-NMOS in-pixel amplifier was implemented in MIMOSA-26. Its schematic and the operation timing waveform are shown in Figure 2.6. Each pixel contains a diode, an in-pixel amplifier with CDS and a source follower (SF) with a select switch Sel. The SF transistor in conjunction with the column bias current source acts as a buffer, which reproduces the sense node voltage on the column line. This SF buffer is only active, when the Sel signal is the logical one. The signal from two successive frames is extracted by the clamping technique. A second double sampling is implemented to remove the pixel-to-pixel offsets in each discriminator stage [31]. Operation of this double sampling is controlled by clock phases $Read$ and $Calib$, which memorize the pixel output signal and the reference level, respectively.

All pixels of a row receive the common signals Sel and $Clamp$, which are generated by the row decoder. Since the column-level buffer and discriminator are shared among all pixels of a column, the pixels of only one row can be active at a time. A solution respecting this criterion is the rolling shutter timing scheme, in which the control signals are row-wise staggered. The described row operation sequence is repeated row by row,

Table 2.1: The explanation of main control signals for the MIMOSA-26 pixel.

Sel	pixel power control signal
Clamp	clamping control signal
I_b	biasing current for driving a parasitic capacitor at each column
Read, Calib	control signals for storing the pixel outputs
Vdc	analog biasing voltage
Vdd	analog power supply voltage

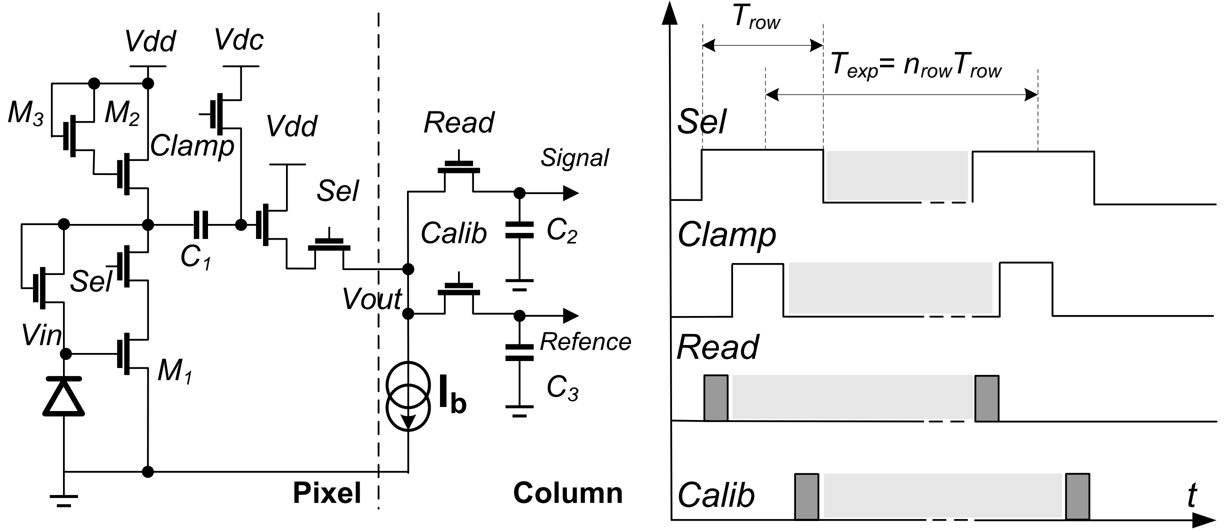


Figure 2.6: Schematic of the pixel amplifier in MIMOSA-26, followed by the parasitic capacitors at the end of each column (left) and the timing diagram of the rolling shutter operation (right). The main control signals are listed in Table 2.1.

the integration time (T_{row}) is the time of selecting sequentially the whole pixel array from top to bottom.

The performance of in-pixel amplifiers plus column-level discriminators was first validated in a prototype, called MIMOSA-22. A special biasing with a transistor M_3 for the load transistor M_2 has been introduced to increase the gain of this amplifier. The AC gain of improved amplifier is increased by about a factor of 2, and the DC operation points and its gain are almost not changed. Negative feedback makes the circuits more resistant to CMOS process variation, it can also be used to stabilize the operation point of the amplifier [32].

2.2.1.2 Calibration procedure

In order to study the electronics properties of CPS, e.g. charge-to-voltage conversion factor (CVF), charge collection efficiency (CCE) and noise performance, a calibration procedure needs to be done by using a X-Ray Fe^{55} source. This source delivers photons with two emission energies: K_{α}=5.9 keV (24.4 % emission probability) and K_{β}=6.5 keV (2.8 % emission probability). The calibration procedure is accomplished by comparing the ADC units translated into the associated electrons. An example of such a distribution of signals from single pixels is shown in Figure 2.7. Three peaks are visible in the typical Fe^{55} spectrum.

The first peak at low values is usually interpreted as a result of the hits outside the

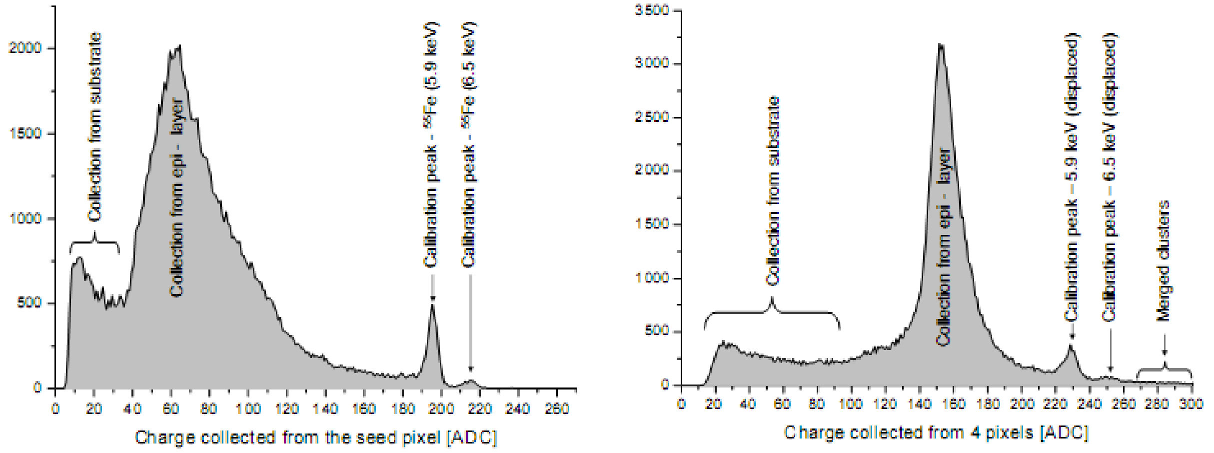


Figure 2.7: Response to a Fe^{55} 5.9-keV X-ray source, the peaks correspond to photons interacting in the thin depleted region under n-well (left) and the corresponding spectrum for signals summed in a 2×2 cluster (right).

EPI layer. This interpretation is probably incomplete, as the hits in the EPI layer close to a sensing diode also contribute to its low high energy part. The second peak is called "charge collection peak", which corresponds to the charge collected from hits occurring inside the EPI layer but outside of depleted zone of the sensing diode, due to a thermal diffusion. The distribution exhibits a small peak, the charge liberated in silicon by a 5.9 keV photon, which amounts to $\sim$ 1640 e^- (an electron-hole pair needs a deposited energy of $\sim$ 3.6 eV). This peak is called "calibration peak", it corresponds to a hit into the depleted zone of the sensing diode. A measurement with a high statistics shows a smaller second peak at a signal level above the calibration peak. This peak corresponds to the interaction of photons of the less intensive 6.5 keV K_β radiation. These calibration peaks are usually used as an absolute reference for estimation of CVF and ENC, they can be given by:

$$CVF = \frac{U_{calib} \cdot G}{1640e^-} \tag{2.1}$$

$$ENC = \frac{U_{noise} \cdot 1640e^-}{U_{calib}} \tag{2.2}$$

where U_{calib} and U_{noise} represent the position of the calibration peak and noise peak in ADC units, respectively. G represents the conversion gain[8].

[8]The output signals are usually given in ADC counts of a 12-bit ADC mounted on the test board, where analog output signals of pixels can be translated into 12 digital outputs.

Table 2.2: Charge collection efficiency for the seed pixel, and for 2x2 and 3x3 pixel clusters using a Fe^{55} source (analog output at the clock frequency of 20 MHz).

EPI layer	EPI thickness	seed	2×2	3×3
standard(10$\Omega.cm$)	14μm	21%	54%	71%
high resistivity(400$\Omega.cm$)	10μm	36%	85%	95%
	15μm	31%	78%	91%
	20μm	22%	57%	76%

The CCE is defined as the ratio of the total charge collection peak to the calibration peak.

$$CCE = \frac{U_{charge}}{U_{calib}} \tag{2.3}$$

where U_{charge} represents the position of the charge collection peak in ADC units.

2.2.1.3 Characterization of MIMOSA-26 sensors

In the laboratory, the measured ENC of MIMOSA-26 sensors with a low resistivity EPI layer is 12-13 e^- and the CVF is $\sim$ 74 μV/e^- at a clock frequency of 80 MHz (the integration time of the sensor is $\sim$ 115 μs) and at an operation temperature of about 20 °C. The charge collection efficiency was also measured. It reached a value of $\sim$ 21% for the seed pixel and of $\sim$ 71% for a small matrix of 3×3 pixels [32].

In order to study the performance of MIMOSA-26 sensors with a high resistivity EPI layer, MIMOSA-26 sensors have been refabricated in 0.35 μm technology with a high resistivity ($\sim$ 400 $\Omega.cm$)[9] EPI layer. They were fabricated on three different wafers featuring the EPI layer thickness of 10, 15 and 20 μm respectively. A comparison of CCE between them has also been listed in Table 2.2 [33]. One observation is that the CCE decreases with increasing thickness of the active volume. Since the average diffusion path of the signal electrons increases, the probability of losing charge carriers also increases by recombination. From the beam tests, the maximum SNR is found for the sensors with the EPI layer thickness of 15 μm . It proves that an optimum SNR needs to not only

[9] 400 $\Omega.cm$ is a lower limit, meanwhile, we learned that the most likely value is $\sim$ 1 k$\Omega.cm$

keep a good CCE but also generate a sizable signal charge in a sufficiently thick EPI layer [34].

2.3 Noise sources in CMOS pixel sensors

CPS suffer from noise of various natures that affect the system at different stages. The most important noise sources to be controlled in CPS are the leakage current shot noise of the sensing element [35], electronic noise of circuits used for the chip-level and board-level signal processing, and possibly also quantization noise (if the system has a digitized output).

2.3.1 Leakage current related shot noise

Semiconductor devices suffer generally from charge leakage by thermal generation and recombination processes. The mechanism of charge leakage is an indirect generation-recombination via energy states in the semiconductor band [36]. The leakage current of a depleted semiconductor volume depends on the density of certain impurities in the semiconductor and can be expressed as a carrier lifetime. Leakage current related shot noise exhibits an exponential increase with temperature and radiation level. It is a growing function of exposure time and is given by (2.4), it is also shown that the number of generated charge carriers in a defined time interval follows a Poisson distribution.

$$q_{n,leak} = q\sqrt{n_{leak}} = \sqrt{q \cdot i_{leak} \cdot t_{leak}} \tag{2.4}$$

where $q_{n,leak}$ is the root mean square (RMS)[10] noise charge due to leakage shot noise, n_{leak} is the mean number of thermally generated charge carriers over a time period t_{leak}, i_{leak} is the leakage current, and q is the elementary charge.

Leakage current related shot noise theoretically affects every reverse-biased PN junction of diodes of CPS. The only shot noise components having an important impact originate from the sensing diodes. For this reason, process technologies for semiconductor pixel sensors are highly optimized for low sensing device leakage.

[10]The RMS value of a set of values (or a continuous-time waveform) is the square root of the arithmetic mean (average) of the squares of the original values.

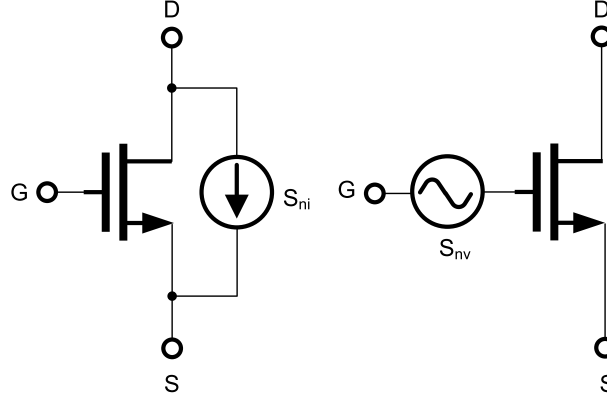


Figure 2.8: Modeling of noise in an NMOS transistor as a drain-source current (left) or a gate voltage (right).

2.3.2 Thermal noise

Thermal noise is the electronic noise generated by the thermal agitation of charge carriers inside an electrical conductor, which happens regardless of any applied voltage. Thermal noise in an idealized resistor is approximately white, meaning that the power spectral density is nearly constant throughout the frequency spectrum. Thermal noise is also generated in the channels of MOS transistors. The expressions (2.5) and (2.6) are given respectively for thermal noise power spectral densities $S^2_{thermal}$ of a drain-source parallel noise current source and of a noise voltage source in series with the gate connection of the MOS transistor [37], as illustrated in Figure 2.8.

$$Drain - source : S^2_{thermal} = 4kT\gamma g_m \tag{2.5}$$

$$Gate - voltage : S^2_{thermal} = \frac{4kT\gamma}{g_m} \tag{2.6}$$

where g_m is the transconductance of the MOS transistor, γ is thermal excess noise factor[11]. T is the absolute temperature, k is the Boltzmann constant.

[11] The factor γ is used for modeling of excess noise. The most important difference between the expressions for thermal noise in resistors and MOS transistor channels is this factor: the theoretical analysis mentioned above suggests a value of γ=2n/3 in the case of strongly inverted and saturated transistors, of γ=n/2 for weakly inverted and saturated transistors, and of γ=n for transistors in triode region independently of their inversion state. In these expression, n is the slope factor of the transistor, which is usually close to unity.

2.3.3 Flicker noise

The mechanism of flicker noise (1/f noise) is the trapping and release of charge carries at the semiconductor-oxide interface, which results in a fluctuation of the number of mobile electrons in the channel [38]. Flicker noise is modeled as a noise source in series with the transistor gate connection. The most common quantitative expression of the flicker noise gate voltage power spectral density, is given by the following expression.

$$S_{flicker}^2 = \frac{K}{C_{ox}WLf} \tag{2.7}$$

where f is the frequency, K is the flicker noise constant for a given process technology and transistor type, W is the gate width, L is the gate length and C_{ox} is the gate oxide area density.

According to the expression of (2.7) and to the theory of interface state trapping, flicker noise is independent of the gate-source voltage and transconductance. It depends on the process technology and channel carrier type. Generally speaking, p-channel transistors often have lower flicker noise and stronger gate-source voltage dependence than their n-channel counterparts. This could be explained that a p-type threshold adjusting implant used in the channel region of p-channel transistors. Moreover, this shallow implant also results in moving channel location where trap density is high due to surface defects, the semiconductor is depleted and the trapping and release probability is relatively low.

A particular case of flicker noise is random telegraph signal (RTS) noise. This low frequency noise is very important for analog designs in advanced CMOS technologies. As device dimensions shrink, the low frequency noise increases, and RTS noise is more likely to be observed with transistors of small gate geometry. The origin of RTS noise is attributed to the random trapping and release process involving one single trap state. Compared to other noise sources, the impact of RTS noise shows a larger statistical spread between the samples of a group of transistors of identical design and operating point. The frequency dependence of RTS noise significantly deviates from exact 1/f behavior and is possibly subject to transistor-to-transistor variation [39].

2.3.4 Board-level noise

The ENC for the entire system is easily obtained from the measurement of the output noise. Note that this determination of ENC fully relies on measured data. Thanks to

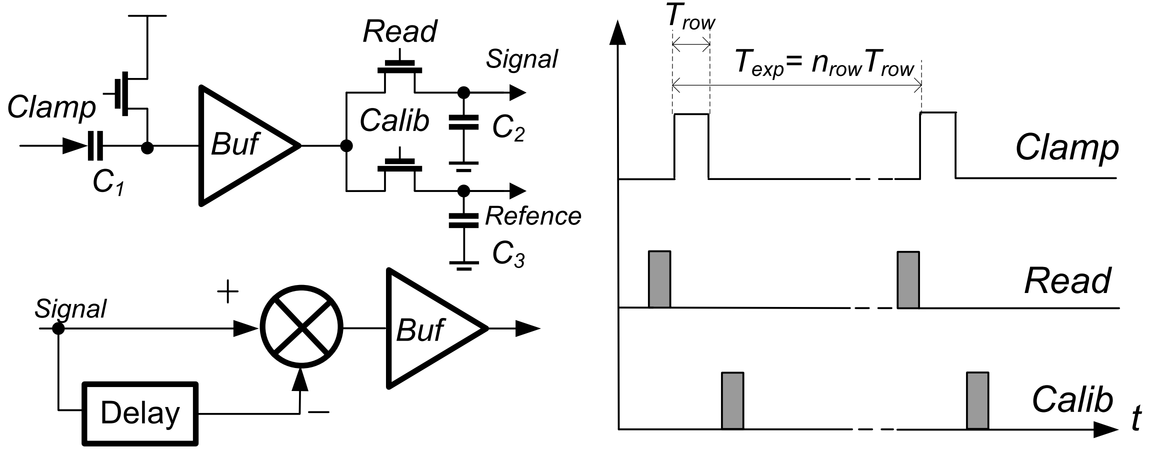


Figure 2.9: The simple example of realizing a CDS circuit and its model of the clamping technique as a filter, consisted of a delay cell and a subtracter (left) and the row timing (T_{row}) of relevant signals (right), T_{exp} is an integration time of the sensor, and n_{row} is the number of the rows.

the use of high resolution board-level ADCs, an ideal ADC's quantization noise (QN) is given by

$$QN = \frac{LSB}{\sqrt{12}} \tag{2.8}$$

where LSB is the least significant bit of an ADC. The noise of board-level electronics should be negligible with respect to the noise of the pixel.

2.3.5 Fixed pattern noise

Mismatches of the leakage current of diodes tend to create FPN. Another important factor affecting FPN is the mismatch in multi-signal paths based on the row-wise readout operation in CPS. FPN can generally be eliminated by specified technique, e.g. CDS [40].

2.3.6 Correlated double sampling technique

CDS is a technique for measuring electrical values that allow for removal of an undesired offset. It is used quite frequently when measuring sensor outputs [41]. The practical realization of the CDS circuit inside a pixel and an equivalent model are shown in Figure 2.9. The CDS technique also reduces low-frequency noise (e.g. flicker noise) because the noise components varying more slowly than the sampling time difference are suppressed by the subtraction operation between $Read$ and $Calib$ phases. The CDS suppresses any DC components and offset voltages affecting the signal up to the column-parallel circuit. The baseband transfer function $H_{cds}(f)$ is defined in the z-transform

representing the CDS operation. The amplitude of this baseband transfer function is periodic with a period of $1/T_{cds}$ and the periodically extended representation of $|H_{cds}|$ is given by(2.9).

$$|H_{cds}(f)| = |2sin(\pi f T_{cds})| \quad (2.9)$$

2.4 Multi-stage in-pixel amplifiers with the CDS circuitry

A high spatial resolution depends not only upon the pixel pitch but also on the SNR of the pixel. The latter depends on the size of diodes, the gain of amplifiers and the thickness of the EPI layer, etc. The SNR of the pixel should be as high as possible to suppress the noise of readout circuits at the column level for a simple reason that signal amplification reduces the impact of noise sources, located in the signal chain after the amplification stage.

Although a single-stage amplifier with a CDS circuitry has been implemented successfully in MIMOSA-26, the gain of a single-stage amplifier may be inadequate, it have led to the use of multi-stage amplification. In order to increase the gain of pixel with a low noise figure, the offset cancellation methods based on input offset storage (IOS) and output offset storage (OOS) are implemented in the multi-stage amplifiers, which are described in the following subsections [42].

2.4.1 Multi-stage amplifiers with input offset cancellation

Figure 2.10 illustrates the application of the input offset storage (IOS) technique in the pixel readout chain, which is composed of a sensing diode, a multi-stage cascade amplifier, an offset storage capacitor (C_1) and a source follower. C_p is the parasitic capacitance at the sensing node, which includes the input capacitance of the preamplifier, the parasitic capacitance at the drain of the transistor and the capacitance of metal interconnections.

The in-pixel amplifier amplifies its input signal in normal operation, while the Sel signal is active. During the offset sampling phase, the switch S_1 turns on, resetting the input and closing a unity gain loop around the preamplifier. In this situation its input voltage,

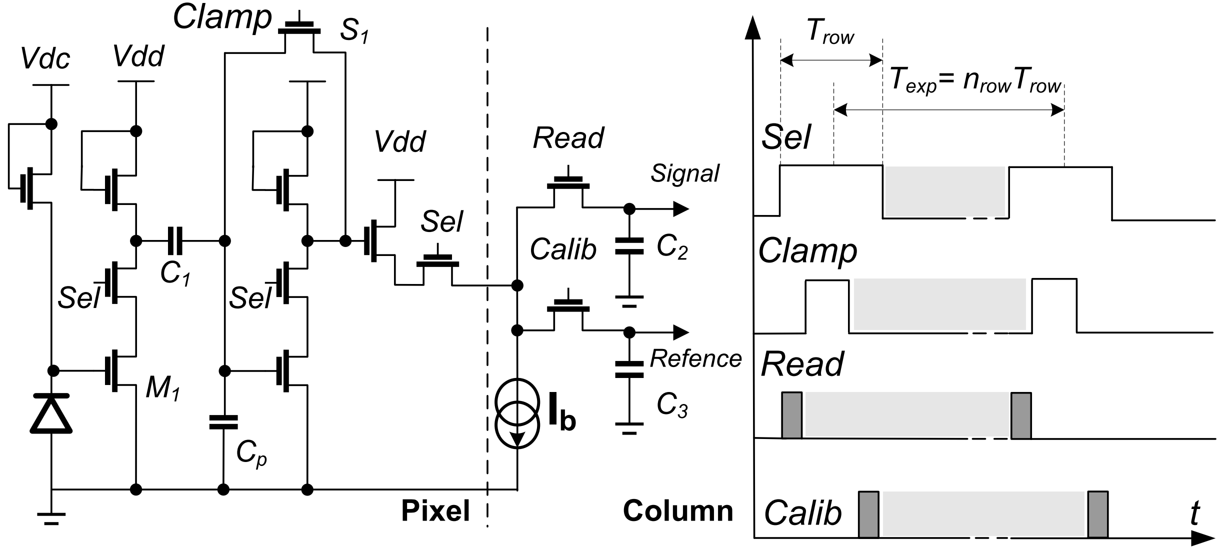


Figure 2.10: In-pixel amplifier with input offset storage technique (left) and the timing diagram of the working operation (right).

$$V_a = \frac{G_0 V_{osa}}{1 + G_0} \tag{2.10}$$

where G_0 is the DC gain of the preamplifier, V_{osa} is its offset voltage. When this switch is turned off, the charges in its conducting channel are released and removed through the MOS source and drain terminals. In this way, when the transistor S_1 opens, a certain amount of charge Δq is injected into the capacitor C_1.

The offset voltage of the source follower, V_{sf}, is not canceled by this technique. To refer it to the input, in addition to the preamplifier gain one must also consider the attenuation introduced by the capacitive divider formed by C_1 and C_p. Thus, the introduction of offset storage capacitors actually increases the contribution of V_{sf}. The total residual offset is

$$V_{os} = (1 + \frac{C_p}{C_1})(\frac{V_{osa}}{1 + G_0} + \frac{V_{sf}}{G_0}) + \frac{\Delta q}{C_1} \tag{2.11}$$

This offset voltage can be minimized by enlarging the gain of the preamplifier, i.e. G_0, but this reduces its settling speed. Normally, the in-pixel amplifiers are simple common source amplifiers, having a G_0 of $\sim$5.

2.4.2 Multi-stage amplifiers with output offset cancellation

Figure 2.11 illustrates the application of the output offset storage (OOS) technique. The offset sampling phase is when switch S_1 and S_2 turn on, a zero DC voltage connects

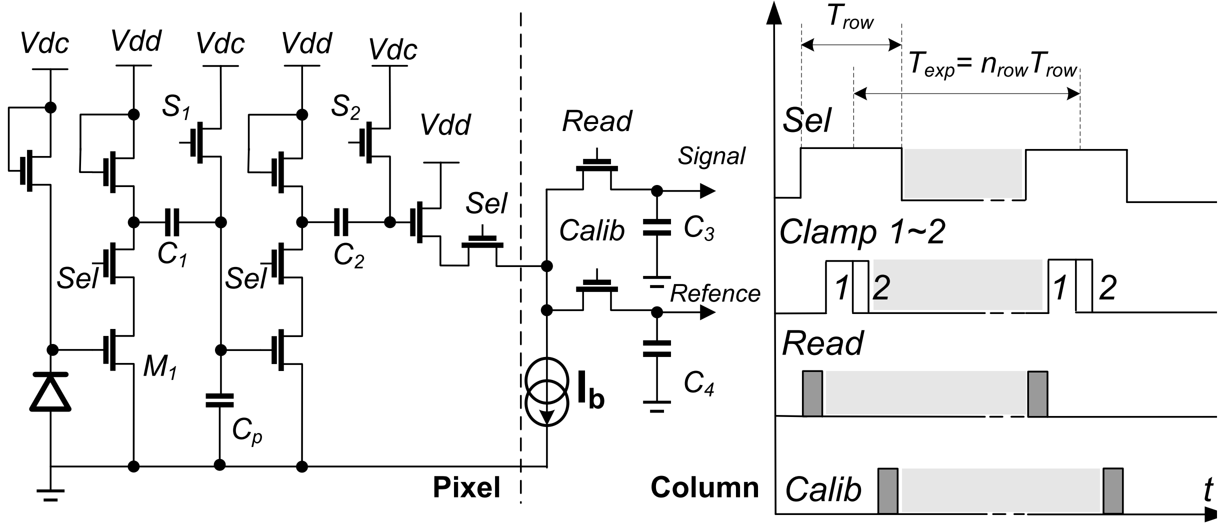


Figure 2.11: In-pixel amplifier with output offset storage technique (left) and its timing diagram of the working operation (right).

at the inputs of the preamplifier and of the source follower. The preamplifier amplifies its own offset voltage, which is stored on the capacitors. This eliminates the contribution from V_{osa} to the residual offset, because the fixed DC voltage at the preamplifier input yields a stable input voltage for the source follower.

When S_1 and S_2 open, their mismatches produce Δq in the charges and inject into the capacitors, therefore disturbing the sampled value. V_{sf} is not stored in the capacitors, and thus it is not canceled by this technique. The residual offset is

$$V_{os} = (1 + \frac{C_p}{C_1})(\frac{V_{sf}}{G_0} + \frac{\Delta q}{G_0 C_1}) \tag{2.12}$$

For the same G_0, the offset voltage is smaller than the one obtained using IOS. Note that the charge injection mismatch is now divided by G_0, because the capacitors are after the preamplifier. Once again the residual offset voltage is minimized by increasing G_0. However, in addition to reducing the operating speed, a high G_0 causes the preamplifier to saturate. When it exceeds the maximum output voltage swing, the offset voltage would not be correctly stored in this case. Thus, usually $G_0 < 10$. Having a large C_1 is desirable to reduce the attenuation introduced by the capacitive divider, and the effect of charge injection mismatches. However, it limits the settling speed of the preamplifier in the offset sampling phase.

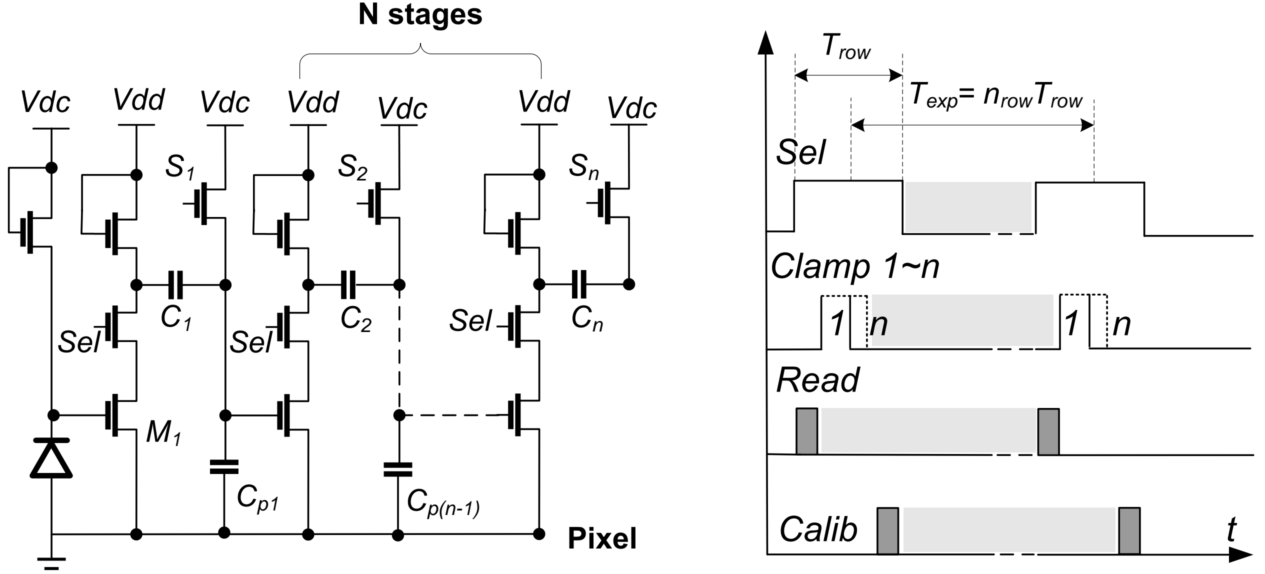


Figure 2.12: In-pixel amplifier with multi-stage output offset storage technique (left) and its timing diagram of the working operation (right).

2.4.3 Multi-stage amplifiers with hybrid offset cancellations

Figure 2.12 shows a cascaded preamplifier using OOS, preceding a latch circuit. As the case of the single stage amplifier, such a multi-stage amplifier can be implemented in the pixel-level discriminators and pixel-level ADCs, which will be described in chapter 4 and chapter 5 respectively. The offset voltages of all preamplifiers can be canceled. To obtain the input referred offset voltage (V_{osl}) of a latch circuit, one must divide V_{osl} by the gain of all preceding stages. Considering the charge injection mismatches in each stage, it allows to be written the residual offset as follows:

$$V_{os} = \frac{V_{osl}}{\prod_{i=1}^{n} G_0[i] \frac{C_s[i]}{C[i]+C_p[i]}} + \sum_{i=1}^{n} \frac{\Delta q[i]/C[i]}{G_0[i](\prod_{i}^{j=1} G_0[j] \frac{C[j]}{C_s[j]+C_p[j]})} \tag{2.13}$$

where V_{osl} is the input referred offset of the latch, $G_0[i]$ is the static gain of the i stage of the CS amplifier, $\Delta Q[i]$ is the charge injection mismatch from the i stage of NMOS switch. Note that the input referred offset voltage is attenuated by the gain of the proceeding stages.

Comparing (2.12) to (2.13) leads to the conclusion that, as expected, the contribution from the offset voltage of the latch is reduced. However, the offset caused by the charge injection of the first stage switch, S_1, remains unchanged. Moreover there are additional contributions from the charge injection mismatches in the subsequent stages. Therefore

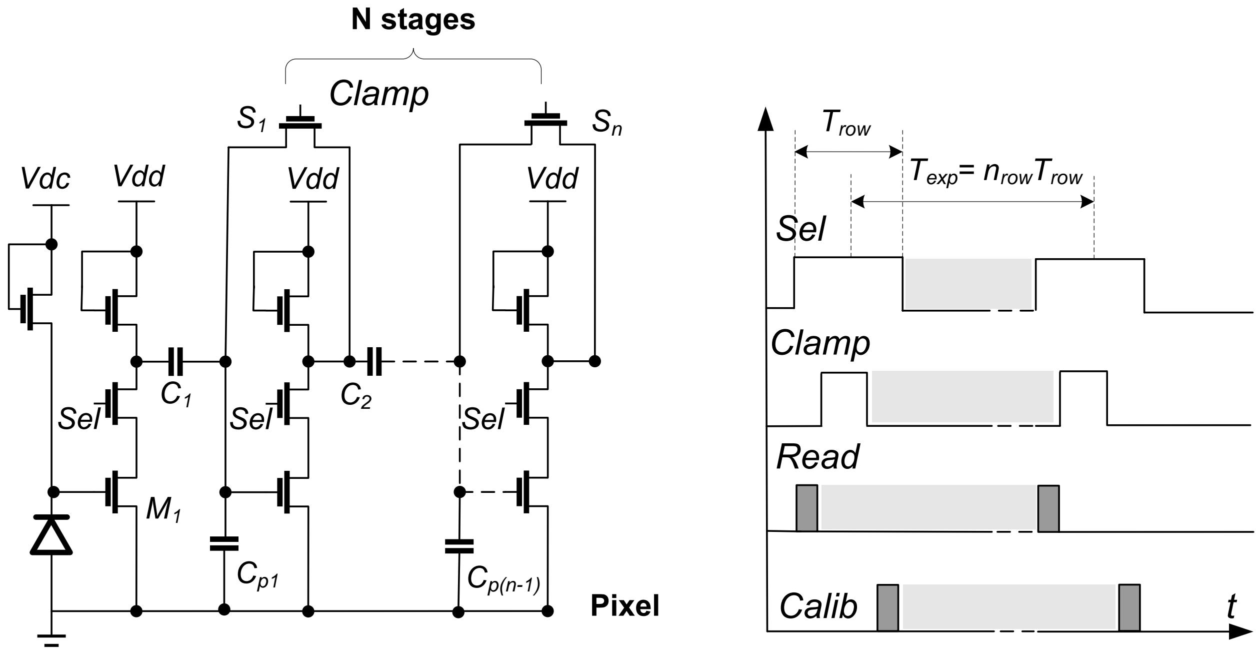


Figure 2.13: In-pixel amplifier with multi-stage input offset storage technique (left) and its timing diagram of the working operation (right).

the resultant offset may not be much smaller than the one achieved with a single stage OOS architecture. To minimize this type of error, this multi-stage preamplifier can utilize sequential clocking, whereas the gain stages leave the offset cancellation mode sequential, S_1 first and S_n last.

When S_1 opens, the first stage of the amplifier leaves the cancellation mode, whereas the following stages are still in that mode. Consequently, the offset due to charge injection mismatch of switches is amplified and stored on the capacitors at its output. In other words, this interval second stage of the amplifier acts as an OOS stage and hence reduces its residual offset to zero. This approach is only valid if the delay between the edges of clock pulses controlling S_1 to S_n is long enough to allow the complete offset storage on the capacitors of subsequent pre-amplifiers. The speed will be a serious restriction to the use of sequential clocking.

Figure 2.13 shows a cascaded preamplifer stages using IOS. The sequential clocking scheme could be utilized to cancel the contributions of all charge injection mismatches again, except the first stage of amplifier. However, as stated above, this solution is hard to be used in high speed operation. In the following analysis, it is considered that all sampling switches open simultaneously to introduce charge injection errors that are not compensated.

The unity gain closed loop around the preamplifier stores the offset voltages on capacitors in series with input. Except for the last amplifier, this voltage is stored simultaneously on the capacitors that precede and follow it, thus canceling its offset. The input referred offset of the latched comparator is obtained as before. The residual offset voltage is,

$$V_{os} = \frac{V_{osl}}{\prod_{i=1}^{n} G_0[i]\frac{C[i]}{C[i]+C_p[i]}} + \sum_{i=1}^{n} \frac{\Delta q[i]/C[i]}{\prod_{i}^{j=1} G_0[j]\frac{C[j]}{C[j]+C_p[j]}} + \frac{V_{osn}}{(1+G_0[n])\prod_{i=1}^{n} G_0[i]\frac{C[i]}{C[i]+C_p[i]}} \tag{2.14}$$

where V_{osn} is the input referred offset of the last stage of amplifier.

When using multi-stage (instead of single-stage) IOS, the contributions from mismatches in the preamplifiers and the latched comparator are reduced. It is even possible to eliminate V_{osn} from the residual offset, by adding another capacitor between the last preamplifier and a latch. However the offset caused by the charge injection of the first stage switch remains unchanged, and there are additional contributions from the charge injection mismatches in subsequent stages.

2.5 Sensor implementation

A prototype sensor has been implemented in order to demonstrate the performance achievable through pixel-level voltage amplification, as outlined in section 2.4.1. Table 2.3 summarizes the most important specification points of this prototype which has been fabricated in an open-access 0.13 μm CMOS Chartered technology.

Die size was chosen equal to one seat size on a multi-project-wafer run in order to limit prototype fabrication cost, the prototype sensor is one of the designs in this chip. Non-epitaxial, high resistivity silicon has been used as a substrate for implementation of pixel sensors in this CMOS technology. Such a substrate without the epitaxial layer may cause a large charge spread (i.e. low CCE) [43], it still can provide a set of measurement

Table 2.3: Selected parameters of the implemented prototype sensor with pixel-level amplification.

pixel dimensions	12μm $\times$ 12μm
pixel array	16×8
diode dimension	3μm $\times$ 3μm

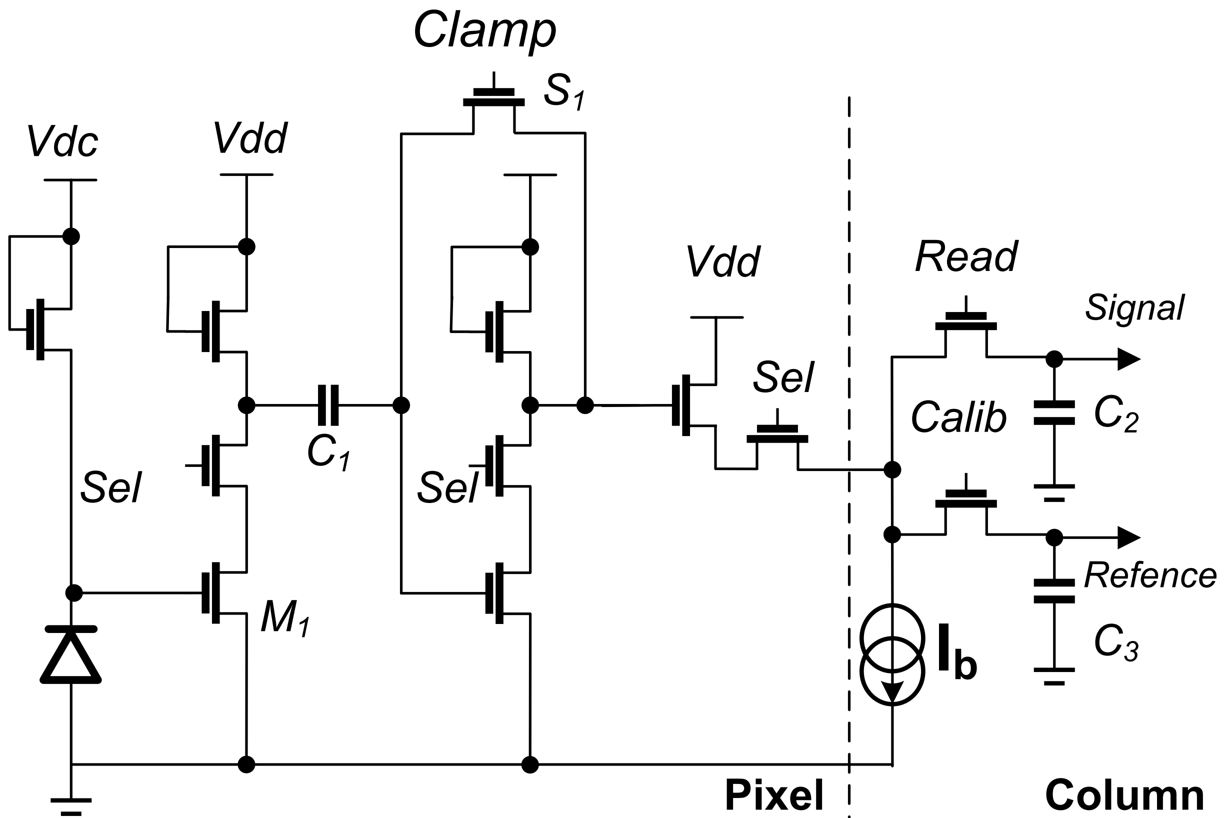


Figure 2.14: Schematic of the pixel implementation.

results with an emphasis on CVF and noise performance.

Although the resulting spatial resolution of 16 μm pitch is sufficient for prototype demonstration, the benefit of selecting a 12 μm pitch is to have a higher spatial resolution of $\sim$ 2.5 μm . On the other hands, it is also noticed that the smaller pixel introduces a higher number of pixels in the same sensitive area, it translates into a high power consumption or/and a slow readout speed of the sensor.

In order to provide a high conversion gain simultaneously with the optimum noise performance, a two-stage voltage amplifier with the proposed input offset-compensated technique is designed. The pixel circuit is shown in Figure 2.14. Each pixel consists of a diode, a pre-amplifier, a second-stage amplifier and a SF. A reset transistor connected between the input and output of the second-stage amplifier allows for a self-biased approach to providing its operation point.

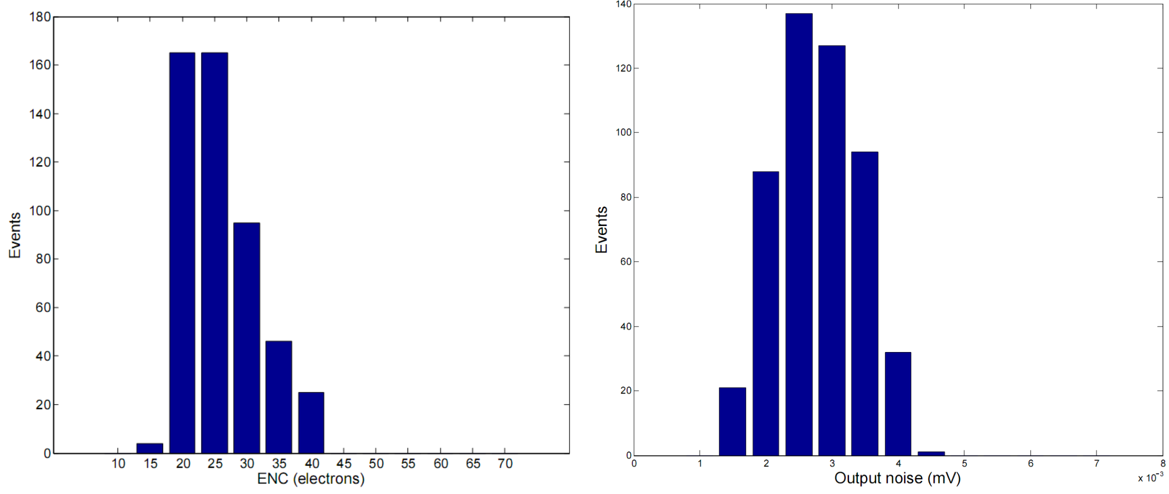


Figure 2.15: Simulated results of pixel noise: the ENC of 22 e⁻ varies with the standard deviation of 5.7 e⁻ (left), the RMS noise of 2.4 mV at the output of the amplifier varies with the standard deviation of 0.63 mV (right).

2.5.1 Simulated characteristics of the pixel architecture

2.5.1.1 DC characteristics of the pixel-level amplifier

The reset voltage is the supply voltage minus the source-gate voltage of the diode connected transistor in a reset configuration, it is expressed in (2.15). An NMOS input device of the 3.3 V supply option is employed for preventing the amplified signal from dropping in the saturation. In combination with a slight reset voltage shift due to the charge-injection effect, this choice provides about 0.8 V of the linear swing, it actually makes full use of the input swing of the column-level readout circuit typically implemented in the standard 1.5 V power supply domain.

$$V_{reset} = \left[\sqrt{\frac{W_2}{L_2}}V_{dd} - (\sqrt{\frac{W_2}{L_2}}V_{th2} + \sqrt{\frac{W_1}{L_1}}V_{th1})\right] \div (\sqrt{\frac{W_1}{L_1}} - \sqrt{\frac{W_2}{L_2}}) \tag{2.15}$$

where W_1/L_1 and W_2/L_2 are the ratios of width and length of input transistor and load transistor, V_{th1} and V_{th2} are the threshold voltages of input transistor and load transistor.

2.5.1.2 Noise analysis

The in-pixel circuit with the column-level load capacitor acts as an effective low pass filter. Generally speaking, noise components, varying more slowly than the sampling

time difference, are suppressed by the subtraction of CDS operation, which attenuates low frequency noise.

The thermal noise of the pixel-level amplifier is generated in the channel of the common-source transistor. Thermal noise power of the load transistor (R), which can be shown to be lower than the input transistor. Thermal noise power spectrum of the amplifier observed on the column line, as expressed in:

$$S_{cs,th}^2(s) = 4kT\gamma \frac{g_m R^2}{|1 + s \cdot R \cdot C_{col}|^2} \tag{2.16}$$

where g_m is the transconductance of the input transistor, C_{col} is the total column line capacitor.

The equivalent noise charge of the amplifier thermal noise is found by referring the output noise after CDS back to the sense node, as expressed in (2.17)

$$q_{cs,th} = C_n \frac{1}{A_{pix}} \sqrt{\int_0^\infty |H_{cds}(f)|^2 \, S_{cs,th}^2(2\pi f)} \tag{2.17}$$

where C_n is the value of the capacitor at the sensing node, A_{pix} is the total gain of the pixel.

The frequency shaping of the pixel-level amplifier noise is defined by the first-order low-pass filtering of the pixel-level amplifier and the frequency response of the CDS operation (2.9). $H_{cds}(f)$ is approximated by its average frequency response amplitude of $\sqrt{2}$. The equivalent noise charge takes the simple expression of (2.18):

$$q_{cs,th} \approx C_n \sqrt{\frac{2kT\gamma}{A_{pix} C_{col}}} \tag{2.18}$$

Two important conclusions can be drawn from expression (2.18) of the pixel-level amplifier's thermal noise as follows:

- CDS does not shape the thermal noise of the pixel-level amplifier because there is no low-pass filtering element.
- The thermal noise on the column line can have very low RMS amplitude, thanks to multiplication of load capacitor on the column line and pixel voltage amplification.

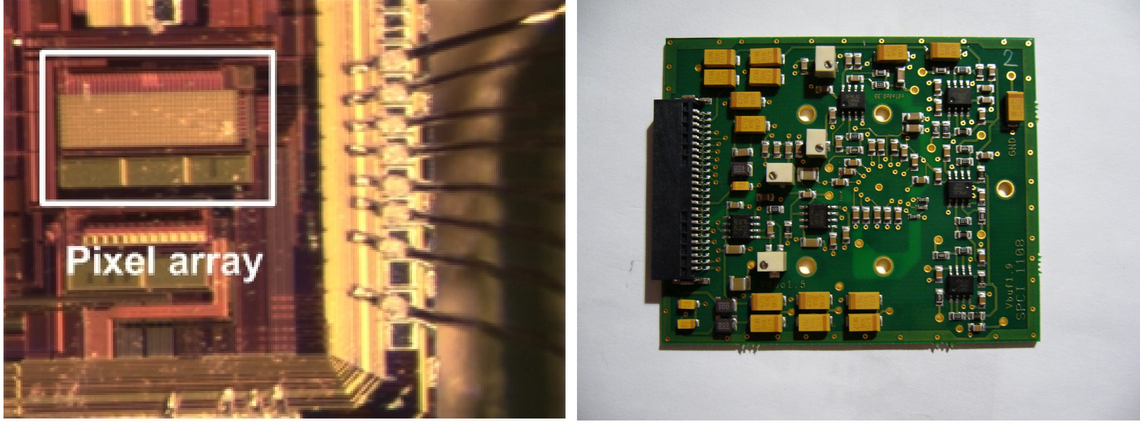


Figure 2.16: Photograph of the prototype sensor (left) and a printed circuit board (PCB) for testing the prototype sensor (right).

Based on the in-pixel schematic, the flicker noise spectrum on the column line generated by the common-source input transistor is given by (2.19)

$$S^2_{cs,1/f}(s) = \frac{K}{C_{ox}WL \cdot f} \frac{A_{pix}}{|1 + s \cdot R \cdot C_{col}|^2} \tag{2.19}$$

where C_{ox}, W, L, K are the gate oxide capacitor density of the input transistor, the gate width, the gate length, the flicker noise constant. The transconductance of the input transistor. The equivalent noise charge of the pixel-level amplifier flicker noise is expressed in (2.20)

$$q_{cs,1/f} \approx C_n \frac{1}{A_{pix}} \sqrt{\int_0^\infty |H_{cds}(f)|^2 \, S^2_{cs,1/f}(2\pi f)} \tag{2.20}$$

The flicker noise of the pixel schematic can be reduced thanks to the low-passing filter, the noise spectrum is directly filtered by the CDS transfer function.

2.5.2 Measurement results

The typical readout chain for CPS testing consists of a mother board as shown in Figure 2.16, an auxiliary board and a data acquisition board connected to a computer. The mother board provides the flexible control signals (e.g. clock and reset signals) and power supply for the chip. Most of these signals are generated from this auxiliary board. The design strategy of the mother board is to make a suitable size and to avoid self-heating in a closed volume. The auxiliary board can be used as a voltage generator, and

as a transceiver for digital signals. A 12-bit ADC with memory banks are designed on the data acquisition board for data digitization. Analog signals from the auxiliary board are converted into the binary outputs and stored in the memories of the data acquisition board. The digital outputs are sampled and sent to the PC via USB ports. The more details of the test system have been described in [44].

2.5.2.1 Noise calculation algorithm

As mentioned in section 2.2, the main objective of noise measurement is to evaluate the values of temporal noise and FPN. A dedicated data analysis program has been developed using C++ builder, the algorithm is described as follows [45]:

According to(2.21), the real signal is obtained by subtraction of the two consecutive samples of the one pixel. The total charge signal of the pixel after CDS operation can be given by:

$$S_{pixel} = S_{signal} + P_{offset} + \sigma_{tem} \tag{2.21}$$

where S_{signal} is the charge signal value due to the interaction between the particles and the silicon, σ_{tem} is the residual random noise value and P_{offset} is the common mode offset value. Considering the accuracy of the noise estimate, an adaptive algorithm is implemented. This algorithm based on weighted sums calculates offset and noise values for each pixel. All of these parameters are digitized in ADC units, which are defined by the data acquisition system. Assuming the acquired data were taken without any source, the simplest offset estimator can be calculated by averaging the measured signals over N events[12].

$$\overline{P_{offset}} = \frac{1}{N}\sum_{n=1}^{N}(S_{pixel,n}(k) - \sigma_{tem,n}(k)) \tag{2.22}$$

where k represents the kth pixel in the array and n represents the nth event in the total N events.

The FPN value, representing the importance of offsets over all pixels, is the standard variance of the offset over a whole pixel array. For an array of M pixels, the FPN value is given by the equation below:

[12] An event is a frame of raw data taken from the pixel array.

$$FPN = \frac{1}{\sqrt{M-1}}\sqrt{[\sum_{k=1}^{M} P_{offset,n}^{2}(k) - M(\overline{P_{offset}})^2]} \quad (2.23)$$

where $P_{offset,n}(k)$ is the offset value of the kth pixel in the array. The temporal noise value is determined for each pixel with the expression below:

$$\sigma_{tem,n}(k) = \frac{1}{\sqrt{N-1}}\sqrt{[\sum_{n=1}^{N} S_{pixel,n}(k)^2 - N \cdot (P_{offset,n}(k))^2]} \quad (2.24)$$

The equation (2.24) gives the temporal noise value of the kth pixel in the array, over total N events. The temporal noise of the array is the average value over all pixels inside it. For an array of M pixels, the mean value of the temporal noise of this array is

$$\sigma_{tem,n} = \frac{1}{M}\sum_{k=1}^{M} \sigma_{tem,n}(k) \quad (2.25)$$

2.5.2.2 Measurement of CVF

The test procedure starts by studying analog outputs with a source Fe^{55}. The signal response of the seed pixel is studied as a function of the diode bias voltage (Vdc) to determine the best working parameters for this pixel architecture, an optimum bias voltage for providing DC operation point of diodes is fixed to 630 mV. The CVF of pixels can be obtained from digital outputs of the board-level ADC per signal charge, it is also a crucial value for calculation of ENC.

The distribution of all extracted signals should exhibit a small peak corresponding to 1640 e^- collected in a single pixel. The CVF can be calculated by the formula of (2.1). The distribution of hits for only one seed pixel, measured by recording a large number of events, is given in Figure 2.17 for all 128 pixels. The measurement was performed at a temperature of 20 °C and at the minimal integration time ($t_{R.O.}$=16 μs). The calibration peak is clearly seen (1 ADC Unit $\approx$ 0.8 mV), when photons deposit all their energy of $\sim$ 5.9 keV on a single pixel. The measured CVF is $\sim$ 166 μV/e^-, it shows that the CVF is about three times larger than one obtained from MIMOSA-26 sensors, due to an additional stage of the amplifier.

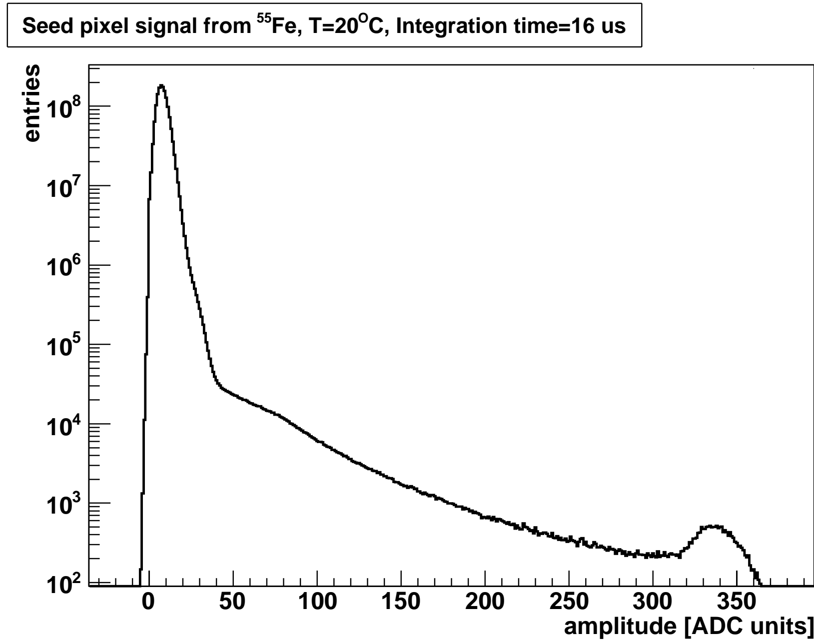


Figure 2.17: The seed pixel signal from Fe^{55} calibration for all 128 pixels. (T=20 °C, $t_{R.O.}$=16 μs)

2.5.2.3 Noise performance

The ENC of the whole pixel matrix is obtained from the measured output noise, expressed by the formula of (2.25). Note that this determination of ENC fully relies on measured output noise and CVF. Thanks to the use of high resolution board-level ADCs, the noise of the board-level electronics is negligible, the pixel noise can be tested accurately. The ENC of $\sim 24\ e^-$ was measured with an integration time of 16 μs for all pixels, this result is shown in Figure 2.18.

2.5.2.4 Lessons learned and future plans

The ENC of the proposed pixel architecture is $\sim$ 2 times larger than the value archived with MIMOSA-26 sensors. The measurement result may reflect an underestimation of the parasitic capacitor at the sensing node, where the extracted capacitor is about $\sim$ 2.3 fF. The noise level of $\sim 15\ e^-$ could be reached by further reducing the parasitic capacitors. A negative feedback configuration built between the pre-amplifier and the diode would be utilized to improve the noise performance in the future designs [32]. In addition, for an unclear reason, nearly 10% of entries in the tail have a large value of noise.

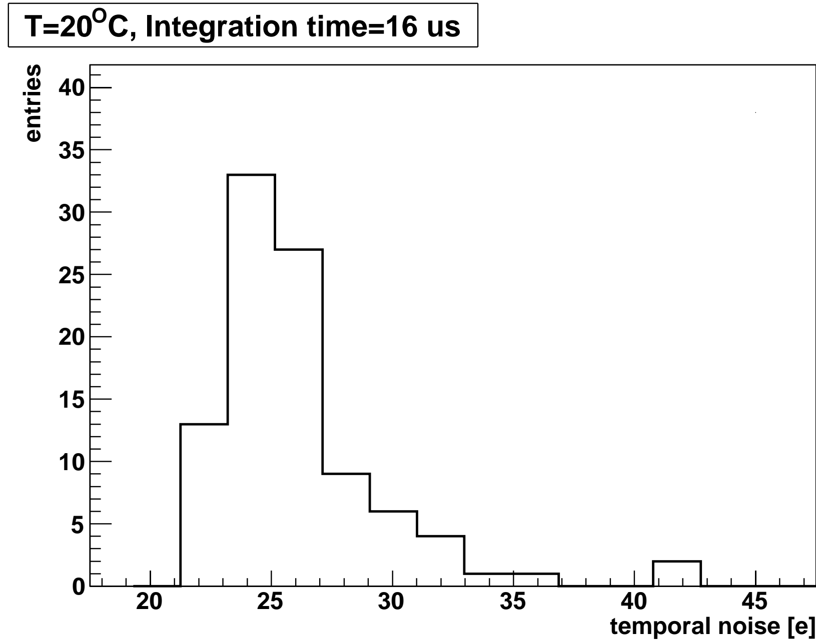


Figure 2.18: Histogram of ENC for all 128 pixels. (T=20 °C, $t_{R.O.}$=16 μs)

Another critical parameter of CPS employing the in-pixel amplifiers is pixel-to-pixel spread of noise (i.e. FPN). The distribution of offsets was calculated statistically by the formula of (2.23). The measured FPN shows that the mismatches of pixels are suppressed by the use of the self-reset configuration, as described in subsection 2.4.1. The analysis of the noise distribution gives a FPN value of $\pm 6.5\ e^{-}$.

2.6 Conclusion

This chapter emphasized the need for fast, granular and thin pixel sensors to equip the innermost layer of a vertex detector adapted to the ILC physics programme. It summarized the state-of-the-art for CMOS pixel sensors of the MIMOSA series, mentioning that they are likely to lead to a device complying with all specifications of the ILD vertex detector operated at a collision energy of 500 GeV or below. The architecture of these sensors is however unlikely to provide the read-out speed needed for the SiD concept, as well for both concepts when going to the highest ILC collision energies foreseen (1 TeV or above).

On the other hand, the intrinsic potential of CMOS sensors is well suited to such requirements, but today's commercial fabrication processes are far from exploiting this potential for the detection of charged particles. It was advocated that the most promis-

ing direction to escape from this major limitation is provided by vertical integration techniques used in industry. A central topic of this PhD was to investigate paths allowing to make CMOS sensors evolve towards multi-tier devices combining different CMOS processes in order to comply with the most challenging among all potential applications.

This chapter, however, was dealing with an approach allowing to circumvent present difficulties encountered with 3D technologies. It exploits the double-sided ladder concept developed for the ILD vertex detector, where the ladders are populated on one face with sensors optimized to reach the ambitioned spatial resolution while the other ladder face is equipped with sensors designed to reach a time resolution significantly better than 10 μs. This approach can be considered as an intermediate step, on the way towards 3D integrated devices, which combine the high spatial resolution and fast architectures in a single chip.

The chapter concentrated on an enhanced in-pixel amplification which would minimize the impact of the noise generated by signal processing micro-circuits implemented downstream of the first processing stage. It showed how a two-stage in-pixel amplifier could be achieved, using an offset compensation technique to mitigate the pixel-to-pixel noise dispersion. Simulations were performed, indicating that the structure would allow increasing the in-pixel gain of present state-of-the-art MIMOSA sensors by a factor of about 3.

A prototype was designed and fabricated in a 130 nm technology, composed of 12 μm pitch pixels. Its tests confirmed the expected gain enhancement, at the expense however of a noise value about twice higher than the typical value of present sensors based on a single-stage pre-amplifier. The noise excess is suspected to originate mainly from the parasitic capacitance of the sensing node, which should be subject to substantial reductions. The prototype also demonstrated that the offset compensation design allowed to suppress quite efficiently the pixel-to-pixel noise dispersion, despite some remaining noise dispersion which needs further investigations.

The pre-amplification circuit developed in this chapter is intended for a continuous, rolling shutter mode, read-out. The next chapter will address an alternative sensor architecture, attractive for its power saving. It exploits the time structure of the ILC, by storing the signals inside the pixels during the full bunch train of the ILC, and by delaying their low frequency readout inbetween consecutive trains.

Chapter 3

3D integrated CMOS pixel sensors with a delayed readout architecture

The access to commercial fabrication processes using vertical integration techniques to staple chips at the pixel level is a recent event. This thesis was driving an effort to explore various alternative architectures relying on such a process for their application to an ILC vertex detector. The targeted specifications went well beyond those motivating the development of 2D chips (see chapter 2) as they addressed the ILC operation at its highest collision energy and include the constrains by both detector concepts, i.e. ILD and SiD.

Since 3DIT improve dramatically the density of functionalities implemented in the pixels, the question raises whether this can be used to realize sensors with delayed read-out, for the benefit of reduced power consumption. This strategy, where the sensor readout is taking place in between bunch trains, is also immune against potential electromagnetic perturbations generated by the e+ e- bunches.

Since all hits generated during a full train are accumulated in the sensor, the main limitation of this scenario comes from pile-up, i.e. hits created at different times inside the train which fire the same pixel. Two alternative approaches may be followed to avoid this obstacle. One consists of making the pixels tiny enough (few μm pitch) to maintain the probability of pile-up at a marginal level. The other approach consists in implementing a counter in each pixel which delivers a time stamping for each hit it has detected.

The second approach requires sizable micro-circuitry inside the pixels, which impacts their dimensions. The challenge of the pixel design consists therefore in realizing an in-pixel micro-circuit offering a time resolution matching the number of hits per pixel integrated over the train duration. This objective translates into the search for a trade-off

between a micro-circuit large enough to provide the required time resolution and a pixel small enough to keep the number of hits per train compatible with the time resolution. 2D sensors would not allow achieving such a trade-off while 3D sensors may allow for it. It is one of the objectives of the thesis to investigate whether they really do. The studies performed for this purpose are summarized in this chapter.

A 2-tier sensor featuring a 12 μm pitch pixel array was developed to suit the constrains of the innermost layer of the ILD vertex detector. Its readout is delayed beyond an integration duration of ~ 1 ms, adapted to the ILC beam time structure. This readout structure is expected to alleviate substantially the sensor power consumption.

The current chapter is organized as follows: the first two sections introduce the advantages of 3DIT and a 3D integration technology used in our design (i.e. Tezzaron 3D integration technology). In the section 3.3, the design strategy of this 3D chip is explained. Section 3.4 discusses the designs and characteristics of the pixels. Section 3.5 shows the test setup and measurement results.

3.1 Advantages of 3D integrated CMOS pixel sensors

As stated earlier, 3D-CPS are expected to resolve most limitations specific to 2D-CPS. By vertically interconnecting two, or more, pixellated chips, the amount of logic per pixel can be increased. The different pixel building blocks can be optimized to a level, where smarter and faster pixel architectures can be implemented. 3DIT therefore provide the following improvements for subatomic physics experiments:

High spatial resolution: The available area per pixel becomes proportional to the number of tiers (layers) in the same 3D stack. With one of the tiers serving as a sensitive device, the functionalities of the circuitry can be partitioned into the analog and digital parts that are used in their optimal processes. A multi-layer structure allows to shrink the pixel pitch, leading to a high spatial resolution (e.g. $\lesssim 3$ μm though the charge is encoded on 1 bit only).

High density in-pixel functionalities: The standard CPS approach may run into another major difficulty, as the need for an efficient charge collection inhibits the use of PMOS transistors within the pixel. By stacking several pixellated structures on top of each other, it becomes possible to use both types of transistors in the non-detecting tiers.

More intelligent structures can also be designed to improve the sensor performance. A smart pixel architecture may also have a beneficial impact on the digital signal processing. (e.g. the application of the pixel-level zero-suppressing readout is very desirable for reducing the volume of the data to the outside world.)

Radiation tolerance: It has already been demonstrated that the radiation tolerance of CPS with a high resistivity epitaxial layer can be extended to the order of 10^{14} n_{eq}/cm^2 [46]. 3DIT allow for combining different CMOS technologies, in which it may provide a separate high resistivity epitaxial layer as a detector layer to improve radiation tolerance.

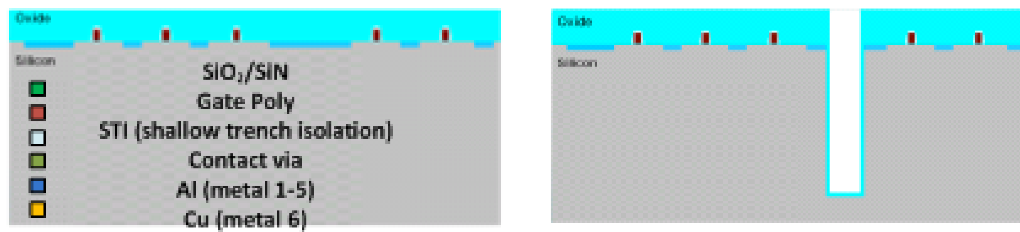
Low material budget: The performance of imaging devices can be greatly enhanced by high-density interconnections of two or more layers with the sensor and advanced readout electronics, which may be thinned to ~ 50 μm by a post-process. By distributing the peripheral readout logics into each pixel, the insensitive zone of 2D-CPS could also be eliminated completely. The application of 3DIT is also expected to provide a very efficient approach to reduce the power consumption [47], because of reduced average interconnect length between analog and digital parts. All the points mentioned above contribute to alleviate the material budget.

High readout speed: 3DIT connect vertically analog and digital electronics tiers, hence the crosstalk will be minimized. Due to the enlarged number of metal layers and reduced load capacitors for the signal processing, the readout speed of the entire pixel array is expected to speed up by at least one order of magnitude compared to the ordinary 2D-CPS.

3DIT, however, may result in temperature hot spots due to increased power density. Therefore, any 3D design should consider the thermal issue in addition to other design parameters [48].

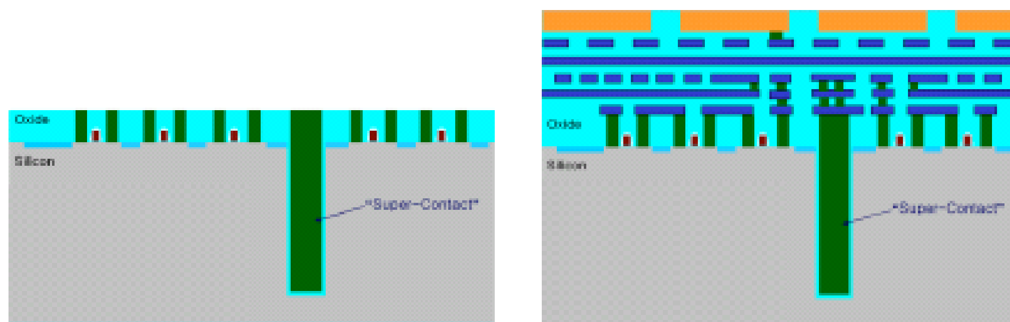
3.2 Tezzaron 3D vertical integration technique

The development of 3D vertical integration in the microelectronic industry brings along significant advantages for pixelated semiconductor sensors in the subatomic physics experiments. 3D-CPS lead the designer towards extending pixel-level processing func-



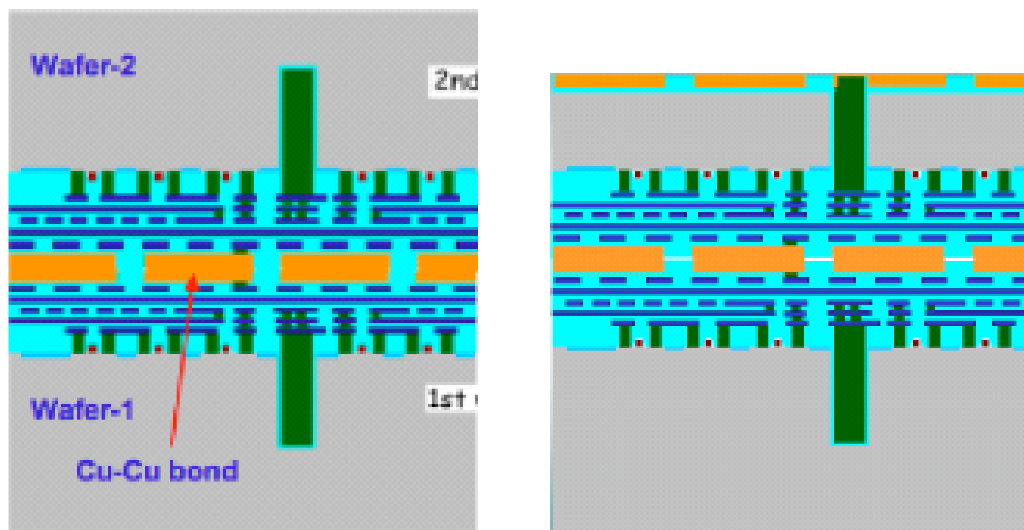
(a) Cross-section of wafer after transistors have been created but before contact metal implementation.

(b) The through silicon via is etched through the oxide and into the silicon substrate.



(c) The TSV is filled with tungsten and finished with chemical mechanical polishing.

(d) The wafer is finished with its normal processing (FEOL processing), which can include a combination of aluminum and copper wiring layers.



(e) The wafers are aligned and bonded in a copper thermal diffusion process.

(f) After bonding the top wafer is thinned to the bottom of the TSVs.

Figure 3.1: Tezzaron's stacking method based on two layers used in the first MPW run.

tionalities and achieving novel structures, where each layer is optimized for a specific function. 3D circuits are stacked by multiple independent electronics layers on top of

each other. By bonding after precise alignment, 3D-CPS are thinned and interconnected through deep metal vias known as through silicon vias (TSVs). Via holes may take place on wafers before or after Front End Of Line (FEOL) processing. This choice, labeled as "via last" or "via first" depends on the fabrication processes [49]. Quite a few bonding techniques are currently developing; the four major bonding approaches [50] are **oxide** bonding, **adhesive** bonding, **eutectic** bonding and **thermo** compression bonding. The two first are via last while the two last techniques are via first.

A consortium [51] was organized to investigate 3D devices, based on two tiers of the 130 nm CMOS Chartered technology interconnected by the 3D Tezzaron integration technology. The Tezzaron process is a kind of via first technology [52]. The TSVs are formed before the Back End Of Line (BEOL) as a part of the Chartered process. In the Tezzaron-Chartered process, the wafers are face-to-face bonded by means of thermo compression technique. The mechanical and electrical connections between two Chartered wafers are created with Cu-Cu thermo compression bonding using the 6th metal layer.

In order to provide a strong mechanical coupling, the pattern of hexagonal metal spots cover completely the chip. The TSVs are drawn with a diameter of 1.3 μm and a minimum pitch of 3.8 μm. As a TSV can only be 12 μm deep at most, the top wafer is so thin that the bottom end of TSVs can be exposed to connect with the buried circuit [53]. Figure 3.1 shows the Tezzaron's stacking method based on two tiers in this MPW run.

The Tezzaron company has stacked successfully five bulk CMOS wafers, using this new enhanced TSV technique. After adding each tier, the height of the total stack is increased by about 15 μm, and there is no fundamental limitation on the number of tiers. Experimental results have shown that the 3D wafers can be thinned to as little as a few microns and stacked with sub-micron alignment. The interconnected wafers can be handled in a normal fashion without special handlers or precautions. The transistors on the stacked, bonded, and thinned wafers were shown to have no discernible performance differences from their original 2D form [54].

3.3 Prototyping strategy of delayed readout architecture

As mentioned earlier, the ILC beam is organized in $\sim$ 1 ms long bunch trains separated by nearly 200 ms periods without beam. The operation of CPS may be tailored to this time structure. It features then two distinct processing phases: a detecting phase

coinciding with the bunch-crossing period, and a readout phase taking place in the beam-less inter-train period.

Most of the hits recorded during a train in the vertex detector are due to beam-strahlung electrons and positrons. In order to facilitate the association of the hits generated by physics processes of interest to the tracks extrapolated from the part of the experimental apparatus less exposed to beam-related background, each pixel is equipped with a time stamping micro-circuit. The strategy consists in making the pixel small enough to be hit at most once per train in a large majority of cases. Once the dimensions are fixed, an in-pixel micro-circuit needs to be designed which provides enough time resolution to fight efficiently against the tracking confusions generated by the high pixel occupancy due to beam background. In absence of this time stamping, the track association would in fact be fooled by this high background hit density.

In order to estimate the sensor specifications, the results of beamstrahlung background simulations were used, which provided the background induced pixel occupancy in the innermost layer. Two extreme values of the average occupancy were considered, in order to account for the uncertainties affecting the Monte-Carlo predictions:

- A low value of the background ($\sim$ Monte-Carlo predictions): 3 hits/cm^2 per bunch-crossing (BX)
- A high value of the background (standing either for more aggressive machine optics or for baseline values with safety factors): 15 hits/cm^2/BX

Two values of the cluster multiplicity were considered in order to sweep the range of possibilities, depending on the signal discrimination threshold, the track bending in the experimental magnetic field (3.5 - 5 T) and its production angle. The values retained were 3 and 6 pixels fired per cluster.

The pixel dimensions were evaluated for the two hypotheses on the background rate and on the hit cluster size mentioned above, using the Poisson distribution function expressing the average proportion (λ) of pixels hit in a bunch train. The goal was to find out how frequently a pixel would fire more than once, and to play with the pixel dimensions in order to keep this probability within an affordable level, making it possible to associate a less accurate time stamping to the second hit firing a pixel, if any.

The frequency at which the pixel fires more than once during a single train is provided by the complement to 1 of the combined probabilities to fire 0 or 1 pixels. Its expression is given hereafter:

Table 3.1: Values of P(N≥2;λ) as a function the pixel pitch, (X,Y) represent the different assumptions: X is the value of the background and Y is the value of the cluster multiplicity.

Pitch	(3;3)	(3;6)	(15;3)	(15;6)
20μm	0.48%	1.80%	9.25%	27.4%
18μm	0.32%	1.21%	6.46%	19.9%
16μm	0.2%	0.77%	4.26%	13.9%
14μm	0.12%	0.46%	2.63%	8.94%
12μm	0.07%	0.25%	1.48%	5.25%

$$P(N \geq 2; \lambda) = 1 - (1 + \lambda) \cdot e^{-\lambda} \tag{3.1}$$

This probability is given in Table 3.1 as a function of the pixel pitch for each of the 2 different assumptions on the hit rates and on the cluster multiplicity quoted earlier [55].

One observes that a pitch slightly in excess of 10 μm may be considered as viable. For instance, a pitch of 12 μm leads to a double hit frequency of $\sim$ 5% in the worst case, i.e. for a hit density of 15/cm^2/BX and a cluster multiplicity of 6. A less extreme situation, where the average cluster multiplicity drops to 3, leads to only 1.5% such cases.

Since the second hit occurs near the end of the train in most cases, a dedicated time stamping[1] is not necessary to record its arrival time. A bit just telling whether or not the pixel has been fired twice should be sufficient. As a consequence, a pitch of 12 μm is considered as a candidate, where 3D-CPS have the capability of recording the time stamping of the first hit and flagging the second hit. For a $\sim$ 1 ms bunch train, a 7-bit time-to-digital converter (TDC) accuracy is required to achieve a satisfactory time resolution of $\sim$ 7.5 μs.

As a consequence, we proposed a pixellated 3-tier CPS device adapted to the innermost layer of the ILD vertex detector, of which the 3 tiers should be integrated into a 12 μm pitch: in the bottom tier, the pixel contains a sensing element and a preamplifier for signal detection. The intermediate tier contains a shaper and a discriminator for signal discrimination. And the digital top tier performs a Time-to-Digital Converter (TDC) for the first hit with a time stamping of $\sim$ 7.5 μs and sets a flag for the potential second hit.

[1] The basic idea of this approach is to record the time at which a hit has occurred in digital form, so called time stamping.

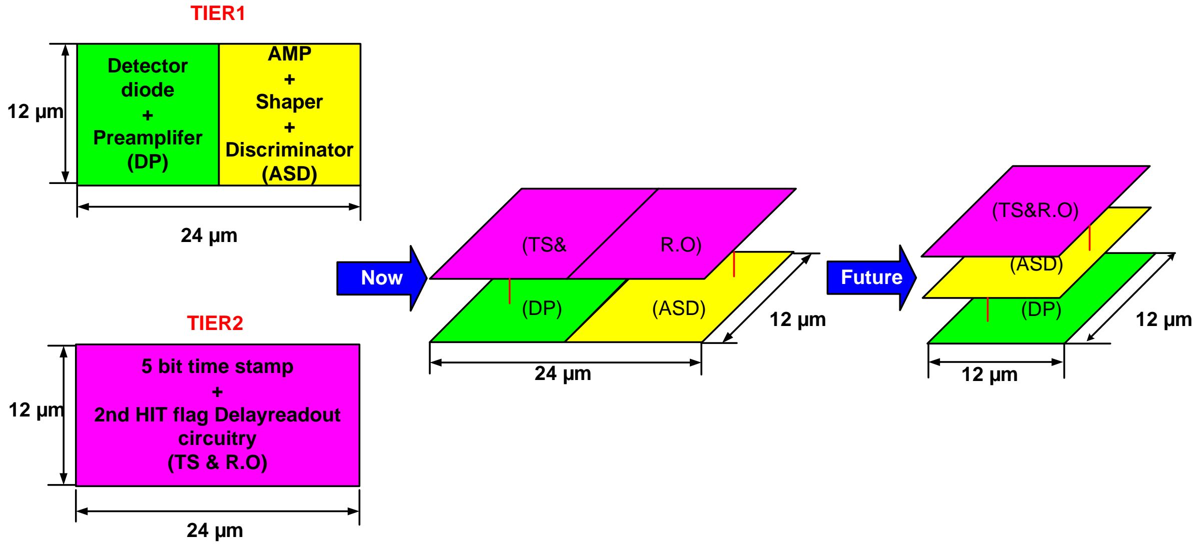


Figure 3.2: Prototyping strategy for the first 3D chip: from so far a 2-tier CPS with 12 μm×24 μm pixels to a 3-tier CPS with 12 μm×12 μm pixels.

Although a 3-tier pixel structure is targeted for specified applications at the ILC, the first 3D submission using Chartered/Tezzaron technology was limited to only two tiers. The main purpose of the prototype is to functionally validate the concept of 3D-CPS, and not to provide an ultimate and optimized version. It was therefore acceptable to make a slight modification, where the circuits of the bottom and middle tiers are spread out on the same tier with a 12 μm×24 μm rectangular pitch.

With this modification, the pitch of the digital pixels reflecting the final top tier was doubled from 12 μm×12 μm to 12 μm×24 μm. Even with twice as large pixel area, there was still not enough space to implement a 7-bit TDC, and a reduced accuracy TDC featuring 5 bits was therefore implemented. For the final chip, the perspective is to use smaller feature processes (e.g. 0.65 μm CMOS technologies) as a digital part to perform a 7-bit time stamping. Figure 3.2 illustrates the prototyping design strategy of such a 2-tier CPS.

3.4 Topology and circuit analysis

During the detecting phase, the counting values of a 5-bit time stamping are sent synchronously to all pixel cells. When a pixel cell is fired, the content of its time stamping is stored in registers. During the beam-less readout period, the inactive detectors have time to cool and perform a delayed readout.

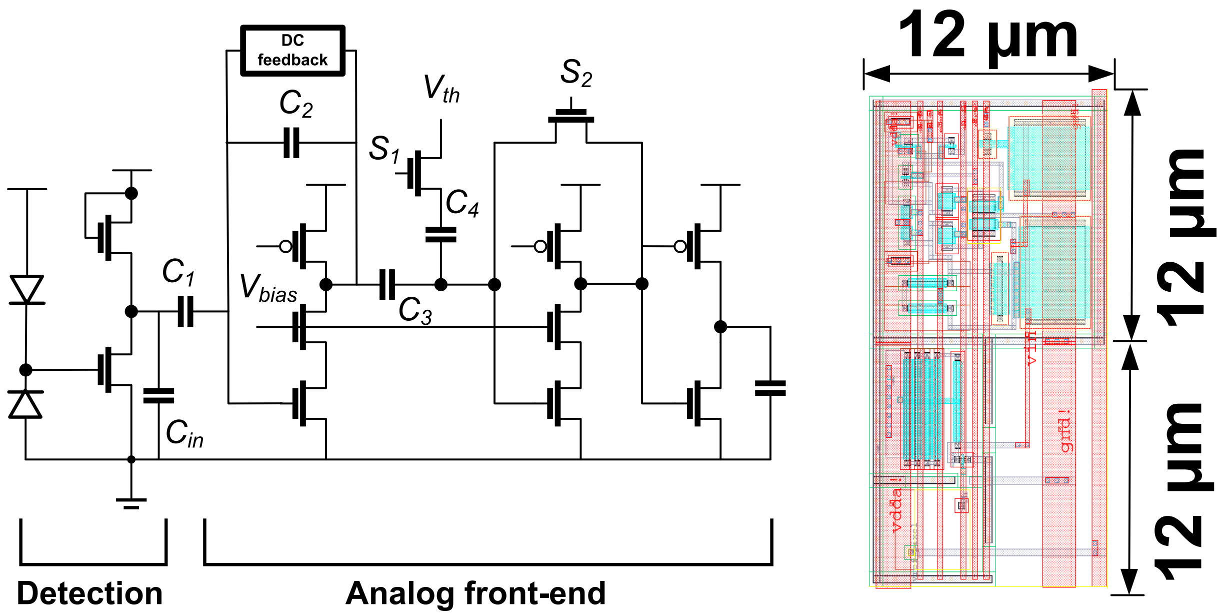


Figure 3.3: Schematic (left) and layout (right) of the proposed analog pixel cell.

The chip features a matrix of 256×96 rectangular pixels. Each "analog pixel"[2] contains a 12 μm ×12 μm detector part and a 12 μm ×12 μm analog front-end. The analog tier is divided into two main types of sub-matrix, the only difference between them is that in one sub-matrix the diodes are replaced by calibration test structures for studying the performance of the front-end electronics.

The digital tier includes the time stamping logics in each pixel and a 5-bit column-level gray counter. The implementation of the gray code is to minimize the cross-talk effects. With 5 bits accuracy, a hit during the $\sim$ 1 ms bunch train will be flagged with a $\sim$ 30 μs time slot. The rare cases of a second hit during the same train will be marked by a flag. When the pixel array is operated in the readout mode, the digital pixels are chained together and formed as a serial register, and the data of hit information is interfaced with an 8b/10b serial transmitter at a data rate of up to 100 MHz.

3.4.1 Pixel design on the analog tier

The block diagram of the analog front-end is shown in Figure 3.3. Two designs of the feedback resistor are implemented, the blocks of the analog front-end with the different DC feedbacks are shown in Figure 3.4.

[2]Analog pixel is defined as the pixel of the analog tier (intermediate tier).

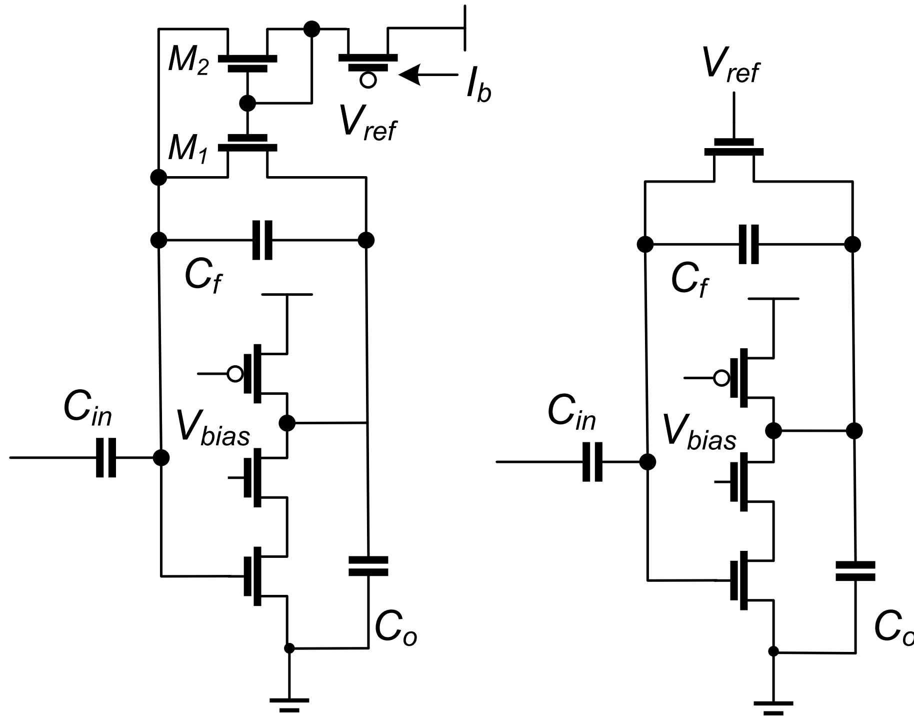


Figure 3.4: Feedback with a constant current source (left) and with a MOS switch (right).

3.4.1.1 Feedback with a constant current

The first version of the shaping stage, a time invariant shaper [56], is an alternative to the feedback network. It consists of a current mirror structure continuously resetting the shaper feedback capacitor C_f. The bias current is externally adjustable and the saturation voltage of the current-mirror transistor is very small. As soon as a signal appears, it generates a current exceeding the bias current. The output of the shaper drops and puts a pair of current-mirror transistors in their saturated regime. Since C_f is discharged by the reference current of the current mirror, the recovery time increases linearly with the signal amplitude and is also suitable to apply in applications with time over threshold detection. The current mirror configuration is capable of providing an attractive trade-off between noise performance, consumed silicon pixel area and power consumption.

The function of the circuit is derived here for identical transistors M_1 and M_2 operating in strong inversion with an usual square law current relation $I_D = K^{'}(V_{GS} - V_T)$ in saturation and $I_D = 2K^{'}V_{DS}(V_{GS} - V_T - 0.5V_{DS})$ in the linear region[3]. The abbre-

[3] The operation of a MOSFET may take place in three different regimes: weak inversion, saturation and linear. It depends on the voltages at the terminals, V_{GS} and V_{DS} are the gate-source voltage and

viation $K^{'} = \frac{K}{2}\frac{W}{L}$ is used, with K being the transconductance parameter and W and L the width and the length of the transistors, respectively.

This configuration is suited for negative input charges which produce positive output signals. A leakage current I_{leak} leads to a slightly positive potential at the output so that the source of M_1 is actually at the input. $V_{GS,1}$ of M_1 can be expressed as

$$V_{GS,1} = V_{GS,2} + V_{DS,1} = V_T + \sqrt{\frac{I_b}{K'}} + V_{DS,1} \tag{3.2}$$

With I_b flowing through M_2 in saturation. Equation(3.2) shows that M_1 operates in the linear region ($V_{DS,1}$<$V_{GS,1}$-V_T) when no output signal is presented and so,

$$I_{leak} = 2K^{'}V_{DS,1}(V_{GS,1} - V_T - 0.5V_{DS,1}) \tag{3.3}$$

Injecting (3.3) into (3.2) and solving for $V_{DS,1}$ leads to

$$V_{DS,1} = \sqrt{\frac{I_{leak} + I_b}{K'}} - \sqrt{\frac{I_b}{K'}} \tag{3.4}$$

and again using (3.2),

$$V_{GS,1} = \sqrt{\frac{I_{leak} + I_b}{K'}} + V_T \tag{3.5}$$

When a negative charge is deposited at the input, the output becomes positive and M_1 goes into saturation. The potential at the input is held nearly constant by the feedback action of the amplifier. $V_{GS,1}$ remains unchanged as long as the voltage at the node V_b does not vary. The current through M_1 becomes

$$I_{active} = K^{'}(V_{GS,1} - V_T)^2 = I_{leak} + I_b \tag{3.6}$$

The feedback in this saturation provides the leakage current (I_b) to discharge C_f. A very similar result is obtained, if both devices operate in weak inversion. The increase of the feedback current by I_b is independent of the output amplitude and so the feedback capacitor C_f is discharged with a constant slope. The output pulse comes back to the baseline after a time

$$\zeta = \frac{Q}{I_b} \tag{3.7}$$

---

drain-source voltage respectively, V_T is the threshold voltage of the transistor.

The width of the pulse increases linearly with the injected charge Q and a measurement of the width of the discriminated output signal can be used to determine the analog charge deposition.

3.4.1.2 Feedback with MOS in saturation

The second version of the shaping stage is a continuous-time MOS-resistor feedback shaper [57]. It allows for a fast return to the output of a cascaded amplifier. A common gate transistor operated in the linear region can achieve very high effective feedback resistance. A MOS transistor has a channel resistance of $R = [K(W/L)(V_{GS} - V_T)]$. If a resistor in parallel to the feedback capacitor is used to discharge, for instance C_f =5 fF in τ= 100 ns, a value of R_f=20 MΩ is required. The transconductance of the common gate transistor increases with the output pulse amplitude. A fast return to the baseline can therefore only be achieved at the cost of distorted energy detection, because the additional noise of the biasing transistor will be brought in. Figure 3.5 shows the transient simulated signal at the shaper output, when a current mirror is used in the feedback network.

3.4.1.3 Zero crossing pixel-level discriminator

In this approach, a discriminator is used to detect a shaper output signal above a given threshold. It generates a digital hit signal which is fed to the readout. Because of the large number of individual pixels comparing a sensor (typically 10^5 to 10^6), the cancellation of the offset voltage is crucial to keep the dispersion of the signals from all pixels at an affordable level. A careful design of the discriminator and all circuit components affecting the hit efficiency is therefore necessary. For this purpose, an offset cancellation method has proposed [58]. If the switch S_2 (see figure 3.3) is turned on, the comparator is in a unity-gain negative feedback configuration, and the offset voltage is stored on the capacitor C_4 with the opposite polarity. This mode is called the "offset cancellation phase". Then the residual input-referred voltage offset is expressed by

$$V_{os} = \frac{V_{os1}}{1 + A_o} + \frac{\Delta Q}{C_3} \tag{3.8}$$

where V_{os1} and A_o are the input offset and open loop gain of the amplifier respectively, ΔQ is the mismatch in charge injection from switches S_1 and S_2 onto the capacitors C_3. In the next phase, when the switch S_2 is turned on and S_1 is turned off, the additional

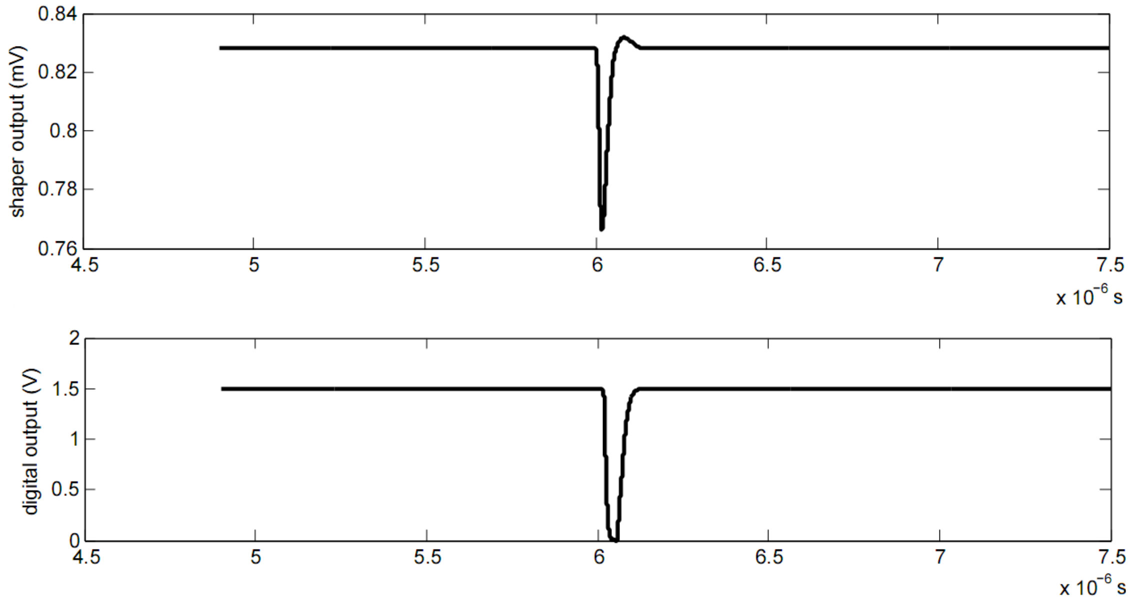


Figure 3.5: Feedback with a constant current source: top figure shows transient simulation outputs of the analog shaper. Bottom figure displays the output of the discriminator, where the discriminator is triggered by a test injection of ∼ 4 mV and the output of the discriminator is changed from logical one (1.5 V) to zero (0 V).

capacitors, C_3 and C_4, are coupled between the input of the amplifier and the threshold voltage node. Then, the voltage at the output of the amplifier is given by:

$$V_{out} = (\frac{C_3 + C_p}{C_3 + C_4 + C_p} \cdot V_s - \frac{C_4 + C_p}{C_3 + C_4 + C_p} \cdot V_{th}) \cdot A_1 \tag{3.9}$$

where V_{out} is the output voltage of the discriminator; V_s is the input voltage of the discriminator; V_{th} is an adjustable threshold voltage; C_p is the parasitic capacitance at the input node of the discriminator, A_1 is open loop gain of the discriminator.

3.4.1.4 Noise in the analog front-end

Figure 3.6 shows the circuit used for the calculation in this sub-section. The shaper consists of a transistor with transconductance g_m driving into a resistor R_0. The capacitor at the shaper output node is C_0. This circuit has the frequency-dependent voltage gain

$$v(s) = \frac{v_{out}(s)}{v_{in}(s)} = -\frac{v(0)}{1 + s/v(0)} \tag{3.10}$$

With the complex frequency variable $s = iw$ and with the DC-gain and band-width constants:

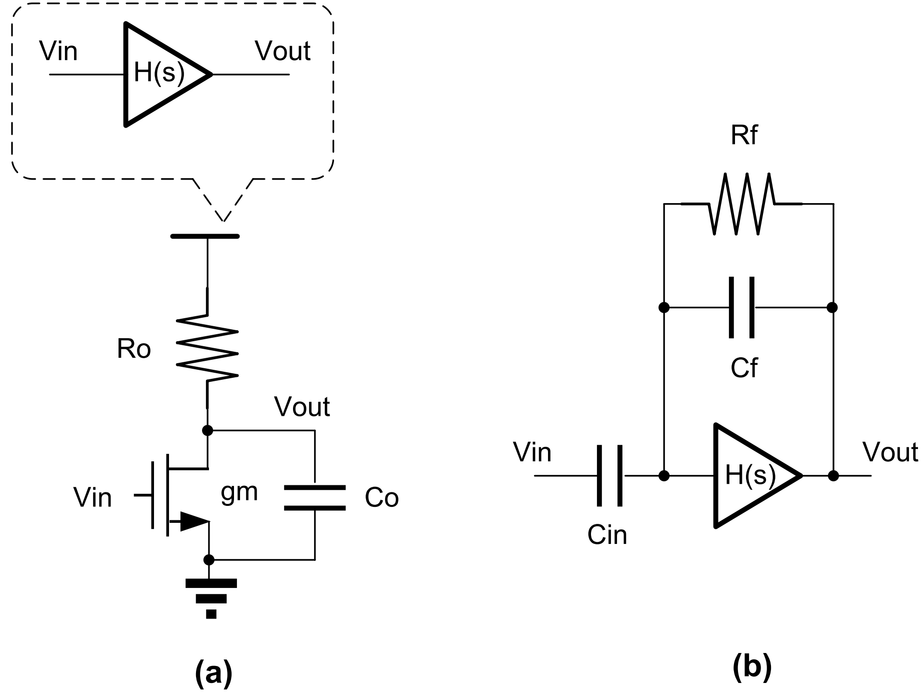


Figure 3.6: Circuit used for the noise calculation. The preamplifier (a) is a simple gain stage with a capacitor load C_0 and (b) the configuration of the shaper. The feedback capacitor C_f is discharged with a resistor R_f.

$$v(0) = g_m R_0, w(0) = \frac{1}{C_0 R_0} \tag{3.11}$$

The feedback capacitor C_f is discharged by a large resistor R_f. Summing currents at the input leads to

$$i_{in} = sC_{in}v_{in} + (v_{in} - v_{out})(\frac{1}{R_f} + sC_f) \tag{3.12}$$

The elimination of v_{in} by (3.10) results in

$$-\frac{v_{out}}{i_{in}} = \frac{v(0)}{\frac{1+v(0)}{R_f} + s[\frac{1}{w_0}R_f + C_{in} + (1 + v(0))C_f] + s^2\frac{C_f+C_{in}}{w(0)}} \tag{3.13}$$

The effective input capacitor of the shaper should be significantly larger than the sensor capacitor. Furthermore, C_f should be usually much smaller than C_{in} in order to achieve a high charge gain. With the conditions

$$v(0)C_f \geq C_{in} \geq C_f, v(0) \geq 1 \tag{3.14}$$

and using (3.11), expression (3.13) simplifies to

$$H(s) = -\frac{v_{out}}{i_{in}} \approx \frac{R_f}{1 + s(\frac{C_0}{g_m} + R_f C_f)} + s^2 \frac{R_f C_{in} C_0}{g_m} \quad (3.15)$$

This transfer function describes how a current signal of frequency $s = iw$ at the input is converted to a voltage signal at the output of the shaper. The term $R_f C_f$ expresses the discharge time constant τ_f of the feedback capacitor. It should be larger than the rise time of the output signal τ_r. It is therefore reasonable to get:

$$R_f C_f \geq \tau_r = \frac{C_0}{g_m} \frac{C_{in}}{C_f} \geq \frac{C_0}{g_m} \quad (3.16)$$

so that (3.15) simplifies to

$$H(s) = -\frac{v_{out}}{i_{in}} = \frac{R_f}{1 + as + bs^2} \quad (3.17)$$

with

$$a = R_f C_f, b = \frac{C_0 C_{in} R_f}{g_m} \quad (3.18)$$

The noise performance of the front-end circuit is usually expressed by the means of the ENC. Fluctuations in the drain current of the input element is modeled by a voltage source e in series with its gate, whose power spectral density includes a channel thermal noise term and a 1/f noise term:

$$\frac{d\overline{e_n^2}}{df} = \frac{8kT}{3g_m} + \frac{K_f}{C_{ox} W L f} \quad (3.19)$$

In (3.19), k is the Boltzmann's constant, T is the absolute temperature, K_f is a 1/f noise intrinsic coefficient. The noise density depends on the frequency f and is largest at low frequencies. As before, the output noise (1/f noise) is provided by the relationship:

$$v_{1/f}^2(out) = \frac{K_f C_{in}^2 R_f^2}{C_{OX} W L} \int_0^\infty \left| \frac{s}{1 + as + bs^2} \right|^2 \frac{df}{f} \quad (3.20)$$

The approximation of widely separated poles has again been used in this calculation and some approximations have been made. The ENC becomes

$$ENC_{1/f} \approx \frac{C_{in}}{q} \sqrt{\frac{K_f}{C_{OX} W L}} \sqrt{ln(\tau_f \frac{g_m}{C_0} \frac{C_f}{C_{in}})} \quad (3.21)$$

Noise calculations will be performed under a simple hypothesis that this DC feedback can be modeled in terms of a resistor R_f. The white thermal noise current of the feedback resistor has the effect on $v^2_{1/f}(out)$:

$$v^2_{Rf}(out) = \int_0^\infty |H(s)|^2 \frac{d(i^2_{Rf})}{df}\frac{df}{f} \tag{3.22}$$

The feedback resistor current has a white noise spectrum with a spectral density (with units A^2/Hz) of

$$\frac{d(i^2_{Rf})}{df} = \frac{4kT}{R_f} \tag{3.23}$$

The ENC of

$$ENC_{Rf} = \frac{C_f}{q}\sqrt{\frac{kT}{C_f}} \tag{3.24}$$

It does not only depend on the value of the feedback resistor but also on the integration time. So the increase of the thermal noise for smaller resistor values can be canceled by the simultaneous reduction of the integration time.

The white thermal noise in the channel of the input transistor leads to an equivalent white noise voltage source at its gate with a white spectral density of

$$\frac{d(v^2_{therm})}{df} = \frac{8kT}{3g_m} \tag{3.25}$$

The output noise becomes

$$\begin{aligned} v^2_{therm}(out) &= \int_0^\infty |H(s)|^2 \frac{d < i^2_{therm} >}{df}\frac{df}{f} = \frac{8kT}{3g_m}\int_0^\infty \left|\frac{s}{1+as+bs^2}\right|^2 \frac{df}{f} \\ &= \frac{2}{3}kT\frac{C_{in}}{C_f C_0} \end{aligned} \tag{3.26}$$

and so

$$ENC_{therm} = \frac{C_f}{q}\sqrt{v^2_{therm}(out)} = \sqrt{\frac{kT}{q}\frac{2C_{in}}{3q}\frac{C_f}{C_0}} \tag{3.27}$$

The approximative calculations of the noise have illustrated some general facts:

- The noise can be determined by manipulating the frequency-dependent transfer function of the shaper.

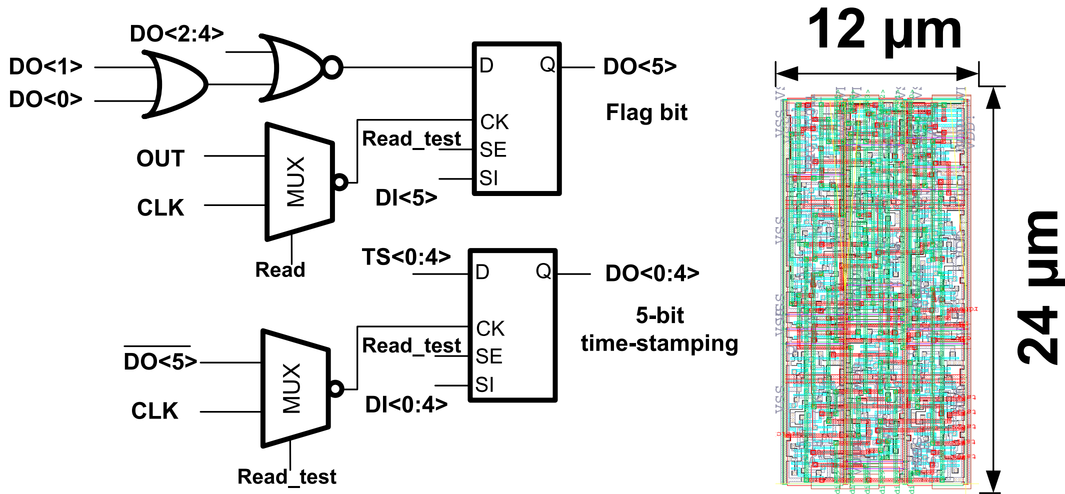


Figure 3.7: Schematic block of the digital pixel (left) and the layout of the digital pixel (right).

- The fundamental noise can be increased in a slower system due to the sensor leakage current and feedback resistor current.

- A relatively modest ENC (about 20-30 e^-) can be achieved without any effect for each pixel with the input capacitance ($\sim$ 1 fF) and input devices with moderate g_m.

When we consider the contribution of the thermal noise and the 1/f noise, the ENC component should be optimized. Meanwhile, in order to save the power consumption of the front-end circuit, the input NMOS device of the shaper features a W/L = 3/0.5 aspect ratio and a drain current of 1.5 μA. The expected ENC is less than 30 electrons and the charge sensitivity is about 250 μV /e^- . The Mont-Carlo simulations from 1000 events with 100 electrons show a shaping time of 20 ns. The simulations show the expected mean ENC value (20 e^-) and its standard deviation (1.6 e^-), and the predicted amplitude of the shaper output, which is equal to 62 mV with a standard deviation of 3.5 mV.

3.4.2 Pixel design on the digital tier

Figure 3.7 shows a block diagram of the "digital pixel"[4] cell, including the logics of time stamping registers and a 2nd hit flag. DO <0:5> are the pixel output signals propagated to the next pixel cell in the column, while DI <0:5> are the signals arriving from the preceding digital pixel cell. During the acquisition mode ($Read = Read_{test} =$

[4] Digital pixel is defined as the pixel of the digital tier (bottom tier).

Table 3.2: Truth table of the digital outputs: out<0:6> are the output signals of the digital pixel, out<0:4> are the value of the time stamping, out<5:6> represent the number of the hits firing the same pixel.

Number of the hits	out<5:6>	out<0:4>
0	00	0
1	01	Certain time-stamping value
2	10	Certain time-stamping value

0), when the first hit is discriminated, the time stamping content is captured immediately by the five scan flip flops.

If a second hit arrives in a pixel, the upper scan flip flop is triggered because the output of NOR-gate has been set to zero by the first hit, so the 2nd hit flag is changed without once again triggering the other five scan flip flops (since they are only sensitive to the rising edge of the $Clock$ signal). However, when the second hit comes up, the flag returns back to zero, which is the same value as the initial state of the flip flop. In order to present the hit information in a simple format, a hit encoder is designed for presenting the time stamping together with a two-bit header that indicates the number of hits in every pixel. Table 3.2 lists the truth table of its functionality.

In order to avoid potential problems from the TSVs, the circuits of the digital tier are designed for standalone functional verification. The circuits of the digital tier can thus be tested separately by injecting a hit like signals independently of the analog discriminated signals. In this test mode, the $Read$ signal is asserted ($Read = 1$), without asserting $Read_{test}$ ($Read_{test} = 0$). The $Clock$ signal is used to inject pulse signals to emulate the hits.

3.4.3 Delayed readout

The timing of the rising edge of the discriminator output can be memorized so that the time stamping can be determined digitally by catching the arrival time of the hit. The time stamping for a hit could be stored, in principle, in the pixel and the trigger coincidence made there. However, this would block a hit pixel during the readout phase, so that the power of the chip is turned off. The time stamping values are therefore transfered to buffers at the bottom of the pixel columns. The most important elements of the digital readout are sketched in Figure 3.8, where three elementary tasks are running

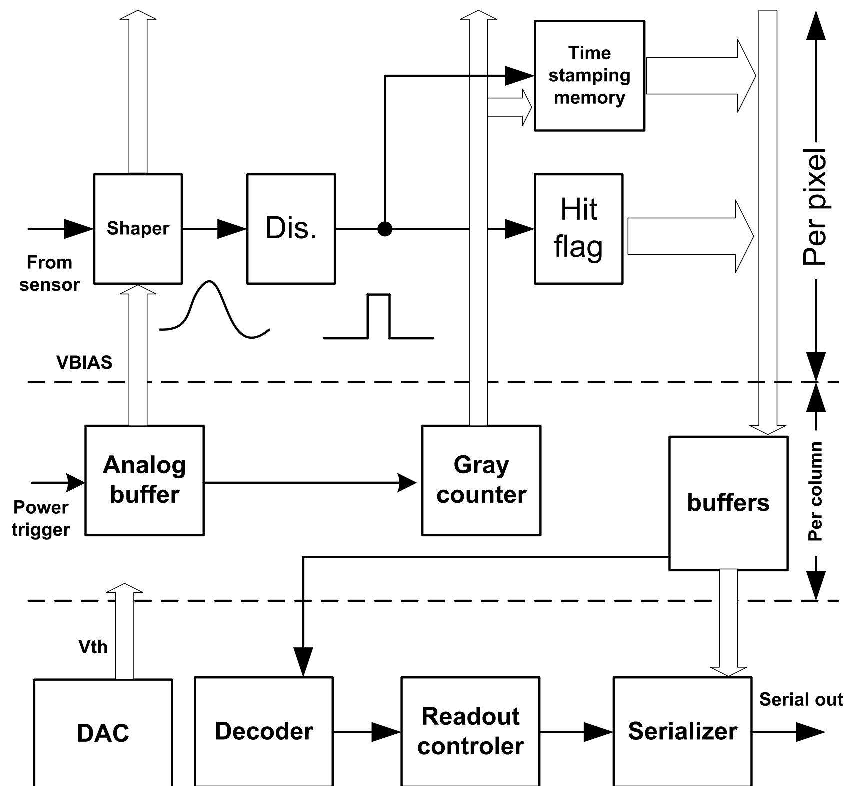


Figure 3.8: Simplified diagram of the time stamp readout used in our chip.

in parallel:

- A 5-bit time stamping counter operated at a period of 31.3 μs generates the time reference which is distributed to all pixels in the chip. The counter uses Gray encoding to avoid out-of-sequence values during transition and to minimize the number of bit transitions and thus power consumption. When a pixel is hit, the time stampings of the rise of the discriminator output signal are stored in memory cells in the pixel. The pixel data are ready to be processed when the second hit has occurred and then a hit flag is set.

- During the readout phase, all pixels are connected and become a long shift register. The information of all pixels stored in the local pixel are transferred to the buffers at a programmable rate of 1-5 MHz.

- A readout controller (i.e. the finite state machine) controls the entire readout of the chip. The controller operates the serial transmitter in the idle, preamble and write modes. During data acquisition phase of the bunch train, the serial transmitter is operated firstly in the idle mode, where it continuously sends a new synchronization

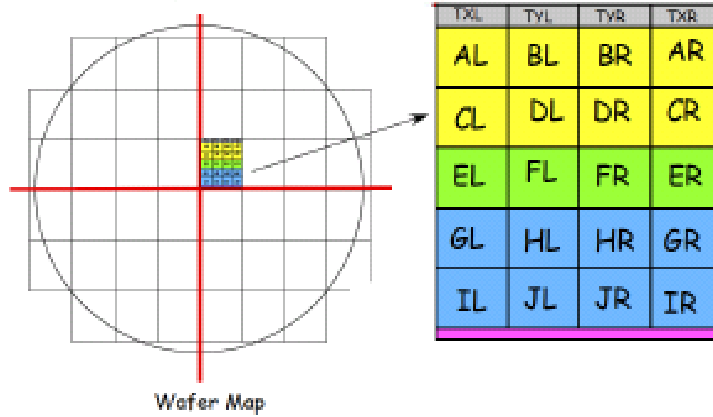


Figure 3.9: Reticule (or frame) for the first multi-project wafer run (left), the frame including A-J sub-reticules (right): L is the top-tier of the 3D chip; R is the bottom-tier of the 3D chip.

vector to synchronize the receiving end. At the end of the bunch train, it goes to the preamble mode and indicates a start of data transmission, and then the write mode is ready for transmitting data until all pixels are read out. The FSM is also responsible of providing the $Clock$ and $Read$ signals to the pixel cells, meanwhile, an integrated 8b/10b serial transmitter is synchronous with a main readout clock generated by a low jitter and low power PLL.

3.5 Experimental results and discussion

3.5.1 Description of the chip

In order to prove the functionalities of the 3D integrated chips, three test chips called CAIRN[5] have been designed by IPHC. One of the three chips, named CAIRN-1, is introduced in this chapter. The chip was submitted for fabrication in September 2009 in this MPW run. The reticule contains twelve sub-reticules allocated to the different MPW contributors, as shown in Figure 3.9. CAIRN-1 is located in sub-reticule B.

The CAIRN-1 design includes:

- 3D integrated CPS pixel matrix of 96 × 256 pixels, featuring a 12 μm × 24 μm pitch, with a delayed readout architecture;

[5] standing for CMOS Active pixel sensors with vertically Integrated Readout and Networking functionalities

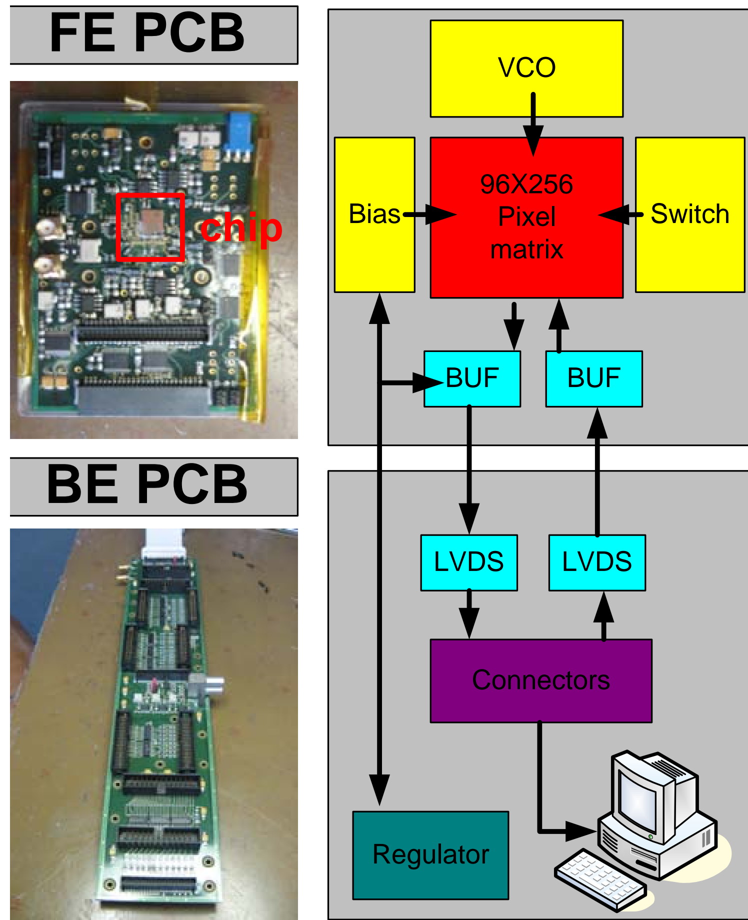


Figure 3.10: The BE PCB board and FE PCB board on which the CAIRN-1 chip is mounted (left), and the main electronic components of FE and BE PCB boards (right).

- Test architectures consisting of a 160 MHz PLL, a 8-bit Digital-to-Analog Converter (DAC) and a 8b/10b encoder;

3.5.2 Test setup

In order to have maximal flexibility and to save the power consumption of the system, the detection system follows a two-board scheme developed for this prototype (see Figure 3.10). A front-end (FE) board is wire-connected to a separate compact back-end (BE) board, which transfers the control signals and the output data. The FE board includes the biasing voltage generators, a programmable DAC and the analog buffers. Two 32-pin connectors on the BE board allow for providing the power supply from the regulator and input control signals from a logic analyzer. A personal computer (PC) is used to store and show the output digital signals.

3.5.3 Measurement of misaligned 2D chips

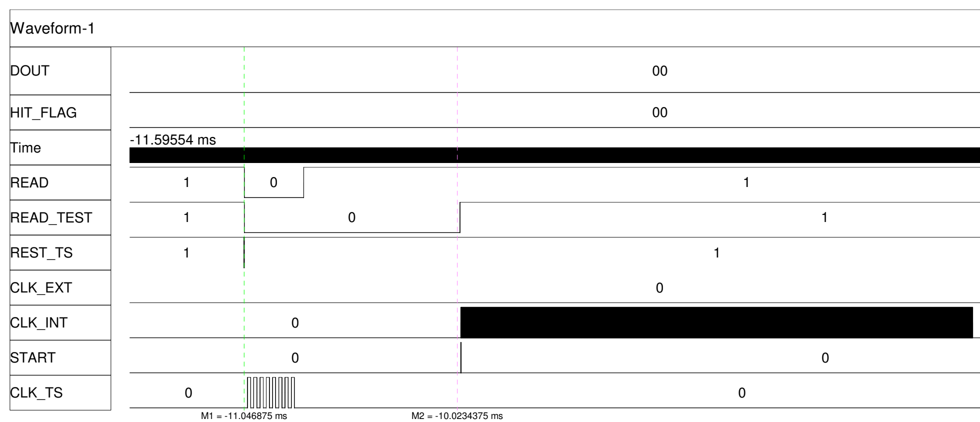
CMOS wafers with the two separate tiers of these CPS were delivered at the end of 2010. One of these wafers was diced before 3D bonding, and the resulting chips were successfully tested. In the layer with digital pixels and readout circuitry, the functionality of delayed readout has been verified and its test result is shown in this sub-section. The wafers from this submission were bonded by Tezzaron and one of the layers was thinned to expose TSVs and provide access to the two device tiers. Presently (October 2011) the first completed 3D wafers are being delivered by Tezzaron and finally, after wafer dicing, 3D chip testing is expected to begin very soon.

Our test chip (CAIRN-1) was designed using a 0.13 μm CMOS Chartered technology. The chip consists of 96 x 256 pixels, providing an active area 1 x 3 mm^2. In the laboratory tests, various patterns were emulated with a pattern generator, and ran through the logic millions of times, but the circuit has been working for clock frequencies up to 10 MHz (i.e. 20 times faster than the nominal readout frequency); beyond 10 MHz logical errors were reported. The delayed readout response was studied on 3 different chips in order to evaluate its basic functionality, all chips exhibited very similar performance.

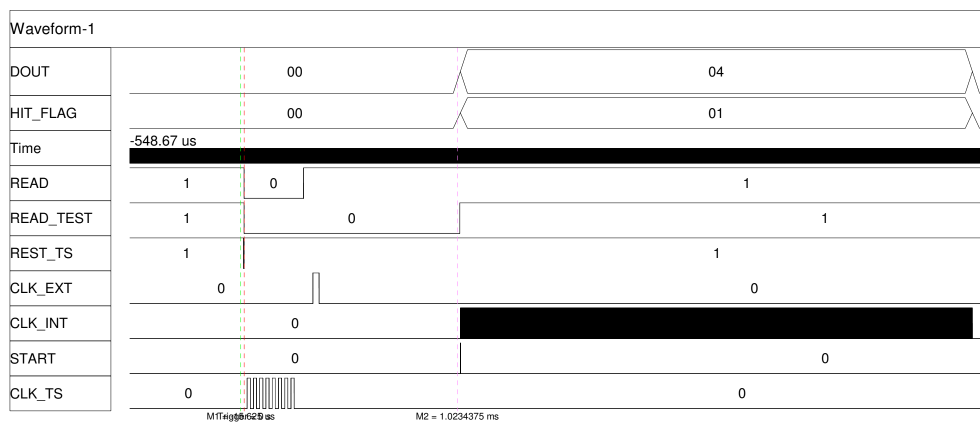
The injection of digital test patterns can be useful for quick tests of the digital section. This feature can be used to simply verify the functionality of the digital tier. During the detection phase, the 5-bit gray codes are sent to each pixel. The time stamping of the emulated hit is latched by the time stamping registers. During the readout phase, all outputs of digital pixels are shifted out serially, i.e. the 7-bit binary codes containing 5-bit time stamping and 2-bit flags are read out.

Test results are shown in Figure 3.11. When only one emulated hit is injected, the flag represents an accurate output code of '01'. When two hits are injected, the flag shows the corresponding binary code of '10', and the time stamping is not changed until the time stamping registers are reset at the next acquisition phase. If there are no hits injected in the pixels, the output code of the flag is always '00'. Since the time stamping registers are not triggered, the time stamping is in a format of '00000'. The pixels of the digital tier were tested, and found to be functional in the standalone test mode. Among three CAIRN-1 chips tested, only 0.1% of all pixels were found dead for unclear reasons.

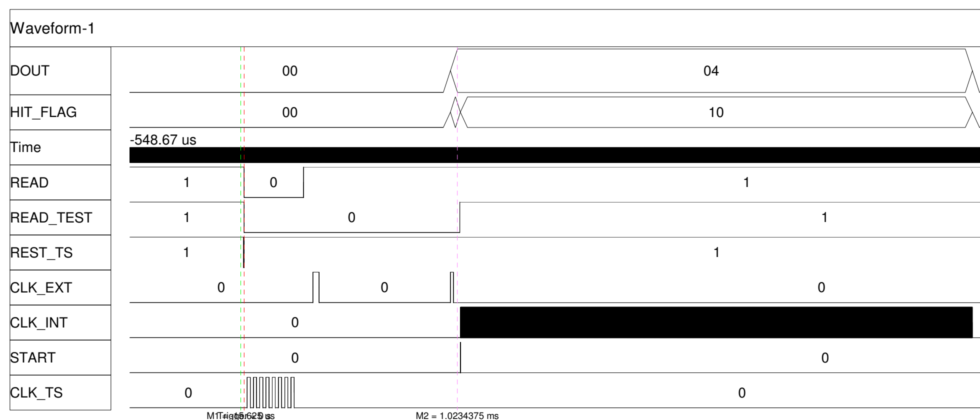
Finally, the power consumption of this chip was measured and found to be ~ 20 mW (only the power consumption of the digital tier). This value agrees well with the one simulated, and corresponds to < 7 mW/mm^2 and to < 1 μW per digital pixel. This



(a)



(b)



(c)

Figure 3.11: Measured waveforms of circuits on the digital tier, when (a) no digital pulse is injected, (b) one digital pulse standing for a hit is injected into each pixel, and (b) two digital pulses standing for two hits are injected into each pixel.

latter value reflects that the power consumption of the digital pixels is not a main power source w.r.t that of the analog pixels. In the other words, the delayed readout may show a promising advantage over low power consumption. In the future, our research should focus on the design effort needed for reducing the power consumption of the analog part.

3.5.4 Discussion

Such 3D devices were manufactured by using 3D Tezzaron integration technology to stack with two tiers of 130 nm CMOS Chartered process wafers. Unfortunately, the fabrication of 3D chips encountered some issues [59], so we just received a misaligned 2D wafer of the digital tier two years after the submission. The functionalities of the circuits in this 2D chips have been verified to work as expected. In May 2011, 30 single wafers were produced, but only 3 bonded wafer pairs of poor quality were accepted up to now. The major problem may be misalignment of the tiers, leading to top tier removal during thinning process. The complete characterization of real 3D devices have to wait until the complete 3D chips are fabricated successfully.

In order to develop the novel architectures of 3D integrated pixel sensors, we had to change the design strategy. It was decided to first verify the functionalities of the non-detecting circuits using the standard 2D CMOS Chartered technology. If the corresponding IC circuits of analog and digital pixels will come out functional as expected, their integration in a single chip using 3D interconnection technologies may be predicted. Meanwhile, we also can compare the performance between the previous 2D chips and real 3D chips. Therefore, our proposed designs mentioned in the following chapters will be based on this idea.

3.6 Conclusion

A 3-tier CMOS pixel sensor featuring a 12 μm pitch has been proposed in this chapter. This small pixel pitch was chosen for keeping low probability ($\lesssim$5 %) of firing the same pixel more than once in the same train. Moreover, a 12 μm pitch also can guarantee a high spatial resolution of 2-2.5 μm in case of binary charge encoding.

Since the first submission of the 3D integrated chips was limited to two tiers, we made a simplified design where the pixels of the top tier (detection tier) and intermediate tier (analog signal processing) were in fact integrated on the same tier. They form a 12 μm $\times$ 24 μm cell resulting from twice 12 μm $\times$ 12 μm element units. Even with

a twice larger pixel area, only a 5-bit time stamping (i.e. time resolution of $\sim$ 30 μs) accompanied by a flag latch could be implemented.

The analog front-end includes a diode, a shaping amplifier and a discriminator. It converts the charge of an impinging particle into a binary output signal. The cell operation was simulated, leading to an average power of $\sim$ 7.5 μW predicted per analog pixel. The simulated CVF of the shaping amplifier is $\sim$ 250 μV $/e^-$. The predicted ENC amounts to $\sim$ 20 e^- , and the discriminator threshold dispersion amounts to $\sim$ 23 e^- . The noise of a preamplifier followed by a simple shaper has been studied. It allows an optimization of noise for a given detector capacitor by an appropriate choice of the current. More current of the shaper is needed for faster shaper with shorter peaking times but the minimal noise value remains unchanged. The contributions to threshold dispersion come from the device mismatch in the shaping amplifier and discriminator; an optimized design of this analog front-end is being investigated. Because of the limited pixel area (12 μm pitch), the development of a single-ended analog front-end without a calibrated pixel-level DAC is still primary.

Prototypes of the proposed 3D-CPS were partly characterized. The test results show a full function of the circuits on the digital tier. It also should be noted that a small pixel (12 μm) in the same active area translates in a modest power consumption. Using this CMOS technology, each 3D integrated pixel cell consumes an average power of $\sim$ 10 μW, the sensor power dissipation is $\sim$ 7 W$/cm^2$. The chip of 3D-CPS introduced in this chapter is a prototype, not taking a full advantage of a delayed readout. The reduction of power consumption is another concern in this design, the main contribution originally comes from the analog part.

In the near future, the fabrication of the 3-tier CPS with a 12 μm pitch will be completed: in this design, the current analog tier is split into two different tiers reflecting their functionalities. In order to realize a 7-bit time stamping (corresponding to a time resolution of $\sim$ 7.5 μs), another CMOS process with smaller feature size (e.g. $\lesssim$65 nm) will presumably be needed for the digital tier. Although this delayed readout architecture is a very attractive candidate for the innermost layer of the ILD vertex detector, the required 7-bit high-precision time stamping is difficult to obtain with a pixel pitch of only 12 μm . The alternative approach, based on a continuous readout architecture was therefore also investigated in this thesis. It will be developed in the next chapter.

Chapter 4

3D integrated CMOS pixel sensors with a continuous rolling shutter readout

In the previous chapter, we have investigated a delayed readout architecture of 3D integrated CPS for the innermost layer of the ILD vertex detector. The essential advantages of this readout architecture have been explained. In this readout architecture, each pixel implements a discriminator and a 5-bit time stamping latch. A main limitation of this readout is the high power consumption, because all pixels in the whole matrix have to be switched on during the detection phase. Another limitation is that a sufficient time stamping requires too many transistors, which may impose a relatively large pixel pitch, depending on the manufacturing feature size.

2D-CPS typically utilize a rolling shutter, where the pixels in the array are selected row-by-row sequentially from top to bottom. The rolling shutter takes the great advantage of saving the power of the pixel array at the expense of the readout speed. A new strategy was devised for the rolling shutter readout as advanced (3D) interconnect technologies allow for a higher degree of parallelism to speed up. The whole pixel array can be divided into several subarrays that are read out in parallel, squeezing the readout time of the pixel array to that of a subarray. As compared to the delayed readout approach, the benefits of a parallel rolling shutter readout are explained and analyzed in this chapter.

In section 4.1, we will first introduce the parallel rolling shutter readout and its advantages in 3D-CPS. In sections 4.2 and 4.3, the main research interest will focus on discussing the pixel design, i.e. a high speed and low offset pixel-level discriminator and a pixel-level zero suppressing readout circuit. A proof-of-concept 2D chip was fabricated for verifying the functionalities of the proposed pixels, the simulation and experimental results are presented and compared in section 4.4. Finally, the conclusion and future

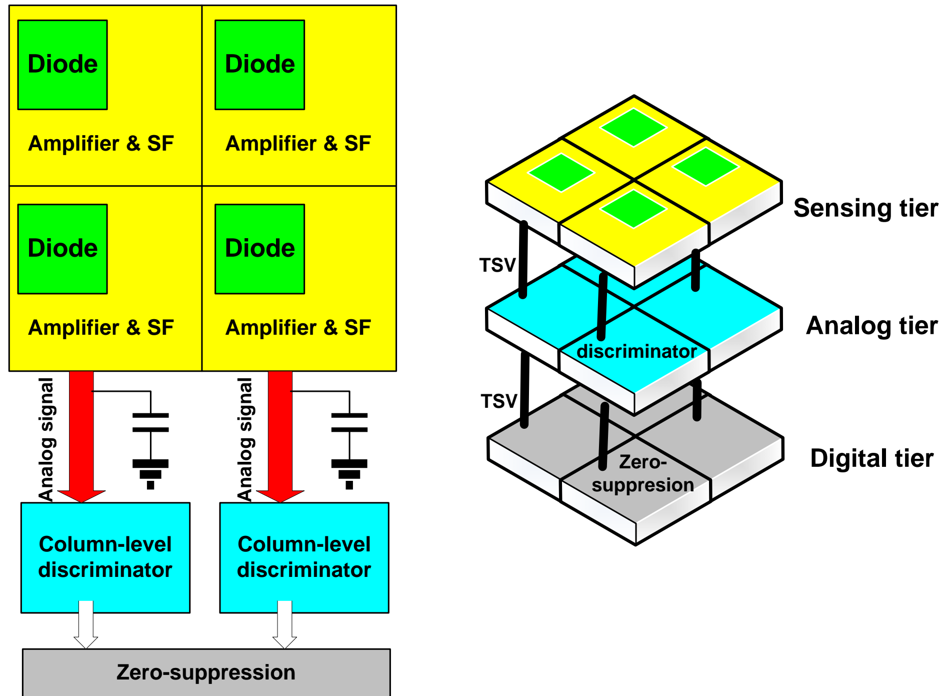


Figure 4.1: A 2 × 2 pixel array of 2D-CPS (left) and a 2 × 2 pixel array of 3D-CPS (right).

plans are given in last section.

4.1 3D integrated CMOS pixel sensors based on a continuous readout

The rapid review of the performance of MIMOSA-26 sensors clearly indicates the pressing need to achieve a faster readout speed, which is also one of the motivations of developing a double-sided ladder. With the column-level processing like that of MIMOSA-26, the pixels (grouped in columns) are read out row by row and routed onto the column level discriminators. These pixel signals need to be buffered for driving a parasitic capacitor[1] at each column. With this typical continuous readout mechanism discussed in chapter 2, the readout speed strongly depends on the row processing time and on the number of rows in the pixel array. On the other hand, either a shorter row processing time or a reduced number of rows can improve the readout speed.

Using two or more vertically interconnected pixellated chips, more intelligence per pixel can be integrated with different CMOS manufacturing processes. Therefore, 3D-

[1]The capacitor consists of the parasitic capacitor of a long routing metal line and the switching capacitor.

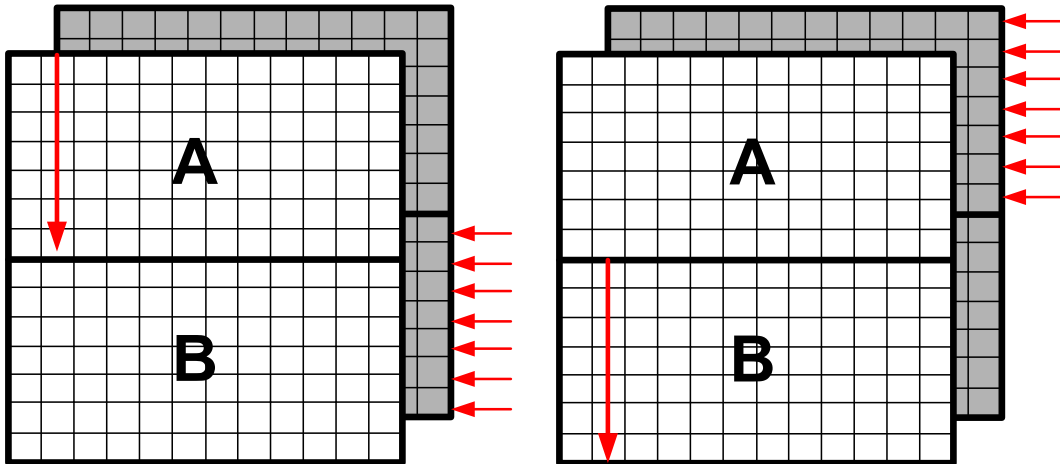


Figure 4.2: Left and right figures illustrate how to work in every subarray of 3D-CPS, where each subarray is divided into two halves.

CPS with small pitch pixels are capable of handling high data rates. Vertical integration allows for a separation of the sensor, the analog front-end electronics and the digital readout sections. The short connections between them offer very small parasitic capacitance ($\sim$ a few fF), as shown in Figure 4.1. The readout speed can be increased by at least one order of magnitude, as compared to the ordinary 2D-CPS. Each chip (tier) is optimized for a given part of the charge generation or signal processing chain.

In this chapter, we present plans of designing a 20 μm pitch 3D-CPS with the following functionalities: detection with analog processing on the top tier, pixel discrimination on the intermediate tier and zero suppressed readout on the bottom tier. It is planned to fabricate the proposed 3D-CPS by using two different CMOS technologies and two different wafer bonding techniques [60]. A CMOS process with a high resistivity epitaxial substrate is used to fabricate the sensor tier (top tier), which is vertically connected to a 2-tier CMOS readout electronics chip. Two tiers (wafers) of this chip are manufactured in a 0.13 μm CMOS Chartered technology and vertically integrated by 3D-Tezzaron technology [61, 62]. The connection of the different tiers is performed by Through Silicon Vias (TSVs).

The whole pixel array is divided into several subarrays, each being split into two halves (i.e. group A and group B). Since the rolling shutter operation has to be compliant with zero suppressed readout, these two operating procedures are consecutively alternated between group (A) and group (B). The working principle of a subarray is illustrated in Figure. 4.2. In the group (A), the pixel signals of selected row are amplified on the top tier and discriminated on the intermediate tier. Binary data values are directly buffered

into in-array storage on the bottom tier before being read out. In the group (B), the zero suppressed readout simultaneously extracts the stored hit patterns of the previous frame in the rows parallel, and vice via.

The zero suppression circuitry, now distributed into the pixel array instead of being located in the periphery of the pixel array, is no more constrained by the row processing time. Instead, it saves half frame readout time to encode patterns of hits. The relaxed timing constraints allow for addressing a much higher hit density, which can be estimated from a statistical study based on the highest occupancy expected in the pixel array.

4.2 High speed pixel-level discriminator

The pixel cell of the top tier includes a diode and a common source (CS) amplifier. The output of the latter is connected to the pixel-level discriminator integrated on the intermediate tier. By embedding a discriminator into this pixel for analog-to-digital conversion, the output of the pixel is transformed into a boolean information. The binary outputs of the pixel-level discriminators are passed through the silicon wafer to the bottom tier by TSVs.

A high-gain cascaded amplifier was designed as a pre-amplifying stage of the pixel-level discriminator. The block diagram of this discriminator, consisting of an auto-zeroed pre-amplifying stage and a dynamic latch, is shown in Fig. 4.3. An all NMOS-transistor architecture was proposed for another possible 2-tier 3D-CPS [63], where the discriminators can be integrated on the sensor tier without degradation of the detection efficiency.

The offset voltage of a multi-stage amplifier can be canceled by an output offset storage method [64]. To minimize the reset noise (or KTC noise) of the switches, this multi-stage amplifier leaves the offset cancellation mode sequential; $Clamp1$ first and $Clamp4$ last. The input referred residual offset V_{offset} of this discriminator is given by

$$V_{offset} = \frac{V_{OSL}}{\prod_{i=1}^{4} G_0[i]} + \sum_{i=1}^{4} \frac{\Delta Q[i]}{C[i] \prod_{j=0}^{i} G_0[j]} + \frac{\Delta Q[Clamp]}{C[1]} \tag{4.1}$$

where V_{OSL} is the input referred offset of the latch, $G_0[i]$ is the static gain of the i-th stage of the CS amplifier, $\Delta Q[i]$ is the charge injection from the NMOS switch of the i-th stage, and $\Delta Q[Clamp]$ is the charge injection of the first $Clamp$ switch. $C[i]$ is the capacitor of the i-th stage. Note that the input referred offset voltage is attenuated by the gain of the overall chain. However, the reset noise of the $Clamp$ switch resetting the

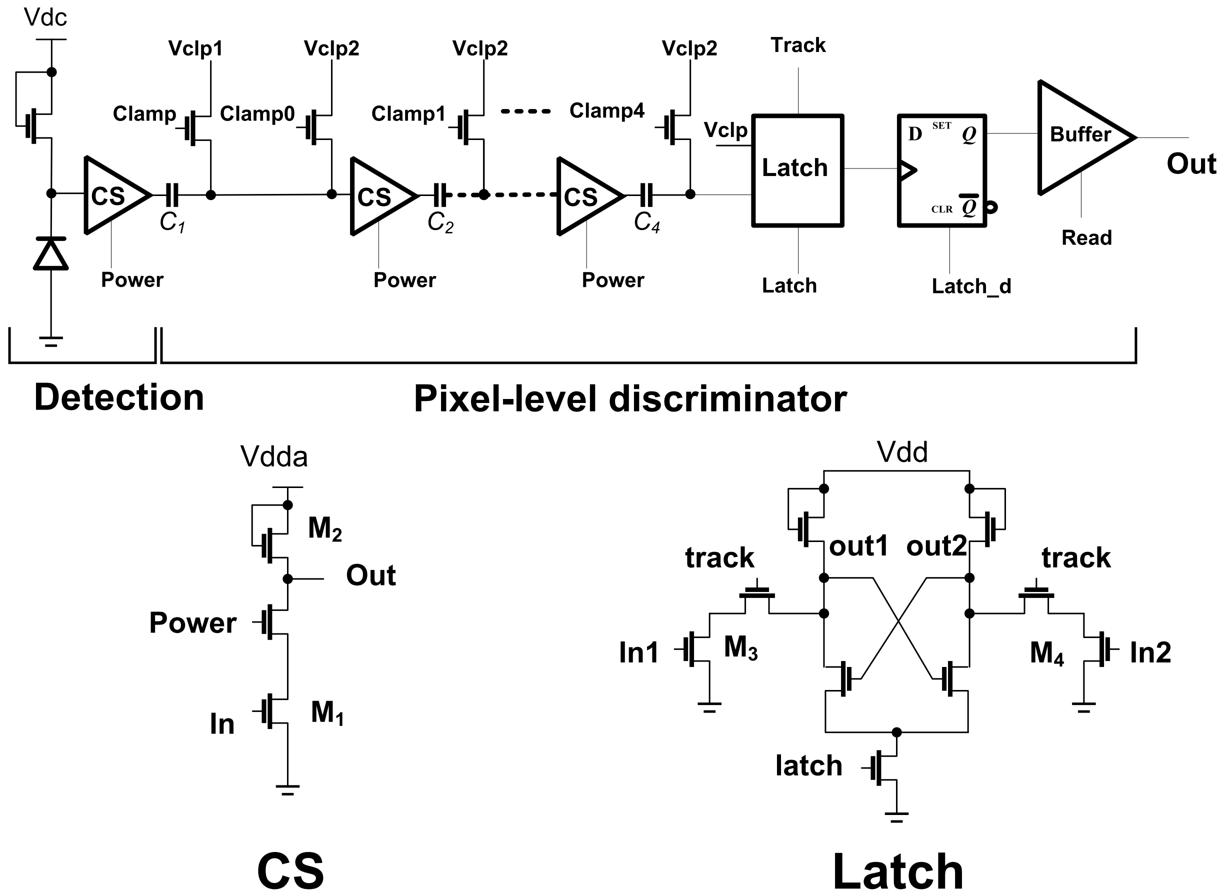


Figure 4.3: Schematic of the proposed pixel-level discriminator (up), schematic of common source amplifier and dynamic latch used in the pixel-level discriminator (down).

coupling capacitor (C_1) remains, but this result can be reduced by an appropriate choice of capacitor [65].

The cascade of low-gain amplifiers allows for a high operation speed together with a high gain. The static voltage gain of each stage is about 4, yielding a gain larger than 200 for the cascade of four stages. The implemented dynamic latch has no static power consumption, its detailed schematic is also shown in Figure. 4.3. The total static power consumption of each discriminator is about 120 μW .

The timing waveform for the pixel-level discriminators is shown in Figure. 4.4. The discriminators are switched on by the $Power$ signal, the hits are stored in latches. The $Read$ signal is used to enable a tri-state buffer for reading out the stored binary output of the last frame. Therefore, two phases are needed for a complete offset cancellation and signal discrimination:

- During T_1 (calibration phase), the offset of each stage is stored on the output

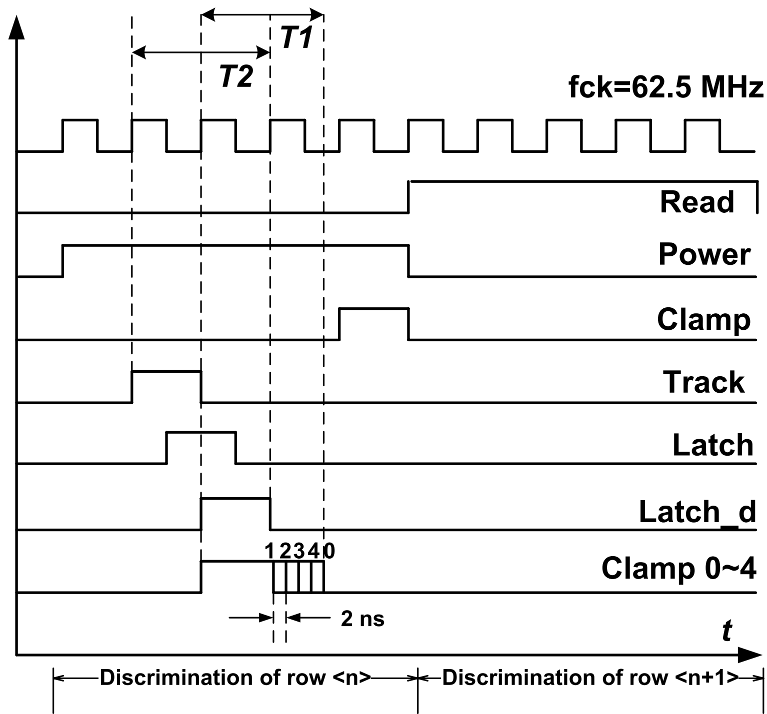


Figure 4.4: Time waveform of the proposed pixel-level discriminator.

capacitances, this offset is corrected, as illustrated in (4.1). Afterwards the $Clamp$ signal delivers immediately a DC voltage V_{clp1} that is different from the voltage V_{clp2}, V_{clp2} is a DC voltage for biasing the four-stage amplifier. The threshold level is defined by V_{th}=V_{clp1}-V_{clp2}, it is stored in the first sampling capacitor.

- During T_2 (discrimination phase), the $Track$ switches are turned on, the subtraction of the stored threshold voltage and input signal is performed, the difference is amplified by the multi-stage amplifier and the resulting logical state is latched and memorized by $Latch$ and $Latch_d$ signals. During the $Read$ phase, the latch is designed to produce logical levels at the output. If the difference is positive, the output of the latch is "1"; otherwise, it is "0".

In the conventional methodology, the pixel signal is read out to a large column bus capacitance which is in the order of pF for the case of one hundred rows [66]. Note that the settling time of the pixel signal decreases as power consumption increases due to the adverse affect of the column-level parasitic capacitance. Pixel-level signal processing helps to overcome the limitations due to much smaller pixel-level parasitic capacitances ($\sim$ a few fF). The readout of the architecture therefore gets accelerated, this contribution comes from two times shorter row processing time ($\sim$ 100 ns) w.r.t the row processing

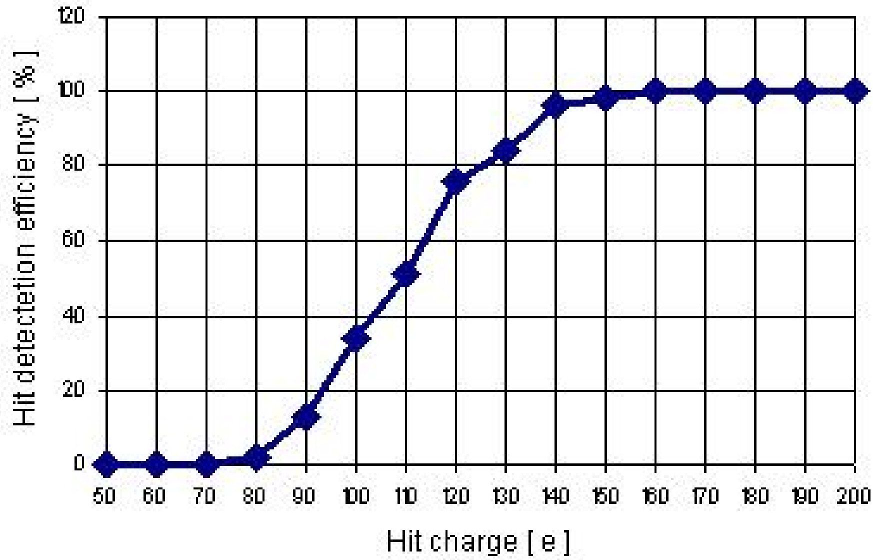


Figure 4.5: The simulated firing efficiency of the proposed pixel-level discriminator.

time of MIMOSA-26 sensors.

In the conventional 2D-CPS designs, a relatively large current is required to drive the column-level parasitic capacitor for maintaining a satisfactory signal-to-noise ratio of the pixel signals, this extra power consumption can be saved in 3D-CPS. As a reference of MIMOSA-26 sensors, the consumed current of the in-pixel amplifier is about 10 μA. The common source follower (i.e. analog buffer) consumes about the current of $\sim$ 50 μA to drive a large column-level parasitic capacitor of $\sim$ 8 pF. The average current of the column-level discriminator is in the order of $\sim$ 70 μA. Therefore, the total average current of the signal processing chain is about 120 μA.

In our design, the analog-to-digital conversion is performed at the pixel level rather than the column level. The source followers consuming such extra power are not required to provide the signal buffering. The average current of the pixel-level signal processing chain is only 65 μA. The total average power consumption is reduced by a factor of $\sim$ 2. Therefore, the in-pixel digital outputs make the continuous (or called rolling shutter) readout more amenable to development of low-power CPS, for it eliminates the analog readout bottlenecks.

Tests of MIMOSA-26 sensors in both the laboratory and particle beams show excellent results, which have been introduced in chapter 2. The behavior of the column-level discriminators isolated from the pixel array was studied on MIMOSA-26 sensors. The temporal noise and FPN values of the column-level discriminators amount to 0.3 mV and

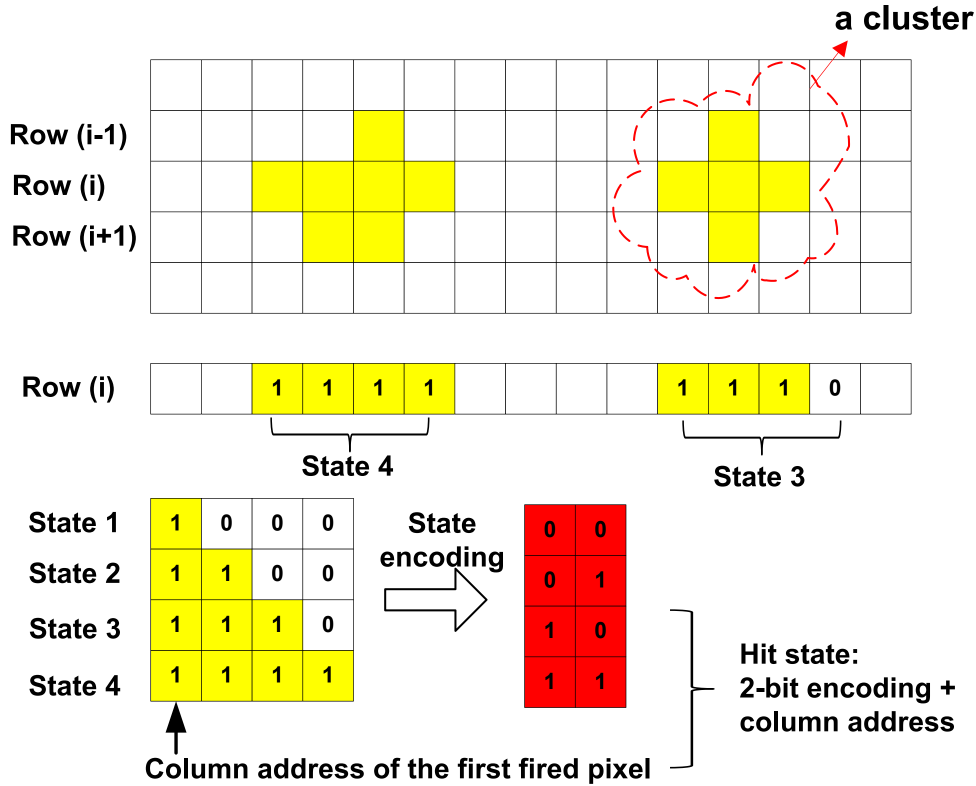


Figure 4.6: Schematic view illustrating the encoding of the pixels delivering a signal above discriminator threshold.

0.2 mV, corresponding to 9 e^- and $6e^-$ respectively. In this case, the noise performance of the pixel-level discriminators should be comparable with that of the column-level discriminators, widely used in 2D-CPS. The firing efficiency of the pixel-level discriminator with the sensing diode, shown in Figure 4.5, was simulated as a function of the input signal magnitude expressed in electrons. The firing efficiency gives the simulated temporal noise of $\sim 10\ e^-$ and FPN of $< 10\ e^-$, which meet the design goals.

4.3 Pixel-level zero suppressed readout

Figure 4.6 shows an example of the pixel array on the bottom tier with some hits. Beam tests with 20 μm pitch CPS have shown the average length of a cluster is less than four pixels in a row. Therefore four successive pixels are required to generate the "cluster information". The cluster information includes the column address of the first fired pixel and a two-bit encoding, which represents the number of the fired pixels in a four-pixel group, as expressed in (4.2) and (4.3).

Figure 4.6 shows an example of the pixel array on the digital tier with some hits. Since the average length of a cluster is less than four pixels with a 20 μm pitch in a row [67], four successive pixels are required for predicting a so called "hit state". Its format includes the column address of the first fired pixel and a two-bit encoding, which represents the number of the fired pixels, as expressed in (4.2) and (4.3). A condition of identifying the i-th pixel as a hit state is that disc(i) and disc(i-1) are the logical one and zero respectively. The two-bit encoding gives the status report of three preceding pixels (i+1, i+2, i+3).

$$code0(i) = disc(i+2) \cdot disc(i+1) \tag{4.2}$$

$$code1(i) = [disc(i+1) \cdot \overline{disc(i+2)}] + [disc(i+2) \cdot disc(i+3)] \tag{4.3}$$

where $disc(i)$ is the discriminator output signal of the i-th pixel. $code0(i)$ and $code1(i)$ are the most significant- and the least significant-bits encoding the number of contiguous pixels receiving signals above threshold.

A condition of identifying the i-th pixel to be the first pixel in a cluster (i.e. the seed of the cluster) is that disc(i) and disc(i-1) are the logical one and zero respectively. The rare cases of overlapping clusters can not be excluded, they may lead to the number of contiguous fired pixels larger than four in a row. To account this, we will also consider the i-th pixel to be the seed of a cluster if the previous four pixels are fired and the dis(i) is the logical one.

Note that the hit information uses fewer bits than the original representation for reducing the raw data flow. The zero suppression is preformed based on a sparse-scan readout scheme. When an individual pixel identifies itself as the cluster of a seed, it is able to trigger the readout of their hit information by generating a signal, named *token*.

$$token(i) = disc(i) \cdot [\overline{disc(i-1)} + disc(i-1) \cdot disc(i-2) \cdot disc(i-3)] \tag{4.4}$$

where $token(i)$ represents an enabling signal of the i-th pixel. The disc(0,1,2) signals in each row are the logical zeros for initiating the readout. Using De Morgan's theorems, the previous expression can be simplified as follows:

$$token(i) = disc(i) \cdot \overline{[disc(i-1) \cdot \overline{[code0(i-4) \cdot disc(i-4)]}]} \tag{4.5}$$

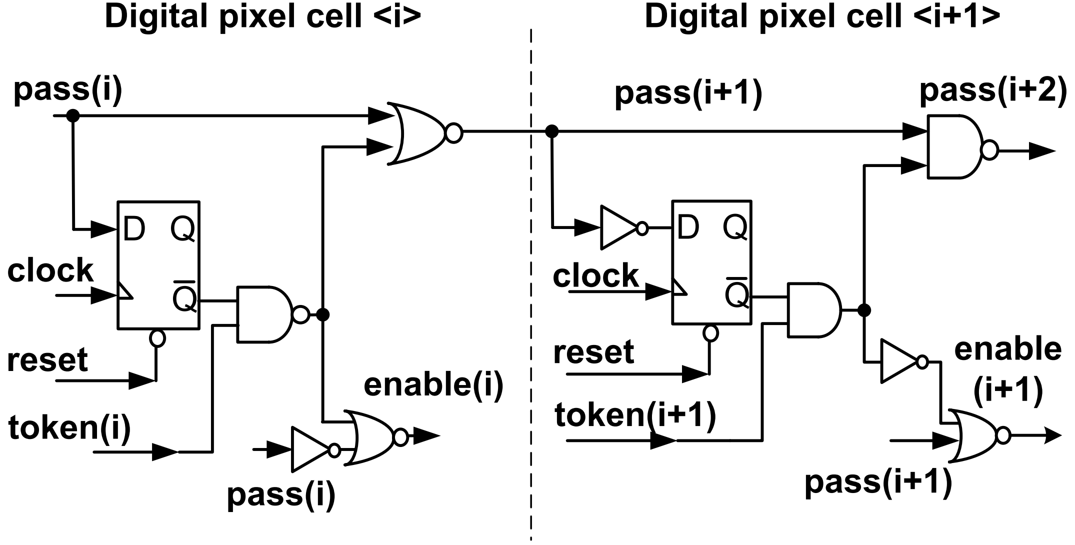


Figure 4.7: Sparse scan logic implemented in the i-th and (i+1)-th pixel cells of the bottom tier.

In order to provide effectively a non-redundant encoding, instead of checking the discriminator value of the fourth pixel ($disc(i-4)$), we recursively check whether this pixel element generates the $token$ signal or not. Therefore, the hit identification logic has been slightly modified:

$$token(i) = disc(i) \cdot [\overline{disc(i-1) \cdot [\overline{code0(i-4) \cdot token(i-4)}]}] \tag{4.6}$$

here we defined:

$$\begin{aligned} state(i-1) &= \overline{disc(i-1) \cdot [\overline{code0(i-4) \cdot token(i-4)}]} \\ &= \overline{disc(i-1)} + code0(i-4) \cdot token(i-4) \end{aligned} \tag{4.7}$$

From(4.7) $force(i)$ can also be defined as:

$$force(i) = code0(i) \cdot token(i) \tag{4.8}$$

and then (4.7) yields

$$state(i) = \overline{disc(i)} + force(i-3) \tag{4.9}$$

Each pixel has a sparse-scan bank that is used to skip unfired pixels, to find the first "cluster seed" in a row and to activate the readout of the hit information generated by

this seed. It has only one flip-flop, initially reset to zero by the $reset$ signal. The sparse scan is implemented using a signal, called $pass(i)$, that is loaded into the flip-flop on the rising edge of the $clock$ signal. The $pass$ signal is propagated through a chain of intertwined NOR and NAND gates (see Fig. 4.7). We have therefore two types of digital pixel cells on the bottom tier, one based on NOR (e.g. the i-th pixel) and the other based on NAND (e.g. the (i+1)-th pixel). This realization of the chain requires the minimum number of gates.

Let us now consider the cell based on NOR: The pass input (i.e. signal $pass(i)$) being equal to logical one indicates that there are seed pixels with a higher hierarchy than the i-th pixel. Only if the i-th pixel identifies itself as a seed (i.e. $taken(i)$=1), and $pass(i)$ is logical zero. The $enable(i)$ signal, acting as an enable for reading out the hit information during the sparse-scan, is active.

Every pixel in a row communicates with its three following pixels $(i+1, i+2, i+3)$

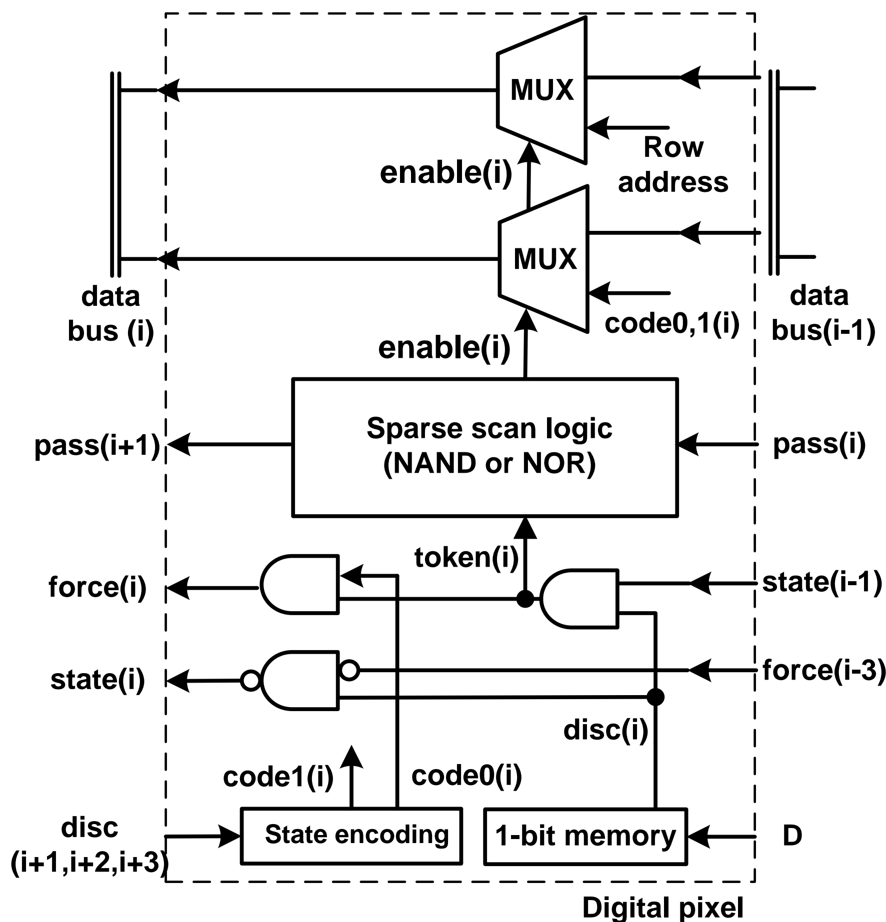


Figure 4.8: Schematic of the digital pixel cell (i).

to determine the state of the hits (i.e. the number of the pixels in the cluster). It also receives $force(i-3)$ and $state(i-1)$ signals from the previous pixels. These signals are used to identify a seed. The schematic of the i-th pixel cell was designed as shown in Fig. 4.8.

4.4 Readout controller design

The minimum number of buffers in each row allowing keeping a low probability ($< 10^{-3}$) of missing hits was derived from physics simulations. For every token clock cycle, new hits data are always stored in the first empty buffer, and then with the content of all hits being shifted from one buffer to the next. After all token clocks, all valid hit states have been stored in the buffers. Meanwhile a hit counter (CNT) increments the number of valid hits as long as the token injected into the row has not been returned [68].

The row buffers are implemented as scan flip-flops, their hit information being shifted row by row during the readout phase. The chip-level readout controls the operation of data transmission. A finite state machine (FSM) calculates exactly when to request a new row from the number of valid hits.

The chip level readout controller illustrated in Figure 4.9 collects hit information from the buffers and sends them out of the chip. To avoid waiting clock cycles during the request of a new row, the pipeline extends two stages, allowing the FSM to read the hit states in a pair of 16-bit FIFO memories. The readout FSM starts by asynchronously scanning through the hit counters of the row segments, and selects serially the valid hit states of the previous frame. If a hit information is extracted from the sub-array, the hit counter is decremented by two in the selected sub-array. The content of row buffers is shifted by two places. Finally, after decrementing and shifting, the procedure can be repeated until the state of counters becomes equal to zero.

4.5 Circuit implementation

In order to save the cost and time and to reduce the exploration risk of 3D integration, this chapter presents a 2D proof-of-concept design to verify the functionalities of the readout electronics chip as an experimental attempt. The prototyping strategy is therefore to spread out the 2-tier CMOS readout electronics on a 2D Chartered wafer. First test results on readout electronics (i.e. pixel-level discriminator) are presented in

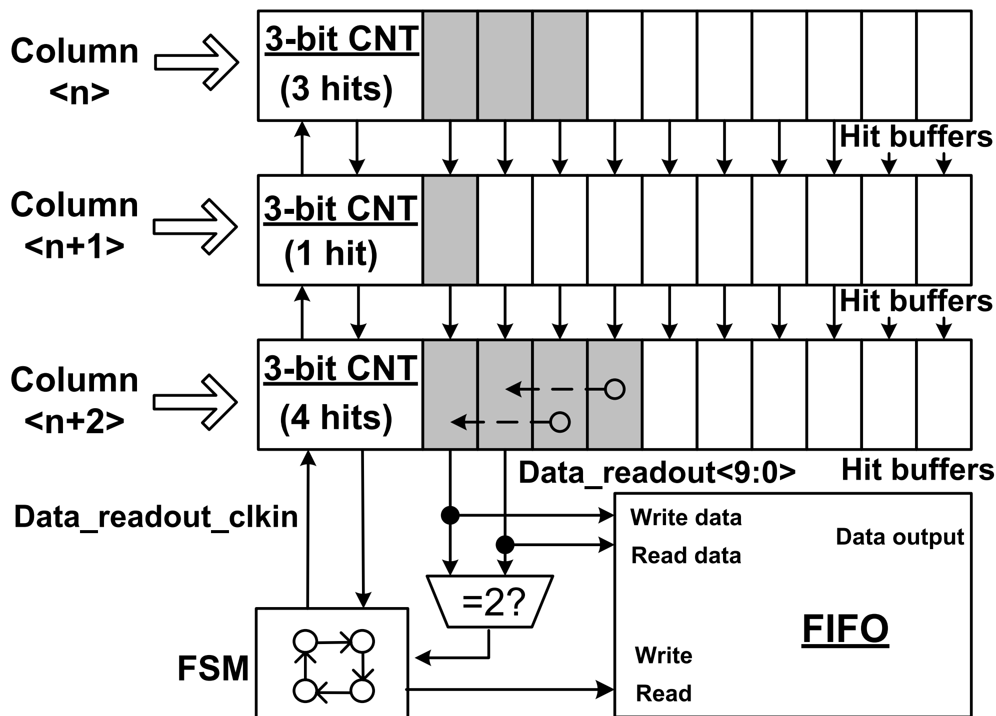


Figure 4.9: Chip-level readout controller. Example where 3, 1 and 4 hits were detected in 3 continuous columns. The states of a hit counter are decremented by two, and the remaining contents of row buffers are shifted to the neighboring two buffers.

this chapter, they will determine the flexibility and adaptability of a future 3D integrated chip with full sensor functionality.

The chip implements a 20×10 pixel array on a 1×1.16 mm^2 core. It has been extensively tested, the electrical performance of different functional blocks were examined individually, the pixel-level discriminators being designed with dedicated test structures. Several test groups were designed for minimizing the noise of the discriminators, three types of transistors with the different noise characteristics were implemented in three main blocks of the discriminator (i.e. the first clamping capacitor, the multi-amplifier and the latch) (see Table 4.1). The micro photograph of the chip and its test board are shown in Figure 4.10.

The outputs were connected to a simple digital multiplexer directly via the output pads. The functionality of the pixel-level discriminators was studied with a main clock frequency of 12.5 MHz (i.e. a row processing time of 80 ns). The firing efficiency of discriminators is measured by scanning the threshold voltage while keeping a stable voltage for inputs [69]. A digitizing scope is used to visualize the output of the comparator and also to compute the average number of "1" over a significant number of cycles for each

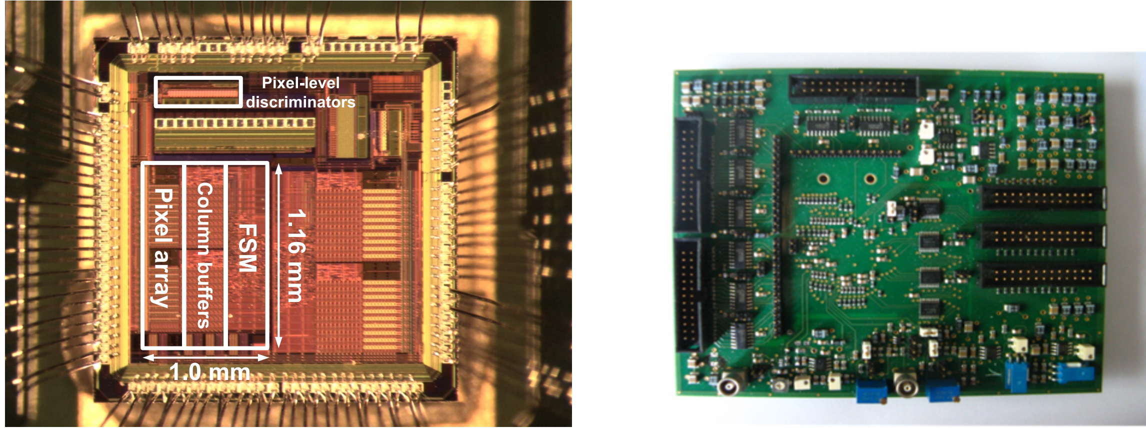


Figure 4.10: Micro photograph of the proof-of-concept chip (left) and its test PCB (right).

threshold value. The threshold of a pixel is measured by the fraction of detected hits as a function of the injected charge - S curves. In the reality, the electronic noise introduces the fluctuations on the signal voltages, and the amplitude of the fluctuation is Gaussianly distributed. Therefore, the possibility of hits to exceed the threshold can be described by the convolution of a step function and a Gaussian distribution, which turns into a complementary error function (Erfc).

Table 4.1: Different types of transistors used in three main blocks of the pixel-level discriminator, as shown in Figure 4.3. "native" means a transistor with nearly zero threshold voltage; "lvt" means a transistor with low threshold voltage. "NMOS 1.5" is a normal NMOS transistor adopted to use 1.5 V power supply, "NMOS 3.3" is a normal NMOS transistor adopted to use 3.3 V power supply.

Groups	M_1/M_2	M_3	C_1 (NMOS capacitor)
N1	NMOS 1.5/NMOS 1.5 (native)	NMOS 1.5	NMOS 1.5 (lvt)
N2	NMOS 1.5/NMOS 1.5 (native)	NMOS 3.3	NMOS 1.5
N3	NMOS 3.3/NMOS 1.5 (native)	NMOS 1.5	NMOS 1.5 (native)
N4	NMOS 3.3/NMOS 1.5 (native)	NMOS 3.3	NMOS 3.3
N5	NMOS 3.3/NMOS 1.5 (lvt)	NMOS 1.5	NMOS 1.5 (lvt)
N6	NMOS 3.3/NMOS 1.5 (lvt)	NMOS 3.3	NMOS 1.5
N7	NMOS 1.5/NMOS 1.5 (lvt)	NMOS 1.5	NMOS 1.5 (lvt)
N8	NMOS 1.5/NMOS 1.5(lvt)	NMOS 3.3	NMOS 1.5 (native)

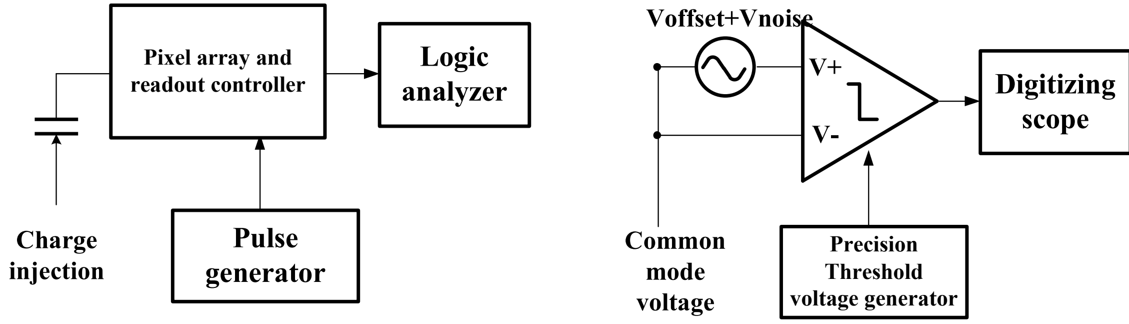


Figure 4.11: Test benches of the pixel-level zero-suppressing readout (left) and pixel-level discriminator (right).

$$P(Q_{inj}) = \frac{1}{2}erfc(\frac{Q_{th} - Q_{inj}}{\sqrt{2} \cdot \sigma_{noise}}) = \frac{1}{\sqrt{\Pi}} \int_0^{\infty} exp(\frac{Q_{th} - Q_{inj}}{\sqrt{2} \cdot \sigma_{noise}})dQ \tag{4.10}$$

where Q_{th} is the threshold, Q_{inj} is the injected charge, and σ_{noise} is the sigma of Gaussian distribution.

The full width of the S curve at half the maximum is ∼2.35 σ_{noise}, and its mean gives the residual offset of the discriminator, where the σ_{noise} is the temporal noise [70]. By plotting the histogram of the offsets of all discriminators, the mean threshold and the threshold dispersion σ_{th} can be obtained. The FPN is defined as the threshold dispersion, which has a similar effect as noise besides it can be treated as a time-independent noise source.

During the measurements, the selection of the threshold value is very important because it influences the detection efficiency and the fake hit rate. When there is no input signal, the random response of the discriminator could be either "1" or "0", the "1" is sometimes caused by noise. By increasing the threshold voltage, the probability of "1" caused by noise can be reduced but the minimum detectable signal will be larger, it means the sensibility of the discriminator is limited. Therefore, the detection efficiency will degrade.

4.5.1 Experimental results of the pixel-level discriminators

In our test bench, the inputs of the discriminator are shorted to a common-mode voltage and different threshold voltages are applied, as shown Figure 4.11. For each pixel-level discriminator, the number of "1"s over 2000 events has been calculated for each threshold value. Figure 4.12 shows the measured firing efficiency of the pixel-level

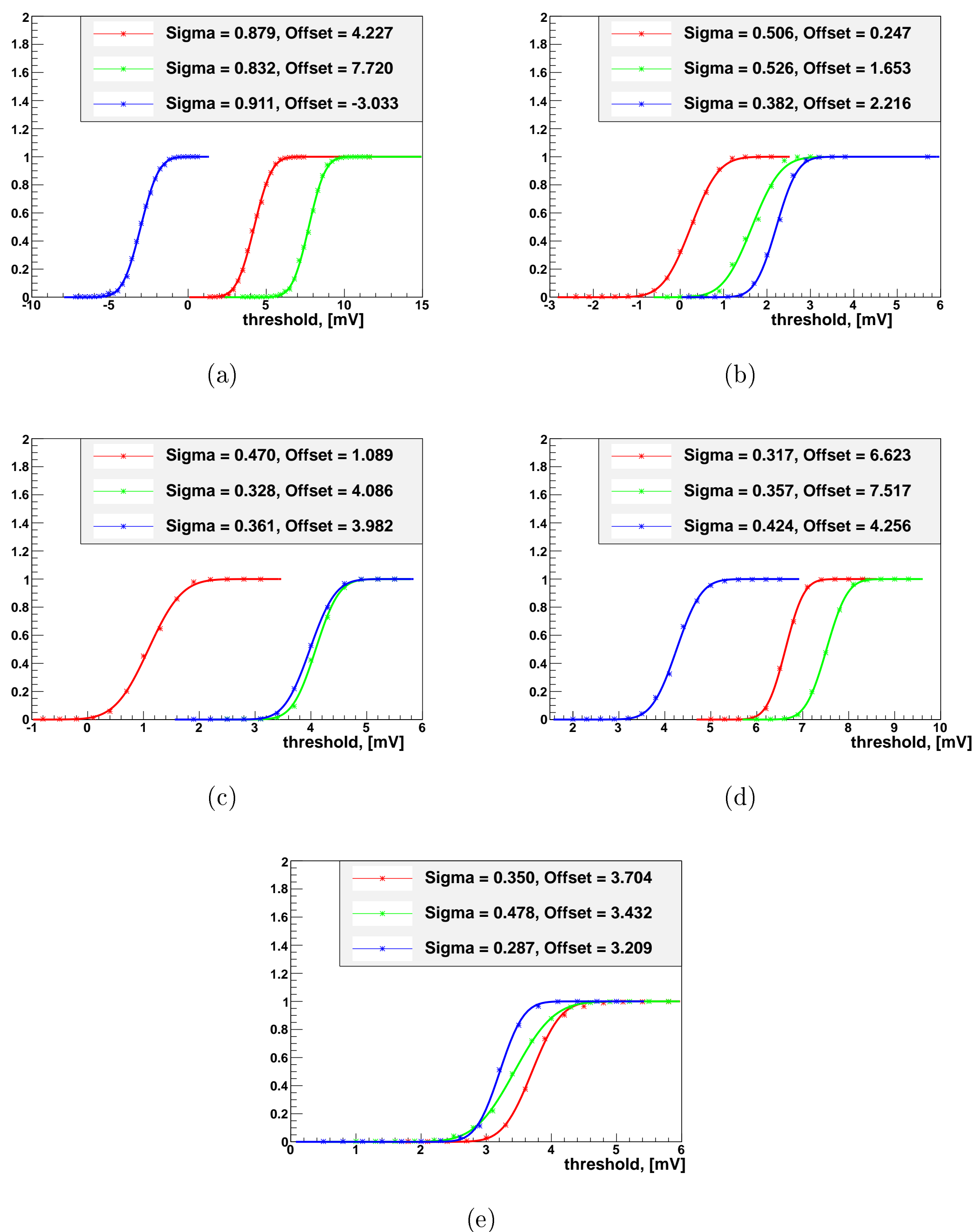


Figure 4.12: The firing efficiency of the pixel-level discriminators versus threshold voltage with the inputs at the same reference voltage. The discriminators were measured at the frequency of 12.5 MHz. The discriminators were designed with different types of transistors, they were classified in different groups (see Table 4.1). (a) N2 group, (b) N3 group, (c) N4 group, (d) N6 group and (e) N8 group.

discriminators versus threshold voltage. The temporal noise and offset distribution of the pixel-level discriminators were achieved.

The offset distribution of test discriminators has been evaluated from one single

Table 4.2: Comparison of simulation results and measurements for 8 different groups.

Groups/noise performance	Temporal noise (simulation/test)	Offset (simulation/test)
N1	0.5 mV/$\sim$ 0.47 mV	$<$ 1 mV/$>$ 100 mV
N2	0.5 mV/$\sim$ 0.8 mV	$<$ 1 mV/$\sim$ 7 mV
N3	0.5 mV/$\sim$ 0.48 mV	$<$ 1 mV/$\sim$ 1.4 mV
N4	0.5 mV/$\sim$ 0.38 mV	$<$ 1 mV/$\sim$ 2 mV
N5	0.5 mV/$\sim$ 0.5 mV	$<$ 1 mV/$>$ 100 mV
N6	0.5 mV/$\sim$ 0.4 mV	$<$ 1 mV/$\sim$ 2 mV
N7	0.5 mV/$\sim$ 0.6 mV	$<$ 1 mV/$>$ 100 mV
N8	0.5 mV/$\sim$ 0.35 mV	$<$ 1 mV/$\sim$ 0.35 mV

chip. The discriminators in the N1, N5 and N7 groups have huge offset voltages of about hundreds of mV, so their S curves are not shown in this section. Temporal noise of the discriminators in most groups is less than 0.5 mV, except the maximum value in the N2 group is found to be about 0.8 mV. Although there is a small number of pixel-level discriminators in this prototype, it is concluded that the proposed pixel-level discriminator operates functionally and provides high enough precision.

Table 4.2 shows a comparison of the noise performance between simulation and measurement. The problem is that in some groups (i.e. N1, N5 and N7), some (or all) of these pixels have large offsets which are in the order of 100 mV. It forces us to resimulate these discriminators for understanding where the offsets originate from. The noise problem was found by performing the transient-noise simulations rather than the Mont-Carlo simulations. The method of the transient-noise simulations is usually used to calculate the reset noise (or KTC). In the proposed discriminator, the reset noise is produced by resetting the coupling capacitor of C_1. It could be extrapolated that the offset voltage contributes from the reset noise of this MOS capacitor.

The MOS capacitor value usually depends on the voltage that is applied to the gate of the NMOS transistor and oxide capacitor per unit area (C_{ox}). A low-threshold NMOS transistor principally has a very small C_{ox}, while an native NMOS transistor has a large one. In our design, a low-threshold NMOS capacitor (see Table 4.1) with a very low capacitor value (only a few fF) is used in the groups of N1, N5 and N7. It results in

an inefficient method of offset cancellation. It could be well understood from (4.1): the lower clamping capacitor value of C_1, the larger offset voltage of the discriminator. On the other hand, a native NMOS transistor can be used as a MOS capacitor, owing to its large capacitor value of $\sim$ 100 fF. The offset voltage can be canceled by the CDS circuitry on the sampling capacitor. The measured results show that temporal noise and FPN (i.e. in N3 group and N8 group with native NMOS capacitors) remain below 0.5 mV and 1.4 mV, respectively. The noise performance of the pixel-level discriminators is therefore at the same level as that of the column-level discriminators successfully used in 2D-CPS [70], as mentioned in the section 4.2.

4.5.2 Lessons learned and future plans

Test results of the pixel-level discriminators show some consequences some of which are mentioned in the following:

- A low noise (i.e. temporal noise of $\lesssim$ 0.5 mV, FPN of $\lesssim$ 1.4 mV) and high speed (i.e. row processing time of 80 ns) pixel-level discriminator has been realized by using the cascaded amplifying architecture.
- The test results showed that the groups N1, N5 and N7 have a huge offset voltage of $\sim$ 100 mV. By re-simulating the pixel circuit, it came out that such offset voltages are not canceled because of a small value of the first MOS capacitor.
- Only 12 test pixel-level discriminators were designed in this prototype, it is difficult to measure the FPN performance. The latter will be verified once a prototype featuring a large enough number of pixels will be submitted.

In this experimental chip, the very encouraging designs of the pixel-level discriminator have migrated from the so far used 130 nm CMOS chartered technology to a specialized 180 nm CMOS technology. This technology allows the PMOS transistors to be used, because the deep P-well layer embedding N-well can host the PMOS transistors. Meanwhile, this squared pixel (16 μm) is elongated by a factor of 4 in a direction (i.e. 16 μm $\times$ 80 μm) for the application of the double-sided ladder, discussed in chapter 2. The pixel-level discriminators are redesigned, most of the problems mentioned above are solved. The new chip including 64 $\times$ 24 pixels was submitted in October 2011. Better noise performance of the pixel-level discriminators is expected, tests of this chip are in preparation.

4.6 Conclusion

3D integrated pixel sensors will unquestionably play an important role in the development of new detectors because they have the potential to satisfy the needs of the next generation subatomic physics experiments. In this chapter, a novel signal processing chain for 3D-CPS architecture has been presented. Taking benefit of segmentation and parallelism, it enables a very efficient method to improve the frame readout time of a very large scale pixel array. In order to demonstrate the pixels functionalities, a proof-of-concept chip was designed and tested.

We have demonstrated the functionality of the high-resolution and high-speed pixel-level discriminators studied up to 12.5 MHz. The measured results show that temporal noise and FPN remain below 0.5 mV and 1.4 mV, respectively. The power consumption of each discriminator is in the order of 120 μW in normal operation speed. A zero-suppression algorithm has been implemented in each digital pixel cell. Furthermore, a fully functional pixel-level zero suppressed readout has also been verified experimentally. The flexibility and adaptability of the proposed approach are suitable for the design and fabrication of actual 3D integrated pixel sensors in the near future.

This readout architecture relies on a very efficient method to short on the frame readout time by taking advantage of 3DIT. The required spatial resolution, which imposes a small pixel pitch is the main limitation of the approach adopted. In order to meet simultaneously the requirements of spatial and time resolution, a 23 μm pitch 3D-CPS with a 3-bit pixel-level ADC will be developed in the next chapter.

Chapter 5

3-bit pixel-level ADCs designed for 3D integrated CMOS pixel sensors

In the previous chapter, 3D-CPS with a continuous readout architecture have been proposed. The advantages of this architecture have been also explained. A 1-bit ADC (discriminator) with a 20 μm pitch may however not allow to reach a high spatial resolution (< 3 μm). Thanks to 3DIT, a full CMOS capability allows for integrating all possible functionalities in a relatively small pixel. Therefore, as a further exploitation of the possible pixel structures, a novel design of a 3-bit pixel-level ADC presented in this chapter will address the mentioned issue. In order to save the sensor power consumption, the proposed pixel-level ADC enables to be read out in a rolling shutter mode.

This chapter is organized as follows: section 5.1 introduces the motivation of integrating ADCs in CPS, whereas section 5.2 and 5.3 explain the designs of the pixel-level ADCs. Section 5.4 shows the test results in terms of dynamic range, noise, nonlinearity and power consumption.

5.1 Motivation of integrating ADCs in CMOS pixel sensors

5.1.1 ADC integration approaches

There are three possible approaches to integrating ADC with CPS. The first is the chip-level approach [71], where a single ADC serves the entire pixel array. This architecture is to integrate a single ADC monolithically along with readout electronics of pixel sensors. Although conceptually simple, a serial single ADC architecture is not the best

option. Firstly, analog circuits of the chip-level ADC are required to operate with a high bandwidth, because the conversion rate is the same as the pixel data rate. The chip-level ADC must be of very high speed (proportional to the number of pixels in the array), at least in the order of hundreds of mega samples per second. Secondly, the problem is compounded by the fact that the chip-level ADC integration approach may require a high resolution. Finally, the high power consumption contribute to high speed analog circuits is a concern [72].

The second is the column-level approach [73], where one or more columns of the pixel array have a dedicated ADC. This structure affords virtually unlimited silicon area in one dimension but feasible design space in the other dimension. Their conversion rate is the row readout speed of pixel sensors, and is slower than the serial pixel data rate by a factor of 100$\sim$1000. Moreover, the column-level ADCs allow for the implementation of shared circuits such as a reference generator, the buffers and a clock sequence. This could lead to considerable power and area saving. Since the conversion rate is much slower than that of the chip-level ADC approach, the complexity of the design on analog circuits is decreased, but another issue is the matching of the column-level ADC between different columns [74].

The column-level ADCs are operated in parallel, low-to-medium speed ADC architectures can be employed such as ramp ADCs, successive approximation ADCs, oversampling sigma delta ADCs or pipelined ADCs. The 4-bit successive approximation ADCs and pipelined ADCs have been developed at IPHC [75]. The successful designs, being within a pixel pitch of $\sim$ 30 μm and the length of $\sim$ 1 mm, have been completed. They also follow the row-wise readout approach, they create a $\sim$ 1 mm wide inactive area at the edge of sensors. They have been demonstrated capable of reading out at the frequency of about 10 MHz. A resolution ($\lesssim$ 3 μm) is likely reachable by such ADCs with a 20 μm pitch instead of shared discriminators at the end of columns.

The third approach, which is the focus of this thesis work, consists in using pixel-level ADCs. So far, CPS with column-level ADCs can be classified as analog pixels because their outputs are analog signals. On the other hand, CPS with pixel-level ADCs can be considered as digital readout pixels since the pixel outputs are digital signals. The notion of having a pixel-level ADC is very promising, for a fully parallel A/D conversion means power efficiency and digital readout means high speed.

5.1.2 Which kind of pixel-level ADC?

Considering the feasibility of the analog signal processing, the pixel-level ADC is generally dismissed as the pixel pitch tends to be too small to host an ADC in the pixel. Therefore, most researches on CPS involve the integration of ADCs at the column-level. The integration of pixel-level ADCs is not widely accepted. With the development of 3DIT, the circuits can be distributed over different tiers instead of being spread out on the same wafer, more intelligence can be integrated in the pixels. 3DIT provide fresh impetus for performing the pixel-level digitalization.

Currently, beam test results of MIMOSA26, obtained with a 120 GeV pion beam at CERN, give a single point resolution of about 3.1-3.2 μm with a pixel pitch of 18.4 μm [76]. The innermost layer of the ILD vertex detector requires the pixel sensors with a higher spatial resolution below 3 μm , associated to a very demanding readout speed. To arrive at a better spatial resolution without further reducing the pixel pitch, it is necessary to replace the column-level discriminator with a 3$\sim$4 bits ADC [75].

Although a 4-bit column-level ADC with a 35 μm pixel pitch can realize such a good spatial resolution, 2D-CPS still have inherent limitations that make it difficult to achieve the ambitioned frame readout times. Using 3DIT, two or more pixelated chips are stacked and the amount of logic per pixel can be increased. The parallel readout approach provides an adaptable readout speed by dividing the whole active area into several sub-arrays. Although relatively low speed converters are used in each pixel, a high level of parallelism allows for short frame readout time.

Approaches to the designs of pixel-level ADCs include oversampled ADCs [77], multi-channel bit-serial (MCBS) ADCs [78], and ramp ADCs [79]. Each oversampled ADC employs a one-bit modulator at each pixel. This kind of ADCs can be implemented using very simple and robust circuits. The implementation of such an architecture has however several shortcomings such as large pixel pitch, high FPN, and very low speed. MCBS ADC overcomes some shortcomings of the sigma delta ADC: non-uniformity is significantly reduced by globally distributing the signals and by performing the method of auto-zeroing offset cancellations. Although the operating speed of the MCBS ADC is improved to the level of 1 kHz by using Nyquist rate conversion instead of oversampling, it can not meet the readout speed requirement of the inner layer of the ILD vertex detector. The ramp ADCs are architecturally simple circuits and can achieve relatively high resolution at medium speeds with minimal power dissipation. They also exhibit

Table 5.1: Relevant characteristics of the pixel-level ADC.

Technique	Bits	Power	Area	Robustness	Speed	Good for CPS
Oversampled ADCs	18-20	low	small	high	low	No
MCBS ADCs	6-8	low	small	medium	low	Maybe
Ramp ADCs	6-12	low	small	medium	medium	Yes

high robustness and may therefore be extremely suitable for integration in the pixels. The characteristics of these ADCs are listed in table 5.1.

5.2 Specifications of the ADC

- In the applications of pixel sensors with pixel-level ADCs, the signals created by particles remain relatively static. The static performance of pixel-level ADCs is more important than their dynamic performance, the pixel-level ADC specifications describing the accuracy of ADCs are offset error, gain error, differential nonlinearity (DNL), integral nonlinearity (INL). These four specifications build a description of ADC's static performance [80].

- As pixel-level ADCs are spread all over the pixel array, uniformity of processing elements becomes an important design issue. Analog circuits often suffer from fabrication inhomogeneities and mismatches of transistors, they can influence the precision of pixel-level ADCs. FPN is therefore another critical design factor for pixel-level ADCs.

DNL: The size of each code width should be the same for an ideal ADC, the code width of an ideal ADC is a Least Significant Bit (LSB). DNL is the maximum deviation in the difference between two consecutive code transition points on the input axis. This can be calculated as expressed in (5.1) and described in Figure 5.1.

$$DNL = Max(\frac{V_{n+1} - V_n}{V_{LSB}} - 1) \tag{5.1}$$

where V_n is the input voltage of the Nth code, and V_{LSB} is the input voltage of one LSB, it can be calculated by (5.2).

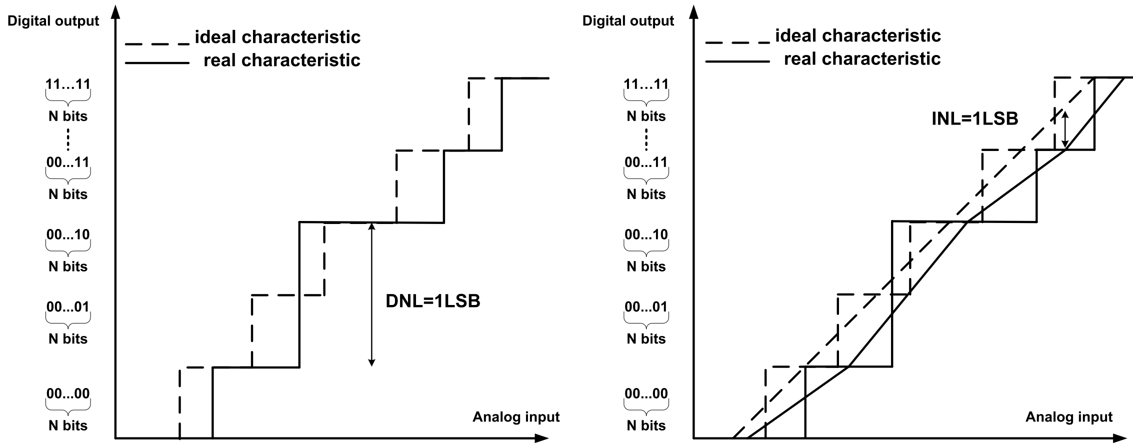


Figure 5.1: DNL of an N-bit ADC (left) and INL of an N-bit ADC (right).

$$V_{LSB} = \frac{V_{in}}{2^N} \tag{5.2}$$

where V_{in} is the full input voltage range of the ADC, and N is the ADC resolution.

INL: The INL is the maximum deviation of an ADC's transfer function from the ideal slope of the ADC. Mathematically, INL can be expressed as the sum of DNL for each code. The difference between the ideal voltage transition level and the actual transition level is the INL, expressed in(5.3) and described in Figure 5.1.

$$INL_i = \sum_{i}^{n} DNL_i \tag{5.3}$$

where DNL_i is the DNL of the i th code.

Offset error Amplifiers and comparators in practical circuits have inherent errors from voltages or currents offset, which are caused by the mismatches of components. The offset results in a non-zero digital code output when a zero signal is applied to the ADCs. The ideal transfer function curve of ADCs will start from the origin, the first code boundary will occur at one LSB. Offset error can be observed as a shifting of the entire transfer function to the left or the right. It is illustrated in Figure 5.2. Trimming or auto zero procedures can remove the offset in an ADC.

Gain error The gain error is the deviation in the non-ideal slope of the transfer function from the ideal slope. It is generally expressed as the percentage difference between these

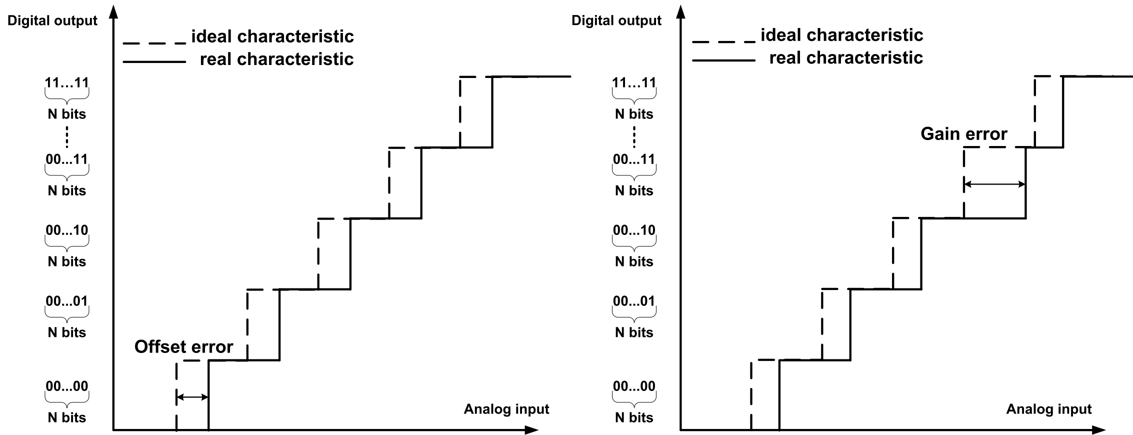


Figure 5.2: Offset error of an N-bit ADC (left) and gain error of an N-bit ADC (right).

two slopes, as illustrated in Figure 5.2. The gain error could be corrected by calibration. In order to avoid to miss the code, the design goal of a linear ADC is that the DNL and INL are less than ±0.5 LSB. This general objective may however be mitigated in the case treated here, which addresses the reconstruction of an impact position, relatively moderately influenced by the DNL and INL.

5.3 A 3-bit pixel-level single-slope ramp ADC

5.3.1 Principle of the single-slope ramp ADC

A block diagram of a ramp ADC is shown in Figure 5.3, the circuit consists of an accurate ramp generator, a comparator and a counter [81]. The input signal is applied to one input of the comparator. When the conversion starts, the counter is set at zero and the ramp generator is reset to the initial value. When a positive input signal V_{in} is applied, the ramp generator starts generating a ramp voltage. In the meantime, a switch is opened and counting codes are injected from the counter. When the output signal of the ramp generator is equal to the input signal, the switch is closed and counting codes are latched by the comparator. The analog input signal is converted into a time that is measured by counting clock pulses during that time. An accurate amplitude-to-time conversion is obtained. The accuracy of the system is determined by the clock generator, the slope of the ramp generator, and the reference source V_{ref}. A simple calculation shows that the time in which an input signal is converted is equal to:

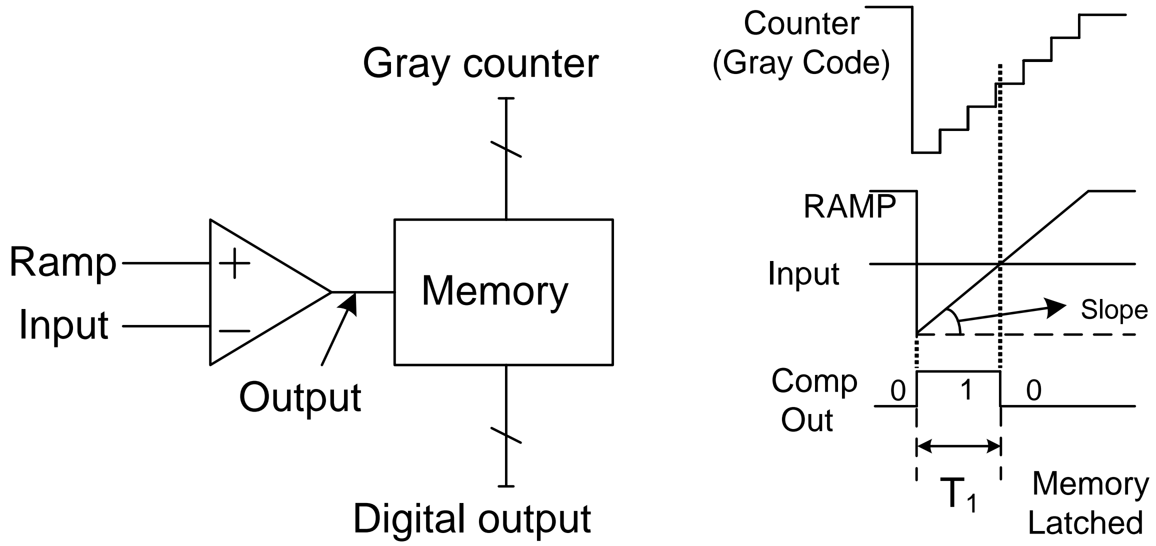


Figure 5.3: A single-slope ramp ADC system (left) and the time diagram for A/D conversion of the single-slope ADC (right).

$$T_1 = Slope \cdot \frac{V_{in}}{V_{ref}} \tag{5.4}$$

The digital values then become:

$$N_{digital} = T_1 \times f_{clock} \tag{5.5}$$

Where the f_{clock} is the frequency of the gray counter. The slope ADC has generally very good linearity. As the slope generation circuit and the counter are common to each column, only one comparator is needed for each pixel. Thus, it does not suffer from the area and the power issue. The conversion time (T_1) is proportional to 2^N. For a 3-bit ADC, a full conversion needs eight comparisons and the conversion time is $8\frac{1}{f_{clock}}$. However, due to the need of the auto-offset cancellation, the comparator needs tens of ns for completing the signal comparison and making the decision.

5.3.2 Pixel-level ADC architecture

To do efficient in-pixel digitization, the resolution of the pixel-level ADC should be at the same level as the voltage (∼1 mV) resulting from the pixel noise [82]. It is expected strongly to have a high precision pixel-level ADC, a high gain amplifier has been proposed. Regarding the readout of the pixel data and minimal power consumption, each pixel sensor employs a row-by-row sequential readout scheme. The pixel-level single-

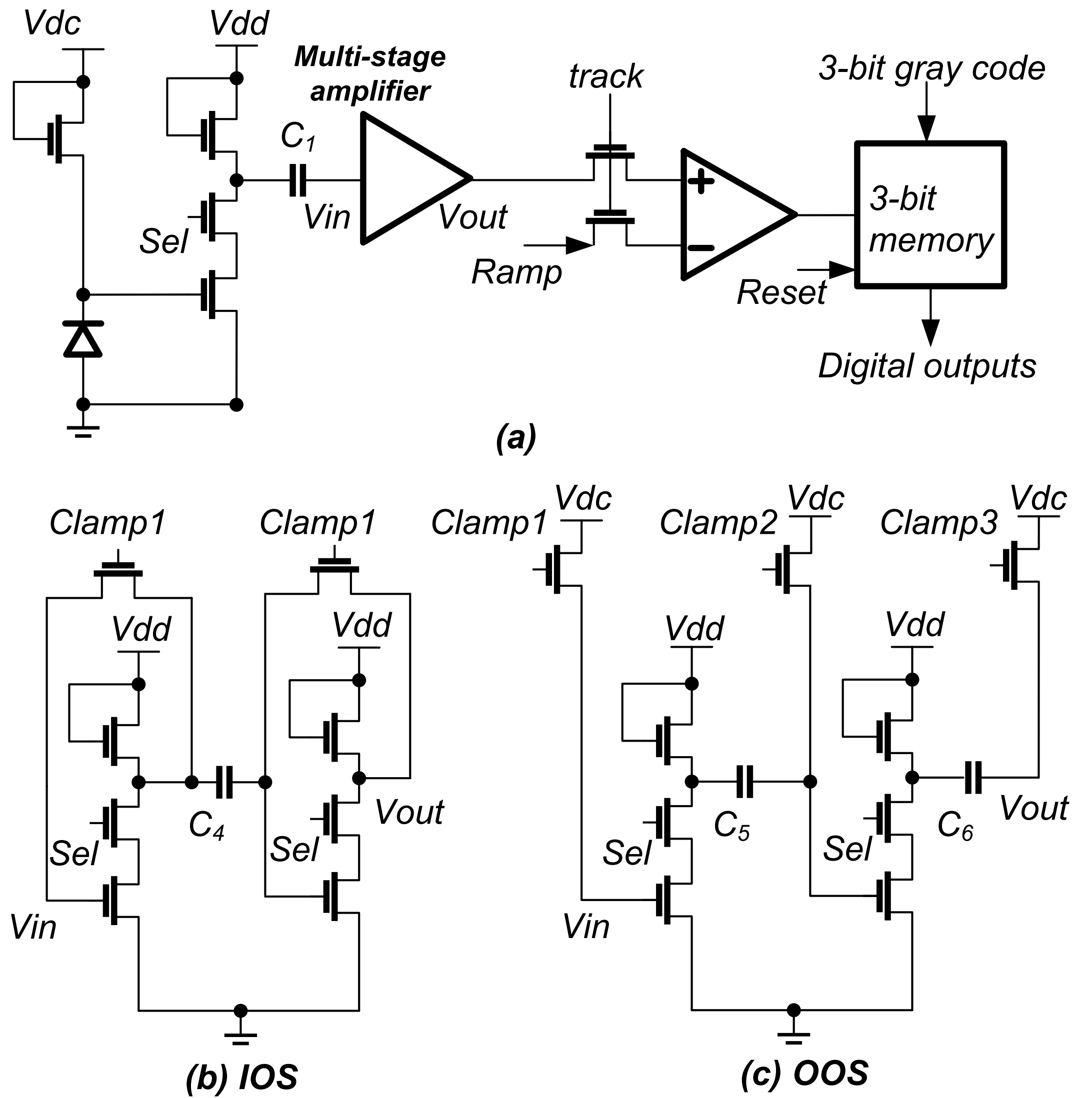


Figure 5.4: Schematic of the proposed 3-bit pixel ADC (a), and two possible types of multi-stage amplifiers with the input (b) and output (c) offset compensated techniques.

slop ADC unit consists of an amplifier, an analog comparator and a 3-bit memory cell, which is located in the digital pixel. The block diagram of the proposed pixel-level ADC is shown in Figure 5.4.

The chip-level analog ramp generator makes an accurate ramp voltage that connects to the negative input of each pixel's comparator. The positive input on each comparator connects directly to the output of the cascaded amplifier. The globally distributed 3-bit gray coded counter values are simultaneously applied to the per-pixel memory bit lines. Once the ramp reference signal exceeds the amplified sensor node voltage V_a, the comparator output enables the per-pixel memory to begin loading the gray code values. Moreover, it is mandatory to implement an output offset storage technique, which reduces

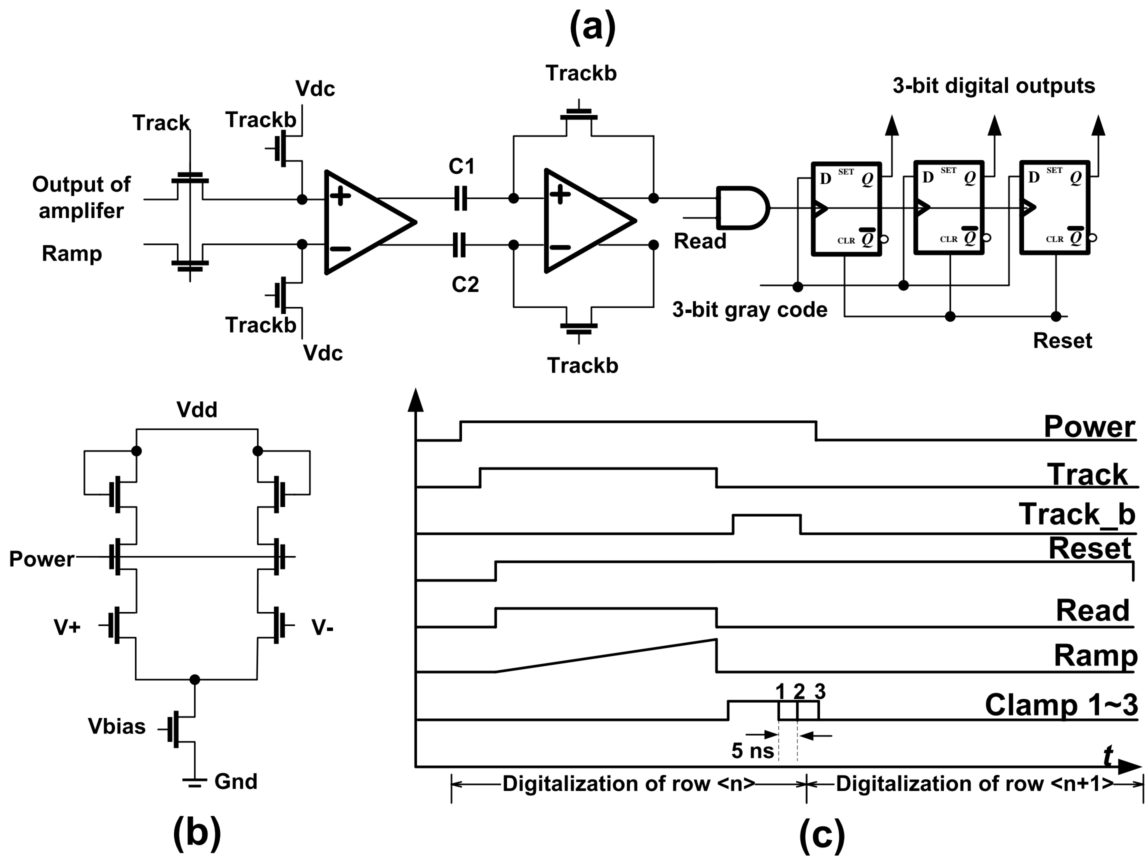


Figure 5.5: (a)Schematic of the comparator and digital memory (b)schematic of the amplifier in the comparator (c)timing waveform of the proposed pixel-level ADC.

further the intrinsic offset voltage of the pixel-level comparator. The block diagram of the comparator and time waveform of the proposed pixel-level ADC are shown in Figure 5.5.

- Sel signal actives the circuits of the pixel-level ADC one row at a time.
- $Clamp1, 2, 3$ signals store the offset voltage of amplifiers for canceling the offsets at the next clock cycle.
- $Track$ signal samples the input signal to compare with the ramp voltage in the current clock cycle. $Track_b$ signal samples the offsets of the comparator.
- $Reset$ signal actives the digital counter, when the input signal is amplified.
- $Read$ signal is used to inject a ramp reference voltage.

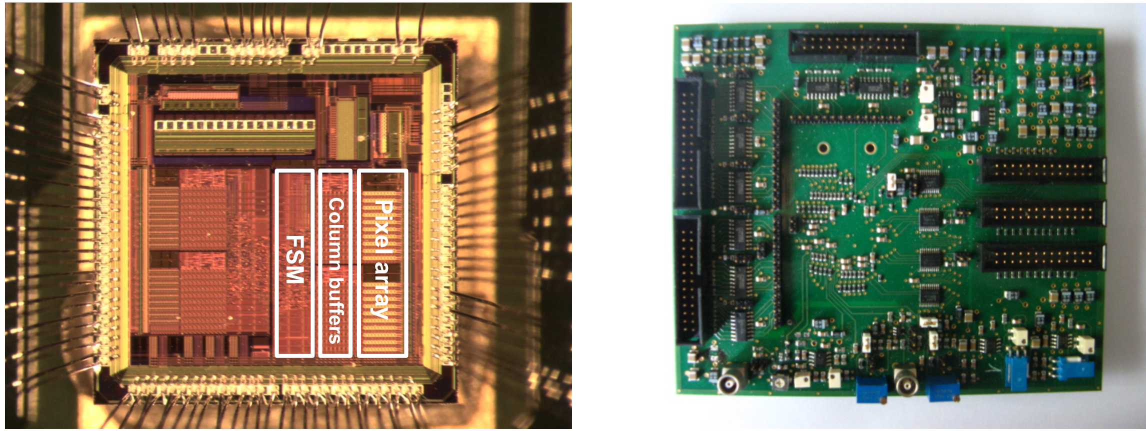


Figure 5.6: The photomicrograph of the chip with pixel-level ADCs (left) and the test board for this prototype (right).

5.4 Experimental measurements

5.4.1 Chip description and test setup

The test chip has been fabricated by using the Chartered 130 nm CMOS process. All circuit blocks are operated at a 1.5 V core voltage. In order to optimize the performance of the proposed pixel-level ADCs, a chip containing pixel-level ADCs with two different types of amplifiers was designed and fabricated. The photomicrograph of the chip is shown in Figure 5.6. The chip implements a 20×10 pixel array with a 23 μm pitch on a 1×1.25 mm^2 core. The corresponding test board was also designed. The test setup comprises several modules: the power generator supplies power voltage, a ramp generator provides the periodic ramp voltage, a logic analyzer supplies and probes the signals from the chip.

5.4.2 Test methods of the pixel-level ADCs

A method for measuring the linearity was developed for determining INL and DNL of pixel-level ADCs. Figure 5.7 shows a test setup for measuring the transition codes of each ADC. The analog input is provided from a precision low-noise voltage generator, and the ADC digital outputs are stored by the digital analyzer. In practice, a triangular waveform is used periodically as a ramp voltage. A large number of samples are collected from each input step, and thus the numbers of occurrences of each code are recorded. The ADC transfer function is then determined by a statistical analysis of samples in a full input range.

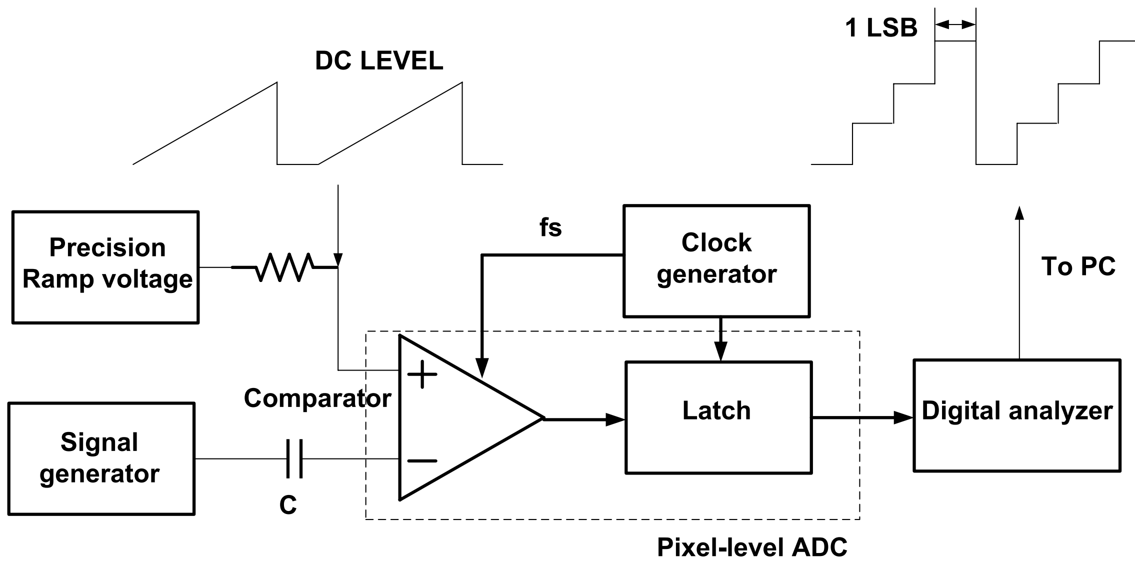


Figure 5.7: The test setup of the pixel-level.

Another useful application of this test method is to measure the ADC input-referred noise. This is easily accomplished by simply terminating the ADC input with the appropriate resistance, applying a DC input and recording a number of output samples. If the peak-to-peak input referred ADC noise is less than 1 LSB, the output samples should correspond to a single code value. Assuming the noise is a Gaussian function, the input-referred noise is simply the standard deviation (σ) of the distribution, and is generally expressed in *RMS-mV*. The input-referred noise of the ADC should be less than one half LSB of an ADC.

5.4.3 Test results of the pixel-level ADCs

In this section, we describe the measured results of the pixel-level ADCs (i.e. 12 test pixel-level ADCs) utilized in our test chip. Two architectures are designed to optimize the performance: the one implements the output offset compensated amplifier, the other uses the input offset compensated amplifiers with or without dummy switches[1]. When the sampling switch turns off and injects the charge onto the capacitor, the dummy switch turns on and absorbs the charge from the capacitor in its channel, as shown in Figure 5.8. Thus, if exactly half of the transistor charge is injected onto C_4, then the held voltage on C_4 will be not corrupted by the charge injection.

Since there are 2^N different output codes, there are at least 2^{N+2} different transition

[1] A dummy transistor with half the width of the sampling (Clamp1) switch is added and driven by $\overline{Clamp1}$ (the complement of the sampling clock Clamp1).

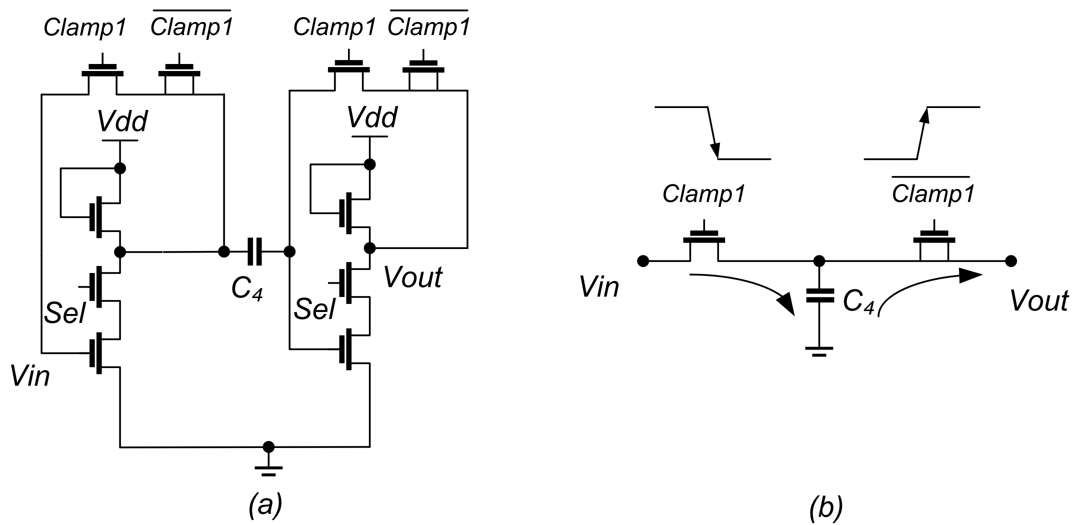


Figure 5.8: Input offset compensated amplifier with the dummy switch (a) and cancellation of MOS charge injection (b).

voltages. Without loss of generality, the transfer curve of pixel-level ADCs is obtained by injecting a linear voltage at the input. Figure 5.9 shows the measured transfer curves of three types of pixel-level ADCs. Some of pixel-level ADCs have the uniform transfer curves, i.e. each step of transition voltage gives an accurate code bin width. There are however a group of ADCs that have the non-uniform transfer curves (from ADC5 to ADC8), where the dummy switches are implemented. In this case, the transfer curves are the non-linearity, they indicated that the dummy switches could not provide accurate charge cancellation. The fraction of the channel charge injected by the switch transistor is independent of the impedance and clock transition speed, it does not receive half of the switch channel charge.

Figure 5.10 and Figure 5.11 show measured DNL and INL of these ADCs operating at the row processing time of 300 ns. The best performance of DNL and INL is found in the group using the input offset compensated amplifier (from ADC9 to ADC12), the peak-to-peak DNL of four ADCs is -0.73/0.57 LSB, the peak-to-peak INL of this four ADCs is -0.73/0.48 LSB. As compared to output offset compensated amplifiers, the method of the input offset storage helps to reduce non-uniformity of the amplifier gain due to the implementation of the feedback operation. The input offset compensated amplifier therefore shows a significant advantage over the output offset compensated amplifier. The worst performance of DNL and INL exists in a group using the amplifier with dummy switches (from ADC5 to ADC8), this is mainly due to the charge injection from dummy switches which were not optimized for canceling the charge injection.

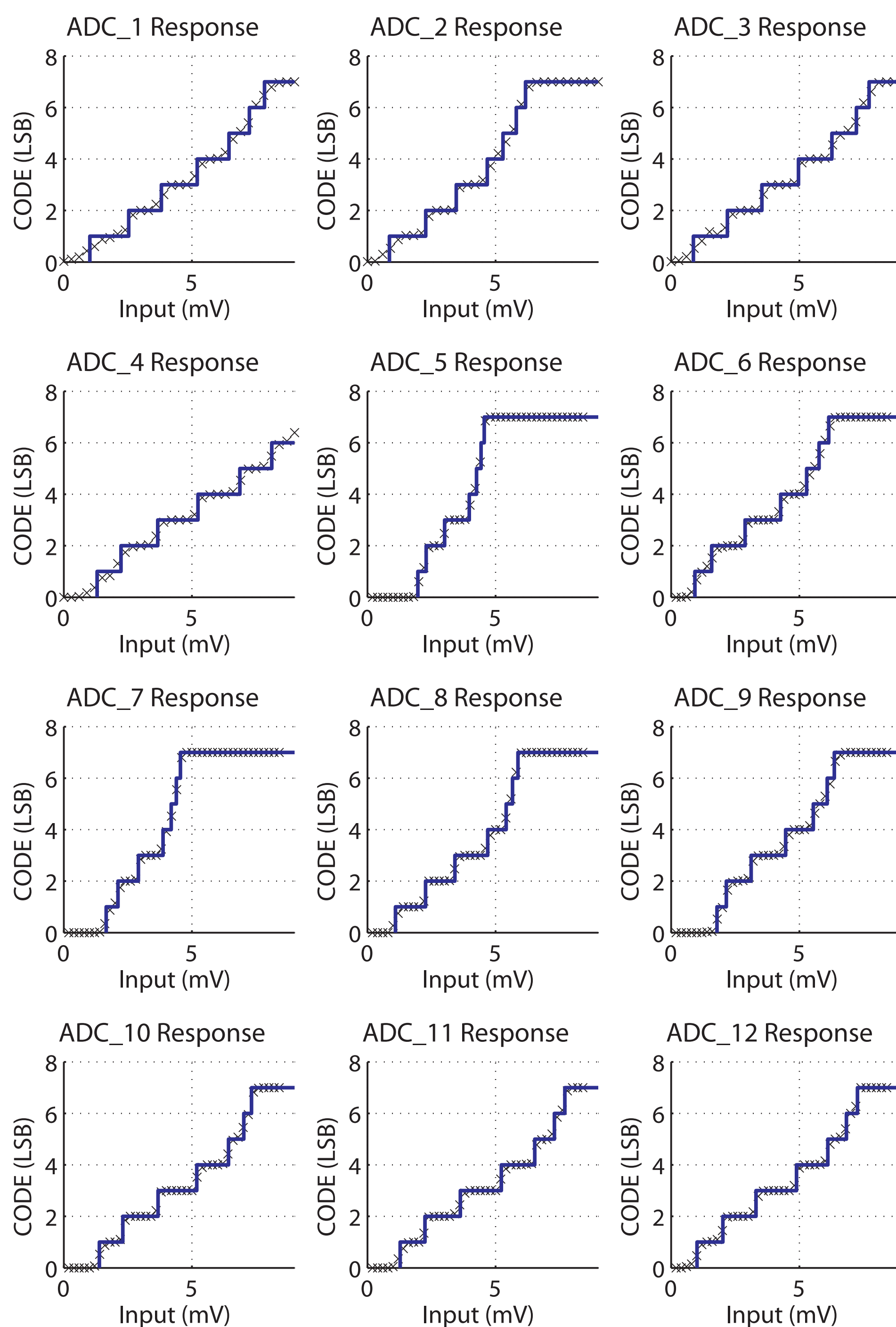


Figure 5.9: Measured transfer curves of pixel-level ADCs: the output offset-compensated amplifiers are implemented in the first group (from ADC1 to ADC4), the input offset-compensated amplifiers with dummy switches are used in the second group (from ADC5 to ADC8), the input offset-compensated amplifiers without dummy switches are used in the last group (from ADC9 to ADC12).

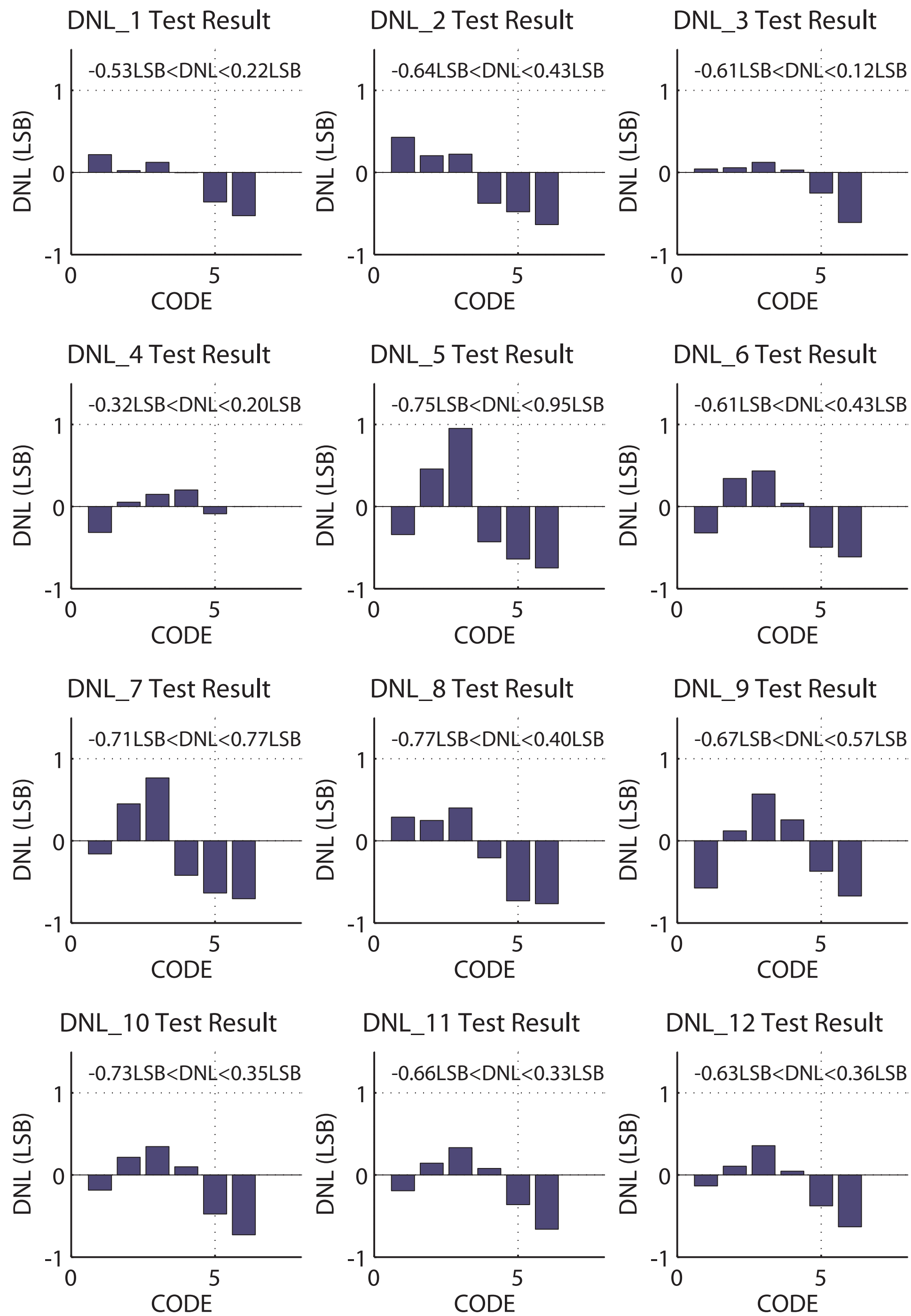


Figure 5.10: Measured DNL of pixel-level ADCs: the input offset-compensated amplifiers without dummy switches are implemented in the first group (from ADC1 to ADC4), the input offset-compensated amplifiers with dummy switches are used in the second group (from ADC5 to ADC8), the output offset-compensated amplifiers are used in the last group (from ADC9 to ADC12).

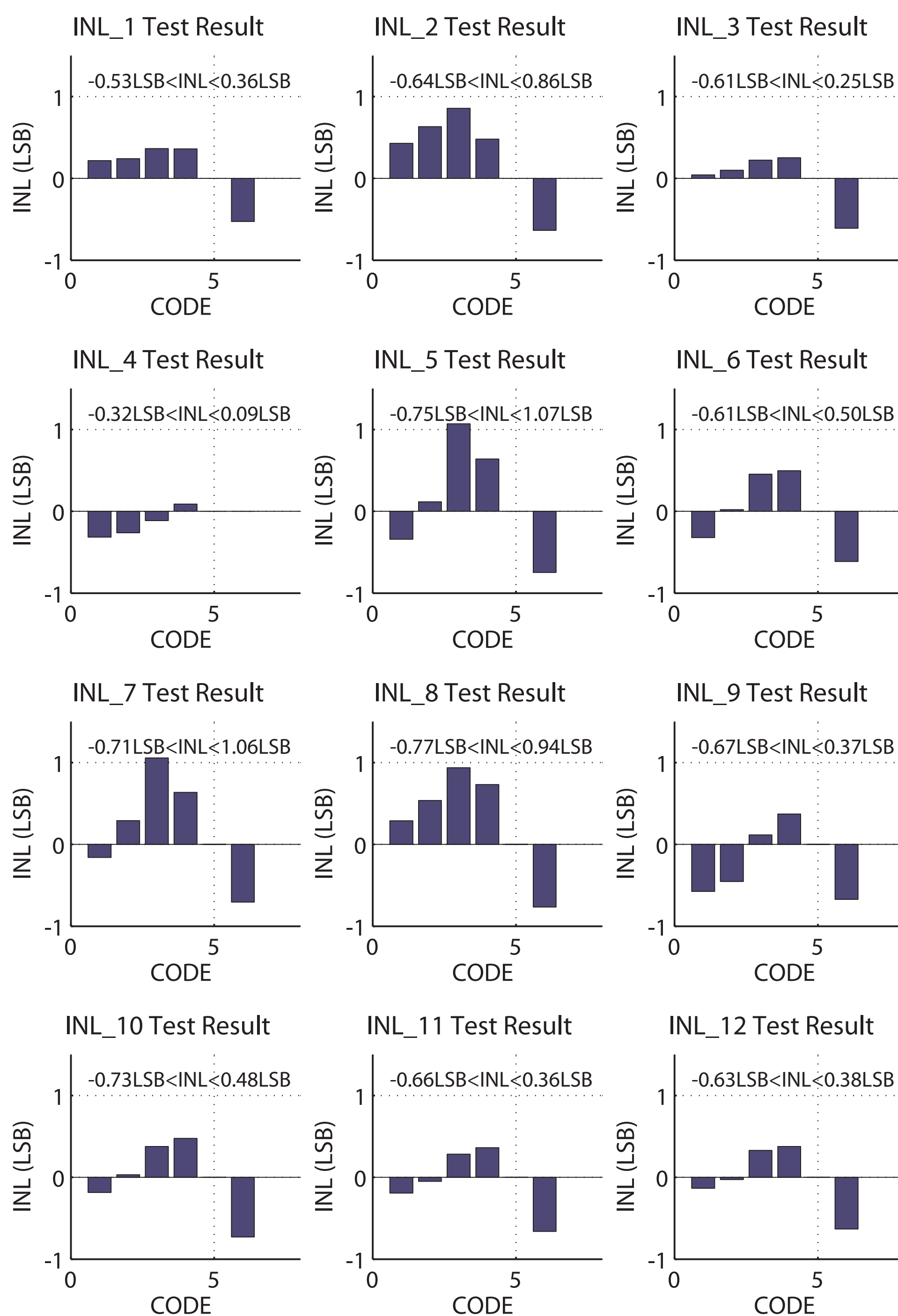


Figure 5.11: Measured INL of pixel-level ADCs: the output offset-compensated amplifiers are implemented in the first group (from ADC1 to ADC4), the input offset-compensated amplifiers with dummy switches are used in the second group (from ADC5 to ADC8), the input offset-compensated amplifiers without dummy switches are used in the last group (from ADC9 to ADC12).

5.4.4 Lessons learned and future plans

Considering a full-scale input voltage of about 10 mV, a full input range[2] will allocate the minimal step of about 1.2 mV to a 3-bit pixel-level ADC. Due to a charge-to-voltage gain of about 60 $\mu V/e^{-}$ achieved by the detecting part, the minimal step voltage corresponds to about 20 electrons at the input. In real case, the event caused by a LSB's signal could not be located in the center of one bit, noise broadening leads to faulty events in neighboring bits [83]. Once such a noise broadening becomes comparable to the ADC's bit width, the conversion system is distorted. As a consequence, it is important to minimize the input-referred noise of ADCs. The RMS noise of each bit step is calculated statistically from 500 different frames. For the pixel-level ADCs with input offset compensated amplifiers, one bit width is about 1.0 mV and input referred noise is in order of 0.3 mV. For the pixel-level ADCs with output offset compensated amplifiers, one bit width is about 1.3 mV and the noise is in order of 0.4 mV. While measurements show that another group with dummy switches has high input referred noise of 1.1 mV, these results also illustrate that the charge injection of dummy switches have an excessive impact on the noise of the pixel-level ADC.

The test results of these test pixel-level ADCs have given three main consequences:

- The pixel-level ADCs with input offset compensated amplifiers exhibited the best performance in terms of input referred noise, input dynamic range and linearity. The input dynamic range of test ADCs is $\sim$ 10 mV, the input referred noise is in the order of 0.3 RMS-mV, and one LSB of the pixel-level ADC reaches $\sim$ 1.0 RMS-mV.

- The pixel-level ADCs with dummy switches represented an insufficient bit width with high noise, showing that the charge injection of dummy switches have an excessive impact on the noise of pixel-level ADCs.

- FPN performance of pixel-level ADCs is not demonstrated because of the limited number of pixels in this prototype. FPN can be eliminated by the in-pixel CDS circuitry, the measured results showed that the offset and gain responses of pixel-level ADCs with input offset compensated amplifiers are almost consistent.

[2]Since one LSB of the ADC is set to the value of the pixel noise ($\sim$ 1 mV observed from the output of the first in-pixel amplifier), a 3-bit ADC gives a full input range of about 10 mV.

5.5 Conclusion

This chapter presents a new concept of developing the pixel-level ADC, which may match a high spatial resolution requirement for a wide range of charged particle tracking applications. 3DIT are close to open a full potential of CPS, the context of this chapter was to investigate a path allowing for using a high pixel functionality of CPS. Their two main benefits were discussed in this thesis. One presented in chapter 4 is how to improve the readout speed or to perform data compression, the other is to increase the resolution.

This chapter concentrated on an in-pixel ADC which would efficiently quantify the charge deposited by particles traversing the sensor. It showed how a ramp ADC technique featuring 3-bit resolution could be implemented in a 23 μm pitch. Each pixel comprises a preamplifier, a voltage comparator and a 3-bit static memory. This pixel architecture clearly shows the potential of the proposed technique in reducing the design complexity.

In order to verify the functionalities of the proposed pixel, a prototype was fabricated on a standard 2D CMOS technology. The standalone pixel-level ADCs were designed. The measurement results showed that the proposed pixel-level ADC can meet the design goals: the input dynamic range is about 10 mV, the input referred noise (RMS) is in the order of 0.3 mV, and one LSB of the pixel-level ADC reaches about 1.0 RMS-mV. A full conversion period is 500 ns/per row, the static power is $\sim$ 90 μW with the power supply of 1.5 V. However, it is worth noting that the proposed ADCs showed a relatively big difference in their transfer curves. This dispersion is suspected to originate mainly from an insufficient resolution, which is expected to be reduced by enhancing the gain of the comparator. Although the required resolution is still not yet optimized for this design, the functionality of this ADC has been verified. This ramp ADC technique has however another inherent limitation on the speed because of a long conversation time. By taking advantage of 3DIT, several pixel-level ADCs can read out in parallel, thus allowing for the readout to comply with the requirements.

The pixel-level ADCs developed in this chapter are intended for a continuous, rolling shutter mode, readout to save the power consumption. The prototype demonstrated that the ramp technique allowed for low power, multi-channel and pixel application, despite some remaining noise dispersion which needs further investigations.

Chapter 6

Summary and outlook

6.1 Achievements of this thesis

In this thesis, 3D integrated CMOS pixel sensors have been proposed for the innermost layer of the ILD vertex detector. The objective is to develop intelligent pixel sensors complying with the requirements of this detector layer, which is particularly demanding in terms of spatial resolution ($\lesssim$3 μm) and frame readout time ($<$10 μs). These specifications are out of reach of state-of-the-art 2D CMOS pixel sensors. The latter may however either meet the required spatial resolution at the expense of the readout time, or reversely.

3D integrated CMOS pixel sensors are expected to breakthrough this bottleneck. Vertical integration of two (or more) CMOS layers (tiers) allows for a separation of the analog front-end electronics and the digital readout sections. The shorter connections between analog and digital parts translate into smaller parasitic capacitors. The readout speed could be increased by at least one order of magnitude, as compared to the ordinary 2D CMOS pixel sensors. It is also possible to increase the complexity and functionality in electronic readout circuits by exploiting a multilayer device structure. This is because their high integration potential allows for smaller pixels, and thus higher spatial resolution, than 2D CMOS pixel sensors.

3DIT are particularly suited to CMOS pixel sensors, since they allow to combine different CMOS processes, each layer being optimized for its own functionality such as charge generation or signal processing. 3DIT are therefore expected to resolve most limitations of 2D CMOS pixel sensors. This appealing evidence has settled the framework of the Ph.D.

Based on the beam time structure of the ILC, two alternative readout strategies have

been investigated in this thesis: delayed readout and continuous readout. The first one where the hits are stored in the sensors during the whole bunch train duration and read out during the beam-less period separating two consecutive trains. The second one, so called rolling shutter readout, where the pixels in the pixel array are continuously read out row by row. In order to evaluate and compare their potential and benefits, these two readouts were explored in parallel in this thesis.

In case of the delayed readout architecture, a 12 μm pitch 3-tier CMOS pixel sensor presented in chapter 3 is proposed. In the bottom tier, the pixel contains a sensing element for the charge collection. The pixel of the intermediate tier contains a shaper and a discriminator for the signal discrimination. And finally, each pixel of the top tier latches the arrival time information of the first hit, and an overflow bit flags a potential second hit. For a $\sim$1 ms bunch train, the required time resolution imposes 7 bits of time stamp accuracy, corresponding to a time resolution of $\sim$7.5 μs.

A 2-tier 3D integrated sensor was designed and fabricated in a 0.13 μm Chartered/Tezzaron technology. The complete readout chain (amplifier-shaper-discriminator) has been designed in the analog pixel. Its simulation predicts an equivalent noise charge of $\sim$ 20 e^- and a threshold dispersion of $\sim$ 23 e^- . A reduced 5-bit time stamping is implemented in the digital pixel because of the limited pixel area. Due to connection mismatches between the stapled circuits occurring in the fabrication, only the functionalities of the digital section could be tested. The test results of the implemented circuits showed that the delayed readout architecture is fully operational.

In case of the continuous readout architectures, MIMOSA-26 with a 18.4 μm pitch as the state-of-art sensor was designed and fabricated in a 0.35 μm CMOS technology. In chapter 2, a 12 μm pitch 2D CMOS pixel sensors with novel in-pixel amplifiers was designed for exploiting the advances of the shrinking 0.13 μm Chartered CMOS technology. Test results showed that a three times higher CVF of 166 μV/e^- was achieved, because more in-pixel functionality can be implemented in a smaller pixel. However, due to the underestimation of the parasitic capacitor at the sensing node, a relatively high noise (24 e^- ENC) was obtained (i.e. $\sim$ 1.8 times higher than that of MIMOSA-26). Simulations were performed, indicating that a reduced value of 15 e^- ENC could be obtained by placing the input transistor of the amplifier closer to the diode. Be that as it may, the implementation of the proposed amplifiers potentially increases the pixel SNR.

In this thesis, another 3-tier CMOS pixel sensors with 20 μm pitch, based on the

continuous readout architecture, is proposed. The sensor is intended ultimately to be composed of 3 tiers of Integrated Circuits (IC) with the following complementary functionalities: detection with in-pixel analogue processing, pixel-level discrimination and zero suppressing readout. In order to demonstrate the functionalities of the pixels, a 2D chip including the proposed pixel-level signal processing chain was designed and fabricated in 0.13 μm Chartered CMOS technology. A low-offset and high-speed pixel-level discriminator was designed in this prototype. The measured results show that temporal noise and FPN remain below 0.5 mV and 1.4 mV, respectively. The power consumption of each discriminator is in the order of 120 μW at a clock frequency of 12.5 MHz. This work could therefore be considered as a relevant contribution to the ongoing improvement of time resolution for the innermost layer of the ILD vertex detector.

The 20 μm pitch discriminator presented in chapter 4 can not meet a spatial resolution below 3μm , which hampers the readout speed (small pixels). A novel approach of a 3-bit pixel-level ADC designed in the same technology was followed to address this problem. The design and tests of the pixel-level ADCs have been discussed in chapter 5. A 23 μm pixel sensor with a 3-bit ADC guarantees the required spatial resolution ($<$3 μm), while maintaining the readout speed of 10 μs by using the parallel continuous readout. The test showed that the INL of the pixel-level ADCs is less than +0.36/-0.66 LSB over the 3-bit input range of $\sim$ 10 mV. The DNL of the ADCs has also been measured to be smaller than +0.33/-0.66 LSB peak-to-peak. The sensor with this 3-bit ADC would allow to meet a high spatial resolution requirement.

Power dissipation is a crucial issue of 3D CMOS pixel sensors and is therefore one of the driving parameters of the designs. Power consumption estimates and comparison have been performed for the two readout architectures developed in this thesis. For a delayed readout, the designed 3D CMOS pixel sensors with a 12 μm pitch consumes about 7 W/cm^2 (only calculating the power of the pixels). This value, though substantially larger than for 3D CMOS pixel sensors based on the rolling shutter readout, may be not affordable. This concern should be addressed at the next step. Starting from the first prototype, it seems possible to reduce the power of each pixel by half ($\sim$ 5 μW) without degrading its noise performance. As a consequence, with a rather conservative duty cycle of 2 %, the average power consumption of the sensor still may be compatible with modest cooling.

6.2 Future plans

The first 3D integrated CMOS pixel sensors with a delayed readout architecture have been designed. In Spring 2009, the wafers were fabricated in a 130 nm CMOS Chartered technology. One of these wafers was diced before the 3D interconnection, so that the different layers can be separately tested. The test results presented in this thesis have shown that the circuits on the 2D wafers are fully functional. Fabrication of 3D wafers took a long time because of a number of obstacles faced both at the foundry and at the vertical integration facilities. In May 2011, wafer bonding and interconnection were performed by the Tezzaron Semiconductor company, the first 3D wafers became available in Summer 2011. However, more detailed tests showed that actual communication between the pixel cells located on two layers is not working. Layer-to-layer misalignment would explain why there is not signal communication between the layers. In order to address this problem, new planar wafers are being vertically integrated. The functionalities of this 3D integrated CMOS pixel sensors will be verified as the next step.

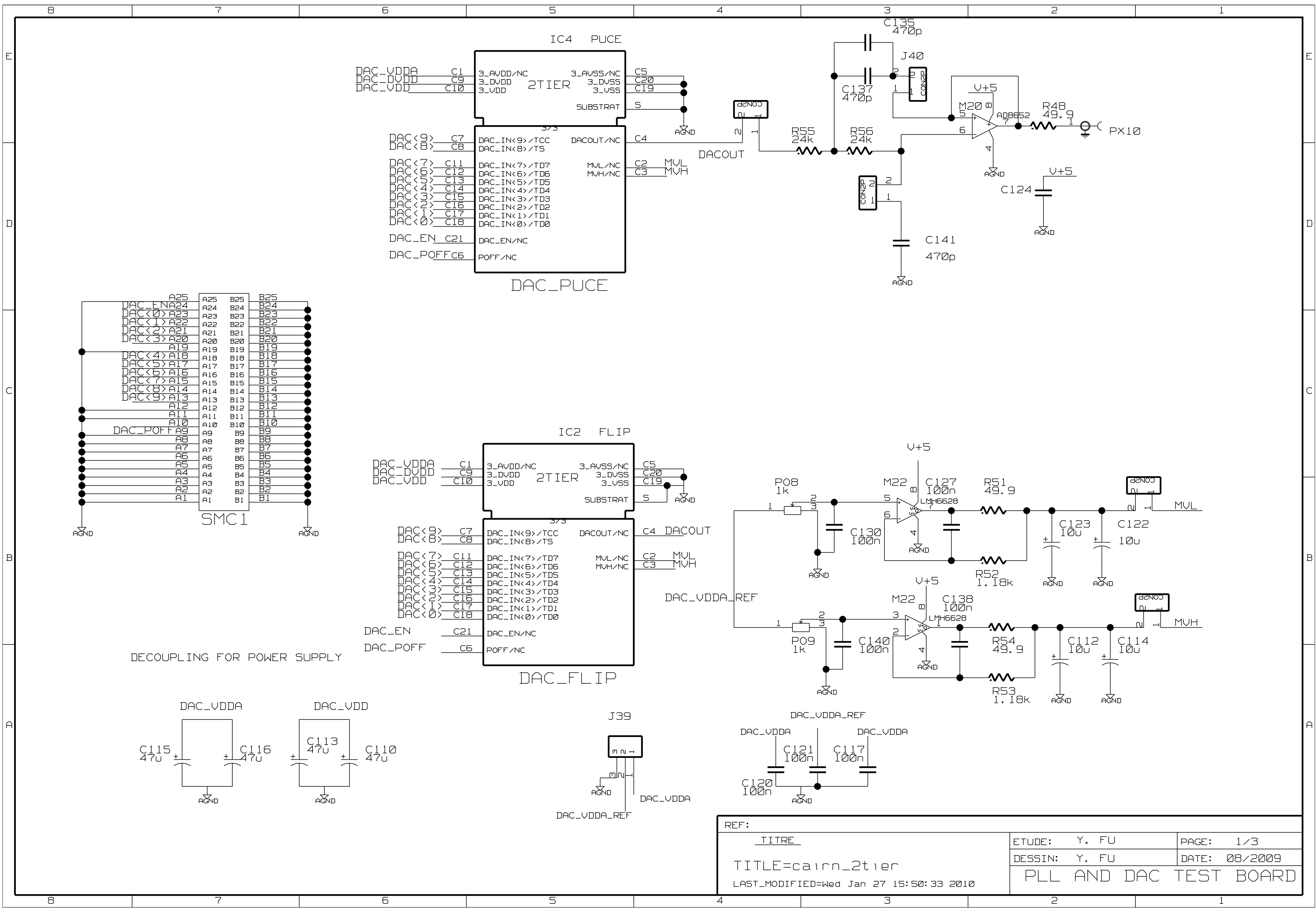
Due to the existing problems of the 3D integration, the novel pixel structures and the parallelized readout method, presented in chapter 4 and 5, have been implemented using a standard 2D CMOS technology. Their functionalities have also been verified experimentally as the initial step. In the near future, the proposed pixel architectures will be vertically integrated using a 3D integration technology. The flexibility and adaptability of the approach followed are suitable for developing real 3D integrated pixel sensors. When future 3D integration technologies become more mature, the advantages of the presented architectures will be fully available. Based on the achievement of these conceptual designs, the development of these architectures is considered as a relevant step towards the next-generation 3D integrated CMOS pixel sensors.

At present, a novel quadruple-well CMOS process with a small feature size (0.18 μm) may become mainstream for the manufacturing of an advanced 2D CMOS pixel sensor. A deep P-well implant that can be used to surround N-wells wherever needed, allows for the use of PMOS transistors in the pixel without degradation of the charge collection efficiency. The previous encouraging design of the pixel-level discriminator presented in chapter 4 has therefore been redesigned in this advanced technology. A low-noise CMOS pixel sensor with improved pixel-level discriminator has been implemented within an elongated pixel (16 μm $\times$ 80 μm), which could be suitable for the applications of the double-sided ladder in the PLUME project. Due to the pixel-level signal processing, the

readout speed and the sensor power consumption are not limited by the large parasitic capacitors in the columns. Therefore, the frame readout time and power consumption can be reduced. The chip was submitted in October of 2011, it is going to be available for testing in Spring 2012. It is hoped that this 2D technology will at the same time push present limitations of 2D sensors and prefigure a high performance sensing tier of future 3D sensors.

Appendix A

Schematic of the test boards for the CAIRN-1 and CAIRN-2D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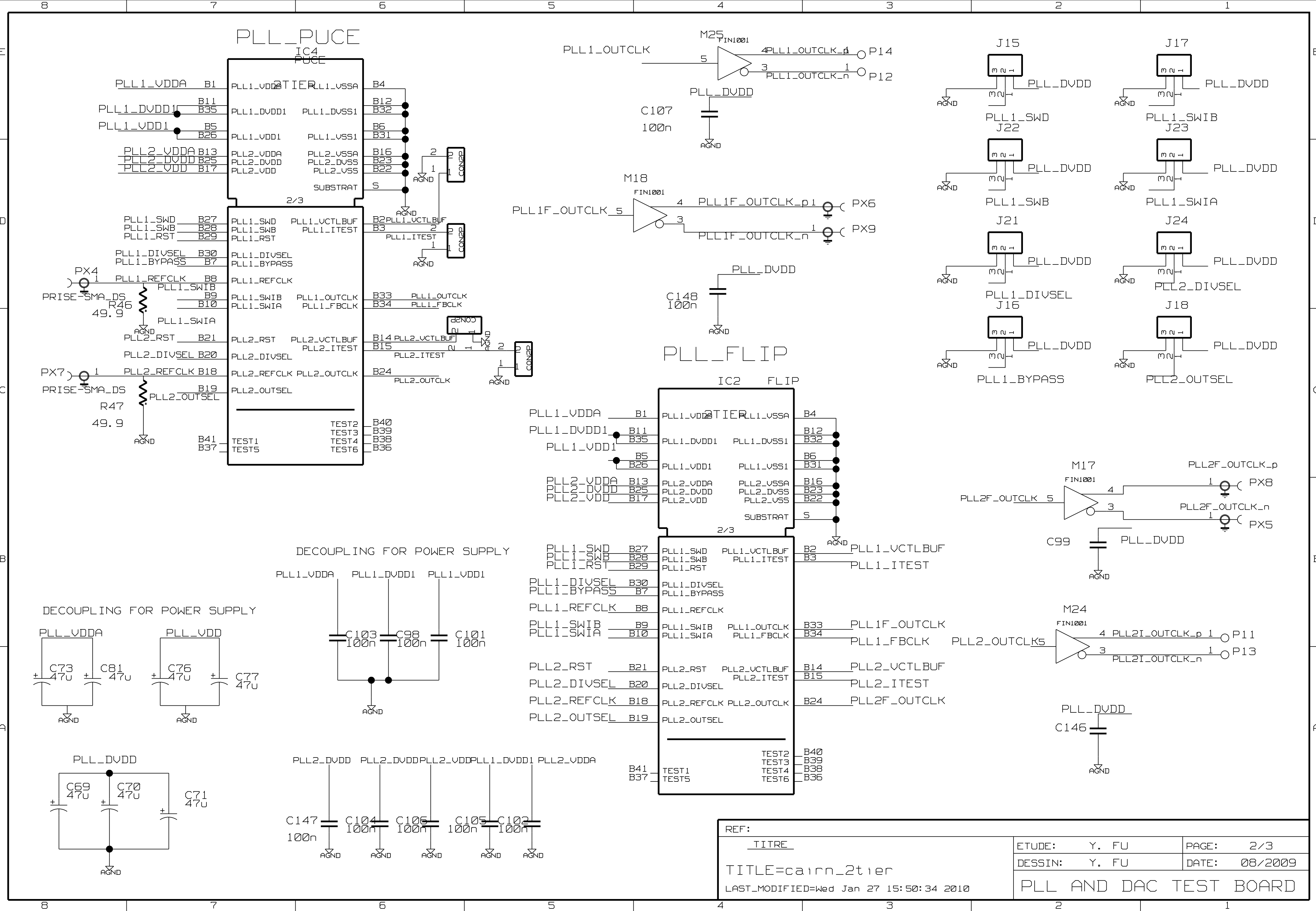
PLL AND DAC TEST BOARD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P14
P12
C107
100n
PLL_DVDD
M18
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PLL1F_OUTCLK_p1
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PX9
C148
100n
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J17
J22
J23
J21
J24
J16
J18
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PX5
C99
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R47
49.9
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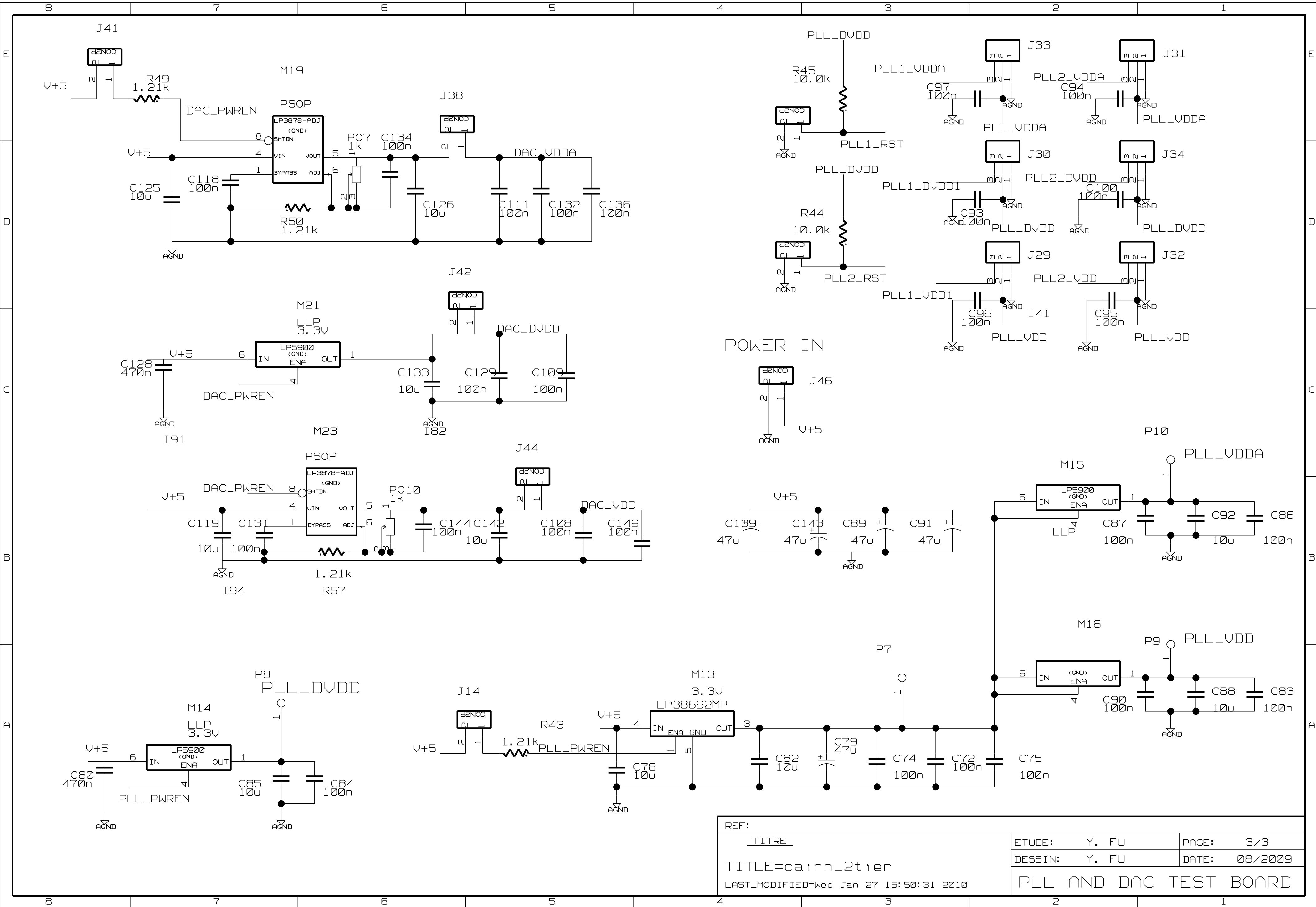

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P07
1k
C134
100n
J38
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470n
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C82
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C74
100n
C72
100n
C75
100n
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I41
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J32
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C95
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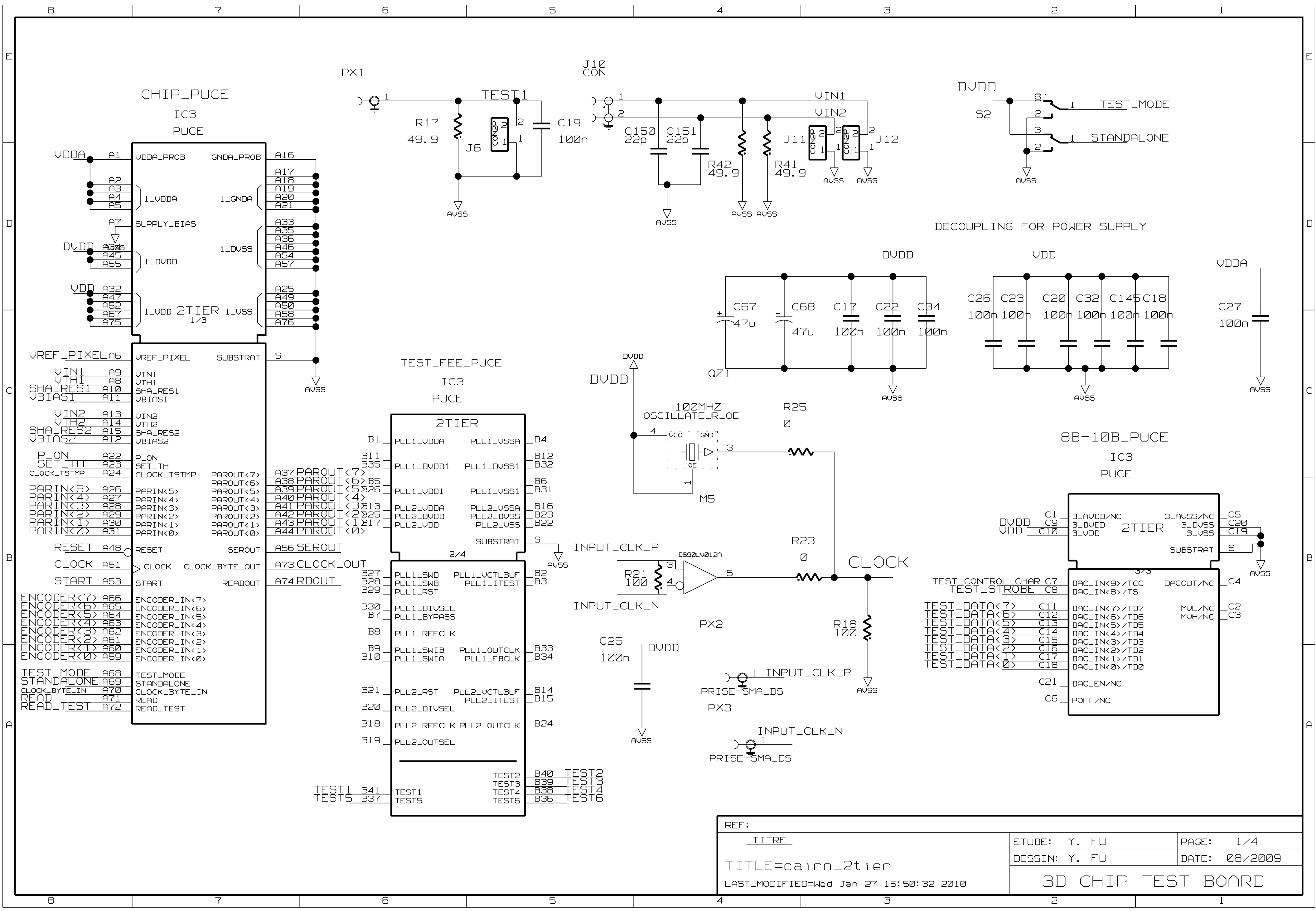
PLL AND DAC TEST BOARD



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R25 0
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3D CHIP TEST BOARD

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Bibliography

[1] GLD concept study group. GLD detector outline document. *Physics*, arXiv:0607154, 2005.

[2] The ILD web site. *http://ilcild.org*.

[3] International large detector community detailed baseline document, in preparation.

[4] C. Damerell et al. ILC vertex detector research and development-report of review committee. *http://ilcdoc.linearcollider.org*, 2008.

[5] N. Wermes et al. New results on DEPFET pixel detectors for radiation imaging and high energy particle detection. *IEEE Trans.Nucl.Sci*, pages 1121–1128, 2004.

[6] Y. Sugimoto et al. R&d status of FPCCD vertex detector for ILD. *Physics*, arXiv:5832, 2012.

[7] ILC reference design report. *http://www.linearcollider.org/Publications/Reference-Design-Report*.

[8] 2009 strawman baseline report. *http://ilc.kek.jp/SB2009/SB20091216A.pdf*.

[9] R. D. Masi et al. Improved estimate of the background on the vertex detector of ILD from beamstrahlung. *Physics*, arXiv:0902.2707, 2010.

[10] J. Baudot. Future of low mass pixel systems with MAPS. *Presented at the 19th International Workshop on Vertex Detectors Vertex 2010*, June 2010.

[11] T. Sluka et al. ATLAS pixel detector commissioning. *Nucl.Instr.Meth.*, A607:27–30, 2009.

[12] N. Wermes. Pixel detectors for charged particles. *Nucl.Instr.Meth.*, A604:370–379, 2009.

[13] A. Andreazza. Test beam performance of the ATLAS pixel detector modules. *Nucl.Instr.Meth.*, A565:23–29, 2006.

[14] A. Dorokhov et al. Improved radiation tolerance of MAPS using a depleted epitaxial layer. *Nucl.Instr.Meth.*, A624(2):432–436, Dec 2010.

[15] G. Rizzo et al. Development of deep n-well MAPS in a 130 nm CMOS technology and beam test results on a 4k-pixel matrix with digital sparsified readout. *Nuclear Science Symposium Conference Record, IEEE*, Dresden, Germany:3242–3247, 2008.

[16] G. Traversi et al. First generation of deep n-well CMOS MAPS with in-pixel sparsification for the ILC vertex detector. *Nucl.Instr.Meth.*, A604(1):390–392, June 2009.

[17] G. Traversi et al. Status and perspectives of deep n-well 130 nm CMOS MAPS. *JINST*, 4, 2009.

[18] J. Ballin et al. Monolithic active pixel sensors (MAPS) in a quadruple well technology for nearly 100% fill factor and full CMOS pixels. *Sensors*, 8:5336–5351, 2008.

[19] P. Dauncey. Performance of CMOS sensors for a digital electromagnetic calorimeter. *Presented at the 35th International Conference of High Energy Physics*, Paris, July, 2010.

[20] G. Nicola Carlo. CMOS solutions for scientific imaging and INMAPS technology. *Presented at the 8th International Meeting on Front-End Electronics*, Bergamo, Italy, May, 2011.

[21] N. B. Sinev. Status of the chronopixel project. *Presented at LCWS11 workshop*, Granada, Spain, September, 2011.

[22] I. Peric. A novel monolithic pixelated particle detector implemented in high-voltage cmos technology. *Nucl.Instr.Meth.*, A582(3):876–885, June 2007.

[23] I. Peric et al. Particle pixel detectors in high-voltage cmos technologyąłnew achievements. *Nucl.Instr.Meth.*, A650(1):158–162, 2011.

[24] R. Yarema and G. Deptuch. 3D and SOI integrated circuit design at Fermilab for HEP and related applications. *Presented at the NSLS/CFN user meeting*, Brookhaven, May, 2008.

[25] W. Deptuch. Vertically integrated circuits at Fermilab. *Nuclear Science, IEEE Transactions on*, 57(4):2178–2186, 2010.

[26] R. Yarema. Details of the first 3D-IC multi-project wafer run. *Nuclear science symposium conference record, IEEE*, Knoxville, USA, 2010.

[27] C. Guo-Hu et al. CMOS pixel sensor development: a fast readout architecture with integrated zero suppression. *JINST*, 4(4):1–10, 2009.

[28] A. Nomerotski et al. PLUME collaboration: ultra-light ladders for linear collider vertex detector. *Nucl.Instr.Meth.*, A650(1):208–212, 2010.

[29] C. Guo-Hu et al. First reticule size maps with digital output and integrated zero suppression for the EUDET-JRA1 beam telescope. *Nucl.Instr.Meth.*, A623(4):480–482, 2010.

[30] Light as a feather. *ILC newsline*, http://newsline.linearcollider.org.

[31] Y. Degerli et al. Development of binary readout CMOS monolithic sensors for MIP tracking. *Nuclear Science, IEEE Transactions on*, 56:354–363, 2009.

[32] A. Dorokhov et al. Optimization of amplifiers for monolithic active pixel sensors. *Proceeding of Topical Workshop on Electronics for Particle Physics.*, pages 423–427, September 2007.

[33] W. Dulinski. CMOS pixel sensors on high-resistivity substrate : process availability and the first experimental results. *Presented at the workshop on vertically integrated pixel sensors.*, Pavia, Italy, 2010.

[34] M. Deveaux et al. Radiation tolerance of a column parallel CMOS sensor with high resistivity epitaxial layer. *Presented at the 12th international workshop on radiation imaging detectors.*, Cambridge UK, July 2011.

[35] M. Szelezniak et al. Application-specific architectures of CMOS monolithic active pixel sensors. *Nucl.Instr.Meth.*, A568:185–190, 2006.

[36] M. Manghisoni et al. Impact of gate-leakage current noise in sub-100 nm CMOS front-end electronics. *Nuclear Science Symposium Conference Record, IEEE.*, 2007.

[37] K. Han; K. Lee; H. Shin;. Thermal noise modeling for short-channel MOSFETs. *Proceedings of the SSPD 2003 International Conference.*, September 2003.

[38] A. Han; S. M. Channel width and length dependent flicker noise characterization for n-MOSFETs. *Proceedings of the ICMTS 2001 International Conference.*, July 2002.

[39] Z. Nical et al. Reduction of rts noise in small-area MOSFETs under switched bias conditions and forward substrate bias. *Electron Devices, IEEE Transactions on.*, 5:1119–1128, 2010.

[40] M. Kite; N. Yale. Precise FPN compensation circuit for CMOS APS. *Electronics Letters.*, 38:1078, July 2002.

[41] W. Hute.; G. Micale.;. Noise transfer characteristics of a correlated double sampling circuit. *Circuits and Systems, IEEE Transactions on.*, 33:1028–1030, July 2003.

[42] R. Biter et al. Design techniques for high-speed, high-resolution comparators. *Solid-state circuits, IEEE journal.*, 27:1916–1926, 1992.

[43] W. Dulinski et al. CMOS monolithic active pixel sensors for minimum ionizing particle tracking using non-epitaxial silicon substrate. *Nuclear Science, IEEE Transactions on*, 51:1613–1617, 2004.

[44] M. Szelezniak. Development of pixel detectors with integrated microcircuits for the vertex detector in the STAR experiment at the RHIC collider. *thesis*, 2008.

[45] G. Deptuch et al. Vertically integrated circuits at fermilab. *Nuclear Science, IEEE Transactions on*, 57(4):2178–2186, 2010.

[46] A. Dorokhov et al. High resistivity cmos pixel sensors and their application to the star pxl detector. *Nucl.Instr.Meth.*, A623:192–194, 2011.

[47] W. Dulinski. CMOS pixel sensors on high-resistivity substrate: process availability and the first experimental results. *Presented at Workshop on Vertically Integrated Pixel Sensors VIPS*, April 2010.

[48] D. Park et al. MIRA: a multi-layered on-chip interconnect router architecture. *IEEE International symposium on computer architecture*, pages 251–261, 2008.

[49] R. Yarema. *3D Circuit Integration for Vertex and Other Detector*, Proceedings of the 16th International Workshop on Vertex Detectors, September 2007.

[50] G. Deptuch. Front end electronics using 3d integrated circuits. *Presented at the 7th International Meeting on Front-End electronics for Particle Physics*, May 2009.

[51] Vertically integrated circuits at Fermilab. *Nuclear Science, IEEE Transactions on*, 57(4):2178–2186, 2012.

[52] http://www.tezzaron.com.

[53] R. S. Patti. Three-dimensional integrated circuits and the future of system-on-chip designs. *Proc. IEEE*, 94(6):1214–1224, June 2006.

[54] R. S. Patti. 3D scaling to production. *Conf. 3D Architecture for Semiconductor Integration and Packaging*, Nov 2006.

[55] M. Winter. Occupancy of ILC-VD inner layer integrated over a complete bunch train. *internal note*, April 2008.

[56] L. Ratti et al. Design of time invariant analog front-end circuits for deep n-well CMOS MAPS. *Nuclear Science, IEEE Transactions on*, 56:2360, 2009.

[57] Y. Hu et al. A low-noise low power CMOS SOI readout front-end for silicon detectors leakage current compensation with capability. *IEEE Transactions on circuit and systems*, 48:1022, 2001.

[58] B. Razavi and B. A. Wooley. Design techniques for high-speed, high-resolution comparators. *IEEE. J. Solid-State Circuits*, 27:1916–1919, 1992.

[59] R. Yarema. 3D CMOS submission. *Presented at the 8th International Meeting on Front-End Electronics*, 2011.

[60] W. Dulinski et al. Thin, fully depleted monolithic active pixel sensor with binary readout based on 3D integration of heterogeneous CMOS layers. *IEEE Nuclear Science Symposium Conference Record*, Oct 2009.

[61] D Passeri et al. 3D monolithically stacked CMOS active pixel sensor detectors for particle tracking applications. *JINST*, 7, August 2012.

[62] M. Winter. From 2D to 3D MAPS. *Presented at Workshop on Vertically Integrated Pixel Sensors*, Italy, 2010.

[63] C. Hu-Guo et all. First reticule size MAPS with digital output and integrated zero suppression for the EUDET-JRA1 beam telescope. *Presented at TIPP 2009*, 12-17 March 2009.

[64] A. Dorokhov et al. Improved radiation tolerance of MAPS using a depleted epitaxial layer. *Proceedings of the 11 th European Symposium on Semiconductor detectors*, 2009.

[65] Y. Degerli et al. A 3D integrated rolling shutter mode MAPS with in-pixel digital memory and delayed readout. *IEEE Nuclear Science Symposium Conference Record*, 2009.

[66] M. Winter. M.i.p. detection performances of a 100 us read-out CMOS pixel sensor with digitised outputs. *Physics*, arXiv:0902, 2009.

[67] W. Dulinski et al. Optimization of tracking performance of CMOS monolithic active pixel sensors. *Nuclear Science, IEEE Transactions on*, 54(1), 2007.

[68] I. Peric et al. The FEI3 readout chip for the ATLAS pixel detector. *Proceedings of the International Workshop on Semiconductor Pixel Detectors for Particles and Imaging*, 565:178–187, September 2006.

[69] Y. Degerli et al. A fast monolithic active pixel sensor with pixel-level reset noise suppression and binary outputs for charged particle detection. *Nuclear Science, IEEE Transactions on*, Dec 2005.

[70] Y. Degerli et al. Design of fundamental building blocks for fast binary readout CMOS sensors used in high-energy physics experiments. *Nucl.Instr.Meth.*, A602:461–466, 2009.

[71] S. Smith; J. Hurwitz; M. Torrie; D. Baxter; A. Holmes; M. Panaghiston; R. Henderson; A. Murray; S. Anderson; P. Denyer. A single-chip 306 X 244-pixel CMOS NTSC video camera. *ISSCC Digest of Technical Papers*, pages 170–171, February 1998.

[72] M. Loinaz; K. Singh; A. Blanksby; D. Inglis; K. Azadet; B. Acland. A 200 mw 3.3 v CMOS color camera IC producing 352 X 288 24b video at 30 frames/s. *ISSCC Digest of Technical Papers*, pages 169–186, February 1998.

[73] S. Decker; R. McGrath; K. Brehmer; C. Soldini. A 256 X 256 CMOS imaging arrays with wide dynamic range pixels and column-parallel digital output. *ISSCC Digest of Technical Papers*, pages 176–177, February 1998.

[74] A. Krymski and N. Tu. A 9-V/lux-s 5000-frames/s 512 X 512 CMOS sensor. *IEEE Trans. Electron Devices*, 50:136–143, 1998.

[75] A. Krymski and N. Tu. A low power and low signal 5-bit 25 MS/s pipelined ADC for monolithic active pixel sensors. *Nuclear Science, IEEE Transactions on*, 4:1195–1200, 2007.

[76] I. Valin et al. A reticle size CMOS pixel sensor dedicated to the STAR HFT. *JINST*, 7(C01102), 2012.

[77] D. Yang; B. Fowler; A. El Gamal. A nyquist-rate pixel-level ADC for CMOS image sensors. *Solid-State Circuits, IEEE Journal of*, 3:348–356, 1999.

[78] D. Maricic; Z. Ignjatovic; M. Bocko;. An oversampling digital pixel sensor with a charge transfer DAC employing parasitic capacitances. *Presented at the 52nd IEEE International Midwest Symposium on*, 623:415–418, 2009.

[79] C. Hu-Guo et al. First reticule size maps with digital output and integrated zero suppression for the EUDET-JRA1 beam telescope. *Nucl.Instr.Meth.*, 623:480–482, November 2010.

[80] L. Staller. Understanding analog to digital converter specifications. *internal note*, 2005.

[81] K. Ito; B. Tongprasit; T. Shibata;. A computational digital pixel sensor featuring block-readout architecture for on-chip image processing. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 56:114–123, Jane 2009.

[82] M. Dahoumane et al. A low power and low signal 4 bit 50MS/s double sampling pipelined ADC for monolithic active pixel sensors. *JINST*, 3:114–123, 2008.

[83] K. Hansen et al. Pixel-level 8-bit 5-MS/s wilkinson-type digitizer for the DSSC X-ray imager: Concept study. *Nucl.Instr.Meth.*, A629:269–276, February 2011.