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Design of a low noise, limited area and full on-chip power management for CMOS pixel sensors in high energy physics experiments

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Better to light a candle than to curse the dark.

—*Chinese proverb*

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Résumé

Capteurs à pixels CMOS (CPS, aussi appelés capteurs monolithiques à pixels actifs) offrent un compromis attirant entre le budget matériel, la tolérance au rayonnement, la consommation d'énergie et la granularité. L'autre avantage est que les CPS peuvent être émincés à 50 μm, ce qui est utile pour diminuer le budget matériel. Le CPS est un bon choix pour détecter les particules chargées dans les détecteurs de vertex. Par exemple, les puces CPSs va équiper le détecteur PXL en «heavey flavor tracker» (HFT) de «Solenoidal Tracker at RHIC (STAR) experiments» (illustré à la figure 1.).Une série des puces CPSs appelées MIMOSA (« Minimum Ionising particle MOS Active sensor») ont été conçus et évalués par le groupe de micro-électronique à l'IPHC (Institut Pluridisciplinaire Hubert Curien), Strasbourg, France, depuis les années 1990. Ce travail de thèse est une partie de la conception des CPS à l'IPHC et dédiée à la gestion de l'alimentation. Ce bloc fournit les tensions nécessaires à les autres circuits, tels que la matrice de pixels et les discriminateurs, etc.

La stratégie de distribution de puissance pour les CPS est d'abord recherchée. Comme l'approche traditionnelle, les alimentations sont indépendantes. Ils échouent. Puisque plus de capteurs va équiper dans le détecteur, le nombre des cb̂les a fortement augmenté. Le budget de matériel ne peut pas satisfaire à l'exigence. En outre, il y aura plus de l'énergie consommé par les cb̂les. Par conséquent, l'efficacité énergétique des systèmes de détection est réduite à une valeur inacceptable. Il y a principalement deux approches alternatives, telles que les alimentations en série et la conversion DC-DC. Puisque les alimentations en série ne sont pas compatibles avec la conception récente des CPS, la conversion DC-DC est utilisée. Comme le montre la figure 2, un convertisseur abaisseur «Buck» DC-DC fournit des alimentations à plusieurs puces de capteurs. Puis, la tension de sortie entre dans la gestion de l'alimentation de chaque puce CPS, où les tensions d'alimentation analogique et numérique sont générées. En outre, il y a quelque tensions critiques utilisées dans les puces CPSs. Les références de tension doivent être à faible bruit en raison du très faible signal détecté. Des cb̂les sont nécessaires si ces tensions sont fournies extérieurement. Toutefois, les puces CPSs sont montées à proximité dans le «ladder». La diaphonie apparaît parmi les puces de détection. Le bruit peut être injecté

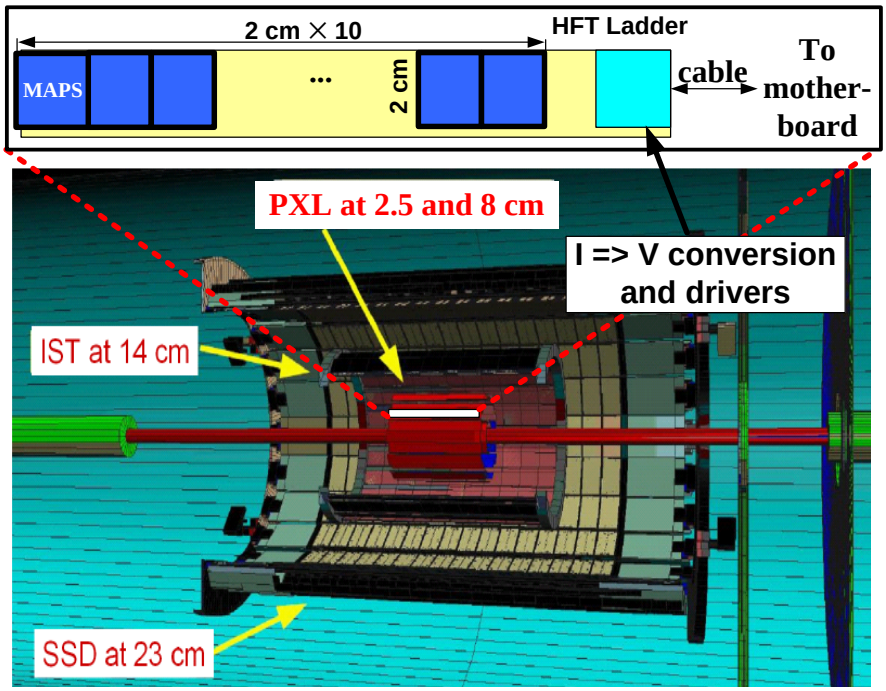


Figure 1: *Schéma de le HFT et le PXL équipée par les puces CPSs.*

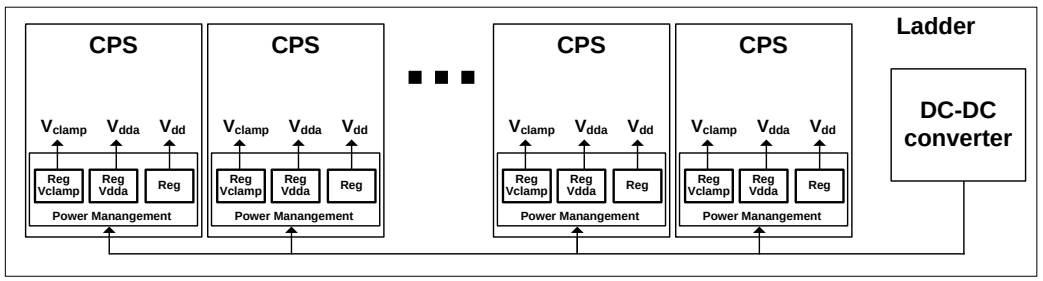


Figure 2: *La distribution de puissance pour les CPS dans un «ladder».*.

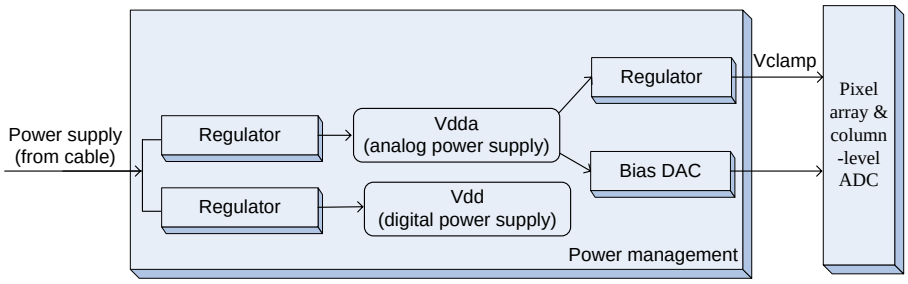
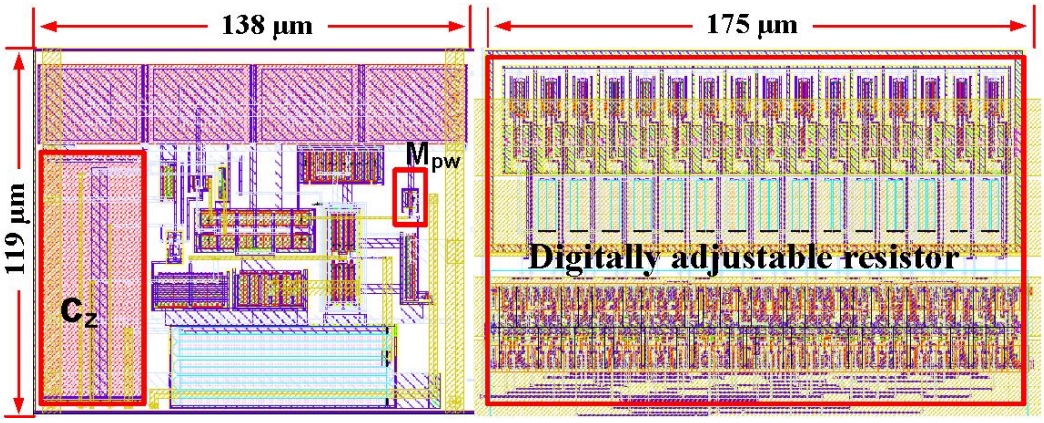


Figure 3: *Diagramme simple de la gestion de l'alimentation dans le CPS.*

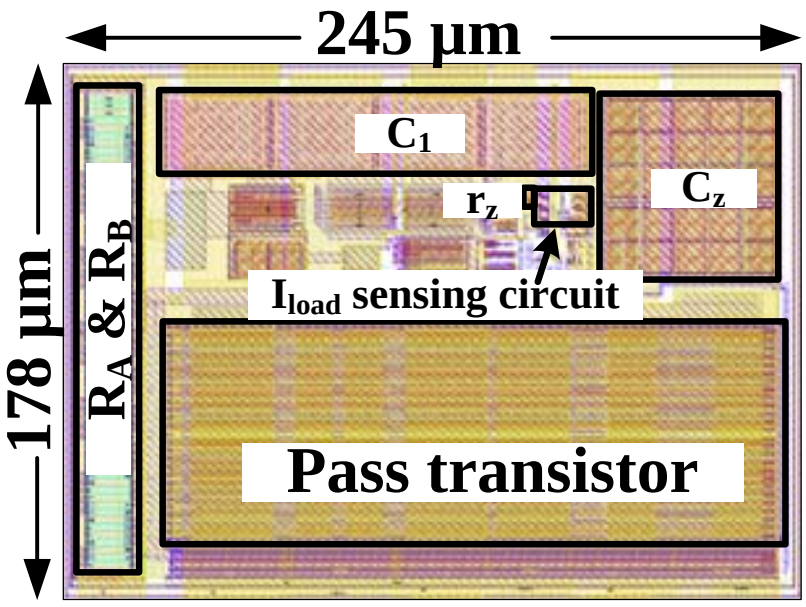
dans les références de tension. Le condensateur de filtrage peut être utilisé pour diminuer le bruit. Toutefois, le budget de matériel est augmenté et la conception «ladder» est compliquée. En conséquence, certaines tensions critiques sont générées dans la gestion de l'alimentation comme l'indique la figure 3.

Le régulateur à faible chute de tension (LDR) est un élément essentiel dans le système d'alimentation. Le bruit et la taille limitent l'application de l'alimentation à découpage, bien qu'elle puisse atteindre un rendement élevé. En outre, il est difficile d'intégrer un inducteur ou un grand condensateur dans la puce. Le LDR comporte généralement une faible chute de tension, un faible bruit et une petite taille. Puisque les circuits analogiques sont sensibles au bruit, les LDRs sont utilisés pour fournir la tension d'alimentation analogique et les références de tension. Afin d'augmenter le rendement élevé, le convertisseur à capacités commutées est utilisé. Le LDR peut également supprimer le bruit de commutation du convertisseur d'abaisseur DC-DC. Toutefois, certains défis sont portés à la conception LDR dans les CPS. La stabilité doit être analysée attentivement, parce que tout élément extérieur n'est pas autorisé en vue de réaliser la conception de sur-puce pleinement. En outre, le bruit et la consommation de l'alimentation devraient être faible. La tolérance au rayonnement doit être également concernée. Deux LDRs sont conçus et évalués dans ce travail de thèse (illustré à la figure 4.). Un régulateur dit «RegVclamp» est utilisé pour fournir la tension de «clamping», qui est utilisé pour le fonctionnement à double échantillonnage corrélé. L'autre régulateur dit RegVdda est utilisé pour fournir la tension d'alimentation analogique.

Une structure basée sur l'annulation de pôle-zéro et l'optimisation de la conception est proposée afin de satisfaire toutes les exigences. Les deux régulateurs sont vérifiés par les deux prototypes. Le RegVclamp est intégré dans MIMOSA22HRE afin d'offrir la tension de clamping à la puce du capteur. Les résultats des mesures montrent que seulement 5,8% du bruit est augmenté par le RegVclamp, qui peut satisfaire à l'exigence du bruit. Il est également vérifié par la puce ULTIMATE, dans lequel la capacité parasite



(a)



(b)

Figure 4: *Disposition des RegVclamp (a) et RegVdda (b).*

est différente avec MIMOSA22HRE. La plupart de capacité de charge de RegVclamp vient de la capacité parasite. Il est d'environ 0,5 nF dans le MIMOSA22HRE et 5 nF dan l'ULTIMATE. Les résultats démontrent que le RegVclamp peut travailler avec un large éventail de capacités de charge. Ainsi, il peut être réutilisé dans les puces CPSs avec les matrices de pixels différents. L'ENC («Equivalent Noise Charge») du pixel est inférieure à 15 e^-, lorsque la tension de «clamping» est fournie par RegVclamp. Il peut satisfaire aux exigences des puces CPSs.

Afin de générer la tension d'alimentation analogique, le RegVdda est conçu. Puisque le courant de charge varie dans une large gamme, tous les pôles et les zéros sont réglables pour garantir la stabilité. Une nouvelle structure est proposée. Une résistance et un condensateur sont connectés en série, qui introduit un zéro dans le demi-plan de gauche. En outre, deux rétroactions de courant sont utilisées pour adapter la valeur de la résistance dans le réseau série et la transconductance du tampon à la mi-étape. Ainsi, tous les pôles et les zéros déplacent à la même direction que le pôle de sortie fait. Le condensateur de compensation utilisé est diminué dans ce régulateur. En outre, le transistor de sortie travaille dans la région à faible inversion et la région linéaire à faible charge et à charge élevée respectivement. Ainsi, la dimension du transistor de sortie est diminuée et le courant de polarisation est aussi diminué. Afin d'atteindre la tolérance au rayonnement, le circuit est fabriqué dans un procédé à la couche épitaxiale avec haute-résistance. En outre, chaque transistor est entouré par l'anneau de garde. Le RegVdda a été intégré dans la puce ULTIMIATE comme un circuit optionnel. Les résultats des mesures montrent que ce régulateur est stable dans la gamme du courant de charge (0 - 200 mA) lorsque la capacité de charge est de 200 nF et 300 nF. Le «power supply rejection» (PSR) est au-dessus de 20 dB à la fréquence de 1 MHz. Le bruit testé est d'environ 65 $nV/\sqrt{Hz}$ à la fréquence de 100 kHz. Toutefois, la chute de tension est de 0,3 V à cause du petit transistor de sortie. Afin de diminuer la chute de tension, un régulateur optimisé a été conçu et il peut fournir jusqu'à 300 mA du courant de charge. Un limiteur de courant a été conçu pour protéger le régulateur et les autres blocs des CPS. Un comparateur de courant est conçu afin de comparer le courant détecté et le courant de seuil. La sortie sera égale à «0» si le courant de charge est supérieur à 460 mA. Il permet de couper le courant d'alimentation. Ce régulateur optimisé est intégré dans le MIMOSA30. Les résultats simulés montrent que la chute de tension est inférieure à 200 mV. La performance PSR est également meilleure. La stratégie de gestion de l'alimentation pour CPS est également étudiée. Différent avec l'électronique grand public, les CPS sont limités par le procédé de fabrication. Toutefois, quelques stratégies de gestion de l'alimentation sont basées sur le processus. En outre, la performance est plus importante que la consommation

d'énergie. Ainsi, le compromis entre la performance et la consommation d'énergie devrait être considérée. Une gestion de l'alimentation basée sur les états de travail est proposée dans les CPS. Les alimentations des blocs inutilisés sont coupées dans l'état de veille. Dans le développement du futur, le convertisseur à capacités commutées sera conçu et intégré dans la gestion de l′alimentation. La tolérance aux radiations des transistors de très grande taille sera analysée et testée.

ABSTRACT

What are the elementary particles and how did the universe originate are the main driving forces in the high energy physics. In order to further demonstrate the standard model and discover new physics, several detectors are built for the high energy physics experiments. CMOS pixel sensors (CPS) can achieve an attractive tradeoff among many performance parameters, such as readout speed, granularity, material budget, power dissipation, radiation tolerance and integrating readout circuitry on the same substrate, compared with the hybrid pixel sensors and charge coupled devices. Thus, the CPS is a good candidate for tracking the charged particles in vertex detectors and beam telescopes.

The power distribution becomes an important issue in the future detectors, since a considerable amount of sensors will be installed. Unfortunately, the independent powering has been proved to fail. In order to solve the power distribution challenges and to provide noiseless voltages, this thesis focuses on the design of a low noise, limited area, low power consumption and full on-chip power management in CPS chips. The CMOS pixel sensors are firstly introduced drawing the design requirements of the power management. The power distribution dedicated to CPS chips is then proposed, in which the power management is utilized as the second power conversion stage. Full on-chip regulators are proposed to generate the power supply voltages and the reference voltage required by correlated double sampling operation.

Two full on-chip regulators have been designed and measured. One regulator provides the reference voltage required by correlated double sampling operation, functioning as a reference generator. It is implemented by a three-stage linear regulator. As the mid-stage, the buffer isolates the high output impedance of error amplifier from the large input capacitor of pass transistor with the aim of pushing the relevant poles to high frequency and improving the transient response. Moreover, a series RC network is employed to introduce a zero compensating the phase. The generator is stable with the load capacitance of 0.5 nF - 10 nF, without any external elements. The average noise value amounts to $\leq 15e^-$ ENC (equivalent noise charge) at 20^o and 40 MHz readout clock frequency, when the clamping voltage is internally generated. The output voltage is programmable at the voltage step of 20 mV for testing flexibility. The chip area is about 313 $\mu m\times$ 119 μm.

Based on the reference generator, a linear regulator is designed to provide the analog supply voltage. Since the current required by CPS chips varies in a large range, a novel structure is proposed. All the poles and zeros are adaptable to move as the output pole does, which is implemented by a current sensing circuit and a current feedback circuit. The measurement results demonstrate that the regulator can be stable in the full range of the load current with the estimated parasitic capacitor in CPS. The power supply rejection

at high frequency is also improved due to the large bandwidth. The measured noise is 340 $nV/\sqrt{Hz}$ and 65 $nV/\sqrt{Hz}$ at 1 kHz and 100 kHz, respectively, when the load capacitor is about 200 nF. The quiescent current is 147 mA and 314 mA at the load current of 0 and 200 mA, respectively.

Two prototypes have verified these regulators. They can meet the requirements of CPS. Moreover, the power management techniques and the radiation tolerance design are also presented in this thesis.

Keywords: CMOS pixel sensors (CPS), Full on-chip, Linear regulator, Low noise, Low dropout (LDO) regulator, Monolithic active pixel sensors (MAPS), Power management.

Chapter 1

Introduction

The integrated circuits have been developing rapidly since 1958 when the first integrated circuit was invented by Jack Kilby. They have been essential in our living from the portable electronics to the large electronic instruments. Silicon is also a good material for sensing due to its proper energy gap. For example, the complementary metal-oxide semiconductor (CMOS) imaging sensors have been widely used in digital cameras for sensing the visual light. Moreover, the doped silicon can react with high energy particles and left electron-hole pairs while they traverse the silicon. In order to rebuild the trace and measure the energy of the high energy particles, the sensor chips are also essential to be employed in high energy physics experiments.

In this chapter, the research background will be presented at first. Then the doctoral work is proposed in brief. At last the layout of this thesis is given.

1.1 Research background

1.1.1 High energy physics (HEP)

High energy physics (HEP), also called particle physics or elementary particle physics, is looking for the smallest constituents of matter (elementary particles) and for the fundamental forces between them. As called, atoms were considered as the fundamental building blocks of all forms of matter until the beginning of 20^{th} century. The experiments of Rutherford and the others proved that atoms were composed of protons, neutrons and electrons in 1900's. The atoms consist of mostly empty space with electrons surrounding a dense central nucleus made up of protons and neutrons. By the early 1960s, as accelerators reached higher energies, a hundred or more types of particles were discovered

Table 1.1: *Force and their carries.*

Force	Gauge Boson
Strong	Gluon (g)
Electromagnetic	Photon(γ)
Weak	$W^{\pm}, Z$
Gravity	Graviton (G)

in many series experiments [1]. Nucleus are thought to be composed of quarks. It is still an unanswered question that what are the fundamental particles. It becomes more clear when "Standard Model" was built late in the last century, which should be further proved by further experiments. Modern particle physics research focus on the subatomic particles, including atomic constituents and particles produced by radioactive and scattering processes. The atomic constituents contain electrons, protons and neutrons. Some particles can be produced in the radioactive and scattering processes, such as photons, neutrinos and muons. They also interest the particle physicists.

The fundamental forces refer to the interactions between fundamental particles. It is considered that Strong Force, Weak Force, Electromagnetism and Gravity are the four different types of forces in the nature. These forces can be regarded as being transmitted through the exchange of particles, which are called gauge bosons. The carriers of the four forces are shown in Table 1.1.

1.1.1.1 Standard model

In 1970s, the "Standard Model" was built to describe the role of the fundamental particles and the interactions between them [2]. In this model, the considered fundamental particles are divided into two classes according to the spin value, the fermions and the bosons, as shown in figure 1.1. The fermions have half integer spin while the bosons have an integer spin. The bosons are the carrier particles of weak, strong, gravity and electromagnetic forces. The fermions contain quarks and leptons, which are considered as the fundamental constituents of matter. Each particle has its corresponding anti-particle having the same properties except the opposite charge and opposite sign of the quantum numbers, so 6 quarks and 6 leptons are included. Moreover, quarks usually cannot be observed in nature and have to combine to form hadrons.

The Standard Model has successfully explained many experimental results and predicted a lot of phenomenons in the past few years. However, it still needs to be further developed and demonstrated by more experiments.

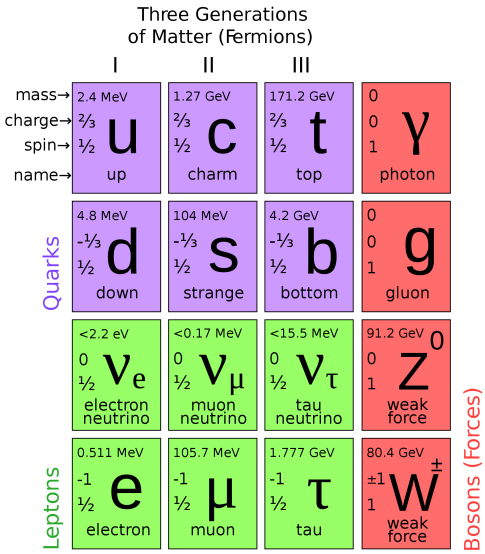


Figure 1.1: *Elementary particles and their interaction in Standard Model.*

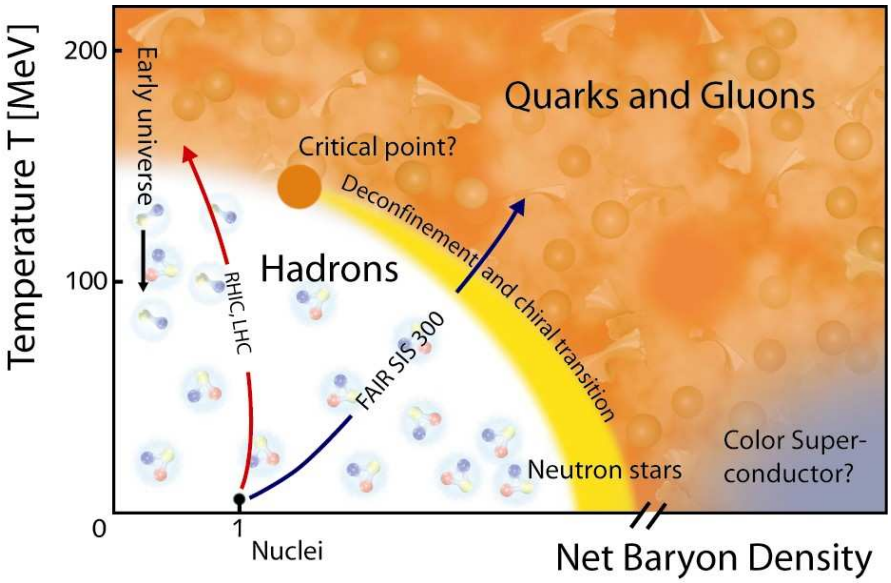


Figure 1.2: *Phase diagram of nuclear matter as a function of the temperature and the baryonic density.*

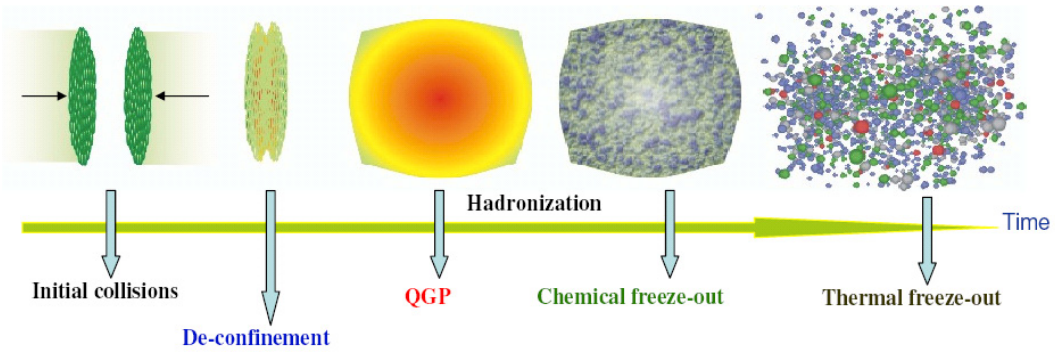


Figure 1.3: *Schematic view of the heavy ion collision with time evolution.*

As a part of the Standard Model, Quantum ChromoDynamics (QCD) is the universally accepted theory to describe the strong interactions, which happen among the quarks, gluons and nucleons [3]. However, the non-perturbative aspects of QCD are still not well understood, as well as the explaining of the quark confinement. According to the phase diagram in figure 1.2, the hadronic matter is expected to enter a deconfined phase, when the temperature and/or baryonic density increase. The deconfined phase may have plasma characteristics. The quarks become free over a large volume. This phase is called Quark-Gluon Plasma (QGP). Its occurrence has been predicted by QCD. However, it has not been observed in the experiments yet. QGP is also expected to occur in the universe after a few microseconds of Big Bang and the neutron stars nowadays. Therefore, studying the formation and characteristics of QGP allows us to well understand non-perturbative aspects of strong interaction, early universe and many astrophysical processes.

It is believed that QGP can be reproduced in the reaction zone of a heavy ion collision, which is the only way to reproduce QGP in laboratory. As shown in figure 1.3, a volume of hot and dense matter called fireball are produced in the initial collisions and then de-confinement evolved to thermal QGP. The main experiments related to QGP are operated at Brookhaven National Laboratory (BNL), New York in USA and at Conseil Européene pour la Recherche Nucléaire) (CERN), Geneva in Switzerland.

1.1.1.2 HEP experiments

In order to verify the Standard Model and search the new physics beyond it, HEP experiments have been built. The QGP is also expected to be reproduced and observed in the HEP experiments. The main idea of HEP experiments is to accelerate, collide two particles and observe what comes out and try to guess what was in [4]. Unlike the other

Figure 1.4: *The bird's eye view of LHC at CERN.*

Figure 1.5: *The bird's eye view of RHIC.*

physics experiments where a theory can be verified by a single measurement, a variety of simultaneous studies are used in the high energy physics experiments to draw strong conclusions. Thus, a great amount of elementary particles such as electrons or hadrons are accelerated by the accelerator and periodically collided [5]. The accelerator is composed of the source, the electric field and the magnetic field. Then the tracks and energy of the particles produced in the collisions are measured and stored with kinds of detectors. The aims of the detectors are to find the tracks of the particles, measure their energy and identify them. Especially, some of them have to be near to the point of the particles' interactions. The dedicated colliders for high energy physics experiments have been built and operated already, for example, the Brookhaven National Lab's relativistic heavy ion collider (RHIC), the large hadron collider (LHC) at CERN (shown in figure 1.4) and the Tevatron in Fermi National Accelerator Laboratory (shown in figure 1.6), which was shut down in September 2011.

In order to detect the particles at a full coverage, the detector is formed as a barrel.

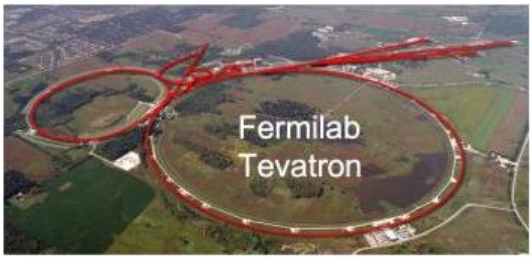


Figure 1.6: *The bird's eye view of Tevatron.*

This barrel is composed of several subsystems to track different particles. As an example, the layout of the Solenoidal Tracker At RHIC (STAR) detector is depicted in figure 1.7 [6]. The detector is composed of Silicon Vertex Tracker (SVT), Time Projection Chamber (TPC), Trigger Barrel, ElectroMagnetic Calorimeter (EMC), Magnet and Coils. The SVT tracks the charged particles close to the interaction region. It should be precise sufficient to locate the primary interaction vertex and identify the secondary vertices. The large volume TPC also tracks the charged particles and identifies them with SVT using ionization energy loss. The Trigger Barrel acquires the data from multiple detectors. EMC measures the transverse energy of events and trigger on and measure high transverse momentum photons, electrons and electromagnetically decaying hadrons. The Magnet and Coils create a strong magnetic field in order to analyze the momentum of charged particles. The maximum value is about 0.5 T.

1.1.2 Silicon detector topologies

Full-custom detectors are required in the HEP experiments due to the extreme environment, which are usually composed of many layers. The vertex detector is the detector nearest to the collision point, which detects and records the position of the charged particles when they pass through. Almost all the physical results rely heavily on the performance of vertex detectors [7]. Since very high spatial resolution, high readout speed and low material budget are required by vertex detector, silicon detectors are usually used in the vertex detector. The charged particles can be detected by the silicon detectors due to the electron/hole pairs induced by them. The collision produces many particles in a very short period of time. Thus, the vertex detector works in a harsh radiation environment.

The silicon sensors that are most commonly used in vertex detectors are hybrid pixel detectors, microstrip detectors, charge coupled devices, Si drift detectors, pad detectors and CMOS pixel sensors. The hybrid pixel detectors, charge coupled devices and CMOS pixel sensors are introduced in detail in following sections.

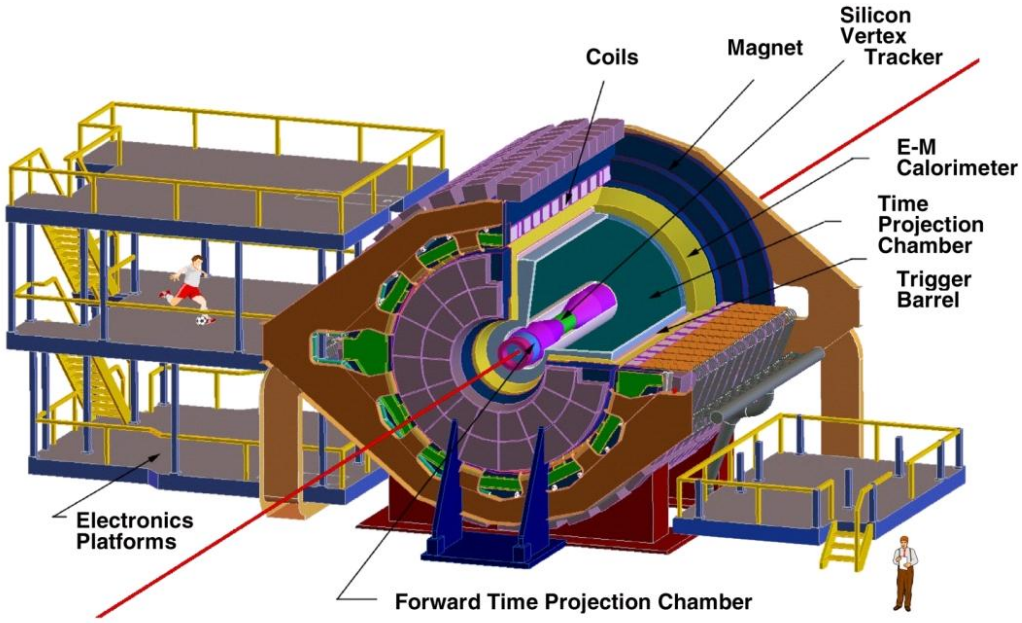


Figure 1.7: *The layout of STAR detector and the cutting view showing the inner detector [6].*

1.1.2.1 Hybrid pixel detectors

Hybrid pixel detectors are composed of two parts: the sensor chip and the readout chip, as shown in figure 1.8 [8]. The sensor detects the signal and transfers it to the readout chip. The sensor chip is built on the high-resistivity silicon substrate. Its active volume is fully depleted by applying an appropriate voltage to the back side. This structure can achieve high spatial resolution and good radiation hardness. The readout chip is usually based on the standard CMOS technology and they can be highly optimized to achieve high readout speed. Combining these two layers, the detectors can achieve attractive radiation hardness, spatial resolution and readout speed. Hybrid pixel detectors have been successfully employed in the pixel detectors for HEP experiments such as WA97, which is a heavy ion experiment to study Pb-Pb collisions at the CERN Omega spectrometer [9]. They are also currently used in ATLAS, ALICE and CMS for LHC experiments with the pixel size of 50 $\mu s\times$ 400 μs, 50 $\mu s\times$ 425 μs, 150 $\mu s\times$ 150 μs, respectively [10] [11] [12]. They are the promising candidates employed in the pixel detectors for HEP experiments owing to their excellent radiation hardness.

However, the hybrid pixel detectors have some disadvantages which limit their applications in HEP experiments. The bump-bonding flip-chip bonding techniques are usually used to connect the sensor chip and the readout chip [13] and each pixel cell of sensor has

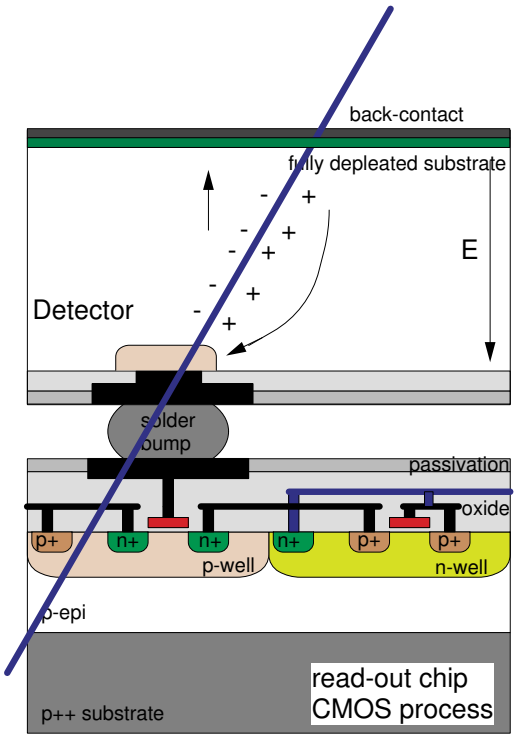


Figure 1.8: *The architecture of hybrid pixel sensor [8].*

its own readout circuit. They are connected via the bump bond. The minimum pixel size is thus limited by the readout electronics and the bump size. The interconnection is also very complex. Moreover, the material budget is high due to the thickness of the sensor chip, bumps and the readout chip. Since large voltage is applied to the sensor, hybrid pixel detectors also suffer high power consumption.

1.1.2.2 Charge coupled devices (CCD)

The charge coupled devices were invented in 1970 by Willard Boyle and George Smith at Bell Laboratories, USA [14] [15]. CCDs have found their applications in the cameras, scanners, cell phones and personal computers in the following years. Most of the imaging devices utilize CCDs as the visual light sensors. They are also used in the space imaging and in high energy physics experiments for tracking particles. As the vertex detectors of NA32 at CERN, the SPS and SLD are equipped with CCDs owning to their high spatial resolution and thin thickness.

CCD is an array of MOS capacitors tightly covering on the substrate. A pixel is composed of three gates, as shown in figure 1.9. Only one gate voltage is high while the other two are low. Thus, a potential well forms. The charged particle induces electron/hole

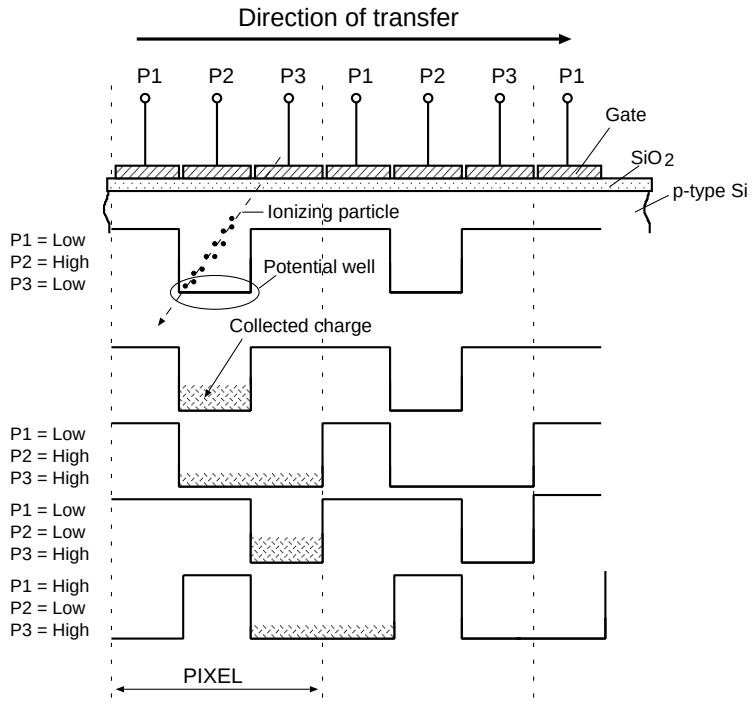


Figure 1.9: *Structure of CCD and the operation timing.*

pairs in the depleted layer under the gate, when it traverses the device. Electrons are collected and stored in the potential well. Then the charges stored in one capacitor can be transferred in the channel of the adjacent device by a appropriate voltage consequence at their gate nodes. The signal is serially read out leading to relatively low readout speed. This will be worsened for a larger pixel array.

The main structures of CCD are the surface-channel and buried-channel. The buried-channel is mostly used, which is not compatible with standard CMOS technology. The gate voltage to transfer the charge is usually high to 10 V. Thus, CCDs can not be integrated on the same substrate with readout circuitry.

Since the performances of CCDs depend on the perfect charge transferring, they are very sensitive to the radiation damage. This drawback limits their applications in the high energy physics experiments.

1.1.2.3 CMOS pixel sensors or Monolithic active pixel sensors

In the early 1990s CMOS sensors were used in visual imaging such as the commercial cameras, video recorders and so on. They can be fabricated in the standard commercial CMOS technology. Thus the sensing elements and the readout circuitry can be integrated

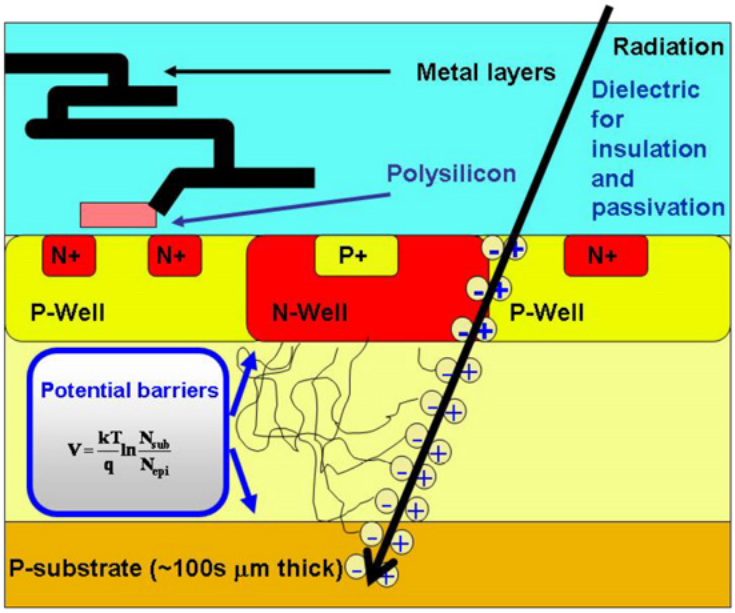


Figure 1.10: *Schematic cross-section of a CMOS pixel sensor [16].*

on the same substrate. They decrease the cost and the chip area. They rapidly develop in the consumer electronics and they are predicted to replace CCD in the future. The CMOS pixel sensors (CPS) were firstly proposed to detect the charged particles in 1999 in IPHC - Strasbourg, France. They have been verified and proved by a series of prototypes called Minimum Ionizing particle MOS Active pixel sensors (MIMOSA) [17]. The test results demonstrated that they had promising features for charged particle tracking. The cross-section of a CMOS pixel sensor is shown in figure 1.10 [16]. Different with the standard substrate in VLSI technology, the substrate is highly doped as p^{++} and the lightly doped epitaxial layer is thicken. The photodiode is formed by the junction between the p-epitaxial layer and the N-well. The electron/hole pairs are generated along the trajectory of the ionizing particle when it traverses the sensor. Recombination finishes very quickly in the substrate, so the particles in the p-epitaxial moves to the highly doped n-well. The current can be integrated by the revers-biased diodes through thermal diffusion during about 100 ns.

The structure of CPS is shown in figure 1.11. CPS are composed of a pixel array, column-level discriminator, bias DACs, power management/regulators, phase locked loop (PLL), zero suppression, memories, sequencer and sequencer controller. The pixel array takes the most of area in CPS. The pixel cell integrates the current induced by the ionizing particle and pre-amplifies the signal. The output analog voltage is digitalized by the discriminator, which is a comparator in fact. When the signal amplitude is higher

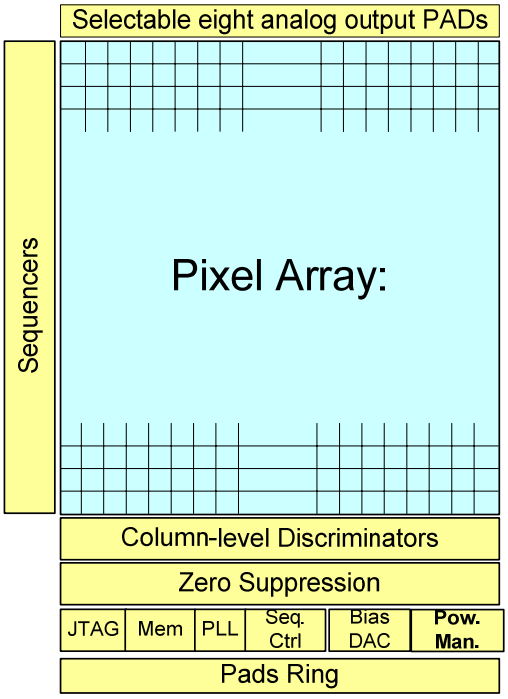


Figure 1.11: *Structure of CPS chip.*

than the threshold, the output is "1". It indicates that one particle may traverse this pixel. Its position can be reconstructed by dedicated algorithms in the following data analysis procedure. To improve the readout speed, the digitalization is parallel done in column level. The aim of zero suppression is to delete the information of the pixel not hit. Thus, the speed and power consumption is significantly decreased. The regulators generate the low-noise reference voltage and the power supply voltage on chip, which is the main work in these thesis. The bias DACs generate bias voltages for other blocks. Utilizing the JTAG interfaces, the bias voltage and current can be adapted to get the optimized value and make tests flexible. The PLL generates the reading clock. The sequencer and sequencer controller provide the correct timing in successive mode.

The comparison of CPS with CCD and hybrid pixel sensors is shown in Table 1.2. CPS can offer an attractive trade-off among the granularity, material budget, readout speed, radiation tolerance and power consumption. The material budget can be further decreased since the sensor chip can be thinned down to 50 μm. The hardening by design (HBD) has improved the radiation tolerance in CMOS process. This technology can meet the requirements of most of the high energy physics experiments. Consequently, CPS is a good choice of the sensors used in vertex detectors.

Table 1.2: *The performance comparisons of CPS with the competitions*

CPS and competitions	CPS	Hybrid pixel sensors	CCD
Granularity	+	-	+
Material budget	+	-	+
Readout speed	+	++	-
Radiation tolerance	+	++	-
Power consumption	+	-	+

1.1.3 Power distribution challenges in the detectors

The independent powering is used in the recent detectors. Each electronics (sensor/readout circuit) is powered directly from power supply located remotely by its own cables. The length of the cables can be longer than dozens of meters. There maybe more than one cable for one electronics, e.g., the analog supply voltage, digital supply voltage and bias voltage. In order to decrease the material in the active volume, thinner cables are used. The resistance of the cables cannot be ignored. Moreover, the electronics requires high current while working. Much power is burnt by the cables due to the unwanted resistive heating I^2R_{cable}. This problem also influences the cooling system. The detectors will be equipped with more sensors in the future, which make the things worse. The independent powering has been proved failed for the future detectors [18]. The reasons are listed as follows:

1. Lack of space to place cables. The cables increase with the number of electronics. For example, the channels increase by a factor of 2-10 in the SLHC. Since the vertex detector is close to beam, the space is limited by the radius of the detector. Moreover, it is impossible to place all the cables in the detector if extreme low material budget is required.

2. Increase of the material budget. It is undoubted that the material budget increases when a large amount of cables are placed in the active material. However, the material budget is required low enough to decrease the multiple scattering, which impacts the momentum and the resolution of the low-momentum particles.

3. Low power efficiency. As mentioned above, the resistive heating significantly increases with the number of the cables. The cables consume higher than 50% of the total power, for example, the power efficiency of the Pixels detector for ATLAS in LHC is only 20%.

Consequently, power distribution becomes a large challenge in the detectors. The new schemes must be designed for the future detectors to decrease the number of the cables. Furthermore, any electronics in the power distribution must be able to work in the harsh radiation and magnetic environment due to close the interaction point.

1.2 Proposed work

This doctor work is one part of the development of CPS. The goal is to build a power management in the CPS. All the voltages required are generated on-chip. Therefore, the pad number is decreased as well as the cable number. The noise and power performances are also improved. Furthermore, the power distribution for CPS was analyzed and proposed. Two full-custom regulators, supplying clamping voltage and analog power supply voltage, were designed and verified. The strategies of the power management in CPS were also analyzed. The radiation tolerance technology was also researched.

The work proposed in this thesis focuses on the linear regulator design in the power management of CPS. These regulators are fully integrated on-chip. Any external elements are not allowed due to the limitation of the space on the ladder and the material budget. In the other hand, CPS will contain more pixels to improve the spatial resolution. The parasitic capacitance is very large, which is proportional to the size of pixel array. Thus, the stability of the regulators must be carefully designed. However, the topologies replying on the external compensation elements can not be applied in these two regulators. Since the signal induced by the charged particles is very weak, low noise is also required and the power supply rejection must be high. Moreover, the power consumption is limited by the cooling system and the detector requirements.

A novel compensation strategy was proposed to guarantee the stability. A series RC network was employed to introduce a zero. Moveover, the main poles and zeros were adaptable by the current feedback. It is easy to be realized. The compensation elements area were decreased, compared with the other schemes. Low extra current is required in this scheme.

A programmable resistance is employed in the feedback resistor network to compensate the process fluctuation and temperature variation. Its value can be adapted by the standard joint test action group (JTAG) interfaces.

1.3 Thesis overview

The power requirement of the CPS is firstly presented. As one part of the CPS design, this work dedicates to the power management. It is also helpful to the power distribution. This thesis is organized as follows:

In Chapter 2, CPS are introduced in detail, including their structure, the requirements of the HEP experiments and their power specifications. The power distribution topologies for CPS are proposed and discussed. This chapter also gives the power requirements of CPS, which must be fulfilled by the power management design. Moreover, the possible power management strategy for CPS is given in order to further decrease the power consumption.

In Chapter 3, the alternative power distributions are presented. As the conventional scheme, the independent powering has been demonstrated failed in the future detectors. Many works addressing this problem have been reported. The state art of the power distributions is presented. These approaches can be summarized as two fundamental approaches [18]: (1) Serial powering the sensors/readout circuits using a recycle current. (2) Parallel powering with local DC-DC conversion. The power is transmitted at high DC voltage and low current. Each topology is presented in detail. The advantages and disadvantages are summarized. According to the analysis, the power distribution for CPS is proposed.

Since the sensor chips work in high radiation environment, the radiation effects and radiation hardening techniques are presented in Chapter 4. The hardening by design (HBD) is focused on in order to achieve good radiation tolerance in standard CMOS process.

In Chapter 5, a linear regulator is proposed in the power management to provide the clamping voltage for correlated double sampling in CPS chip. The linear regulator is briefly introduced at the beginning. The regulator topologies are summarized then. The design specifications are presented according to the requirements of CPS. The load capacitor and load current are introduced in detail, since they influence the stability and noise performance. Circuit implementation is presented in detail. The simulation and experimental results are given to validate the design at last.

In Chapter 6, the other linear regulator named RegVdda is presented. It is utilized to supply power to the analog circuit. In order to guarantee the stability with the load current in a large range, a novel compensation strategy is proposed. The compensation capacitance is remarkably decreased. The simulation and measurement results are also

given.

Finally, this thesis work is summarized and the perspectives are given.

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Chapter 2

CMOS pixel sensors

CMOS pixel sensors are also called monolithic pixel sensors (MAPS), since they integrate the sensing element and the readout circuitry on the same substrate. They are fabricated by standard process and can be thinned down to 50 μm. Thus, low cost and low material budget are achieved. CPS are not only widely used in visual imagining but also are good choices to track the charged particles in HEP experiments. This chapter will introduce CPS in detail. At first, the structure of CPS is presented. Each block in CPS is introduced. Secondly, the power requirements of the high energy physics experiments are discussed. Finally, the power specifications of CPS are given.

2.1 CPS structure

CPS have developed fast in the past a few years. A series of prototypes called MIMOSA (Minimum Ionizing particle MOS Active pixel sensor) has been designed and measured in Institut Pluridisciplinaire Hubert Curien (IPHC), Strasbourg, France, since 1999 [1]. The measurements have demonstrated that CPS is a promising candidate for charged particle tracking and it can be also used in biology imaging [2]. Charge collection efficiency was the main driving force in the first years. Different technologies were tested in order to find a proper process for CPS fabrication. The radiation tolerance was also analyzed. In recent years, the driving force comes from the physics domain. CPS chips usually are full-customer to fulfill the requirements of different detectors. The design effort is developing the chip architecture and fast column-parallel readout. The recent structure is significantly different with the previous chips. For example, the output is analogue signal in MIMOSA 1-21 from 2001 to 2006. The output is digital and correlated double sampling (CDS) operation is complemented in latter CPS chips. As shown in figure 2.1, CPS are

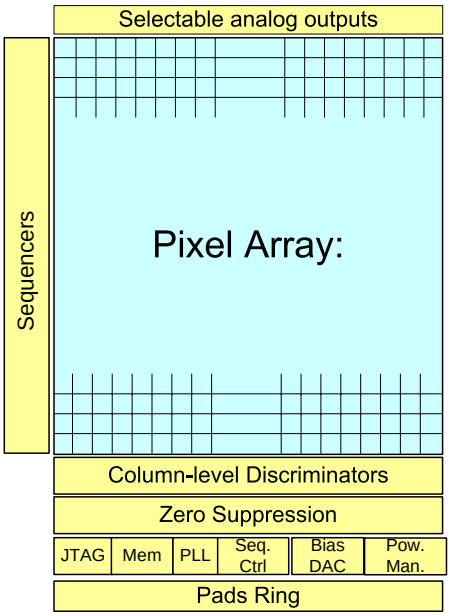

Figure 2.1: *Structure of current CPS chip.*

composed of pixel array, row sequencers, column-level discriminators, zero-suppression, bias DAC, power management/regulators and joint test action group (JTAG) in their recent versions. The function of each block is listed as follows:

- Pixel array: sensing and pre-amplifying the signal induced by the charged particles. Unlike the simple three-transistor pixel used in visual imagining, pixel used for HEP experiments is more complex. It consists more transistors, as shown in figure 2.2. One pixel is composed of sensing element, pre-amplifier, a correlated double sampling (CDS) circuitry, source follower and so on. The sensing element, which is implemented by Psub-Nwell diode, collects electrons. Thus, the voltage at the diode decreases when the particle hits this pixel or one nearby. The pitch of the diode is decided by the charge collection efficiency and the equivalent noise charge (ENC). Obviously, large diode can improve charge collection. However, the ENC is increased since large diode increases the input node capacitance. For a typical pixel size of 30 $\mu m \times$ 30 μm, the optimum diode size was found to be approximately 15 μm^2. Pixel with multiple charge collecting diodes (up to four diodes per pixel) is also tested. It is demonstrated failed due to introducing very large input node capacitance [3]. As a consequence, only one diode is usually used in recent pixel.

  The self-biased structure (SB) takes the place of simple reset due to simplifying the pixel architecture and eliminating the pedestal inherent to pixel operation [4].

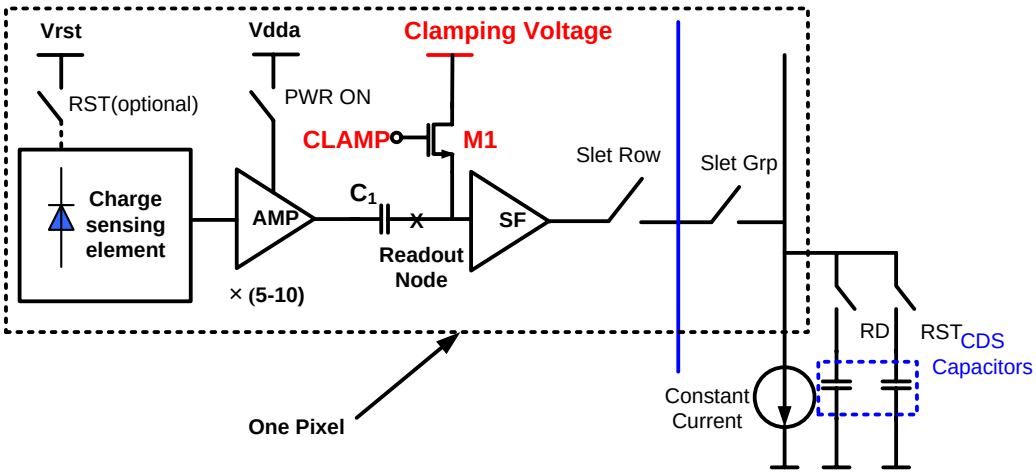

Figure 2.2: *Simplified pixel topology [1].*

Since the detected signal is weak and the output voltage of sensing element is of a few millivolts, the low noise pre-amplifier follows to improve the signal to noise ratio (SNR). The CDS circuitry is employed to decrease the noise and extract the required signal. The source follower is necessary to drive the output voltage to discriminator, since large parasitic capacitors and resistors are induced by the long signal wire. The load current of source follower in one column is shared in order to decrease power consumption. Since Nwell is used to collect the electrons, PMOS transistors are not allowed to be fabricated in pixel with a standard CMOS process. The pixel design is constrained, such as the pre-amplifier and combinational logic. Fortunately, the deep Nwell and the 3D integration (introduced latter) are promising to solve this problem in these years [5] [6].

- Row sequencers: generating the readout timing. Since the discriminator in one column is shared, the pixel array is usually read out row by row, which is called rolling shutter operation. Each row is processed at a fixed time interval. Thus, the frame readout time is limited by the number of the rows and the time to process a row.

- Column-level discriminators: converting the analog voltage to digital data. The output is '1' ('0') when the output voltage from the pixel is higher (lower) than the threshold voltage. The digital data of one pixel represents whether it is hit and can be easily processed with computers. Physicists require these digital data to locate the particle position with specific softwares. The reference voltages required by the column-level discriminator are generated by a low noise DAC, which can be

configured by JTAG interface. Consequently, the threshold of the discriminator is programmable in order to get a proper trade-off between useful signal and ground noise. In fact, the discriminator is single-bit ADC. More bits means higher resolution in high energy physics experiments. Some 4 or 5 bit ADCs in column level has been designed to improve the spatial resolution [7] [8]. A second correlated double sampling is implemented in each discriminator stage, which can remove pixel-pixel offsets induced by each in-pixel buffer [9]. This allows all discriminator to use a common threshold. The offset compensation are also implemented in discriminators.

- Zero suppression: suppressing data '0', which means the pixel is not hit by particle. It scans the sparse data of current row in pipeline mode. The non hit pixel is ignored and the signal above the threshold is identified. The zero-suppression can decrease the data amount to increase the readout speed. The idea is based on row by row sparse data readout. The zero suppression is organized in pipeline mode in three steps, including sparse data scan, state multiplexer and memory management [10]. The data compression factor ranging from 10 to 1000 can be achieved, which also depends on the hit density per frame. Thus, the data amount is decreased and the readout speed of one frame is improved.

- Power management/regulators: providing power supply voltages and some critical voltages required by CPS. The voltages used in readout chain should be low noise in order to read out the very weak signal in pixel. Thus, they are proposed to be generated on chip in power management. Full customer regulators are designed for different voltages. They can provide low-noise voltage and can isolate the core circuit from the noisy environment. All the regulators are fully integrated on-chip in order to decrease cables/traces on the ladder as well the noise. Any external component is not required. The power management is also dedicated to solving the power distribution challenges.

- Joint test action group (JTAG): accessing the internal registers and assisting test. The interface is standard. The on-chip programmable biases, reference voltages and the selection of the test mode can be set via a JTAG controller. Each block can be separately tested in order to increase the testability and measure the performance parameters of each block. Moreover, the functionality of each part can be validated with large number of configurations.

- Bias digital to analog converter (DAC): supplying the bias voltage or reference voltage for the discriminators and other blocks. The input digital data are store in

registers. Thus, the bias voltage and reference voltage can be adapted by changing the value of resisters. The registers can be accessed by JTAG interfaces. Consequently, the test is flexible and the power consumption can be optimized.

- Memories: temporarily storing the digital results and functioning as buffers. In CPS, the pixels are parallel read out in column, while the output of the whole chip is transmitted in serial. Thus, two memories are utilized to decrease the readout speed and allow continuous readout. They are operated in a Ping-Pong mode. One works in writing mode and the other works in reading mode. Their working mode alternates between writing and reading.

- Phase locked loop (PLL): generating clock on-chip. A frequency multiplier is included [11]. Thus, a high frequency clock can be generated based on a low frequency reference input clock.

- Selectable analog outputs: for test. The analog voltage from each pixel before the discriminator can be measured by these eight pads in test mode. These analog voltages are utilized to evaluate the noise of the pixels.

As mentioned above, the CPS are mixed signal chips, which contain analog circuitry and digital circuitry. In order to protect analog circuitry against the interruption from analog circuitry and digital circuitry, it is essential to power them with two different power supply voltages.

2.1.1 Correlated double sampling

Correlated double sampling (CDS) is an efficient method to suppress noise, which is widely used in CCDs and CMOS image sensors in recent years [12]. Since signal detected is very weak (ranging from several hundreds to a thousand electrons), the CDS is used to read out and extract the signal in CPS. The idea is sampling the output voltage of pixel twice (before and after the reset). Then the two sampling are subtracted. It should be noticed that the CDS operation was performed by software during off-line data processing in earlier CPS chips, such as MIMOSA8. As depicted in Fig.2.3, two consecutive frame samplings are subtracted one from the other with computer. The hit candidate is gotten after the noise correction. In order to implement on-chip data processing and further decrease noise, CDS circuitry has been integrated on recent CPS chips. The signal is extracted by subtracting two consecutive samples acquired from each pixel before and after the reset [14] [15].

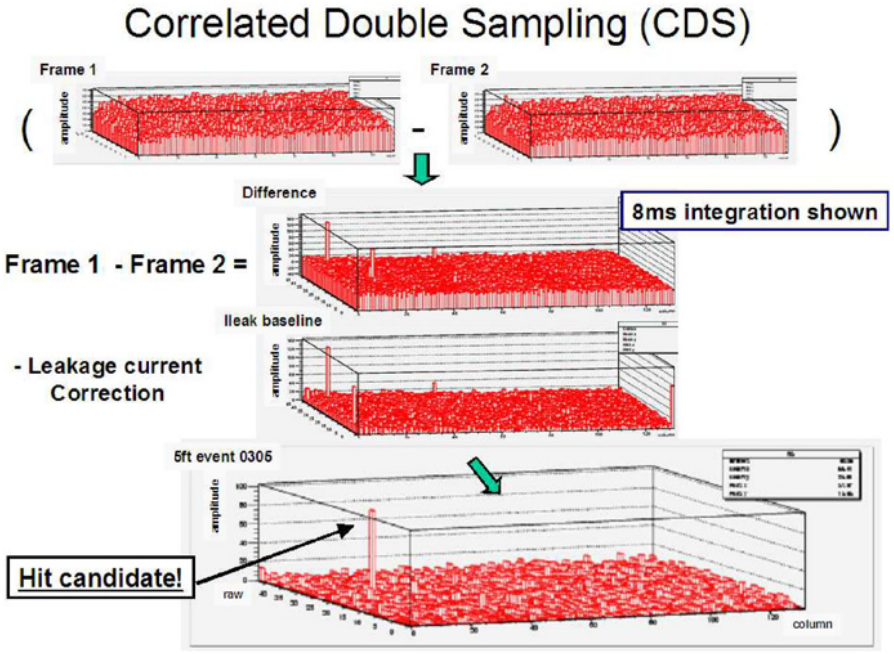

Figure 2.3: *Signal extraction with CDS operation for early CPS chips [13].*

Therefore, reset noise, fixed pattern noise (FPN) and majority of the flicker noise in the pixel can be removed [16]. CDS operation is realized in column-level and in pixel-level. The block diagram and its corresponding timing is depicted in figure 2.4. The column-discriminator is represented by two CDS capacitors. In order to decrease noise, discriminator is implemented by a multi-stage, full-differential, switched-capacitor comparator. It functions as a high-pass filter so low frequency noise can be removed.

In order to remove the pedestals of the pixels, CDS operation is implemented in pixel level. As illustrated in figure 2.4, MOSCAP is a AC-coupling capacitor to remove the individual pedestal of each pixel. The pixel is read twice (before and after the signal Clamping) and the two samples subtract with each other. The output potentials are amplified by a source follower and are stored in the RD memory cell and CALIB memory cell, respectively. These two voltages enter the discriminator to subtract each other and compare with the subtraction of two reference voltages, which is the threshold voltage of the discriminator. Since the subtraction of two samples results in doubling of the power density of the uncorrelated high-frequency noise [17], the thermal noise is increased. The CDS operation can not completely eliminate all the noise. For example, the noise introduced by clamping voltage can enter the readout circuit at high frequency. Consequently, the clamping voltage must be sufficient low.

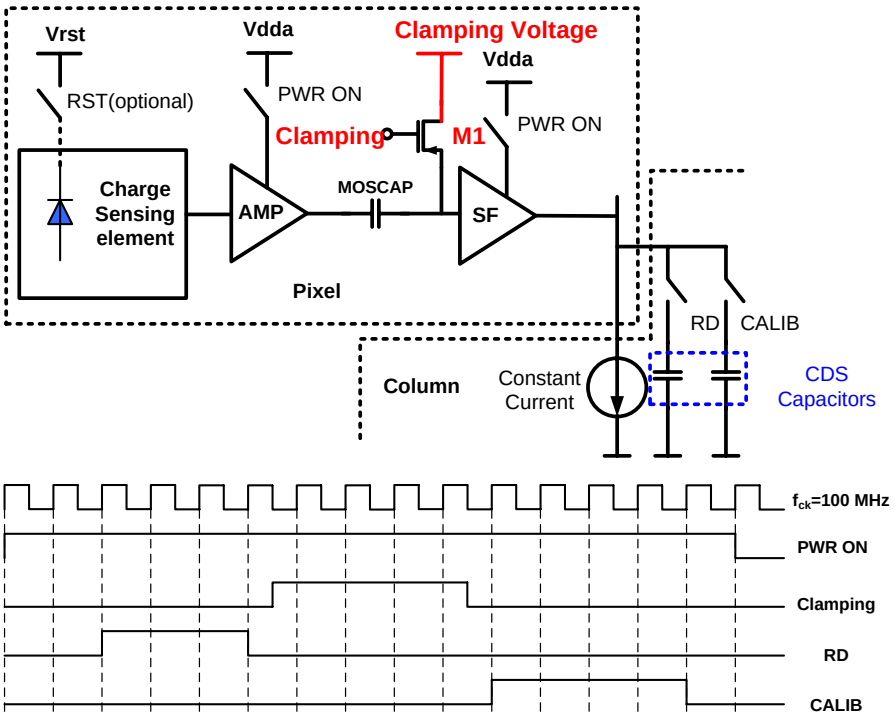

Figure 2.4: *Block diagram and timing of CDS operation [14].*

2.2 Sensor requirements in HEP experiments

2.2.1 Material budget

Sensors are expected to not change the original path of the particles and record the location where the particles pass through. That means they should be transparent for the particles. However, the particles unavoidably interact with surrounding material. Random scattering happens, which lead to a problem of finding the wrong hits. Moreover, the performance parameters of sensors are degraded, such as momentum resolution, energy loss, secondary particles and so on. Thus, the material inside the detector should be sufficient low to prevent the random scattering. The volume of cooling system, sensors and their external components (e.g., resistors and capacitors) are constrained. Thin sensors and devices are required. Especially, the cooling system should be lightened, which means that the power consumption of sensors must be low. Furthermore, the future detectors are proposed to be equipped with more sensors. Thus, the material budget must be low in order to decrease the cost.

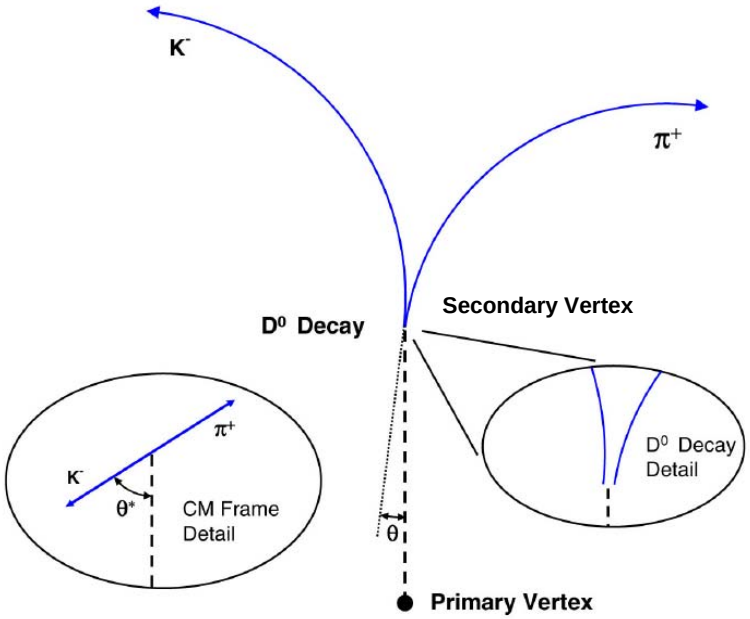

Figure 2.5: *Diagram of D^0 decaying.*

2.2.2 Spatial resolution

Hadrons originate at the interaction point (primary vertex) and decay soon. These heavy particles have short lifetimes and quickly decay into less massive daughter particles. Displaced secondary vertex is created at the same time. As shown in figure 2.5, D^0 decays into a kaon (k^-) and a pion (π^+) after travailing a distance of about 100 μm. Reconstruction of short-lived D mesons requires measurements of displaced vertices with a precision of approximate 50 μm. It is very crucial to identify different particles and vertexes. In order to directly reconstruct mesons and baryons and measure the displaced vertex, pointing resolution must be excellent, especially for the inner most detector. As the inner most detector for STAR experiments, PXL is required to achieve the spatial resolution of smaller than 30 μm.

2.2.3 Readout speed

Particle physicists need enormous number of particle collisions to make analysis more precise and believable. Thousands of collisions may happen in one second. Readout speed becomes an important performance to avoid missing any information. For example, the integration time is about 20 - 100 μs in ILC. About 10^4 frames/s is required.

2.2.4 Radiation tolerance

Sensors used in vertex detector is close to the interaction point. It is a relatively high radiation environment when detector normally works. Radiation and non-radiation effects happen. For example, threshold voltage of MOS transistors shifts and the voltage can be changed by a single charged particle with high energy. The silicon integrated circuits can be damaged. Thus, radiation tolerance design is required.

2.3 New developments on CPS

The development on CPS is driven by the requirements of HEP experiments. In order to complete the new tasks, some performance parameters of CPS should be improved, which brings new challenges. The pixel detectors in future HEP experiments require high spatial resolution, high time resolution, high readout speed, high radiation tolerance and low material budget. However, these performances can not be simultaneously improved in the current architecture, due to the conflicting among them.

2.3.1 Fast readout speed

The readout speed is an important performance parameter of vertex detectors, since thousands of events happen during the collision. Very fast readout speed is required to avoid missing any event. For example, the readout time is proposed to be about 25 μs or smaller in the innermost layer of ILC vertex detector [18]. Since the pixel array is read out in rolling shutter mode in CPS, the number of rows is inversely proportional to the readout speed. The speed may be unacceptable in a larger sensor containing almost one million pixels. Reducing the number of pixels per column is an effective method to improve readout speed. The sensors are foreseen to be read out from two sides, instead of one only, as shown in Fig.2.6. This architecture is also called two sided readout. 3D technology is also helpful to improve the speed.

2.3.2 3D vertical integration technologies

3D vertical integration technologies has become real and popular among IC designer as the new wafer thinning and bonding techniques emerge [19]. Several thinned wafers are stacked and are connected by through-silicon vias (TSV) to forme one monolithic circuit. Thus, some important limitations correlated with CMOS feature size scaling can

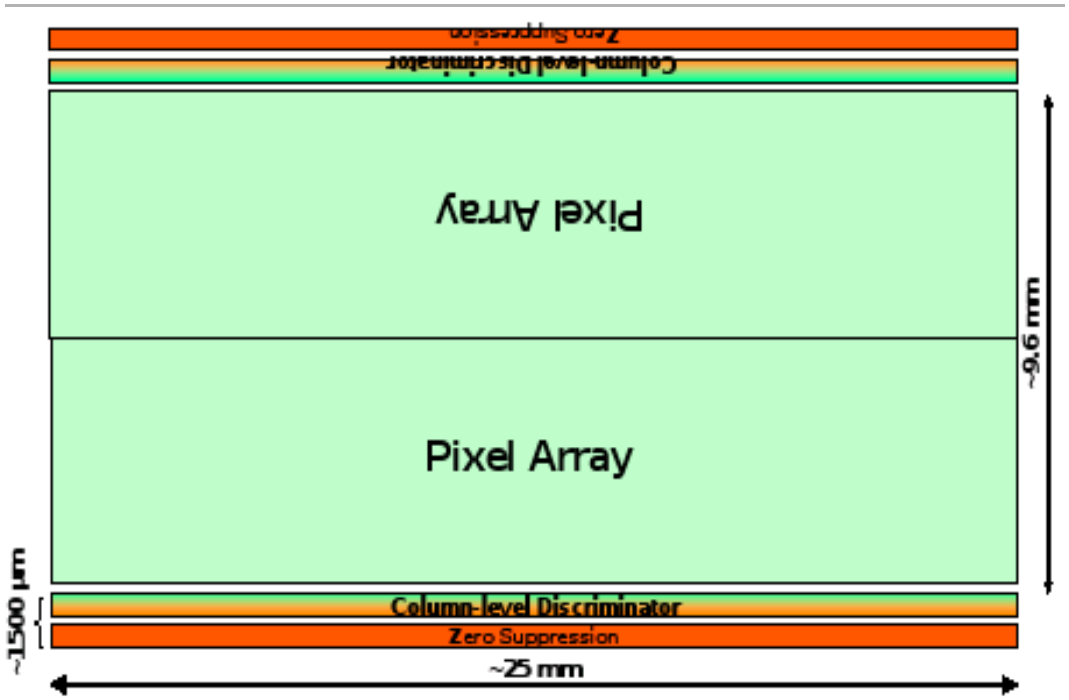

Figure 2.6: *Diagram of two sided readout.*

be alleviated. Five main elementary technologies are included in the 3D vertical integration, such as TSV formation, bump formation, wafer thinning, chip/wafer alignment, chip/wafer stacking and reconstructing the entire process and structure [20]. 3D devices are expected to have high energy efficiency, small form factor, heterogeneous integration the capability to realizing new architecture, multiple functions and low cost. It has become mature in the industry chip such as memory. The potential applications of 3D are wide, as shown in figure 2.7.

Since PMOS transistors are forbidden to presenting inside sensing area, the readout circuitry is limited and digital cells are not allowed in pixels. Moreover, the optimal for minimum ionizing particles (MIP) tracking epitaxial wafers are usually offered by industry with old fashioned CMOS process [6]. The interconnect delay becomes dominate with respect to transistor delay in 0.18 μm, 0.13 μm and smaller feature size process. In order to address this problems, CPS chips are considered to be fabricated by 3D vertical integration technologies. Some prototypes of 3D CPS have been designed and fabricated. The CPS chip is divided into several dedicated functional circuits, which are also called tiers. As shown in figure 2.8, charge sensing, analog readout and digital processing are placed on their own tiers. Each tier may be fabricated on wafer with its optimal process. Then, the wafers are thinned down to about 10 microns and are connected by TSV. Since

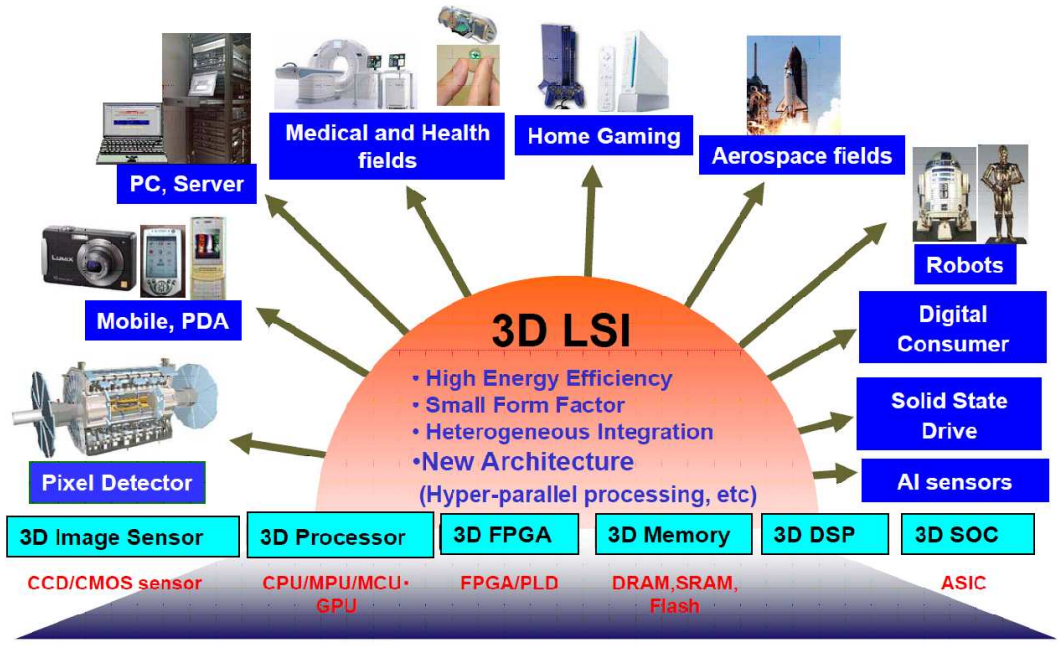

Figure 2.7: *Potential applications of 3D technology [20].*

the charge sensing and analog readout are fabricated on different wafers, each pixel can be read out by its own complex circuit. It is possible to contain PMOS transistors and digital cell in readout circuit. Some complex functions can be realized. The performances of CPS can be improved such as noise and material budget. 3D integration, where modules can be stacked on top of each others instead of being spread out on the same die, minimizes the interconnect lengths as well the delay [21]. High readout speed is achieved. However, more design and fabricated work on 3D CPS should be done. Since every tier may be fabricated by different foundries, the cooperation among the foundries and packaging companies is necessary. The electrical design automation (EDA) tools of 3D design are also expected to be researched and developed.

2.4 Power management

The CPS chips are usually close mounted on a ladder, which forms a barrel in order to track the particles from every direction. PIXEL/PXL is the innermost layers (at 2.5 and 8 cm) of heavy flavor tracker (HFT) for STAR experiments, as depicted in figure 2.9. Ten CPS chips are proposed to be mounted in a ladder. These chips share the same power supply voltages and other external voltages which comes from one end of the ladder. The size of one CPS chip is about 2 $cm\times$ 2 cm. Thus, the distance between

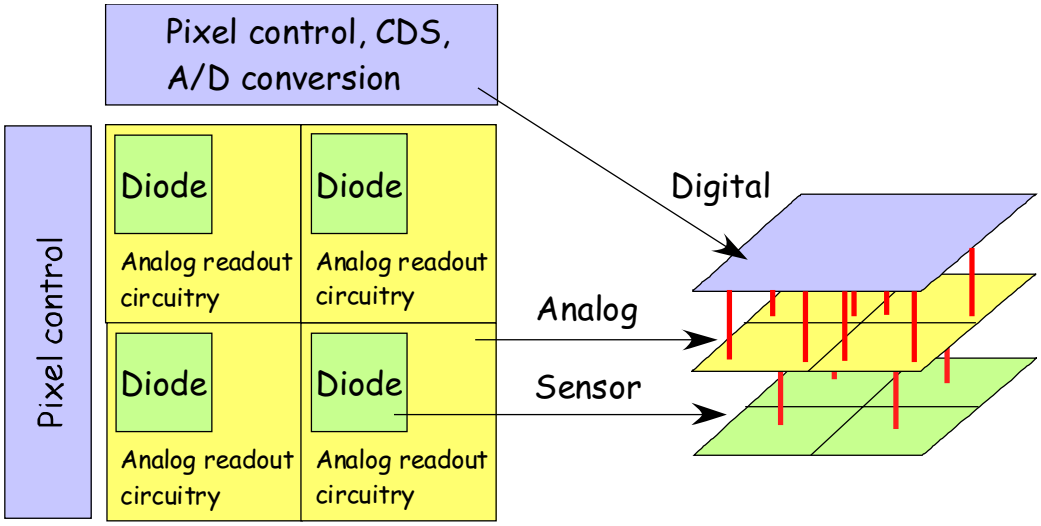

Figure 2.8: *Transforming 2D into 3D.*

the discrete electronics and the CPS in the other end is at least 18 cm. The trace/wire in the ladder is too long. It is very difficult to achieve a precise and low-noise reference voltage in this case. Moreover, the sensors influence each other by the same trace/wire. Since the detected signal is weak, the noise of the analog power supply voltage and the reference voltages are required to be sufficiently low. To address these problems, a power management is built in CPS. Some critical reference voltages and analog power supply voltage are proposed to be generated on-chip. The number of the pads and cables can be also decreased, which is helpful to solve the problems of power distribution.

The proposed block diagram of power management in CPS is shown in figure 2.10. The power supply voltage coming from the cable enters power management in CPS to decrease noise and generated different voltages required by other blocks. The digital power supply voltage (vdd) and analog power supply voltage (vdda) are generated by two regulators. In order to achieve low-noise clamping voltage, a regulator is employed, whose input is vdda. Thus, the clamping voltage can be seen as the output of a two-stage regulator. High power supply rejection (PSR) can be achieved for clamping voltage. The bias voltages and reference voltages required by the column-level ADCs (also called discriminators) are provided by a low noise DAC, which can be configured by JTAG interface. Consequently, the bias voltage is programmable, as well the reference voltages.

As mentioned in Section 2.1, the analog circuit is composed of a pixel array, column-level discriminators and bias DAC in CPS. In order to meet the air-cooling requirement in ILC, power pulsing is proposed to be used, as depicted in figure 2.11 [19] [22]. During

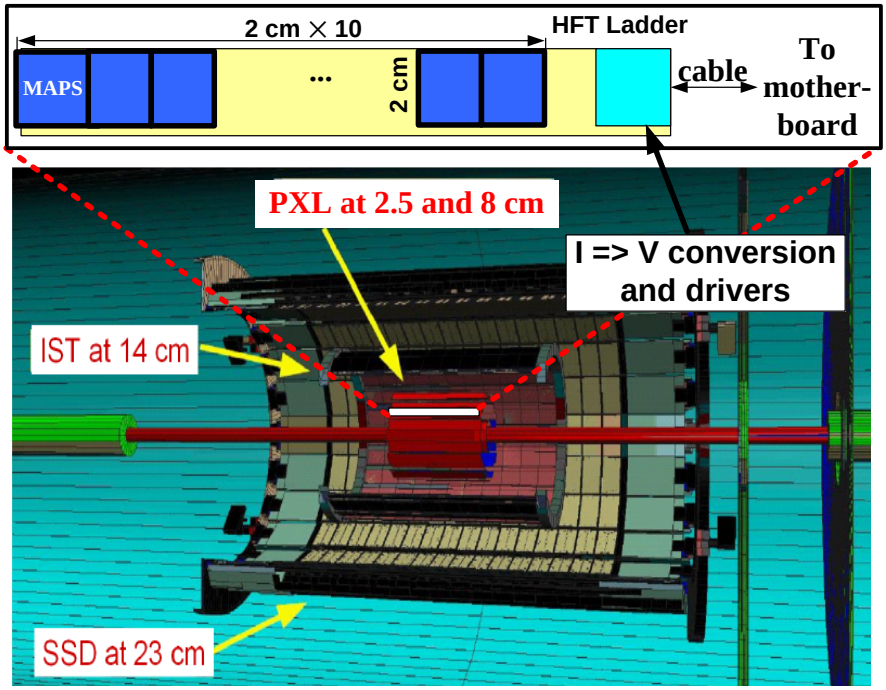

Figure 2.9: *Diagram of the HFT and one ladder.*

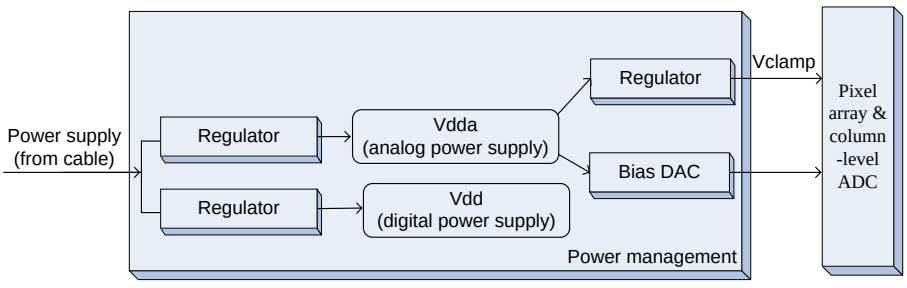

Figure 2.10: *Block diagram of power management in CPS.*

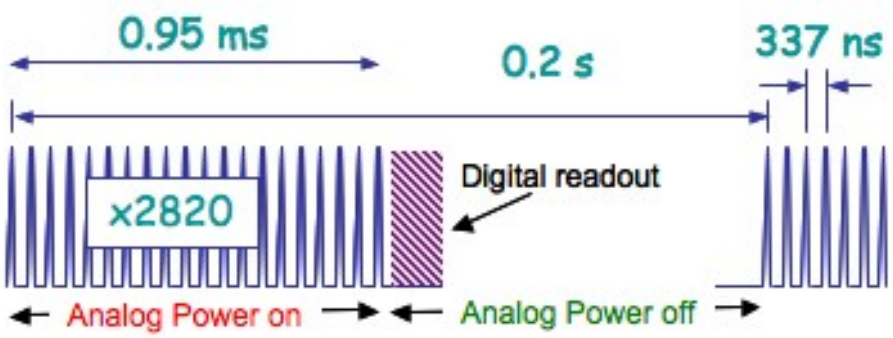

Figure 2.11: *Power cycling options of ILC bunch timing [22].*

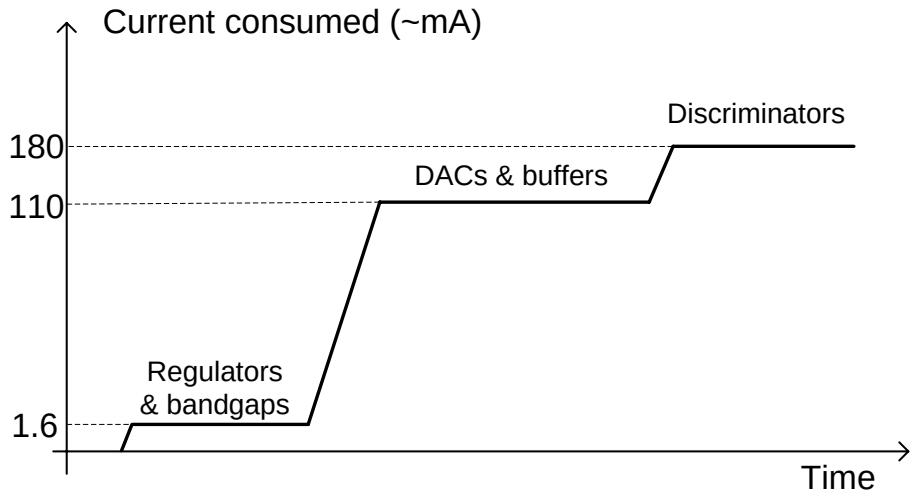

Figure 2.12: *Current consumed by CPS during the startup.*

the collision (1 ms), CPS chips are operated in full speed. A current of about 200 mA will be consumed by the analog core circuit. On the other hand, all or some blocks will be standby/shutdown in the off interval (199 ms). Very low current near zero will be consumed. Moreover, the situation of low load current also happens in CPS during their start-up. As shown in figure 2.12, three states are included in the start-up. In the "power-on reset" state, the regulators and bandgaps start to work. Then the buffers and the DACs start to supply reference voltages and bias voltages for the other blocks. Finally, the pixels are readout in rolling-shutter readout mode and the column-level discriminators digitize the output coming from the pixels. Therefore, the load current dramatically varies during the start-up. Its range is approximately from 0 mA to 200 mA. The regulator of analog power supply may work in zero-load, light-load or heavy-load cases. Thus, the regulator to be designed must be stable in the full range of the load current.

2.4.1 Research on power management techniques

With advanced semiconductor technology nodes, power management is a global system issue that affects software development, including the operating system down to the silicon technology itself. Technology scaling allows more transistors to be fabricated per unit area. Additional functionalities are available without a significant increase in price. However, the scaling of power supply voltage is poor and leakage power fast increases. Power becomes a global crisis. Moreover, portable devices powered by battery have become more common. The power requirements and constraints are even more severe. Consequently, efficient low power design solutions are forced to be implemented.

The static power in CMOS circuit is dissipated by leakage currents. The dynamic power is dissipated when the circuit works, which includes the switching power for charging and discharging the load capacitances. Though the dynamic power is dominant in processes with 0.25 μm and larger feature sizes, the static power becomes larger component in processes with smaller feature sizes. Though the CPS chip is recently fabricated in process with 0.35 μm, the process with smaller feature size is the developing trend. Thus, both dynamic power and static power should be researched for CPS. Since voltage is the strongest handle for managing power consumption, it is utilized as a variable at system-level. Circuitry can be operated at different voltages and frequencies while executing different functions. The main power management techniques based on handling voltage are listed as follows [23] [24].

- Dynamic power reduction

  The dynamic power is consumed only when the circuits work. Thus, disabling the inactive circuits can significantly reduce the dynamic power consumption. The main blocks are controlled by the enable signals, which can switch the blocks off/on to decrease the dynamic power consumption to zero. Only the necessary blocks work during the standby state. The dynamic power is reduced without influencing functions.

- Dynamic voltage scaling with frequency scaling (DVFS)

  DVFS is utilized to reduce power when the system requires several performance levels. High processing performance is achieved via the highest voltage at maximum frequency. Low processing performance is achieved via the lowest voltage at minimum frequency. However, switching between the two modes is a challenge. The current significantly varies during the transition. Since the blocks work in different voltages, DVFS technique also requires voltage island, in which each block are

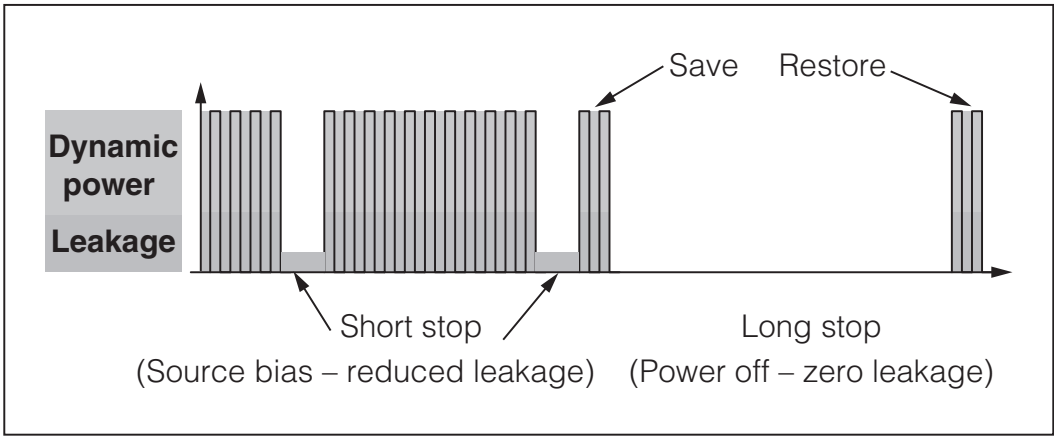

Figure 2.13: *Pulse width modulation activity/inactivity sequence over time [23].*

placed. The level shift circuits are used between two voltage islands. Moreover, double wells must be allowed in the fabrication process. Additional hardware and design verifications are also essential.

- Pulse width modulation (PWM)

  Pulse width modulation (PWM) is another efficient technique of reducing the dynamic power consumption. It can achieve a power reduction equivalent to that of DVFS with two or more frequencies. Different with DVFS, only one single clock frequency is used in PWM. The width of the clock is modulated according to the working periods. The sequences of clock cycles are alternated between the activity periods and inactivity periods, as shown in figure 2.13. During short inactivity periods, no dynamic power is consumed. The static power is also decreased in PWM (e.g., during the long stop). The current context is saved in an always-on low-leakage memory before a long inactivity period begins. Then this block is completely powered off. The static power is therefore zero. After the long inactivity period, the block is powered on and the clock is started. The operations can continue by restoring the context from the memory. The power pulsing applied in international linear collider is based on this technique.

- Power gating (PG)

  The leakage current of unused blocks leads to waste power in certain operation modes, especially for the large scale of digital circuits. In order to decrease leakage current, power switches are inserted between the power supply and blocks. The power switches can be realized by a fixed-size power switch on one side of a block

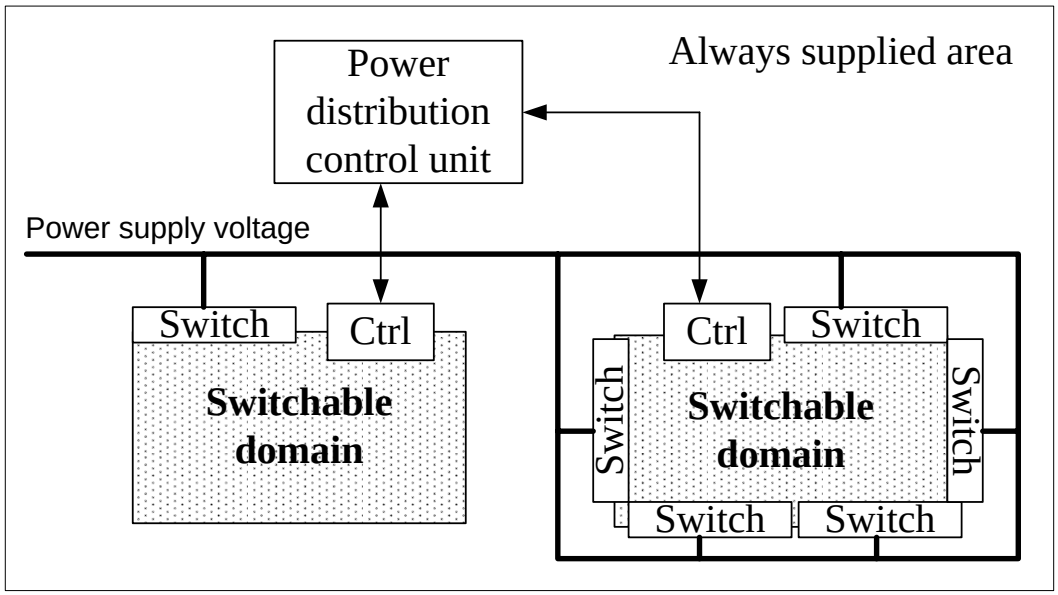

Figure 2.14: *Power gating using one switch or several switches.*

or a variable-size switch all around the block, as shown in figure 2.14. The power supply of the unused blocks can be cut off by their dedicated power switches in certain modes of chip operation. Thus, the outputs of the blocks float and the leakage current is almost entirely eliminated. Moreover, the power switches are turned on when the blocks are active. PG can fall into the two categories of Coarse-Grain power gating (CPG) where PG is carried out on large functional areas of the chip and Fine-Grain power gating (FPG) where PG is implemented on smaller blocks of logic.

The power switches can be implemented by PMOS or NMOS devices, which are connected to power supply or ground, respectively. The transmission gate is also a good choice if the chip area allows. The power supply drops over the switch when it is on, especially for a large current. Moreover, leakage current may increase power. In order to perform like a ideal switch, the on-resistance and cutoff-current of the realized switches must be as small as possible. Two types of transistors are good candidates to meet those requirements by using either: a thick-oxide transistor with a small length and a positive gate bias in the on mode or a low V_{TH} thin-oxide transistor with negative gate bias in off made. Obviously, the choice may be constrained by fabricated process.

Peak current occurs during the start-up, when the circuits are switched on from off. They may degrade the circuit performances. However, high peak current results in

short wake-up time, after which the blocks normally work from inactive state. The peak current influences the speed of the system. Thus, trade-off between peak current and wake-up time must be carefully considered. Moreover, the control signals are required to activate or inactivate the blocks.

- Multi-voltage

  A chip is usually composed of several blocks. Different blocks can operate at different fixed voltages with satisfying the system performance requirements. Higher operation voltages can be used for the blocks requiring high speed while other blocks operate at lower voltage. The power consumption can be decreased by the decreased voltages. Level-shifter circuits are needed by the signals that cross voltage boundaries. This technology is similar to the dynamic voltage scaling with frequency scaling. However, it is simple. No complicated controlling is required. It is suitable for the circuit systems with few working states.

- Multi-threshold CMOS (MTCMOS)

  Threshold voltage effects the leakage current and other performances. Especially, sub-threshold leakage increases exponentially with decreasing threshold voltage. However, lower threshold voltage means higher performance since the performance is dependent upon the difference between power supply voltage and threshold voltage. Transistors with different threshold voltages are usually supported by foundries. Transistors with different threshold voltages can optimize the leakage current without decreasing performance. Low threshold voltage transistors can be used in the critical paths, which require high performance. High threshold voltage transistors are used where leakage current should be decreased. However, using multiple threshold voltages is expensive due to the additional masks.

- Active body bias (ABB)

  Active body bias (ABB) voltage is applied to the wells of NMOS and PMOS transistors, which can be seen as the body voltage. Since threshold voltages can be adapted by the source-body voltage, the ABB voltage is used to precisely adapt the threshold voltage. Thus, leakage current can be controlled and the performance can be improved at the same time. Moreover, ABB can compensate the process variations due to age and temperature. It should be noticed that ABB has an intrinsic drawback. Multi-well process is necessary to fabricate NMOS and PMOS in P-Well and N-Well, respectively.

Since 0.35 μm CMOS process is considered as the optimum fabricated process for recent CPS chips, the power management technique applied to recent CPS is limited by the process. Moreover, performance is more important than the power consumption in HEP experiments, which is different with the consumer electronics. Sensor chips are required to read out the position of the particles as fast as possible during the collision. The power management techniques based on voltage island are not suitable for CPS chips. Fortunately, leakage current takes low ratio of total power consumption in 0.35 μm CMOS process. Decreasing dynamic power is an efficient method to achieve low power. As mentioned before, complex power management techniques are not allowed in CPS. It is proposed to disable the inactive blocks in certain modes of CPS. It should be noticed that the operation mode of CPS is determined by the dedicated HEP experiments. For example, pulsing power will be applied in ILC. The CPS maybe shut down most of the analog circuits, such as discriminators and pre-amplifiers, during analog power off (figure 2.11). Consequently, the regulator generating analog power supply is required to be able to cut off its output with a dedicated signal in the power management of CPS.

2.4.2 Radiation tolerance

The radiation damage to semiconductor devices has been researched in the past a few years. High energy particle can cause transient and permanent effects. The effects may decrease the performances of circuits. Chapter 4 will present them in detail. Many particles are generated from the interaction point forming strong radiation environment. The radiation dose and fluence of some HEP experiments are listed in Table 2.1. Therefore, the radiation tolerance of power management in CPS must be considered and researched.

2.4.3 Low power consumption

As it is known, power consumption is expected to be as low as possible for physicists and circuit designers. Since more sensors will equip in the future detectors, the power consumption of sensor chip should be low to make it possible. In the other hand, most of the power consumed by circuits transmitted to heat. The operating temperature of sensors are improved. Thus, cooling system is required to keep the temperature in the suitable range. Obviously, high power consumption makes the design of cooling system difficult. The heat conductor is required to be liquid so the material budget will be increased. As a consequence, the power consumed by the power management is required low. For example, the power consumption should be lower than $\sim 100\ mW/cm^2$ in the

Table 2.1: *Radiation dose and fluence of HEP experiments.*

HEP experiments	ionizing	non-ionizing
STAR	∼150 kRad/year	few $10^{12} N_{eq}/cm^2/year$
CBM [25]	34 MRad	$2 \times 10^{14} N_{eq}/cm^2/year$
ILC [26]	∼50 kRad	$6 \times 10^{10} N_{eq}/cm^2/year$

vertex detector for STAR experiments.

2.4.4 Low noise and low silicon area

The power management generates the critical reference voltages. They are used in pixels and discriminators. The signal detected by CPS is very weak, which is about a few tens of millivolts. In order to correctly read out the signal, the noise introduced by the readout circuity must be sufficient low. In order to prevent the signal being corrupted, low noise is required for the power management.

Since only pixel can sense the charged particles, the silicon area occupied by other blocks is expected to be as low as possible in order to detect all the charged particles. The low cost can also be achieved. Obviously, the power management must avoid using too large capacitance or resistance fabricated on chip.

2.5 Conclusions

CPS have been presented in detail in this chapter, including their structures and the new developments. The main performance parameters of CPS chips are given in terms of the requirements of HEP experiments. As one of the important blocks in CPS, power management is introduced, on which this thesis is focused. Power management techniques are summarized. Finally, the requirements of power managements are drawn.

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Chapter 3

Alternative power distribution approaches

As mentioned in Chapter 1, the independent powering has been proved failed in the future detector due to its low power efficiency, large space required for placing cables and bad material budget. In order to address the power distribution challenges, several alternative power distribution schemes have been reported in the past few years, which fall into the two categories of serial powering and DC-DC conversion. This chapter will describe them in detail and finally propose a power distribution scheme for CPS.

3.1 The solution of power distributions

Since the power lost in cables is directly proportional to the square of the transmitting current, the power distribution challenges are mainly caused by the increase of the current. The readout/sensor chips operate at high readout speed and their number will more than 2-fold increase in the future detector. Moreover, the leakage current will also increase in 0.13-μm or smaller feature-channel fabricated processes, which further degrades the power efficiency. Thus, novel power distributions are essential to be designed.

In order to improve the power efficiency, decreasing the current flowing through the cables is an efficient approach. Most of the alternative approaches reported are based on this idea. The resistive power loss in the cables can be significantly decreased in these approaches to increase the power efficiency of detectors. They fall into the two categories of serial powering and power transmission at high DC voltage and low currents combined with local DC-DC conversion [1]. The two different power strategies are presented in the next sections.

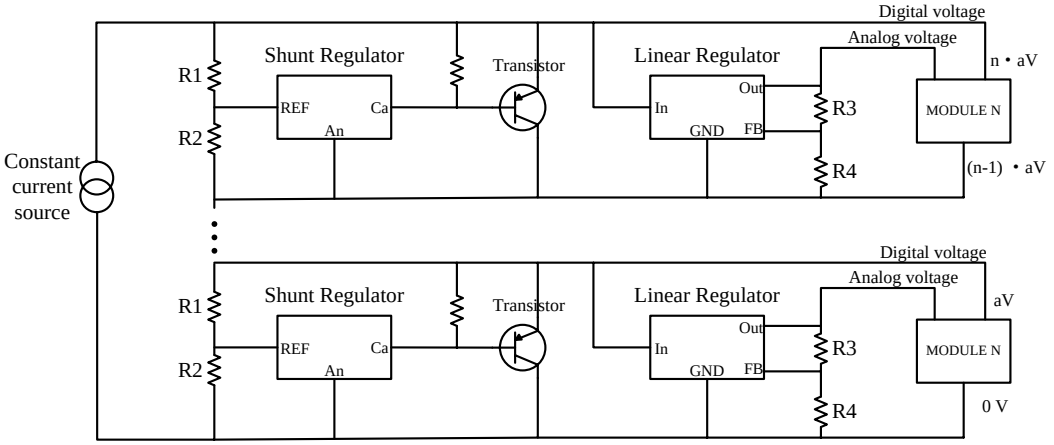

Figure 3.1: *Scheme of a serial powering without shown AC-coupling of signal. (The module voltage is assumed about aV.)*

3.2 Serial powering

Though the serial powering was proposed many years ago, it has not yet been widely used due to its unorthodox structure. It is recently considered as a good candidate of power supply distribution in detectors for high energy physics experiments. The serial powering is composed of an external constant current source, shunt regulators, shunt transistors, linear regulators and AC-coupling or optical decoupling of signal, as shown in figure 3.1 [2]. The shunt regulator and shunt transistor generate the power supply voltage required by the modules from the constant current source. The linear regulator is employed to power the analog circuits in the modules. Since the ground level of the modules is different, the AC-coupling or optical decoupling is necessary to transmit the digital control and output signals. All the detector modules are connected in series and powered by the same constant current source. The current is recycled, which is required by one module. Compared with independent powering, the transmitting current is decreased by 1/n, where n is the number of modules.

3.2.1 Structures and implementation of the serial powering

The structures of the serial powering have three options, depicted in figure 3.2 [1]. As the simplest approach, Single shunt regulator and its corresponding shunt transistor supply power to several readout chips (ROIC). However, it is not reliable. A very high current shunt may flow through the shunt transistor if one or more readout chips do not work. This current may destroy the shunt transistor leading to fatal error in the

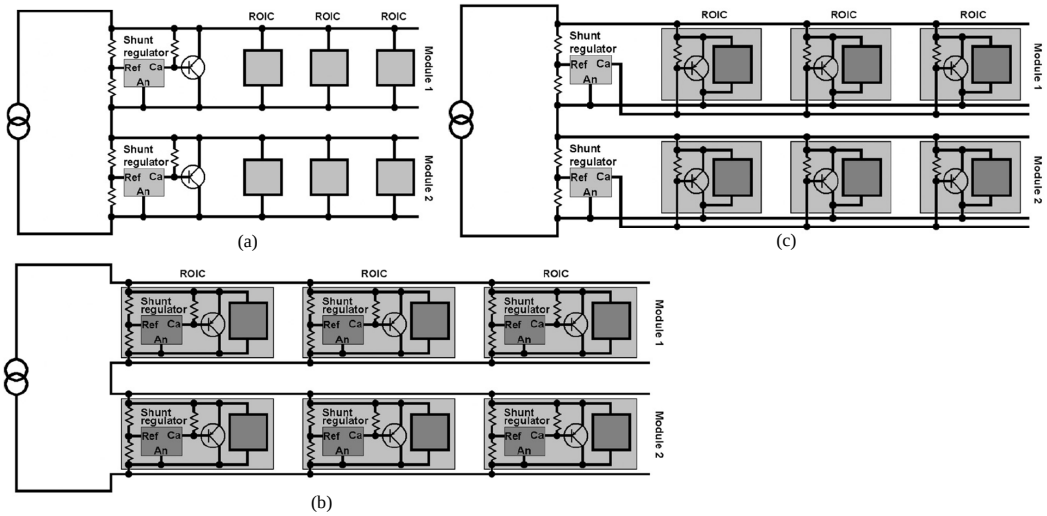

Figure 3.2: *Sketch of alternative serial powering implementations in a two-module configuration with three ROICs. A single shunt regulator and shunt transistor external to the ROICs (a). Parallel shunt regulators and shunt transistors, one each in each ROIC (b). A single external shunt regulator combined with parallel shunt transistors, one in each ROIC (c). [1]*

power system. Thus, a dedicated power chip is required with the capability to sink a significant current through the shunt regulator in case of the failure conditions. The dedicated power chip can be replaced by placing a shunt regulator and a shunt transistor beside each readout chip. The shunt transistors can share the high current. Nevertheless, other challenges appear. The shunt transistors are required to well match with each other, as well the shunt regulators. Especially, the switch-on behavior of the shunt transistors may be different due to the process fluctuation. Most of the total current is possibly carried by the shunt transistor with lowest threshold voltage. This shunt transistor can be damaged by the abnormally high current. The third option, known as the distributed shunt, is to use single external regulator and distributed shunt transistors. It can resolve the mismatching issue. This scheme is developed by M. Newcomer [3] [4]. All the shunt transistors are integrated in the readout chip. They are certainly connected to the external shunt regulator by bond wires and hybrid power traces/planes, which introduces the inductance and resistance and impacts the performance at high frequencies. As mentioned above, all the options have specific benefits and defects. The optimal choice strongly depends on the specific requirements of the detectors and experiments.

The serial powering has already been implemented and demonstrated. One promising implementation of the serial powering is to have a power management device on the modules. This power management device is called serial powering interface (SPI) [4]. It

provides the voltages required by modules and monitors the working condition of modules at the same time. The communication and module diagnostics are also contained. The communication can be realized by AC coupling or optical decoupling, such as the AC coupled low voltage differential signaling (LVDS) drivers and receivers. It should be noted that the serial powering has an innate drawback. The whole power system can not work if any module serially powered fails. In order to address this problem, the protection circuits are designed in SPI chip. The modules are monitored. The failed module can be shut down and its current is bypassed by a power field-effect transistor (FET). Therefore, the remaining detector systems can still maintain operation in case of a failure condition.

3.2.2 Performances achieved

The cable number is significantly decreased and the power efficiency is improved in serial powering. Each module employs a cable in independent powering, while only one long power cable is required in serial powering. The cable number is decreased by 1/n, where n is the number of modules. The thermal losses on one cable are calculated by $P = I^2R$, where I is the total current consumed by one module and R is the resistance of one cable. Since the cable number is decreased, the thermal losses are significantly decreased. The power efficiency is improved.

The serial powering can also achieve low noise. Since the voltages required by modules are derived locally from external constant current source, the interference between modules is suppressed. Figure 3.3 shows the equivalent noise charge (ENC) of barrel modules in ATLAS Semi-Conductor Tracker(SCT), when they are powered independently and in series [1]. Almost the same or even better noise performance can be achieved in serial powering, compared with independent powering.

The reliability is a big challenge for serial powering, since all the modules are connected like a chain. The serial powering becomes more risky when the number of modules powered is larger [2]. The risk analysis must be considered. Moreover, the monitoring circuits and protection circuits are essential to detect failure and protect the remaining modules, respectively. Many works in serial powering focus on this issue.

The other drawback of serial powering is that it is not compatible with the existing sensors or detectors. Thus, the design of the sensors should be upgraded to fulfill the requirements of serial powering. The AC-coupling or photo decoupling circuits should be designed for sensors in order to transmit the controlling signal and the digital output due to their different ground potential.

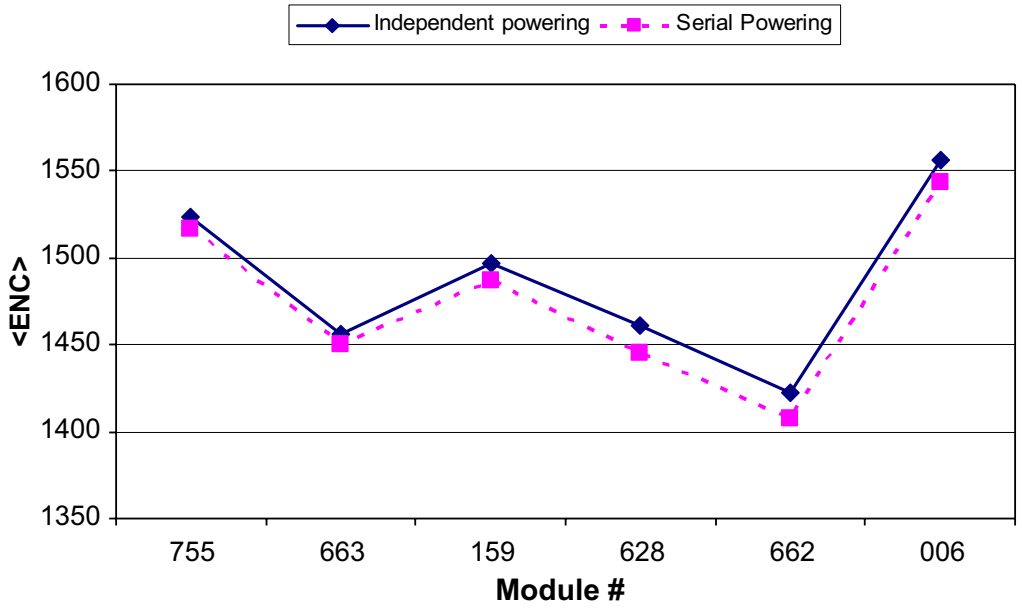

Figure 3.3: *The comparison of the noise between independent powering and serial powering [1].*

3.3 DC-DC conversion powering

DC-DC conversion is a natural and conventional approach, compared with the serial powering. Power are transmitted with high voltage and low current to decrease power burnt by the long cables. Local DC-DC step-down converter is utilized to generate the voltage required by sensors/readout chips. Consequently, DC-DC conversion is compatible with recent detector systems, which brings huge benefits. Almost no change is required for sensor chip. The DC-DC conversion can be based on the independent powering. Only one DC-DC step-down converter is required to be placed on each module. The thermal losses on cables are reduced from nI^2R to $n(I/g)^2R$, where n is the number of modules, I is the current consumed by one module and g is the ratio of input voltage to output voltage of the DC-DC converter. It should be noted that the DC-DC conversion powering does not decrease the number of cables. The DC-DC conversion can also be implemented by parallel powering. Only a single cable provides power to all modules. The cable number are decreased and the thermal losses are reduced to n^2I/g^2R. Same reduction is achieved as in serial powering, if g equal n. The step-down converter is the critical element in DC-DC conversion, which can be implemented by buck DC-DC converter, switched capacitor DC-DC converter or piezoelectric transformers.

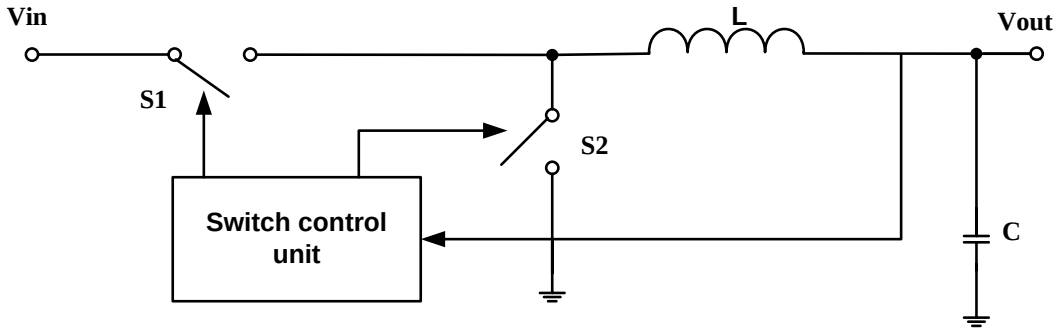

Figure 3.4: *Architecture of buck converter.*

3.3.1 Buck DC-DC converter with air-core inductors

The buck DC-DC converter is popular in the power system. As shown in figure 3.4, the buck converter consists of an inductor as an energy storage unit, two switching transistors, a switch control unit and a filtering capacitor. The inductor is charged/discharged by switching the transistor s1 on/off (s2 off/on). The gate voltages of the switching transistors come from the switch control unit. Thus, the output voltage can be stable with proper charging and discharging time/frequency, which is adapted by the switch control unit according to the feedback. The control modes usually used are pulse width modulation (PWM), pulse frequency modulation (PFM) and hysteresis mode. PWM is the most common control mode. Some converters are designed to work in PWM/PFM modes to achieve high efficiency, which work in PFM at low load and in PWM at high load. New challenges are brought to the buck DC-DC converters used in high energy physics experiments. These DC-DC converters are certainly exposed to very strong magnetic and radiation fields, since they are placed near the interaction point. Though buck converters can be widely found in the marketplace, the commercial DC-DC converters can not fulfill the requirements of the high energy physics experiments [5]. Firstly, the ferromagnetic inductors are not allowed. In DC-DC converter, the parasitic resistance of the inductors should be as small as possible to achieve high power efficiency. Thus, ferromagnetic core is used to get a larger inductance (several μH) with small parasitic resistance. Unfortunately, the ferromagnetic core saturates in very strong magnetic field of the high energy physics experiments (e.g., about 4T in LHC). The ferromagnetic inductors have to be replaced by the coreless (or air-core) inductors. If the same inductance must be achieved as the ferromagnetic inductors, a greatly longer wire needs to be wound. The parasitic resistance becomes unacceptable, as well the space occupied. Consequently, the inductance must be decreased down to below 1 μH. In order to supply high output current and limit the

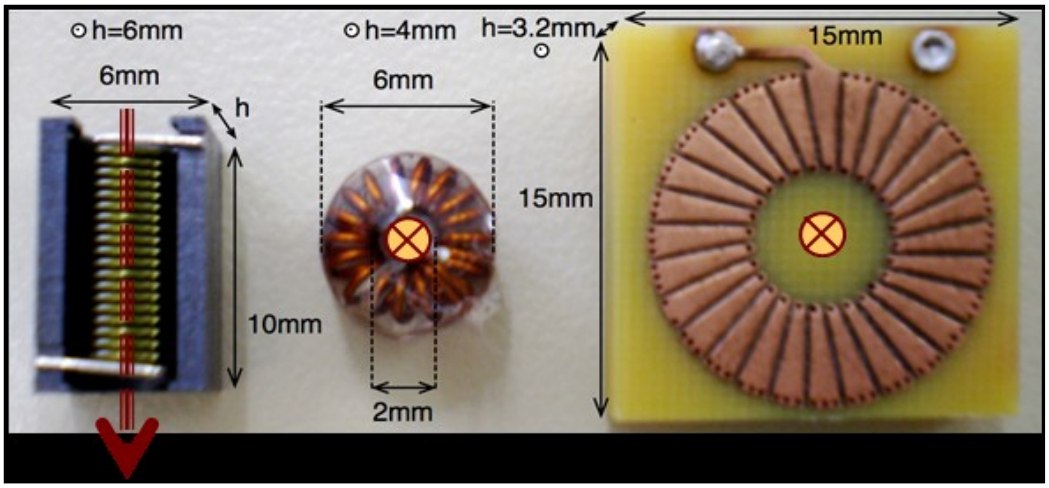

Figure 3.5: *Solenoid (left), air core toroid (center), PCB toroid (right) [8].*

current ripple, the switching frequency of the converters has to be set beyond 1 MHz with such a low inductance. Secondly, the commercial converters are fabricated in commercial-grade semiconductor processes. The radiation tolerance may not be considered. They fail to work in the strong radiation field, which is proved by the test [5]. The radiation hardness design is essential to be involved in the DC-DC converter. Consequently, full customer buck converters must be designed [6] [7].

Choosing or designing a proper inductor is an important issue in the design of the full customer buck converters. In order to meet the requirement of high power efficiency, low space occupied and low material budget, the inductance is limited to maintain affordable size. The work in [9] indicates that the inductor with an inductance value between 500 nH and 1 μH is foreseen as a good trade-off. In addition, the switching current inside the air-core inductor will produce an AC magnetic field [10]. However, the magnetic field lines are not well confined inside a definite volume in air-core inductor compared with ferromagnetic-core inductor. Therefore, the AC magnetic field degrades the neighboring sensor/readout circuits. The inductor should reduce the emission of magnetic field. Three inductors with different shapes (see figure 3.5) were tested in [8]. The toroidal topology allows enclosing the main magnetic field inside the coil volume, compared with solenoid and PCB toroid. Though shield PCB toroid has shown lowest emission of magnetic field, it is very difficult to be manufactured and the shield reduces the inductance value. Thus, the air-core troidal inductor may be a good choice.

Switching noise is an intrinsic feature of buck DC-DC converter due to the operation of switches. Ripple appears in the output voltage. The following electronics may be

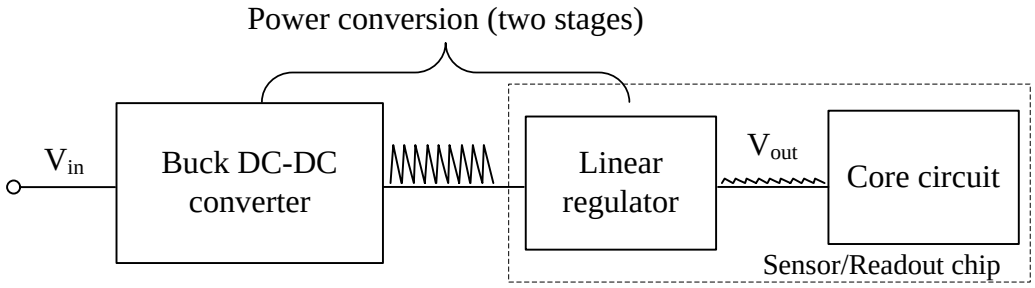

Figure 3.6: *Post-regulator built-in the low-noise electronics.*

influenced by the noisy power supply. Though shied or filter capacitors can decrease the ripple voltage, the material budget are increased. In order to suppress the switching noise and not to increase material budget, a linear regulator is integrated in the sensor/readout chip to function as the post-regulator of the buck DC-DC converter, as shown in figure 3.6 [11] [12].

3.3.2 Switched capacitor DC-DC converter

Another alternative implementation is the switched-capacitor DC-DC converter (also called charge-pump), which is composed of a few capacitors/pump capacitors and a control unit. The capacitors are utilized to store energy. Lower output voltage can be achieved by altering the connection structure of pump capacitors, as depicted in figure 3.7. The capacitors are connected in series between input voltage and output voltage during charge phase. Then they are connected in parallel during discharge phase. Thus, the output voltage is decreased to 1/n of the input voltage where n is the number of the pump capacitors of same value.

Compared with buck DC-DC converter, switched capacitor DC-DC converter is more promising to be fully integrated on-chip. Ceramic capacitor miniaturization makes great progress in recent years, while inductor can not be greatly improved. Moreover, capacitor can be easily integrated on-chip. Fully integrated on-chip switched capacitor DC-DC converters have been designed and fabricated [13] [14]. The small size can decrease the material budget and board space. On-chip converter is also helpful to reduce noise and simplify the design of ladder.

The pump capacitance is constrained by the affordable silicon area. Moreover, the ripple voltage should be sufficient low, which is proportional to the output current, as

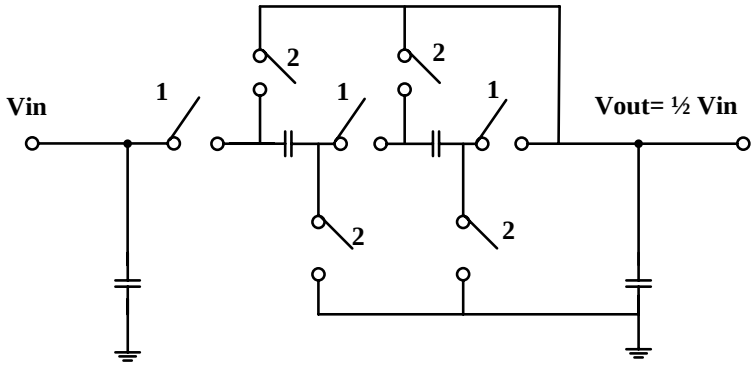

Figure 3.7: *Simplified schematic diagram of a divide-by-two charge pump, "1" and "2" represent "charging" and "discharging" phase, respectively.*

expressed in 3.1 [15].

$$\Delta V_o \approx 2 I_o ESR_{C_{pump}} \frac{I_o}{2 f_{switch} C_{pump}}, \tag{3.1}$$

where ΔV_o is the output ripple voltage, I_o is the output current, f_{switch} is the switching frequency, C_{pump} is the pump capacitance and $ESR_{C_{pump}}$ is the equivalent series resistance (ESR) of C_{pump}. Assuming that $ESR_{C_{pump}}$ is negligible, C_{pump} is 500 nF when ΔV_o is 0.1 V, I_o is 100 mA and f_{switch} is 1 MHz. The silicon area consumed is about 0.25 mm^2 with the sheet capacitance of 2 $fF/\mu m^2$. Thus, the maximum output current is limited to few 100 mA in order to achieve an affordable size of pump capacitance. The advanced technology of fabricating higher sheet capacitance is also needed.

3.3.3 Piezoelectric transformers

The piezoelectric transformer (PT) was invented in the 1950s [17], but has become of significant commercial interest only recently. Piezoelectric materials are characterized as smart materials. The piezoelectric effects are considered to be the result of linear interaction between electrical and mechanical systems. Piezoelectric materials can sense the electric field (or vibration) and then vibrate (or generate charges). They can develop a charge when mechanically stressed (the direct piezoelectric effect) and develop a strain upon the application of an electric field (the converse piezoelectric effect) [18]. The operation principle of the piezoelectric transformer is a combined function of actuators and sensors so that energy can be transformed from electrical form to electrical form via mechanical vibration. Piezoelectric transformers are made from piezoelectric ceramics. Thus, the favorable attributes of the PT are its high energy storage capacity, high energy efficiency, low size, low electromagnetic noise and large gain [1] [19] [20]. Good high volt-

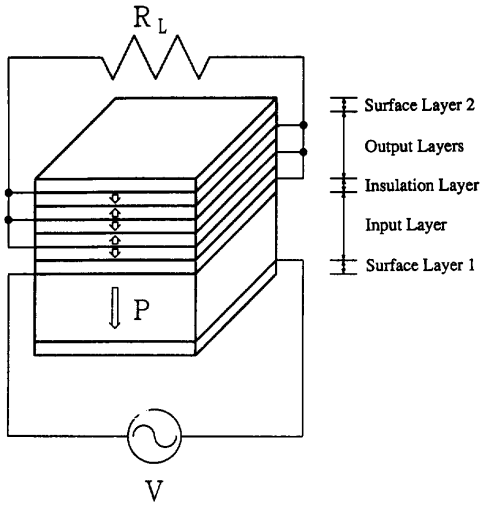

Figure 3.8: *Piezoelectric transformer construction [16].*

age isolation characterizes the piezoelectric ceramics. Thus, PT is widely applied in high voltage applications with lower size and lower costs, compared with high voltage electromagnetic transformers. The potential applications of PT include ionizers, ion generators, electron microscope, photomultiplier power supplies and others [19].

PTs can be simply classified into the longitudinal vibration mode PTs and the thickness vibration mode PTs by their vibration modes. Figure 3.8 depicts the thickness vibration mode PT, which is suitable for high frequency and step-down operations [21]. The input layer is thick while the output layer is divided into several thinner layers. The insulation layer separates the adjacent layers. Thus, the input voltage is decreased with a radio of the thickness of the input layer to the thickness of a single output layer [21] [16]. Moreover, the voltage gain of a PT is also dependent upon the load resistance, the operating frequency and temperature. The PT behaves like a resonant band-pass filter. Thus, the efficiency of a PT is maximal when the device is operated closed to its resonant frequency [22].

The PT also find its application in DC-DC conversion. The PT control strategies are complex in order to maintain a desired efficiency level. Several control schemes have been proposed including PWM, PFM and the schemes using a combination of the two [20]. Figure 3.9 depicts a control topology for PT [1]. A voltage-controlled oscillator (VCO) and its driver modulate the frequency of the driving voltage at the input layer of PT, according to the load resistance and the input voltage. An output voltage of different amplitude is generated from the output layer, which enters a rectifying and filtering circuit to be a DC level. The feed-back circuitry is utilized to set the driving frequency and stabilize the

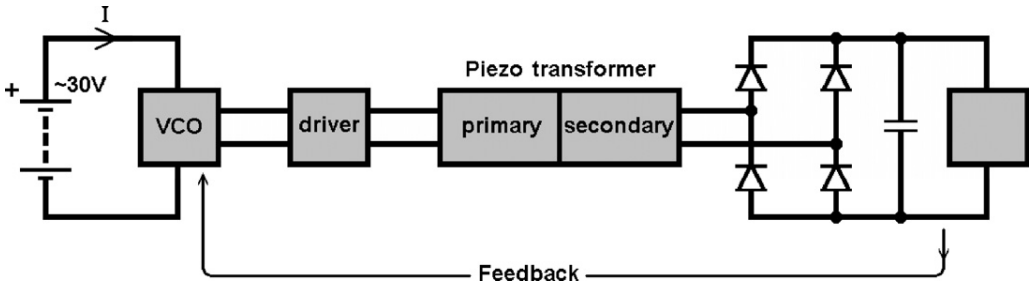

Figure 3.9: *Sketch of a four-terminal piezoelectric transformer used as a DC-DC converter powering a module [1].*

output voltage.

The PTs should be further researched in order to be realized in the power distribution for particle physics experiments due to their specified requirements. Some critical features of PT must be clarified, such as the size, packaging and assembly on hybrid, material budget and radiation tolerance [1].

3.4 Comparison of serial powering and DC-DC conversion

As mentioned above, both approaches are promising and have specific benefits and drawbacks. The features of independently powering (IP), serial powering (SP) and DC-DC conversion are listed in Table 3.1. The alternative approaches can result in high power efficiency and less cable number. They can replace the independently powering in the future detectors. However, more efforts must be paid for the implementation. The reliability and protection of the powering are required in the new approaches. Moreover, the additional circuits should be designed for serial powering, such as the AC-coupling of the digital signal. It is still very difficult to evaluate which one is better, recently. The optimal choice strongly depends on the detector characteristics and the experiments requirements.

3.5 The power distribution proposed for CPS

Since the DC-DC conversion with parallel powering is compatible to the existing detector systems compared with the serial powering, it is proposed to be used in the power

Table 3.1: *Features of IP and alternative approaches [1].*

	IP	SP	DC-DC conversion (parallel powering)	Comments
Power efficiency	10-20%	60-80%	60-80%	Varies with I, the number of module (SP); gain (DC-DC)
Local regulator inefficiency	N/A	∼10%	<20%	This is without linear regulator for analog
Number of power cables	4 per hybrid	Reduction by factor 2n	Reduction by factor 2n	n= number of hybrids
System ground potential	One ground level	Different for every module	One ground level	
Noise	Noiseless	Noiseless, even better	More noise due to the switching and the electromagnetic in buck	
Compatibility with existing detector systems	Adapted in the trackers now	Many changes are needed. AC-coupling or optical decoupling of digital control and data signal.	Very little changes. Integrating the converter on chip will be a problem.	
Reliability/ Protection	Separate set of cables for each hybrid	Local over-current protection; redundant regulators	converter failure leads to loss of modules possibility to switch off individual modules	Protect against open (SP) and short (DC-DC)

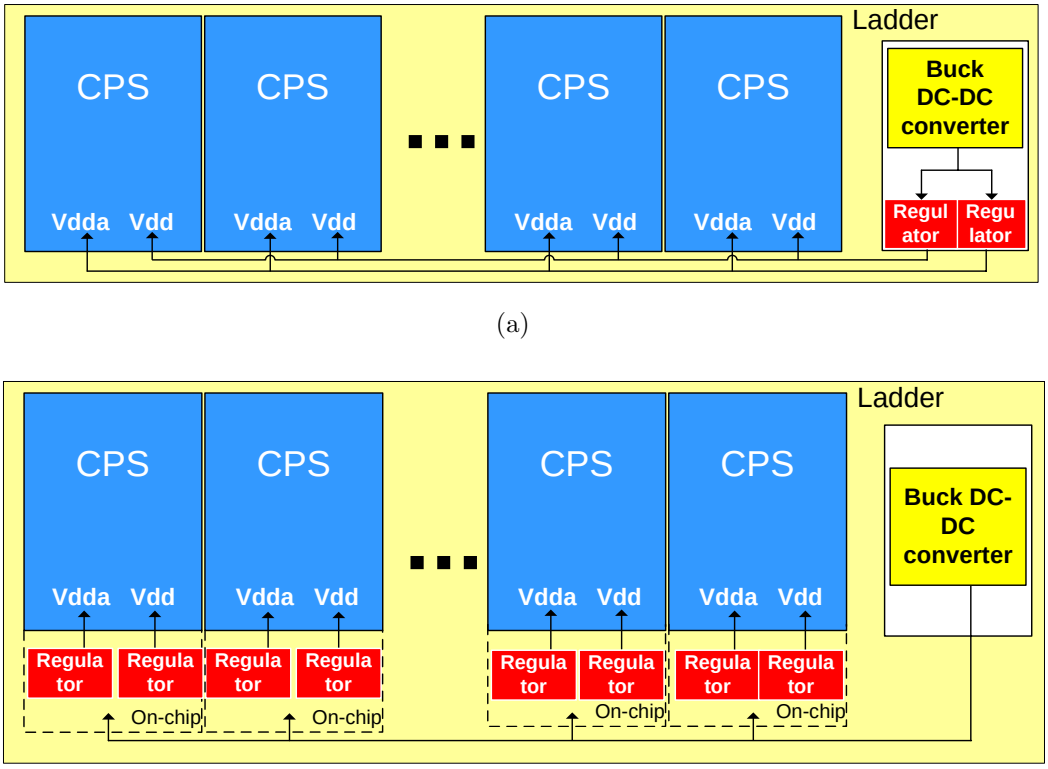

Figure 3.10: *Schemes of the power distribution for CPS chips in a ladder: employing discrete regulators (Reg) (a) and on-chip regulators (Reg) (b).*

distribution for CPS with less extra effort. The pixel array of CPS is usually powered by a separate analog supply voltage, which should be low-noise since the signal detected by pixel is very weak. Thus, the post regulator for analog supply-voltage is necessary. Two schemes of power distribution are proposed for CPS chips in a ladder, as depicted in figure 3.10. Two discrete regulators are used to generate the analog power supply (vdda) and digital power supply (vdd), respectively. Only one discrete regulator following the buck DC-DC converter supplies power (vdd/vdda) to several CPS chips in a detector ladder, as shown in figure 3.10(a). However, this scheme complicates the post regulator design due to the extremely high load current. Moreover, the CPS chips in a ladder influence their neighbors since they share the same long power line and any extra decoupling capacitors are not allowed to meet low material budget. In order to address this problem, the discrete regulator can be placed near to each CPS chip if there is sufficient space in the ladder, as shown in figure 3.10(b). However, the material budget is worsened and the ladder design becomes complicated. Consequently, it is essential to fully integrate regulators on CPS chip.

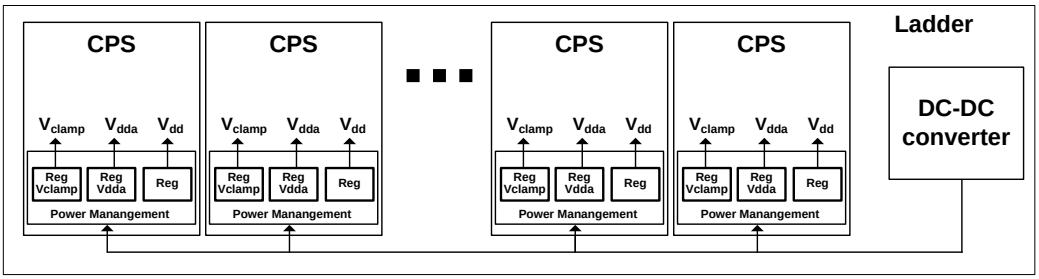

Figure 3.11: *Power distribution for CPS in a ladder.*

The scheme of the power distribution for CPS is proposed in figure 3.11. Power of several CPS chips (about 10) in a ladder is supplied by a buck DC-DC converter. Then, the output voltage enters a power management built in each CPS, which generates different voltages required and directly supplies power to other core circuits. Thus, the noise of the converter and crosstalk can be eliminated by the post-regulators.

In order to avoid interference between analog circuit and digital circuit in CPS, they are powered by analog supply voltage and digital supply voltage, respectively. Especially, the noise of the analog supply voltage should be sufficient low due to the weak signal detected in the order of about a few millivolts. Though switching regulator has higher power efficiency, its output ripple voltage is troublesome. Thus, a linear regulator named RegVdda is designed and employed in CPS [23]. This linear regulator can also function as a post-regulator to suppress the ripple voltage coming from the DC-DC converter at the end of the ladder. In order to improve the power efficiency, the dropout voltage is low to 0.3 V. The digital supply voltage is proposed to be generated by a switched capacitance converter.

Some reference voltages are required when CPS chips work. In order to decrease noise and the number of the cables, they are also generated by the power management. Clamping voltage is one of the critical reference voltages used in the correlated double sampling (CDS) operation at pixel level. The noise induced by it can corrupt the readout signal, which cannot be completely eliminated by the CDS operation. Thus, an ultra-low noise voltage is necessary. An full-custom linear regulator named RegVclamp, is dedicated to generating clamping voltage in the power management [24].

3.6 Conclusions

In order to improve the power efficiency and decrease material budget in detectors, two promising approaches have been presented. The structures and implementation of these approaches are described in detail. The modules are connected in serial in serial powering. Thus, the current is shared and the number of cable is decreased. The DC-DC conversion powering transforms the power with high voltage and low current. The voltage required by modules is generated by local regulators. The feature comparison among these approaches is also given. DC-DC conversion is compatible with the existing detector systems without changing sensors. Thus, a possible power distribution is proposed for CPS, which is based on DC-DC conversion.

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Chapter 4

Radiation effects and radiation hardening by design

As mentioned in Chapter 2, CMOS pixel sensors usually work near the interaction point in high energy physics experiments. A great number of particles are produced during the collision, including charged particles and neutral particles. Thus, CMOS pixel sensors operate in harsh radiation environment. The regulators are required to resist the radiation to be integrated in the CMOS pixel sensors, as mentioned in Chapter 3. In this chapter, the radiation effects are firstly introduced including their mechanics and their effects to CMOS integrated circuits. Then, the radiation hardening techniques are presented. The techniques of hardening against ionizing radiation is focused.

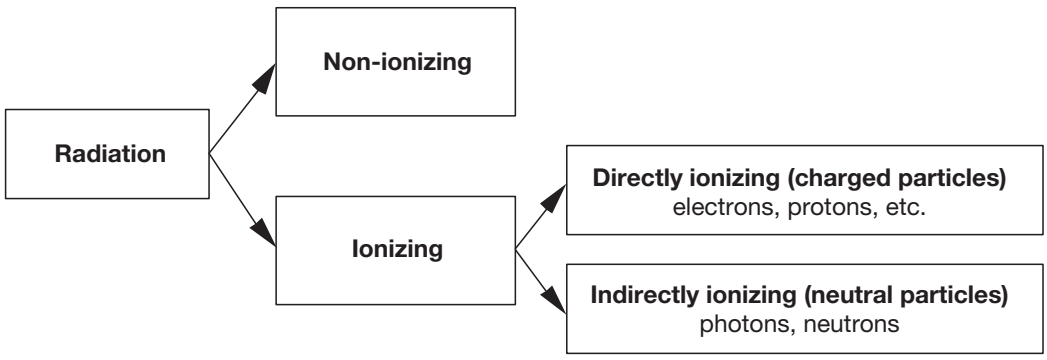

Figure 4.1: *Classification of radiation [1].*

4.1 Introduction

Radiation can be classified in many ways. According to whether the matter is ionized, the radiation is classified into ionizing radiation and non-ionizing radiation, as shown in figure 4.1. The non-ionizing radiation refers to any radiation, that dose not ionize the atoms of medium. There are two types of ionization radiation: directly ionizing radiation and indirectly ionizing radiation. The charged particles, such as electrons, protons, alpha particles and beta particles, can deposit energy in the medium and eject orbital electrons directly from its atoms by interacting with the Coulomb force. The atoms are ionized and directly ionizing radiation happens.

The neutral particles, such as photons and neutrons, can result in ionizing by the indirectly ionizing radiation, though they do not carry charges. Different with directly ionizing radiation, indirectly ionizing radiation is complicated and happens through a two step process [1]:

- In the first step a charged particle is released in the medium by the neutral particles due to electromagnetic or nuclear interaction (photons release electrons or positrons, neutrons release protons or heavier ions);
- In the second step the released charged particles deposit energy to the medium through direct Coulomb interactions with orbital electrons of the atoms in the medium, like the directly ionizing radiation.

The ionizing and non-ionizing radiation may happen and damage the semi-conductor devices in different ways. Thus, the radiation effects and radiation hardening by design are necessary to be researched and analyzed. The following sections will discuss that in detail.

4.2 Ionizing radiation

Oxides and insulators are the fundamental components in electronic devices fabricated in CMOS process. When the devices are exposed to strong radiation, significant charges are built up in these components due to ionizing radiation [2]. These charges can be classified into two primary types: oxide-trapped charges and interface-trapped charges. If sufficient charges are accumulated after a period, the characters of CMOS transistors vary, such as large threshold voltage shifts, leakage current increase and mobility degradation. These effects are called total ionizing dose effects (TID effects). In addition, one single

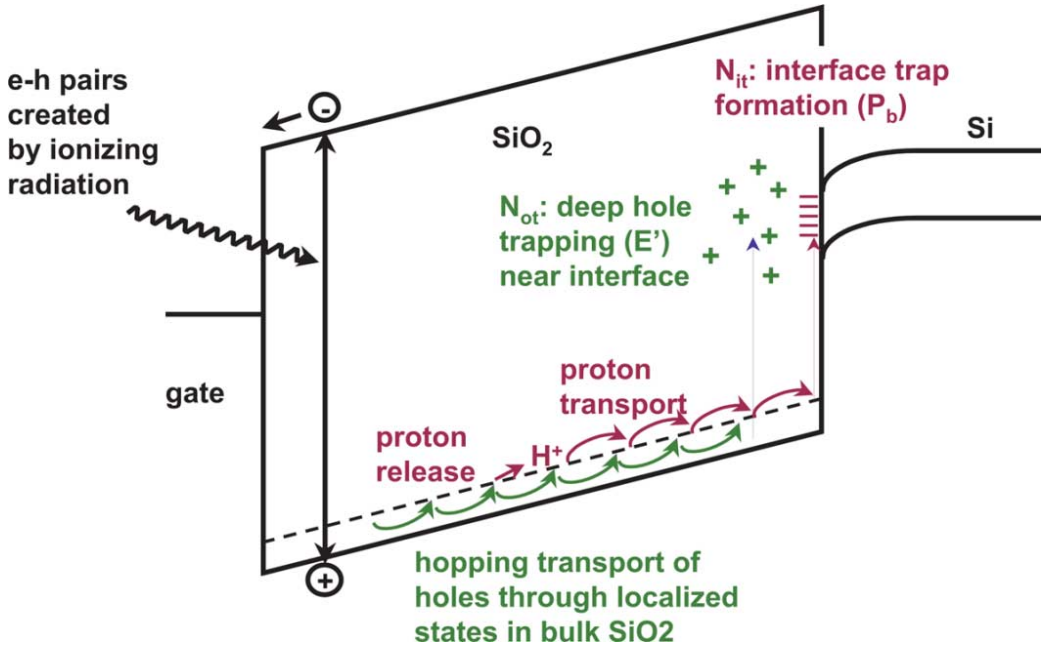

Figure 4.2: *Band diagram of an MOS capacitor with a positive gate bias. Illustrated are the main processes for radiation-induced charge generation [2].*

particle with high energy can cause an immediate malfunctioning of one or more transistors and then influence the entire circuit, which are called single event effects.

4.2.1 Total ionizing dose effects

Total ionizing dose refers to the integrated radiation dose that is accrued over a certain period of time (e.g., 1 year or over 15 years). This effect is related to time. The injecting particles may release charges in the semiconductor devices when they are placed in radiation environment. For example, high-energy electrons and protons can ionize atoms, generating electron-hole pairs. As long as the energies of the electrons and holes generated are higher than the minimum energy required to create an electron-hole pair, they can in turn generate additional electron-hole pairs. Thus, one high-energy particle can generate many electron-hole pairs. All the charges are deposited and accumulated with time. As a consequence, the semiconductor devices can be damaged if the accumulated charges are sufficient. For example, the insulating materials become less insulating. The capacitors may fail or the capacitance decreases [3]. Especially, the features of CMOS transistors change, which can influence the entire circuits.

As shown in figure 4.2. The incident charged particles create electron-hole pairs in the

insulating oxide (SiO_2) layer of MOS structure, when they pass through the oxide. In the first few picoseconds, some electrons and holes recombine. The fraction of recombination depends on the applied field and the energy and type of incident particles [2] [4]. After the recombination, the electrons and holes are free to diffuse and drift away from their points of generation in the presence of applied bias voltage. Since the electrons are more mobile than the holes, they are swept out of the oxide by the electric field. However, some of the holes still stay near their point of generation, which are like being trapped in the oxide. They cause a net positive charge and are called "oxide traps". Other holes reach the SiO_2/Si interface undergoing a slow, stochastic "trap-hopping" process through the oxide. A fraction of these holes are captured in long-term trapping sites called "interface traps". These interface traps are negatively charged, which are localized states with energy levels within the Si bandgap. They can cause small negative voltage shifts which may persist in time for few hours to several years. Moreover, the interface traps may cause a degradation in mobility of the carriers in the channel of MOS transistors. The speed of the digital circuit and the channel conductance are degraded.

4.2.1.1 Threshold-voltage shift in MOS transistors

The total threshold-voltage shift of MOS transistors depends on the combination of the effects of oxide traps and interface oxide, expressed by 4.1.

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it}. \tag{4.1}$$

$$\Delta V_{ot,it} = \frac{-1}{C_{ox} t_{ox}} \int_0^{t_{ox}} \rho_{ot,it}(x) x dx. \tag{4.2}$$

where $\Delta V_{ot,it}$ is the threshold-voltage shift induced by oxide traps or interface traps, C_{ox} is the unit capacitance of oxide layer, t_{ox} is the thickness of oxide layer and $\rho_{ot,it}(x)$ is the charge distribution of radiation-induced oxide-trapped or interface-trap charge. The sign of radiation-induced interface-trap charge is different in PMOS transistors (positive) and NMOS transistors (negative) due to the different gate bias voltage. However, the oxide-trap charges are positive in PMOS transistors and NMOS transistors, as described in last section. As a result, the threshold-voltage shift of PMOS transistors is negative, as depicted in figure 4.3. In other words, the PMOS transistors are more difficult to be turned on when they are exposed to the radiation. However, the threshold voltage of NMOS transistors may decrease due to the oxide-trap charges. The NMOS transistors are easier to be turned on, even remain on with zero gate bias. Thus, the PMOS transistors are more

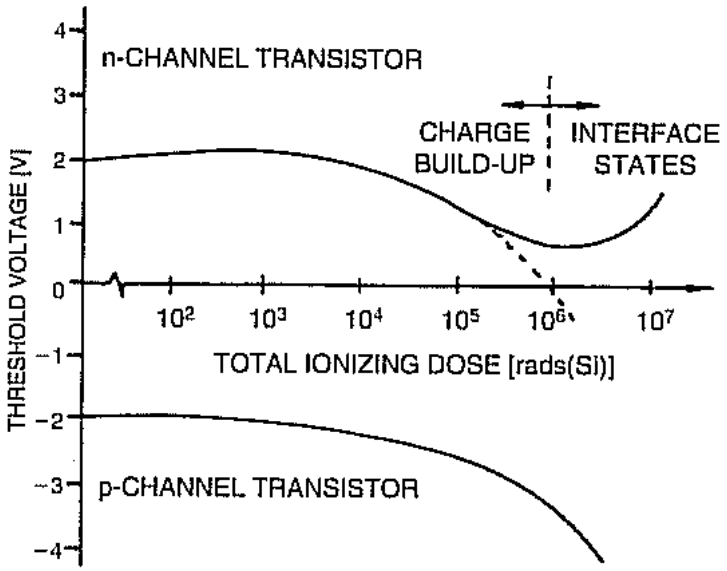

Figure 4.3: *Threshold voltage shift of NMOS and PMOS transistors versus dose [5].*

radiation-resistant than the NMOS transistors. Since the processes of oxide-trap buildup and interface-trap buildup have relationship with dose and time, the threshold-voltage shift of NMOS transistors varies, as shown in figure 4.3. More interface-trap charges are built up with long time. However, the exiting oxide-trap charges are neutralized and decreased. The threshold-voltage shift can be large and negative for either NMOS or PMOS transistors at high dose rates with short time, where the oxide traps dominate. At moderate dose rates, both ΔV_{ot} and ΔV_{it} are large. However, they compensate with each other in NMOS transistors resulting in relatively high failure level of an integrated circuit. At low dose rates for long times, a large fraction of the oxide-trap charges are neutralized. More interface-trap charges are allowed to build up and dominate due to the long time. The threshold voltage of NMOS transistors is increased. Nevertheless, the carrier mobility are decreased because of the interface traps [6].

4.2.1.2 Increase of leakage current

The threshold voltage decreases in NMOS transistors at high and moderate dose due to the oxide-trapped charges in gate oxide. Thus, the leakage current increases, as depicted in figure 4.4. The increase of leakage current depends on the dose level. After the long time radiation, the leakage current tends to decrease with time, since the threshold voltage increases as mentioned in last section. Moreover, the radiated field oxide also leads to larger leakage current.

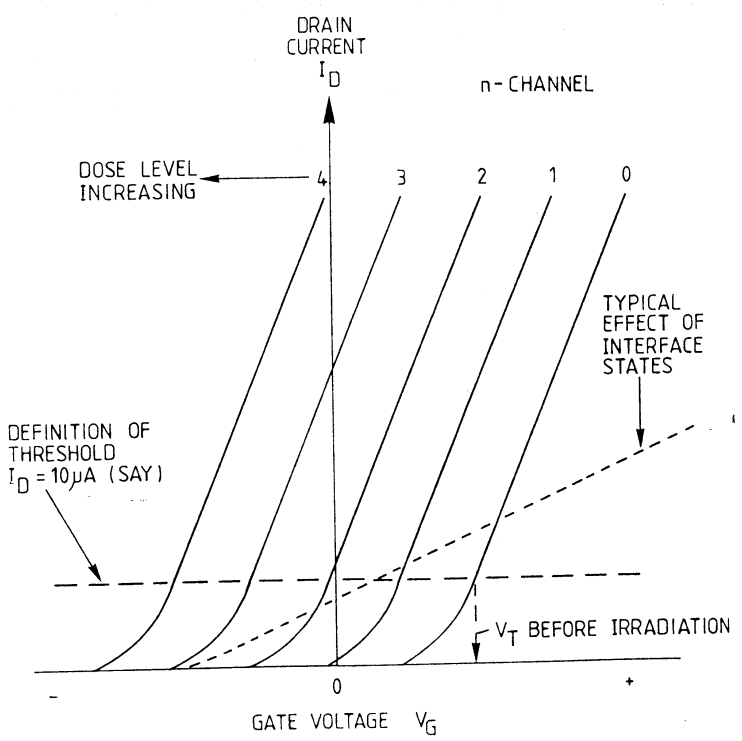

Figure 4.4: *Drain current of NMOS transistors with increasing dose level [7].*

Since all the CMOS transistors are rounded by the field oxide, the radiated field oxide not only induces current path between source and drain in one transistor, but also induces oxide traps in field oxide between adjacent transistors. Two common types of field oxide isolation used today are local oxidation of silicon (LOCOS) and shallow-trench isolation (STI) [8]. Unfortunately, radiation-induced positive charges were observed in both topologies [9]. An n-type region can be formed by these positive charges. Therefore, conducting paths are generated if sufficient charges build up. Figure 4.5 illustrates the two possible leakage pathes in field oxide. One is at the edge of the gate oxide between source and drain in a NMOS transistor. Another path is between the source or drain region of a NMOS transistor and the n-well of adjacent PMOS transistors. Since the radiation-induced charge in field oxide is predominantly positive, the static power supply current increases in NMOS transistors. Though the gate oxide is significantly decreased in the advanced commercial processes, the field oxide is still thick (100 nm - 1 μm). The field oxide has become the dominant source of integrated circuits failures.

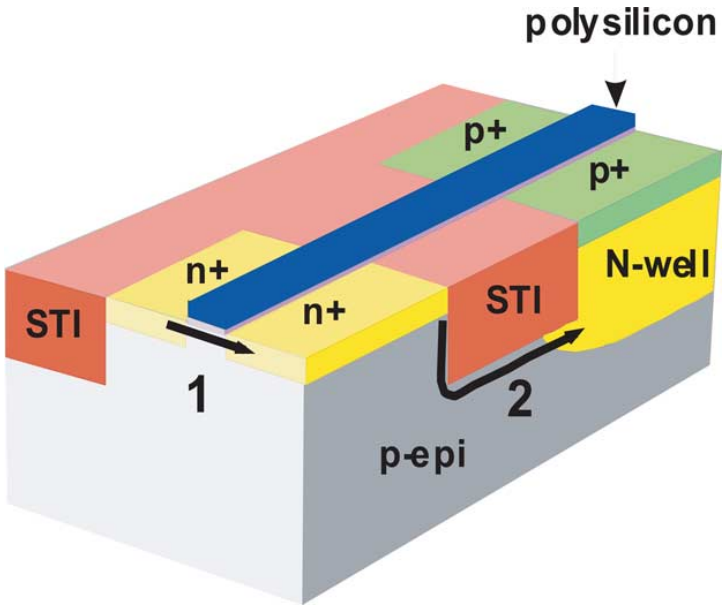

Figure 4.5: *Possible leakage pathes in a shallow-trench isolation technology [10].*

4.2.1.3 Decrease of mobility

The radiation reduces the mobility of CMOS transistors, since the oxide-trapped charges and interface-trapped charges act as scattering centers for carriers in the channel [5] [11] [12]. The mobility degradation is essentially related to the increase of the interface-trapped charge and oxide-trapped charge near the $SiO_2 - Si$ interface, especially in high dose level. Their relationship can be expressed by

$$\mu = \mu_0 \frac{1}{1 + \alpha_{ot}\Delta N_{ot} + \alpha_{it}\Delta N_{it}}, \tag{4.3}$$

where μ_0 is the pre-irradiation mobility, α_{ot} and α_{it} are the coefficients describing the effects of oxide-trapped charge and interface-trapped charge, respectively, and ΔN_{ot} and ΔN_{it} are the concentrations per unit area of oxide-trapped charge and interface-trapped charge, respectively [11] [13].

It has been demonstrated that the interface-trapped charge is dominant in the channel-mobility degradation mechanism [5]. More interface traps can result in decrease of channel mobility, as shown in figure 4.6. Since the conduction of a MOS transistor is due to the carrier motion close to the silicon-oxide interface, the transconductance of transistor decreases. Noise increases in turn, such as the flicker noise.

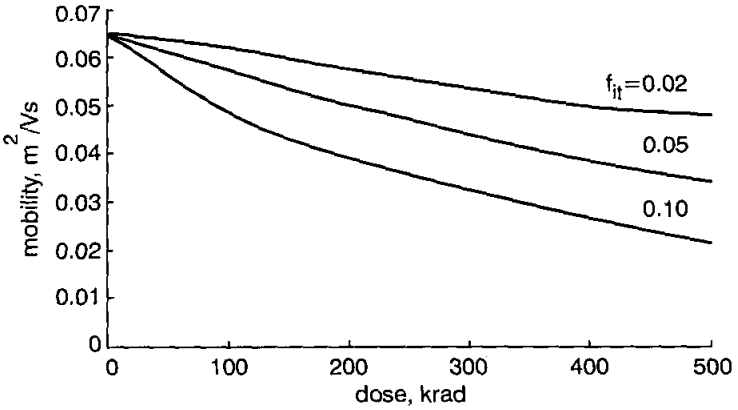

Figure 4.6: *Variation of mobility of surface channel with increasing dose and three different generation efficiencies of interface trap charge [11].*

4.2.2 Single-event effects (SEE)

As the geometries of integrated circuits and operating voltage decrease, a single high energy particle (e.g., a proton, neutron or heavy ion) may disturb an active electronic device. These effects are induced by a single particle in short time. Thus, They are called single-event effects. SEE may result in soft errors, transient upsets, hard errors and permanent failures. The main SEE include single-event upset (SEU), single-event transient (SET), single-event latch-up (SEL) and single-event burnout (SEB), which will be respectively introduced in following subsections.

4.2.2.1 Single-event upset (SEU)

SEU happens when a single particle passes through a device and deposited energy in semiconductor devices leading to instantaneous modification of the logic state. This usually occurs in digital circuits, such as the memories, latchs and so on. The incoming particle generates charges along its track. If the sensitive node in the circuits collects sufficient charges, the logic "1" ("0") may convert to logic "0" ("1") in a memory or latch cell. The function of the whole system may be influenced. Fetal errors may happen if the critical data is converted due to SEU. Fortunately, the value will become correct when it is refreshed after the next logic cycle. Thus, SEU is a kind of soft error.

It should be noted that not all particles can cause SEU in semiconductor devices. Only the generated charges, which are sufficiently close to the sensitive node, can be collected. In addition, the collected charges should be sufficient to induce converting. Thus, critical charge is proposed to consider and evaluate the SEU susceptibility in devices.

The critical charge is defined as the minimum charge that must be deposited in a device to cause an upset, which is equivalent to the number of stored electrons representing the difference between logic ”0” and logic ”1” [14]. Obviously, the critical charge varies with the capacitance of sensitive node, power supply voltage and circuit implementation. However, both the node capacitance and the power supply voltage are decreased in the advanced technologies, which characterize smaller feature size. Moreover, a latch usually follows several combination logical elements in digital circuits. This latch may store error data, if a combination logical element is hit by a high energy particle at the jump edge of the system clock. Thus, SEU is easier to happen and has become a challenge in digital circuit design used in radiative environment. The cells of register and latch are the most susceptible circuits to SEU.

4.2.2.2 Single-event latch-up (SEL)

Latch-up may happen due to the parasitic PNPN thyristor in CMOS process. As shown in figure 4.7, the power supply voltage (V_{DD}) and ground (V_{ss}) are connected, if the PNPN thyristor are turned on. The significant large current can burn the entire chip. The latch-up has been already well solved in non-radiative environment. However, electrical latch-up may be initiated by a high energy particle, such as a heavy ion, a proton or a neutron. The charge generated by the single particle can turn on the PNPN thyristor and current flows in the loop formed by the two parasitic bipolar transistors, as depicted in figure 4.7. The current becomes significantly large between power supply voltage and ground, until latch-up happens. This can result in destructive of entire circuit if the power supply is not turned off quickly enough. Thus, SEL is a hard error. It has been demonstrated that the SEL threshold is a strong function of the particle energy, the power supply voltage and the system temperature [8].

4.2.2.3 Single-event burnout (SEB)

SEB usually happen in the power MOSFET (vertical DMOSFETs) or other high voltage devices biased in the OFF state, when a heavy ion passes through. In general, p-channel MOSFETS are much less sensitive to burnout than equivalent n-channel devices [15] [16]. As shown in figure 4.8, a parasitic bipolar transistor is formed in the n-channel power MOSFET structure, where the n+ source acts like emitter, p-body acts like base and the epitaxial layer acts like collector [17]. The transient current caused by the heavy ion may turn on this parasitic bipolar transistor. Therefore, the forward biased second breakdown happen and significant large current occurs leading to the burnout of transistor.

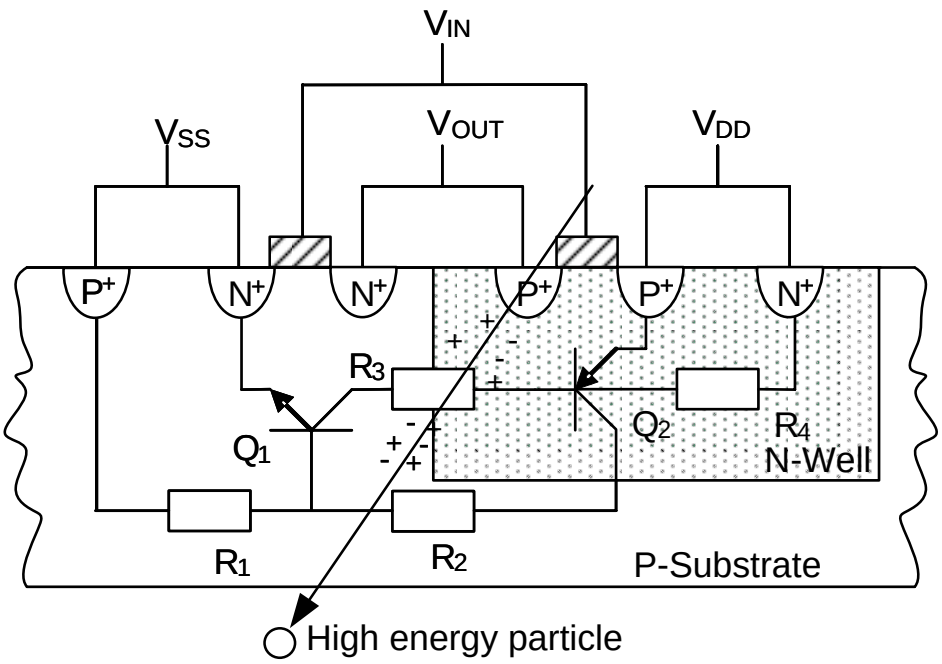

Figure 4.7: *Principle of SEL in an inverter illustrating charges induced by a single high energy particle.*

SEB is a kind of hard error and can permanently damage the entire circuit. Thus, the SEB must be considered in the switching power circuits where the power MOSFETs are employed. In order to prevent the burnout events, the single power MOSFET is replaced by two power MOSFETs connected in series [18]. The power MOSFET protects each other from SEB.

4.2.2.4 Single-event gate rupture (SEGR) or single-event gate damage (SEGD)

Besides the SEB, SEGR is another destructive effect when the power MOSFET is exposed to the radiation harsh environment [19] [20]. SEGR can rupture the gate oxide insulation leading to the gate leakage current and even device failure. The charges generated by the high energy particle (e.g., a heavy ion) can be accumulated in the silicon at the silicon-silicon oxide ($Si - SiO_2$) interface, when the power MOSFET is under appropriate bias conditions. The sufficient accumulation charge can result in significantly high electric fields across the gate oxide. Thus, the gate oxide insulation can be ruptured in this case [21]. The SEGR becomes a major concern, since the gate oxide is thinner in the modern CMOS processes.

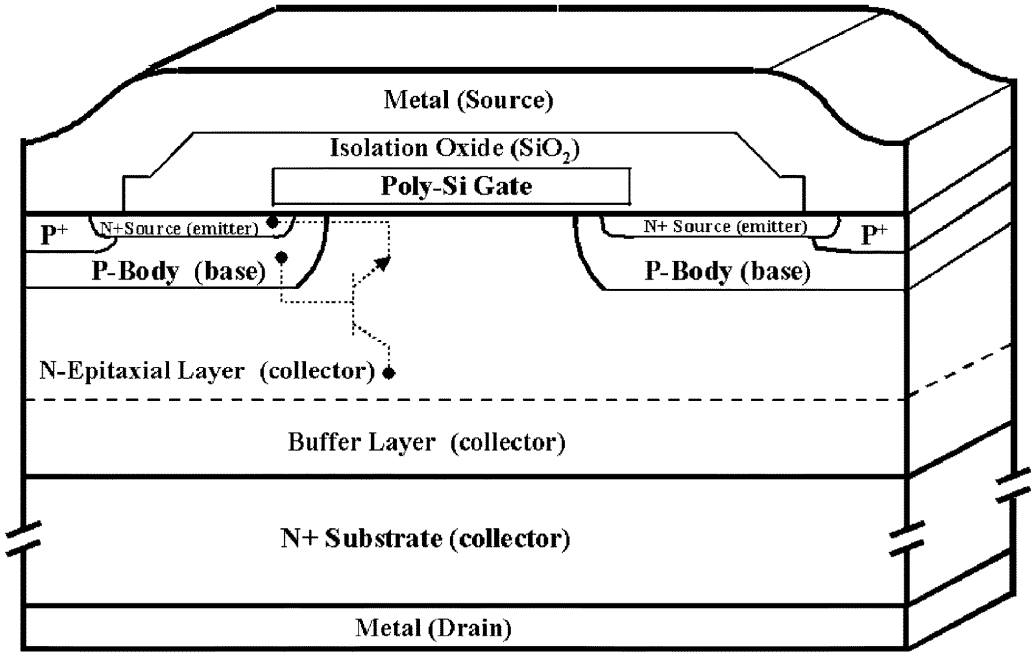

Figure 4.8: *Cross section of n-channel power MOSFET [17].*

4.3 Non-ionizing radiation or displacement damage

High energy particles lose their energy not only in ionizing process but also in non-ionizing process, when they inject and travel through a given material. The non-ionizing radiation results in displacement damage and produces defects in the material. The injecting energetic particle can displace an atom from their normal lattice position, where a vacancy is created. If that displaced atom moves into a non-lattice position, it becomes an interstitial. The combination of a vacancy and an adjacent interstitial is known as a Frenkel pair, as shown in figure 4.9. Additional types of defects can form when vacancies and interstitials are adjacent to impurity atoms [22]. In this way, many defects can be induced by a single energetic particle. Consequently, the displacement damage in semiconductors usually reduces the mobility and lifetime of the carriers. Moreover, the carriers can also be removed by trapping. Thus, dark current increases in imaging sensors, when displacement damage happens. Fortunately, the field effect transistors (FETs) are less sensitive to the displacement effects, compared to bipolar transistors [7].

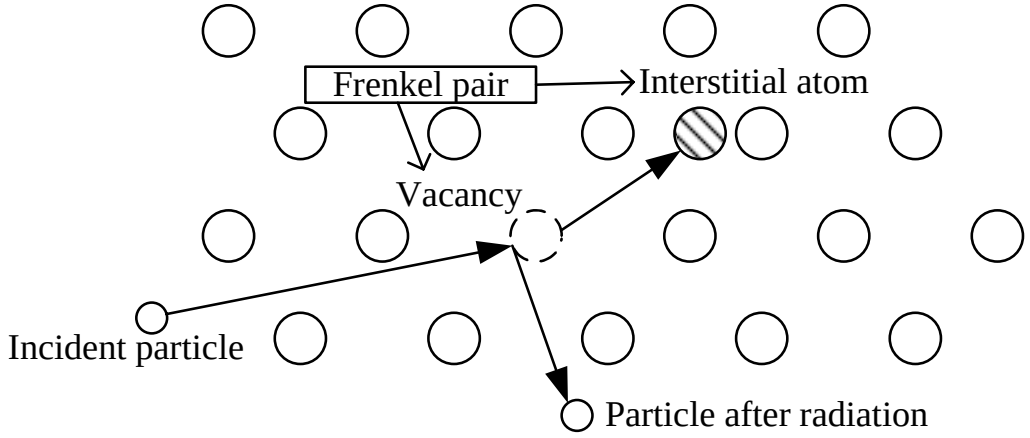

Figure 4.9: *Atom displacement damage.*

4.4 Radiation hardening by design

Since the CMOS pixel sensors used in high energy physics experiments work in high radiative environment, radiation hardening must be considered to assure the sensors work normally during its lifetime. The radiation hardening can be improved in three levels: process, layout and circuit architectures. Radiation hardening by design (RHBD) is popular with circuit designer, since it can achieve good radiation hardness with standard CMOS fabricated process. The main approaches are discussed below to harden against TID effects and/or single event effects.

4.4.1 Hardening against TID effects

TID effects depend on the oxide-trapped charges and interface-trapped charges in gate oxide and field oxide. Thus, decreasing the thickness of gate oxide can reduce TID effects. Fortunately, modern deep submicron CMOS processes decrease the thickness of gate oxide down to smaller than 5 nm (e.g., 5 nm in 0.25 μm). Few oxide-trapped charges and interface-trapped charges appear in the gate oxide. The threshold voltage shift is small enough to be negligible in these processes [23]. However, the field oxide is still thick even in the shallow trench isolation (STI) process. The leakage current between n+ doped regions at different potential is still too large. Avoiding the contact of field oxide and any p-doped region is an obvious method to decrease the leakage current. The enclosed layout transistor (ELT) has been proved to eliminate the leakage current under

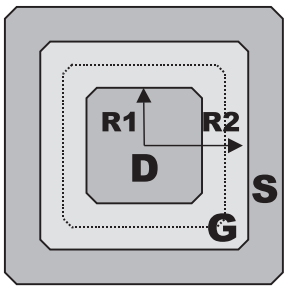

Figure 4.10: *Layout of the enclosed layout transistor [24].*

the gate edge of NMOS transistor [24] [25]. As shown in figure 4.10, the source or drain is completely surrounded by the thin gate oxide. Thus, the field oxide at the gate edge is removed and the leakage current path is prevented. In order to eliminate the leakage current paths between different NMOS transistors or NMOS transistor and its adjacent N-Well, p+ guard rings are inserted between these n+ diffusions [26]. The guard rings are heavily doped and are connected with ground. ELT NMOS transistors and guard rings are the radiation hardening design in layout level, not depending on particular manufacture. Consequently, they can be applied in the standard commercial CMOS processes without significantly increasing cost. However, ELT transistors bring difficulties in modeling, limitation in the W/L ratio, asymmetry and mismatch [27]. The ELT transistors also remarkably increase the silicon area.

4.4.2 Hardening against SEE

Though the downscaling of commercial CMOS technologies can help to improve the TID tolerance, they are more vulnerable to SEEs.

4.4.2.1 Hardening against SEU

The node capacitance and power supply voltage decrease in smaller feature size processes. Thus, they are more sensitive to SEUs. The memory cell and latch are vulnerable to SEU, as mentioned before. Some SEU tolerance cell architectures and layouts are proposed to decrease the sensitivity to SEU. Since the critical charge is directly proportional to the node capacitance, increasing the node capacitance of cell is a simple method to improve SEU tolerance. Larger capacitance was integrated either by increasing the size of some transistors or by adding metal-metal capacitors on top of the cells [28]. The larger transistors are also benefit to increase their current drive [27]. However, the power

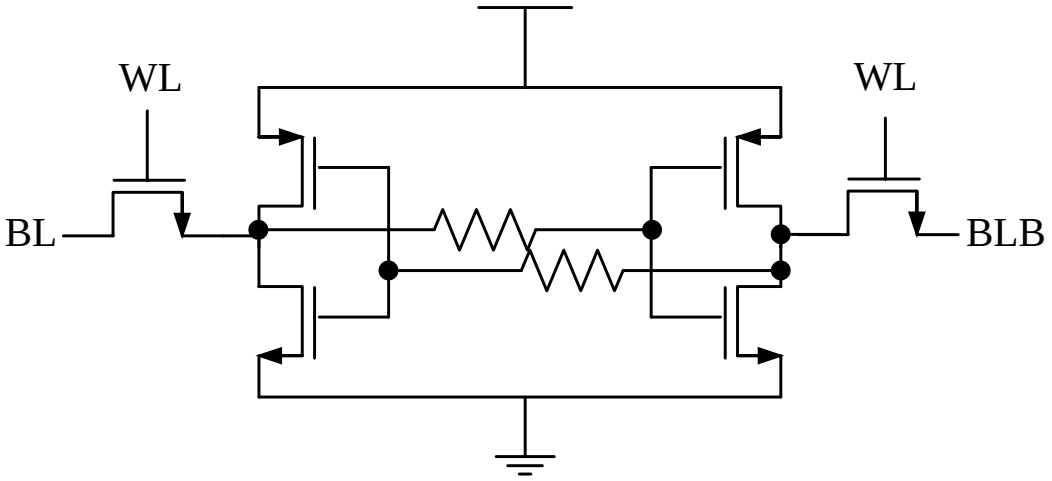

Figure 4.11: *Schematic diagram of a conventional RAM cell with feedback resistors [14].*

consumption becomes larger and two metal layers on top of the cells are occupied by the metal-metal capacitors.

The memory cells can be harden to SEU by increasing the delay in the feedback inverters, which delays the propagation of the signal across the loop. One of the most common approaches is adding two large resistors in the cross-coupling segment of each cell. One example is shown in figure 4.11. These two resistors with the gate capacitances of transistors create an RC time constant between the target node and feedback inverter [14]. However, this approach slows circuit response and increases the minimum cell write time.

Figure 4.12 depicts another SEU immune CMOS memory cell called Whitaker cell [29]. A logic configuration separates p-type and n-type diffusions nodes within the memory circuit. The storing nodes are duplicated so the data is stored in four nodes. Two nodes only have n-type diffusions and the other two only have p-type diffusions. The two nodes of the same type store opposite information. As we know, the particle strikes in n-type diffusion can only induce SEU when the stored value is logic ”1”. The particle strikes in p-type diffusion can only induce SEU when the stored value is logic ”0” [27]. Therefore, there are always two nodes storing uncorrupted data after SEU occurrence. In fact, the redundancy is used in this memory circuit to maintain a source of uncorrupted data, which can recover the corrupted data by feedback. Moreover, a particle hit-inducing current always flows from n-type diffusion to p-type diffusion [29].

Another dedicated architecture is dual interlock cell (DICE), as shown in figure 4.13 [30]. It has been extensively used in real applications owing to its property of being

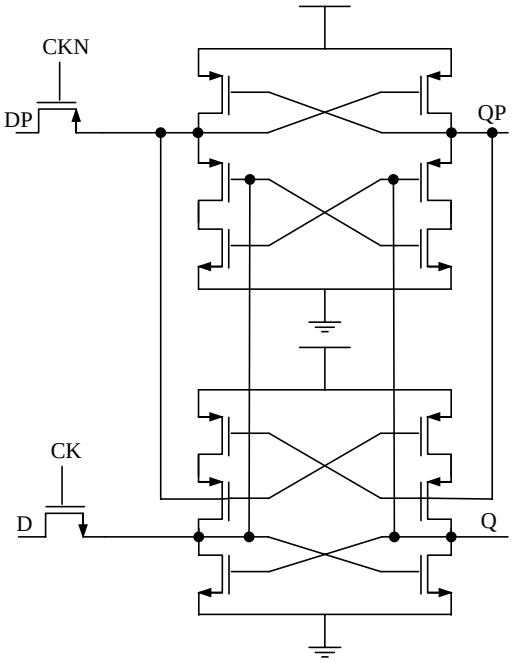

Figure 4.12: *Improved SEU immune RAM cell (Whitaker cell) [29].*

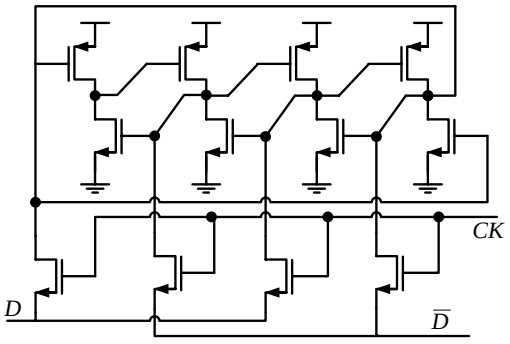

Figure 4.13: *Schematic diagram of DICE [30].*

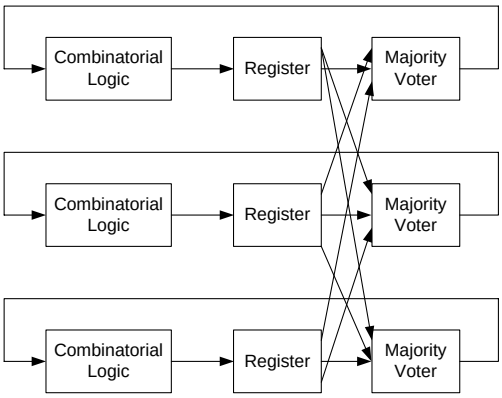

Figure 4.14: *Triple modular redundancy with three independent voters [27].*

compact, simple and hence compatible with the design of high performance circuits in advanced CMOS processes.

Adding redundancy is usually used in high-reliability devices. It is also suitable for radiation tolerance design, although very large space and power are consumed. The information is stored in all of the three different modules, as depicted in figure 4.14. The same combinatorial logic circuits and memories are used in these modules. Voters are also employed to compare the results of the three modules. The major value is considered as the right value. In order to prevent the error induced by the voter itself, the voter is also duplicated. This approach is called as triple modular redundancy (TMR). The redundancy can be also realized in the data encoding or the error detection and correction (EDAC) techniques. The data to be stored is encoded by a complex logic block, in which some redundant bits are added. These bits are used to check or correct the corrupted bits by a complex set of logic operations during decoding. In general, more redundant bits can better protect the original data from the SEU. However, some penalties have to be paid. Since encoding and decoding circuitries become more complex, more area is consumed in EDAC. The speed of processing data is also decreased. Several codes can be used for EDAC, such as Hamming, Reed-Solomon and BCH [31]. Each of them has different detection and correction capabilities and different complexities [27].

4.4.2.2 Hardening against SEL

As mentioned before, latch-up may happen due to the parasitic thyristor structure. Reducing the resistances and the gain of the bipolar transistor are the intuitive methods to prevent current flowing in the loop formed by the two parasitic bipolar transistors. An effective method is to add p+ guard rings surrounding all the regions containing

NMOS transistors, which also benefits TID tolerance [32]. In addition, enlarging the space between NMOS transistors and N-WELL can also decrease the sensitivity to SEL. Guard rings and large space between NMOS transistors and N-WELL are extensively used to harden against SEL, although the silicon area consumed is increased.

4.5 Conclusions

The radiation effects and radiation hardening by design have been presented in this chapter. Total ionizing dose effects and single-event effects are introduced. The radiation hardening techniques are given, which are dedicated to different radiation effects. In order to harden radiation, some efforts should be made in the fabricated technologies, circuit design and layout design. Since the hardening by design can achieve good radiation tolerance with standard process, it is focused on in this chapter. Since adding guard rings around each transistors and enlarge space between NMOS transistors and N-WELL are simple and efficient to against TID effects and SEL, they are utilized in the regulator design.

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Chapter 5

Design of linear regulator for clamping voltage, RegVclamp

Parallel powering with DC-DC converter is proposed to be applied in the CPS, since little change is required for sensor chip. A step down DC-DC converter powers several CPS chips acting as the first conversion stage. Post-regulator is built in each CPS chip used as the second conversion stage to decrease noise and generate the voltage required. The post-regulator must be full on-chip due to the requirements of low material budget and low noise. Thus, the linear regulator is chosen and employed. Though its power efficiency is lower than that of switching power, it provides low noise, low power consumption and low silicon area. The design of a linear regulator named RegVclamp is presented in this chapter, which generates the clamping voltage. Firstly, the linear regulator is briefly introduced. Secondly, the regulator topologies and compensation strategies are presented. Finally, the linear regulator of clamping voltage is proposed including system design consideration and circuit design in detail.

5.1 Introduction

The block level diagram of linear regulator is shown in figure 5.1, which is composed of an error amplifier, a pass element and a feedback network. The error amplifier modulates the gate voltage of the pass transistor according to the difference between reference voltage and feedback voltage. Thus, the output voltage can maintain a constant value because of the regulation loop. The regulator can operate with very small input-output differential voltage [1], so it is also called low dropout (LDO) regulator in some applications. The main performance parameters of LDO are listed as below:

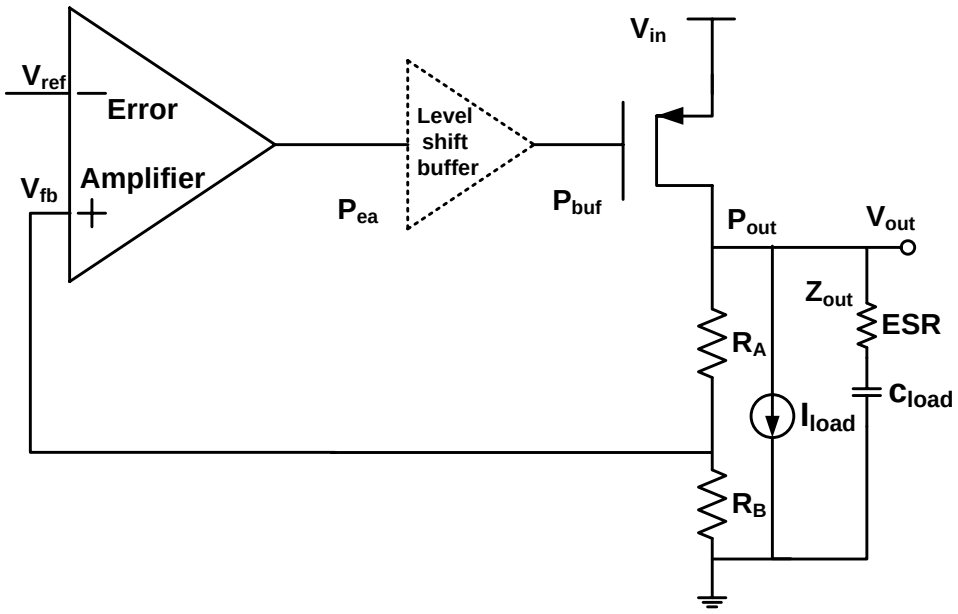


Figure 5.1: *Block diagram of traditional linear regulator with buffer depicting the main poles and zeros.*

- Dropout voltage

  The dropout voltage is the differential between input voltage and output voltage, when the regulator normally works. The regulator may fail when the input voltage is very close to the output voltage. The worst dropout voltage occurs at the maximum output current. The minimum dropout voltage limits the input voltage range in which LDO can output a regulated value. Thus, minimizing dropout voltage is necessary to maximize dynamic range within a given power supply voltage. The LDO with low dropout voltage can be easily reused in the smaller feature-size process, whose power supply voltage is lower. Furthermore, low dropout voltage can also increase the power efficiency.

- Load regulation

  Load regulation is a measure of the LDO's ability to maintain the specified output voltage as the load current changes. It is defined as $\frac{\Delta V_O}{\Delta I_O}$, when the input voltage is constant. The load regulation can be measured by measuring the output voltage variations, when a current pulse acts as the load current variation at the output node. The current pulse can vary from zero to the maximum current of regulation or vice versa. Since it is a steady-state parameter, the load regulation can be also measured with the characteristic curve $(V_O - I_O)$ of the regulator.

Since ΔI_O can be expressed by $\Delta V_O A_{v\_ea} \frac{R_B}{R_A+R_B} g_{mpass}$, the load regulation is rewritten as

$$Loadregulation = \frac{R_A + R_B}{A_{v\_ea} R_B g_{mpass}} = \frac{1}{A_{v-loop} g_{mpass}} \tag{5.1}$$

where A_{v_ea} is the open-loop gain of the error amplifier, A_{v-loop} is the loop gain of the LDO, g_{mpass} is the transconductance of the pass transistor [2] [3]. High load regulation can be achieved by a high loop gain or employing an output transistor with large W/L ratio.

- Line regulation

  Line regulation is a measure of the LDO's ability to maintain the specified output voltage as the input voltage changes. It is defined as $\frac{\Delta V_O}{\Delta V_I}$, when the load current is constant. The line regulation can be measured by measuring the output voltage variations, when a voltage pulse acts as input voltage variation at the input node. The worst line regulation occurs at the maximum load current, like the dropout voltage. Since it is a steady-state parameter, the line regulation can be also measured with the characteristic curve $(V_O - V_I)$ of the regulator. In terms of the feedback loop, the line regulation can be rewritten as

$$Lineregulation = \frac{1}{g_{mpass} A_{v-loop} (R_{ds} + R_L)} \tag{5.2}$$

  where R_{ds} is the drain-source resistance of the pass transistor and R_L is the load resistance [2]. Like load regulation, improving loop-gain can get a better line regulation.

- Efficiency

  The efficiency of a LDO is defined by

$$Efficiency_{power} = \frac{V_o I_o}{V_i [I_o + I_q]} 100\%, \tag{5.3}$$

  where I_q is the quiescent current assuring that the LDO works at right operation point. The efficiency is a parameter evaluating the ratio of the useful power and the total power. It is limited by the quiescent current and ratio of output voltage and input voltage. Thus, lower dropout voltage means higher efficiency. The current efficiency is usually used to represent the total efficiency, when the dropout voltage is very small. The quiescent current must be very small in order to improve efficiency and to decrease the power consumed by LDO itself.

- Power supply rejection (PSR)

  Power supply rejection, also known as ripple rejection, is the measure of LDO's ability to maintain a clean output voltage when there are some ripples in the power supply voltage (input voltage for LDO). PSR is defined by

$$PSR = \frac{V_{o,ripple}}{V_{i,ripple}}. \tag{5.4}$$

  The PSR can be expressed by line regulation without taking into account the frequency, according to 5.4. In general, high PSR can be easily achieved at low frequency, since the open-loop gain of error amplifier is high at low frequency and all the parasitic capacitors are negligible. It may decrease at high frequency. However, the PSR is very important at high frequency when its power comes from a switching power [4]. Increasing the bandwidth or applying cascade regulators can improve the PSR. The low equivalent series resistance (ESR) is also required for high PSR performance at high frequency [5].

All these performance parameters are expected to be good by designers. However, they conflict with each other and affect the other circuit parameters, such as die area, power consumption, output noise and so on. A large size output transistor can improve the load regulation and decrease the dropout voltage but the PSR is degraded at high frequency. The quiescent current and die area are also increased. Therefore, it is essential to analyze the trade-off among these parameters in the regulator design, according to the specified requirements.

5.2 The regulator topologies

The stability is an important design issue, since the regulator can be considered as a two-stage operation amplifier. In general, there are two poles and one zero in the traditional regulator, as shown in figure 5.1. The output pole P_{out} is relevant to the output capacitor and load current, which is located at the output node of the regulator. The other pole, P_{eaout}, is induced by the high impedance of the error amplifier and the input capacitor of the output transistor. They are usually close to each other, which may lead to the instability. Thus, a level shift buffer is inserted to separate the error amplifier and the output transistor. It provides small capacitance and low impedance for the former stage and the latter stage, respectively. Thus, the pole P_{eaout} is divided into two poles, which are located at high frequency. The zero Z_{out} is relevant to the electrical

series resistance or the equivalent series resistance (ESR) of the load capacitance. The Z_{out} may cancel with P_{out} so the regulator can be stable. It should be noted that this zero disappears if no ESR is contributed by the load capacitor. Several topologies and frequency compensation approaches have been reported in order to guarantee the stability and simultaneously achieve good performances, such as line regulation, load regulation, noise, power consumption and so on.

5.2.1 Frequency compensation based on current buffer

Miller compensation is usually utilized to compensate regulator, especially in the two-stage regulator. However, the right half-plane (RHP) zero degrades the phase margin, which is due to the forward path through the Miller capacitor to the output. In order to break the forward path and cancel the RHP zero or shift it to the left half-plane (LHP), the nulling resistor, voltage buffer or current buffer is connected with the Miller capacitor in series. Nevertheless, the output swing of error amplifier is reduced by the voltage buffer. The frequency compensation with nulling resistor is effected by the process fluctuation. Moreover, both achieved a limited gain-bandwidth production and provide a poor power supply reject ratio (PSRR) at high frequency [6]. Compared with the nulling resistor and voltage buffer approaches, the compensation with current buffer is the best choice and it successfully overcomes these drawbacks [7].

The current buffer can be implemented by a common-gate amplifier (shown in figure 5.2) or current mirror. Thus, it can be used in the fold-cascode amplifier without extra current for frequency compensation. The dominant pole is given by

$$P_{dominant} \approx -\frac{1}{r_{o2}C_L + Bg_{m2}r_{o1}r_{o2}C_C}. \tag{5.5}$$

where r_{o1} and r_{o2} are the output resistances of error amplifier and output stage, respectively, g_{m2} is the transconductance of the output stage, B is the current gain of the current buffer and C_C is the compensation capacitance [7]. The dominant pole is relevant to the Miller capacitor C_C, of which the value required is expressed by

$$C_C \approx \frac{1}{B}(\sqrt{\frac{g_{m1}}{g_{m2}}C_{o1}C_L(\sqrt{1+\frac{4}{tan\phi}}-1)} - \frac{C_L}{2g_{m2}r_{o1}}), \tag{5.6}$$

where g_{m1} is the transconductance of the error amplifier and ϕ is the expected phase margin. Equation 5.6 indicates that C_C can be decreased by improving current gain B. The compensation capacitor is smaller than the value required in frequency compensations

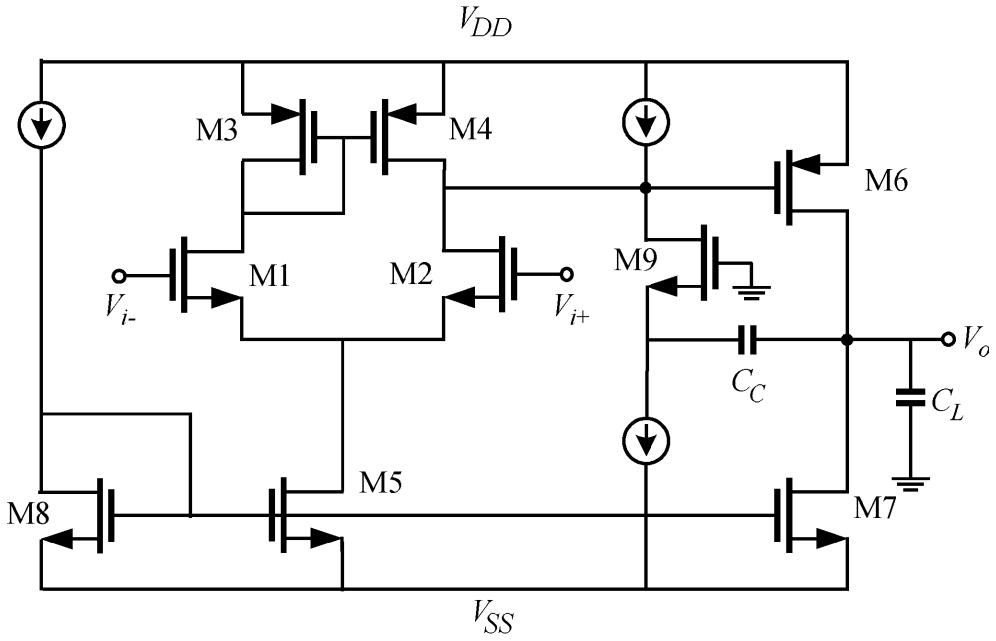


Figure 5.2: *An example of frequency compensation based on employing buffer [8].*

with nulling resistor and voltage buffer [9]. Since C_C provides the forward feedback path in standard Miller compensation, the PSRR at high frequency is low. The feedback path is blocked by the current buffer. Thus, the PSRR performance is improved.

However, the current buffer requires more transistors and bias current. The chip area and power consumption are also high. Larger compensation capacitance are required with a larger load capacitor, since the Miller effect is degraded. Moreover, the output stage amplifies the noise induced by the current buffer. The noise performance is worsened.

5.2.2 Nested-Miller compensation (NMC)

Nested-Miller compensation is usually applied in multi-stage amplifiers to guarantee their stability. It is widely used in the low-voltage applications, since the multi-stage amplifiers are utilized to achieve high gain instead of the cascode amplifier. The NMC is also based on the standard Miller compensation. Two capacitors are employed to form two feedback loops, as shown in figure 5.3. It should be noted that the gains of the second stage and the output stage are positive and negative, respectively in order to obtain the negative feedback loop of the output stage. Rosario Mita et al. presented the reversed nested Miller compensation for the amplifier, in which only the gain of second stage is

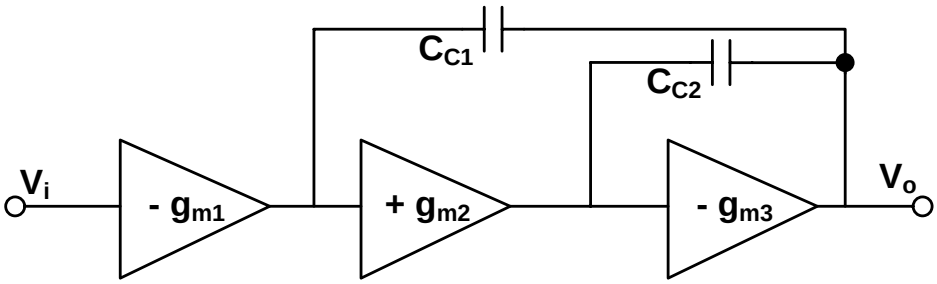


Figure 5.3: *A three-stage amplifier with nested Miller compensation.*

negative [10]. The required compensation capacitor C_{C1} and C_{C2} are given as follows [11],

$$C_{C1} = [tan\phi + \sqrt{tan^2\phi + 2}]\frac{g_{m1}}{g_{m3}}C_L, \tag{5.7}$$

$$C_{C2} = tan\phi\frac{g_{m2}}{g_{m3}}C_L, \tag{5.8}$$

where ϕ is the phase margin, C_L is the load capacitance and g_{mi} is the transconductance of the ith stage amplifier.

Equation 5.7 and 5.8 indicate that the transconductance of output stage must be larger than that of the other two stages in order to decrease the compensation capacitors. Thus, NMC is more suitable for a amplifier with a high transconductance of last stage. Similar to the standard Miller compensation, two zeros are created. One is located in left half-plane. The other one is a right half-plane zero located at a lower frequency. These two zeros can be canceled by nulling resistor, voltage buffer or current buffer connected with the compensation capacitor in series. NMC is simple and easier to be realized. It can also improve the transient response, since the compensation capacitance is smaller, compared to the standard Miller compensation. However, The bandwidth is poor mainly due to the presence of C_{C2}, which is part of capacitive load to the amplifier [12] [13]. Moreover, the application of NMC is limited by the premise of $g_{m3} >> g_{m1}, g_{m2}$. It is also not suitable for the regulator with large load capacitor, since the Miller effect is degraded.

5.2.3 Damping-factor-control frequency compensation

Since poor bandwidth is achieved in nested Miller compensation, damping-factor-control frequency compensation is reported in [14]. The block diagram is shown in figure 5.4. There are two additional building blocks, compared to nested Miller compensation. The damping-factor-control is used to control the damping factor of the nondominant

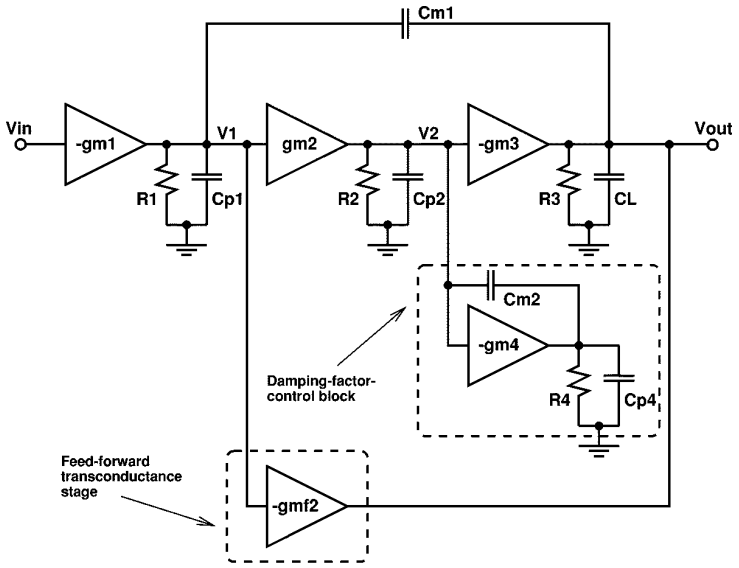


Figure 5.4: *Block diagram of a multi-stage amplifier with damping-factor-control frequency compensation [14].*

complex pole to maintain the amplifier stable. The feed-forward transconductance stage is used to implement a push-pull output stage to improve the slewing performance. The transfer function is given in 5.9 [14].

$$A_v(s) = \frac{A_{dc}(1 + s\frac{C_{p2}g_{mf2} - C_{m1}g_{m4}}{g_{m2}g_{m3}+g_{mf2}g_{m4}} - s^2\frac{C_{p2}C_{m1}}{g_{m2}g_{m3}+g_{mf2}g_{m4}})}{(1 + s(C_{m1}g_{m2}g_{m3}R_1R_2R_3))(1 + s\frac{C_Lg_{m4}}{g_{m2}g_{m3}+g_{mf2}g_{m4}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{m3}+g_{mf2}g_{m4}})}, \quad (5.9)$$

where R_i and C_{pi} are the output resistance and capacitance of the ith stage amplifier, respectively and g_{mi} is the transconductance of the ith stage amplifier. The dominant pole is $(C_{m1}g_{m2}g_{m3}R_1R_2R_3)^{-1}$, according to 5.9. The damping factor and the location of the complex pole is controlled by g_{m4}. The gain bandwidth product is controlled by C_{m1}. Moreover, the effect of the compensation capacitor C_{m2} is canceled in the transfer function of the amplifier as long as $C_{m2} >> C_{p2}$. C_{m2} should be set to equal C_{m1}, if C_{m1} is small. Otherwise, $C_{m1} > C_{m2} > C_{p2}$ should be set [14]. The required g_{m4} and C_{m1} are given in 5.10 and 5.11, respectively.

$$g_{m4} = g_{mf2}(\frac{C_{p2}}{C_L})[1 + \sqrt{1 + 2(\frac{C_L}{C_{p2}})(\frac{g_{m2}g_{m3}}{g_{mf2}^2})}] \quad (5.10)$$

$$C_{m1} = \frac{4}{1 + \sqrt{1 + 2\frac{C_L}{C_{p2}}\frac{g_{m2}g_{m3}}{g_{mf2}^2}}} \frac{g_{m1}}{g_{mf2}} C_L \tag{5.11}$$

C_{m1} is decreased, compared to nested Miller compensation. A low dropout regulator based on damping-factor-control is presented in [15]. Moreover, a capacitor is connected with feedback resistor in parallel in order to create a zero, which is used for improving stability. This low dropout regulator provides high stability even in capacitor-free operation. However, the reference voltage is required to be much smaller than output voltage and the minimum load current is limited to maintain stability.

5.2.4 Buffer impedance attenuation

The regulator stability is difficult to be maintained in a large range of the load current, since the output pole varies with the load current. As previously mentioned, a buffer can be employed between the error amplifier and the pass transistor. Thus, the pole, which is relevant to the output resistance of error amplifier and the gate capacitor of pass transistor, is separated into two high frequency poles. Good stability is achieved at low load current. However, the bandwidth of regulator is extended at high load current. The pole located at the output of the buffer may be under the unity-gain frequency, since the pass transistor is usually large to be able to source high load current while achieving low dropout voltage [16]. In order to address this problem, the output resistance of the buffer is proposed to be decreased at high load current with little increase of quiescent current.

Mohammad Al-Shyoukh et al. proposed a low-dropout regulator with buffer impedance attenuation [17]. The output resistance of the intermediate buffer is reduced through dynamically-biased shunt feedback. As a consequence, the pole at the gate of the pass transistor is pushed far beyond the unity-gain frequency under the entire load current range. The buffer proposed in [17] is illustrated in figure 5.5. In order to decrease the quiescent current and improve the current efficiency, the bipolar transistor Q_{20} is utilized due to its large current gain. The bias current of Q_{20} and M_{24} is adapted by the load current. The output resistance of this buffer is given by

$$r_{ob} = \frac{1}{g_{m21}(1 + \beta) + g_{m24}}, \tag{5.12}$$

where β is the current gain of Q_{20} and g_{m21} and g_{m24} are the transconductance of the transistor M_{21} and M_{24}, respectively. According to 5.12, the output resistance is significantly decreased by β and g_{m24} at high load current. The pole located at the gate of

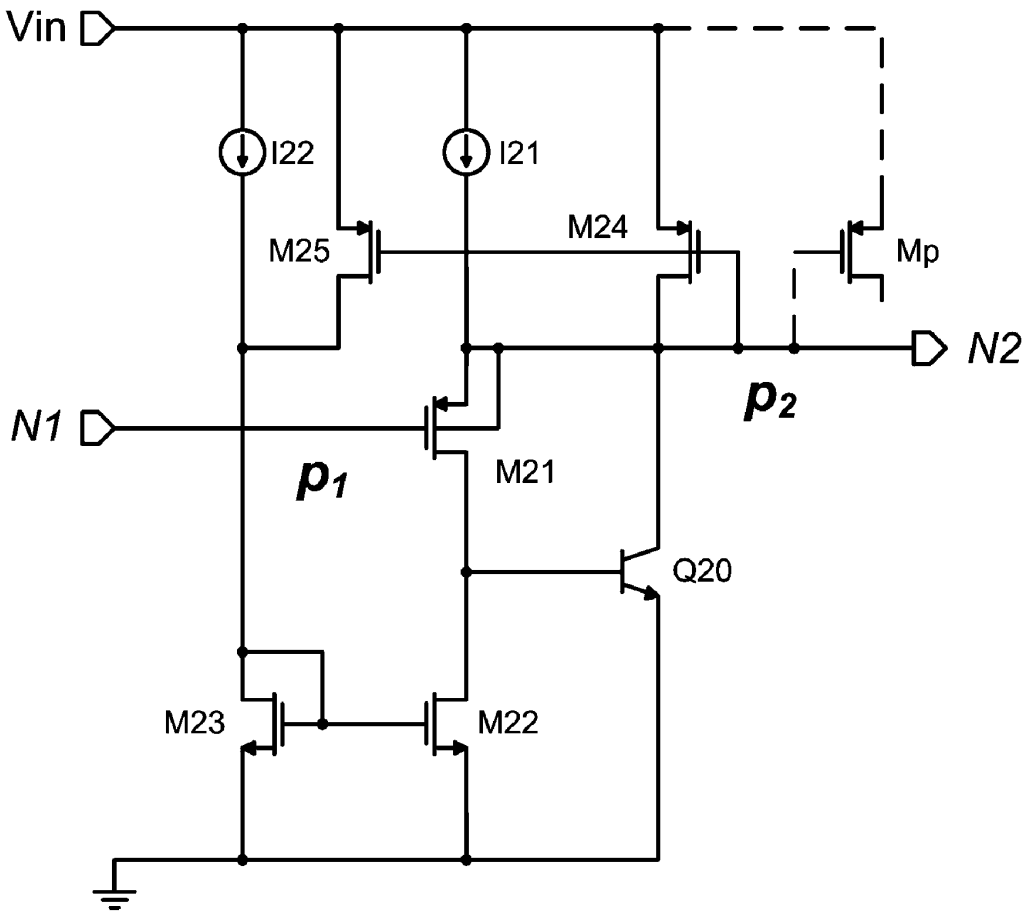


Figure 5.5: *Buffer with dynamically-biased shunt feedback [17].*

pass transistor is negligible for the stability, since it is pushed to very high frequency. It should be noted that the buffer impedance attenuation only effects the pole at the gate of the pass transistor. However, there are still two poles located at the low frequency. Thus, another compensation strategy should be employed to achieve good stability in the full range of the load current, such as the frequency compensation based on the current buffer.

5.2.5 Pole-zero cancelation

The effects of pole and zero can cancel with each other in frequency domain, since zero provides positive phase shift while pole provides negative phase shift. Zero is usually utilized to compensate the phase response. This method is called as pole-zero cancelation. A very common approach refers to the ESR of an externally connected capacitance. An

zero is formed by this capacitance and its ESR, which is given as

$$Z_{ESR} = \frac{1}{r_{ESR} C_{ext}}, \tag{5.13}$$

where C_{ext} is the externally connected capacitance and r_{ESR} is its ESR. The zero Z_{ESR} can cancel with the output pole, especially for a large capacitance. It is a simple compensation approach, which is widely used in commercial linear regulators. However, the ESR value varies with temperature, DC bias voltage and operating frequency. The compensation based on ESR may not guarantee the stability for all temperature and voltage. The output undershoot and output overshoot are very large during massive load-current step changes when the ESR is used to generate zero [17]. Moreover, an external capacitance is impossible for full on-chip regulator. In order to address these problems, zero is generated by the regulator itself. Since the poles and zeros are relevant to the combination of capacitors and resistors, a simple way is to connect a resistor and capacitor in series, named as series RC network. However, the stability may be degraded when the load current varies in a large range, since the output pole varies with load current. The zero used for compensation can not cancel with the output pole if its position is fixed. A pole-zero tracking frequency compensation is proposed in [18] [19]. A MOS transistor is designed to work in linear region to operate as a resistor, the value of which depends on the gate-source voltage. Thus, zero can move with the output pole by the feedback. The good phase margin can be achieved in a large range of load current.

It should be noted that each topology mentioned above has its own limitations. In order to simultaneously satisfy different performance parameters, some compensation strategies are employed in a regulator at the same time. For example, the regulator reported in [20] is based on nested Miller compensation and current buffer.

5.3 Linear regulator for clamping voltage, RegVclamp

Based on the topologies mentioned above, RegVclamp is designed to provide the clamping voltage in CMOS pixel sensors. Since clamping voltage is utilized as a reference, the regulator RegVclamp can be also called as reference generator. The pole-zero cancelation is utilized to maintain the stability. All the compensation components are integrated on-chip.

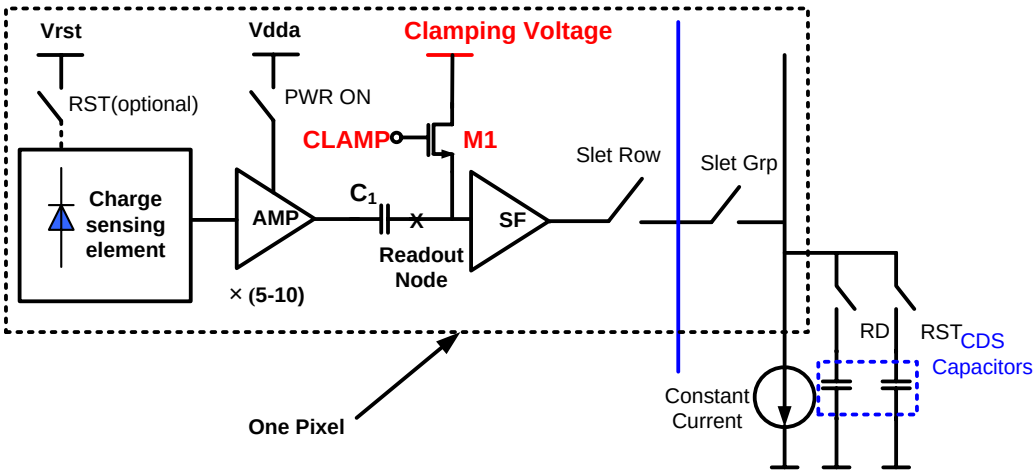


Figure 5.6: *Pixel topology [21].*

5.3.1 Design considerations at system level

In their most recent versions, CMOS pixel sensors are composed of pixel array, row selector, column-level discriminators, zero suppression, regulators and so forth. The simplified pixel topology is shown in figure 5.6 [21], as mentioned in Chapter 2. The charge sensing elements in pixels collect the charges induced by the ionizing particles. These charges are converted to voltage signal of about a few millivolts by the diode capacitance [22]. The gain of the following preamplifier is only 5 to 10, which is limited by the pixel size. Consequently, the signal is very sensitive to the noise. To efficiently suppress the pixel-to-pixel and column-to-column fixed-pattern-noise (FPN), the CDS operation is implemented at the pixel level and at the column level [23]. The value of the capacitor C_1 is chosen large enough (about 100 fF, which is about 10 times more than the collecting electrode capacitance) to decrease the KT/C noise during the clamping operation. However, the noise of clamping voltage is directly injected into the readout node during the reset (CLAMP) phase. Thus, the CDS operation can not completely eliminate the influence of this noise and the clamping voltage must be sufficiently clean to prevent signal corruption due to the noise. Furthermore, the clamping voltage must be constant to guarantee the correct CDS operation.

Since the clamping voltage is connected to every pixel in CPS, its load capacitance drastically increases with the pixel array size due to the parasite. The parasitic capacitance is composed of the internal capacitance in pixel and the wire capacitance, which is the main parasitic source. According to the parasitic extraction from layout, the total capacitance is about 0.5 nF in a 576 × 136 pixel array. It increases to about 5 nF when the pixel array

Table 5.1: *Design specifications of RegVclamp.*

Item	Specification
Full on-chip	Yes
Input voltage (V)	$2.7 \sim 3.3$
Output voltage (V)	$2 \sim 2.3$ (adjusted by JTAG registers)
Load capacitance (nF)	$0.5 \sim 5$
PSRR	$\leqslant$ -50 dB
Power dissipation	$\leqslant$ 1 mW

is 928 × 960. The on-chip regulator to be designed should fulfill the stability requirements in presence of such a large load capacitance. Moreover, the regulator must work in a large range of load capacitances (0.5 nF $\sim$ 5 nF) in order to be reused in CPS chips with different pixel array size.

Compared with the large capacitive load, the resistive load of clamping voltage is almost zero. The DC load current is not required because there is no DC path to ground, as shown in figure 5.6. Since the pixel array is read out in rolling shutter mode, a dynamic current of a few hundred micro-amperes is sufficient to charge the internal capacitors in one row. In addition, the clamping voltage is usually at least a threshold voltage (about 0.6 V) less than the power-supply voltage (Vdda) so that the following source follower can work in saturated region and the switch transistor M1 can work in linear (triode) region to behave like an ideal switch. It is possible to employ a relatively small output transistor due to the small load current and low output voltage.

Finally, the regulator is required to be compact and low-power due to the limited die area of non-sensing elements and the air cooling system, respectively. Since the clamping voltage is very critical to the CDS, its value must be adjustable to compensate the influence of process parameter fluctuations. The design specifications are summarized in Table 5.1.

The block diagram of the proposed circuit is illustrated in figure 5.7. The regulator is composed of three stages: the error amplifier, the level shift buffer and the output stage. A source follower (SF) operated as level-shift buffer, and a series RC network are inserted to improve the phase margin. The buffer also enhances the transient response. Since the output voltage is directly determined by the feedback resistor, resistor R_A is adjustable to compensate the output voltage values for process parameter fluctuations. The register RV<3:0> can be accessed by the joint test action group (JTAG) standard interface mentioned in Chapter 2. The stability analysis will be given in the following subsections. The noise analysis and power supply rejection ratio will be also discussed.

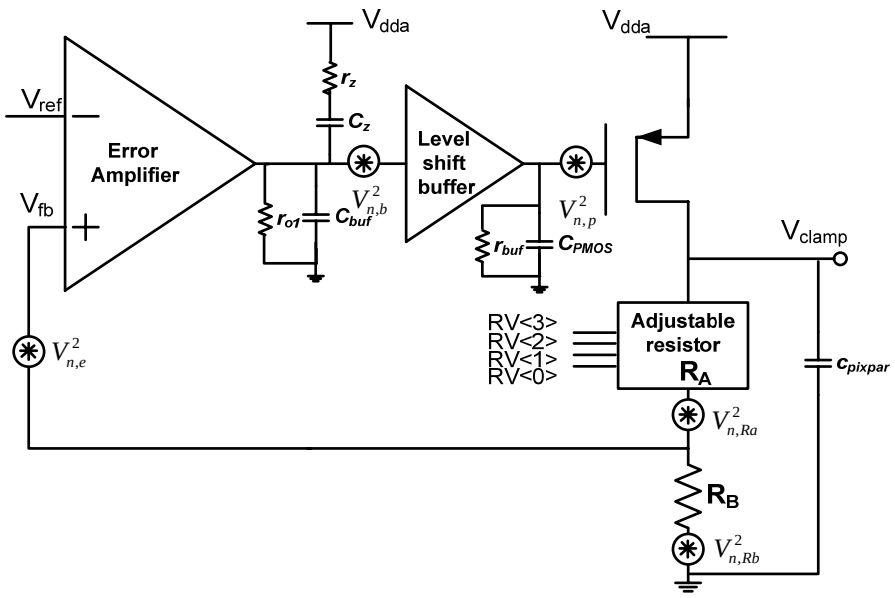


Figure 5.7: *The block diagram of the proposed regulator depicting the equivalent resistors and capacitors of each stage and the main noise sources.*

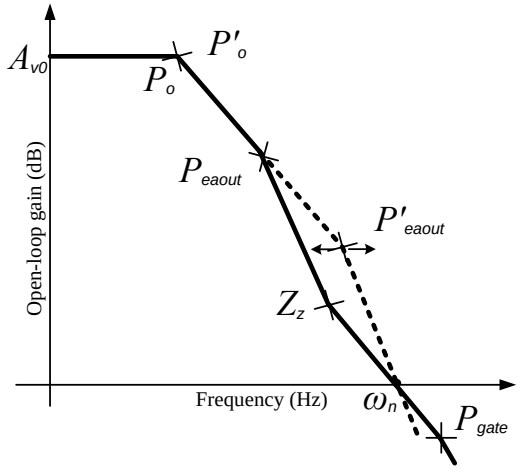


Figure 5.8: *The pole-zero location of the regulator before (dashed line) and after (solid line) compensation.*

5.3.1.1 Stability analysis

In the traditional two-stage regulator, there are two dominant poles, as shown in figure 5.8. One pole, P'_o, is relevant to the output node of the regulator. The other pole, P'_{eaout}, is induced by the high impedance of the error amplifier and the input capacitor of the output transistor. They are usually close to each other, which will lead to the instability. Thus, a level shift buffer is inserted to separate the error amplifier and the output transistor. It provides small capacitance and low impedance for the former stage and the latter stage, respectively. The pole P'_{eaout} is divided into two poles, P_{eaout} and P_{gate}, as depicted in figure 5.8. According to figure 5.7, the main poles and zeros are simply calculated as

$$Z_z = \frac{1}{r_z C_z} \tag{5.14}$$

$$P_o = \frac{1}{R_{out} C_{pixpar}} \tag{5.15}$$

$$P_{eaout} = \frac{1}{r_{o1}(C_z + C_{buf}) + r_z C_z} \tag{5.16}$$

$$P_{gate} = \frac{1}{r_{buf} C_{PMOS}} \tag{5.17}$$

where R_{out}, r_{o1} and r_{buf} are the output resistances of the output stage, error amplifier and buffer, respectively. C_{pixpar} is the total parasitic capacitance connected to the clamping voltage. C_{PMOS} is the gate capacitance of the output transistor. The pole P_{gate} will be pushed to high frequency due to the small value of r_{buf}. Since C_{buf} is negligible, the effect of pole P_{eaout} can be almost canceled by that of zero Z_z with a proper compensation capacitance and resistance, according to equation 5.14 and equation 5.16. Therefore, P_o is the dominant pole under the unity-gain frequency (ω_n) as in the "before compensation" case. The bandwidth is not decreased by the compensation elements. Despite that P_o will vary with the adjustable resistor R_A, the regulator is stable. The location variation of P_o is negligible since R_A is adjusted in a constrained range from 8 kΩ to 10.8 kΩ.

Assuming that the P_{gate} is beyond 10 times the unit-gain frequency, the phase margin (PM) is given by

$$PM = 180^o - tan^{-1}\frac{\omega_n}{P_o} - tan^{-1}\frac{\omega_n}{P_{eaout}} + tan^{-1}\frac{\omega_n}{Z_z} \tag{5.18}$$

Substituting the poles and zeros with equation 5.14, 5.15 and 5.16, the compensation

capacitance and resistance can be drawn as below

$$C_z r_z \approx tan(PM)\frac{R_{out}C_{pixpar}}{A_{v0}} \tag{5.19}$$

where A_{v0} is the DC gain product of the three stages. The compensation capacitance is significantly reduced by the gain and the compensation resistor. It indicates that the high gain error amplifier can achieve a smaller area.

5.3.1.2 Noise analysis and power supply rejection ratio (PSRR)

The main noise sources are shown in figure 5.7. Assuming that the reference voltage is noiseless, the output noise is simply given by

$$V_{n,out}^2 = [(V_{n,b}^2 + \frac{4kT}{r_z C_z^2 \omega^2})/A_{ea}^2 + \frac{V_{n,p}^2}{A_{ea}^2 A_b^2} + V_{n,e}^2](1 + \frac{R_A}{R_B})^2 + V_{n,Rb}^2\frac{R_A^2}{R_B^2} + V_{n,Ra}^2, \tag{5.20}$$

where $V_{n,b}$, $V_{n,p}$ and $V_{n,e}$ represent the input-referred noise of error amplifier, buffer and output transistor, respectively. A_{ea} and A_b are the gain of the error amplifier and the buffer, respectively. $V_{n,Ra}$ represents the noise of the adjustable resistor including the noise induced by the decoder. $V_{n,Rb}$ is the noise of R_B.

Since the gain of error amplifier is very high, the noise of the compensation circuit and output transistor can be ignored. The main noise comes from the feedback resistors and the error amplifier. Thus, decreasing their noise is an effective way to minimize the total noise [24]. It is necessary to employ small feedback resistors to meet the low noise requirement, which needs trade-off with the power consumption. The PSRR is an important performance for the regulator due to the power supply ripple. The PSRR value at the low frequency can be improved by increasing the gain of the error amplifier. However, it does not work at the high frequency. One solution is to improve the unit-gain frequency [25]. Since the compensation scheme does not decrease the bandwidth, the proposed circuit can achieve high PSRR in the full frequency range with a high gain error amplifier.

5.3.2 The proposed reference generator RegVclamp

The schematic diagram of the proposed RegVclamp is shown in figure 5.9. The error amplifier is implemented by a differential-to-single-ended gain stage. The reference voltage V_{ref} comes from a low noise bandgap, which is an IP core provided by foundry. As previously mentioned, the error amplifier is designed to be high-gain and low-noise. The

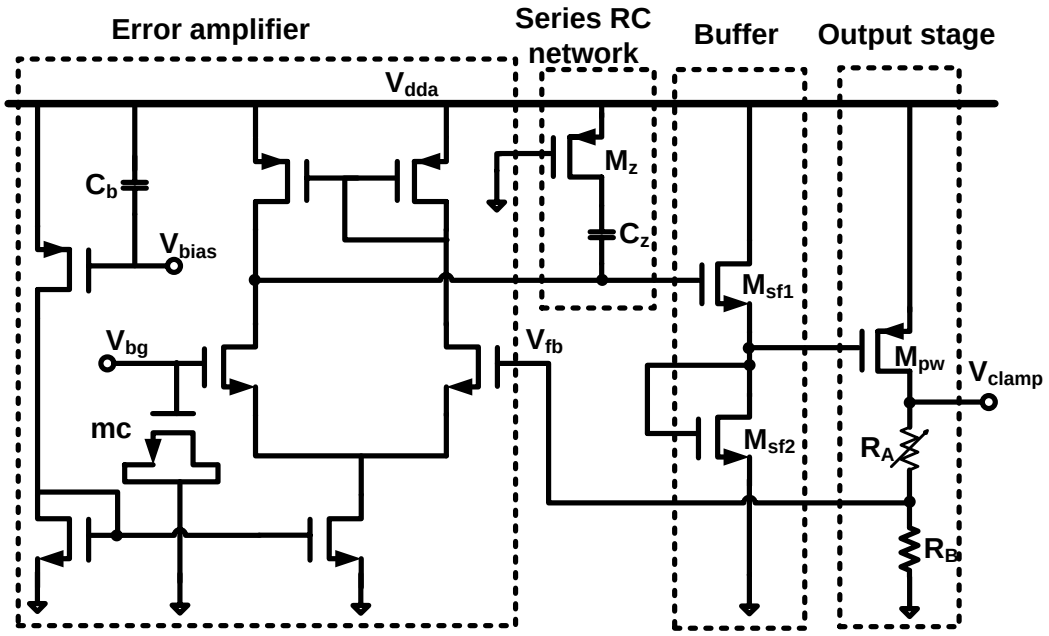


Figure 5.9: *Schematic diagram of the RegVclamp.*

physical sizes of the transistors, especially the differential pair, should be large enough to decrease the flicker noise [26]. Furthermore, the transconductance of the transistors needs to be high in order to keep low thermal noise and achieve high gain. As a result, the transistors are lengthened to satisfy both noise and gain requirements. Though the flicker noise of PMOS is less than that of NMOS, a NMOS differential pair is employed in this design due to the trade off between gain and noise. In order to filter the noise from reference and bias voltage, two bypass capacitors (C_b and mc) are employed.

The second stage is composed of a series RC network and a source follower with diode-connected load. The resistor is implemented by a PMOS transistor operating in linear region, the gate of which is connected to the ground. Since this transistor provides the AC path to the ground by its parasitic capacitance, it can prevent the high-frequency noise from $Vdda$ coupling into the critical nodes via C_z.

The output stage consists of the output transistor and the feedback resistor network. Since the load current is very low and the gate-source voltage of the output transistor can be raised by the source follower, the dimension of the output transistor is significantly decreased. The feedback resistor R_A is realized by the digitally adjustable resistor shown in figure 5.10. Thus, the clamping voltage is adjustable and independent of the process. Assuming the offset voltage of the error amplifier is negligible, the value of V_{clamp} is given

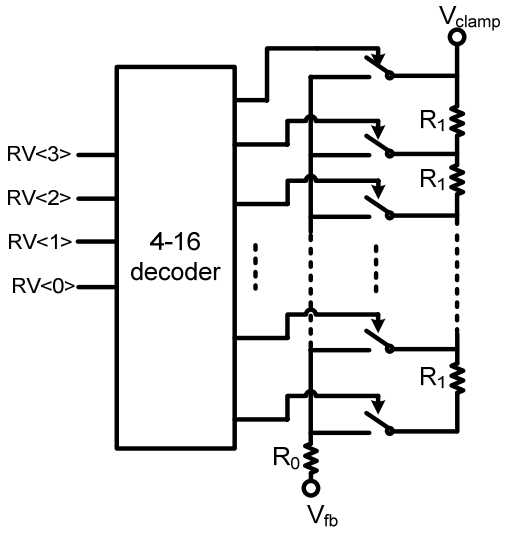


Figure 5.10: *The digitally adjustable resistor R_A.*

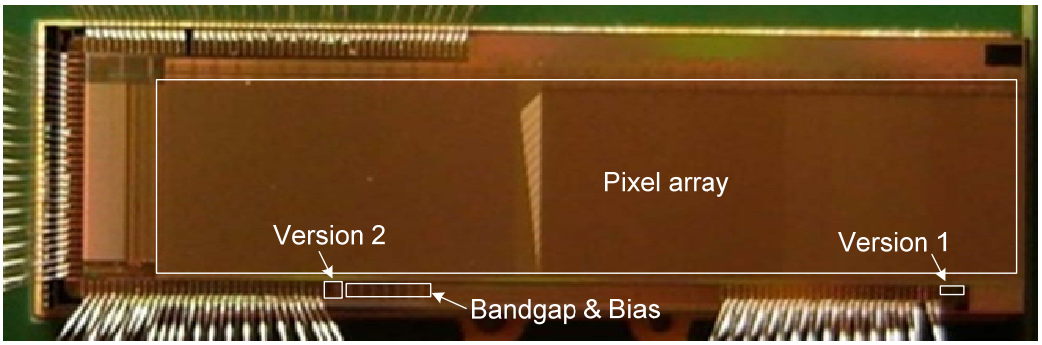


Figure 5.11: *Microphotograph of the MIMOSA22-HRE chip.*

as

$$V_{clamp} = V_{ref}[1 + \frac{R_0 + (2^{f(RV<3:0>)} - 1)R_1}{R_B}], \tag{5.21}$$

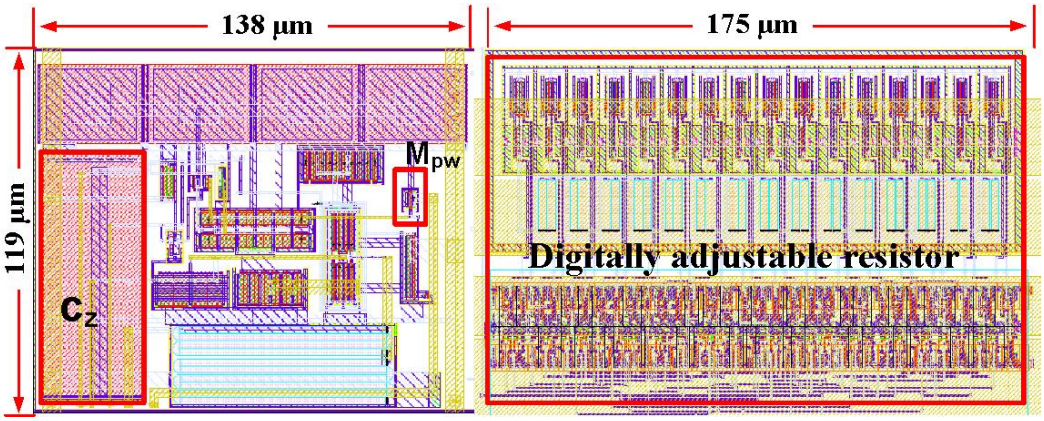
where V_{ref} is the bandgap reference, R_0 and R_1 are two poly resistors of different values, R_1 is the minimum adjustable resistor of a few hundred ohms, $RV < 3 : 0 >$ is a 4-bit register accessed by JTAG. The resolution of clamping voltage is 20 mV. Furthermore, only one switch is closed for each state of the decoder so as to degrade the influence of the switch on-resistance.

5.3.3 Measurement results and discussions

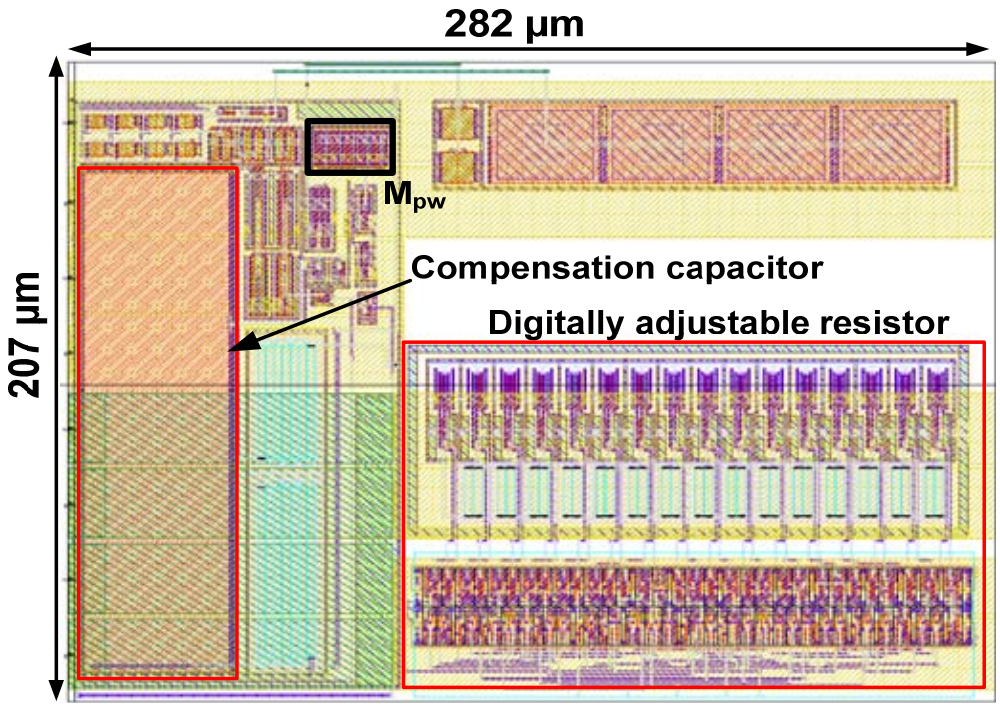
The proposed RegVclamp has been integrated as an optional circuit in MIMOSA22AHR, fabricated in a commercial standard 0.35-μm CMOS process. The MIMOSA22AHR chip is one of the prototypes for the preparation of the ULTIMATE chip. Its microphotograph is shown in figure 5.11. In the pixel array, 16 sub-arrays with different pixel architectures are contained. In order to compare the performances and choose a better design, two versions of the reference generators are designed and fabricated. Version 1 is the proposed circuit RegVclamp. Version 2 is a traditional two-stage regulator based on current buffer. They share the same bandgap voltage, bias voltage but employ separated adjustable resistors. The error amplifiers and the adjustable resistors are the same in these two circuits. Each circuit can be disabled with different signals, which allows us to separately test them. The layouts of version 1 and version 2 are shown in figure 5.12. In order to be radiation tolerance, all the transistors are surrounded by guard ring. The silicon area of version 1 is 327 μm $\times$ 119 μm, while that of version 2 is 282 μm $\times$ 207 μm. About 33% silicon area is saved. The compensation capacitor used in version 1 is half of the compensation capacitor in version 2. Moreover, the size of output PMOS transistor is significantly decreased by the source follower. The digitally adjustable resistor occupies large area due to the process limitation and the small on-resistance of the switches.

The simulated phase margin of the proposed regulator is shown in figure 5.13. The compensation capacitance C_z is realized as a poly-poly capacitor of 2 pF, while the transistor M_z is realized with an aspect ratio W/L of 1/20. The simulation results demonstrate that the phase margin is higher than 46^o with the capacitive load ranging from 500 pF to 10 nF in worse power (WP), nominal (NOM) and worse speed (WS). The phase margin decreases in worse power corner due to the smaller on-resistance of M_z. Replacing this transistor with a poly-resistor will improve the phase margin in worse power at the cost of die area. Figure 5.14 depicts the PSRR simulated results with load capacitances of 0.5 nF and 10 nF. It is higher than 50 dB at the low frequency. Tough it decreases near 100 kHz, the minimum value is 41.8 dB at 1 MHz in all cases. The proposed scheme is helpful to improve the PSRR at high frequency. It will be better for a larger capacitance.

Circuit performance was also tuned with respect to transient load excursions. Since it takes unacceptable time to simulate the proposed generator with one-row pixels ($\sim$136 cells), only capacitance C_1 (shown in figure 5.6) is extracted from each pixel. This is due to that the most of dynamic current is required to charge/discharge C_1 during the clamping operation. In order to verify in the worst case, the on-resistance of switch ($M1$ in figure 5.6) is set to 0 ohms. Assuming that all the pixels in one row are hit by the



(a)



(b)

Figure 5.12: *Layout of the version 1 (a) and version 2 (b).*

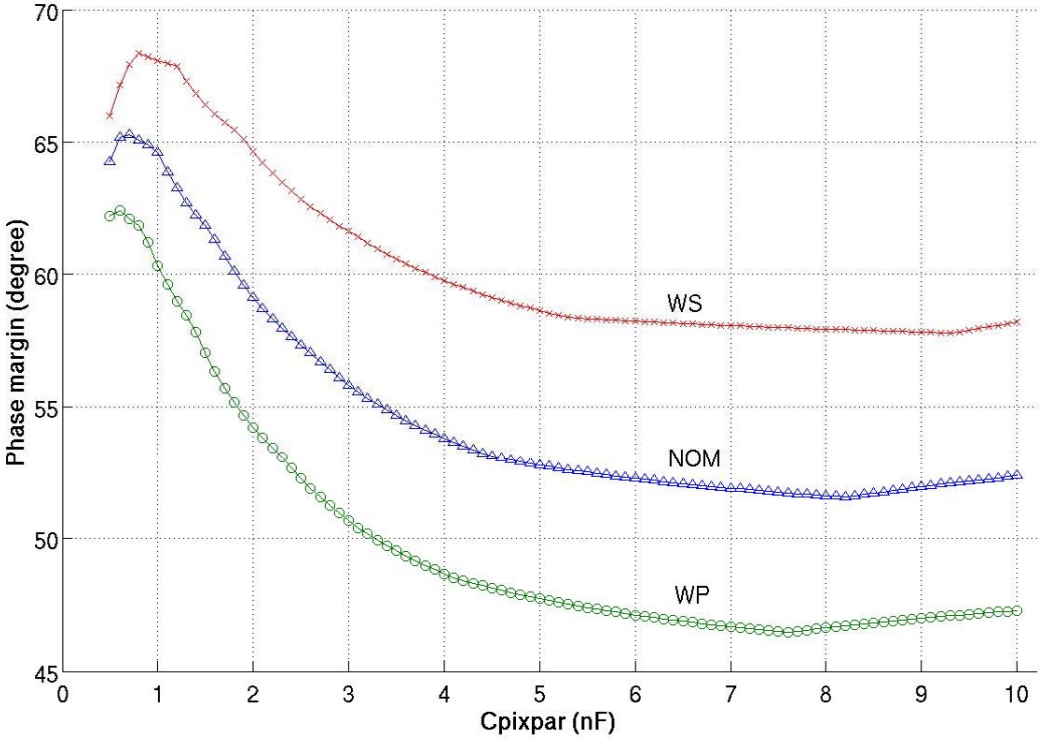


Figure 5.13: *Simulated results of phase margin with respect to the load capacitor.*

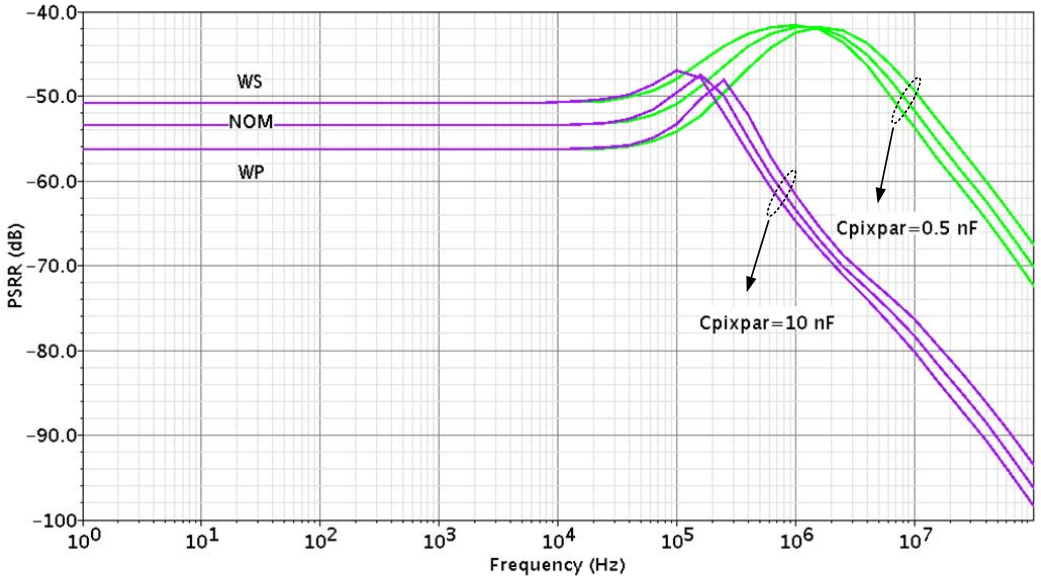


Figure 5.14: *Simulated results of PSRR with capacitance of 0.5 nF and 10 nF.*

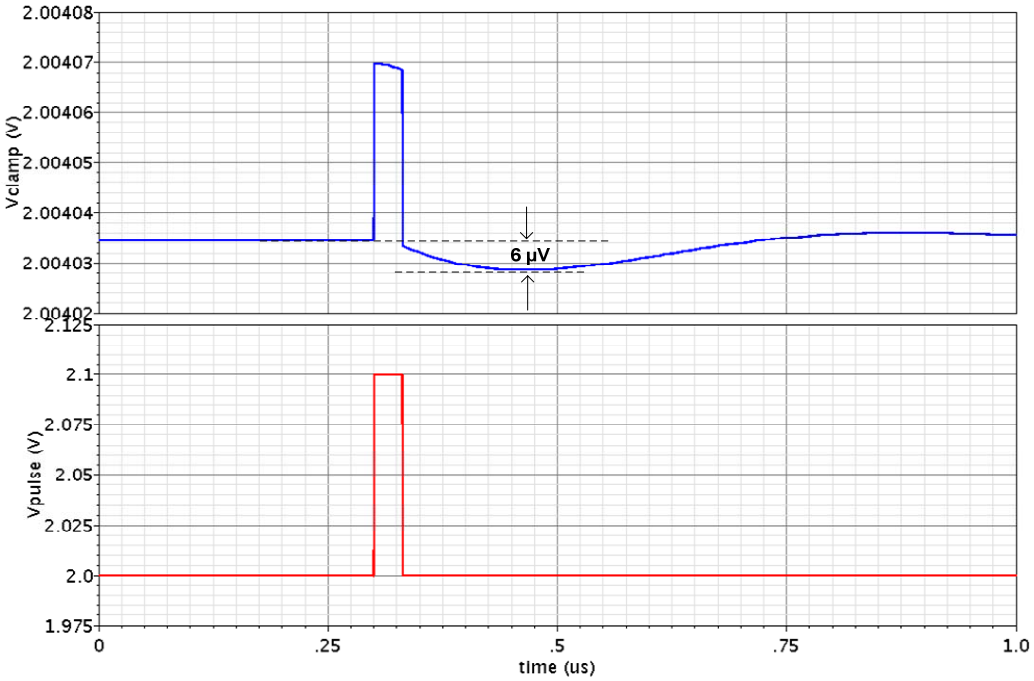
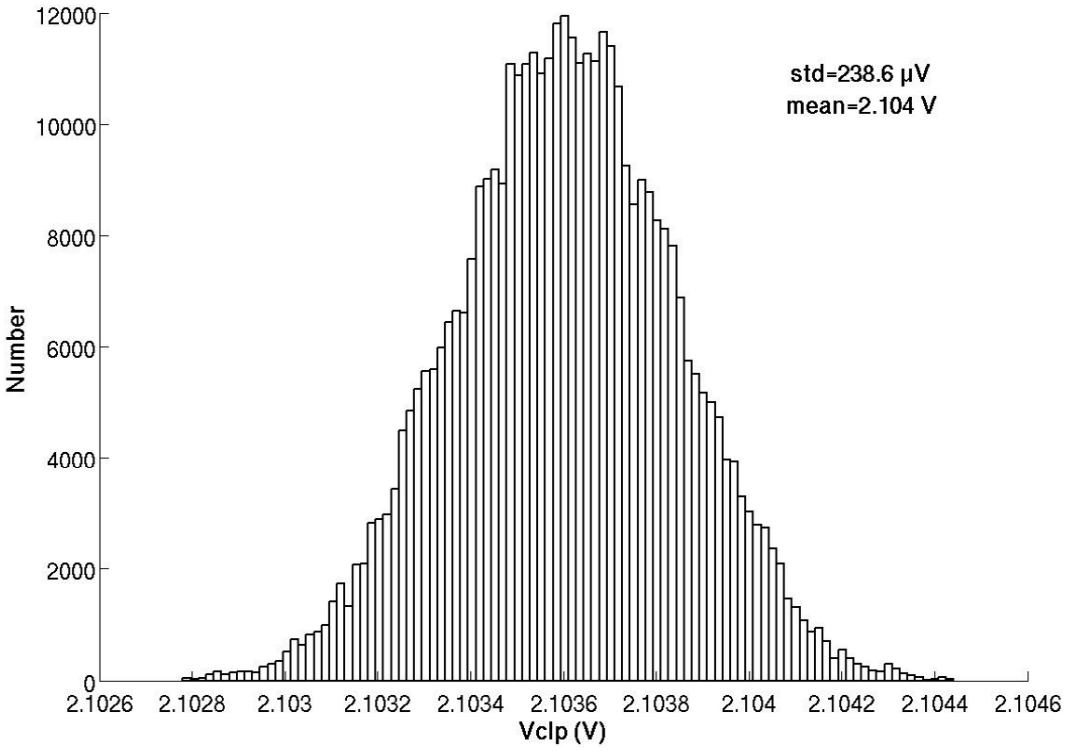


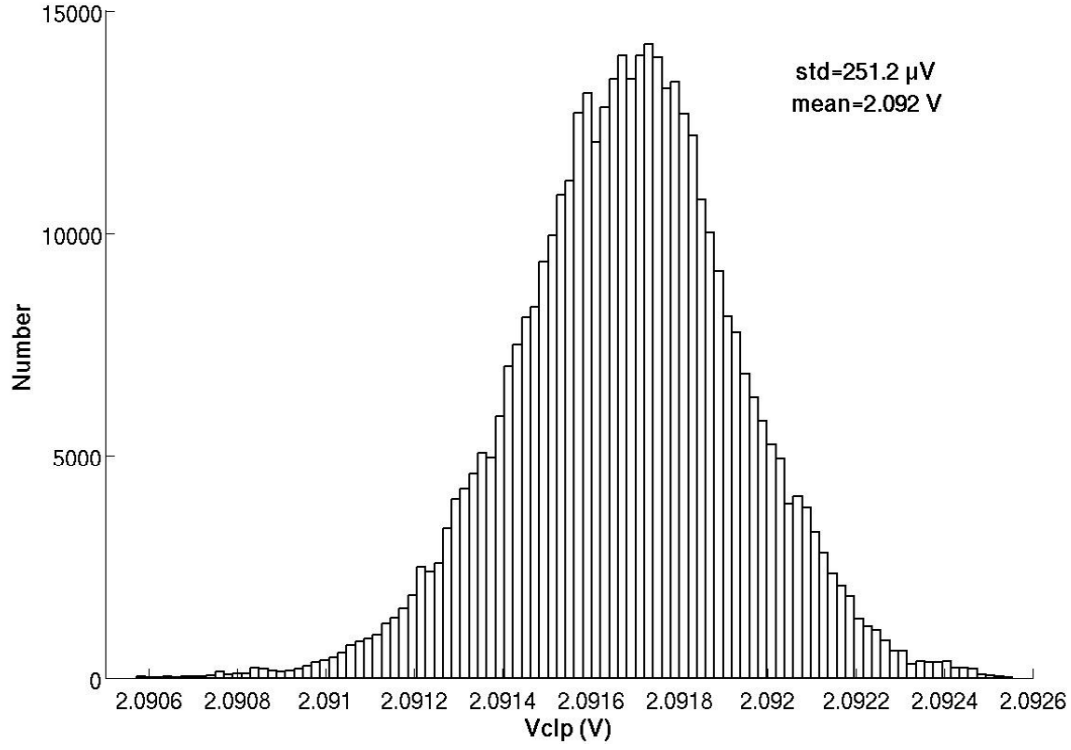
Figure 5.15: *Simulated output voltage during the clamping operation.*

particles, the preamplifier output voltage is modeled as a pulse voltage varying from 2 V to 2.1 V. As a result, 136 C_1s are connected in parallel between this pulse voltage and the generator output in the simulation model. Since the load capacitance of 0.5 nF is always connected with the generator, it is also analyzed. It presents the parasitic capacitance as mentioned in Section 5.3.1. The simulation result is shown in figure 5.15. The maximum variation of the output voltage is about 6 μV. It is less than 10% of the threshold voltage resolution ($\sim$250 μV) of discriminator in the CDS operation, which can be accepted in this design.

In order to verify the noise performances of the generators, both circuits have been connected to the bandgap, the bias circuit and one pixel. They are verified in transient noise analysis, which calculates the output adding the noise to the input. Since the sampling frequency of the pixel array is around 10 MHz, the noise frequency injected is from 1 kHz to 100 MHz. The histograms generated by MATLAB are shown in figure 5.16. The standard deviations (std) of the clamping voltage is 238.6 μV in version 1, while it is 251.2 μV in version 2. The proposed circuit has better noise performance. The output spectral noise density of the circuits is also simulated in the noise analysis. For version 1, the values are 222 nV/$\sqrt{Hz}$ and 74.8 nV/$\sqrt{Hz}$ at 100 Hz and 1 kHz, respectively. For version 2, the values are 1.25 μV/$\sqrt{Hz}$ and 386 nV/$\sqrt{Hz}$ at 100 Hz and 1 kHz,



(a)



(b)

Figure 5.16: *Histograms of the clamping voltage refer to version 1 (a) and version 2 (b)*

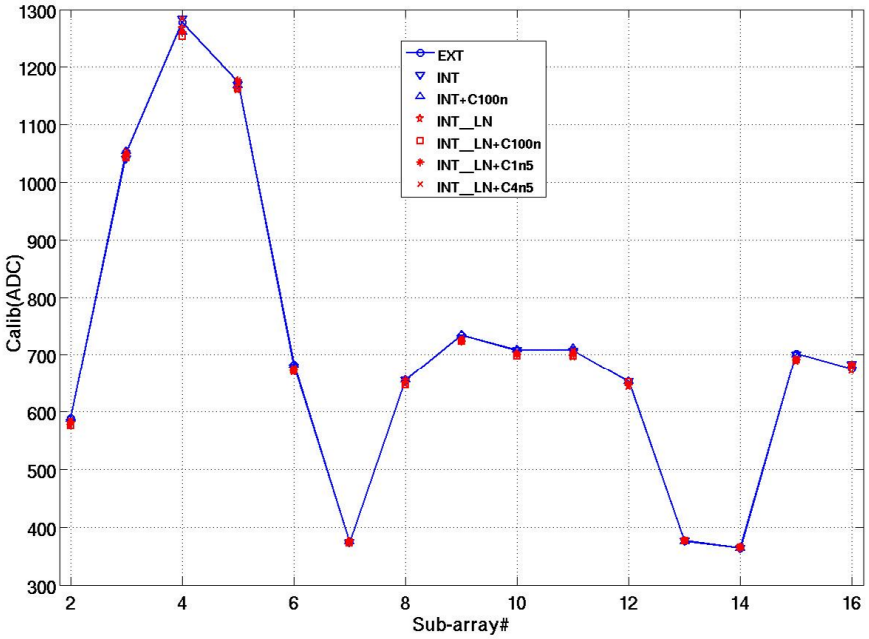


Figure 5.17: *Calibration results with different reference generators and load capacitances.*

respectively. The main noise comes from the current buffer.

The two versions have been measured with CPS test board. The noise induced by the RegVclamp can not be measured directly due to its small value. Thus, it must be extracted from measured results of the whole chip. The read nodes are read out in test mode when there is no particle source. As mentioned in Chapter 2, there are eight selectable analogue output pads in the upside of CPS chips. The pixel matrix is divided into several stripes of eight columns and is fully scanned at each frame. In fact, the analog test is performed considering a reduced size of the array (about 576 rows $\times$ 8 columns for MIMOSA22AHR). Then the next block of 8 columns at right is swapped and so on until all the columns are analyzed. In this way, the output of the CPS can be seen as the total noise. In order to automatically analyze the measurement results and achieve the calibration results, eight fast 12-bit ADCs are connected to the eight analog outputs of CPS on the test board [27]. Then, the outputs are used in the calibration process. After the pixel array is read at least one thousand times, the mean value of each sub-array is considered as the noise induced by the whole readout chain including the ADCs and discriminators. To distinguish the noise induced by the sole voltage references, the clamping voltage has been supplied by means of a clean external source with a filter capacitor of 100 nF, used as a test reference. Figure 5.17 depicts the mean outputs of the ADCs when the clamping voltage is provided by the external voltage (EXT), version 1

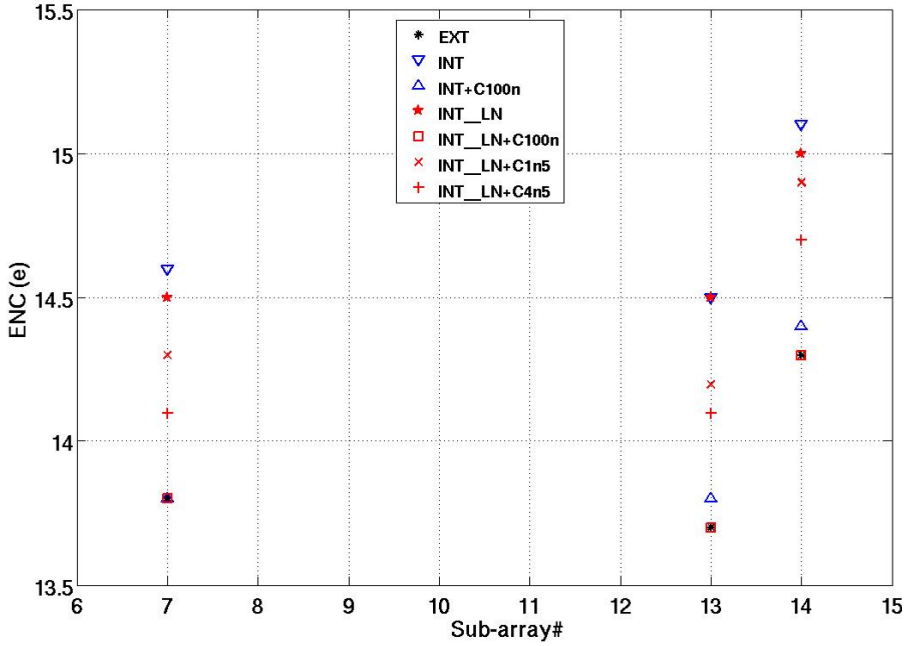


Figure 5.18: *Measured noise of the clamping voltage in different sub-arrays.*

(INT_LN) and version 2 (INT). In order to verify the noise and stability of the proposed circuit in the larger pixel array, the external capacitances of 1.5 nF (INT_LN+C1n5) and 4.5 nF (INT_LN+C4n5) are connected to the output of the proposed circuit, respectively. The first sub-array is excluded as it is faulty. Since the sub-arrays are composed by different preamplifiers architectures, the values vary from 364 ADC units to 1284 ADC units [22]. The results also demonstrate that the proposed generator is stable even with the load capacitance of 100 nF (INT_LN+C100n).

The noise results represented by equivalent noise charge (ENC) are shown in figure 5.18, after the calibration. Only the sub-arrays composed by the improved common source with feedback are shown for clarity. This structure shows very good noise performance and is chosen to be implemented in CPS [21]. The noise of CPS is 14.5 ENCs with version 1, while the noise is 13.7 ENCs with the test reference in sub-array 13. In other words, we have 5.84% more noise when using the proposed circuit without any external components. The measured noise is higher than the value expected. The possible reason is that the version 1 was placed too far with the bandgap and bias circuits, as shown in figure 5.11. Moreover, the digitally adjustable resistor of the version 2 cannot be disconnected from the clamping voltage during version 1 testing. About 100 μA current is drawn from the clamping voltage, while the maximum load current of version 1 is only 0.19 mA. This design is not optimal because these two versions are expected to be tested when they

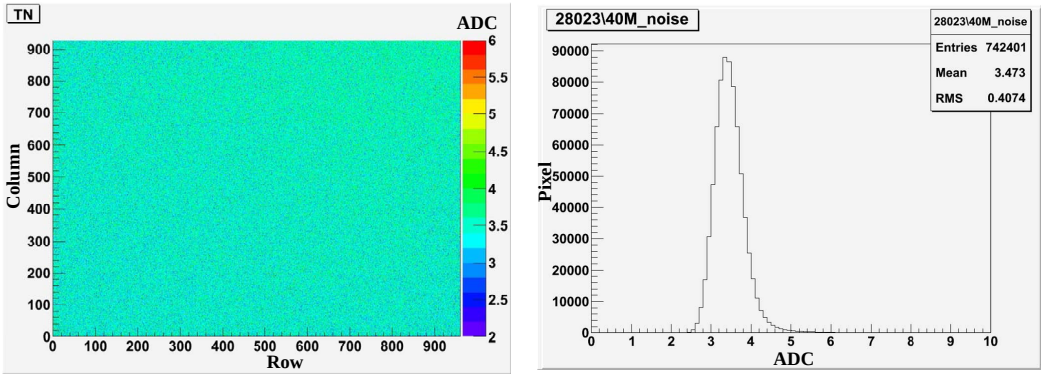


Figure 5.19: *Distribution of the pixels noise in ULTIMATE at 40 MHz clock frequency (left) and Histogram of pixel noise in ADC unit (right) (1 ADC unit=4.15 e^-) [28].*

Table 5.2: *Performances comparison of the two versions.*

	Version 1	Version 2
Chip Area	0.0389 mm^2	0.0584 mm^2
Imax @-5%Vout	0.19 mA	1.3 mA
Dropout Voltage	0.5 V @Iload=0 A	0.1 V @Iload=0 A
PSRR	-52 dB @10 kHz	-49 dB @10 kHz
	-38 dB @1 MHz	-16 dB @1 MHz
Power @3.3 V(no load)	677 μW	726 μW
Current Efficiency @Imax	48.1%	85.5%
Output Noise	222 nV/$\sqrt{Hz}$ @100Hz	1245 nV/$\sqrt{Hz}$ @100Hz
	74.8 nV/$\sqrt{Hz}$ @1 kHz	386 nV/$\sqrt{Hz}$ @1 kHz

are used by the same pixel matrix chip. Only one version will be used in the final chip. The layout can be optimized and the noise can be smaller. It is noted that the noise will decrease with the larger load capacitance. The noise is even smaller than the test reference when the load capacitance is 100 nF. Applying the proposed generator, CPS with larger pixel array will decrease the noise under the premise of stability.

The RegVclamp has been also integrated and demonstrated in ULTIMATE chip, which is dedicated to the PXL detector for STAR experiments. The size of pixel array is 928 × 960 in ULTIMATE. As shown in figure 5.19, good noise uniformity is achieved and the average noise value is less than 15 e^- ENC. The test results show that only 3% noise is distributed by the reference generator RegVclamp [28].

The main performances of the two versions are listed in Table 5.2. Although the noise performance is almost the same in the two versions, version 1 achieves better power

performance and smaller silicon area than version 2. Since the same error amplifiers are employed, the PSRR at low frequency is close in these two versions. However, the PSRR at high frequency is improved by 22 dB with the proposed compensation strategy. The quiescent power dissipation of the RegVclamp is less than 677 μW at power voltage of 3.3 V, 49% of which is consumed by the small feedback resistors in the output stage. The output transistor in version 1 is decreased to save silicon area so the current efficiency is only 48.1%. The current efficiency can be improved with a larger output transistor for other applications.

5.4 Conclusions

In order to implement the power management, a linear regulator named RegVclamp is proposed. This regulator is utilized to generate clamping voltage, which is a critical reference voltage in the CDS operation. Thus, RegVclamp is required low noise, low power consumption and low area. Moreover, it must be full on-chip design. Any external components are not allowed. The reported regulator topologies are summarized at the beginning. However, none of them is suitable for CPS application. Based on the topology of pole-zero cancelation, a series RC network internally introduces a zero to compensate the phase response. One feedback transistor is realized as an adjustable resistor. Thus, the output transistor is adjustable by standard JTAG interface. The measurement results demonstrate that the proposed regulator can meet the requirements of CPS. This regulator has been applied in latest CPS chip.

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Chapter 6

Design of linear regulator for analog supply voltage, RegVdda

RegVdda was designed in order to generate the analog supply voltage in the power management of CPS. Based on the structure of RegVclamp, a novel structure is proposed to maintain the stability and achieve low noise, low power consumption and high power supply rejection at the same time. An optimization design of RegVdda is also given at last.

6.1 Design considerations

As mentioned in Section 2.4, Chapter 2, the load current of RegVdda varies in a large range. Beside the load current, the parasitic capacitance in CPS also should not be neglected due to the long and wide power wires. It becomes significantly large in a large pixel array. Moreover, it is very difficult to directly extract the total parasitic capacitance from the layout of the whole sensor chip (about 4 cm^2). The minimum value is estimated as 200 nF in this design according to the parasite extraction from the layout of each analog block. It is noted that the parasitic capacitances beyond these blocks are not taken into account and the parasitic capacitance varies with process fluctuation. Therefore, design margin must be considered. With such a large capacitance and a large load current range, the output pole location significantly varies with the load current [1] and it must be the dominant pole at low-load condition. In addition, any external component is not allowed to achieve a full on-chip regulator. In order to guarantee the stability in the full range of load current, a novel compensation strategy is proposed as shown in figure 6.1. The regulator employs a series RC network, which introduces a zero to compensate the phase.

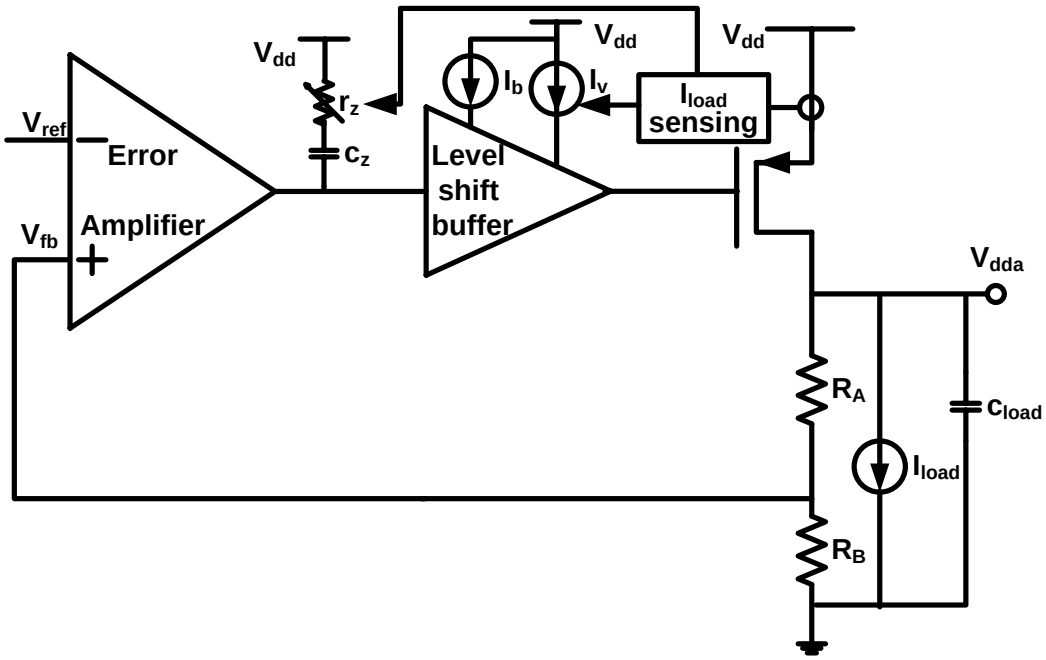


Figure 6.1: *Block diagram of RegVdda.*

Moreover, the locations of the poles and zeros are adapted by the current feedback. They move towards the same direction as the output pole does. Thus, the output pole is always the dominant pole at the light load or heavy load. The next section will present the stability analysis in detail.

The power supply rejection (PSR) performance is important in this design. Especially, the regulator is used following the DC-DC converter in the power system of detectors. Since the inductor must be air-core, the DC-DC converter usually works at the frequency of higher than 1 MHz to supply high current [2]. In order to suppress the switching noise, the PSR should be high at high frequency. The noise induced by the regulator is also needed to be low. Moreover, low power is required due to the cooling system and the silicon area is severely limited to be fully built in CPS. The design specifications are listed in Table 6.1.

6.2 Circuit design

The schematic diagram of the proposed regulator down to transistor level is depicted in figure 6.2. The regulator is composed of three stages: an error amplifier, a buffer and an output stage. The error amplifier is implemented as a simple differential amplifier, so it can be reused in the smaller feature size technology. The basic idea of the compensation

Table 6.1: *Design specifications of RegVdda.*

Item	Specification
Full on-chip	Yes
Dropout voltage (V)	$\leqslant 0.3$
Output voltage (V)	3
Load capacitance (nF)	$\geqslant 200$
Load current (mA)	$0 \sim 200$
PSR @ 1 MHz (dB)	$\leqslant$ -20
Power dissipation (mW)	$\leqslant 4$

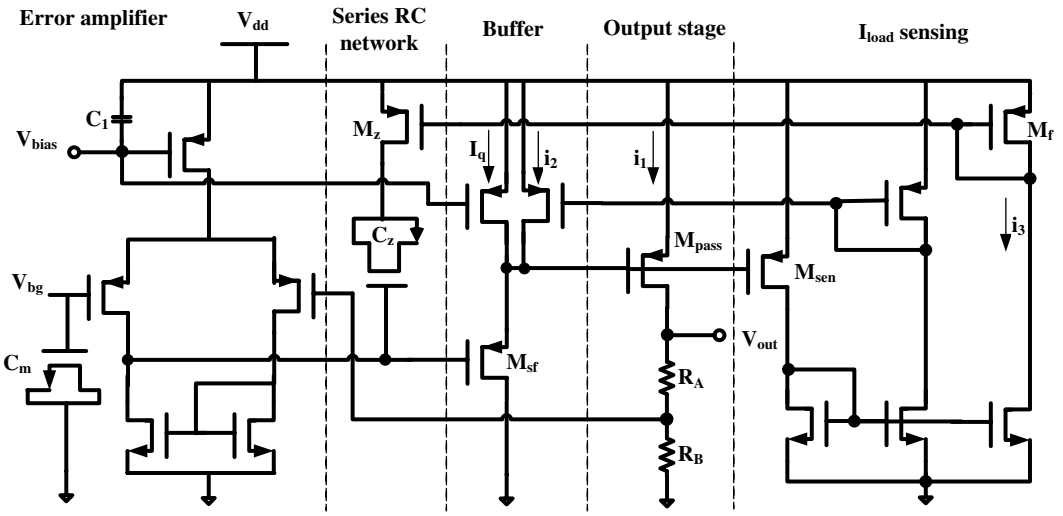


Figure 6.2: *Implementation of the proposed regulator.*

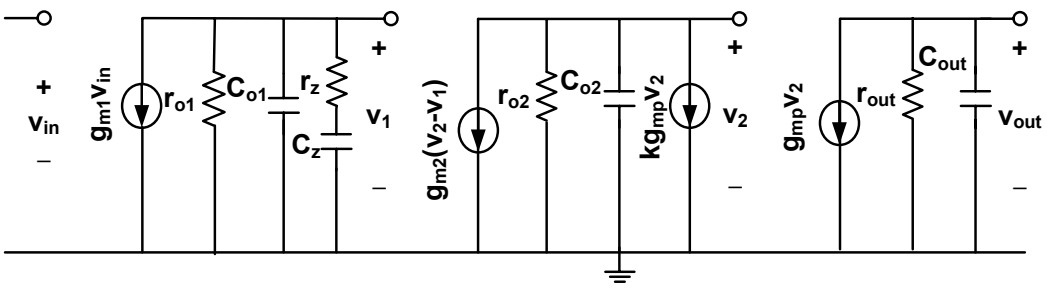


Figure 6.3: *Equivalent small-signal model of the proposed regulator (open-loop).*

strategy is to keep the output pole being the first dominant pole and to adapt the locations of the other poles and zeros with the load current. The pole between the error amplifier and the pass transistor is usually located at low frequency in the uncompensated regulator, so a buffer is inserted to divide this pole into two higher-frequency poles [3]. This buffer is also helpful to improve the PSR at high frequency, which will be presented later. A series RC network (M_z and C_z) contributes a zero, which is connected between the power and the input of the buffer. Since the location of the output pole varies in a large range (proximately from 30 Hz to 50 kHz), a larger compensation capacitance is chosen to limit the bandwidth in [4]. Nevertheless, the integrated capacitance occupies large silicon area and the bandwidth is limited. To maintain the stability and decrease the compensation capacitance, current feedback is employed. A load current sensing circuit senses the current flowing through the pass transistor and forms current feedback in two paths. One adapts the current flowing through the buffer as well its transconductance. The other adapts the source-gate voltage of the transistor M_z to adapt its resistance. Therefore, the other poles and zeros are adaptable with the current feedback. The capacitor C_z is implemented by PMOS capacitances which can save silicon area and can be easily fabricated in the P-substrate standard CMOS process.

6.2.1 Stability analysis

According to figure 6.2, the equivalent small-signal model of the regulator is illustrated in figure 6.3. The gain of the buffer and the output stage is low so the Miller-effect is ignored. The loop-gain of the regulator is given as

$$A_{v-loop} = \frac{\beta g_{m1} g_{m2} g_{mp} r_{o1} r_{o2} r_{out} (1 + r_z C_z s)}{(g_{m2} + k g_{mp} + C_{o2} s)(1 + r_{out} C_{out} s) D} \tag{6.1}$$

where $D = r_z C_z r_{o1} C_{o1} s^2 + (r_{o1} C_{o1} + r_z C_z + r_{o1} C_z) s + 1$, β is the feedback factor $R_B/(R_A + R_B)$. g_m, r_o and C_o represent the transconductance, output resistance and output capacitance, respectively. The subscript $1, 2, p$ represent the error amplifier, buffer and pass transistor, respectively. r_{out} is the output resistance of the regulator including the load resistance. C_{out} is the output capacitance dominated by the load capacitance. C_z and r_z are the series RC network. k is the radio of i_2 to i_1, (shown in Fig.6.2). In terms of (6.1), there are four poles and one zero in the proposed regulator, which are expressed in detail as follows.

$$P_{out} = \frac{1}{r_{out} C_{out}} \approx \frac{1}{C_L[(R_A + R_B)//r_{dsp}//r_{load}]} \tag{6.2}$$

$$P_{ea} \approx \frac{1}{[(r_z + r_{o1})C_z + r_{o1}C_{o2}]} \approx \frac{1}{(r_z + r_{o1})C_z} \tag{6.3}$$

$$P_{buf} = \frac{g_{m2} + kg_{mp}}{C_{o2}} \approx \frac{g_{m2} + kg_{mp}}{C_{gsp} + C_{gdp}} \tag{6.4}$$

$$Z_z = \frac{1}{r_z C_z} \tag{6.5}$$

$$P_h \approx \frac{r_z + r_{o1}}{r_z r_{o1} C_{o1}} \tag{6.6}$$

where C_{gdp} and C_{gsp} are the gate-drain capacitance and gate-source capacitance of the pass transistor, respectively. C_L is the load capacitance and r_{load} is the load resistance. r_{dsp} is the output resistance of the pass transistor M_{pass}. Though there are four poles appearing, only P_{out} and P_{ea} are located below the unity-gain frequency. The effect of P_{ea} is compensated by Z_z. It is noted that the precise cancelation is not required according to (6.3) and (6.5). Thus, the proposed circuit is easily realized, compared with the other pole-zero cancelation strategies. P_{buf} and P_h are pushed to high frequency by the buffer due to its low output impedance and small input capacitance. According to (6.3)-(6.6), the poles and zeros move with the load current due to the terms r_z and g_{m2}. They are expressed as the functions of the load current i_{load} for clear analysis.

$$r_z = [\mu_p C_{ox}(W/L)_{Mz}(\sqrt{\frac{ji_{load}}{2\mu_p C_{ox}(W/L)_{M_f}}} - V_{thp})]^{-1} \tag{6.7}$$

$$g_{m2} = \sqrt{2(I_q + ki_{load})\mu_p C_{ox}(W/L)_{M_{sf}}} \tag{6.8}$$

where j is the radio of i_3 to i_1 (shown in figure 6.2). The location of the output pole P_{out} is directly proportional to the load current, while the others are located in direct proportion to the square root of the load current. P_{out} is located at very low frequency when the load current is low. C_{gdp} and C_{gsp} are small since the pass transistor works in subthreshold region. P_{buf} is beyond the unity-gain frequency. Consequently, the regulator is certainly stable at light load. Though the bandwidth is extended in the heavy load case, the other poles and zeros also move to high frequency. The regulator thus can be still stable. Taking into account of P_{buf}, the phase margin ϕ is given as

$$\phi = 90^o - arctan\frac{\omega_n}{P_{ea}} - arctan\frac{\omega_n}{P_{buf}} + arctan\frac{\omega_n}{Z_z} \tag{6.9}$$

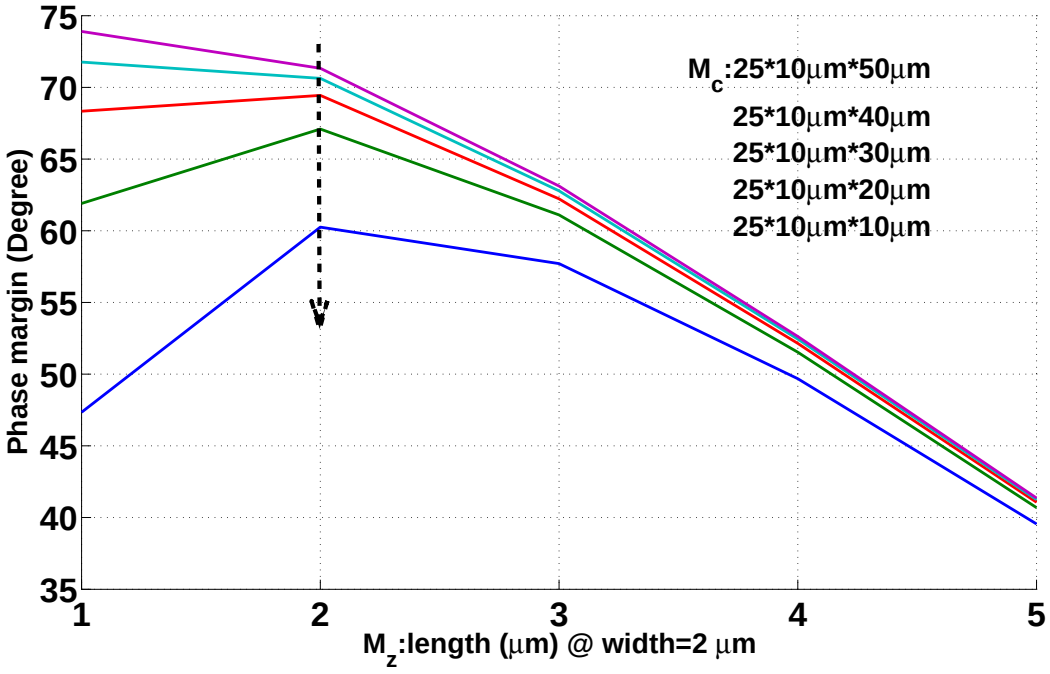


Figure 6.4: *Optimization of M_z and M_c.*

where ω_n is the unity-gain frequency. Substituting (6.3) - (6.5) into (6.9), $tan\phi$ is approximately given as,

$$tan\phi = \frac{r_{out}C_{out}A_{vdc}C_z^2 r_z(r_{o1}+r_z)}{r_{out}^2C_{out}^2C_z r_{o1} + A_{vdc}^2C_z^2 r_z r_{o2}C_{o2}(r_{o1}+r_z)} \tag{6.10}$$

where A_{vdc} is the open-loop DC gain of the regulator. Since r_{out} varies in a large range (approximately from 15 to 25k Ω), (6.10) is analyzed at light load and heavy load, respectively. When the load current is very low, $r_{out}^2C_{out}^2 \gg A_{vdc}^2C_z^2r_z(r_{o1}+r_z)$, r_zC_z is drawn as follows

$$r_zC_z \approx \frac{r_{out}C_{out}tan\phi}{A_{vdc}}. \tag{6.11}$$

When the load current is very high, $r_{out}^2C_{out}^2 \ll A_{vdc}^2C_z^2r_z(r_{o1}+r_z)$, r_{o2} is drawn as follows

$$r_{o2}^{-1} \approx kg_{mp} + g_{m2} = \frac{A_{vdc}(C_{gsp}+C_{gdp})tan\phi}{r_{out}C_{out}}. \tag{6.12}$$

Equation (6.11) implies that the compensation capacitance and resistance can be decreased by the open-loop gain. Furthermore, larger r_z can be chosen in order to save more silicon area occupied by C_z. However, P_h will move close to the unity-gain frequency leading to poor stability when a large r_z is utilized. Assuming that the other parameters are

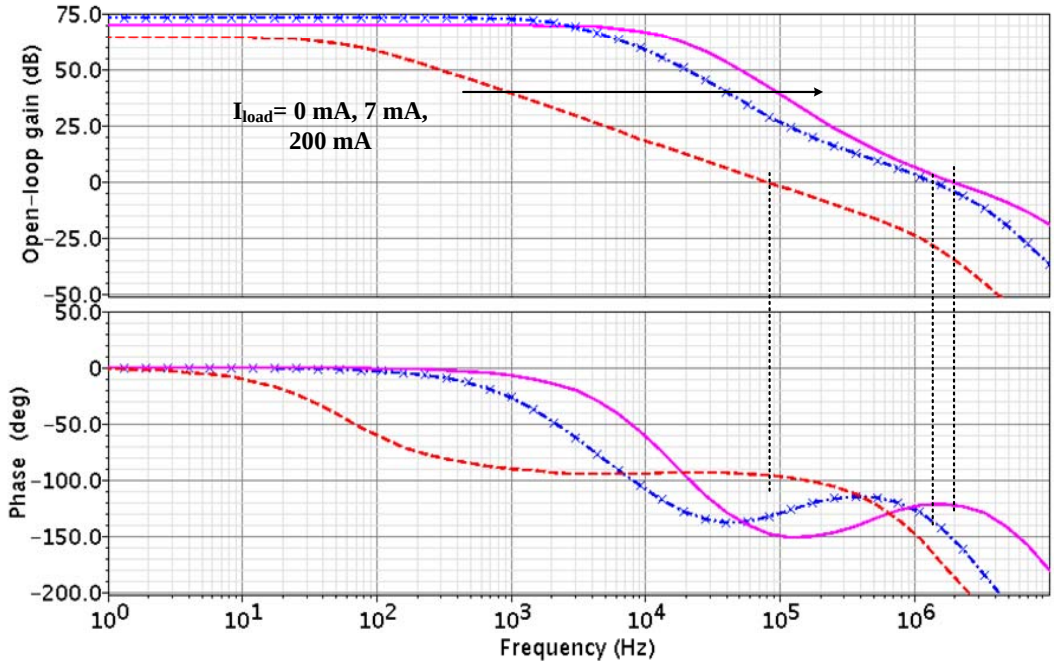


Figure 6.5: *Open-loop frequency responses at load current of 0 mA, 7 mA and 200 mA when load capacitance is 200 nF.*

given, the tradeoff between silicon area and stability is shown in Fig.6.4. Since C_z and r_z are realized by transistor M_c and M_z (shown in figure 6.2), respectively, their values are presented by width and length. The phase margin is certainly improved with larger C_z. However, the improvement is around 10^o with five time increase in the dimension of C_z. In terms of the silicon area limitation, the dimension of M_c is chosen as 25 $\times$ 10 $\mu m\times$ 10 μm, which generates a capacitance of about 10.5 pF. M_z is chosen as 2 $\mu m\times$ 2 μm.

The stability of the proposed regulator is verified by SPECTER when the load capacitance is 200 nF. Figure 6.5 shows the frequency response of the regulator as the load current varies. It demonstrates that the poles and zeros move to higher frequency when the load current becomes larger. The phase margin of regulator is larger than 45^o over the full range of load current. Moreover, the minimum phase margin happens at the load current of 7 mA. In this case, the pass transistor enters saturated region from subthreshold region so its gate-source capacitance and gate-drain capacitance dramatically increase, according to the volt-capacitance of CMOS capacitor. On the other hand, the feedback current is low so P_{buf} is close to the unity-gain frequency. The phase margin begins to increase when the load current continues to increase. The simulation results also verify (6.12). I_q and k should be large enough to guarantee the stability at the load current of 7 mA.

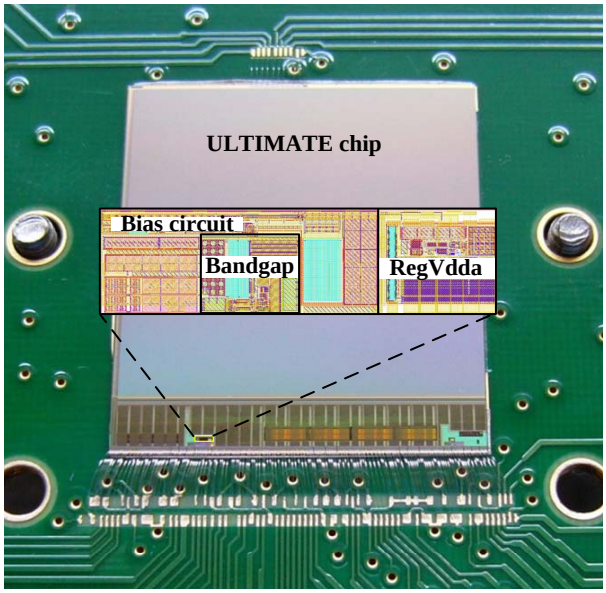
6.2.2 Dropout voltage and PSR

The dropout voltage is required to be low to achieve high power efficiency. It is only 0.3 V in this design. Thus, the pass transistor is undoubtedly very large if it works in the saturated region. In addition, quiescent current also increases. The chip area and power dissipation become large. Therefore, the pass transistor is designed to work in linear region at heavy load and a smaller pass transistor can be employed. The load regulation is decreased due to the small pass transistor and the negative current feedback for stability. Thus, tradeoff should be considered. Since the current required by CPS is almost constant after their start-up, the load regulation is sacrificed in the proposed circuit. The source follower implemented by NMOS transistors can form positive feedback to improve the load regulation. However, the noise performance degrades and the operation point is difficult to be set.

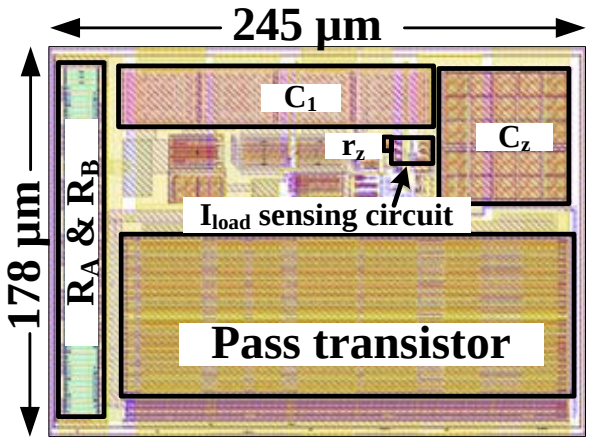
In order to be free of the power supply ripple, the proposed regulator not only achieves large bandwidth, but also employs ripple cancelation technique. As mentioned before, the bandwidth is not sacrificed for the stability so good PSR is achieved at high frequency [5]. The buffer is simply implemented by a source follower with current-source load. It allows the ripple of the power supply to be present at the gate of the pass transistor. Therefore, the ripple cancels [6]. Compared with the cascade regulator [7], the proposed scheme remarkably saves the silicon area and power dissipation.

6.3 Experimental results and discussions

The proposed regulator is designed based on a 0.35-μm commercial CMOS technology (2Poly4Metal). As shown in figure 6.6, the regulator has been fabricated as an optional circuit in ULTIMATE chip, which is proposed to be installed in PXL (also called PIXEL) detector for STAR experiments. The bias and bandgap circuits are placed near the regulator. The bandgap circuit is a low-noise commercial IP core. In order to filter noise, many capacitances are employed in the bias circuit. The regulator occupies 178 μm $\times$ 245 μm silicon area. The compensation capacitor C_z, resistor M_z and the load current sensing circuit do not significantly increase the chip area. The pass transistor size is also decreased. R_A and R_B are implemented by common-centroid layout to achieve good match. Moreover, each transistor is surrounded by guard ring and the space between NMOS transistors and N-WELL is enlarged in order to achieve good radiation tolerance. Though the bandgap and bias circuits occupy large silicon area, they can be shared with other blocks in ULTIMATE chip.



(a)



(b)

Figure 6.6: *ULTIMATE chip micrograph (a) and layout of the regulator RegVdda (b).*

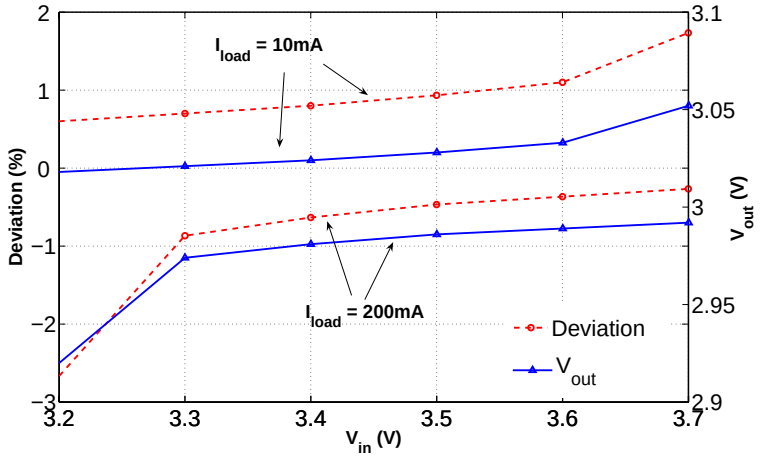


Figure 6.7: *Measured line and load regulation.*

The regulator has been tested for line and load regulation and the output voltage is 3 V. As shown in figure 6.7, the minimum dropout voltage is about 0.3 V when the load current is 200 mA. The output deviation is less than 1.8% when the input voltage is higher than 3.3 V. The line regulation at 200 mA is 34 mV/V due to the current feedback and the voltage drop on the bonding wire.

The load transient response of the regulator was tested when the load current varied between 0 mA and 110 mA. The rising and falling time is about 10 ns. Different load capacitances are connected with the regulator. Since zero-ESR (equivalent series resistance) is impossible in practice, the low-ESR (about 0.02 Ω) ceramics capacitors are used in this test. As shown in figure 6.8, the regulator can stay stable with the different capacitances of 200 nF and 300 nF. The settling time is less than 3 μs. An undershoot of less than 120 mV appears. This is owing to the negative current feedback, which charges the gate capacitance of the pass transistor when the load current becomes large. The overshoot is less than 30 mV when the load current decreases to 0 mA. The regulator is still stable at the load capacitance of 35 μF, which is a tantalum capacitance with ESR of about 0.1 Ω. The overshoot and undershoot disappear because of the large capacitance. This result demonstrates that the compensation strategy can be utilized in larger capacitance cases with the help of ESR. The output voltage approximately decreased by less than 90 mV when the load current is 110 mA due to the smaller size of the pass transistor.

The PSR was measured with the setup shown in figure 6.9(a). The reference voltage is 1.2 V and the output voltage is 3 V. A sinusoid signal is injected to the power as the noise source via a capacitance of 95 μF. In order to isolate the DC power and AC power, a resistor of 10 Ω is connected between the power supply and the input voltage of the regulator. The load capacitance is 200 nF. The PSR performance is measured at the load

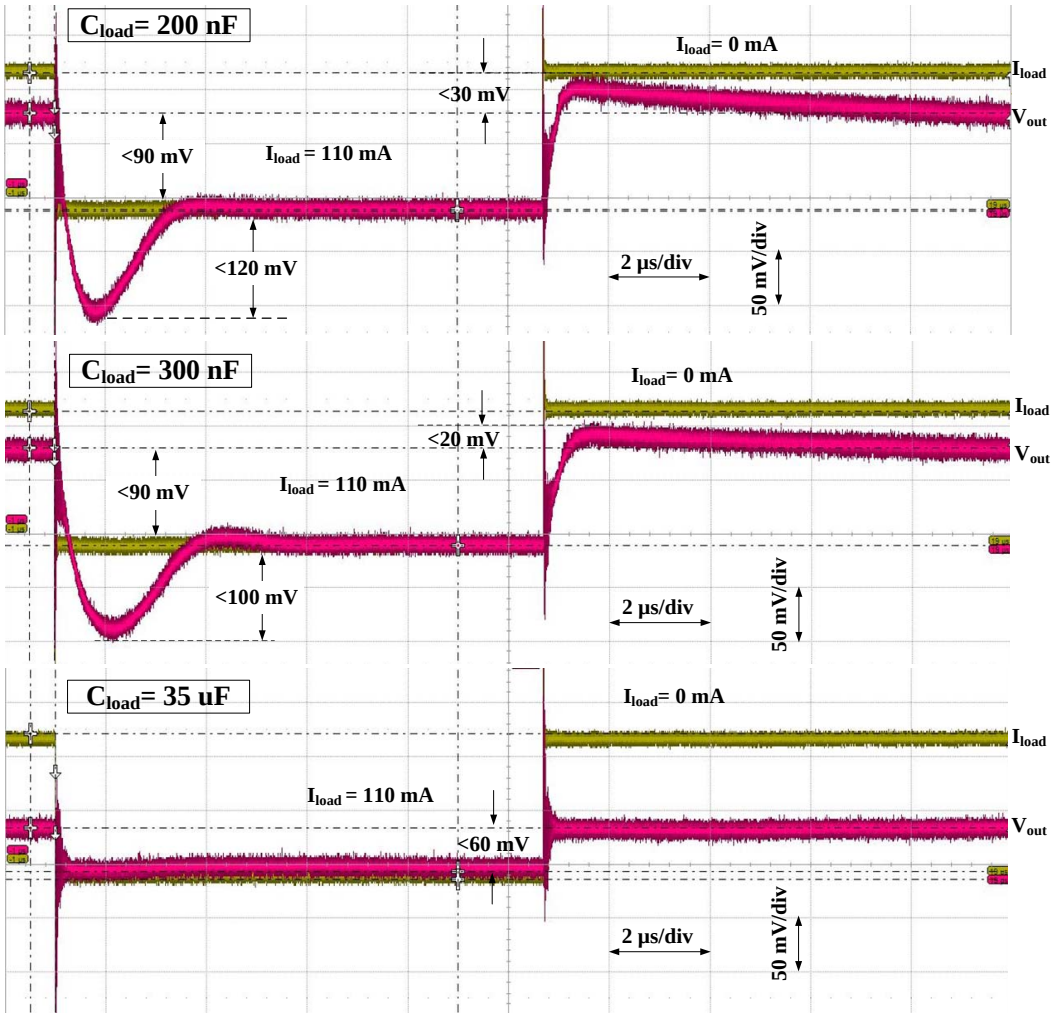


Figure 6.8: *Transient response when the load current varies with different load capacitances. (I_{load} (Yellow),V_{out}(Red))*

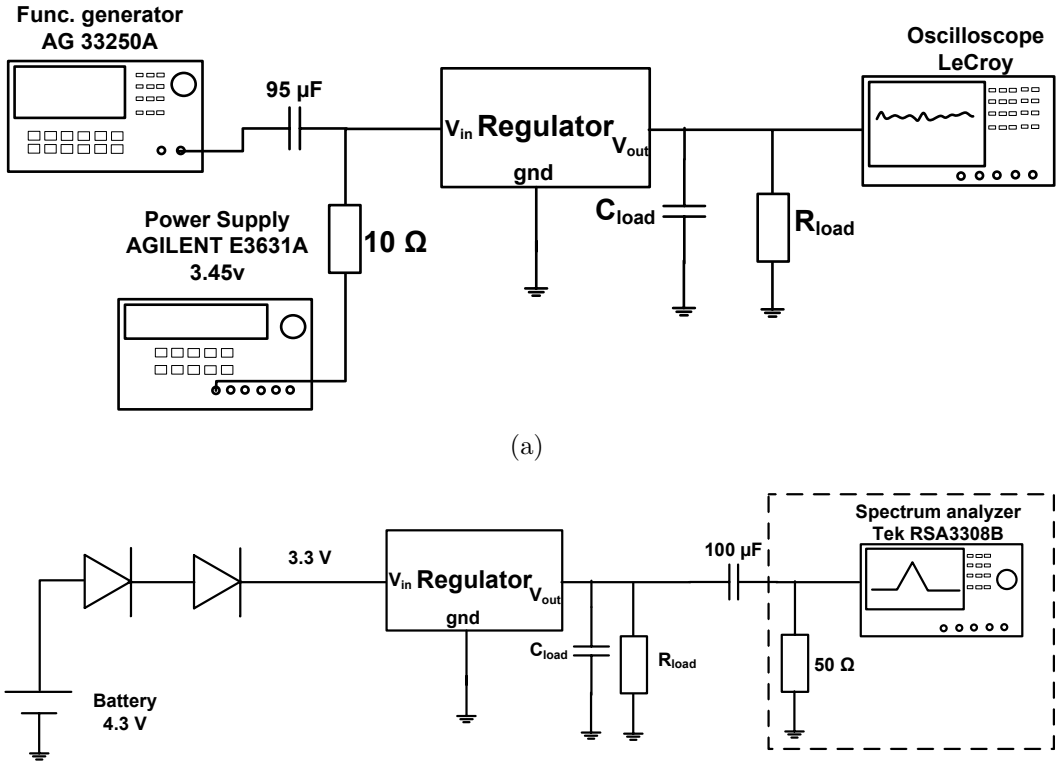


Figure 6.9: *Measurement setup of PSR (a) and output noise (b).*

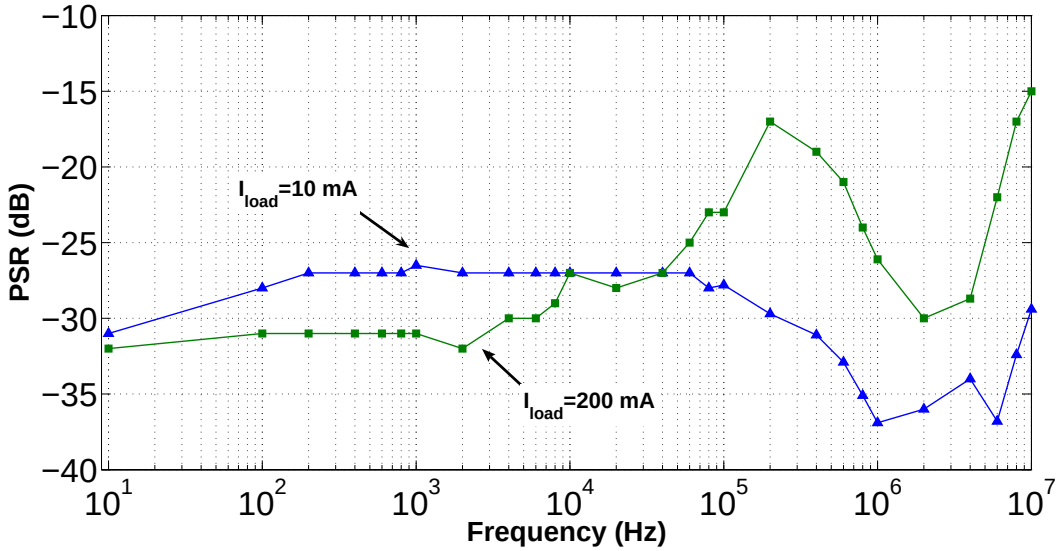


Figure 6.10: *Measured PSR.*

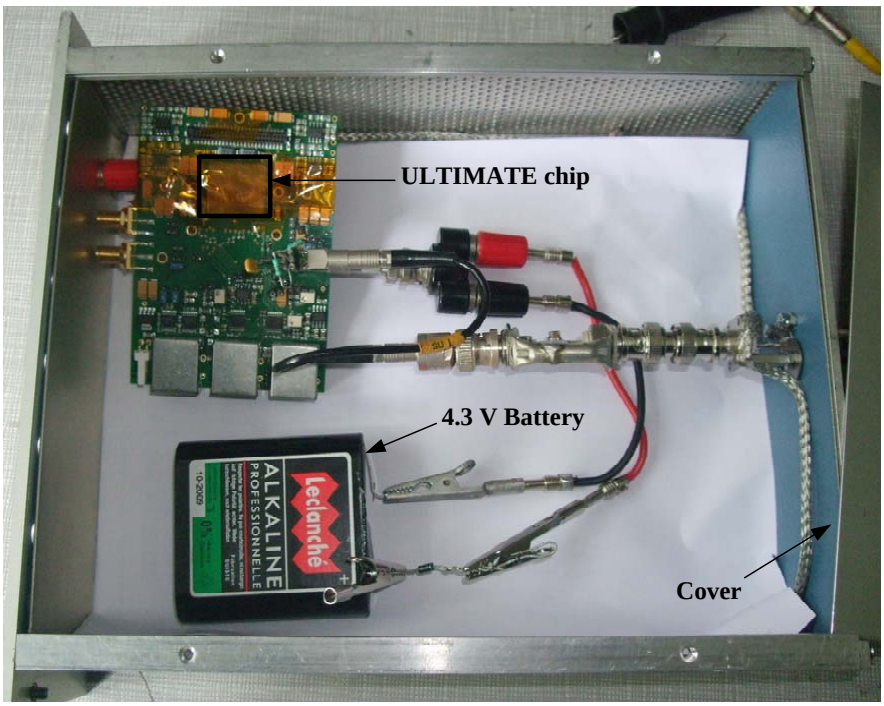


Figure 6.11: *Tested chip and battery are placed in the metal box for shielding.*

current of 10 mA and 200 mA. Since the loop-gain is low due to the small feedback factor (about 0.4), the PSR is not very high at the low frequency [8]. Since the pass transistor works in linear region at the high load current, the PSR increases at 100 kHz, as shown in figure 6.10. However, it decreases to -25 dB at 1 MHz and is lower than -20 dB at 6 MHz. It demonstrates that the proposed structure improves the PSR at high frequency. Thus, the proposed regulator is helpful to suppress the switching noise of the DC-DC converters, whose frequency is higher than 1 MHz. The PSR can be further improved by increasing the output transistor size and employing the higher reference voltage.

The output noise was measured by the setup depicted in figure 6.9(b). The input resistance of the spectrum analyzer is 50 Ω. The load current and capacitance are 0 A and 200 nF, respectively. In order to achieve a low noise floor, the chip is powered by a battery of 4.3 V. Moreover, the chip and battery are placed in a metal box with cover for shielding the noise from surrounding equipments (figure 6.11). This metal box is connected to the ground. The noise is displayed in dBm unit owing to its small value. As shown in figure 6.12, the integration noise is 41 μV(-74.51 dBm in power unit) from 10 Hz to 100 kHz. The output noise spectrum density is shown in figure 6.13. It is calculated by the expression

$$V_{RMS}/\sqrt{Hz} = 10^{(dBm-10lg(RBW\times R)+30)/20} \tag{6.13}$$

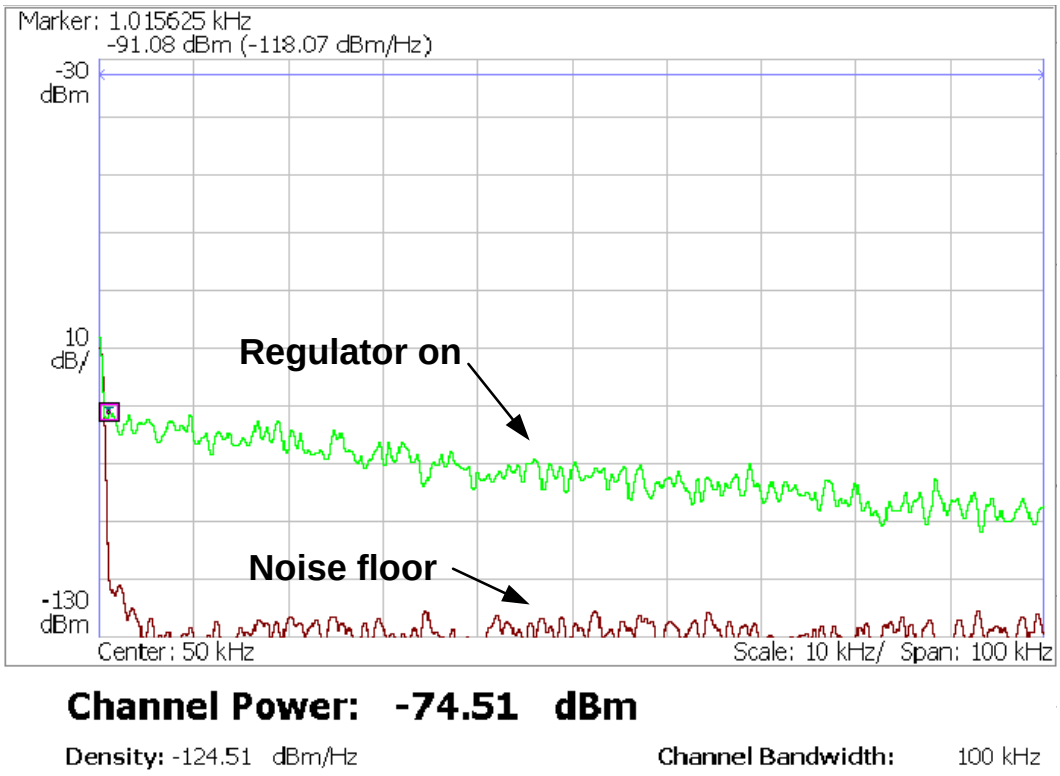


Figure 6.12: *Measured noise.*

where RBW is the resolution bandwidth of the spectrum analyzer and R is its input resistance. The output noises are lower than 0.34 $\mu V/\sqrt{Hz}$ and 65 $nV/\sqrt{Hz}$ at 1 kHz and 100 kHz, respectively.

The main performance parameters of the proposed regulator are listed in Table 6.2, as well the comparisons with the previous works. Since the feedback resistances are small to decrease noise, most of the current (about 100 μA) is consumed by these resistances. The current feedback also increases the quiescent current to decrease the compensation capacitance and maintain stability at high load current. Though the proposed circuit consumes higher quiescent current, the current efficiency is very close to that of the other works. The figure of merit (FoM) presented in [9] is usually used to compare the performances of regulator. It is smaller in the proposed regulator, compared with work in [4], where a load-tracking circuit is also introduced for stability. Since the PSR and noise performance are not contained in this FoM, another FoM reported in [8] is also calculated, which includes the PSR performance. It indicates that the proposed regulator is better than the work in [7] though its PSR value is smaller. The proposed circuit also achieves the lower silicon area and lower noise, compared with the other works.

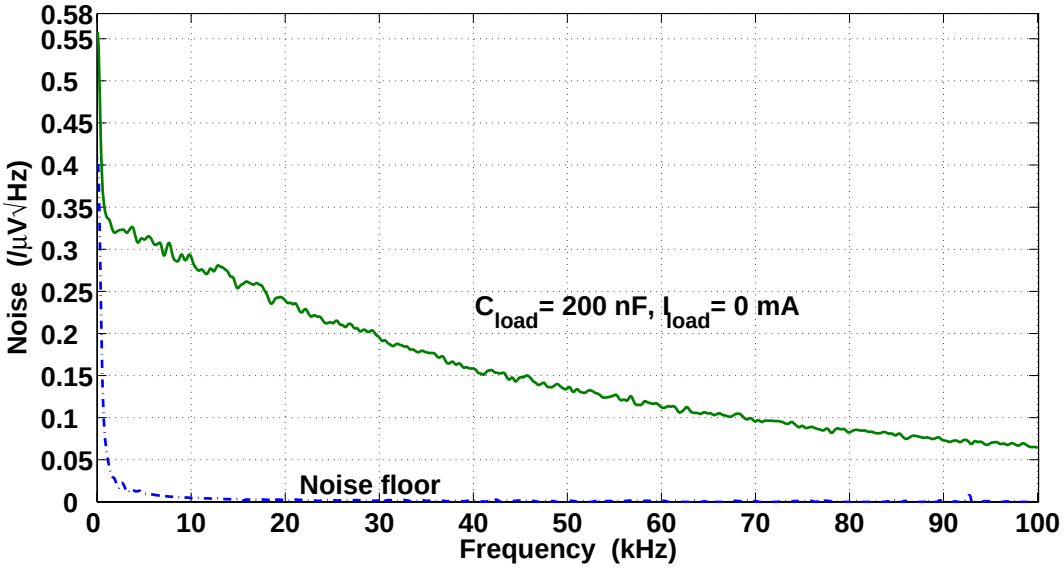


Figure 6.13: *Measured output noise spectrum density.*

Table 6.2: *The performance comparisons of the proposed work and reported work*

	[1]	[4]	[7]	[This work]
Process (μm)	0.35	0.35	0.13	0.35
Silicon area (mm^2)	0.12	0.412	0.166	0.044
V_{in}	3-4.2	3-6	3	3.3-3.7
V_{out}	2.8	2.8	2.8	3
$V_{dropout}$	0.2	0.2	0.2	0.3
I_{max} (mA)	50	100	150	200
I_q (μA)	65	72 @0 mA 120 @100 mA	100	147 @0 mA 314 @200 mA
Current efficiency @Full load (%)	99.87	99.88	99.93	99.843
Line regulation @Full load(mV/V)	15	4.09	1.5	34
Load regulation (mV/mA)	N.A.	0.085	0.017.4	0.45
PSR@1 MHz (dB)	-37	N.A.	-40	-26
Output spectral noise density ($nV\sqrt{Hz}$)	4600 @100 Hz 630 @100 kHz	N.A.	338 @1 kHz 100 @100 kHz	340@1 kHz 65 @100 kHz
FoM in [9] (ns)	0.00023	113	N.A.	0.188
FoM in [8]	N.A.	N.A.	11 M	57 M

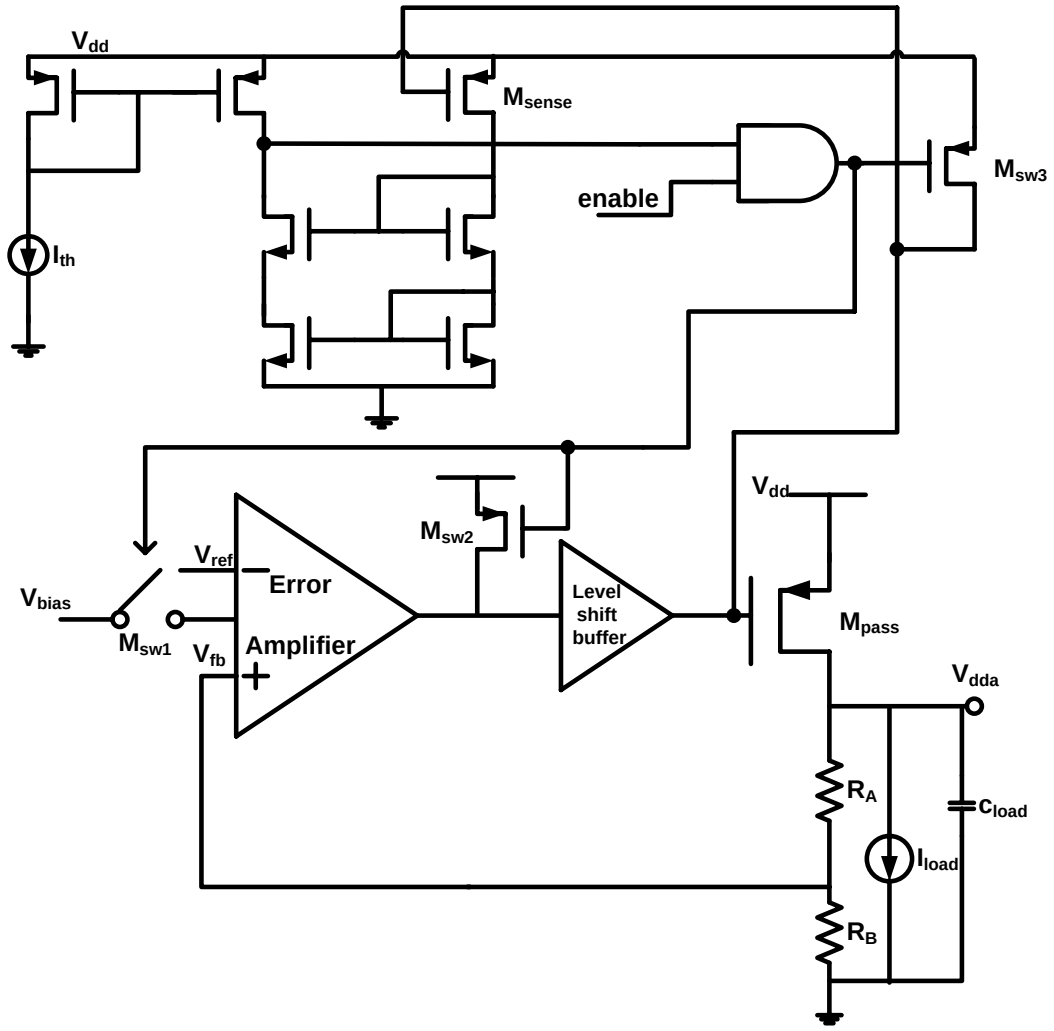


Figure 6.14: *Implementation of the current limiter.*

6.4 Optimization design of RegVdda

An optimization design of RegVdda has been submitted to supply higher current and decrease dropout voltage. In order to protect CPS chips, a current limiter is integrated in RegVdda. The optimization design has been integrated in MIMOSA30 as an optional circuit.

- Current limiter

  The CPS works in harsh radiation environment. Some failures may happen leading to very large short current. Consequently, a current limiter was designed in regulator RegVdda in order to protect the CPS chip. The current limiter can shut down the RegVdda when failures happen. As shown in figure.6.14, the current limiter is

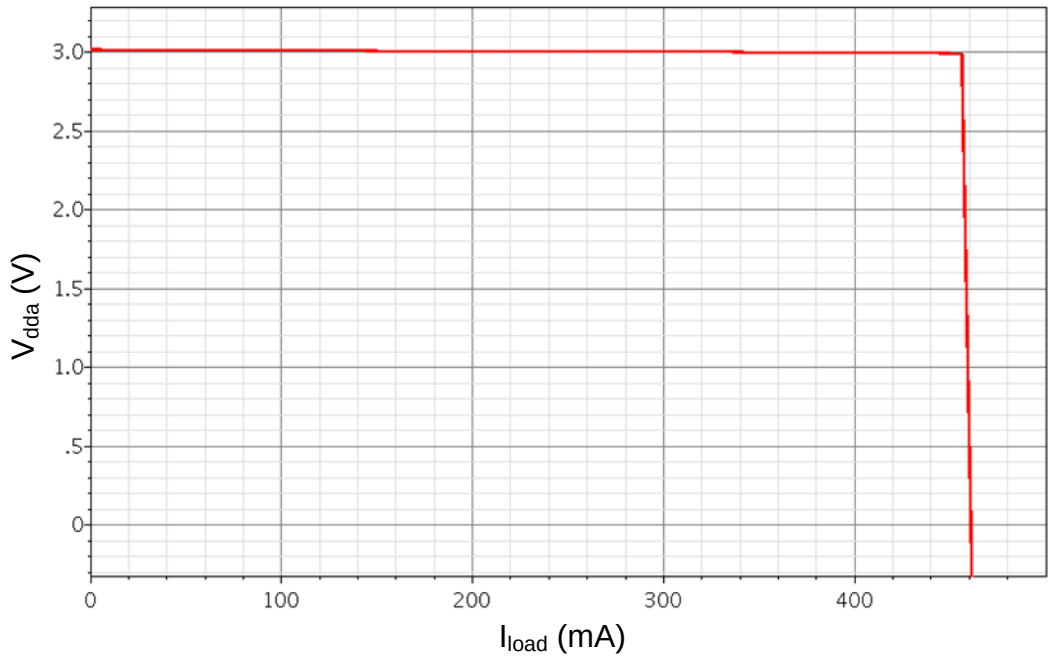


Figure 6.15: *Simulated results of current limiter in nominal corner.*

realized by a current comparator. A sensing transistor M_{sense} is employed to copy one part of the current flowing through the pass transistor. In order to decrease the sensing current, the ratio W/L of M_{sense} is 1/1300 of the pass transistor. Obviously, the precision of the current limiter depends on the precision of the copied current. Thus, the cascode current mirror is used. When the sensing current is larger than the threshold current (I_{th}), all stages of RegVdda are shut down by switches M_{sw1}, M_{sw2} and M_{sw3}. The current limiter is also shut down results in lower quiescent. The threshold current is set to be two times larger than the normal value, when the failures may happen.

The current limiter is fabricated in MIMOSA30 with 0.35 μm commercial CMOS process. As shown in figure 6.15, the regulator can be shut down when the load current is larger than 460 mA. However, the current comparator is influenced by the process, which should be further researched.

- Lower dropout voltage

  In order to improve the design margin and avoid generating not sufficient high analog power voltage, the dropout voltage is designed to be lower. The dropout voltage is high due to the small pass transistor in the previous design. Thus, the pass transistor is enlarged to 2 cm/ 0.35 μm. Figure 6.16 illustrates the curve of output voltage versus input voltage at the load current of 200 mA. A dropout voltage of

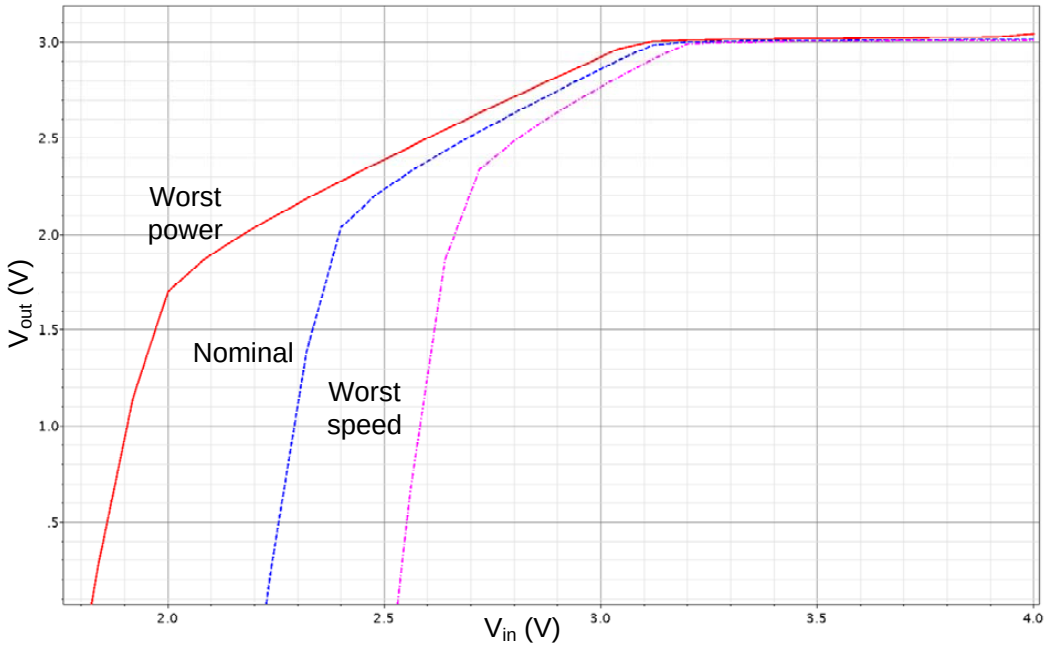


Figure 6.16: *Simulated results of V_{dda} versus V_{dd}.*

about 0.2 V is achieved in difference cases. Though the chip area is increased from 178 $\mu m\times$ 245 μm to 288 $\mu m\times$ 200 μm, it can be still acceptable by utilizing the area left in CPS.

6.5 Conclusions

The linear regulator RegVdda is presented in this chapter. A novel structure is proposed in order to simultaneously achieve good stability, low noise and low power consumption. The measurement results show that the proposed regulator is stable in the full range of load current (0 - 200 mA). In order to protect the CPS chip from over-current failure, a current limiter built-in RegVdda has been designed. Moreover, the dropout voltage is decreased in an optimization design of RegVdda. The proposed structure can be also used in other applications, such as system on chip and radio frequency circuits.

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Conclusions and perspectives

Conclusions

CMOS pixel sensors (CPS, also called monolithic active pixel sensors) offer the attractive trade-off among material budget, radiation tolerance, power consumption and granularity. The other advantage is that CPS can be thinned down to 50 μm, which is helpful to decrease the material budget. CPS is a good choice to track the charged particle in vertex detectors, for example, the PXL detector in heavy flavor tracker (HFT) for STAR experiments.

A series of CPS chips called MIMOSA have been designed and measured by the microelectronic group in IPHC, Strasbourg, France, since 1990s. This thesis is one part of the CPS design in IPHC, which is dedicated to the power management. This block provides the required voltages for the core circuits, such as pixel array, column-level discriminator and so on. There are some critical voltages used in CPS chips including the analog power supply voltage and digital power supply voltage. Some reference voltage is required to be low noise due to the very weak signal detected. Cables or traces are required if these voltages are provided from ladder via pads. Since more sensors will equip in the detector, the number of the cables is significantly increased. The material budget is weakened. In addition, the power burnt on the cables increases. Thus, the power efficiency of the detector systems is decreased to an unacceptable value. Moreover, the CPS chips are close mounted in the ladder. The crosstalk happens among the sensor chips. A chip may influence its neighbors, since the power supply voltage is shared. The reference voltages also become noisy. Though the filter capacitor is helpful to decrease the noise, the material budget is increased and the ladder design is complicated. As a consequence, some critical voltages are proposed to be generated by on-chip regulators in power management.

The low dropout regulator is a critical element in the power system. Although the switching power converters can achieve high power efficiency, the noise and area limit their applications. It is also difficult to integrate the inductor or large capacitor on-

chip. The low dropout regulator usually features low dropout voltage, low noise and low area. Thus, the low dropout regulator is chosen. It can function as a post regulator of the switching power converters (e.g. DC-DC converter) in ladder to decrease noise and generate required voltages. However, some challenges are brought by the requirements of CPS. Since any external element is not allowed to achieve full on-chip design, the stability should be carefully analyzed. Moreover, low-noise and low-power are required. The radiation tolerance should be also concerned. Two low dropout regulators are designed and measured in this thesis work. One called RegVclamp is utilized to provide the clamping voltage used for correlated double sampling operation. The other called RegVdda is utilized to provide the analog power supply voltage.

A structure based on pole-zero cancellation and optimization design are proposed to meet all the requirements. The two regulators are verified by two prototypes. The regulator RegVclamp is integrated in MIMOSA22HRE to offer the clamping voltage to the sensor chip. The measurement results show that only 5.8% noise is increased by RegVclamp, which can meet the noise requirement. It is also verified by the ULTIMATE chip, in which the parasitic capacitance is different with MIMOSA22HRE. The most of load capacitance of RegVclamp comes from the parasitic capacitance. It is about 0.5 nF in MIMOSA22HRE and 5 nF in ULTIMATE. The tested results demonstrate that the RegVclamp can work with a wide range of load capacitance. Thus, it can be reused in CPS chips with different pixel array size. The equivalent noise charge (ENC) of the pixel is lower than 15 e^-, when the clamping voltage is provide by RegVclamp. It can fulfill the requirements of CPS chip.

In order to generate analog power supply voltage, RegVdda is designed. Since the load current varies in a large range, all the poles and zeros are adaptive to guarantee the stability. A novel structure is proposed. A series RC network is employed to introduce a left half-plane zero. Moreover, two current feedbacks are used to adapt the value of the resistor in series RC network and the transconductance of the buffer in mid-stage. Thus, all the poles and zeros move to the same direction as the output pole does. A small compensation capacitor is required in this regulator. Moreover, the output transistor is designed to work in sub-threshold region and linear region at low load and high load, respectively. Thus, the dimension of the output transistor is decreased and bias current is decreased. In order to achieve radiation tolerance, the circuit is fabricated in a process with high-resistance epitaxial layer. Moreover, each transistor is enclosed by the guard ring. RegVdda has been integrated in ULTIMIATE chip as an optional circuit. The measurement results demonstrate this regulator is stable in the full range of the load current (0 - 200 mA) when the load capacitance is 200 nF and 300 nF. The power supply

rejection is higher than 20 dB at the frequency of 1 MHz. The tested noise is about 65 $nV/\sqrt{Hz}$ at 100 kHz. However, the dropout voltage is 0.3 V due to the small output transistor. In order to decrease the dropout voltage, an optimized regulator was designed and it can supply the load current up to 300 mA. A current limit circuit was designed to protect the regulator and the other blocks in CPS. A current comparator is designed to compare the sensed current and the threshold current. A logic "0" will be output if the load current is higher than 460 mA. It can cuts off the power supply. This optimized regulator is integrated in MIMOSA30. The simulation results show a dropout voltage of lower than 200 mV is achieved. The PSR performance is also better. The measurement results are still expected.

The power distribution strategy for CPS is researched. Since the serial powering is not compatible with the recent design of CPS, the DC-DC conversion is proposed to be used. A step-down DC-DC converter supplies power for several sensor chips. Then the relative high output voltage enters the power management of CPS. The analog supply voltage and digital supply voltage are generated by the low dropout regulator and switched capacitance converter, respectively. Since the analog circuit is sensitive to the noise, the local regulator is employed to decrease the switching noise. In order to increase the power efficiency, the switched capacitance converter is used. Different with the consumer electronics, CPS is limited by the fabricated process. However, some power management strategies are based on the process. Moreover, the performance is more important than the power consumption for CPS. Thus, the tradeoff between the performance and the power consumption should be considered. A power management based on work states is proposed in CPS. The power supply of the unused blocks are cut off in the steady state.

Future work and perspectives

The future work and perspectives are listed as follows.

- Since the load capacitance and load resistance are estimated value in the design, the RegVdda should be internally connected with the CPS chip to be tested. It is also required by the power management. However, the power wire routing should be analyzed due to the voltage drop on the long wire and the lack of space for wire. The distributed powering is a promising method, in which more than two regulators are utilized to drive the same voltage. Each regulator is placed close to the blocks in order to simplify the routing. One of the problems may be the mismatch among them. Moreover, the stability of regulator should be verified since

the load capacitance and load current vary.

- The switched capacitor converter will be designed for supplying the digital power voltage in the power management. The challenge is that how to decrease and integrate the pump capacitors on-chip. The pump capacitance is inversely proportional to the ripple voltage. Thus, the operation frequency should be increased in order to decrease the pump capacitance under the premise of acceptable ripple voltage.

- The current limiter will be improved to not be influenced by the process fluctuation. Since very large transistors are used as the pass transistors, the radiation tolerance of transistors with very large size will be analyzed and tested.

- The linear regulators designed in this doctoral work are also suitable for other low-noise applications, such as system on chip (SoC), radio frequency (RF) circuits and so forth.

Biography

Mr. Jia Wang was born in Henan Province, P. R. China, in 1985. He received his B.Sc. degree in computer science and technology from Northwestern Polytechnical University, Xi'an, China, in 2006. He jointed the continuous academic program (Master & Doctor) of Northwestern Polytechnical University in 2007. Since October 2009, he has been working toward his Ph.D. degree on microelectronics as a jointed educated student at Northwestern Polytechnical University, Xi'an, China and University of Strasbourg, Strasbourg, France.

From February 2007 to October 2009, he jointed the Engineering Research Center of Embedded System Integration, Ministry of Education, Xi'an, China as an IC designer to develop the GAMMA circuit in the thin-film-transistor liquid crystal display (TFT-LCD) driver. He also designed two power IC circuits and finished the system block design of a CMOS imaging sensor during that period. From October 2009 to now, he jointed the microelectronics group of Institut Pluridisciplinaire Hubert Curien (IPHC), Strasbourg, France as a PhD student. His research interests focus on the design of analog and mixed-signal integrated circuits, the power management design, low noise, low power consumption design for CMOS pixel sensors used in high energy physics experiments.

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