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Development of CMOS Pixel Sensors for the Inner Tracking System Upgrade of the ALICE Experiment

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Résumé en Français

La collaboration ALICE (A Large Ion Collider Experiment: expérience sur un grand collisionneur d'ions) prépare dès maintenant une importante amélioration des performances du détecteur ALICE. La mise à jour du détecteur est prévue pendant la longue période d'arrêt (LS2) de la machine LHC (Large Hadron Collider) en 2018/2019 visant à en augmenter la luminosité d'un facteur 10 par rapport à sa valeur noiminale. Le nouveau programme de physique de l'expérience ALICE impose la mise à jour du trajectometre interne (ITS: Inner Tracking System) qui va permettre de reconstruire les traces des particules chargées à faible impulsion et de déterminer leur point d'origine avec une plus grande précision. Le nouvel ITS va ainsi permettre d'améliorer d'un facteur 3 la résolution sur le point d'impact des particules par rapport à sa version actuelle. Il va devoir également traiter le flux de données très important produit par l'expérience. Face aux limitations des technologies existantes largement utilisées dans les différents trajectometres au LHC parmi lesquelles on peut citer les capteurs en silicium à micro-pistes ou à pixels hybrides, une nouvelle génération de capteurs plus fins et plus granulaires s'avère nécessaire pour réaliser ce défi technologique.

Les capteurs CMOS à pixels (CPS: CMOS Pixel Sensor ou MAPS), initiées par l'IPHC (Institut Pluridisciplinaire Hubert Curien, Strasbourg), sont d'excellent candidats pour ce domaine d'application car ils permettent de combiner granularité, faible épaisseur, tolérance aux radiations et vitesse de lecture. Plus de 30 prototypes de capteurs intitulés MIMOSA (Minimum Ionizing particle MOS Active pixel sensor) réalisés en technologie standard CMOS ont été développés depuis maintenant plus de 10 ans et leurs performances démontrées pour la réalisation de trajectometre de particules chargées. Ainsi, les capteurs ULTIMATE (alias MIMOSA 28), fabriqués en technologie CMOS 0.35 μm, équipe depuis janvier 2014 le détecteur PXL (PIXEL) de l'expérience STAR (Solenoidal Tracker) au RHIC (Relativistic Heavy Ion Collider). Le pixel d'ULTIMATE comprend une diode de collection, un préamplificateur et un cir-

cuit CDS (Correlated Double Sampling: double échantillonnage corrélé). La matrice de pixels est lue ligne par ligne (en mode volet déroulant) pour réduire la consommation. Chaque colonne de pixels se termine par un discriminateur afin de convertir les signaux analogiques issus de la sortie des préamplificateurs en valeur binaire. Les résultats sont ensuite envoyés à la logique de suppression des zéros ("Zero suppression") permettant de réduire le flux de donnée à la sortie du capteur. Le schéma fonctionnel du capteur MIMOSA 28 et l'architecture du pixel sont illustrés par la Fig. 1

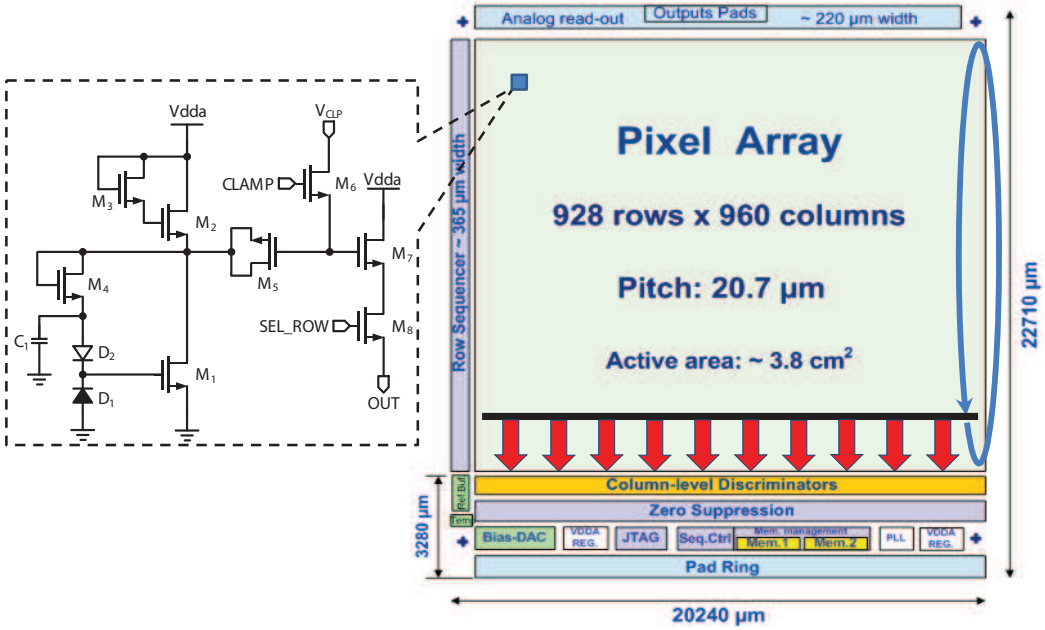


Figure 1: Digramme fonctionnel du capteur MIMOSA 28.

Le nouvel ITS de l'expérience ALICE partage, avec le PXL de l'expérience STAR, un but similaire qui est la reconstruction précise des particules à impulsion faible et de durée de vie courte. Cependant, par rapport au PXL, le nouvel ITS nécessite des améliorations substantielles des performances du capteur, en particulier la vitesse de lecture, la tolérance aux radiations et la puissance consommée.

L'équipe PICSEL (Physics with Integrated Cmos Sensors and ELectron machines) de l'IPHC s'est impliqué activement dans les développements de la nouvelle génération de CPS dédiée à la jouvence de l'ITS d'ALICE. Celle-ci s'appuie sur la technologie CIS (CMOS Image Sensor) 0.18 μm fourni par *TowerJazz*. Les capteurs fabriqués dans cette nouvelle technologie ont montré une meilleure tolérance aux radiations que les capteurs ULTIMATE réalisé dans une technologie CMOS 0.35 μm plus ancienne, satisfaisant déjà une des exigences de l'ITS. En outre, elle permet d'accroître considérablement la

capacité de traitement de signal dans le pixel. En effet, avec sa technologie à quatre puits (quadruple well), elle offre la possibilité d'implémenter des transistors de type P dans chaque pixel sans dégrader la capacité de collection de la diode. Il devient donc possible d'intégrer un discriminateur dans chaque pixel et obtenir un pixel à sortie binaire. Ce faisant, le traitement du signal analogique est contenu dans le pixel et le buffer analogique, qui charge la colonne de sortie sur une longue distance lorsque le discriminateur est en bas de la colonne, peut ainsi être retiré. En conséquence, la consommation de courant statique par pixel sera largement réduite. De plus, en ne devant considérer que les éléments parasites locaux de la chaîne de lecture analogique, le temps de traitement de la ligne peut être potentiellement réduit. À partir de cette étude, une nouvelle génération de prototypes de capteur CMOS à lecture rapide et à faible consommation dénommé AROM (Accelerated Read-Out MIMOSA: MIMOSA avec lecture accélérée) a été développée et est rapportée dans cette thèse. Basé sur ces nouveaux prototypes, le capteur ASTRAL (AROM Sensor for the inner TRacker of ALICE: capteur AROM pour le trajectometre interne d'ALICE) proposé pour la mise à jour de l'ITS d'ALICE devrait permettre de répondre à toutes les spécifications. Afin d'aboutir au capteur final, trois étapes de développement sont menés en parallèle. La première étape, à laquelle se rattache principalement ce travail, consiste à développer, valider et optimiser le concept du capteur CMOS avec l'intégration du discriminateur à l'intérieur du pixel. Différent versions de ce nouveau type de capteur AROM ont ainsi été réalisées. Les deux autres étapes de travail consistent à optimiser le système de détection (la diode de collection et le préamplificateur) et à étudier une logique de suppression des zéros adapté à l'environnement ALICE. Enfin, tous ces efforts se rejoindront pour concevoir le capteur final ASTRAL.

Les études réalisées dans cette thèse

L'objectif de cette thèse est de développer, à partir de plusieurs itérations de prototype du capteur AROM, un capteur qui serait l'élément de base du capteur final et dont les performances prometteuses, pourraient satisfaire pleinement les spécifications du nouvel ITS.

Dans la première partie de la thèse, un premier prototype de petite taille, intitulé AROM-0, a été conçu et fabriqué afin d'étudier la faisabilité de la discrimination de signal dans un petit pixel et d'évaluer ses performances. Dans ce prototype, chaque

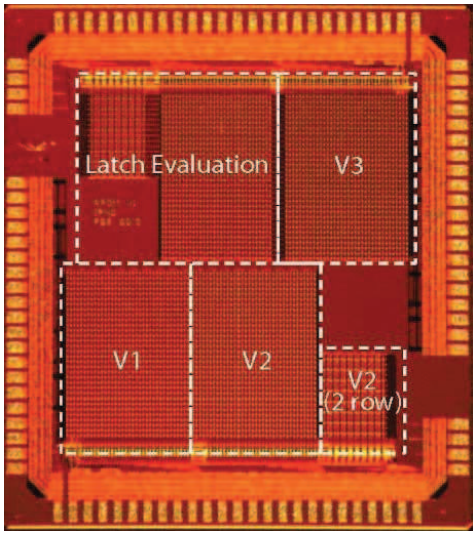


Figure 2: Schéma physique du capteur AROM-0.

pixel de surface 22 μm $\times$ 33 μm contient une diode de détection, un préamplificateur et un discriminateur à tension d'offset compensée. Trois versions différentes de pixels, nommées V1, V2 et V3, ont été implémentées dans des matrices séparées contenant chacune 32 par 36 pixels. Les différences entre ces trois versions de pixels ne concernent que les topologies des discriminateurs. Par rapport au capteur ULTIMATE, le temps de lecture d'une ligne pour le capteur AROM est réduit de moitié passant de 200 ns/ligne à 100 ns/ligne. Sa consommation de courant statique par pixel est également divisée par au moins un facteur deux. Afin d'augmenter encore la vitesse de lecture, le pixel V2 a été implanté dans une matrice de 16 par 18 pixels qui est lue deux lignes par deux lignes. Les mesures en laboratoire ont montré que le bruit ENC (Equivalent Noise Charge) du circuit complet d'un pixel est d'environ 30 e^- pour toutes les versions de pixels. Le discriminateur dans les pixels contribue autant au bruit total que le système de détection. Son bruit en tension est plus de 1 mV. Ce résultat est encourageants pour le premier prototype, mais la performance de bruit doit être améliorée. La distribution de bruit temporel (TN: temporal noise) présente une longue queue vers la valeur haute, ce qui est à cause du bruit télégraphique (RTS noise: Random Telegraph Signal noise) du préamplificateur. La contribution principale au bruit FPN (fixed pattern noise) du circuit complet est due au discriminateur. En raison de la complexité du layout, le bruit FPN pour la matrice avec une lecture par double ligne est plus grand que ce qui est avec une lecture par une seule ligne. La valeur de FPN dépend en grande partie des couplages capacitifs liée aux croisements des pistes dans le layout très dense du

pixel. Des études postérieures ont mis en évidence une source de couplage critique entre un nœud sensible et un signal numérique qui aurait pu être évité par un dessin plus soigneux et par des simulations après routage. A partir des résultats de mesure, deux topologies de discriminateur ont été sélectionnés pour le développement suivant.

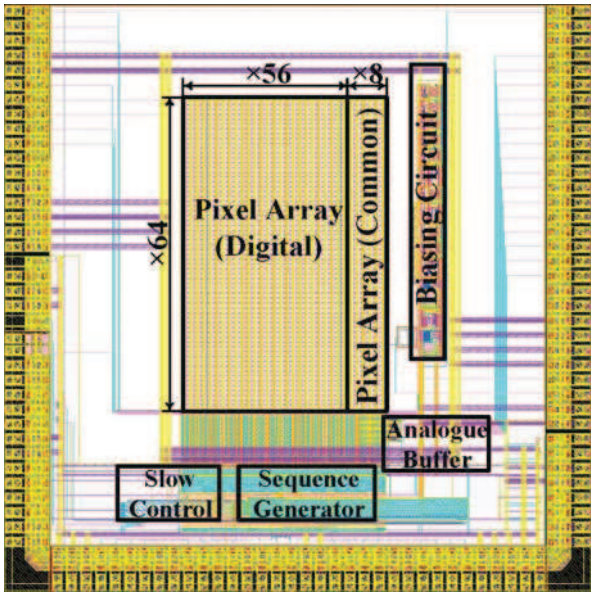


Figure 3: Schéma physique du capteur AROM-1.

La deuxième partie de la thèse débute par l'analyse du bruit temporel des deux versions de pixel sélectionnées dans AROM-0. Cette étude a montré que le pixel V1 dans AROM-0 aurait un bon potentiel pour un fonctionnement à faible bruit à condition que de légères modifications soient apportées. Ensuite sera détaillé le développement des capteurs AROM-1. Ce sont les capteurs intermédiaires vers le capteur final ASTRAL. Ils ont deux objectifs principaux, l'un est de valider les optimisations de conception du pixel et l'autre est de mettre en place une architecture du capteur évolutive intégrant l'intelligence nécessaire dans le circuit. Comme l'illustre la Fig. 3, chaque AROM-1 contient une matrice de 64 × 64 pixels qui est lue deux lignes par deux lignes. Les DACs (Digital to Analog Converter: Convertisseur numérique-analogique) de référence et le générateur de la séquence de lecture sont intégrés sur la périphérie du circuit; tous sont programmables à travers des registres JTAG (Joint Test Action Group) embarqués. La série de capteurs AROM-1 comporte cinq versions qui ont été réparties en deux groupes: le premier comprend les circuits AROM-1 A/B/C intégrant des pixels dérivés d'AROM-0 V2 ; le second comprend les circuits AROM-1 E/F incorporant des

pixels dérivés d'AROM-0 V1. Les variantes de pixel à l'intérieur d'un même groupe se différencient les unes des autres par le pas du pixel aussi bien que par le placement des composants et le routage des signaux dans le dessin du pixel. Tous les circuits ont été testés en laboratoire. L'utilisation d'une couche épitaxiée de haute résistivité dans AROM-1 a permis d'obtenir une plus grande efficacité de collection de charges. En outre, l'augmentation des dimensions des transistors d'entrée des préamplificateurs a contribué à la réduction du bruit RTS observé dans AROM-0. Le discriminateur implémenté dans AROM-1 E s'est montré le plus prometteur et a donc été choisi comme référence pour les développements à venir. Le circuit AROM-1 E est composé de pixels ayant le même pas que celui d'AROM-0. Le discriminateur, basé sur la topologie d'AROM-0 V1, a été optimisé afin de le rendre bas bruit et faible consommation. Le courant statique par pixel d'environ 18 μA est beaucoup plus faible que celui consommé par le pixel d'AROM-0. Le bruit total du discriminateur d'AROM-E mesuré à 0.33 mV est significativement plus faible que celui de la génération précédente. Le bruit ENC de la chaîne complète du pixel, de l'ordre de 20 e^-, est principalement dominé par la contribution du système de détection. S'appuyant sur le pixel d'AROM-1 E, AROM-1 F intègre une autre variante de discriminateur qui minimise la consommation en relaxant la contrainte sur les performances de bruit. Le pas du pixel d'AROM-1 F est de 27 μm $\times$ 27 μm pour lequel on s'attend à une résolution spatiale similaire au pixel de pas 22 μm $\times$ 33 μm. Le bruit du discriminateur d'AROM-1 F est mesuré à 0.42 mV avec un courant statique par pixel inférieure à 15 μA.

Conclusions et perspectives

Le nouvel ITS de l'expérience ALICE sera équipée avec des capteurs CPS. Le capteur ASTRAL proposé par l'IPHC représente l'une des solutions pour cette application. Dans cette thèse, plusieurs variantes de capteurs incorporant la discrimination de signal à l'intérieur du pixel ont été développées dans une technologie CIS 0.18 μm à quatre puits et sont les précurseurs d'ASTRAL. Les résultats de bruit très prometteurs du discriminateur dans le pixel combiné à une très faible consommation ont été démontrés dans les capteurs AROM. Par rapport à l'architecture de CPS classique comprenant une discrimination du signal en bas de la colonne, le capteur AROM ouvre des perspectives intéressantes en termes d'augmentation de la vitesse de lecture et de réduction de la consommation qui permettent d'approcher de très près les spécifications de l'ITS.

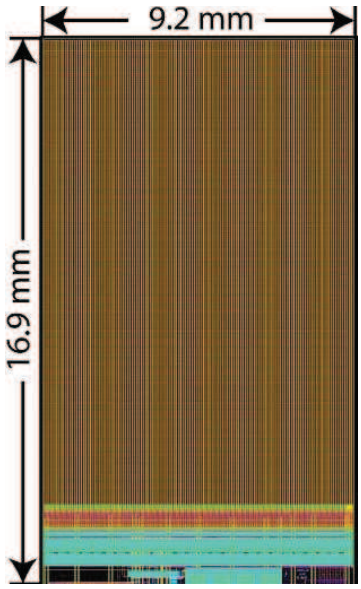


Figure 4: Schéma physique du capteur FSBB-A0.

L'élément de base pour le capteur ASTRAL, appelé FSBB-A (full scale building block for ASTRAL), a été construit en étendant l'architecture du capteur AROM-1 à une matrice de pixels pleine échelle occupant ainsi une surface sensible supérieure à 1 cm^2 et en intégrant la logique de suppression des zéros. Le capteur final ASTRAL sera composé de trois FSBB-A fonctionnant en parallèle et multiplexés au niveau de leurs noeuds de sortie. La Fig. 5 en donne un schéma fonctionnel du capteur ASTRAL.

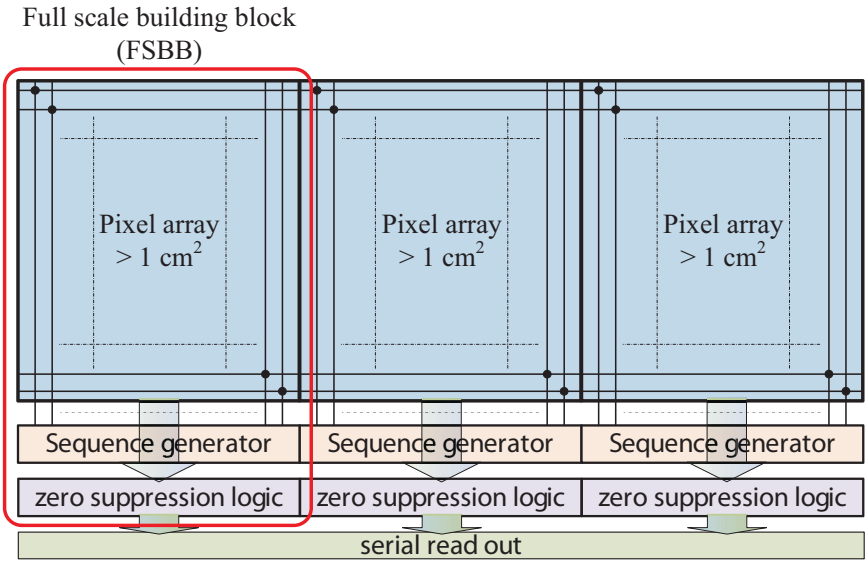


Figure 5: Digramme fonctionnel du capteur ASTRAL.

Pour la suite de cette thèse, plusieurs questions concernant le capteur AROM doivent encore être résolus, notamment comprendre le faible rendement et l'absence des tensions de référence dans les capteurs AROM-1 et le capteur FSBB-A. En parallèle avec le développement d'ASTRAL, une autre architecture de CPS, également dédié au nouvel ITS, et comprenant un mode de lecture guidée par les données a été étudiée dans les prototypes ALPIDE (ALICE PIxel DEtector) conçus au CERN. Les capteurs ASTRAL et ALPIDE, tirant profit de l'évolution de la technologie CMOS, ont confirmé le potentiel des CPS qui ont été choisis pour la mise à jour de l'ITS d'ALICE ainsi que pour de nombreux autres projets à venir, comme par exemple le détecteur de vertex de l'ILC (International Linear Collider).

Introduction

The ALICE collaboration is preparing for a major upgrade of its apparatus during the second long shut down of LHC (LS2) in the years 2018/2019. The proposed physics programs at ALICE require a new Inner Tracking System (ITS) with enhanced low-momentum vertexing and tracking capabilities, and at the same time allowing data taking at a substantially higher rate. Existing sensor technologies like microstrip detectors and hybrid pixels, which have been extensively employed in various experiments at LHC, are inadequate for this application. Therefore, a new generation of sensors, which would be much thinner and more granular than those in use, are required to equip the new ITS.

CMOS pixel sensors (CPS), pioneered at IPHC (Institut Pluridisciplinaire Hubert Curien, Strasbourg), are very attractive for this kind of applications, where the physics driven performances are privileged while relatively less stringent radiation tolerance and read-out speed are required. During the last fifteen years, more than 30 different MIMOSA (Minimum Ionizing particle MOS Active pixel sensor) prototypes have been developed by using the standard CMOS processes, in order to demonstrate their capability for charged particle tracking and to optimize their performances. The ULTIMATE sensor (alias MIMOSA 28), fabricated in a 0.35 μm CMOS process, has been successfully used to equip the STAR (Solenoidal Tracker At RHIC) PIXEL detector (PXL). And it is the first vertex detector using CPS. The pixel of the ULTIMATE sensor contains a sensing diode, a pre-amplifier and a CDS element. The pixel array is read out row by row (the so called rolling-shutter read-out mode). Each pixel column is terminated by a discriminator to convert the analogue signals from the pixels into binary values. Then, these binary values are sent to a zero-suppression logic to reduce the data flow for serial output. The ALICE-ITS upgrade and the STAR-PXL detector are conceived with a similar purpose of accurately reconstructing the short lived and low momentum particles. This greatly encourages the use of CPS in the upgrade

ALICE-ITS. However, as compared to the STAR-PXL detector, the ALICE-ITS upgrade calls for some substantial improvements on the sensor performances, especially on read-out speed and radiation tolerance.

In order to break the limitations of the ULTIMATE sensor, a 0.18 μm CMOS Image Sensor (CIS) process, provided by *TowerJazz*, was explored at IPHC. As compared to the 0.35 μm process used for the ULTIMATE sensor, the CPS fabricated in the new process is more radiation tolerant, satisfying the requirement of the ALICE-ITS upgrade. In addition, the new process can greatly enhance the in-pixel signal processing capability, thanks to the innovative deep P-wells. Therefore, it is possible to place a discriminator inside each pixel, achieving a fully digital output pixel. By doing this, the strong analogue buffer, used in the conventional analogue pixel to drive the long distance column line, is removed. Thus, the power consumed for analogue readout and A-D conversion can be largely reduced. Moreover, by dealing with only the small local parasitics in the analogue readout chain, the row processing time can be potentially decreased.

In this thesis, the concept of in-pixel discrimination, was realized in the AROM (Accelerated Read-Out MIMOSA) prototypes by employing the 0.18 μm process. After several iterations of prototyping the AROM sensors, a scalable CPS, with promising performances fully adapted to the ALICE-ITS upgrade, has been achieved. The thesis is organized as follows,

Chapter 1 introduces briefly the scientific motivation for the upgrade of the ALICE-ITS, addresses the limitations of the current ITS and gives an overview of the new ITS. Several silicon based detector technologies, that are currently mature enough for high energy physics experiments, are reviewed, among which the CMOS pixel sensor steps up as the most promising solution for this particular application.

Chapter 2 presents the basic physics principles of charge generation in materials after a passage of an ionizing particle, with an emphasis on silicon devices. The detection principle of the CMOS pixel sensor and its prominent features for charged particle detection are described. Then, the radiation induced effects, deteriorating the detector performance, are briefly reviewed. And the mechanisms of various internal electronic noise are presented. The chapter ends with the introduction of the global read-out architecture for a typical rolling shutter CMOS pixel sensor, which provides a great solution for high speed applications.

In Chapter 3, the state-of-the-art CPS, called ULTIMATE, is first introduced as

the starting point for the ALICE pixel chip development. It is followed by a summary of some recent developments of the CPS based on a new 0.18 μm quadruple-well CMOS process, directing the CPS to accommodate the requirements of the ALICE-ITS upgrade. Then, the roadmap towards the final sensor we have proposed for the ALICE-ITS upgrade, named ASTRAL (AROM Sensor for the inner TRacker of ALICE), is described.

The major part of this work follows the roadmap introduced in Chapter 3 and deals with the design of rolling shutter CMOS pixel sensors with in-pixel signal discrimination. As compared to the former CPS, with the signal discrimination performed at the column level, the sensors developed in this work can achieve a higher read-out speed, with a significantly reduced power consumption. Chapter 4 presents the design of the prototype chip named AROM-0, which contains several test structures to study the feasibility to realize the signal discrimination with a small pixel pitch, i.e. 22×33 μm^2. The measurement using a ^{55}Fe source and the noise evaluation using the "S" curve method are presented. Some improved pixel designs are integrated in a series of more advanced prototype chips named AROM-1. The AROM-1 sensor incorporates a larger pixel array and more periphery intelligence with respect to the AROM-0 prototype. Chapter 5 describes in detail the design and laboratory measurement results of those AROM-1 chips.

This work concludes in Chapter 6. The FSBB-A0 sensor, which is the first full-scale building block composing one third of the ASTRAL sensor, is introduced. Issues found in this work, which need to be addressed in the future, are discussed. Perspectives for using CPS in HEP (High Energy Physics), and their potential for applications beyond the HEP are presented.

Chapter 1

The ALICE-ITS upgrade

ALICE (A Large Ion Collider Experiment) [1] is a general-purpose, heavy-ion experiment at the CERN LHC (Large Hadron Collider)—the world's largest and most powerful particle accelerator. It is designed to study the physics of strongly interacting matter at extreme values of energy density and temperature in nucleus-nucleus collisions, where a phase of matter called quark-gluon plasma (QGP) forms.

Prior to the start-up of the LHC heavy-ion program, efforts were made at CERN SPS (Super Proton Synchrotron) and at BNL RHIC (Relativistic Heavy Ion Collider), revealing the nature of the QGP as almost "perfect" liquid [2–6]. ALICE has confirmed the RHIC observations and provided additional evidence of the existence of the QGP at the new energy regime [7], with the precision of measurements and kinematic reach exceeding those previously obtained for all significant probes of the QGP.

With the High Luminosity upgrade for the LHC (HL-LHC) after the second long shutdown (LS2) in 2018, it will be possible to achieve the luminosity to the order of at least L = 6×10^{27} $\mathrm{cm}^{-2}\mathrm{s}^{-1}1$, with Pb beams reaching an interaction rate of about 50 kHz [8]. In order to fully exploit the scientific potential of the new LHC running conditions and to enhance the physics capabilities, the ALICE collaboration has devised a comprehensive upgrade strategy, enabling a detailed and quantitative characterization of the QGP with high statistics and high precision measurements [9–12].

The major goals of the proposed upgrade are:

- To increase the experiment's data-taking capabilities by at least an order of magnitude;

- To extend the momentum reach at low transverse momenta (e.g., signals like low-mass di-leptons,);

- To open the possibility to study previously inaccessible rare probes (e.g., Λ_c and Λ_b).

Such a program relies on a new Inner Tracking System (ITS) with a significantly lower material budget and largely improved tracking and vertexing capabilities [13]. This is where the CMOS[1] pixel sensors fit in, and this thesis is devoted to the development of CMOS pixels sensors adapted to the new ALICE-ITS.

In this chapter, a brief introduction to the current ALICE-ITS and its limitations are first given. Then, the new requirements imposed on the upgraded ITS are outlined. After that, an overview of the expected new ITS, together with the general requirements on the sensor chip, is presented. Several silicon detector technologies, that are currently mature enough to be readily used in high energy particle experiments, are introduced. It can be seen that among the various detector technologies, CMOS pixel sensors will provide the most promising solution for the ALICE-ITS upgrade.

1.1 The present ALICE ITS and its limitations

The ITS is a detector system installed at the heart of ALICE. Its main functions are

- reconstruction of the primary and secondary vertices;

- reconstruction of low-p_T tracks that do not reach the ALICE Time Projection Chamber[2] (TPC);

- reconstruction of high-p_T tracks that are lost inside the dead zones between the TPC sectors.

[1] CMOS stands for Complementary Metal–Oxide–Semiconductor. It is a commonly used technology for constructing integrated circuits

[2] The Time Projection Chamber (TPC) is the main tracking detector in the central barrel of the ALICE experiment at LHC. Its function is to provide track finding (efficiency larger than 90 %), charged particle momentum measurement (resolution better than 1 % for pions at about 1 GeV/c), particle identification (dE/dx resolution about 5.5 % in the non-relativistic region and statistically on the dE/dx relativistic rise up to p_T of a few tens of GeV/c), and two-track separation (resolution in relative momentum below 5 MeV/c) in the region $p_T < 10$ GeV/c and pseudo-rapidity $|\eta|<0.9$. [14]

It also aims to improve the momentum and angle resolution for particles reconstructed by the TPC. In addition, it contributes to the particle identification at low momenta (< 200 MeV/c) [15].

1.1.1 Overview of the current ALICE ITS

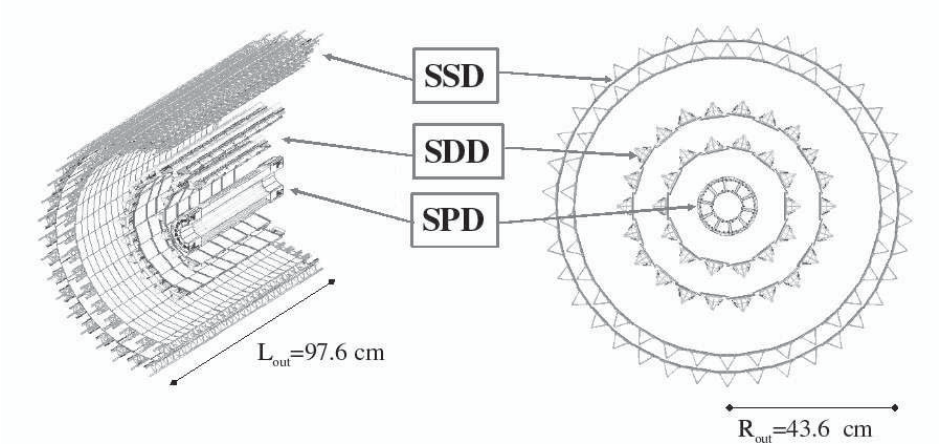


Figure 1.1: The layout of the current ALICE ITS. (Source [15])

The current ALICE ITS, as shown in Fig. 1.1, consists of six cylindrical layers of silicon detectors coaxially surrounding the beam pipe, located at radii between 39 mm and 430 mm. They cover the pseudo-rapidity[3] range $|\eta| < 0.9$ for vertices located within $z = \pm 60$ mm with respect to the nominal interaction point. The innermost radius is the minimum allowed to approach the beam pipe, and the outermost one is determined by the track matching with the TPC. In order to achieve the required impact parameter[4] resolution and to cope with the high particle multiplicities expected in heavy-ion collisions at LHC (the system is designed for up to 100 particles per cm^2 for the inner layer [16]), the first two layers are composed of Silicon Pixel Detectors (SPD) using the hybrid detector technology. The two middle layers are made of Silicon Drift Detectors (SDD) which can provide truly two-dimensional information with only one dimensional readouts, however, at the expense of speed [17]. The two outer layers,

[3]In experimental particle physics, pseudo-rapidity, η, is a commonly used kinematics variable describing the angle of a particle relative to the beam axis. It is defined as $\eta \equiv -ln[tan(\frac{\theta}{2})]$, where θ is the angle between the particle three-momentum P and the positive direction of the beam axis.

[4]The impact parameter of a track is defined as the distance of closest approach of the track to the interaction vertex. The two projections of the impact parameter, in the transverse plane and along the beam direction, are usually considered separately.

Table 1.1: Characteristics of the current ITS.

Layer/Type	r (cm)	± z (cm)	area (m^2)	Intrinsic resolution (rϕ - z) (μm)	$\%X/X_0$
1/Pixel	3.9	14.1	0.07	12 - 100	1.14
2/Pixel	7.6	14.1	0.14	12 - 100	1.14
3/Drift	15.0	22.2	0.42	35 - 25	1.13
4/Drift	23.9	29.7	0.89	35 - 25	1.26
5/Strip	38.0	43.1	2.20	20 - 830	0.83
6/Strip	43.0	48.9	2.80	20 - 830	0.83

where the track density decreases significantly compared to the inner layer (below one particle per cm^2), are equipped with double-sided Silicon Strip Detectors (SSD). The four outer layers have analogue readout and therefore can be used for particle identification (PID) via dE/dx measurement in the non-relativistic ($1/\beta^2$) region. With careful optimization for each detector element, the ALICE ITS currently has the lowest material budget among various experiments at LHC, achieving between 0.8 % and 1.3 % of X_0[5] per detector layer (in particular, 1.14 % of X_0 for the SPD layer). Combining the thermal shields and supports inserted in between each group of two detector layers with the same technology, the total material budget for tracks perpendicular to the detector surface amounts to 7.63 % of X_0. Table 1.1 summaries the main characteristics of the current ITS [1, 18].

1.1.2 The limitations of the current ALICE ITS

At mid-rapidity $|\eta|<0.9$, the ITS is the key ALICE system for detecting particles containing heavy quarks. It is capable to precisely isolate the secondary decay vertices from the primary interaction vertex. The production of heavy flavour particles can therefore be studied by reconstructing their decays with a typical mean proper decay length ($c\tau$) on the order of 100 - 300 μm [19].

With the current ITS, the impact parameter resolution in the transverse plane ($r\phi$) at $p_T > 1$ GeV/c is better than 75 μm for pp collisions [20], and better than 65 μm in the Pb-Pb case [21]. This precision is adequate to study the production of charm

[5]Radiation length, X_0, is a characteristic of a material, related to the energy loss of high energy particles due to electromagnetic interactions with that material. It is defined as the mean distance over which a high-energy particle loses all but 1/e of its energy. Typically, the radiation length is multiplied by the material density, and so the X_0 is measured in g·cm^{-2}

mesons in exclusive decay channels (e.g. $D^0 \rightarrow K\pi$ and $D^+ \rightarrow K\pi\pi$) at transverse momentum values down to 2 GeV/c. However, at lower transverse momenta, the large combinatorial background leads to poor statistic significance of the measurement. The challenge is even greater for charm baryons, given that the most abundantly produced charm baryons (Λ_c) have a mean proper decay length of only 60 μm, which is lower than the impact parameter resolution of the present ITS in the transverse momentum range where the majority of Λ_c daughter particles is produced. For the same reasons, the study of beauty mesons, beauty baryons, and of hadrons with more than one heavy quark cannot be addressed by the current ITS [16].

Another crucial limitation of the current ITS comes from its incapability of high rate readout. Mainly constrained by the SDD layers, the current ITS can run maximumly at a rate of about 1 kHz, assuming a dead time close to 100 % [18, 22]. As previously mentioned, the ALICE upgrade strategy is based on the assumption that the LHC will increase the Pb-Pb interaction rate eventually to about 50 kHz after LS2. The present ITS is clearly inadequate to fulfill the required rate capabilities envisaged for the ALICE long-term plans.

1.2 The requirements of the ALICE ITS upgrade

A detailed discussion of the proposed program at the upgraded ALICE experiment can be found in the Letter of Intent (LoI) [18]. The main physics motivation for the upgrade of ALICE ITS is to perform new measurements on heavy flavour (for charm and beauty separately) and low-mass dilepton production in heavy-ion collisions, which address important questions about the QGP properties that cannot be answered with the present experimental setup . In order to achieve the mentioned goals, as is discussed in [16, 23], the upgraded ITS detector should:

- allow for improving the resolution of the track impact parameter by a factor of three or better (at $p_T = 1$ Gev/c), with respect to the present ITS;
- have stand-alone tracking capability with a momentum resolution of a few percent up to 20 GeV/c, and with coverage in transverse momentum as wide as possible, in particular down to very low momentum;
- have an improved read-out rate capability to exploit the expected Pb-Pb interaction rate of up to 50 kHz.

The targeted new performance calls for an ultra thin detector with high granularity, fast readout and low power consumption. Besides, the detector should also stand the radiation environment it is exposed to. Achieving all these goals simultaneously is not a trivial task, since they often come in contradiction. The high granularity and fast readout tend to compete with each other, and both of them will increase the power consumption. An increased power consumption, on the other hand, will complicate the cooling system, leading to more material in the detector. Below, we will discuss these detector specifications in detail.

Granularity The granularity of the sensor segmentation determines the intrinsic spatial resolution of the reconstructed track points. Assuming a randomly distributed track points, the intrinsic spatial resolution for a binary encoded detector can be estimated as by [24]

$$\sigma = d/\sqrt{12} \tag{1.1}$$

where d is the dimension of the segments in a given direction. However, the signal generated by an impinging particle might be shared by several neighboring segments that form a cluster. By taking advantage of this phenomenon, the spatial resolution can be further improved when certain algorithms (e.g., center of gravity) are used to estimate the hit position from the geometry of the cluster. For example, a pixel senor called ULTIMATE [25], fabricated in a standard 0.35 μm CMOS process, can provide a spatial resolution better than 4 μm in both directions with a pixel size of 20.7 μm $\times$ 20.7 μm.

In high momentum range, where the effect of multiple scattering becomes negligible, the impact parameter resolution depends mainly on the spatial resolution of the first detection layer and its radial distance from the main interaction vertex. Moreover, due to the high track densities, a small segmentation for layers close to the interaction point is necessary to keep the occupancy at a low level. For outer layers, a good resolution is also important to improve the momentum resolution and the tracking efficiency in the ITS stand-alone mode.

The design goal of the ITS upgrade is to have pixels with the same granularity for all the detection layers, achieving an intrinsic resolution of (5 μm, 5 μm) in $r-\phi$ and z respectively. This implies a pixel size on the order of 20 μm $\sim$ 30 μm in both directions. However, studies have shown that having a lower granularity for the outer layers is still acceptable [16, 23].

Thickness Particles passing through matter suffer repeated elastic Coulomb scattering from nuclei. As a result, particles are deflected from their original trajectory after traversing a certain thickness of material. Reducing the overall material budget ensures that the particles traversing the detector are less affected by multiple Coulomb scattering, and allows for a significant improvement in the tracking performance and momentum resolution. Therefore, in order to precisely reconstruct the secondary decay vertices at low momenta, an outstanding spatial resolution has to be complemented by very light and thin first detection layers.

The anticipated material budget of the new ITS is 0.3% of X_0 for the inner layers and 0.8% of X_0 for the outer layers (silicon chip + flex cable + power distribution + cooling + supporting structures). Currently, the SPD equipping the innermost layer of ALICE ITS, taken alone, has a thickness of 350 μm (200 μm sensor + 150 μm readout ASIC[6]), contributing already a material budget of more than 0.3 % of X_0. Therefore, a new sensor chip, with a thickness much lower than that in use, needs to be developed.

Speed The new detector aims to cope with the interaction rate up to 50 kHz for Pb–Pb collisions and 200 kHz for pp collisions. The high interaction rate implies a high time resolution in order to prevent significant losses of reconstruction efficiency because of pile-up effects. With a 50 kHz interaction rate and 20 μs (30 μs) integration time, about one (two) extra Pb-Pb collision will on average be read-out on top of the triggered event. A certain amount of pile-up can be tolerated, since the global ALICE tracking can often separate hits from tracks belonging to different events based on the information coming from other detectors. As a design goal, the integration time for the inner layers with high occupancy is expected to be $\lesssim 30$ μs to limit pile-up effects and a consequent loss of tracking efficiency. For outer layers where occupancy is relatively low, the speed requirement is less stringent. However, a similar time resolution is still desirable to facilitate the cluster matching throughout the whole detector.

Power consumption The material budget is dictated not only by the thickness of the sensor, but also by the services (e.g., mechanical support, read-out system, power distribution, cooling system). The maximum tolerable material budget puts severe limitations on the amount of material that can be used for power distribution and detector cooling. Thus, the power consumption of the sensor must be well controlled.

[6] ASIC stands for Application-Specific Integrated Circuit. It is an integrated circuit (IC) customized for a particular use, rather than intended for general-purpose use

In order to comply with the material budget requirement as mentioned previously in this section, the power density on the sensor should not exceed 300 mW/cm^2 for the inner layers and 100 mW/cm^2 for the outer layers.

Radiation tolerance In order to address the physics program proposed for the ALICE upgrade, an integrated luminosity of 10 nb^{-1} is required for Pb-Pb collisions, inspecting about 10^{11} interactions. This will allow ALICE to gain a factor of 100 in statistics for minimum bias data with respect to the current program up to LS2. As for the measurements that are currently based on rare triggers, the increase in statistics will be of one order of magnitude. Together with the foreseen integrated luminosities of 6 pb^{-1} for pp collisions and 50 nb^{-1} for p-Pb collisions as reference data, the corresponding radiation dose expected at the innermost layer for the full upgraded physics program is up to 2700 krad[7] of Total Ionizing Dose (TID) and 1.7×10^{13} 1 MeV n_{eq}/cm^2 of Non-Ionizing Energy Loss[8] (NIEL), including a safety factor of ten [16,26,27]. Under these radiation conditions, the sensor must maintain full functionality and avoid any significant performance degradation.

1.3 Overview of the new ITS

Table 1.2: Design parameters of the upgraded ITS.

Layer	r (mm)	z (mm)	Pseudo-rapidity coverage[a]	Active area (cm^2)	$\%X/X_0$
0	24.55	271	± 2.5	421	0.3
1	32.35	271	± 2.3	562	0.3
2	39.95	271	± 2.0	702	0.3
3	196.05	843	± 1.5	10483	0.8
4	245.45	843	± 1.4	13104	0.8
5	343.85	1475	± 1.4	32105	0.8
6	393.35	1475	± 1.3	36691	0.8

[a]The Pseudo-rapidity coverage of the detector layers refers to tracks originating from a collision at the nominal interaction point (z=0).

[7]The rad is a deprecated unit of absorbed radiation dose, defined as 1 rad = 0.01 Gy = 0.01 J/kg. The gray (Gy) is the SI unit. However, rad is sometimes also used

[8]Non-Ionizing Energy Loss expresses energy lost to non-ionizing events per unit length, normalized to 1 MeV neutron

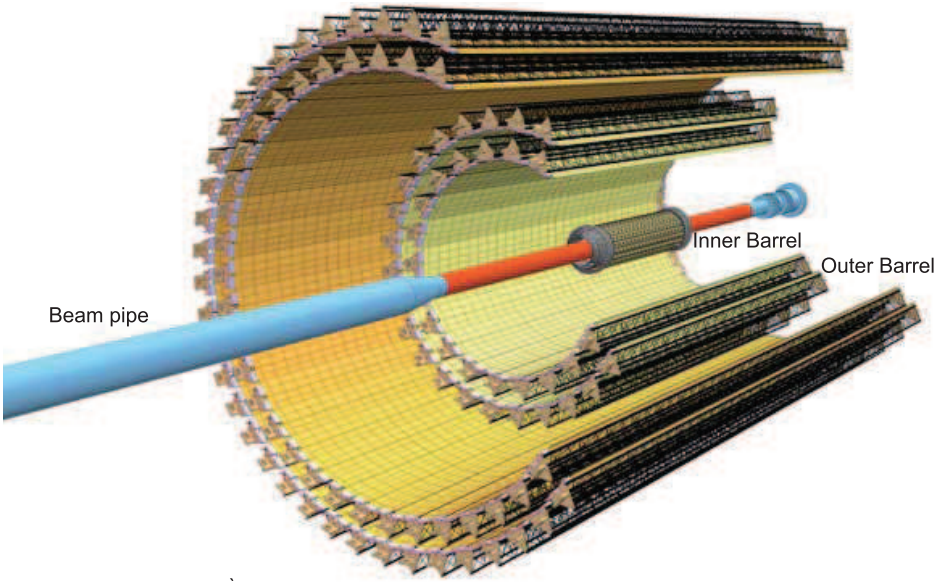


Figure 1.2: The layout of the new ALICE ITS.(Source [16])

The upgrade strategy of the ALICE experiment includes a new beampipe with smaller diameter. It will allow for installing the innermost detection layer much closer to the beam line as compared to the current ITS, thus improving the impact parameter resolution. Based on the available space between the new beam pipe and the outermost radius of the current ITS, the number of detection layers and their radial positions were tuned to obtain the optimal combined performance in terms of pointing resolution, p_T resolution and tracking efficiency. As shown in Fig. 1.2, the upgraded ITS will fully replace the present one with seven layers of pixel detectors, grouped in two separate barrels, the Inner Barrel (IB) consisting of the three innermost layers and the Outer Barrel (OB) with the four outermost layers. Each layer is segmented azimuthally into units called Staves. Each Stave consists of a space frame made of carbon fiber, which provides mechanical support to the Stave, and a cold plate made of carbon ply, which embeds the cooling pipes. The pixel chips are glued on the cold plate and laser soldered over a Flexible Printed Circuit (FPC). In the OB, the Staves are further segmented in azimuth in two halves, each of which is segmented longitudinally in modules glued on a common cooling unit. Each module consists of a number of pixel chips bonded on an FPC. The Staves for the Inner Barrel and the Outer Barrel are schematically shown in Fig. 1.3, and the overall characteristics of the ITS upgrade are summarized in Table 1.2.

Based on this upgrade scenario and combined with the discussion in Section 1.2,

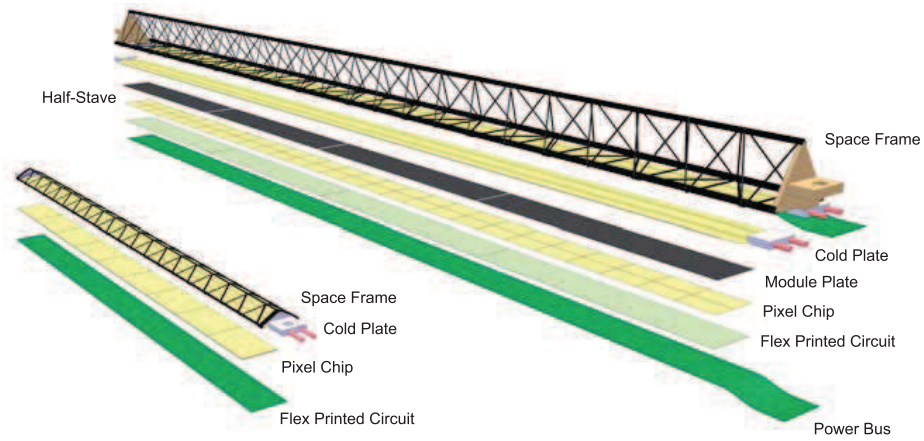


Figure 1.3: Schematically drawing of the Inner Barrel (left) and the Outer Barrel (right) Staves.(Source [16])

the general requirements for the pixel chip equipping the new ITS are summarized in Table 1.3. Because the main challenge is imposed on the pixel detector for the Inner Barrel, this thesis focuses primarily on the development of CMOS pixel sensors satisfying the inner barrel requirements.

Table 1.3: General requirements on the pixel detector.

Parameter	Inner Barrel	Outer Barrel
Max. silicon thickness	50 μm	
Intrinsic spatial resolution	5 μm	10 μm
Chip size	15 mm $\times$ 30 mm ($r\phi \times z$)	
Max. dead area on chip	2 mm ($r\phi$), 25 μm (z)	
Max. power density	300 mW/cm^2	100 mW/cm^2
Max. integration time	< 30 μs	
Min. detection efficiency	> 99 %	
Max. fake hit rate	$< 10^{-5}$	
TID radiation hardness[a]	2700 krad	100 krad
NIEL radiation hardness[a]	1.7×10^{13} 1 MeV n$_{eq}$/cm^2	10^{12} 1 MeV n$_{eq}$/cm^2

[a] $10 \times$ radiation load integrated over approved program ($\sim$ 6 years of operation). [27]

1.4 Silicon detector technologies

In general, silicon detectors work as ionization chambers with patterned detector electrodes inducing electric field in the medium. Absorbed radiation liberates charge carrier pairs, i.e. electrons and holes, which are separated in the electric field and induce signal currents that can be read out by the front-end circuitry. Due to their excellent energy and spatial resolution and a small amount of required material, silicon based detectors have been widely used in high energy physics (HEP) experiments near the primary vertex, in form of microstrip or pixel detectors [28, 29].

Since their first introduction to HEP just over thirty years ago, the use of silicon detectors has expanded following a version of Moore's law in terms of both covered surface and number of readout channels [30]. Several silicon detector technologies have been well established, following the advancing physics needs addressed in various HEP experiments. They include the charged couple devices (CCDs), microstrip detectors, hybrid pixel detectors and CMOS pixel sensors. However, as discussed in the previous section, to develop a sensor satisfying all the requirements of the new ALICE-ITS is a real challenge. As a matter of fact, none of the detectors currently in commission is suitable to equip the new ITS directly, which implies that some substantial advancements in the existing sensor technologies are needed.

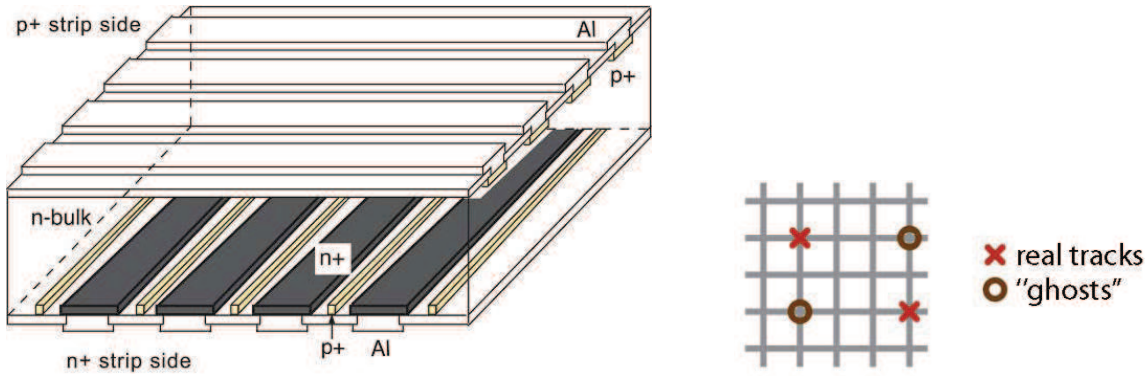
The CCD was introduced in 1970 [31]. It is a major piece of technology in digital imaging. The idea of using CCDs in a vertex detector was first realized in a fixed target experiment at CERN SPS [32], and then followed by SLD at SLAC [33]. The CCDs provide thin detectors with very high granularity. However, attributed to their charge transfer machanism, they are inherently sensitive to radiation damage and reading out a large sensor takes a significant amount of time. These limitations have excluded the CCDs as an option for the ALICE-ITS upgrade. Therefore, the following parts of this section focus on the other three technologies mentioned above, and it will eventually become clear that the CMOS pixel sensor seems to be the most promising solution for this particular application.

1.4.1 Microtrip detectors

Silicon microstrip detectors were first used in HEP experiments, as the position sensitive detector, in early 1980s [34]. Since then, they have become the most widely used silicon detectors in HEP experiments where a high-precision tracking is required.

A microstrip detector is an arrangement of strip shaped implants, placed on a low doped fully depleted silicon wafer. These implants, typically 10 - 50 μm wide and a few centimeters long, form a one-dimensional array of diodes acting as charge collection electrodes. The read-out electronics, located aside the sensor, can be connected to the strips by either a direct current (DC) coupling or an alternating current (AC) coupling way. Depending on the actual detector geometry, and the algorithm used for processing signals from the detector, the spatial resolution of a single plane detector can be as good as a few micrometers in one dimension.

A more sophisticated design, allowing for two-dimensional position measurements on a single detector, can be achieved by applying an additional strip like doping on the wafer backside. Fig. 1.4(a) gives an example of a double-sided microstrip detector. It includes orthogonally implanted N and P strips on both sides of the detector.



(a) (b)

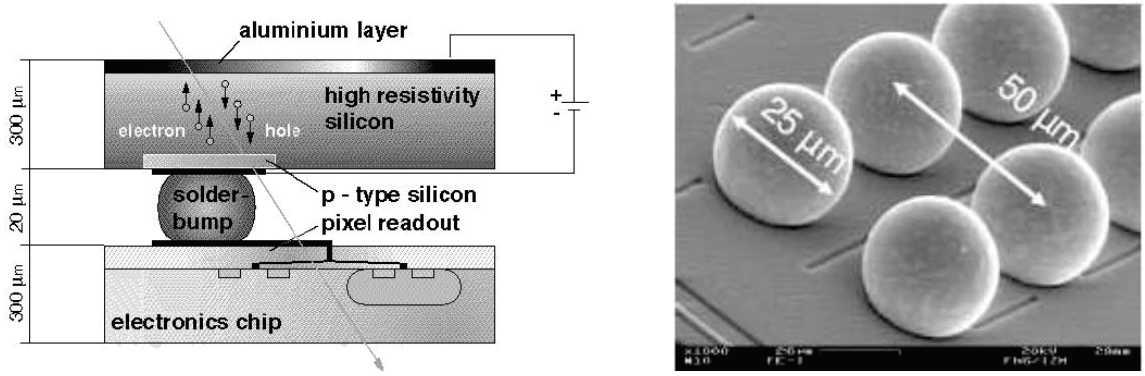
Figure 1.4: (a) The double-sided strip detector. (b) True hits and ghost hits in double-sided strip detectors in case of two particles traversing the detector.

However, if there are multiple events within one readout period, a strip detector is not able to assign the hit positions unambiguously. As illustrated in Fig. 1.4(b), in case of two particles traversing a double-sided strip detector, two ghost hits are generated, confusing the track reconstruction. The ambiguities can be reduced by decreasing the stereo angle. As the case of the SSDs equipping the current ALICE-ITS, the strips on the two sides form a stereo angle of 35 mrad. Nevertheless, strip detectors are not suitable for the environment with high particle density. In addition, small values of the stereo angle significantly decrease the spatial resolution in the direction perpendicular to the strips. In the ALICE experiment, pixel detectors are mandatory for layers close

to the interaction point. As for layers located relatively far from interaction point, where particle density drops to an affordable value, using strip detectors is still an option. In addition, the strip detectors can provide the analogue information used for particle identification.

1.4.2 Hybrid pixel detectors

Hybrid pixel detectors represent a well-known technology with proven radiation hardness compatible with the requirements of various experiments at the LHC. They were used to equip the two innermost layers of the present ALICE ITS, as well as the tracking detectors of CMS and ATLAS[9] experiments [35, 36].



(a) (b)

Figure 1.5: (a) Cross-section view of a hybrid pixel detector and (b) an array of solder bumps.

The fabrication of the detecting components of hybrid pixel detectors is very similar to that of a silicon strip detector. In the pixel case, the implants have a higher segmentation, which is accomplished by subdividing each strip into some number of short pieces constituting the pixels. Unlike the strip detector, due to the large channel density, the read-out electronics of the hybrid pixel detector are vertically connected to the detecting layer. Fig 1.5 gives the cross section view of a hybrid pixel detector based on a N-type sensing volume. The connection of the detecting layer and the read-out electronics is customarily done by means of the flip-chip bonding technique. The array of small balls of solder, indium or gold, typically with the diameter of 20 - 30 μm ,

[9]CMS and ATLAS are two general-purpose detectors at the LHC.

establishes the electrical and mechanical connection between each detection element and its read-out circuit [37].

The detecting array of a hybrid pixel detector and its matching read-out chip are processed independently, and are connected together only at the final step. In this way, the material and processes can be optimized for the detector and electronics, separately. The detector substrate is high resistivity silicon with high immunity to radiation. And the read-out electronics is built in an industrial CMOS foundry, and its architecture can be similar with that of the classic front-end topology used for strip detectors. By profiting from the modern sub-micrometer processes, it is possible to integrate very complex and fast circuitry on a single segment of the read-out chip, matching the pixel pitch [38].

One of the prominent advantages of using the small pixelated segmentation in a hybrid pixel detector is its capability to provide unambiguously two-dimensional information. In addition, as compared to the strip detector, the smaller sensing element of a hybrid pixel results in a lower capacitance on the sensing node, which allows for fast signal shaping with low noise. However, the fabrication of hybrid pixel detectors is highly complex and expensive, which prevents their use in applications where large surfaces need to be covered, e.g., the outer layers of the ALICE-ITS. Moreover, even the state-of-the-art developments of hybrid pixel detectors exhibit abundant material budget, not complying with the requirement of the upgrade of the ALICE-ITS. Recently, efforts have been made, trying to thin down the hybrid pixel detector to 150 μm (100 μm sensor + 50 μm ASIC) [39]. Still, even if the robustness of fabricating such a thin hybrid detector is proven to comply with the time line for the ALICE upgrade, the hybrid detector is not a very optimal option because of the high production cost.

1.4.3 CMOS pixel sensors

The CMOS pixel sensor (CPS) is a relative newcomer in the field of charged particle detection. Its development was initiated by the IReS/LEPSI[10] research group in 1999 [40, 41], inspired by the use of the CMOS technology in the visible light application [42]. Profiting from the great achievements in the industrial CMOS processing, a feasible path has been paved, over the last ten years, to build a charged particle de-

[10]Institut de Recherches Subatomiques and Laboratoire d'Electronique et de Physique des Systèmes Instrumentaux, Strasbourg, France. In 2006 these units became a part of Département Recherches Subatomiques at Institut Pluridisciplinaire Hubert Curien (IPHC), Strasbourg.

tection sensor in a monolithic manner, namely integrating the read-out and processing electronics directly on the sensor substrate.

CMOS pixel sensors are fabricated by using the standard, cost effective and easily accessible CMOS processes. They are typically designed as an array of pixels, with the read-out and processing electronics located at the periphery of the chip. Featuring an amplifier integrated in each pixel, they are also known by the name of Monolithic Active Pixel Sensor (MAPS). One major difference of the CMOS pixel sensors with respect to the traditional microstrip or hybrid pixel detectors is its active volume, which is usually based on a lightly doped and undepleted epitaxial layer grown on a highly, P++-type doped substrate. The epitaxial layer is available in many modern CMOS VLSI[11] processes featuring twin tubs (twin wells). The active silicon components, forming transistors and the detecting diodes, are embedded into this layer. Typically, the epitaxial layer has a thickness on the order of 10 μm. By removing partially the substrate, it potentially allows for thinning the sensor chip down to a thickness of few tens of micrometers. The detailed working principal and some general discussions about the CMOS pixel sensors are given in Chapter 2.

The first generation of CMOS sensors, named MIMOSA[12], was tested with charged particle beam. These sensors showed for excellent detection efficiency close to 100 % and very high spatial resolution of about 1.5 μm, both resulting from a high signal to noise ratio (more than 30) [43–45]. These results stimulated a steady progress, during the last fifteen years, towards an ultra thin, large scale CMOS sensor with fast read-out architecture and radiation-tolerant design [46–53]. The state-of-the-art design of CMOS pixel sensors has combined the advantages of CCDs and hybrid pixel detectors, reaching an appropriate balance between granularity, material budget, radiation tolerance and readout speed. Thus, they have offered a cost effective and flexible solution for high precision tracking systems.

A great success of the CMOS pixel sensor development was achieved in early 2014, when the STAR-PXL detector, the first vertex detector equipped with CMOS pixel sensors, began to take physics data [54]. The PIXEL detector (PXL) forms the innermost sub-detector of the Heavy Flavor Tracker (HFT), a new inner tracking detector installed at the STAR (Solenoidal Tracker at RHIC) experiment [55]. With this new HFT, the STAR experiment is going to address a heavy flavour physics program similar

[11] Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining thousands of transistors into a single chip.

[12] MIMOSA stands for Minimum Ionizing particle MOS Active pixel sensor

to the one proposed for ALICE upgrade.

The successful implementation of the STAR-PXL detector greatly encourages the ALICE-ITS upgrade to use the same detector technology, since the STAR-HFT was conceived with a similar purpose as the upgraded ITS of ALICE. They both require very thin detectors, with high granularity, to be used as the innermost tracking devices. And at the same time, they don't have very stringent requirements of radiation-tolerance and read-out speed, as compared to CMS and ATLAS. Unfortunately, the CPS for the STAR-PXL detector, fabricated in a 0.35 μm CMOS process, does not correspond to all the specifications for the ALICE-ITS upgrade, particularly in terms of read-out speed and radiation tolerance. Besides, the currently used twin well process prohibits the use of PMOS transistors inside pixel, limiting the flexibility of circuit design for pixel-level intelligence. In order to reveal the true potential of CMOS pixel sensors for the upgraded ALICE-ITS, a more advanced CMOS process with a smaller feature size should be exploited. As will be discussed in Chapter 3, the very recent development of CMOS pixel sensors based on a 0.18 μm quadruple well CMOS process represents a promising solution to break through the current CPS limitations.

1.5 Summary

The ALICE experiment at LHC has scheduled a major upgrade of its apparatus, which will significantly enhance its physics capabilities. It particularly aims for high precision measurements of rare probes at low transverse momenta. Within this upgrade program, a new Inner Tracking System, with highly improved tracking and vertexing capabilities, plays an important role. The new ITS should also be able to cope with the substantially increased data rate, expected after the LS2 of LHC. These targeted performances call for a very thin and granular pixel sensor, with sufficient read-out speed and radiation tolerance, to equip the new ITS. The CMOS pixel sensor, a relatively new technology for charged particle detection, shows its great potential for this application. However, the state-of-the-art design of CMOS pixel sensor still suffer from a limited speed and radiation tolerance. Thus, the main purpose of this thesis is to develop a CMOS pixel sensor that can break the current limitations and accommodate well the requirements of the new ITS.

Chapter 2

CMOS pixel sensors for charged particle detection

In order to be detectable, a particle must interact with the material of the detector, and deposit energy as it moves through matter. In this work, the particles are detected from the ionizing events they produce, releasing charge carriers from the atoms of the detector material. By collecting these freed charges on the usually segmented electrodes of a detector, one can tell the presence, the impacting position and even the energy loss of an impinging particle. This chapter starts with introducing the interactions of particles with matter and their energy loss mechanisms. Then the principle of operation and the features of the CMOS pixel sensor are presented. After that, the radiation damage and the electronic noise in a silicon based charged particle detector are discussed, with a focus on the CMOS pixel sensor. The chapter ends with the global architecture and strategy for a fast readout CMOS pixel sensor.

2.1 Interaction of particles with matter

In order to develop a particle detector, a knowledge of the phenomena which occur when particles and radiation interact with matter, is necessary. This section is dedicated to clarify those basic physics mechanisms that lead to signals in a silicon radiation detector. For the convenience of discussion, the ionizing radiation is often divided into the three major categories: charged particles, photons, neutrons [56]. The former two are related to this work and thus will be discussed.

2.1.1 Charged particles

A charged particle interacts primarily through Coulomb forces, with the negative electrons and the positive nuclei that constitute the atoms of the material it passes through.

In the case of heavy charged particles[1], although interactions with nuclei are also possible, they are not important for charged-particle energy loss and detection. A heavy charged particle, moving through the detector material, exerts electromagnetic forces on atomic electrons and imparts energy to them. The energy transferred may be sufficient to remove an electron from an atom, causing ionization, or it may leave the atom in an excited, non-ionized state. In a single interaction, a heavy charged particle can transfer only a small fraction of its energy, thus it loses energy almost continuously in small amounts through electronic collisions with atomic electrons [57]. Except at the very end, the particle track tends to be quite straight because the particle is not greatly deflected by any single encounter, and interactions occur in all directions simultaneously

In contrast to heavy charged particles, fast electrons follow much more tortuous paths through the absorbing material, and a much larger fraction of their energy can be lost in a single interaction. These are because their mass is equal to that of the orbital electrons with which they interact. Electrons also differ from heavy charged particles in that energy may be lost by radiative processes, taking the form of bremsstrahlung[2]. These radiative processes are most important for high electron energies and for absorbing materials of large atomic number [58]. At electron energies above a few tens of MeV, bremsstrahlung dominates completely other processes.

Energy loss of heavy charged particles

The commonly used quantity to characterize the energy loss process is the average energy loss per unit track length $-dE/dx$. For moderately relativistic charged heavy particles, the mean rate of energy loss is well-described by the "Bethe equation" [59],

$$-\frac{dE}{dx} = Kz^2\frac{Z}{A}\frac{1}{\beta^2}[\frac{1}{2}ln\frac{2m_ec^2\beta^2\gamma^2W_{max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma))}{2}] \tag{2.1}$$

where

[1]The "heavy" charged particles refer to the charged particles other than the electron and positron.

[2]Bremsstrahlung is a German word which means "braking radiation". It is the electromagnetic radiation produced by the deceleration of a charged particle when deflected by another charged particle

- z is charge number of the incident particle;
- A is atomic mass of the absorber;
- Z is atomic number of the absorber;
- $m_e c^2$=0.510 998 928(11) MeV, is the electron mass $\times$ c^2;
- r_e=2.817 940 3267(27) fm, is the classical electron radius;
- K=$4\pi N_A r_e^2 m_e^2 c^2$=0.307 075 MeV mol^{-1}cm^2;
- N_A=6.022 141 29(27) $\times$ 10^{23} mol^{-1}, is the Avogadro's number,
- I is the mean excitation energy ([eV]);
- β=v/c, is the velocity of the particle in units of speed of light;
- γ=$\frac{1}{\sqrt{1-\beta^2}}$, is the Lorentz factor;
- $\delta(\beta\gamma)$ is the density effect correction to ionization energy loss;
- W_{max} is the maximum kinetic energy which can be transferred to a free electron in a single collision which is given by

$$W_{max} = \frac{2m_e c^2 \beta^2 \gamma^2}{1 + 2\gamma m_e/M + (m_e/M)^2}. \tag{2.2}$$

  where M is the mass of the incident particle.

The units for dE/dx described in (2.1) are MeV g^{-1} cm^2, so that dx is measured in mass per unit area. This equation gives the mean rate of energy loss in the region $0.1 \lesssim \beta\gamma \lesssim 1000$ for intermediate-Z materials with an accuracy of a few % . A minor dependence on M at the highest energies is introduced through W_{max}, but for all practical purposes, dE/dx in a given material depends on β only. The parameter δ accounts for the density effect due to the polarization of the medium by the incident charged particle [60], truncating the logarithmic rise of the energy loss function (2.1). This leads to the saturation of the ionization energy loss of very energetic charged particles in matter. It is noted that radiative effects begin to be important at extreme energies, and it is not included by the "Bethe equation".

On rare occasions, large energy can be transferred to a few electrons (knock-on electrons, or δ rays), and carried away from the track vicinity. This energy loss is generally not measured by the detector, and it is therefore more appropriate to consider the mean energy loss excluding energy transfers greater than some cutoff W_{cut} $\leq W_{max}$. The mean *restricted* energy loss rate is used to describe the mean rate of energy deposited along the track in the detector (in contrast to the energy lost by the particle), which is given by [59]

$$-\frac{dE}{dx} = Kz^2\frac{Z}{A}\frac{1}{\beta^2}[\frac{1}{2}ln\frac{2m_ec^2\beta^2\gamma^2W_{cut}}{I^2} - \frac{\beta^2}{2}(1+\frac{W_{cut}}{W_{max}}) - \frac{\delta}{2}]. \tag{2.3}$$

This form approaches (2.1) as $W_{cut} \to W_{max}$. Fig. 2.1 gives the mean energy loss rates for pions in silicon, evaluated by using (2.1) and (2.3) respectively. It can be seen that the mean energy loss shows a minimum at $\beta\gamma \approx 3$. Then, the mean *restricted* energy loss approaches a constant value, suppressing the relativistic rise of Bethe dE/dx at high energies. In practical cases, most relativistic particles have energy loss rates close to the minimum, and are said to be minimum ionizing particles (MIP).

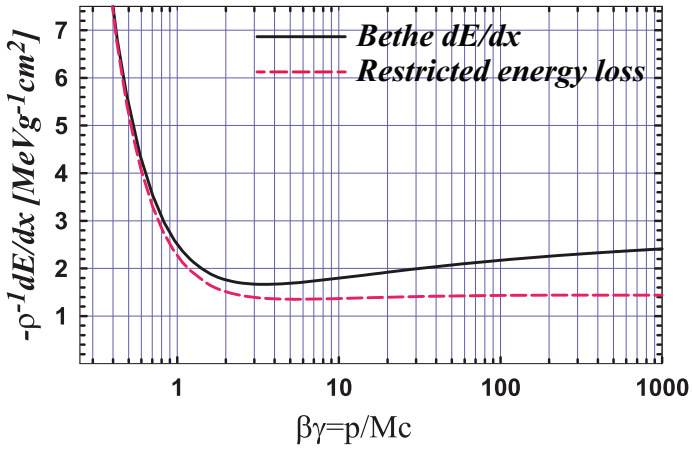


Figure 2.1: The mean rate of energy loss for pions in silicon as a function of the ratio between the particle momentum p and the particle mass M. (Source [61])

Fluctuations in energy loss

The "Bethe equation" forms the basis of much of our understanding of energy loss by charged particles. However, it is of limited use in practice. The energy loss is a discrete stochastic process. For finite thickness of medium, there are fluctuations in

the actual energy loss. In general, the distribution for the energy deposit is positively skewed, due to the rare large single-collision energy transfers that extend a long tail towards high energy values. The large weight of these rare events makes the mean of an experimental distribution consisting of a few hundred events subject to large fluctuations and sensitive to cuts. Thus the mean of the energy loss given by the "Bethe equation" is ill-defined experimentally and is not useful for describing energy loss by single particles.

The most probable energy loss is far better and more easily measured, and is also far more useful in situations where single-particle energy loss is observed. The distribution of the energy loss is described by the "straggling function" [62]. Fig. 2.2 gives the examples for 500 MeV pions incident on thin silicon detectors with different thicknesses. These distributions exhibit long tails apart from the Gaussian form. The peak in the distribution defines the most probable energy loss, which is considerably below the mean value given by the "Bethe equation". When the mean energy required for charge carrier generation in a given material is known, the most probable energy loss allows defining the most probable number of charge carriers generated along the particle track per unit length. For a typical CMOS pixel sensor discussed in this thesis, with $\sim$ 5 - 15 μm thick active volume, the signal charge generated by a single MIP particle ranges from a few hundreds to $\sim$ 1000 e^-.

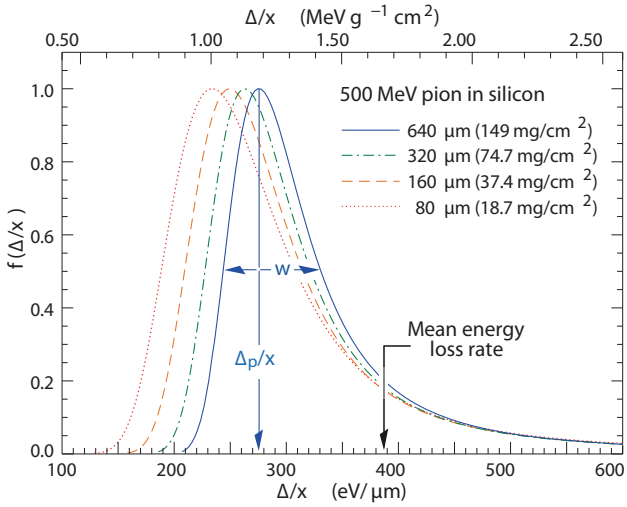


Figure 2.2: Straggling functions $f(\triangle/x)$ in silicon for 500 MeV pions, normalized to unity at the most probable value. x is the silicon thickness; $\triangle$ is the energy loss; $\triangle_p/x$ is the most probable energy loss; w is the full width at half maximum. (Source [59])

2.1.2 Photons

In contrast to the charged particles, photons, which are not subject to the Coulomb or nuclear forces, do not interact with matter at long distances, but only interact or "scatter" in localized or discrete interactions. In other words, when a photon penetrates in matter, nothing happens until the photon undergoes one interaction on one single atom. As a consequence of interactions, an incident photon either disappears or is scattered. Different physics processes are responsible for the energy loss of incident photons, among which the photoelectric effect, the Compton effect and the electron–positron pair creation are important for nuclear measurements. The contribution of the three interaction mechanisms depends on the photon energy and the atomic number of the absorber.

Photoelectric effect

For silicon, the photoelectric effect is a dominant process for photon energies below 100 keV. In photoelectric absorption, a photon disappears, being absorbed by an atomic electron. The process results in ionization by subsequent ejection of the electron, named photonelectron, from the atom. The energy of the liberated electron is the difference between the photon energy and the energy needed to extract the electron from the atom, i.e., the binding energy of the electron. The recoil momentum is absorbed by the nucleus to which the ejected electron was bound. If the resulting photoelectron has sufficiently enough of kinetic energy, it may be a source of a secondary ionization occurring along its trajectory. If the electron does not leave the detector, the deposited energy corresponds to the energy possessed by the incident photon.

The range R of the primary electron having the kinetic energy E is given by [63]

$$R = 40.8 \times 10^{-3}(E)^{1.5} \tag{2.4}$$

where the unit for R is μm and the energy E is in keV. R is on the order of some micrometers, thus the cloud of generated charge is confined close to the photon absorption point. This feature of the photoelectric effect allows for calibrating the gain of the detector chained with its readout system, if the energy required to create a single electron-hole (e-h) pair is known. Soft X-rays (photons with energies below 10 keV) interact with silicon predominantly through the photoelectric effect. The CMOS pixel sensors, which will be described in the following parts of this work, were tested by uti-

lizing a ^{55}Fe X-ray source. The iron source emits photons in two γ emission modes with energies of $\sim$ 5.9 keV and $\sim$ 6.5 keV. The yield of the latter mode is only about 12% of the first mode. The attenuation lengths for these two kinds of photons in silicon are $\sim$ 29 μm and $\sim$ 37 μm respectively, which are large enough to allow them to penetrate the whole active volume of the CMOS pixel sensors discussed in this work. The active volume here is the epitaxial layer with the thickness of the order of ten micrometers. Knowing that a 5.9 keV photon will generate approximately 1640 e-h pairs ($\sim$ 3.6 eV per e-h pair generation) in a silicon detector, an absolute calibration of the gain of the detector with its readout chain can be performed. The calibration is based on the fact that it is possible for a single charge collecting diode to collect the total charge released by the impinging photon, if the interaction point is inside or very close to the charge collection diode. One great feature of using the ^{55}Fe source is that the magnitude of the charge generated after photon conversion is comparable with the amount of charge expected from a minimum ionizing particle, assuming the epitaxial layer thickness to be approximately 15 μm.

Compton effect

Compton scattering (also called incoherent scattering) occurs when a photon has a much greater amount of energy than the binding energy of the electron, effectively considering the electron as 'free'. It is the most dominant mode of interaction for most materials in the photon energy range from 50 keV to 1.5 MeV [64]. Entering such an energy range, the photon begins to behave like a particle. When this particle-like photon collides with another particle, such as an atomic electron, the laws of conservation of momentum and energy apply to the kinematics of this collision-like process. In Compton scattering, the incoming photon transfers some energy to the atom, via its electrons (assumed to be initially at rest). The electron, which is given part of the energy by the photon, recoils while the photon carrying the remaining energy is emitted in a different direction from the initial one, so that the overall momentum of the system is conserved.

Pair production

At very high energy, another effect starts to be relevant: the pair production. Pair production can only occur when the energy of a photon exceeds 1.02 MeV. In pair production, a photon interacts with the electric field of the nucleus of an atom. The

photon's energy is transformed into an electron-positron pair. The rest energy of an electron is 0.511 MeV and this is why the energy threshold for this reaction is 1.02 MeV. Photon energy in excess of this threshold is imparted to the electrons as kinetic energy. The electron and positron lose their kinetic energy via excitation and ionization. When the positron comes to rest, it interacts with a negatively charged electron, resulting in the formation of two oppositely directed 0.511 MeV annihilation photons. In fact, the pair production does not become significant unless the photon energies greatly exceed the 1.02 MeV energy threshold.

2.2 Detection principle and features of CPS

Generally, silicon detectors use the reverse-biased p-n junction as the charge collection electrode, allowing for a very limited DC leakage current with possible large electric field to separate the charge carriers with opposite signs (e.g., e-h pairs) in the active volume. In microstrip detectors or hybrid detectors, as described in Chapter 1, a very large reverse bias voltage is applied on the p-n junction, leading to a fully depleted active volume. The high electric field, in the fully depleted active volume, accelerates the charge collection and minimizes the charge trapping in the lattice defects and the recombination. However, this is not the case for CMOS pixel sensors, as they are fabricated in a standard CMOS process, where limited voltage range is allowed to deplete the active volume. Despite this, CMOS pixel sensors still show great potential for charged particle detection.

A cross section of a typical cell of the CMOS pixel sensor is shown in Fig. 2.3. The active volume of the sensor is a P-type epitaxial layer, grown on a highly doped substrate. The charge generated by the impinging particle is collected by the N-well/P-epi diode, created by the floating N-well implantation reaching the epitaxial layer. This structure forms a potential well that attracts electrons. The pixel-level read-out electronics is placed in the P-well. The fact that the active volume is underneath the readout electronics allows a CPS to achieve $\sim 100\%$ fill factor, which is necessary in tracking applications. Due to the limited reverse bias voltage that can be applied on the diode, the electric field is present only in the vicinity of the electrode, and the charge generated in the undepleted active volume is collected through thermal diffusion. The doping levels of the P+ wells and the P++ substrate are much higher than that of the epitaxial layer lying in between them, resulting in potential barriers at the

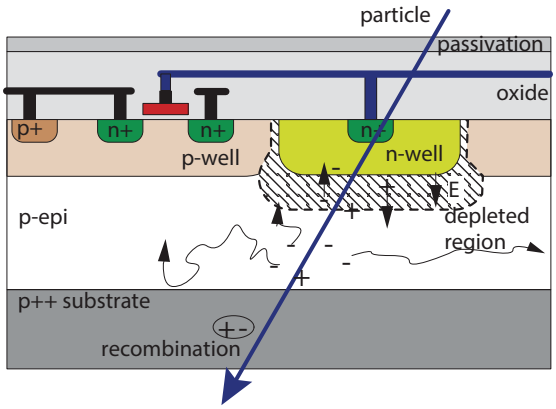


Figure 2.3: The cross section view of a single cell of a CMOS pixel sensor. The epitaxial layer, commonly used in modern CMOS processes, forms the active volume of the detector. Typically, the thickness of the epitaxial layer is limited to approximately 15 μm. The charge collection diode is formed by the implanted N-well reaching the epitaxial layer. The depleted region appears in the vicinity of the diode. In the undepleted region, the charge deposited in the active volume by an impinging ionizing particle moves by thermal diffusion.

layer boundaries that restrict the diffusion of the electrons within the epitaxial layer. The majority of charge carriers generated in the highly doped, low-quality substrate will quickly recombine and only a small fraction will reach the active layer. Device simulations at the physical level showed the charge collection time, for a typical pixel pitch of 20 μm, to be likely in the range of 10 - 100 ns [40, 61].

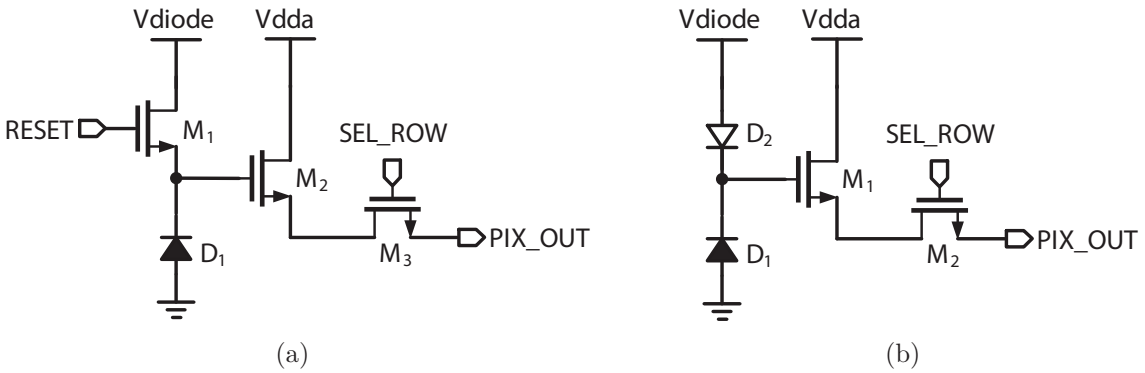


Figure 2.4: (a) The 3T pixel and (b) the self-bias pixel.

The signal sensed in the CPS has a form of weak and short in time current pulses induced on pixel electrodes by the liberated charge carriers. The signal current is integrated on the N-well/P-epi junction capacitance, resulting in a voltage drop on the collection diode. This voltage can be directly processed by the frond-end electronics, integrated on the same substrate close to the collection diode. Fig. 2.4(a) gives one basic structure of a CMOS pixel, called the 3T structure. Each pixel employs three transistors: one is used for resetting the sensing diode voltage (M_1); the second acts as the input transistor of a source follower (M_2); and the third is a switch to address the pixel for the readout and signal transfer (M_3). The current source for the source follower is placed at the chip periphery. For applications with a relatively low or moderate hit occupancy, the self-biased (SB) structure was proposed by the PICSEL group [65]. As shown in Fig. 2.4(b), the leakage current of the sensing diode (D_1) is continuously compensated by a forward biased diode (D_2). At the same time, the very high resistance of the forward biased diode allows for treating the N-well as a floating node. Therefore, in case of an impinging particle, a voltage drop appears on the sensing diode with a very slow recovery time. As compared to the 3T structure, the SB pixel is free from the reset noise and dark current induced pedestal. It is noted that in a conventional twin-tub process, the pixel-level read-out circuit is restricted to only NMOS devices, since any additional N-well hosting the PMOS transistors in a pixel cell would compete in the charge collection against the sensitive electrode. At the chip periphery, both NMOS and PMOS transistors are allowed.

The following summarizes of advantages of using CPS for charged particle detection:

- High granularity: because of the integration of front-end electronics directly on the sensor substrate, the pixel pitch of CMOS pixel sensors is no longer constrained by the bonding bump, as the case for the hybrid pixels. With a simple pixel structure, e.g. 3T structure, a pixel size of 10×10 μm^2 or even smaller is possible;

- Low noise: thanks to the small pixel size and the short-distance on-chip interconnection between the sensing diode and the front-end electronics, the total capacitance appearing on the sensing node is very small, leading to a very low intrinsic noise. Noise performance of a typical CMOS pixel sensor can be optimized to as low as 10 e$^-$ at room temperature [66];

- Low material budget: as a result of the low noise performance, an active volume

as thin as on the order of 10 μm is enough to obtain sufficient signal charge ($\sim$ 1000 e^-) for a satisfactory signal-to-noise ratio (SNR). Moreover, by using a commercial post-processing (back-thinning) to remove most of the substrate until it is very close to the epitaxial layer, a CMOS pixel sensor can be thinned down to 50 μm without degrading their mechanical and electrical properties [67, 68].;

- Low cost: the CMOS processes are easily accessible through multi-project[3] and engineering runs, which allows cost-effective and fast design-to-verification cycle in the detector design;
- High integration level: the design and fabrication of CPS profits largely from the fast advancing microelectronic industry. Modern deep sub-micron technologies offer the opportunity to implement very compact and complicated on-chip digital logic with low power consumption, making it possible to approach eventually the integration of the whole detecting system on a single chip.

It is noted that the use of commercial CMOS process, which has given the CMOS pixel sensor so much power, also becomes a limitation. This is because the CMOS industry evolves in a direction to meet the mass market requirements, and the manufacturing parameters may depart substantially from those needed for charged particle detection. The selection of industrial processes for CPS is often driven by the characteristics of the epitaxial layer, including thickness of the epitaxial layer and doping profiles. These basic manufacturing parameters are fixed by the manufacturer and are quite often not known reliably. Therefore, the exploration of fabrication processes is of prime importance for the development of high performance CMOS sensors [69].

2.3 Radiation damage in silicon detectors

The SNR of a silicon detector decreases with progressing radiation damage. On one hand, the charge collection process could be severely affected due to the radiation induced defects in the silicon bulk, creating charge trapping or recombination centers and modifying the effective doping concentration. On the other hand, the noise performance is degraded mainly due to the increased leaking current [70]. As far as the

[3]Many small area IC designs from different institutions are processed on the same wafer effectively reducing a single user costs. The limitations come from a minimum and maximum area available for a single project and the number of fabricated devices. On the contrary, in the engineering run, a requested number of wafers are dedicated to a single project.

readout electronics is concerned, the parameters of bipolar and MOS devices can be degraded by the radiation induced surface effects at the Si-SiO_2 interface, as well as by defects in the bulk.

The silicon tracking and vertexing devices are placed very close to the interaction point in high energy physics experiments, being exposed to intense fluences of damaging radiation. Therefore, the radiation tolerance of these devices is of great interest, in order to retain a minimum SNR for efficient particle detection. Radiation damage in silicon can be roughly categorized in two classes: bulk damage and surface damage. The former are usually caused by the displacement of crystal atoms, while the latter includes all effects in the covering dielectrics and the interface region. In this section, both of these radiation damages are shortly reviewed. Special focuses will be put on the CMOS pixel sensor.

2.3.1 Bulk damage

In the undepleted bulk of the semiconductor, the high charge carrier density allows the deposited charge carriers to recombine. Therefore, ionizing energy losses of particles will not lead to any relevant changes in the silicon lattice. However, the impinging particles, which impart an energy higher than the displacement threshold energy of about 25 eV [71, 72], can knock out a single silicon atom from its lattice site, causing bulk damage.

The primary knock-on atom (PKA), displaced by an impinging particle, results in a silicon interstitial and a left over vacancy (Frenkel pair)[4], both of which can migrate through the lattice. And finally, a point defect may be formed, with an impurity atom being resident in the silicon. Along the path of a recoil atom with sufficient kinetic energy, the energy loss is attributed to both ionization and further displacements, the latter of which gives rise to a PKA cascade. At the end of any heavy recoil range, the non-ionizing interactions prevail and a dense agglomeration of defects (disordered regions or clusters) is formed. Both point defects, along the particle paths, and the clusters, at the end of their range, are responsible for the various damage effects in the bulk of the silicon detector [73]. The defect clusters, usually result from interactions of massive particles such as protons and neutrons, are more critical, since they have high local defect density and can be tens of nanometers wide. Neutrons, protons and

[4]The vacancies are referred as empty lattice sites and interstitial atoms are those which are knocked out of their normal positions in the crystal lattice.

pions need about 15 KeV of energy to produce clusters. Whereas, the energy transfer from electrons and gammas of up to more than 5 MeV is not high enough to produce cluster damages [74].

The defects in the crystal structure introduce additional energy levels within the silicon band gap, which has an important impact on macroscopic properties of the devices, especially those fabricated from a detector grade material (high quality, high resistivity, lowly doped, long minority carrier lifetime). The bulk damage manifests itself in three important ways [75, 76]:

- Formation of mid-gap states, which facilitate the transition of electrons from the valence to the conduction band. In depletion regions, this leads to the generation current, i.e., an increase in the current of reverse-biased PN-diodes. In forward biased junctions or non-depleted regions, mid-gap states facilitate recombination, i.e., charge loss.

- States close to the band edges facilitate trapping, where charge is captured and released after a certain time.

- A change in doping characteristics (donor or acceptor density).

To good approximation, the displacement radiation damage in silicon is proportional to the non-ionizing energy deposited by energetic nuclear recoils [77]. This is the so-called Non-Ionizing Energy Loss (NIEL) hypothesis, which allows one to predict the electrical device degradation by only determining experimentally the proportionality constant at a few or even only one particle energy. The damage at another particle energy (or even for another particle with the same or a different energy) can then be determined from the theoretical NIEL [78]. The NIEL value is usually scaled by referring to the equivalent fluence of 1 MeV neutrons, producing the same damage as an examined particle beam with a given spectral energy distribution.

CMOS pixel sensors are relatively vulnerable to non-ionizing radiation due to their charge collection mechanism of thermal diffusion [79]. The bulk damage reduces the lifetime of free electrons in silicon, which increases the probability of charge loss due to recombination. This may be compensated by reducing the pixel pitch and, accordingly, the diffusion path of the electrons. An alternative way is to accelerate the charge collection by increasing the depletion depth of the active volume, which was restricted by the high doping level in the epitaxial layers of standard CMOS processes. However,

this limit tends to vanish, as a new industrial trend has made CMOS processes with a dedicated high resistivity epitaxial layer commercially available [52, 53] [80].

2.3.2 Surface damage

The term surface damage summarizes all defects in the overlaid dielectrics, e.g., the silicon oxide, and the interface between the silicon and the dielectric. As the crystal structure of silicon oxide is highly irregular, displacements of single atoms due to irradiation do not lead to macroscopic changes. Ionization in the oxide, however, is not fully reversible and may cause steady changes of the interface properties.

As in the detector bulk, electron-hole pairs are created by ionizing radiation in the oxide. The electrons are collected quickly by the the positive electrode close by, due to their high mobility in the oxide ($\mu_{n,oxide} \approx 20$ cm^2/Vs). However, the holes have a very low mobility in the oxide ($\mu_{p,oxide} \approx 2 \times 10^{-5}$ cm^2/Vs). Due to a large number of shallow hole traps, they move by a rather complex and slow hopping mechanism, which enhances the probability of the hole trapping in the oxide volume and thus leaves an associated fixed positive charge. Holes that diffuse or drift to the Si-SiO_2 interface, where there are numerous traps resulting from the strained or dangling silicon bonds at the boundary between the two materials, can be captured by the interface traps, and positive charges are built up at the silicon interface [81].

The density of the interface traps depends strongly on the processing parameters, such as oxidation temperature. Ionizing radiation can increase the trap density and modify their energy distribution. Hence, new energy levels are introduced in the band gap at the Si-SiO_2 interface. They play the roles of additional acceptor or donor states, which are charged under thermal equilibrium. Trapped charges alter the electrical characteristics of the devices by modifying the electric fields inside. Besides, these energy levels act either as trapping centers for charge carriers generated by incident particles, blocking partially the signal charges, or as generation-recombination centers, translating into an increased leakage current.

In CMOS pixel sensors, ionization damage manifests itself most clearly in the readout electronics, as the operation of the MOS transistors lies in the oxide that couples the gate to the channel. Positive charge build-up due to hole trapping in the oxide and at the interface shifts the gate voltage required for a given operating point to more negative values. This shift affects the operating points in analog circuitry and switching times in digital circuitry. Moreover, in a standard bulk CMOS process using

P-type substrate wafers, accumulated positive charges may provoke short circuits in the design. This effect is strongly enhanced under thick oxide regions, where shallow surface channels can be created between N-type implants of different MOS devices if they are separated only by lightly doped P-type silicon. The increased density of the interface states also has impacts on the flicker noise of MOS transistors, which is more pronounced for NMOS transistors than for PMOS devices.

Some of the stuck holes, i.e., those that are closest to the interface, may recombine with electrons mounting from silicon. The electrons can reach the oxide volume through the tunneling effect[5], which reduces the amount of positive charge trapped in the oxide. The probability of the tunneling electron jump increases exponentially with decreasing the thickness of the oxide volume. Thus, the MOS transistor, fabricated in a modern deep sub-micrometer technology, usually tends to be more radiation tolerant than that in a past technology, thanks to the scaling down of the gate oxide. Certain design techniques can also be applied to increase radiation tolerance of readout electronics. Two widely used techniques are P+-type guard-rings, separating N-type regions, and the enclosed gate NMOS transistor layout, avoiding thick oxide at the ends of the polysilicon gate of a classical rectangular shape NMOS transistor [82].

2.4 Noise

An important figure of merit for tracking and vertexing detectors is the detection efficiency, which depends a lot on the SNR. A detector with a good SNR can effectively distinguish between signals generated by ionizing particles (real hits) and noise fluctuations (fake hits). Generally, the amplitude of the signal is limited due to physics or detector limitations. A typical CPS uses an almost undepleted active volume, and the signal charge collected by the seed pixel[6] is only on the order of several hundreds of electrons. Therefore, noise performance can become a critical issue.

Noise in a detector system can result from many sources, both internally and externally. The external sources, such as electromagnetic interference or power supply fluctuations, can often be minimized to a negligible level by proper circuit design tech-

[5]Quantum tunneling or tunneling refers to the quantum mechanical phenomenon where a particle tunnels through a barrier that it classically could not surmount.

[6]Due to the charge sharing, the signal charge is often collected by several neighbouring pixels, forming a cluster. The central pixel of a cluster is typically referred to as seed pixel. Seed pixel is expected to have collected most of the charge in a cluster.

niques or shielding and grounding. The internal electronic noise defines intrinsically the ability of a detector to distinguish signals. This section deals only with the internal noise. Customarily, detector readout systems that measure signal charge are characterized in terms of equivalent noise charge (ENC). This is the charge that would equalize the output signal to the noise level. In other words, it is the charge that yields an SNR equal to one. The value is derived based on the output noise of the system, which is a combination of all noise contributions within the system's bandwidth.

The noise in a CPS is often divided into two categories: the temporal noise (TN) and the fixed pattern noise (FPN). This section gives an introduction to both of them. Moreover, a commonly used noise reduction technique, correlated double sampling (CDS), is described.

2.4.1 Temporal noise

Temporal noise is the temporal variation of the pixel output values when the input does not undergo any changes. There are many sources of temporal noise in a CMOS pixel sensor. It includes primarily the photodiode shot noise, and the output amplifier's thermal and flicker noise.

In reality, the operation of CMOS pixels is typically divided into three phases: the reset phase, the integration phase and the readout phase. A detailed analysis of temporal noise, which can be found in [83, 84], should take into account all the three phases separately and is out of the scope of this thesis. This section deals with the basic physics mechanisms of different types of noise, and their characterization.

Shot noise

Shot noise is associated with the flow of current in diodes and bipolar transistors. It is generated by the fluctuations occurring when charge carriers cross a depletion region. There must be both a flow of current and a potential barrier to generate shot noise. Shot noise is modeled as white Gaussian noise (WGN), since it is zero mean, Gaussian and has a very flat and wide bandwidth power spectral density (PSD). Shot noise is often represented by a current source in parallel with the DC source I. Its PSD is proportional to I, and is given by

$$S_{shot}(f) = 2eI, f \geq 0 \tag{2.5}$$

Shot noise occurs when dark current electrons pass through the diode. One aspect about the shot noise, that should be noted, is its dependence on the integration time. The signal in a detector is proportional to the electric charge accumulated on the photodiode, and this charge is subjected to a continuous loss due to the leakage current integrated on the photodiode. The charge loss is proportional to the time with the relation:

$$Q = I_{leak} \times t_{int} \tag{2.6}$$

where I_{leak} is the leakage current and t_{int} is the integration time. If we assume I_{leak} as a stochastic process with a given variance, Q is a stochastic process, in turn, with a variance t_{int} times higher than the variance of the leakage current.

Thermal noise

Thermal noise is the electronic noise generated by the thermal agitation of the charge carriers (usually the electrons) inside an electrical conductor at equilibrium, which happens regardless of any applied voltage. It is zero mean, and has a very flat and wide bandwidth Gaussian PSD. Consequently, it can be also modeled as WGN. Thermal noise is represented either as a voltage source in series with a resistor R, with the PSD given by

$$S(f)_{v,R} = 4k_B T R, f \geq 0 \tag{2.7}$$

or as a current source in parallel with the resistor, with the PSD given by

$$S(f)_{i,R} = \frac{4k_B T}{R}, f \geq 0 \tag{2.8}$$

where k_B is Boltzmann's constant and T is the absolute temperature.

MOS transistors also exhibit thermal noise. The most significant source is the noise generated in the channel. It can be proved that for long-channel MOS devices operating in saturation, the channel noise can be modeled by a current source connected between the drain and source terminals with a spectral density

$$S(f)_{i,MOS} = 4k_B T \gamma g_m, f \geq 0 \tag{2.9}$$

where the coefficient γ is derived to be equal to 2/3 for long-channel transistors and may need to be replaced by a larger value for sub-micronmeter MOS transistors.

Thermal noise on capacitors is referred to as kTC noise. The kTC noise in an RC

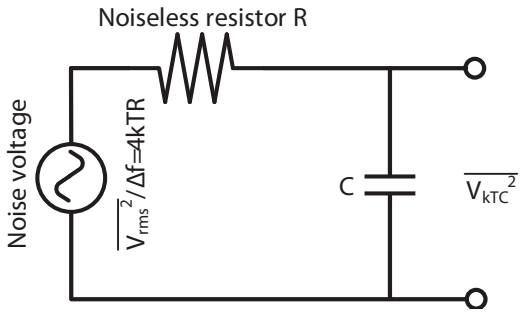


Figure 2.5: Noise in a RC circuit.

circuit (see Fig. 2.5) has a very simple expression, as the value of the resistance (R) drops out of the equation. The mean-square noise voltage generated in such a RC circuit is

$$\overline{V_{kTC}^2} = k_B T/C. \tag{2.10}$$

It can be seen that the total noise power depends only on the capacitor. This is because higher R contributes to more filtering, as well as to more noise. The noise bandwidth of the RC circuit is $1/(4RC)$, reversely proportional to R. Hence, the integral of (2.7) throughout the noise bandwidth results in (2.10), with R eliminated. In reality, a larger R in a RC circuit may lead to more noise for the overall circuit system. One example is when the RC circuit is followed by a stage with a narrow bandwidth, working as a low-pass filter for the kTC noise. For a larger R, the kTC noise exhibits more low-frequency component and narrower noise bandwidth. Hence, more noise will present at the output after the noise filtering.

In a sampling circuit, where a switch is connected in series with a sampling capacitor, two phases are required to operate. The thermal noise from the switch is sampled on the capacitor in one phase, and processed by the following circuits in the other phase. In this case, the overall power of the kTC noise remains, and depends only on the capacitance value of sampling capacitor, following the formula (2.10). This sampled kTC noise applies in the circuit of Fig. 2.4(a), where the sensing diode is reset periodically by a MOS switch. For a capacitance of several fF on the sensing node, the kTC noise contribution is in the order of 40 - 50 e^-. In reality, the kTC noise is less than the value predicted by equation (2.10), because the reset time is not long enough for the circuit to reach a steady state [84]. But the kTC noise is still the dominant noise source in the CMOS pixels, and needs to be removed by certain circuit design techniques, e.g., correlated double sampling.

Flicker noise

As has been mentioned in Section 2.3.2, at the interface between the gate oxide and the silicon substrate in a MOS transistor, many "dangling" bonds appear, giving rise to extra energy states. As charge carriers move at the interface, some are randomly trapped and later released by such energy states, introducing "flicker" noise in the drain current. In addition to trapping, several other mechanisms are believed to generate flicker noise [85]. The flicker noise can be modeled by a noise voltage appearing in series with the gate, whose PSD is given by [86]

$$S_{v,f}(f) = \frac{K}{C_{ox}} \frac{1}{WL} \frac{1}{f} \tag{2.11}$$

where K is a process-dependent constant, C_{ox} is the oxide capacitance in MOSFET devices, W and L are the channel width and length respectively. The flicker noise does not depend on the bias current or the temperature. Due to the fact that its noise spectral density is inversely proportional to the frequency, flicker noise is also referred to as $1/f$ noise. Note that (2.11) is only an approximation and in reality, the flicker noise equation is more complex [85,86]. Generally, the power spectral density of flicker noise in a P-channel device is found to be significantly less than that of the N-channel device with the same dimensions and fabricated in the same CMOS process (by 1 order of magnitude or more). It is because the former carries the holes in a "buried channel", i.e., at some distance from the oxide-silicon interface.

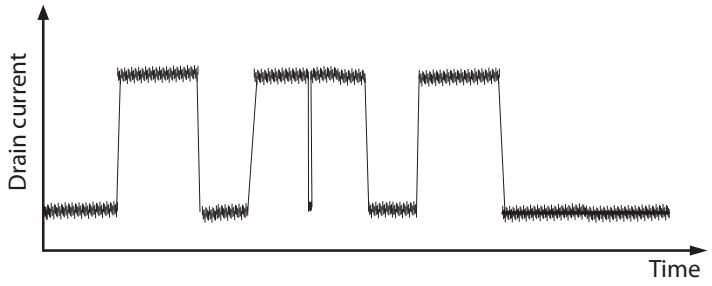


Figure 2.6: The drain current as a function of time for a transistor exhibiting RTS.

Equation (2.11) also suggests that the device area must be increased in order to decrease $1/f$ noise. If the gate area WL is very small (a fraction of 1 μm^2), there will be only a few traps which can exchange charge with the channel, and their individual effects will be noticed, rather than tending to average out as in the case of large gate area. In fact, it is possible that only a single trap of this type exists in a very small

device. Then, as it captures and releases charge, abrupt changes in the drain current can be noticed. These sudden step-like changes will be on top of the more common noise variation (as shown in Fig. 2.6) and are called "random telegraph signal (RTS)". In the context of continuously downscaling the transistor dimension, the RTS noise has become an issue for CMOS image sensor [87,88], and has also been observed to be significant for the CPS fabricated in a 0.18 μm process [89].

2.4.2 Fixed pattern noise

Fixed pattern noise is the term that refers to a particular noise pattern on imaging sensors. It is the spatial variation in pixel output values in the dark or under uniform illumination, due to device and interconnect parameter variations (mismatches) across the sensor. Fixed pattern noise is spatial in nature and ideally does not change with time for a particular illumination. Hence, the name "fixed" is used to differentiate it from the temporal random noise.

Strictly speaking, the FPN includes two different components: the dark signal non-uniformity (DSNU), that is a measure of non-uniformity due to pixel-to-pixel output variation in the dark, and the photo response non-uniformity (PRNU), that represents the different manners with which the pixels react to a uniform irradiation. The dark component (DSNU) contributes almost constant to output signal under varying illumination, whereas the "gain" component (pure PRNU) is with magnitudes that change with illumination [90].

As the case of a particle tracking detector, the "gain" component corresponds to the charge conversion non-uniformity. In practice, this gain component is less detrimental, as long as it is limited to a few percent. And the correction of the charge conversion non-uniformity can be applied off-line, when the accurate amplitude of the measured signal is requested. However, the DSNU of an active pixel matrix can be much higher than magnitudes of signal expected from a particle impact. By using the CDS technique described in the following section, the DSNU can be effectively mitigated. As a result, the FPN in the pixel can be very small, as compared to the temporal noise.

2.4.3 Correlated double sampling

Correlated double sampling (CDS) is a commonly used technique to remove the undesired offset from the sensor outputs. When used in the CMOS sensor, the CDS element

generates a difference of two voltages at a sampling node, with the second voltage representing the integrated signal superimposed on a fixed DC offset, and the first voltage representing the offset alone. As a result, the signal produced by the radiation is retrieved, and the offset variation due to the read-out electronics is removed.

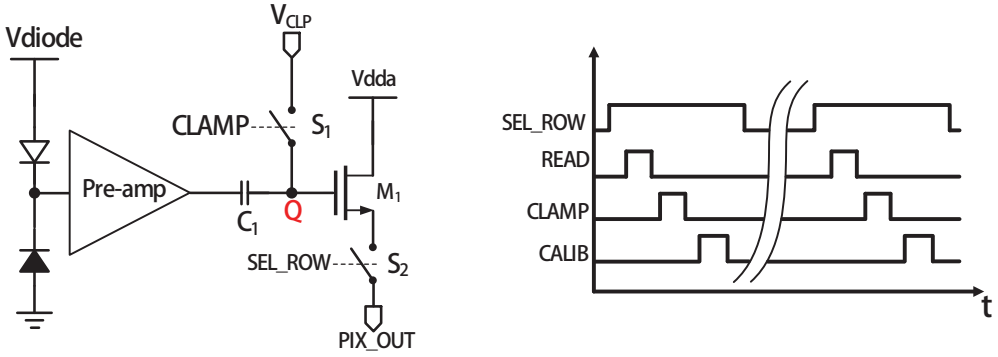
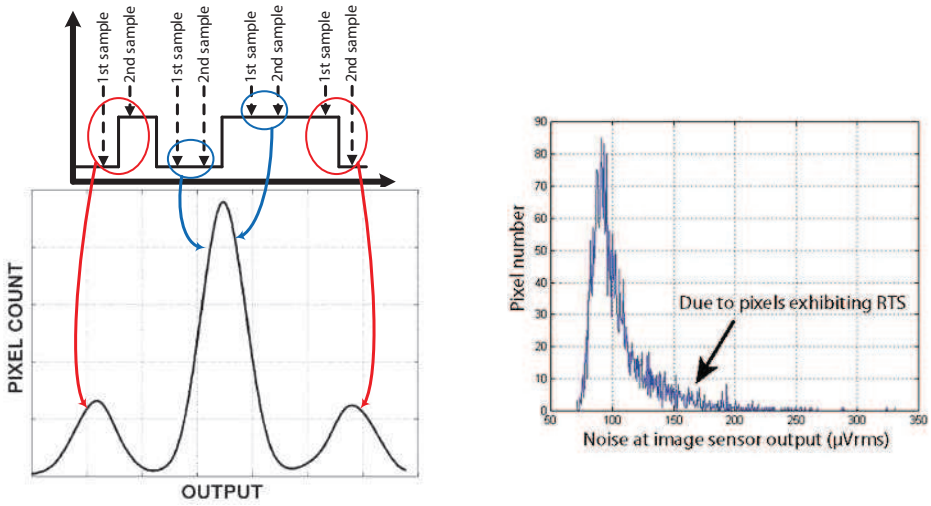


Figure 2.7: A typical CMOS pixel with in-pixel CDS (left) and the corresponding chronogram for operation (rignt).

Fig 2.7 shows a typical CMOS pixel with in-pixel CDS, along with the timing diagram for operation. A pre-amplifier is used to increase the signal amplitude, and thus to ensure a satisfactory SNR through the whole read-out chain. The CDS element is formed by capacitor C_1 and switch S_1. During the *CLAMP* phase, the voltage on node Q is clamped to the reference level V_{CLP} through S_1. By doing this, the offset of the pre-amplifier is memorized on capacitor C_1 and is "invisible" at node Q. At the next access to the pixel, the voltage at node Q becomes the instantaneous output voltage of pre-amplifier, subtracted by the offset voltage stored on C_1. Then, the node Q is reset again to the reference level for the next read-out cycle. In practice, two samples are needed at each pixel access, one taken before the voltage clamping (*READ* phase), and the other taken right after the voltage clamping (*CALIB* phase). The former contains the integrated voltage signal superimposed on the reference level, and the latter represents the reference level. The subtraction of those two samples result in the signal voltage free from offset. If the detecting diode is reset periodically by a switch, as the 3T structure shown in Fig. 2.4(a), the kTC noise sampled on the diode (reset noise) can also be taken as an offset and eliminated by the CDS. In addition to the elimination of pixel offset, the subtraction of two samples of the same noise also results in a cancellation for very low frequency noise, like the 1/f noise [91, 92].

The small penalty of using CDS is an increased white noise foldover component due

to the aliasing of the amplifier's thermal noise, as well as the l/f noise. In most practical cases, this foldover term is dominated by the aliased thermal noise component [91]. It is also worth mentioning that the CDS cannot remove the RTS noise. As shown in Fig. 2.8(a), if the transistors of the in-pixel read-out electronics produce significant RTS noise, the pixel dark response at the sensor output shows different levels, even after CDS. For the two level RTS noise, each sample may be taken at either of the two levels, and three states can be seen at the output, resulting from the four possible combinations of the two sampling levels. The two "side peaks", as those in Fig. 2.8(a), give rise to the pixel temporal noise. As a result, the noise distribution of all the pixels in the matrix shows a non-Gaussian shape with a positive skew. Fig. 2.8(b) gives the noise distribution of a CMOS image sensor from reference [88], and the positive skew comes from the pixels exhibiting significant RTS noise.



(a) (b)

Figure 2.8: (a) Illustration of three output states of a pixel, resulting from the two level RTS noise, and (b) the noise distribution of all the pixels in a CMOS image sensor from reference [88].

2.5 Read-out architecture

The easiest and most intuitive way to read out CMOS pixels is to address sequentially the pixels for analogue readout, as it was the case of the first MIMOSA chip [43, 61].

However, reading out a sizable pixel matrix using this approach is too slow, and thus is not compatible with the running conditions of modern high energy physics experiments with very high event rates. In order to accelerate the readout, pixels in a matrix can be divided into groups and read out in parallel. The *rolling shutter* architecture is based on the concept that the pixel matrix is read periodically row by row, resulting in a column parallel readout. For a reticule sized sensor comprising of millions of pixels, the readout speed can be increased by orders of magnitude if the rolling shutter architecture is used instead of the simple series readout. Thus, a time resolution reaching the μs level is possible. However, the drawbacks of developing fast sensors are the high genuine data flow one has to cope with, and also the increased power consumption. In this section, a global read-out architecture for a fast and power efficient CMOS pixel sensor is described.

In a real detector system, the analogue information from the pixels needs to be digitized and transmitted to the central data acquisition (DAQ) system. Using a high resolution analog-to-digital converter (ADC), e.g., 12-bit ADC, retains better the charge diffusion information, and is capable of achieving a much higher spatial resolution than the binary resolution as expressed in Eq. (1.1). However, this is at the cost of increased data flow. For complex systems such as micro vertex detectors, where tens of sensors operate in parallel, a high read-out speed produces an enormous data flow. The transfer of such an amount of data to a central DAQ is considerably complicated. Moreover, it is questionable if the central DAQ system can cope with the raw data stream delivered by a sizable vertex detector. As a result, the complications induced by this high data stream may dominate the benefit of "analog" readout.

Using the binary encoding pixel is a practical and promising solution, where only 1-bit digital signal is used to represent whether the signal charge collected in the pixel exceeds a certain threshold value (signal discrimination). A fast 1-bit A-D converter, named discriminator in the context of this thesis, can be easily implemented on the sensor chip close to the detecting pixel array, with affordable area and power consumption. A spatial resolution of $\lesssim 5$ μm can be achieved by using binary encoded pixels with a pixel pitch of 20 - 30 μm.

In reality, the binary encoding scheme has to be complemented by a data sparsification logic to confront the drawbacks of fast sensors, e.g., large data flow. The use of data sparsification logic relies on the fact that the occupancy of the pixel detector is very low (within several percent) in order to efficiently reconstruct the tracks. So the

important information from one event is delivered only by a limited number of pixels in a detector. The other pixels, that are not touched by traversing particles, do not produce any relevant information, thus give "0s" after the signal discrimination. These "0s" should be filtered out by using a fast zero-suppression circuit, placed as close as possible to the sensitive area to reduce the data flow. CMOS sensors are particularly well suited to this type of requirement, as they allow to integrate the necessary sparsification micro-circuits on the sensor itself [69]. Depending on the pixel occupancy, the data suppression level is usually between 10 and 1000.

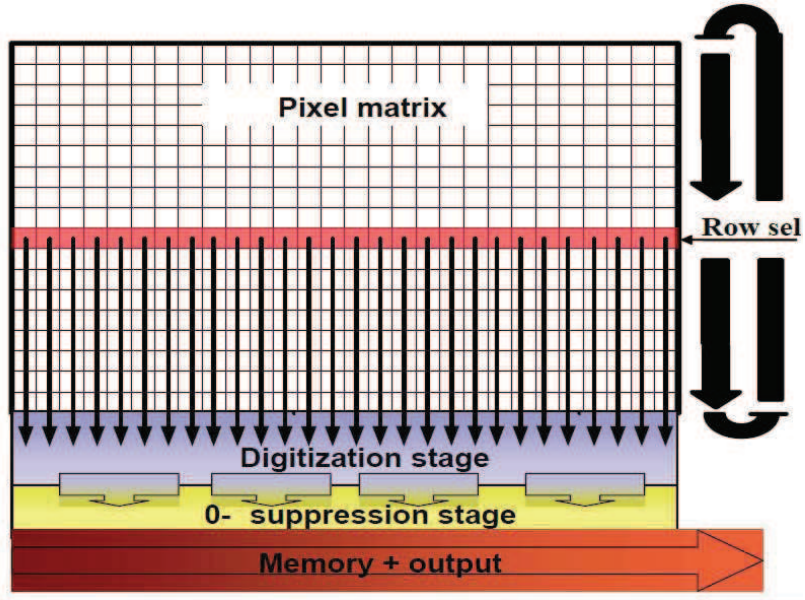


Figure 2.9: The global architecture of a rolling shutter CPS.(Source [93])

The global architecture of a typical rolling shutter CPS is shown in Fig. 2.9. It combines the signal discrimination and data sparsification functions on the sensor substrate, located at the bottom of the pixel array. The pixel array is addressed in a rolling shutter mode, with the pixels in the same row read out in parallel. In order to save power, the front-end circuit of a pixel is only switched on when the pixel is addressed for readout. The pixels, which are not selected, are powered off, but they remain sensitive and the hits can be registered on their sensing nodes. In order to increase the SNR, the pixel incorporates the pre-amplifying and CDS functions. Each pixel column is terminated by a discriminator at the bottom edge, in order to decide whether a pixel is fired or not. The discrimination results are sent to a zero suppression logic stage, which filters out the irrelevant information and stores only the fired pixel

addresses in memory for output.

At any moment, three main operations are conducted simultaneously: pixel read-out and signal discrimination of a given row (denoted n), zero suppression of all the discriminator outputs of the row (n-1) and storage in memory, reading out from the memory of the fired pixel addresses of the row (n-2). The matrix read-out time with this architecture is given by the product of the number of rows and the time to read a row. Up to the discrimination stage, the readout speed is not limited by the hit rate. However, the occupancy level strongly drives the design and size of the zero-suppression logic and of the memories. For a fixed pixel size, the higher the occupancy and the desired readout speed, the larger the logic micro-circuitry and the memories.

To conclude this section, we should point out the contradictions between different requirements on the sensor performance. In a given chip size, a high granularity means more pixels in the same row to be switched on simultaneously for readout, and thus consumes more power. Moreover, the smaller pixel also leads to more rows to be processed in one read-out frame, slowing down the readout if the time to process one row is fixed. When a very short read-out time is required, a high parallelism is indispensable, which will inevitably increase the power consumption. Increased power dissipation in turn leads to an increased material budget.

2.6 Summary

Heavy charged particles lose their energy gradually in matter, mainly through ionization, releasing freed charge carriers along their traversing paths. These liberated charge carriers can be collected by the usually segmented electrodes of a detector. As a result, the impacting position, and even the energy loss, of a charged particle penetrating the detector, can be determined.

CMOS pixel sensors for charged particle detection, inspired by the CMOS image sensor, employ a thin, almost undepleted, epitaxial layer as the active volume. The signal charge carriers diffuse thermally in this layer and are collected by the sensing elements formed by regularly implanted N-wells in direct contact with the P-type epitaxial layer. The pixel-level read-out electronics can be placed very close to the sensing elements above the epitaxial layer. During the last decade, remarkable progress has been made to use these sensors for charged particle tracking. Benefiting largely from the fact that their manufacturing technology is a world wide standard, the cost of fab-

ricating CMOS pixel sensors is low and their turnover is fast. By employing the rolling shutter read-out architecture, combined with the on-chip signal digitizing and filtering functions, CMOS pixel sensors have offered a great balance between granularity, material budget, read-out speed, power consumption and radiation tolerance.

One should notice that the CMOS pixel sensor still needs to be proved to be compatible with the LHC running conditions. One important aspect is the radiation tolerance. Due to its charge collection mechanism of thermal diffusion, the CPS is relatively sensitive to the radiation induced bulk damages. Generally speaking, this can be improved by using an active volume with high resistivity. However, the manufacturing parameters are fixed by the foundries, which may depart from one would require for charged particle detection. As for the surface damages, the immunity of CMOS pixel sensors to ionizing radiation is improved steadily, as their development follows the trend of the CMOS industry to scale down the feature size. Using the process with a smaller feature size also leads to lower power consumption, as well as higher compactness. The penalties are the increased design difficulties for analogue circuits, and more importantly, the emerging of RTS noise.

In conclusion, the design of a CMOS pixel sensor involves a wide range of trade-offs to optimize its performances. And especially, the selection and exploration of a proper manufacturing process is of primary importance to push the potential of CPS to its best.

Chapter 3

The state-of-the-art CPS and new developments towards the ALICE ITS upgrade

As is discussed in Chapter 1, the state-of-the-art CMOS pixel sensors built with the 0.35 μm CMOS process cannot satisfy all the requirements of the ALICE-ITS upgrade. The requirements for both STAR-PXL and the new ALICE-ITS are compared in Table 3.1. From the table, it is clear that the main challenges for the new ITS come from the read-out speed and the radiation tolerance. In this chapter, an overview of the ULTIMATE sensor, designed for the STAR-PXL, is first given. Then, after addressing the features of a new 0.18 μm CMOS process, it is eventually demonstrated that the CPS based on this new process tends to break through the current limitations and is well adapted to the ALICE-ITS upgrade. Finally, based on the current achievements, an R&D roadmap towards a fast and power efficient CMOS pixel sensor dedicated to the ALICE-ITS upgrade is established.

Table 3.1: Comparison of the requirements of STAR-PXL and new ALICE-ITS, in terms of read-out speed (σ_t), intrisic spatial resolution (σ_{sp}) and radiation tolerance related to the total ionizing dose(TID) and non-ionizing particle fluence.

Expt-System	σ_t (μs)	σ_{sp} (μ)	TID[a] (MRad)	Fluence[a] (n_{eq}/cm^2)
STAR-PXL	$\lesssim 200$	~ 5	0.150	3×10^{12}
ALICE-ITS upgrade	$\lesssim 30$	~ 5	0.700	10^{13}

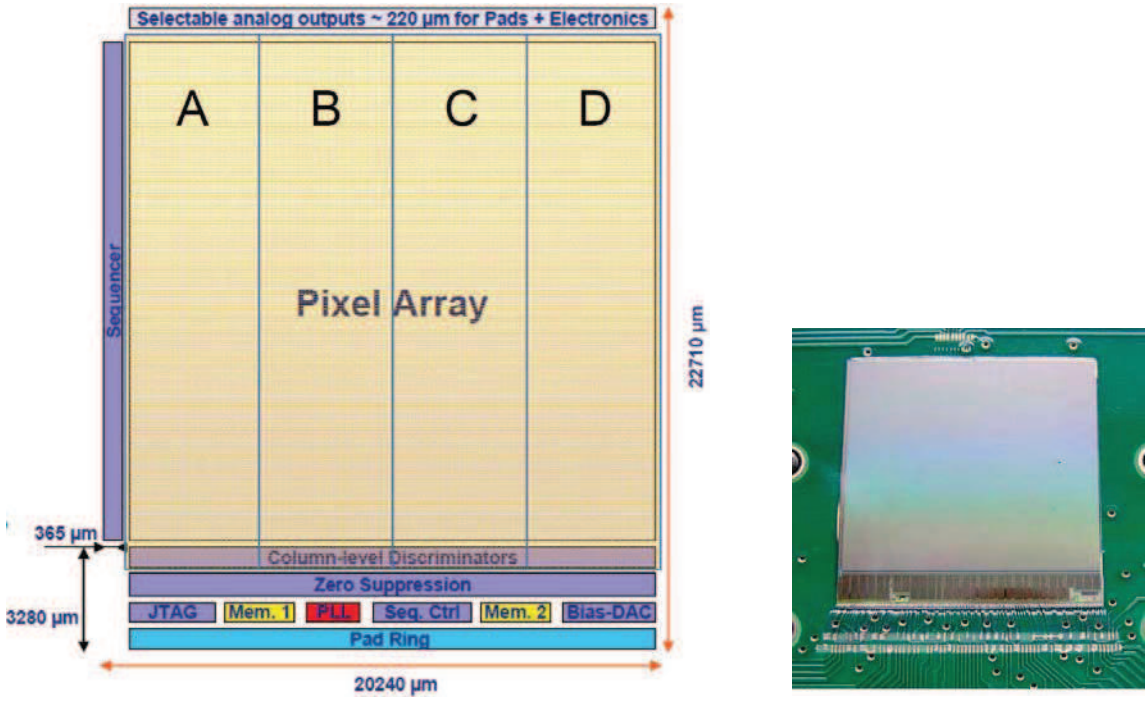
[a]Data taken from the technical design report of ALICE-ITS [16].

3.1 State-of-the-art CPS: the ULTIMATE sensor

The state-of-the-art CMOS pixel senor can be best represented by the ULTIMATE (aliased MIMOSA-28) sensor. It is a reticule size CMOS pixel sensor designed for the two inner layers of the STAR-HFT, allowing for a precise measurement of the displaced vertex. Given that the STAR-HFT is conceived with a similar purpose as the upgraded ITS of ALICE, the ULTIMATE sensor serves as a starting point for the development of CPSs dedicated to the upgraded ALICE-ITS.

3.1.1 Architecture overview

The architecture of the ULTIMATE sensor follows its forerunner MIMOSA-26, designed for the EUDET beam telescope [51]. MIMOSA-26 is the first reticule size MIMOSA sensor with digital output and integrated zero suppression. The design of the ULTIMATE sensor was optimized for the STAR-PXL environment [94].



(a) (b)

Figure 3.1: (a) Functional block diagram of the ULTIMATE sensor and (b) The picture of the sensor on its PCB.

The block diagram of the ULTIMATE sensor, together with its picture, is shown in Fig. 3.1. The sensor is fabricated in the 0.35 μm CMOS Opto process, provided by AMS (Austria Micro System), using 4 metal- and 2 poly- layers. The thickness of the epitaxial layer stretches out up to 20 μm with high-resistivity (> 400 Ohm·cm). The sensor has a matrix composed of 928 (rows) × 960 (columns) pixels with a pixel pitch of 20.7 μm, covering a sensitive area of $\sim$ 3.8 cm^2. The pixel features the in-pixel pre-amplifying and Correlated Double Sampling to achieve a high Signal-to-Noise Ratio. The pixel matrix is read out in the rolling shutter mode, with column-level discriminators to convert the analogue signals to binary values at a speed of 200 ns/row. The integration time is 185.6 μs [95]. These binary signals are then processed by a zero suppression logic to provide sparse outputs. The sparsified data is multiplexed onto two 160 Mbits/s LVDS[1] outputs. Operating at 3.3 V supply voltage, the power consumption is $\sim$ 160 mW/cm^2.

This architecture is capable to cope with a hit rate of 10^6 hits/cm^2/s. The sensor includes enhanced testability with large number of configurations to validate the functionality of each part (pixels, discriminators, zero suppression and data transmission). The on-chip DACs (digital-to-analog converters) for circuit biasing and the discriminator thresholds, the test mode selection and the configurations of the sequence control circuit are set via a JTAG[2] controller. An on-chip voltage regulator is used to provide the pixel clamping voltage, labelled "V_{CLP}" in Fig. 3.2(a), for the CDS operation, in order to minimize interference on this critical node [96]. The sensor is divided into 4 sub-arrays (from A to D in Fig. 3.1(a)), each having 240 columns. A single threshold setup is used for the 240 discriminators connected to one sub-array.

Pixel

The schematic of the pixel used in the ULTIMATE sensor is shown in Fig. 3.2(a). As introduced in Section 2.2, only NMOS transistors are allowed in the pixel circuitry. The sensitive part uses the self-biased architecture (diodes D_1 and D_2). The amplification stage following the sensing element is based on a common source (CS) amplifier. Biasing the load transistor of the amplifier (M_2) with another transistor (M_3) can increase

[1]LVDS stands for low voltage differential signaling. It is a standard for communicating at high speed in point-to-point applications

[2]JTAG stands for Joint Test Action Group, as defined by the IEEE Std.-1149.1 standard, it is an integrated method for testing interconnects on printed circuit boards (PCBs) that are implemented at the integrated circuit (IC) level.

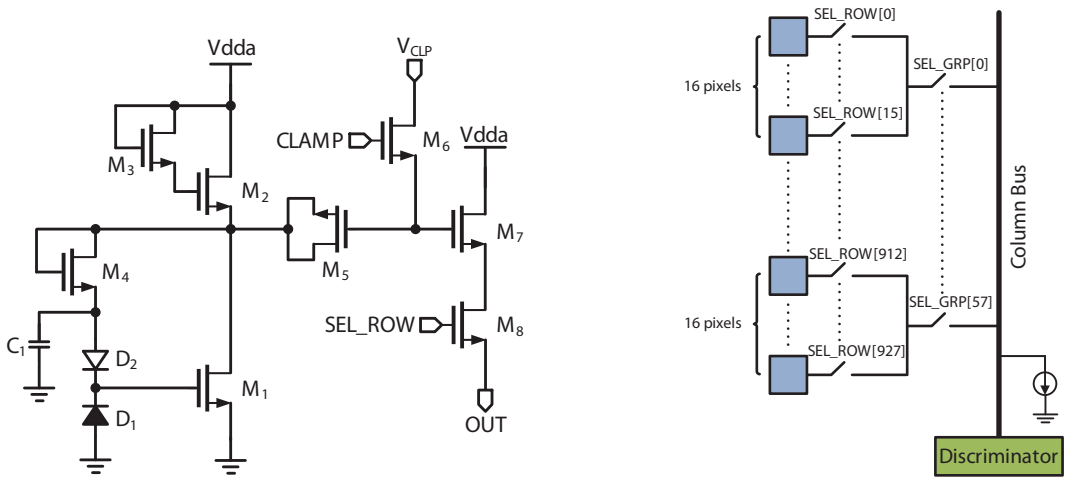


Figure 3.2: (a) Schematic of one pixel. (b) Each 16 pixels in a column are grouped together and selected by the SEL_GRP signal in order to reduce the parasitic capacitance seen by the output node.

the AC gain by about a factor of two [97, 98]. A low-frequency feedback, formed by the diode-connected transistor M_4 and capacitor C_1), is employed to compensate the leakage current of the collection diode (D_1) and to match actively the reverse bias of the diode to the working point of the amplifier [53]. More importantly, this feedback configuration ensures optimal working conditions for all $\sim 10^6$ pixels with respect to temperature changes, irradiation and process parameter variations [25]. In order to enhance the ionizing radiation tolerance, the feedback transistor (M_4) features an enclosed layout to reduce the edge leakage current [82, 99]. The MOS capacitor M_5 and the MOS switch M_6 form the in-pixel CDS element. They remove the offset and attenuate the low-frequency noise from its upstream circuitry by resetting the clamping node (gate of M_7) in each read-out cycle to a pre-defined voltage V_{CLP} through M_6. And the integrated signal is therefore superimposed on this pre-defined voltage value. M_7 is the input transistor of the output source follower, whose current source is located at the column end and shared sequentially by all the pixels in the same column. In order to achieve a reasonable time constant for stabilizing the signal sample from the pixel, each column is split into 58 groups of 16 pixels as shown in Fig. 3.2(b). With only one common switch connecting a pixel group to the column bus, the capacitance seen by the output node is reduced and is estimated to be ~ 4 pF.

Discriminator

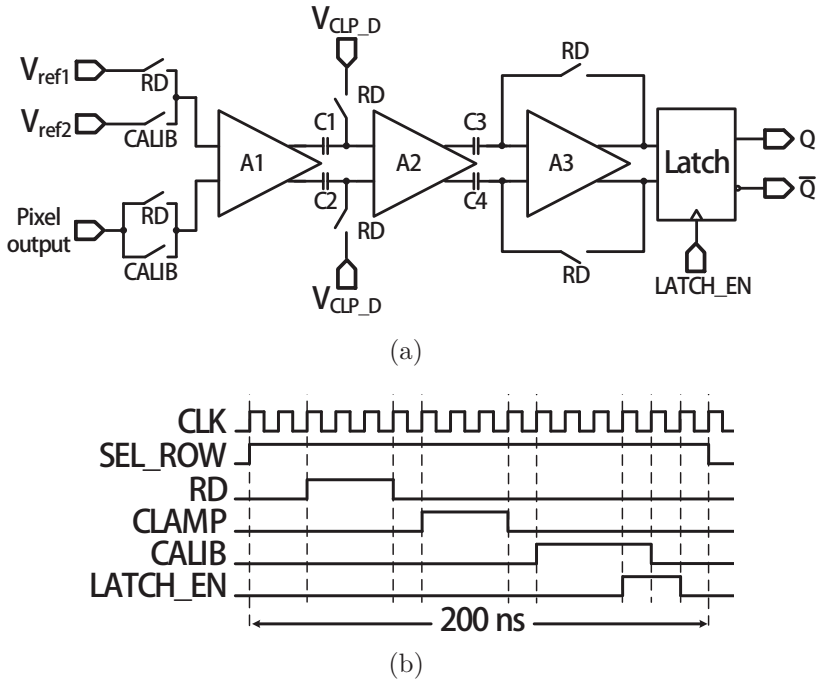


Figure 3.3: (a) Schematic of the discriminator. (b) The timing diagram.

Due to the small signal delivered by a pixel ($\leqslant$ 20 mV), a fully differential, offset compensated architecture of discriminator is chosen to provide the required high precision [100]. As sketched in Fig. 3.3(a), the discriminator consists of three auto-zeroed amplifying stages and a dynamic latch. The auto-zeroing is accomplished by applying two non-overlapping phases, i.e., the $CALIB$ phase and the RD phase, to the circuit, with one phase memorizing the amplifier offsets on the offset storage capacitors ($C1 - C4$) and the other phase cancelling the offsets. The $CLAMP$ signal controls the in-pixel CDS element in Fig. 3.2(a), which resets the pixel output. Following the timing diagram shown in Fig. 3.3(b), the discriminator subtracts the pixel output of the $CALIB$ phase, which represents the offset, from that of the $READ$ phase, which represents the integrated signal superimposed on the pixel offset. This inherent double sampling operation of the discriminator allows to remove the pixel-to-pixel offsets introduced by the pixel output source followers. The threshold voltage amounts to the difference between the two reference voltages V_{ref1} and V_{ref2}, injected at the discriminator input during the $READ$ phase and the $CALIB$ phase respectively. The

$LATCH\_EN$ signal activates the latch, which rapidly amplifies the difference between the pixel output signal and the threshold value, and a logical signal is given according to this difference.

In order to reduce the charge injection coming from nearly a thousand switches and to ensure a stable reference voltage, the 960 discriminators are sub-divided into 4 groups of 240 discriminators, corresponding to sub-arrays A - D in Fig. 3.1(a). Each group has its own threshold that can be adjusted by programming a separate DAC circuit. The test results showed a resolution better than 1 mV at the nominal row read-out frequency (5 MHz). The static current consumption of one discriminator is about 70 μA.

Zero suppression

In order to optimize the data bandwidth, the zero suppression logic is implemented right after the A/D conversion, where the digital signals are processed in parallel in 15 banks of 64 columns. Based on the "Sparse Data Scan" algorithm [101], the non hit pixels are skipped, leaving only the information from the hit pixels encoded in terms of string. Each string stands for $\leqslant 4$ contiguous pixels in a row, delivering a signal above the discriminator threshold. Within each bank, up to 6 strings can be memorized with their column addresses. Next, a second stage combines the outcomes of the 15 banks and keeps up to 9 strings per row. The results are then stored in a memory, which is split into 2 buffers, allowing to perform read and write operations simultaneously. The collection of sparsified data for a frame are serialized and sent out to the acquisition via two LVDS outputs running at 160 MHz, providing the total 320 Mbits/s data rate required to send out all data within the integration time. The memory depth, the maximum accepted strings per bank and per row are customized to adapt the STAR PXL environment. A more detailed discussion of the zero-suppression logic can be found in [102]

3.1.2 Performances

Laboratory test results

The sensors were first studied in the laboratory with a ^{55}Fe X-ray source in order to assess the analogue performances of the pixel, including noise, charge-to-voltage conversion factor (CVF), the charge collection efficiency (CCE), as well as the uniformity

of the pixel response. A good noise uniformity was observed across the ~ 4 cm^2 sensitive area and the average noise value amounts to $\lesssim 15$ e$^-$ of ENC at 30 - 35 °C. The pixel CVF is around 65 μV/e$^-$. For the most common case, the charge generated by the X-rays is shared among several pixels, forming a cluster. Nearly all the cluster charge is concentrated in a pixel group of 5×5. The seed pixel, defined as the one who has collected the largest amount of charge in a cluster, collects typically ~ 25 % of the total cluster charge.

The digital outputs were studied in the configuration where all discriminators were connected to the pixel array. The temporal noise and the fixed pattern noise, resulting from the pixels in combination with the discriminators, were measured for each sub-array. The average TN values amount to 0.9 - 1mV and the FPN values amount to 0.4 - 0.6 mV, varying slightly between different sub-arrays. The TN is mainly coming from the pixel array, whereas the FPN is dominated by the discriminator threshold dispersion. These values comply with the PXL requirements.

Beam test results

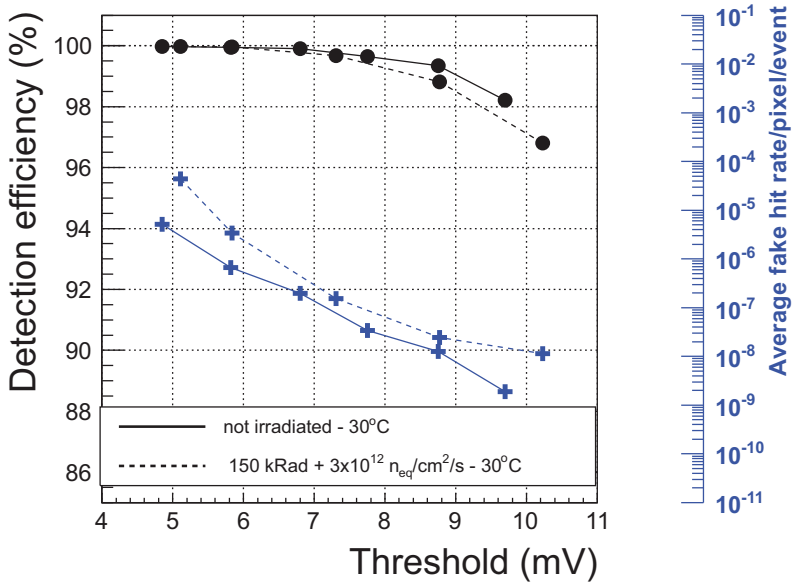


Figure 3.4: Performances of the ULTIMATE sensor before and after irradiation doses corresponding to the STAR-PXL requirements.

The detection performance of the ULTIMATE sensor was assessed at the CERN-SPS, with a ~ 120 GeV/c pion beam. A single point resolution better than 4 μm was

observed. In addition, the detection efficiency[3] and the fake hit rate[4] are displayed in Fig. 3.4 as a function of the discriminator threshold, before and after radiation doses corresponding to the STAR-PXL specifications (150 k Rad + 3×10^{12} $n_{eq}/cm^2/s$) at the expected operating temperature of 30 °C. The detection efficiency is maintained almost at 100 % for a very low average fake hit rate ($< 10^{-4}$), which is sufficient to allow the track reconstruction to remain unaffected by spurious hits due to electronic noise. The sensor was evaluated at both 3.3 V and 3 V analogue power supplies and the performances remained almost the same. Operating the sensor at 3 V analog power supply allows mitigating by 6 % the total power consumption, thus reducing it to ~ 150 mW/cm^2.

3.2 Building CPS with a new technology

Building a monolithic pixel sensor with a standard CMOS process is one of the prominent advantages of the CMOS pixel sensors. However, their industrial manufacturing relies on parameters optimized for commercial items which may depart substantially from those needed for charged particle detection. Therefore, the real potential for CMOS pixel sensors may be intrinsically confined by the available manufacturing processes. Fortunately, CMOS industry has evolved in a direction which allows CPS to progressively approach their real potential. The relatively recent availability of the 0.18 μm quadruple-well CMOS Image Sensor (CIS) process by *TowerJazz* has triggered a great interest [89].

3.2.1 The *TowerJazz* 0.18 μm quadruple well process

As mentioned in Chapter 2, the traditional CMOS pixel sensors allow only NMOS transistors being implemented inside the pixel, due to the parasitic charge collection node generated by any additional N-well hosting the PMOS transistors. The *TowerJazz* 0.18 μm CMOS process features an innovative option of the deep P-well, which can selectively "mask" the N-wells from the P-doped epitaxial layer [103,104]. As illustrated in Fig. 3.5, this additional implant prevents the collection of particle track induced charge by unrelated N-wells, i.e., the ones where PMOS transistors are embedded. Therefore, both NMOS and PMOS transistors are allowed for the pixel-level circuit,

[3]Detection efficiency is the probability of detecting an event if it has taken place
[4]Fake hit rate is the fraction of pixels generating a noise fluctuation above threshold

and the in-pixel processing capability and flexibility can be significantly enhanced, without compromising the pixel sensitivity.

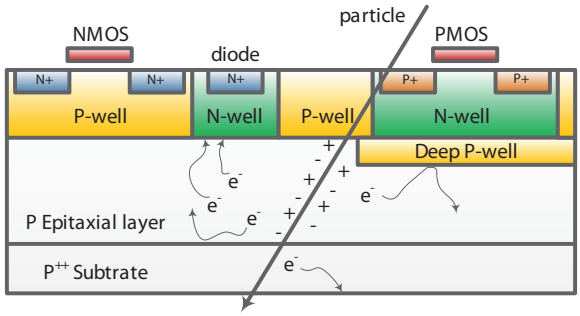


Figure 3.5: Cross section view of a CMOS pixel cell with the deep P-well implant. The deep P-well provides shielding to the N-well hosting the PMOS transistor.

Besides this unique feature of deep P-well, the mentioned process also provides some other features which tend to help address several key issues that have currently restricted the CMOS pixel sensors to be used in the ALICE environment. The most relevant ones that distinguish this technology from the formerly used 0.35 μm technology, and make it attractive for the implementation of the new ITS Pixel Chip, are listed below:

- An epitaxial layer of up to 40 μm thickness, with a resistivity higher than 1 kΩcm, is possible. This ensures a proper amount of signal charge needed for a reasonable SNR. And at the same time, due to the high resistivity, a sizeable part of the epitaxial layer can be depleted with a reverse bias voltage normally applied to the collection diode in a CMOS sensor (about 1 - 2 V). A larger depletion region in the active volume will benefit the charge collection and may improve the non-ionizing radiation tolerance;

- Due to the scaling down of the gate oxide thickness, this 0.18μm process may be substantially more resistant to the total ionizing dose than the 0.35 μm technology used for the ULTIMATE sensor;

- Six metal layers are available for dense interconnections. Combined with the smaller feature size, it allows to implement low power circuits with high density, both in pixel and at the chip periphery;

- The metal–insulator–metal (MIM) capacitor is allowed, which can provide an accurate capacitance value without dependence on the voltage applied.

R&D efforts have been made since 2011 by several groups, within the framework of the ALICE ITS upgrade, in order to investigate this new process. Various prototype chips were designed, fabricated and thoroughly tested, demonstrating that the CMOS pixel sensors based on the *TowerJazz* 0.18 μm CMOS process can provide satisfactory charge detection performance under the ALICE radiation environment. The following parts concentrate on the main R&D activities by the PICSEL group at IPHC.

3.2.2 The first exploration

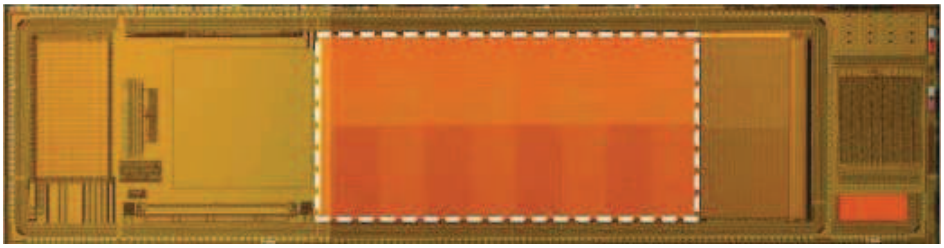
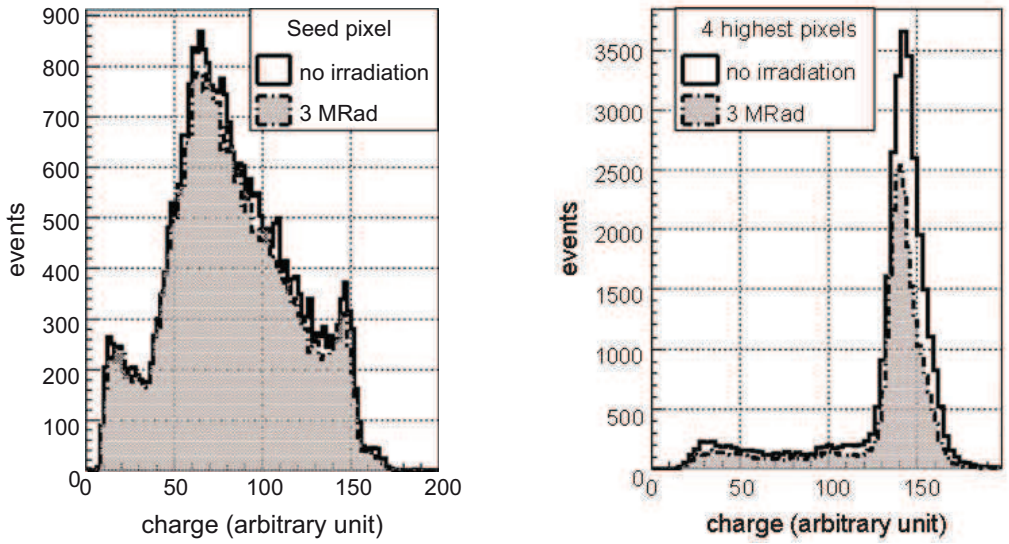


Figure 3.6: Image of MIMOSA-32. The area framed by a dashed white line indicate the main block of interest, including 32 pixel sub-arrays.

MIMOSA-32 is an exploratory prototype produced in the *TowerJazz*r 0.18 μm CMOS process mentioned above, based on a high-resistivity ($\rho > 1$ kΩ·cm), supposedly 18 μm thick, epitaxial layer. It was submitted for production in December 2011, and received from the foundry in March 2012. The chip consists of several blocks aimed at studying different aspects of CMOS pixel sensors in this new technology. The main block of interest in this thesis, enclosed within the white dashed line in Fig. 3.6, includes thirty-two small pixel arrays featuring different pixel designs (diode size, transistor implementation, in-pixel amplification structure and pixel dimension), covering an area of 5.2 mm $\times$ 3.3 mm. The goals are to compare their charge collection properties, which are poorly predictable by simulation tools, to evaluate various pre-amplifiers and to investigate the radiation tolerance of the technology. Twenty-two of these sub-arrays contain pixels having only a sensing diode and its biasing element connected to an NMOS source follower (as the structures shown in Fig. 2.4). It is worth mentioning that some pixel designs include the deep P-well implants, hosting the dummy PMOS transistors, in order to study their influence to the pixel charge collection performance. The other ten sub-arrays incorporate a pre-amplification stage inside the pixel. Most of the aforementioned sub-arrays consist of 16 $\times$ 64 square pixels with a pixel pitch

of 20 μm. There are also four sub-arrays composed of larger pixels elongated in one dimension. The read-out chain allows to select one sub-array at a time to be read out in the rolling shutter mode. With a clock frequency of 2 MHz, the time for reading out a full sub-array (integration time) is 32 μs [80, 89, 105, 106].



(a) (b)

Figure 3.7: The response to the ^{55}Fe X-rays illumination of a sub-array in MIMOSA-32 before irradiation (solid empty histogram) and after a TID of 3 MRad (dotted filled histogram). (a) The charge collected by the seed pixel alone and (b) the charge collected by the set of 4 pixels in a cluster with the largest signal. (Source [89])

The MIMOSA-32 sensors were first studied in the laboratory with a ^{55}Fe source. The noise measured ranges from $\sim$ 15 e^- to $\sim$ 20 e^- for various pixel architectures at room temperature. Fig. 3.7 displays the response of a sub-array to the ^{55}Fe X-ray illumination. This sub-array is composed of pixels of 3T structure, including dummy PMOS transistors embedded in the deep P-wells. The pixel pitch is 20 μm. Fig. 3.7(a) gives the distribution of the charge collected in the seed pixels of the clusters. It exhibits a small peak at large charge values, which originates from those X-rays impinging the chip in the vicinity of a sensing diode, resulting in a full charge collection (about 1640 e^-). And the highest peak in the middle indicates the most probable charge value collected by the seed pixel. Thus, it demonstrates that the seed pixel collects typically over 40 % of the total charge, resulting in an SNR over 30 as the most probable value. Fig. 3.7(b) shows the charge collected by the set of 4 pixels in a cluster with the largest

signal. Nearly all the cluster charge is concentrated in those 4 pixels. The figure shows also the distributions measured after an exposure of the chip to a TID of 3 MRad (in dotted filled histogram). No significant degradation is observed.

Table 3.2: Beam test results for selected pixel designs in MIMOSA-32.

Pixel	Irradiation	SNR (MPV)		Detection efficiency (%)	
		T=15 °C	T=30 °C	T=15 °C	T=30 °C
Simple 20×20 μm^2	0	32.3±0.4	31.4±0.6	99.84±0.07	99.64±0.16
	1 MRad + 10^{13} n_{eq}/cm^2	22.3±0.3	16.2±0.3	99.87±0.08	99.77±0.11
Deep P-well 20×20 μm^2	0	30.9±0.4	29.7±0.4	99.91±0.06	99.7±0.1
	1 MRad + 10^{13} n_{eq}/cm^2	22.6±0.4	19.3±0.2	99.92±0.08	99.87±0.07
Simple 20×40 μm^2	0	22.6±0.2	21.8±0.3	99.86±0.06	99.78±0.08
	1 MRad + 10^{13} n_{eq}/cm^2	13.9±0.3	10.9±0.1	99.51±0.25	97.99±0.25

Beam tests were performed in summer 2012 at the CERN-SPS, with with 60 - 120 GeV negatively charged pions. The performances of three selected pixel designs are summarized in Table 3.2, for sensors before and after radiation doses of 1 MRad combined with 10^{13} n_{eq}/cm^2 at two different coolant temperatures (15 °C and 30 °C) [80]. Two of the selected designs feature square pixels with a pitch of 20 μm, differing from each other in the existence of deep P-well implants. The third design consists of elongated pixels of 20 μm $\times$ 40 μm with no deep P-well implants. For the sake of radiation tolerance and single point resolution, the sensing elements of the elongated pixels were patterned in a staggered manner. In addition, the size of the sensing diode for the elongated design is 9 μm instead of 10.9 μm used in the two square pixel variants. The purpose of the elongated pixel is to investigate the possibility to reduce the number of rows, and thus increase the read-out speed without degrading significantly the resolution and detection efficiency. As can be seen in table 3.2, the detection efficiency is about 100% before irradiation, and remains nearly unchanged within 0.5% after irradiation. The only exception is for the elongated pixel, whose efficiency is lowered to $\sim$ 98% for radiation doses of 1 MRad combined with 10^{13} n_{eq}/cm^2 at 30 °C coolant temperature. This can be explained by the smaller collecting diodes used and

the longer distance between neighboring collecting diodes. These two factors lead to less efficient charge collection by the elongated pixels, resulting in a lower SNR and therefore affecting the detection efficiency. This efficiency loss could be mitigated with an optimization of the charge sensing system design. These results obtained with the MIMOSA-32 chip demonstrated a good potential of the *TowerJazz* 0.18 μm CMOS process for charged particle detection in the ALICE radiation environment.

3.2.3 Optimization of the in-pixel amplifier

MIMOSA-32 successfully validated the charge collection performances of the *TowerJazz* 0.18 μm CMOS process. However, the performances for pixels with the pre-amplifier were still not convincing. Given that a proper in-pixel pre-amplification is essential to maintain an excellent SNR through the whole read-out chain, this issue was therefore addressed by several following prototype chips. This section focuses the R&D efforts that were concentrated on the in-pixel pre-amplifier.

The emerging candidate: P25 in MIMOSA-32Ter

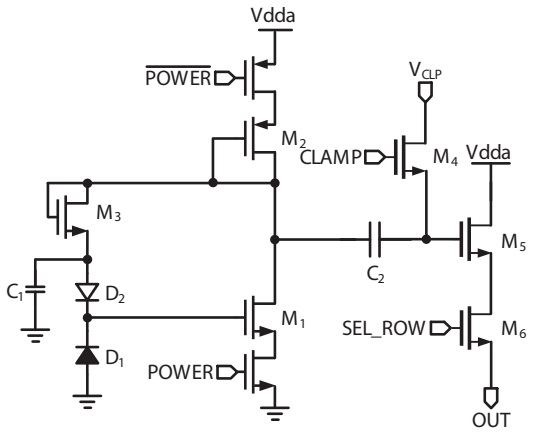


Figure 3.8: The schematic of the pixel P25 in MIMOSA-32Ter.

Extrapolating from the MIMOSA-32, another prototype chip, named MIMOSA-32Ter, was submitted in July 2012 and received from the foundry in October 2012. Like MIMOSA-32, the main block of interest in MIMOSA-32Ter features 32 sub-arrays with various pixel designs. Fifteen of the sub-arrays contain 20 μm $\times$ 20 μm pixels with integrated pre-amplifiers, among which a pixel named P25 emerged as the most promising candidate for further development. The schematic of the pixel P25 is shown

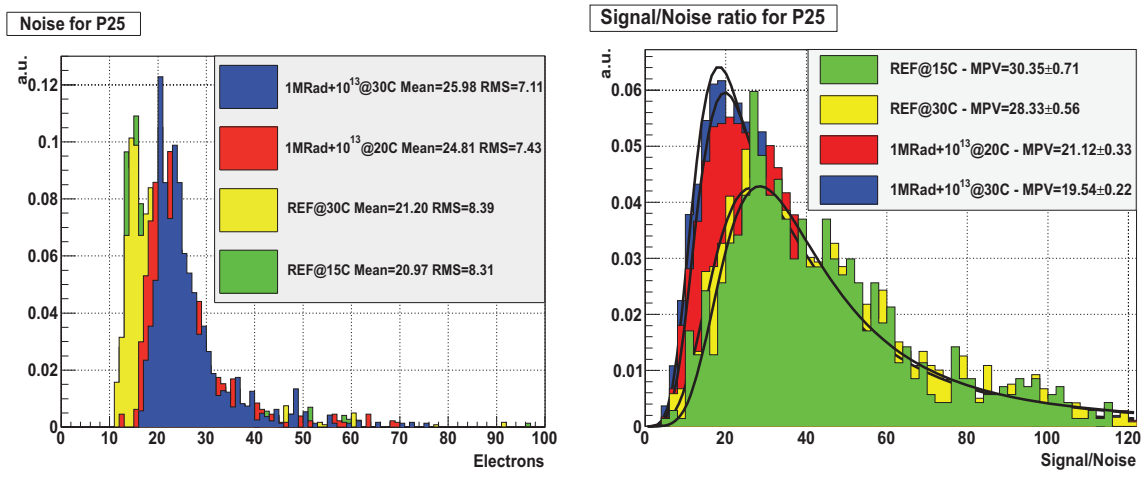
in Fig. 3.8. The structure of its pre-amplifier is similar to that used in the pixel of the ULTIMATE sensor (see Fig. 3.2(a)), except that the load is replaced by a single diode-connected PMOS transistor (M_2 in Fig. 3.8). Another difference of P25, departing from the ULTIMATE pixel, is the use of an MIM (Metal-Insulator-Metal) capacitor as the coupling element (C_2 in Fig. 3.8). Unlike the MOS capacitor, the MIM capacitor does not require a voltage biasing to sustain its capacitance value. This is beneficial for the circuit design when the supply voltage scales down with the feature size, reducing the voltage margin that can be utilized to bias a MOS capacitor. However, the capacitance density of an MIM capacitor is usually lower than that of a MOS capacitor. The *POWER* and $\overline{POWER}$ are two complementary signals used for switching ON/OFF the pre-amplifier.

The beam test of MIMOSA-32Ter was performed in November 2012. Fig. 3.9 gives the noise distributions of the pixel P25, before and after radiation doses of 1 MRad TID combined with 10^{13} 1 MeV n_{eq}/cm^2 under different coolant temperatures. The average noise value slightly exceeds 20 e^- before irradiation, about 10 % higher than the pixel featuring a source follower [89, 107]. Table 3.3 summaries the SNR and detection efficiency values for P25 under different radiation and coolant temperature environments. The detection efficiency stays above 99 % even for the harshest condition expected for the ALICE-ITS upgrade (1 MRad + 10^{13} 1 MeV n_{eq}/cm^2 at 30 °C).

Table 3.3: Beam test results for P25 in MIMOSA-32Ter.

Radiation dose	0 MRad + 0 n_{eq}/cm^2		1 MRad + 10^{13} n_{eq}/cm^2	
Coolant temperature	15 °C	30 °C	20 °C	30°C
SNR	30.4 ± 0.7	28.3 ± 0.6	21.1 ± 0.3	19.5 ± 0.2
Detection efficiency	99.86 ± 0.14 %	99.59 ± 0.14 %	99.34 ± 0.19 %	99.35 ± 0.13 %

The study was then followed by an offline beam data analysis by applying a single discriminating threshold to all the pixels, resulting in binary cluster information. This analysis allows to emulate the behavior (detection efficiency, fake hit rate, spatial resolution) of a real size binary output sensor as a function of threshold value. For a practical threshold set (5 - 7 times of the average noise value), the emulated efficiency is above 99 % for all radiation doses and the spatial resolution is $\lesssim 4$ μm, which are well inline with expectation for a 20 μm pitch, binary output pixel. However, the emulated fake hit rate is significantly higher than that was measured with sensors fabricated in a 0.35 μm process [25, 108], staying above 10^{-4} for all the practical threshold values [89].



(a) (b)

Figure 3.9: (a) The noise distribution and (b) the SNR distribution for the cluster seed pixel of P25, before and after radiation doses of 1 MRad combined with 10^{13} n_{eq}/cm^2 at two different coolant temperatures.

A more detailed analysis indicated that the noise excess is due to several percent of the pixels exhibiting RTS like noise, leading to a non-Gaussian distribution of noise with a positive skew as shown in Fig. 3.9(a). Fig. 3.10 gives the signal histogram of one pixel in the P25 sub-array, which exhibits clearly the behavior of a two level RTS noise. The next step of the R&D is expected to mitigate this effect and downscale the fake hit rate to an acceptable level by optimizing the in-pixel transistors' geometry.

Further optimization of P25

An engineering run including 26 prototype chips was submitted in March 2013, of which 10 chips were developed by the PICSEL group in order to validate different building blocks of the final design proposed for the ALICE-ITS upgrade. One chip, named MIMOSA-32FEE1, integrates numerous pixel variants of the P25 design in order to search for the optimized transistor geometry for the pre-amplifier. The chip was measured in laboratory and the study revealed that the RTS noise can be mitigated by avoiding very small dimensions for the pre-amplifier's input transistor. Fig. 3.11 shows the noise distributions of two different pixel designs. One is the reference design (the same as P25 in MIMOSA-32Ter) using a minimum gate length (0.18 μm) for the pre-amplifier's input transistor (M_1 in Fig. 3.8). The other is a modified design,

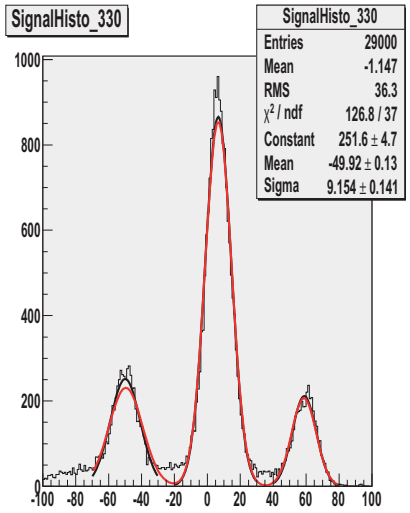
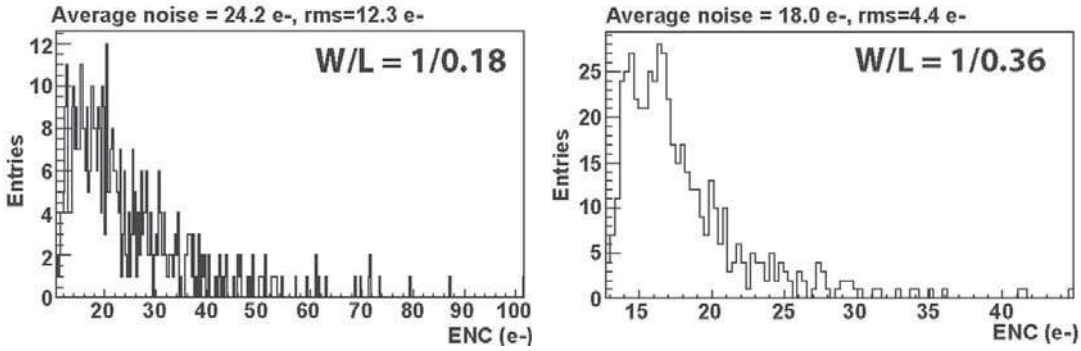


Figure 3.10: The signal histogram of a single pixel in the P25 sub-array. The two peaks presented on both sides of the main peak indicate the existence of RTS noise.

featuring a doubled gate length for the input transistor as compared to the reference design. The latter clearly has a much reduced extension of the right tail, exhibiting a more Gaussian like distribution. And the noise dispersion in Fig 3.11(b) was reduced by almost three times.



(a) (b)

Figure 3.11: Noise distributions for (a) the reference design in MIMOSA-32FEE1 and (b) the pixel variant featuring a doubled length of the pre-amplifier's input transistor.

These observations were further verified by another prototype chip, with the name of MIMOSA-22THR-A1, included in the same engineering run. MIMOSA-22THR-A1 is a binary output sensor with integrated end-of-column discriminators. One of its sub-arrays, named S2, contains the same modified pre-amplifier design mentioned above.

The beam test was performed with the electron beam at DESY[5]. As shown in Fig. 3.12, the sub-array S2 can achieve a particle detection efficiency higher than 99.5 %, and at the same time the fake hit rate can be kept at an acceptable level of $\sim 10^{-5}$ or below [109].

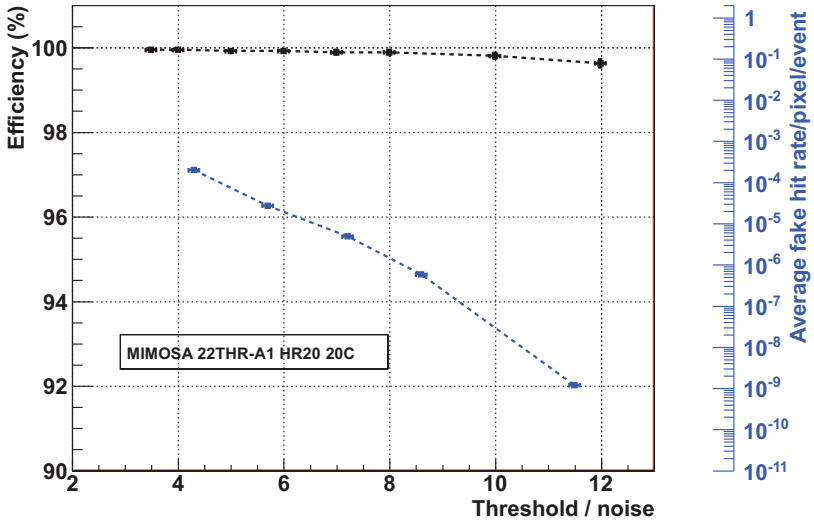


Figure 3.12: The detection efficiency and fake hit rate measured with the electron beam at DESY, for the sub-array S2 in MIMOSA-22THR-A1.

3.3 A roadmap to ASTRAL

The R&D efforts presented in the previous sections demonstrate that the *TowerJazz* 0.18 μm CMOS process has great potential to build a CMOS sensor adapted to the ALICE radiation environment, offering satisfactory particle detection performances. The remaining challenge is to explore and verify a fast readout architecture that is capable of coping with the expected data rate in the upgraded ALICE.

As mentioned in Section 2.5, the rolling shutter read-out offers a proper balance between speed and power consumption. However, in order to achieve the spatial resolution required by the upgraded ITS, a high granularity is necessary. If the dimension of the final sensor is assumed to be ~ 1 cm in the column direction, hundreds of pixel rows need to be read out in a single frame. For a typical row processing time of ~ 200 ns

[5]DESY (Deutsches Elektronen-Synchrotron: German Electron Synchrotron) is a national research center in Germany that operates particle accelerators used to investigate the structure of matter

as in the ULTIMATE sensor, to read out the whole sensor row by row leads to an integration time on the order of ~ 100 μs. Therefore, new strategies were explored to accelerate the current column-parallel readout. These strategies include:

- elongating the pixel in one dimension to decrease the number of rows to be read out;
- reading out two or four rows simultaneously instead of just one;
- subdividing the matrix in four to eight sub-areas read in parallel.

It is worth mentioning that increasing the degree of parallelism is at the expense of increasing proportionally the power consumption, which may exceed the requirement of the new ALICE ITS.

Another approach, profiting from the new *TowerJazz* 0.18 μm CMOS process, tends to diminish the dilemma between speed and power consumption by achieving a full digital matrix treatment. Therefore, the AROM[6] prototypes were proposed and developed to study the concept of binary pixel by integrating a discriminator inside the pixel [110]. Fig. 3.13 compares the column-level discrimination, used in the state-of-the-art MIMOSA sensor, and the pixel-level discrimination, employed by the AROM sensor. The AROM sensor sets the analog signal processing inside one pixel, and it does not require a power consuming in-pixel source follower (biased at ~ 50 μA in the ULTIMATE sensor) to drive the long distance column line. As a result, the static current consumption can be largely reduced as compared to the column-level discrimination. Furthermore, by dealing with only the small local parasitics in the analog readout chain, the row processing speed can be accelerated.

Based on the AROM sensor, an R&D roadmap towards the sensor called ASTRAL[7] was established [111]. The ASTRAL sensor features one of the architectures that have been proposed for the ALICE-ITS upgrade [26]. Following the roadmap shown in Fig. 3.14, we first started with the feasibility study by prototyping the chip AROM-0. The development was pursued with several AROM-1 chips to optimize the pixel design and verify the upstream architecture of the ASTRAL sensor. In parallel, a new zero suppression logic, called SUZE-02, was being realized. Extending the architecture of AROM-1 to the full scale pixel array and combining it with the SUZE-02 circuit result

[6] AROM stands for Accelerated Read-Out Mimosa
[7] ASTRAL stands for AROM Sensor for the inner TRacker of ALICE

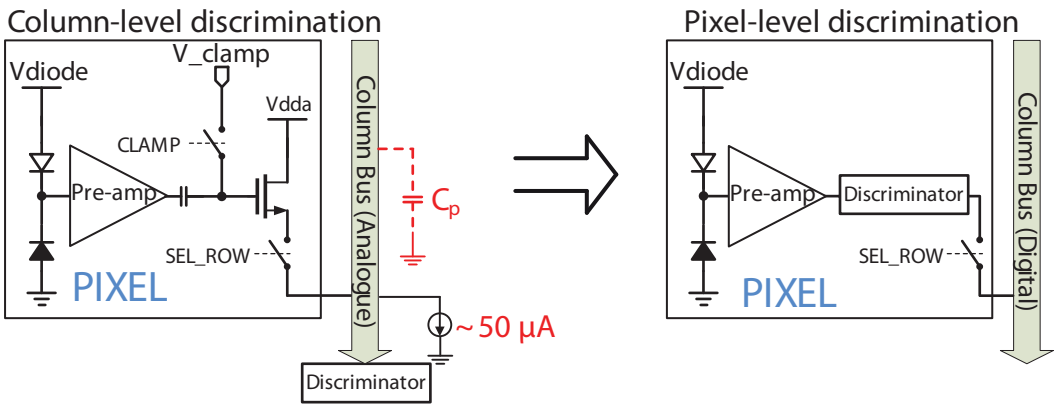


Figure 3.13: Column-level discrimination vs. pixel-level discrimination.

in the FSBB-A[8] sensor, which features a sensitive area exceeding 1 cm^2. The final ASTRAL sensor, as shown in Fig. 3.15, will be composed of 3 FSBB-A chips operated in parallel and multiplexed at their output nodes [112]. It is noted that the sequence generator circuitry of the ASTRAL sensor, shifting and driving the control signals for the pixel array, is placed at the bottom of the pixel array, whereas that of the ULTIMATE sensor is located alongside the pixel array (see Fig. 3.1). By doing this, the inactive area between neighbouring FSBBs is eliminated. However, it increases the complexity to distribute the row control signals. In other words, these control signals must be first transmitted vertically and then distributed horizontally to the corresponding rows.

3.4 Summary

The CMOS pixel sensor is a very promising technology for the upgrade of ALICE-ITS. As compared to the other experiments at LHC, the ALICE has less stringent radiation tolerance and read-out time requirements, and at the same time high granularity and low material budget are privileged for its new ITS design. The ULTIMATE sensor, designed for the STAR-PXL detector, represents the state-of-the-art development of CPS for vertexing and tracking detection systems in particle and nuclear physics. Unfortunately, the foreseen ALICE running condition imposes more stringent requirements on the sensor chip as compared to the STAR experiment does, especially concerning the read-out speed and radiation tolerance. Therefore, R&D efforts were concentrated on

[8]FSBB-A stands for Full Scale Building Block for ASTRAL

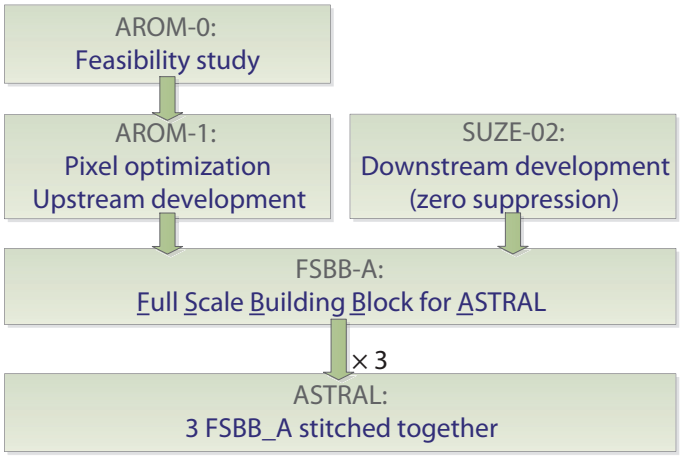


Figure 3.14: The R&D roadmap towards the ASTRAL sensor dedicated to the ALICE-ITS upgrade.

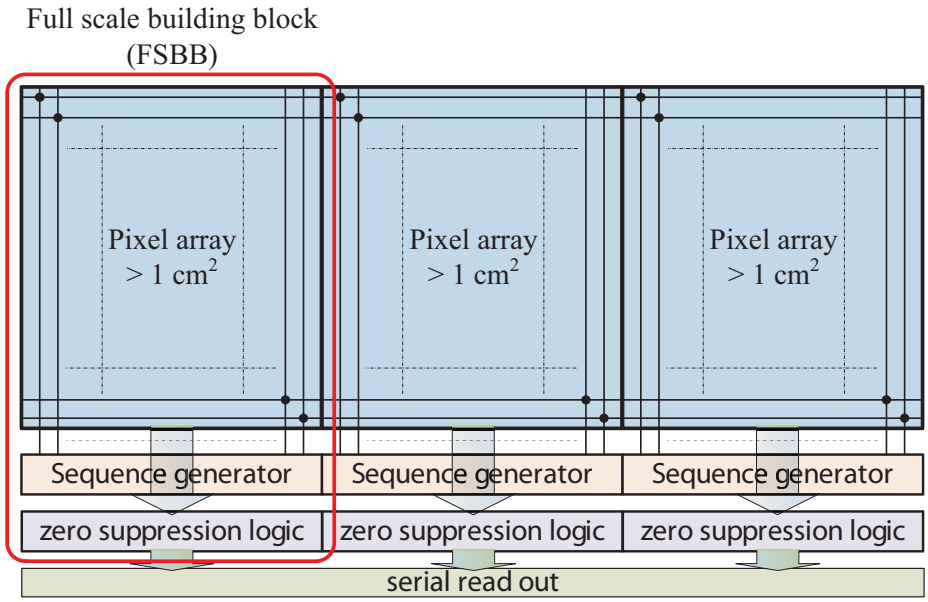


Figure 3.15: The architecture of the proposed ASTRAL sensor for the ALICE-ITS upgrade.

investigating a 0.18 μm quadruple-well CIS process, provided by *TowerJazz*. By using this new technology, it tends to overcome the limitations of the ULTIMATE sensor based on the 0.35 μm technology.

In this chapter, the ULTIMATE sensor is first reviewed, whose architecture serves as starting point for the future designs dedicated to the ALICE-ITS upgrade. Then some main R&D efforts made by the PICSEL group within the framework of the ALICE-

ITS upgrade are presented, demonstrating the *TowerJazz* 0.18 μm CMOS process as a qualified candidate for this application. Satisfactory charge detection performances were achieved for sensors with in-pixel pre-amplification and CDS, even after the radiation doses corresponding to the requirements of the upgraded ITS. Finally, profiting from the innovative option of deep P-well provided by the foundry, the idea of AROM sensor is introduced to accelerate the readout and at the same time to reduce the power consumption, by integrating a discriminator inside each pixel. Based on the AROM sensor, a R&D roadmap towards the ASTRAL sensor, which is the final sensor we have proposed for the ALICE-ITS upgrade, is outlined. Following the roadmap, this thesis contributes mainly to the development of the AROM sensor. The following chapters will focus on the design and measurement of various AROM prototypes.

Chapter 4

Feasibility study: AROM-0

Following the roadmap presented in the previous chapter, the development was initiated by the prototype chip AROM-0, in order to validate the feasibility of in-pixel discrimination with a small pixel area, satisfying the spatial resolution and power consumption requirements of the upgraded ALICE ITS. The chip was implemented in an engineering run in March 2013, the same one as mentioned in Section 3.2.3. Various pixel-level circuit structures were integrated in separate small-sized pixel arrays, in order to search for the best candidate. As compared to the ULTIMATE like sensors with column-level discrimination, the AROM sensor was expected to be twice as fast, and at the same time with significantly reduced power consumption.

4.1 Chip implementation

The AROM-0 chip, whose microscope picture is shown in Fig. 4.1, has 6 individual pixelated arrays, each with a dedicated purpose. Three different topologies of discriminators, named V1, V2 and V3, are explored in separate 32 $\times$ 36 single-row readout pixel arrays. The discriminator V2 is also implemented in a 16$\times$18 pixel array with a double-row readout scheme. The remaining two arrays are used to study the performance of the latch circuit. Each array can be addressed and enabled at a time for operation.

Fig. 4.2 illustrates a typical 32 rows array. The main pixel array contains 32 $\times$ 32 digital pixels. Each digital pixel is composed of a charge collection diode (sensing diode), a pre-amplifier and a discriminator. In order to calibrate the CVF (charge-to-voltage conversion factor), alongside the main array, there are also 4 columns of

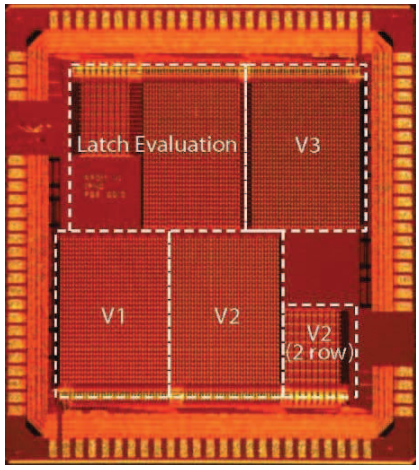


Figure 4.1: The microscope image of AROM-0.

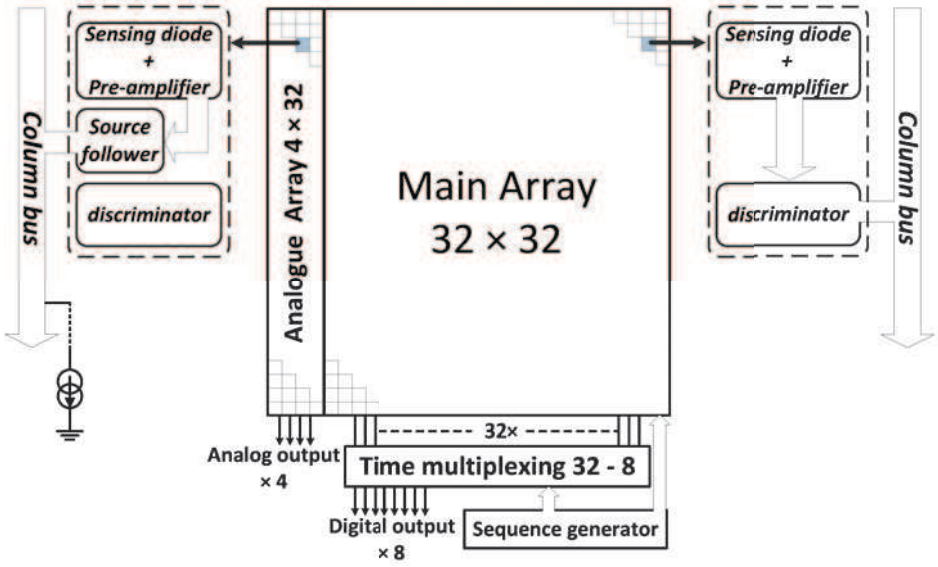


Figure 4.2: The structure of a typical 32-row sub-array.

pixels, called analogue pixels, with an additional source follower in each pixel to drive the analogue signal from the pre-amplifier to the column end for readout. It is noted that the discriminator is implemented in the analogue pixel to reproduce the possible cross coupling and parasitic effects from the discriminator element, since similar effects should exist in the digital pixels and need to be taken into account. The sequence required for the pixel operation and signal output is generated off chip and distributed by the shift registers (the sequence generator circuit) implemented at the bottom of the pixel array. The 32-bit outputs from the main pixel array are sent out by 8

channels using the time-division multiplexing. The four analogue pixel columns have their own output channels. It is worth mentioning that the 16 rows arrays have a similar architecture, and due to the double-row readout, their output data rate is the same as the 32 rows arrays.

4.2 Pixel design

The pixel pitch of the AROM sensor should comply with the spatial resolution requirement of the ALICE-ITS upgrade as mentioned in Section 1.2. Thus, the main challenge of the pixel design is to achieve a high precision signal discrimination inside a small pixel area. In this section, the design of the pixels in AROM-O, confronting the challenge, is presented.

4.2.1 Pixel pitch

The pixel pitch sets a primary constraint on the design of a complex pixel, since it defines intrinsically the complexity of the pixel-level functionalities. In order to achieve a spatial resolution ~ 5 μm, a pixel pitch in the order of 20 μm - 30 μm is expected for a binary output CMOS pixel sensor. The selection of the pixel pitch is not a main concern of this thesis, and its study is only briefly reviewed.

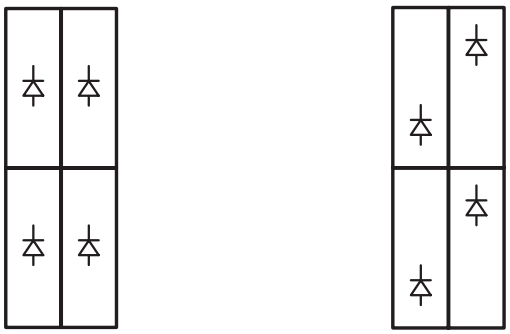


Figure 4.3: Elongated pixels (a) without staggered diode placement and (b) with staggered diode placement.

As mentioned in Section 3.3, to elongate the pixel in the column direction allows to reduce the row number, and thus can be adopted as a strategy to optimize the time

resolution for the rolling shutter CPS. In fact, the requirement of fast readout is the main driving force to employ the elongated pixel geometry in the AROM sensor. It is worth mentioning that the sensing diodes of elongated pixels are normally arranged in a staggered manner, as shown in Fig. 4.3(b). The staggered diode placement tends to equalize the resolutions in both dimensions. In addition, it avoids long diffusion path for the charge carriers to reach the collection diodes in the elongated direction. Hence, the staggered pattern tends to be less sensitive to the lifetime degradation of the charge carriers resulting from the bulk damages. The first study of the elongated pixels in the *TowerJazz* 0.18 μm technology was performed with the MIMOSA-32 prototype, which integrated a sub-array composed of 20 μm $\times$ 40 μm pixels with a staggered diode pattern. Then in the MIMOSA-32Ter prototype, the pixel with the longitudinal dimension of 33 μm was explored. The study was further pursued in the chip MIMOSA-34 [109], where different combinations of the pixel pitches and the sensing diode areas were studied. Due to the analogue readout of these chips, additional data post-processing is needed to emulate the behavior of a binary output CPS. The reprocessed single point resolution for some selected pixel designs are summarized in Table 4.1 [113, 114]. The information of the ULTIMATE sensor is also included in the table for comparison purpose. Based on these results, the pixel with an area of 22 μm $\times$ 33 μm and staggered diode pattern was chosen for the AROM-0 and also as a baseline for the ALICE-ITS proposed sensor [89].

Table 4.1: Single point resolution corresponding to the binary cluster encoding for different pixel dimensions.

Process	Chip name	Pixel size (μm^2)	σ_{sp} (μm)
AMS 0.35 μm	ULTIMATE	20.7 $\times$ 20.7	3.7 $\pm$ 0.1
TowerJazz 0.18 μm	MIMOSA-32	20 $\times$ 20	3.2 $\pm$ 0.1
	MIMOSA-34	22 $\times$ 33	$\sim$ 5
	MIMOSA-32	20 $\times$ 40	5.4 $\pm$ 0.1
	MIMOSA-34	22 $\times$ 66	$\sim$ 7

4.2.2 Sensing system

The sensing system includes the sensing diode and the pre-amplifier, which defines fundamentally the charge collection property and the SNR of the sensor. The sensing system used in AROM-0 adopted directly the design of P25 in the MIMOSA-32Ter chip

(see Section 3.2.3), which was the most promising one when AROM-0 was submitted.

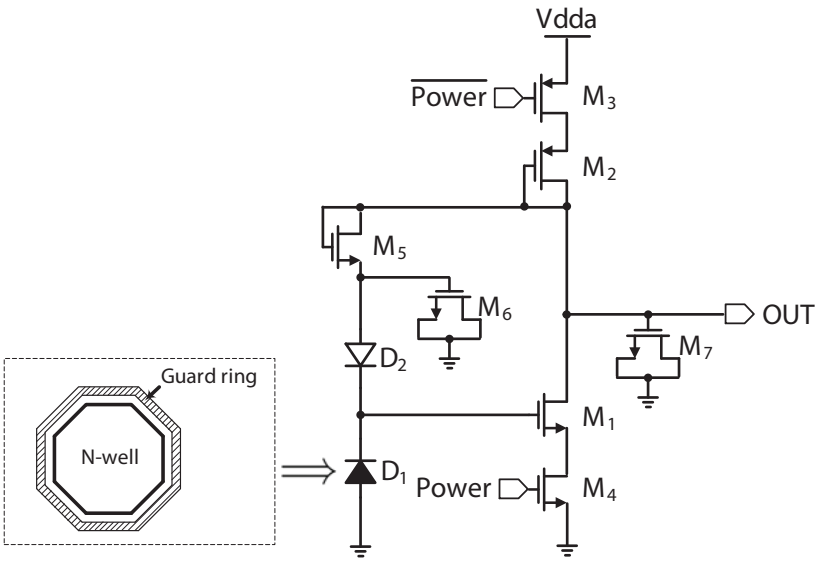


Figure 4.4: Schematic of the sensing system in AROM-0.

As illustrated in Fig. 4.4, the floor plan of the sensing diode (D_1) has an octagonal shape, with a total N-well area of about 11 μm^2. The diode is surrounded by a guard ring for protection. The pre-amplifier has a similar structure as the one used in the ULTIMATE sensor. However, the use of a biasing transistor for the load transistor to boost the gain, as in Fig. 3.2(a), is not suitable for the new design in the 0.18 μm process. This is because the supply voltage scales down from 3.3 V, in the 0.35 μm technology, to 1.8 V in the 0.18 μm technology. And the lower supply voltage restricts the dynamic range of the amplifier. By taking advantage of the unique feature of deep P-wells in the new process, a PMOS transistor (M_2 in Fig. 4.4) is used here as the load of the pre-amplifier. Consequently, a proper balance between the gain and the dynamic range can be achieved. M_6 and M_7 are two MOS capacitors, used for low-pass filtering. M_3 and M_4 are MOS switches, which can turn off the amplifier when the pixel is not addressed for readout.

The replicas of the same sensing system as in Fig. 4.4 were integrated in the prototype chip MIMOSA-32FEE1 (see Section 3.2.3) as the reference design. Besides the sensing system, the pixel in MIMOSA-32FEE1 also contains the CDS element and a source follower to buffer the signal. The measured average ENC of these replicas is about 24 e$^-$. With a CVF about 63 μV/e$^-$, the noise voltage at the output of the pre-amplifier is about 1.5 mV. In order to maintain a satisfactory SNR through the

whole read-out chain, the noise voltage from the discriminator circuit should contribute marginally to the total noise of the pixel circuit.

4.2.3 Discriminator design

In an area as small as 22 μm $\times$ 33 μm, the pixel of AROM-0 contains a discriminator in addition to the sensing diode and the pre-amplifier. The pixel is expected to be read out in 100 ns, and thus a high speed of the discriminator is required. Furthermore, the discriminator circuit should be carefully trimmed to provide a high, but not superfluous, precision, since redundant precision will inevitably increase the circuit area and power consumption. In this section, a brief introduction to the design of a fast and high precision comparator is first given, based on which the three topologies of the in-pixel discriminators implemented in AROM-0 are described. Then, the working principle of the discriminator is presented, followed in the end by the design of the main building blocks of the discriminators.

High-speed discriminator design: the multi-stage approach

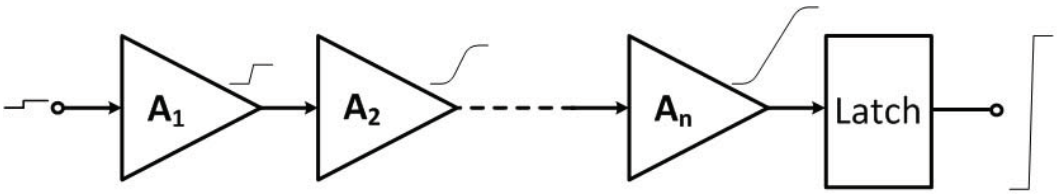


Figure 4.5: Conceptual illustration of a comparator formed by a number of cascaded amplifying stages and a latch.

The discriminator used for the CMOS pixel sensor is practically a comparator circuit that determines whether an input signal is larger than a pre-defined threshold or not. To use a number of cascaded low-gain amplifying stages followed by a regenerative latch circuit, as conceptually illustrated in Fig. 4.5, is the most efficient and widely used way to build a fast, high-precision comparator [115, 116]. In such a comparator, the input signal is amplified stage by stage, resulting in a signal amplitude large enough to be resolved by the latch circuit. Given that a low-gain amplifier can generally provide a large bandwidth, the propagation delay of the signal in the amplifying chain is kept small as compared to using a single amplifier with the same total gain, and consequently the high speed is achieved.

To see why the multi-stage approach can be fast, consider the simplified case of using the first-order amplifier for each amplifying stage in Fig. 4.5. The transfer function of a first-order amplifier is given by

$$A(j\omega) = \frac{A_0}{1 + j\omega/\omega_c} \tag{4.1}$$

where A_0 is the DC gain and ω_c is the cutoff frequency of the amplifier. The overall transfer function of the n stages is given by

$$A_n(j\omega) = (\frac{A_0}{1 + j\omega/\omega_c})^n \tag{4.2}$$

The -3 dB frequency of the transfer function (4.2) can be obtained by solving the equation

$$|A_n(j\omega_{-3dB,n})| = \left|(\frac{A_0}{1 + j\omega_{-3dB,n}/\omega_c})^n\right| = (\frac{A_0}{\sqrt{1 + (\omega_{-3dB,n}/\omega_c)^2}})^n = \frac{A_0^n}{\sqrt{2}} \tag{4.3}$$

and the result is

$$\omega_{-3dB,n} = \omega_c\sqrt{2^{1/n} - 1} = \frac{GBW\sqrt{2^{1/n} - 1}}{A_0} \tag{4.4}$$

where GBW is the gain-bandwidth product of the first-order amplifier.

If the transfer function (4.2) is approximated by a first-order transfer function, with the cutoff frequency as expressed in (4.4), the time constant of the system can be given by

$$\tau_n = \frac{1}{\omega_{-3dB,n}} = \frac{A_0}{GBW\sqrt{2^{1/n} - 1}} \tag{4.5}$$

which can be used as a figure of merit to evaluate the speed of the system.

Then consider the case when the n-stage amplifiers are replaced by a single first-order amplifier with the same overall gain of

$$G = A_0^n \tag{4.6}$$

Here, for simplicity, a constant GBW is assumed for all the mentioned amplifiers, and the bandwidth can be traded for gain. As a result, the time constant of the single

amplifier, with a gain of G, is given by

$$\tau_{single} = \frac{G}{GBW} = \frac{A_0^n}{GBW} \tag{4.7}$$

One can use the ratio of (4.7) and (4.5), expressed by (4.8), to compare the speed between the single-stage approach and the multi-stage approach.

$$\frac{\tau_{single}}{\tau_n} = A_0^{n-1}\sqrt{2^{1/n} - 1} \tag{4.8}$$

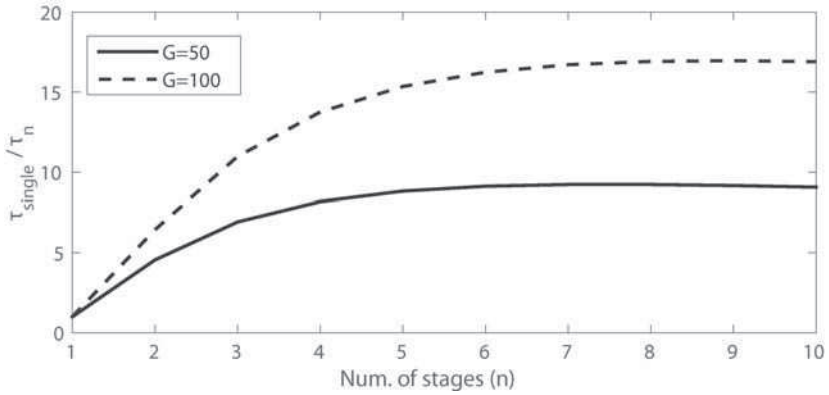


Figure 4.6: The time constant ratio between the single stage approach and multiple stage approach, as a function of stage number. The total gain G is set to 50 (solid line) and 100 (dotted line), respectively.

Fig. 4.6 gives the plots of (4.8) as a function of n, when the total gain G is set to 50 and 100 respectively. It can be seen that using 3 identical amplifying stages to achieve an overall gain of 50 is more than five times faster than the single-stage approach. And the high speed advantage of the multi-stage approach is more pronounced when a very high gain is required. In fact, an optimum number of stages n exists for the fastest response [115, 117]. However, this optimum is very broad and is not a strict rule for a practical design. For a total gain less than 100, the number of stages n typically ranges between 2 and 4.

Offset cancellation techniques

The resolution for the comparator mentioned above is mainly defined by the input referred offset caused by the process variation. In high-precision applications, offset cancellation techniques are mandatory [118]. The offset from the amplifier can be

cancelled, or largely removed, by the offset storage techniques, and the offset from the latch circuit is attenuated by the overall gain of the amplifying stage (stages).

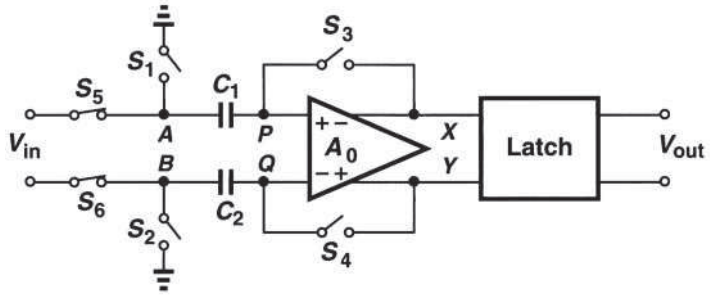


Figure 4.7: The comparator employing IOS.

Fig. 4.7 illustrates a comparator employing the Input Offset Storage (IOS) technique. It has three modes of operation: offset cancellation, tracking, and latching. During offset cancellation, S_1 - S_4 are on, S_5 and S_6 are off, nodes A and B are grounded, a unity-gain feedback loop is established around A_0, and the input offset is stored on C_1 and C_2. During tracking, S_1 - S_4 are off, S_5 and S_6 are on, the feedback loop is open. The offset memorized on the capacitors is added to the input signal in such a way that the real offset is neutralized, leaving only the useful signal to be amplified. In the latching mode, the latch is strobed so as to regeneratively amplify the difference produced at the amplifier output, hence providing logic levels at V_{out}. The residual offset for IOS is

$$V_{OS,IOS} = \frac{V_{OSA}}{1 + A_0} + \frac{\Delta q}{C} + \frac{V_{OSL}}{A_0} \tag{4.9}$$

where V_{OSL} is the latch offset, V_{OSA} is the input offset of the amplifier, A_0 is the gain of the amplifier, Δq is the charge injection mismatch between S_3 and S_4 and C is the value of C_1 and C_2. This offset can be minimized by enlarging the gain of the amplifier, A_0, but this will reduce the settling speed of the amplifier. Moreover, $V_{OS,IOS}$ is ultimately limited by the charge injection of the switches, whose effect can only be reduced by increasing C.

The Output Offset Storage (OOS) technique shown in Fig. 4.8, on the other hand, measures the output-referred offset of the amplifier during the offset cancellation mode by grounding the nodes A, B, X and Y. The amplifier offset is amplified and stored on C_1 and C_2, while keeping a zero difference at the latch input (nodes X and Y). In the tracking mode, S_1 - S_4 are off and S_5 and S_6 are on. The circuit thus senses and

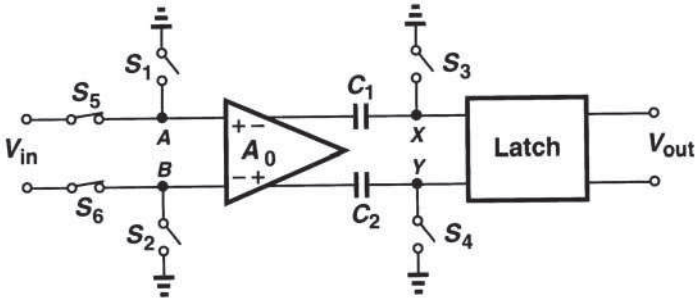


Figure 4.8: The comparator employing OOS.

amplifies the input signal, generating a differential voltage at nodes X and Y. Then, similarly as the IOS, the latch produces a logic level in the latching mode. The residual offset after the OOS is given by

$$V_{OS,OOS} = \frac{\Delta q}{A_0 C} + \frac{V_{OSL}}{A_0} \tag{4.10}$$

The amplifier offset is totally removed and the charge injection mismatch is attenuated by the gain of the amplifier. Therefore, for the same amplifier, the residual offset of OOS is smaller that of IOS. Similarly as IOS, the residual offset of OOS can be minimized by increasing A_0. However, in addition to reducing the speed, a high A_0 may lead to saturation of the amplifier during the offset cancellation mode, if the product of its input offset and its gain exceeds the maximum voltage swing allowed at its output. Thus, OOS usually adopts a single-stage amplifier with the gain less than 20 [118, 119].

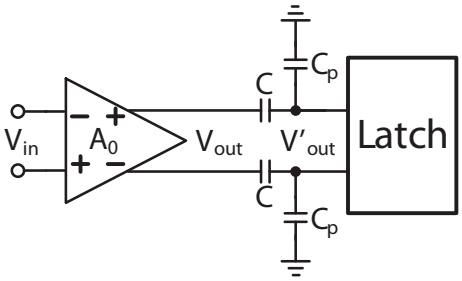


Figure 4.9: The capacitive divider formed by the offset storage capacitor C and the parasitic capacitor C_p.

In practice, the gain before the latch is attenuated by the capacitive divider introduced by the parasitic. Fig. 4.9 illustrates an amplifier with OOS in the tracking mode.

A voltage divider is formed by the the offset storage capacitor C and the parasitic capacitor C_p with the attenuation factor of

$$\frac{V'_{out}}{V_{out}} = \frac{C}{C + C_p}. \tag{4.11}$$

In order to minimize the capacitive attenuation effect, as well as to reduce the effect of charge injection mismatches, it is desirable to have a large C. However, for OOS, a large C will limit the settling speed of the amplifier in the offset cancellation mode. In the tracking mode, on the other hand, the settling is not limited by the offset storage capacitor, because the capacitance "seen" by the amplifier corresponds to series of C and the parasitic capacitance at the latch input, which should be much smaller than C. Thus, the settling issue in the offset cancellation mode is the main concern.

For a large latch offset, generally expected for a regenerative latch, one stage of amplification is usually not sufficient to achieve a high precision and at the same time to maintain a fast response. This is because the offset of the latch is attenuated by the total gain of the preceding amplifier, and a single high-gain amplifier suffers from long delay. In this case, the multi-stage cancellation scheme, where several cascaded amplifiers using IOS, OOS or a combination of both, can be employed. In practice, due to the large bandwidth required for a short delay, the gain of each amplifier cannot be very large and is usually limited to be less than 10. The number of amplifying stages is then determined by the overall gain needed to effectively suppress the latch offset and the selected gain of each amplifier. Generally, the offset for a regenerative latch, fabricated in a modern sub-micrometer CMOS technology, is expected to be on the order of 10 mV in RMS (Root Mean Square) value, assuming the transistor dimensions are carefully chosen [120, 121]. In order to achieve a satisfactory resolution well below the expected noise voltage value of about 1 mV from the sensing system, two amplifying stages, each of which has a gain of ~ 6, will adequately attenuate the latch offset.

Circuit topology of in-pixel discriminator

Based on the discussion above, all the three discriminator versions developed in AROM-0 are composed of two offset-compensated amplifying stages and a regenerative latch. Their circuit topologies are introduced in the following.

The discriminator V1 is illustrated in Fig. 4.10. Here, *calib* and *read* are non-overlapping signals, and V_{ref1}, V_{ref2} are two reference voltages. By closing alternatively

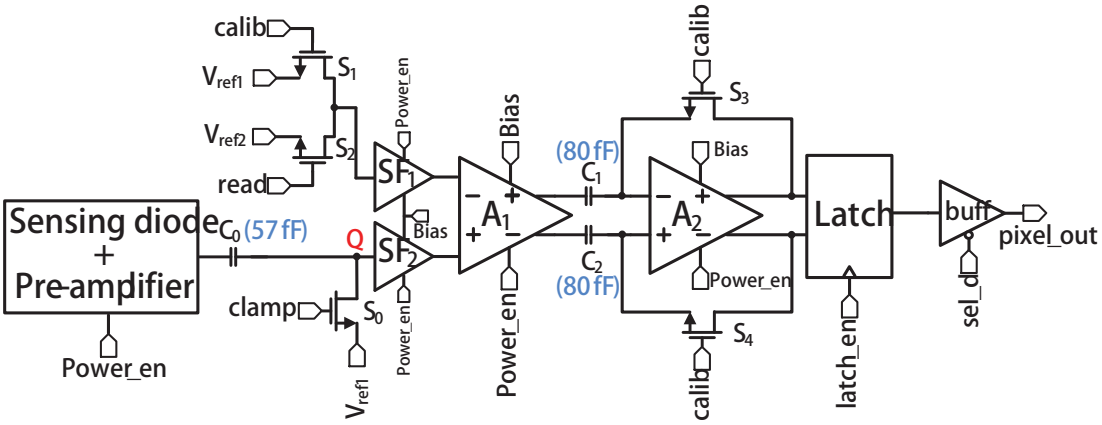


Figure 4.10: Simplified schematic of pixel V1.

the MOS switches S_1 and S_2, an arbitrary offset will be introduced to the circuit, constituting the threshold voltage. In order to ensure a proper DC input voltage for the discriminator, the sensing system is AC connected to the discriminator through the coupling capacitor C_0. The capacitor C_0 and the MOS switch S_0 can be seen as the CDS element to extract the signal and to remove the offset from the pre-amplifier, similarly as described in Section 2.4.3. The source follower SF_2 following C_0 is used to protect the sensitive high impedance node Q. The other source follower SF_1 is implemented for matching purpose. The first amplifier A_1 adopts the OOS to eliminate its offset, whereas the offset of the second amplifier A_2 is compensated by the IOS. The capacitors C_0 - C_2 should be as large as possible as allowed by the pixel area, in order to reduce the charge injection mismatch, KTC noise and the capacitive attenuation effect. The values of those capacitors are noted in Fig. 4.10. Neglecting the gain loss caused by the capacitive attenuation and the source followers, the input referred offset value for discriminator V1 is given by

$$V_{OS1} = \frac{V_{OSA2}}{G_1(1+G_2)} + \frac{V_{OSL}}{G_1 G_2} + \frac{\Delta q}{G_1 C} + \frac{q_0}{C_0}. \tag{4.12}$$

where V_{OSL} is the input referred offset of the latch, V_{OSA1} and V_{OSA2} are the input referred offsets of the amplifier A_1 and A_2, G_1 and G_2 are the gains of the amplifiers A_1 and A_2, Δq is the charge injection mismatch from the MOS switches S_3 and S_4, C is the capacitance value of the offset storage capacitors C_1 and C_2, and q_0 is the charge injection offset introduced by the switch S_0.

The discriminator V2, shown in Fig. 4.11, has a different topology, where two

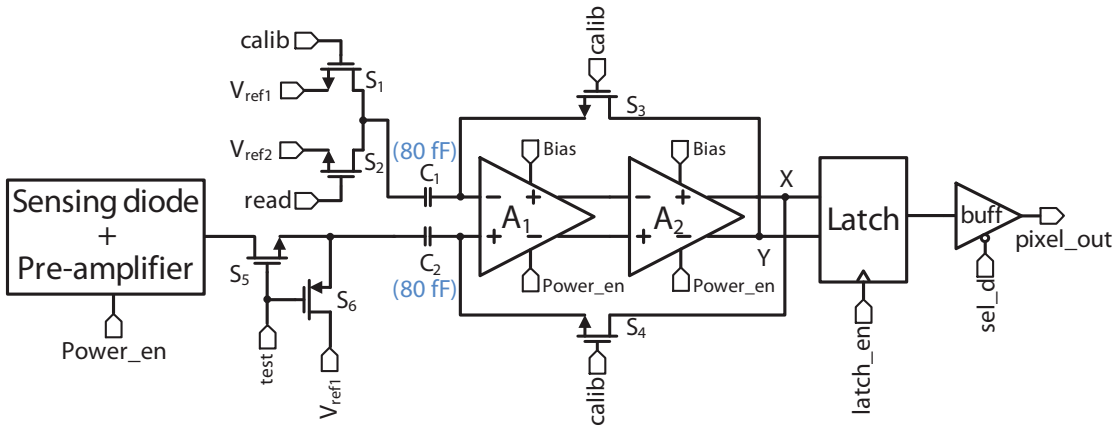


Figure 4.11: Simplified schematic of pixel V2.

directly cascaded amplifiers form a two-stage high-gain amplifier with its offset compensated by IOS. With the IOS scheme, the offset storage capacitor C_2 also provides the AC connection between the sensing system and the discriminator. As compared to V1, the discriminator V2 contains fewer components, and in particular one less MIM capacitor. The AROM-0 pixel uses the stacked MIM capacitor, due to its relatively high capacitance density. This stacked MIM capacitor utilizes three of the total six metal layers and has a capacitance density of about 3.4 fF/μm^2. As compared to a MOS capacitor, the capacitance value of the MIM capacitor is not dependent on the applied voltage. However, the MIM capacitor consumes more area for a given capacitance value and will obstruct the signal routing. Thus, with one less MIM capacitor, V2 alleviates the layout difficulty and routing congestion. Profiting from its simpler structure, the layout of pixel V2 can be modified without much difficulty to adapt the double-row readout scheme. Therefore, V2 is also implemented in a pixel array of 16×18 with double-row readout, so as to further explore the potential of fast readout for AROM pixels. However, the second-order system, formed by the two identical amplifiers A_1 and A_2, has a limited phase margin. In the closed loop configuration during the offset cancellation mode, an under-damped behavior will occur, and this behavior may degrade the noise performance. Moreover, the intrinsic input referred offset of V2 is slightly higher than that of V1. This is because the offset of A_1 is not totally eliminated and the charge injection mismatch on the capacitor C_1 and C_2 appears directly at the inputs and is not attenuated. The resulting input referred offset is given by

$$V_{OS2} = \frac{V_{OSA1}}{1 + G_1 G_2} + \frac{V_{OSA2}}{G_1(1 + G_1 G_2)} + \frac{V_{OSL}}{G_1 G_2} + \frac{\Delta q}{C}. \tag{4.13}$$

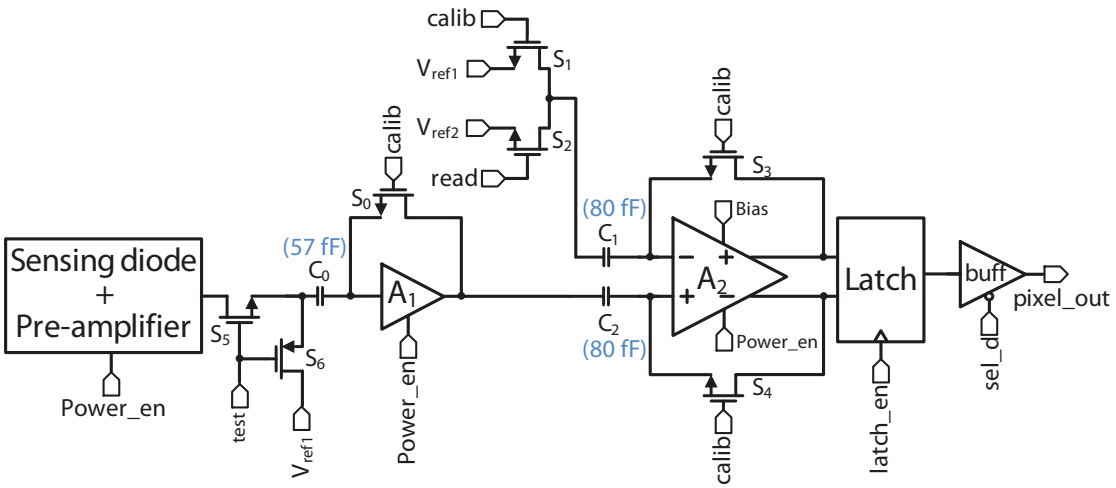


Figure 4.12: Simplified schematic of pixel V3.

The third version, V3, is illustrated in Fig. 4.12. It uses a single-ended amplifier A_1 as the first stage, which is AC coupled to the sensing system through the capacitor C_0. C_2 acts as one of the IOS capacitors for A_2, and also as the OOS capacitor for A_1. Therefore, the offset of A_1 is totally removed. The use of single-ended amplifier results in less area and power consumption for a given gain [86]. However, it has several drawbacks. Unlike differential designs, the single-ended amplifier suffers from poor power supply rejection ratio [119]. Furthermore, the power dissipation of the circuit is strongly process- and supply-dependent because its bias current is generally not given by a current source. When the feedback switch is on, the amplifier is self-biased. For a common source amplifier with the diode-connected load, the bias current is the current drawn from the supply by two diode-connected MOSFETs in series, which is much less rigorously defined than by a current source. In addition, it may require a large coupling capacitor at the input, so that the amplifier does not escape the high-gain region due to the charge injection effect of S_0. The total input referred offset is given by

$$V_{OS3} = \frac{V_{OSA2}}{G_1(1+G_2)} + \frac{V_{OSL}}{G_1 G_2} + \frac{\Delta q}{G_1 C} + \frac{q_0}{C_0}. \tag{4.14}$$

It is noted that the switches S_5 and S_6 in V2 (Fig. 4.11) and V3 (Fig. 4.12) are implemented to increase the testability. The *test* signal enables either the NMOS switch S_5 or the PMOS switch S_6, connecting either the sensing system or the reference voltage V_{ref1} to the discriminator input. Therefore, when the *test* signal is set to "0", the sensing system is isolated from the discriminator and the discriminator can be

characterized separately. For V1 in Fig. 4.10, a different approach is used. The input of the discriminator can be fixed to the reference voltage V_{ref1} by activating the switch S_0 permanently, so that the signal from the sensing system is overwhelmed.

Working principle

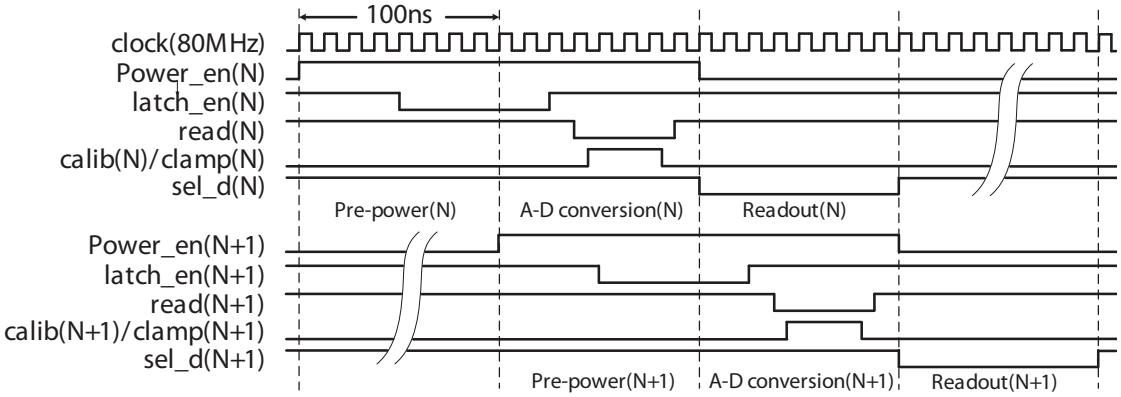


Figure 4.13: Timing diagram.

The three pixel versions share the same timing sequence for operation. Fig. 4.13 shows the timing diagram for two consecutive rows, i.e., row N and row N+1. Each row is activated by a corresponding *power_en* signal for readout. Each *power_en* signal lasts for 200 ns and the first half is intended for settling the circuit after being switched on, especially the pre-amplifier. All the rows in the pixel array are activated sequentially in a pipeline manner, delayed by 100 ns from one to the next. Therefore, the actual readout speed is 100 ns/row (or 100 ns/2rows for double-row readout).

When the pixel works in the normal mode, the *test* signal is set to "1" and the *clamp* signal in V1 shares the same timing as the *calib* signal. In this way, the discriminator will sense the output of the pre-amplifier. The offsets of the pre-amplifier, as well as the amplifiers of the discriminator are cancelled by the offset storage techniques described previously, with a two-phase operation, i.e., the *calib* phase and the *read* phase. In the *calib* phase, the offsets are memorized on the offset storage capacitors. At the same time, the reference voltage V_{ref1} is applied to the circuit through S_1 (also from S_0 in V1). In the *read* phase, the offsets are corrected. Moreover, V_{ref1} is disconnected and the second reference voltage V_{ref2} is applied to the discriminator through S_2. The

threshold voltage V_{th} is then defined by

$$V_{th} =\mid V_{ref2} - V_{ref1} \mid \tag{4.15}$$

which is adjusted by fixing the V_{ref1} and varying V_{ref2}. Ideally, if there is no signal from the sensing system and the threshold is set to zero, the latch circuit should have a very small input voltage, corresponding to the remaining circuit offset. When an arbitrary threshold is set, the voltage at the latch input should be the threshold value multiplied by the gain from the threshold injection node to the latch input.

If a particle arrives during a read-out frame, the sensing diodes close to the particle traversing path will collect the charge signal and convert it proportionally to a voltage signal. Once the pixel carrying the signal is activated, the signal voltage on the sensing node is pre-amplified and sensed by the discriminator. If the signal value is large enough to overcome the threshold, the polarity of the voltage at the latch input will be reversed. In the latching phase, the latch circuit is first reset by the falling edge of the *latch_en* signal, clearing its latched state from the previous read-out cycle. Then, on the rising edge of the *latch_en* signal, the latch circuit regeneratively develops an output logic level based on the polarity of its input voltage. Since a signal value exceeding the threshold can reverse the polarity of the latch input voltage, a fired pixel will have a different output logic value from the unfired ones. After the latching phase, the circuit goes back to the *calib* phase for the offset storage. The binary signal from the latch is sent to the column bus by a tri-state buffer, which is negatively enabled by the *sel_d* signal.

From the timing sequence given in Fig. 4.13, one can also observe that the read-out strategy of AROM-0 is based on a pipeline manner. The pixel readout can be divided into three working phases: the first is for circuit settling after being powered on (pre-power); the second is for signal discrimination (A-D conversion); and the last is to read out the binary result (readout). The duration for the three phases are equally allocated, and the readout of row N+1 is delayed by one working phase with respect to the readout of row N.

The amplifier design

The discriminators introduced above require relatively low gain and fast response for the amplifiers preceding the latch circuit. Therefore, the amplifier with the diode-

connected load is chosen. Fig. 4.14(a) gives the schematic of the differential amplifier that has been implemented for all the three discriminator versions, and Fig. 4.14(b) shows the schematic of the single-ended amplifier used in discriminator V3.

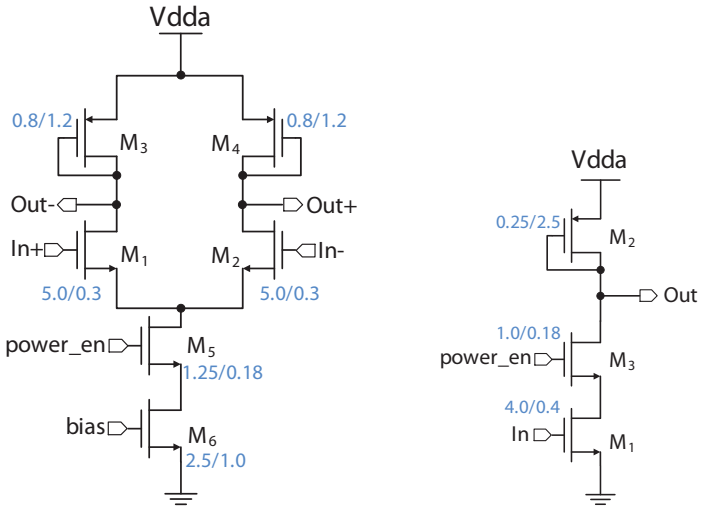


Figure 4.14: The schematics of (a) the differential amplifier and (b) the single-ended amplifier used in AROM-0.

The gain for a amplifier with the diode-connected load is defined by the transconductance ratio of the input transistor and the load transistor. Thus, the gain for the amplifier in Fig. 4.14(a) is given by

$$A_{diff} = \frac{g_{m1,2}}{g_{m3,4}} = \frac{\mu_n(W_{1,2}/L_{1,2})}{\mu_p(W_{3,4}/L_{3,4})}, \tag{4.16}$$

and the gain for the amplifier in Fig. 4.14(b) is given by

$$A_{single} = \frac{g_{m1}}{g_{m2}} = \frac{\mu_n(W_1/L_1)}{\mu_p(W_2/L_2)} \tag{4.17}$$

where g_m is the transconductance of the transistor, μ_n and μ_p are the mobilities of electrons and holes, W and L are the width and length of the transistor gate. Both of the amplifiers in Fig. 4.14 use NMOS as input transistors and PMOS as load transistors. This is because the mobility of holes is smaller than that of electrons, and using such a combination results in the highest gain when the same area is assumed. Typically,

a gain of 5 - 10 can be easily achieved with such amplifiers. The *power_en* signal is used to switch off the amplifier when the pixel is not scanned for readout.

The bandwidth of the amplifier is mainly determined by the required settling time after switching the working mode. When the system is switched from the *read* phase to the *calib* phase, the settling time of the circuit must be less than the duration of the *calib* signal, in order to correctly memorize the offset values.

First, V1 (Fig. 4.10) and V3 (Fig. 4.12) are considered. It can be seen from the following that the amplifier A_1 in V1 has the most stringent requirement of bandwidth among all the four amplifiers in V1 and V3. During the *calib* phase, only the amplifier A_1 in V1 works in the open-loop mode, whereas the other amplifiers, employing the IOS, are configured as unity-gain feedback loops. Due to a constant gain-bandwidth product of a first-order system, the unity-gain feedback loop has a larger bandwidth than that of the open-loop configuration [86], and thus can respond faster. The second fact, making the amplifier A_1 in V1 the critical amplifier, is that it has the largest capacitive loading during the *calib* phase. Similarly as discussed in Section 4.2.3, in the *calib* phase, the load capacitors of A_1 in V1 are approximately equal to the offset storage capacitors, C_1 and C_2. Whereas, in the *read* phase, the loop of A_2 is open, and the load capacitors for A_1 become the offset storage capacitors in series with the input parasitic capacitors of its following stage A_2, which should have a smaller value. The following describes how the required bandwidth for the amplifier A_1 in V1 is obtained.

The transfer function for a single-pole amplifier is given by

$$A(s) = \frac{A_0}{1 + s\tau} \tag{4.18}$$

where A_0 is the low frequency gain of the amplifier and τ is the time constant. And the unit step response for such a circuit is

$$V_{out}(t) = A_0(1 - e^{-t/\tau}) \tag{4.19}$$

The output signal never actually equals its final value A_0 for finite values of t. If an error of 2 % is assumed to be acceptable, the settling time of the system can be resolved by replacing the $V_{out}(t)$ in (4.19) with $0.98A_0$. The resulting settling time of the system is $\sim 4\tau$, and thus the bandwidth of the system can be determined by

$$4\tau = \frac{4}{2\pi f_{-3dB}} \leq T_s \Rightarrow f_{-3dB} \geq \frac{2}{\pi T_s} \tag{4.20}$$

where T_s is the required settling time and f_{-3dB} is the -3 dB bandwidth of the amplifier. If 35 ns is allocated for the *calib* phase, a bandwidth of $\sim$ 20 MHz is needed for the open-loop amplifier. In practice, the additional parasitic introduced in the layout and the process variation must be taken into account, and a safety factor should be applied.

For design simplicity, all the differential amplifiers in the AROM-0 pixels use the same design. The simulated results for the differential amplifier, as well as the single-ended amplifier, are summarized in Table 4.2. All the parameters given are simulated in open loop.

Table 4.2: Simulation results for the amplifiers used in AROM-0.

Amplifier type	Biasing current	Gain	Bandwidth
Differential[a]	15 μA	6.9	35.2 MHz
Single-ended[b]	8 μA	6.8	163 MHz

[a]Simulated with 0.7 V DC input and 80 fF load capacitor.
[b]Simulated with 10 fF load capacitor.

Then, the discriminator V2 (Fig. 4.11) is considered. During the *calib* phase, the loop is closed by connecting the output of the second amplifier to the input of the first amplifier, and thus a second-order closed loop is formed. To calculate accurately the settling time of such a system is very complicated. So, the simulation is used to verify the settling time. Using the same differential amplifier described above, the simulated transient response at the output of the amplifier A_2 (node X and node Y in Fig. 4.11) during the *calib* phase is shown in Fig. 4.15. An under-damped behavior of oscillation can be seen, and the amplitude of oscillation diminishes to a negligible value (less than 100 μV) after $\sim$ 10 ns.

The latch design

The dynamic latch offers fast response and no-static power, at the expense of large kickback noise. The so called kickback noise is due to the large voltage variations in the internal nodes of the comparator. These internal nodes are coupled, through the parasitic capacitance of the transistors, to the comparator input nodes, and thus disturbing the input voltage [122, 123]. However, with two amplifiers before the latch, the kickback noise is not a main issue.

A typical dynamic latch, as shown in Fig. 4.16, consists a current tail (M_{11}), a differential pair (M_1 and M_2), two cross coupled inverters (M_3, M_5, and M_4, M_6) and

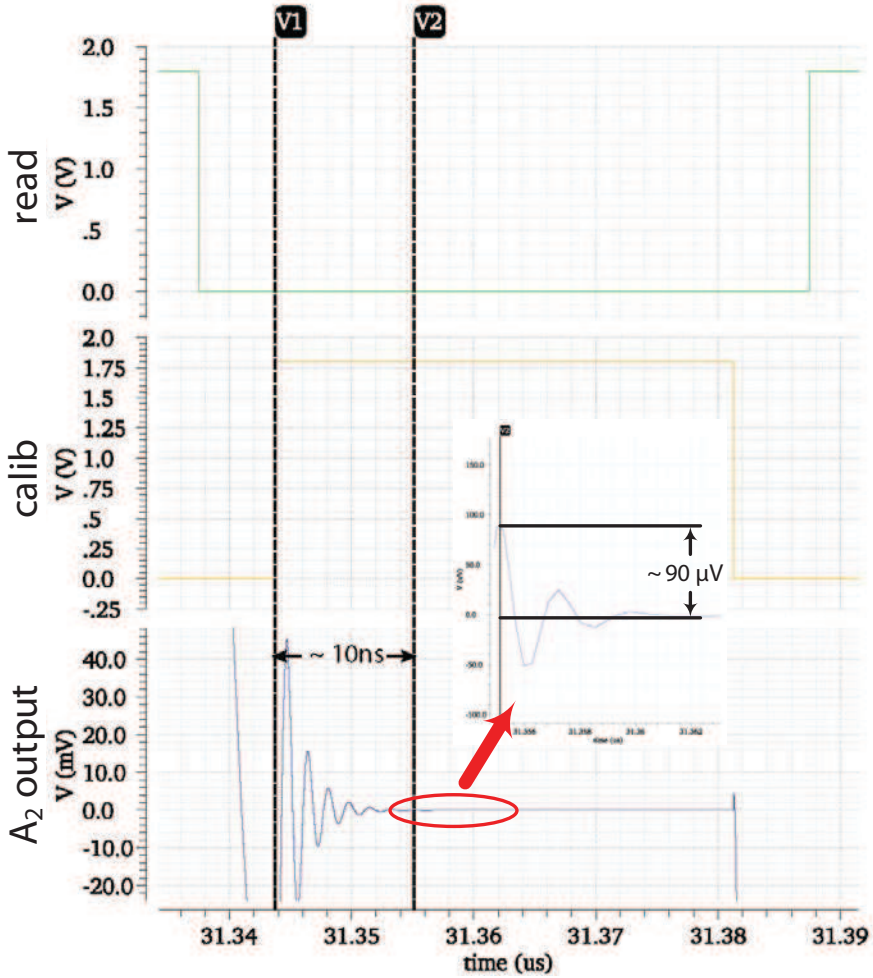


Figure 4.15: The simulated transient response at the output of the second amplifier in V2.

the reset switches (M_7 - M_{10}). Its operation principle can be described as follows. When *latch_en* is low (reset phase), the transistors M_7 - M_{10} reset the nodes P and Q and the drains of the differential pair M_1 and M_2 to the supply voltage. Moreover, M_{11} is OFF and no supply current exists. When *latch_en* goes high, the reset transistors M_7 - M_{10} are switched OFF, and M_{11} is ON. The latch enters the decision-making phase. In this phase, the current flows in the differential pair M_1 and M_2. Depending on the input voltage, the drain current of the input pair discharges the parasitic capacitors at nodes A and B with different speeds, turning on transistor M_3 and M_4 one after the other. Then, the regeneration process is initiated by the cross coupled inverters, with the final state quickly developed at the outputs. After the regeneration is completed,

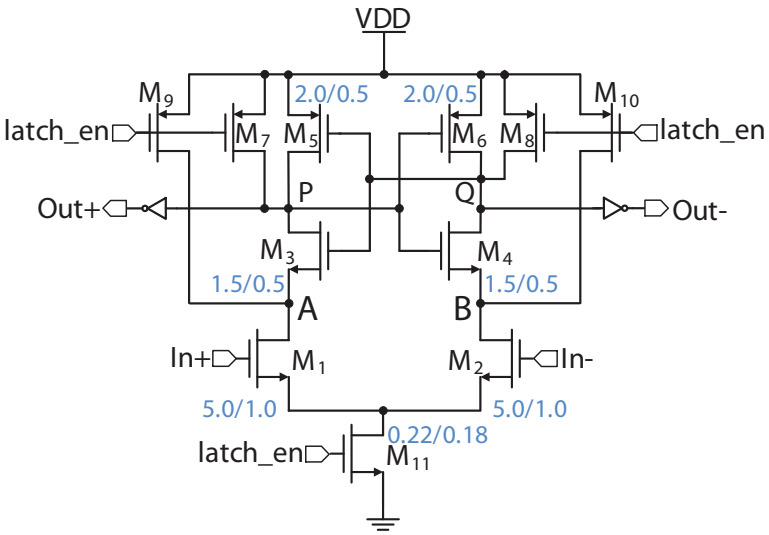


Figure 4.16: Schematic of the dynamic latch.

one of the output nodes is at "0", and the other output is at "1". Both drains of the differential pair have a 0-V potential. There is, in this situation, no supply current, which maximizes power efficiency [124].

The total input referred offset voltage of the dynamic latch is dominated by the input differential pair M_1 and M_2. This is because the offset resulting from the cross coupled inverters is attenuated by the gain of the input transistors. The offset voltage caused by the differential input pair can be derived as follows. At the beginning of the decision-making phase, the transistor M_3 and M_4 remain OFF, and the input differential pair starts to operate in the saturation region, and their drain current is defined by

$$I_{d1,2} = \frac{1}{2}\beta_{1,2}(V_{In+,-} - V_{th1,2})^2 \tag{4.21}$$

where V_{th} is the transistor threshold voltage, β is the current factor and $V_{In+,-}$ is the input voltage which in this case equals to the gate-to-source voltage of the input pair. Before the regeneration process begins, the voltage at nodes A and B is

$$V_{A,B}(t) = VDD - \frac{I_{d1,2}}{C_{A,B}}t \tag{4.22}$$

where $C_{A,B}$ is the parasitic capacitance at nodes A and B.

The offset voltage is defined by input voltage that makes $V_A(t)$ equals to $V_B(t)$.

Then, the following equation is obtained from (4.22)

$$\frac{I_{d1}}{I_{d2}} = \frac{C_A}{C_B} \tag{4.23}$$

and from (4.21), one can get

$$V_{offset} = V_{In+} - V_{In-} = (\sqrt{\frac{2I_{d1}}{\beta_1}} + V_{th1}) - (\sqrt{\frac{2I_{d2}}{\beta_2}} + V_{th2}) \tag{4.24}$$

If it is assumed that

$$I_{d1} = I_d, \quad I_{d2} = \Delta I_d + I_d \tag{4.25}$$

$$V_{th1} = V_{th}, \quad V_{th2} = \Delta V_{th} + V_{th} \tag{4.26}$$

and

$$C_A = C, \quad C_B = \Delta C + C \tag{4.27}$$

by taking the first-order approximation and using (4.23), (4.24) can be written as [125]

$$\begin{aligned} V_{offset} = \sqrt{\frac{2I_d}{\beta}}(1 - \sqrt{\frac{1+\frac{\Delta I_d}{I_d}}{1+\frac{\Delta\beta}{\beta}}}) - \Delta V_{th} &= \sqrt{\frac{I_d}{2\beta}}(\frac{\Delta\beta}{\beta} - \frac{\Delta I_d}{I_d}) - \Delta V_{th} \\ &= \frac{V_{In} - V_{th}}{2}(\frac{\Delta\beta}{\beta} - \frac{\Delta C}{C}) - \Delta V_{th} \end{aligned} \tag{4.28}$$

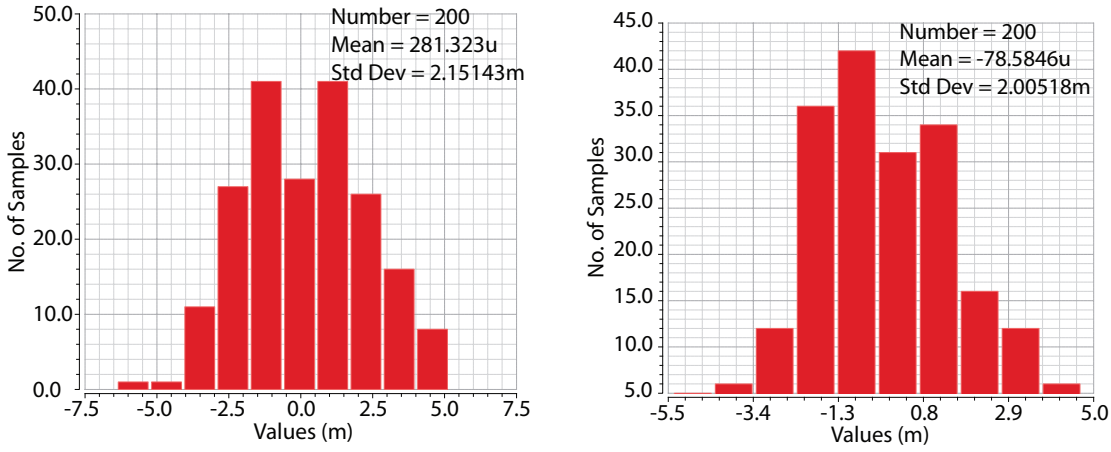
where V_{In} can be seen as the common input voltage of the latch. The random mismatch in threshold voltage V_{th} and current factor β for each transistor pair can be modeled as [125, 126]

$$\sigma_{\Delta V_{th}} = \frac{A_{\Delta V_{th}}}{\sqrt{WL}}, \quad \sigma_{\Delta\beta} = \frac{A_{\Delta\beta}}{\sqrt{WL}} \tag{4.29}$$

where $A_{V_{th}}$ and A_β are process dependent parameters. It can be seen from (4.28) and (4.29) that the variation of the input referred offset depends a lot on the dimension of the input pair and the input common mode voltage. The dimensions of the transistors are noted in Fig 4.16, and the input pair has the largest dimension in order to minimize the offset variation.

It is also noted that the mismatch of the parasitic capacitance on the output nodes P and Q will also result in residual offset. In the AROM pixels, only one output node

is connected to a digital buffer for readout, with the other left floating. Hence, in order to reduce the residual offset, two inverters are placed at nodes P and Q to balance their capacitive loads.



(a) (b)

Figure 4.17: Simulated offset distribution of the dynamic latch. (a) the mismatches of all the transistors are considered and (b) only the mismatch from the input pair is considered.

The latch offset was estimated by using Monte Carlo simulation. Fig. 4.17(a) gives the simulated histogram of the latch input referred offset, when the common input voltage is 0.75 V. The simulated random offset is about 2.2 mV in RMS value, with the mean value of 280 μV. Divided by the gain of the two amplifiers before the latch, the discriminator input referred offset contributed by the latch should be marginal. The simulation was also performed when only the mismatch contribution from the input pair was included, and the result is given in Fig. 4.17(b). It verifies that the input pair is most critical component for offset, leading to about 2 mV of random offset.

4.2.4 Layout

Even though the pixel-level discrimination provides fast readout and low power consumption, it brings some drawbacks as compared to the conventional analogue pixel. The additional pixel-level functionality requires more electronic components to be laid out inside the area-limited pixel. In addition, more digital control signals need to be distributed over the whole pixel array. These will increase the layout congestion and

cross coupling. Therefore, the layout design is one of the main challenges of AROM-0.

As discussed in Section 3.3, the final ASTRAL sensor will be composed of 3 identical FSBB-A sensors abutted side by side and multiplexed at their output nodes. In order to minimize the dead zone between sensor blocks, the sequencer for each block is placed at the bottom of the pixel array. Therefore, the control signals must be first transmitted vertically through the pixel array and then shared horizontally by a corresponding row. Moreover, in the elongated pixel geometry, the sensing diodes are placed in a staggered manner for the sake of radiation tolerance and single point resolution. Both the cross distributed control lines and the staggered diode arrangement will add difficulties in the layout design.

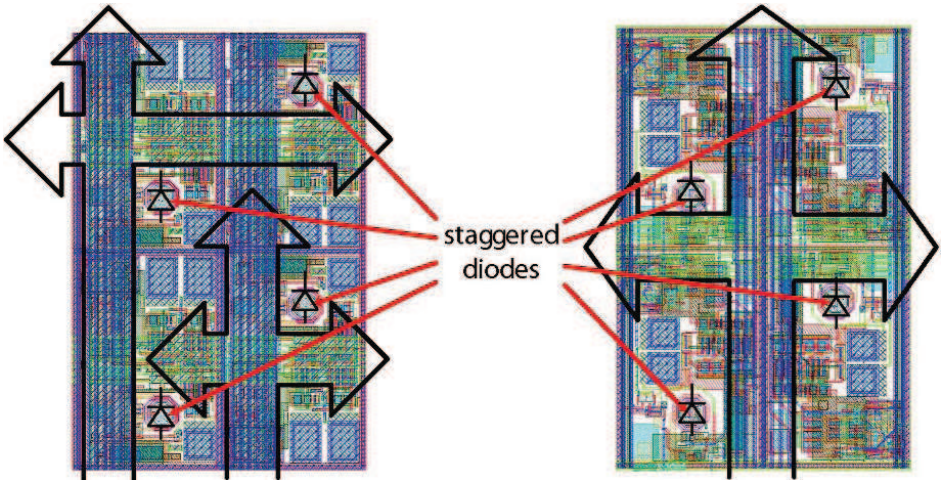


Figure 4.18: The layouts of the 4 pixels for V1 (left) and the double-row readout V2 (right). The black hollow arrows indicate the digital control signal distribution.

The layouts of four pixels as a group are shown in Fig. 4.18, for both V1 pixels and the double-row readout V2 pixels in AROM-0. The black hollow arrows indicate the control lines passing through these pixels. The single-row readout V2 pixels have a similar floor plan of layout as the pixels of V1. The digital control signals (*calib*, *read*, etc.) are distributed by using the two highest metal layers, i.e. metal six for vertical transmission and metal five for row distribution. Metal four is used to shield the analog circuit underneath the digital control lines, in order to minimize the mixed signal cross coupling. The reference and biasing signals are mainly distributed by using the metal three. The analog power supply and the ground are distributed by using metal two and metal one respectively, surrounding each pixel.

4.3 Laboratory measurement

The chip AROM-0 was extensively tested in laboratory to verify the functionality, and to evaluate the noise performance. The clock, as well as all the control signals required for chip operation, are generated off-chip by the built-in pattern generator of a logic analyzer (Agilent 16822A). On the data acquisition side, the output signals from the chip are digitized by 12-bit ADCs and sent to PC for further processing. In this section, the measurement results of AROM-0 are presented. Some issues found during the test are also discussed.

4.3.1 Sensing calibration

A crucial figure of merit for CPS is the ENC. In order to convert the noise into the charge value, the CVF of sensing system must be calibrated. As mentioned in Section 4.1, dedicated analogue pixels, with the integrated source follower to drive the analogue signal from the sensing system, were implemented in the pixel array of AROM-0. So, the sensing calibration can be performed by utilizing these analogue pixels. As illustrated in Fig. 4.19, the in-pixel source followers, buffering the analogue signal, were placed after the coupling capacitor C_0 for pixel V1, whereas for the other two pixel versions, the source followers were placed directly after the pre-amplifiers. The analogue signal in pixel V1 is obtained similarly as the conventional analogue pixel with in-pixel CDS, using the subtraction of two samples taken before and after the *clamp* phase respectively from the same read-out frame. For V2 and V3, the analogue signal is extracted from the subtraction of the signal samples in two neighbouring read-out frames. The *sel_A* signal is the row selection signal for analogue readout.

An ^{55}Fe radioactive source, emitting mostly the 5.9 keV X-rays, was used to perform the calibration. As described in Section 2.1.2, the interactions between soft X-rays and silicon are point-like and the electron-hole pairs are generated in a limited distance ($\sim$ 1 μm) from the interaction point. In most cases, the charge is naturally spread among several pixels, since the charge collection relies mainly on thermal diffusion in a typical CPS. However, the charge, released inside the charge collecting diode and in its vicinity, is collected rapidly and with a full efficiency. Therefore, the distribution of all extracted signals should exhibit a small peak corresponding to the collection of 1640 e^- in a single pixel.

Fig. 4.20 shows the signal distributions recorded by illuminating the chip with an

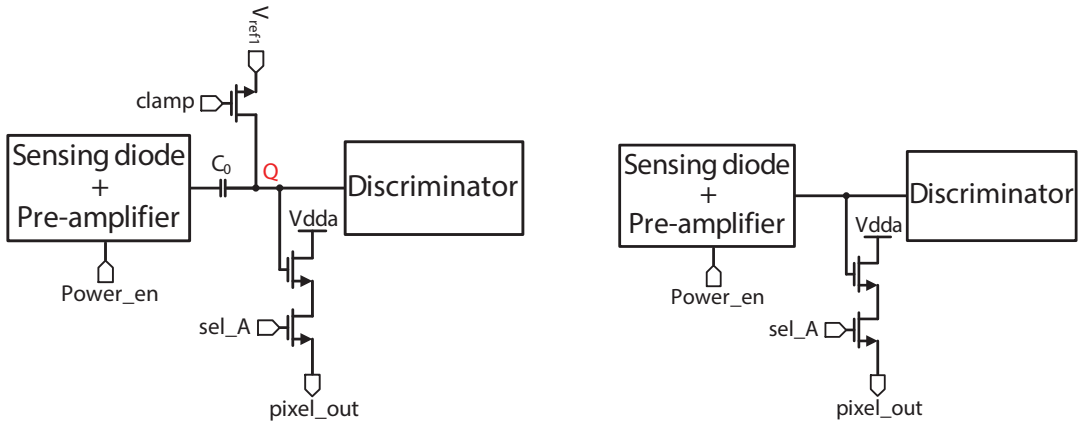


Figure 4.19: Illustration of the analogue pixels for (a) pixel V1, and (b) pixel V2 (or V3).

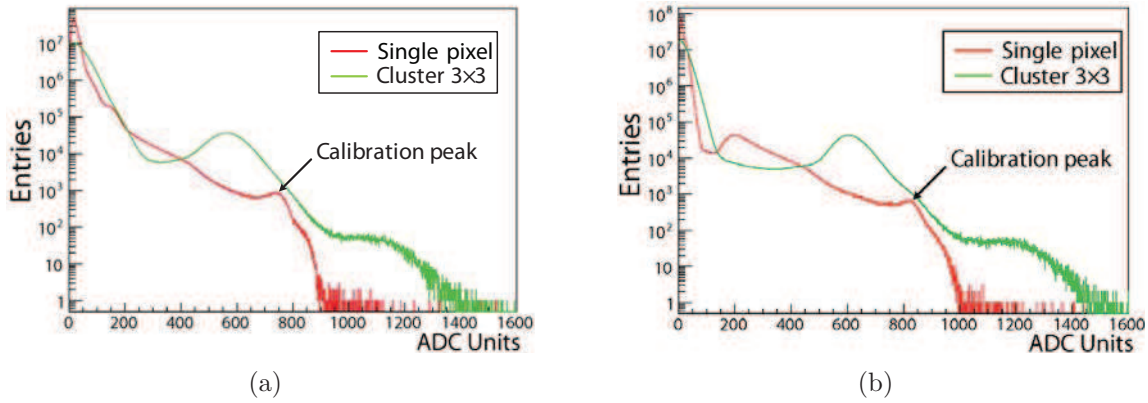


Figure 4.20: Spectra of signals from an ^{55}Fe source, registered with (a) the four analogue columns containing the pixel V1, and (b) the four analogue columns containing the pixel V2. Both the signal distributions from seed pixels (red) and the spectra of summed signals from 3 × 3 pixel clusters (green) are shown.

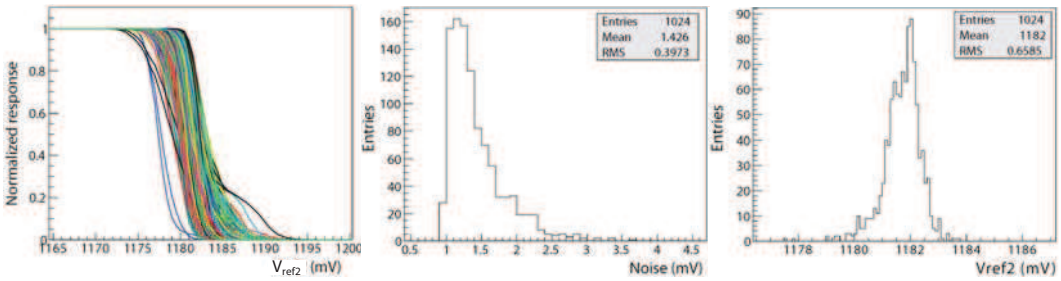
^{55}Fe X-ray source at the coolant temperature of 15 °C. Because pixel V3 has the same implementation for analogue readout as V2, here only the calibration results from V1 and V2 are presented. The red line gives the spectrum of signals collected by the seed pixels. The calibration peak, corresponding to the collection of $\sim$ 1640 e$^-$, is marked in the figure. When referred to the input of the source follower, 1 ADC unit corresponds to $\sim$ 116 μV, and thus the CVFs are calculated to be 52 μV/e$^-$ for pixel V1 and

57 μV/e$^-$ for pixel V2. The slightly lower CVF for V1 is due to the voltage divider formed by the coupling capacitor C_0 and the total parasitic capacitors at node Q in Fig. 4.19. Fig. 4.20 also gives the distribution of the summed signals for the 3 × 3 pixel cluster around the seed pixel (shown in green line). The peak that appears at around 600 ADC units indicates the most probable value for the charge signal collected by the 3 × 3 cluster. The ratio of this peak to the calibration peak gives the charge collection efficiency (CCE) for the 3×3 cluster, whose value is about 76 %. The tails of the spectra, exceeding 1000 ADC units, are caused by the rare events of two or more photon impacts on the same pixel or cluster during one read-out period. It is noted that the results shown in this section is based on a chip fabricated in the low-resistivity ($\sim$ 10 Ω·cm) epitaxial layer. A better charge collection efficiency would be achieved if the high resistivity epitaxial layer were used. And the benefit of using the high resistivity epitaxial layer for the AROM sensor can be seen in Chapter 5.

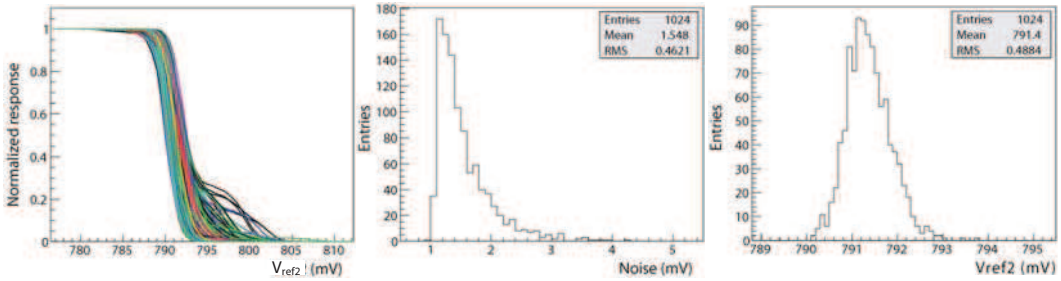
4.3.2 Characterization of the full in-pixel circuitry

The noise performance of the full in-pixel circuitry, including both the sensing system and the discriminator, was characterized by using the "S" curve method. The "S" curve for each pixel can be measured by calculating the probability of "1" events at the pixel output over a large quantity of readout cycles ("normalized response"), as a function of threshold voltage. The distribution of the "S" curves can be used for noise extraction.

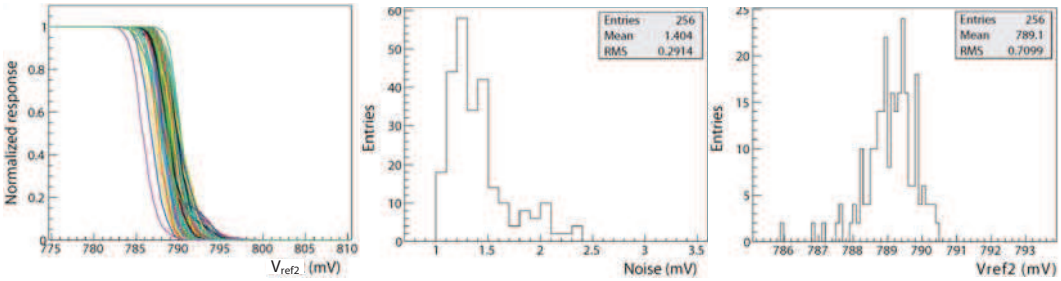
The measurement results for the three pixel versions are shown in Fig. 4.21. The figure gives the measured "S" curves (left), the extracted TN distribution (middle) and the threshold distribution (right). The threshold voltage is adjusted by varying V_{ref2} with respect to V_{ref1}. The TN of each pixel can be extracted by taking the derivative of a corresponding "S" curve, and then calculating the standard deviation of the distribution. The mean value of the aforementioned derivative gives the mid-point threshold of a pixel. Then, the FPN here is defined as the dispersion of the mid-point threshold. It can be seen from the TN distributions that a long tail towards the high value exists, representing the RTS noise. This RTS noise can be mitigated by optimizing the transistor dimension of the pre-amplifier (see Section 2.4 and Section 3.2.3). Table 4.3 summarizes the extracted noise values for the three pixel versions. Note that the TN shown in the table is the average TN value of all the pixels. The total noise is defined



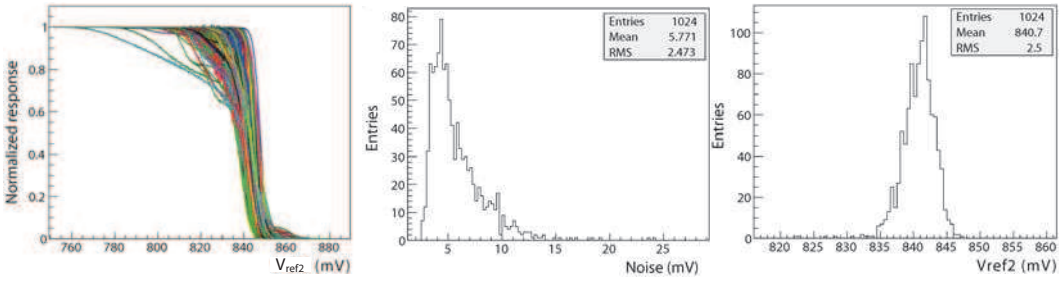
(a)



(b)



(c)



(d)

Figure 4.21: "S" curves of the full in-pixel circuitry at the nominal speed (left), the extracted TN distributions (middle) and threshold distributions (right) for (a) V1, (b) V2, (c) double-row readout V2 and (d) V3.

as

$$Total \quad noise = \sqrt{TN^2 + FPN^2} \tag{4.30}$$

and it is dominated by the TN. For V1 and V2, the equivalent noise charge (ENC) can be calculated by dividing the noise voltage by the CVF, which come out to be ~ 30 e^- in both cases.

For V3, the measured noise is referred to the output of the amplifier A_1 (see Fig. 4.12). In order to refer the noise to the input of the discriminator, the gain of the amplifier A_1 was measured and the result came to be 3.4. This value is much lower than the simulation value. In order to estimate the ENC of V3, a same CVF as the sensing system of V2 was assumed for V3, and the result is given in Table 4.3.

The measurements were also performed at lower speeds. It is found that the TN value increases slightly when the row processing time is longer. This is because the low frequency noise from the sensing diode and pre-amplifier becomes more significant when the integration time is longer. Another observation is that the FPN values of V1 and V3 decrease significantly to ~ 0.35 mV and ~ 1.8 mV, respectively, when the readout speed is slower than 400 ns/row. This is because the influence of the cross coupling becomes less significant when reading out the pixels with a lower speed. Thus, the FPN performance can be potentially improved by layout optimization to reduce the cross coupling effects. However, the pixel V2 does not show similar decrease in the FPN value as the other two versions, when slowing down the read-out speed. In addition, the double-row readout array has a larger FPN value than the single row readout array, as expected from its more complex layout of pixel array. The extracted noise values, measured when the row processing time is 400 ns, are also given in table 4.3.

Table 4.3: Noise performance of the full in-pixel circuitry in AROM-0.

Pixel version	Speed	TN (mV)	FPN (mV)	Total noise (mV)	ENC (e^-)
V1	100 ns/row	1.43	0.66	1.57	30.2
	400 ns/row	1.66	0.34	1.69	32.5
V2	100 ns/row	1.55	0.49	1.62	28.4
	400 ns/row	1.70	0.58	1.79	31.4
V2 (2-row)	100 ns/2-rows	1.40	0.71	1.57	27.5
	400 ns/2-rows	1.67	0.67	1.80	31.6
V3	100 ns/row	5.77	2.50	6.29	32.5
	400 ns/row	6.70	1.83	6.95	35.9

For a first generation of the AROM prototype, the pixel noise performances are encouraging, but improvements are still needed. It is noted that further development, including the optimization of noise and power consumption, is focused on V1 and V2. The pixel V3 is not considered as a primary option for the future AROM chips due to several reasons. The first is that the gain of the single-ended amplifier (A_1) in V3 is poorly predictable by simulation. Moreover, in order to obtain the ENC value, the single-ended amplifier needs to be calibrated, which complicates the test. The third is that the measured noise performance of V3 is worse than the other two. And finally, the advantages of the single-ended amplifier, e.g. low power and small area, tend to diminish if the differential amplifier is carefully optimized in the future.

4.3.3 Characterization of the in-pixel discriminator

Based on the measurements of other prototypes (e.g., MIMOSA-32TER and MIMOSA-32FEE1), containing the same sensing system as that in AROM-0, the ENC value of the sensing system is between 20 e^- and 25 e^-. Combined with the results in table 4.3, the discriminator alone should contribute by a significant amount to the noise, about 20 e^-. Therefore, the discriminators were isolated from the sensing system and measured separately, in order to have a complete understanding of the pixel noise performance.

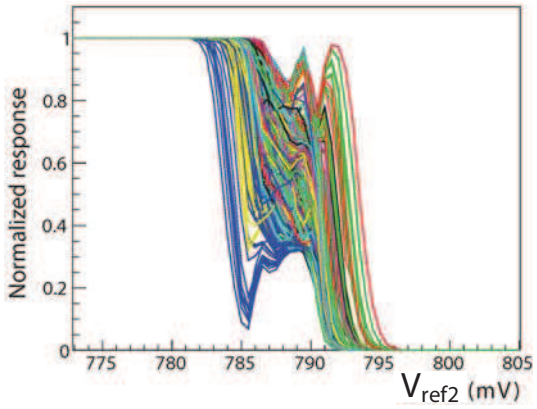


Figure 4.22: The measured "S" curves for the in-pixel discriminator V2 at nominal speed. Due to the coupling between column data line and V_{ref1}, the "S" curves are strongly disturbed.

As described in Section 4.2.3, the in-pixel discriminators can be isolated from the sensing system by setting the *clamp* signal permanently to "1" for V1, and setting the *test* signal to "0" for V2. Then, the "S" curves of the in-pixel discriminators can

be measured by raising progressively V_{ref2} and recording the discriminator response. Fig. 4.22 shows the "S" curves of the discriminators in V2 at the nominal read-out speed (100 ns/row). These curves are strongly disturbed in the transition region and cannot be exploited. This happens also for the other pixel arrays at the nominal read-out speed. Further study showed that the disturbance was caused by the capacitive coupling between some digital signals to the reference voltage V_{ref1}.

As described in Section 4.2.4, in AROM-0, the digital signals are mainly distributed across the pixel array by using the fifth and sixth metal layers. However, due to very limited place reserved for signal distribution, the column output lines, which were expected to have the least activities among the digital lines, were routed in the third metal layer for the single-row readout array. This layer is also used for the analog signal distribution. Fig. 4.23 takes the layout of pixel V1 as an example, where the reference voltage V_{ref1} is routed next to the column output line in the same metal layer. When there are activities on the column output line, the voltage V_{ref1} could be disturbed through the parasitic capacitance (C_p) between those two metal lines.

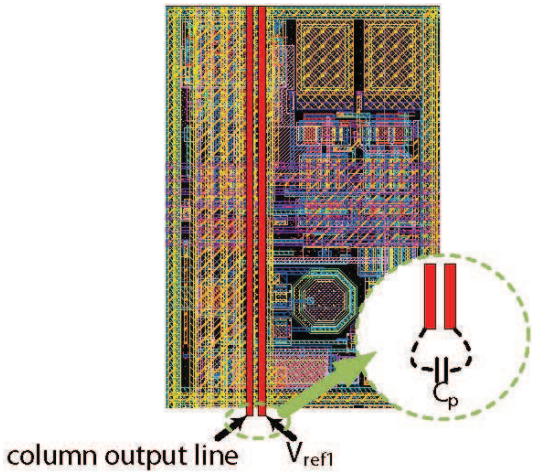


Figure 4.23: The coupling between the digital output bus and the reference voltage V_{ref1}.

Simulation with the extracted parasitic parameters was used to confirm this coupling effect. Fig. 4.24 gives simulated wave forms of the V_{ref1}, when a positive pulse (the shaded area) appears on the column when a pixel is fired. Because the readout of the pixel array uses the pipeline manner, the binary information of the fired pixel is presented on the column line during the A-D conversion phase of the next row. One should notice that when the in-pixel discriminator is characterized separately, V_{ref1} is used as one permanent discriminator input voltage, replacing the sensing system. If

V_{ref1} is not settled before the rising edge of the *latch* signal, as shown in Fig. 4.24, the output of the pixel will be consequently determined based on the influenced input value of V_{ref1}. This effect is most significant when the threshold is scanned into the region related to the intrinsic noise range of the discriminator, leading to large amount of activities on the column data line. Therefore, the transition region of the "S" curves is strongly deformed.

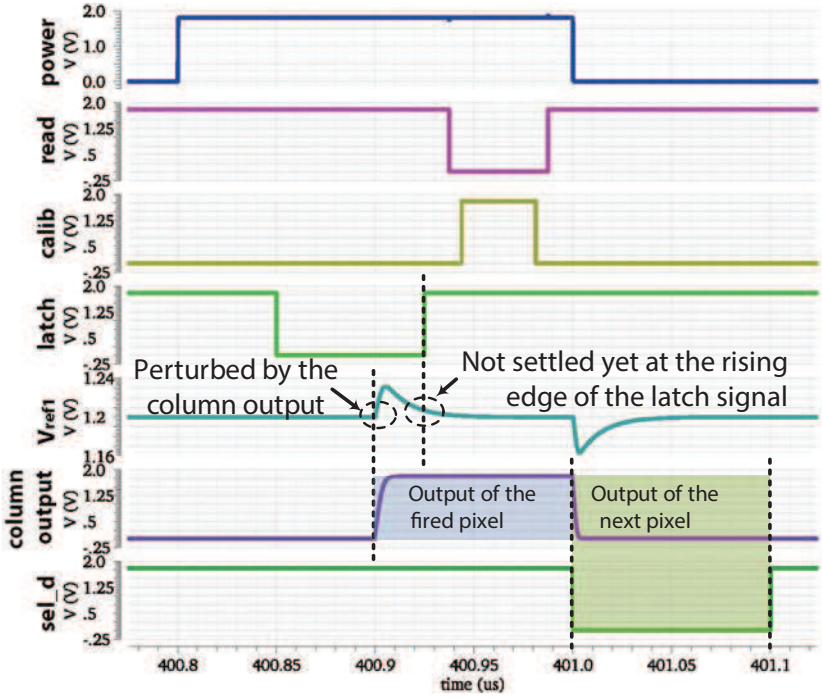
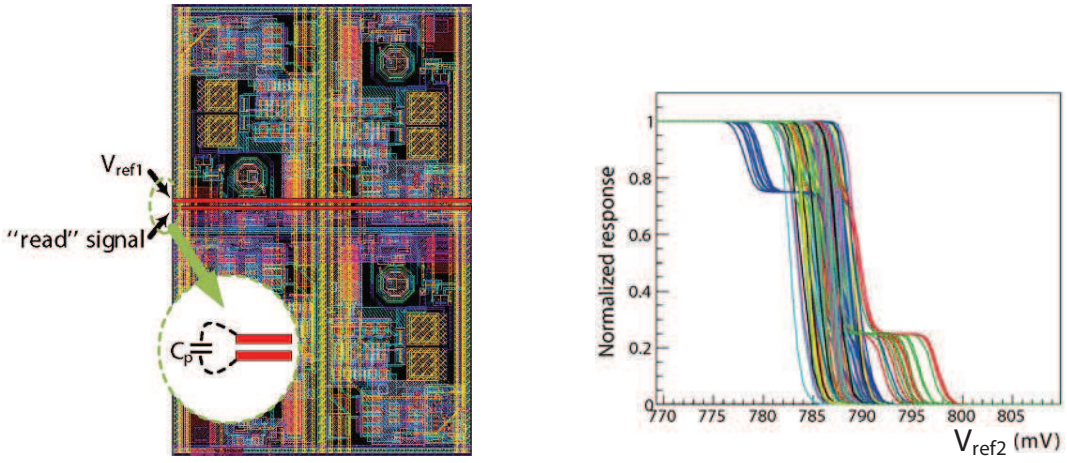


Figure 4.24: The simulated wave forms including the parasitic parameters extracted from layout. The voltage V_{ref1} is disturbed by the activities on the column output line.

However, when characterizing the full in-pixel circuitry, a major difference is that V_{ref1} is only applied to the discriminator during the *calib* phase. As can be seen from Fig. 4.24, V_{ref1} tends to be more stable in the *calib* phase. In addition, for V1, even if V_{ref1} is not fully settled, this voltage is applied to both of the discriminator inputs in the *calib* phase, resulting in no differential influence on the discriminator. Therefore, the full in-pixel circuitry can be characterized at the nominal speed with satisfactory "S" curves.

As for the double-row readout array, the layout strategy is different from the single-row readout array (see Fig. 4.18). The coupling mechanism in this double-row read-out array is more complicated, and is very difficult to be fully identified. One suspected

coupling source is illustrated in Fig. 4.25(a), where part of the reference V_{ref1} is coupled to the *read* signal in the fifth metal layer. Fig. 4.25(b) gives the "S" curves of the in-pixel discriminators in the double-row read-out array, measured at the nominal speed. These curves are less disordered as compared to the single-row read-out array, which may indicate that activities of the coupling sources are regular, e.g., the periodical *read* signal.



(a) (b)

Figure 4.25: (a) Illustration of the suspect coupling source (the layout shown contains four pixels) and (b) the "S" curves of the in-pixel discriminators measured at nominal speed for the double-row read-out V2.

Due to the coupling described above, the characterization was performed at lower speeds to study the discriminator performances. Fig. 4.26 gives the measured "S" curves when the row processing time is 200 ns and 400 ns. The derived average TN and FPN values are summarized in table 4.4. Due to a more complex structure, the in-pixel discriminators in V1 are more sensitive to the cross coupling effect. Their "S" curves are still disturbed when the row processing time is 200 ns (see the left part of Fig. 4.26(a)). It is also discovered that the FPN approaches to a constant value when the row processing time is longer than 400 ns, which agrees with the measurement results from the full in-pixel circuitry. This indicates that the mixed signal cross coupling effect is no longer a significant issue when the row processing time is longer than 400 ns, under which circumstance V1 gives a very promising FPN value of ~ 0.25 mV. As for V2, its FPN value approaches to ~ 0.4 mV, which is larger than V1. Moreover, the double-row readout array shows a larger FPN value than the

single-row readout array, but still less than its TN. These measurement results indicate that the noise of the in-pixel discriminators is dominated by the TN. The optimization of TN is addressed in the next Chapter.

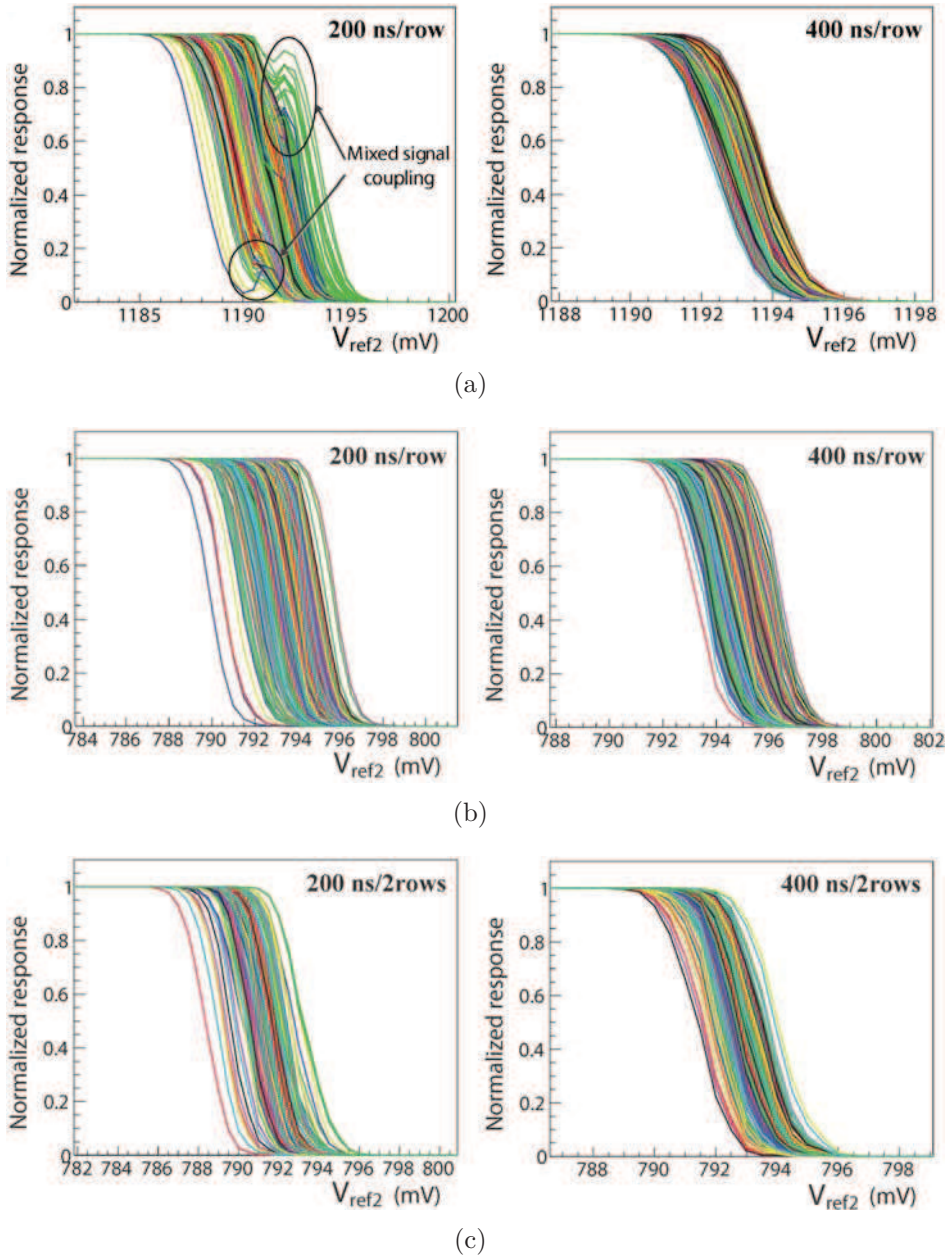


Figure 4.26: "S" curves of the in-pixel discriminators when row processing time is 200 ns (left) and 400 ns (right): (a) V1, (b) V2 and (c) double-row readout V2.

Table 4.4: Noise performance of the in-pixel discriminator in AROM-0.

Pixel version	Speed	TN (mV)	FPN (mV)	Total noise (mV)
V1	200 ns/row	1.03	0.60	1.19
	400 ns/row	0.97	0.25	1.00
V2	200 ns/row	0.81	0.65	1.04
	400 ns/row	0.85	0.41	0.95
V2 (2-row)	200 ns/2-rows	0.91	0.85	1.24
	400 ns/2-rows	0.85	0.55	1.01

4.3.4 Characterization of the latch circuit

In AROM-0, two dedicated arrays, one with 16 × 16 pixels and the other with 32 × 32 pixels, were implemented in order to verify the latch performance. The pixels in the former array are the same as those in the array of double-row readout V2, except that the latch inputs are connected to the two reference voltages, V_{ref1} and V_{ref2}, instead of the amplifier outputs, This is illustrated in Fig. 4.27. So, the latch can be studied separately, while the environment, where the latch is implemented, is preserved. The pixels in the 32 × 32 pixel array are similarly configured, but the array is divided equally into two sub-arrays, one containing the pixels as V1 and the other containing pixels as the single-row readout V2.

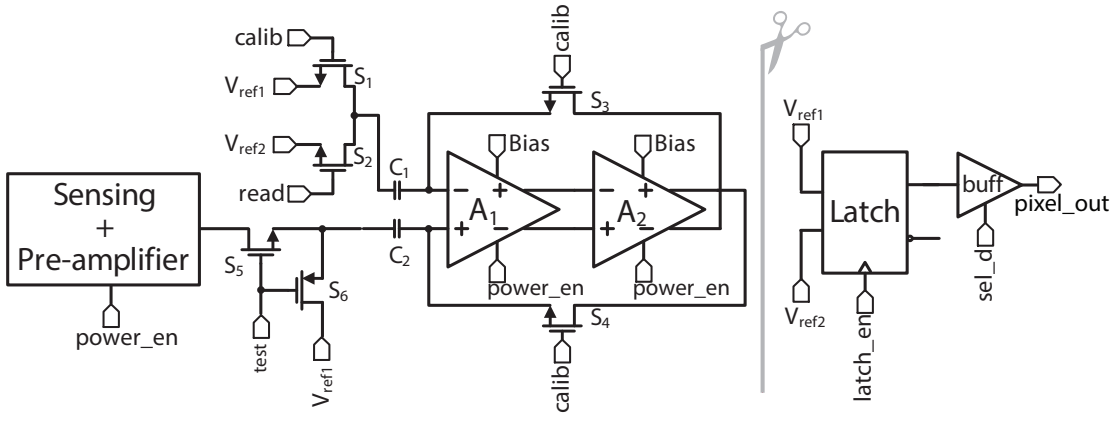


Figure 4.27: The illustration of the pixel used for latch measurement.

The noise of the latch circuit was measured using the "S" curve method. The common mode input voltage used for the measurement ranges from 0.7 V to 0.9 V, in order to study the sensitivity of the offset variation to the common mode input voltage. The extracted noise values are summarized in table 4.5. The offset variation (FPN)

stays below 3 mV for all the measured arrays. This verifies that the simulated result given in Section 4.2.3 only underestimated slightly the offset variation. In addition, the FPN increases with the common mode input voltage, agreeing with the equation (4.28).

Table 4.5: Noise performance of the latch.

Pixel version	Common mode input (V)	TN (mV)	FPN (mV)	Total noise (mV)
V1	0.7	0.70	2.19	2.30
	0.8	0.75	2.32	2.44
	0.9	0.76	2.49	2.61
V2	0.7	0.70	2.29	2.39
	0.8	0.75	2.48	2.59
	0.9	0.77	2.77	2.88
V2 (2-row)	0.7	0.74	2.22	2.33
	0.8	0.82	2.38	2.52
	0.9	0.73	2.55	2.66

4.4 Summary

The concept of in-pixel discrimination for CMOS pixel sensor was studied within the framework of the ALICE-ITS upgrade. The prototype chip, called AROM-0, was designed and fabricated in the *TowerJazz* 0.18 μm CIS process. Three topologies of discriminators were implemented in separate single-row readout pixel arrays, each containing 36 $\times$ 32 pixels. One of the three topologies (V2) was also implemented in a 18 $\times$ 16 double-row readout array. There are also two pixel arrays dedicated to evaluating the latch performance.

The chip was measured in laboratory to verify the functionality and to study the noise performance. The full in-pixel circuitry was characterized by using the "S" curve method at the nominal speed. The total ENC for all the pixel versions is around 30 e^-, which is encouraging for a first generation of AROM prototype. However, the noise still needs to be studied and improved. The measurements were also performed at lower speed to study the influence of the cross coupling. The FPN values for V1 and V3 first decrease significantly with the speed slowing down, and then stay almost constant when the row processing time is larger than 400 ns. These results indicate that the FPN values can be potentially improved, after careful layout design to minimize the

mixed signal cross coupling. However, V2 is less affected by the cross coupling for both the single-row and double-row readout arrays. But the ultimate FPN value V2 can achieve is larger than that of V1. It is noted that V1 and V2 were chosen for further development, since the disadvantages of V3 seem to defeat its advantages.

The in-pixel discriminators of V1 and V2 were characterized separately, being isolated from the sensing system. A strong coupling from some digital signals to the reference voltage has led to abnormal "S" curves when discriminators were measured at the nominal speed. Therefore, the discriminator performance was evaluated based on the measurements with lower speeds (e.g. 200 ns/row and 400 ns/row). The noise of the discriminators is dominated by the TN, which was unexpected. Furthermore, the FPN values become steady when the row processing time is longer than 400 ns. The steady FPN value for V1 is only ~ 0.25 mV, which is very promising. The study of TN and the layout optimization to minimize the cross coupling are addressed in the next prototype chips, called AROM-1, which will be discussed in the next chapter.

Chapter 5

Further pixel optimization: AROM-1

The AROM-0 has verified the feasibility of integrating an in-pixel discriminator into a small pixel, meeting the spatial resolution requirement of the inner layers of the ALICE-ITS upgrade. The noise performances are encouraging, but still need to be improved both for TN and FPN. The FPN can be improved by layout optimization and careful post layout simulation. As for the TN, the noise source should be further studied. In this chapter, the TN of the discriminators in AROM-0 is first analyzed, in order to gain some perspectives to optimize the pixel TN performance. Then, the next generation of prototype chips, called AROM-1, are introduced. The AROM-1 chips were designed as the intermediate prototypes that approach the ASTRAL sensor in many aspects, including the readout scheme and the periphery circuitry. Various new pixel designs, foreseen to have better noise performance than the AROM-0 pixels, were integrated in separate AROM-1 prototypes. Following the description of the AROM-1 design, the measurement results from laboratory are given.

5.1 Lessons learned from AROM-0

In the previous chapter, based on the measurements at different speeds, it is seen that the FPN of the discriminator, especially for V1, is largely affected by the cross coupling. If the layout of the pixel is carefully designed and verified with post layout simulation, the FPN performance of the in-pixel discriminators may be improved. However, the TN value of the discriminators is much larger than the FPN, which has to be reduced.

This section mainly focuses on the TN analysis for the discriminators in AROM-0, in order to gain some lessons and provide guidelines for further pixel optimization.

5.1.1 Pixel V1

The schematic of the pixel V1 in AROM-0 is recalled in Fig. 5.1. The main TN noise sources are the components at the input nodes of the discriminator, including the two NMOS source followers SF_1 and SF_2, and the three NMOS switches S_0 - S_2. With carefully designed biasing current and tuning the transistor dimensions, the source followers can achieve low noise performances. However, they still add noise to the input signal while providing a voltage gain less than unity. Moreover, concerning the voltage shifting effect of the source followers, the reference voltage V_{ref1} is set to 1.2 V in order to adapt the DC input range of the amplifier A_1. With 1.8 V gate control voltage, the switches mentioned above stay in the sub-threshold region when closed, which leads to a very large on-resistance. We consider the switch S_1. In principle, the noise of the switch represents itself as the kTC noise. The total kTC noise value over the entire bandwidth should depend only on the parasitic capacitance value at the input node of SF_1, regardless the resistance of the switch [127]. However, the shape of the noise spectrum does depend on the switch on-resistance. As illustrated in Fig. 5.1, if S_1 has a small on-resistance, its noise spectrum (shown in red line), has a small magnitude at the low frequency, but spreads over a wide frequency range. The PSD (power spectral density) of the switch thermal noise, $S_{ni}(f)$, is then shaped by the low-pass transfer function $H(f)$, formed by the following source follower SF_1 and the amplifier A_1. As a result, the noise PSD $S_{no}(f)$ at the output of A_1 only retains the low-frequency noise component, and then is sampled on the capacitors C_1 and C_2. It is clear that the total noise remaining within the system bandwidth is smaller for the switch with a small on-resistance. Thus, in order to optimize the noise performance, the input switches must be biased in the linear region (triode region) to achieve a small resistance value.

The conclusions above were verified by noise simulation of selectively choosing the noisy devices. The simulation results showed that the noise from the switches S_0 - S_2 dominated the total discriminator noise. The removal of the source followers, SF_1 and SF_2 in Fig. 5.1, will improve the biasing of the switches and thus reduce the impact of the switch noise. With this modification, the noise voltage value of the discriminator can be significantly decreased. Fig. 5.2 shows simulated noise distribution, referred to

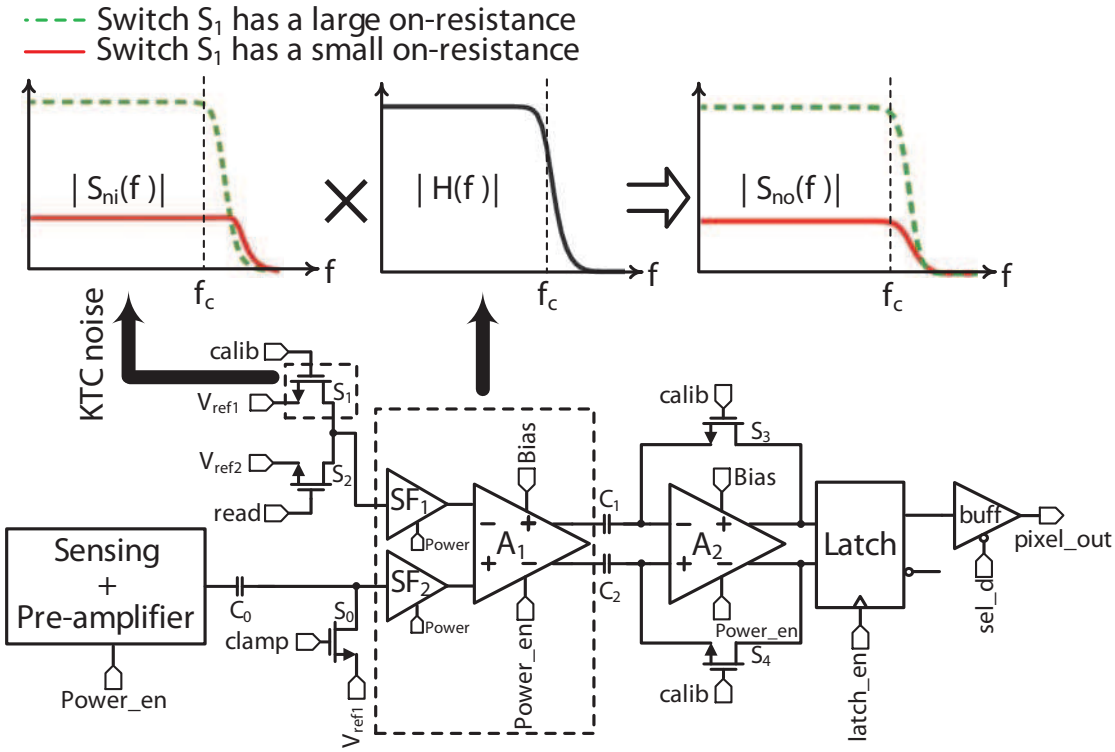


Figure 5.1: The noise spectral of the kTC noise from the switch S_1, $S_{ni}(f)$, is shaped by the transfer function $H(f)$ containing the source follower SF_1 and the differential amplifier A_1. f_c is the cutoff frequency of $H(f)$

the discriminator input, before (green) and after (red) the modification for AROM-0 V1. The transient noise simulation (TNS) was used. During the simulation, one noise sample was registered at each pixel access, and the sample is taken right before the latching phase of the discriminator. One thousand noise samples were registered for each simulation and the RMS value was calculated. The resulting noise is reduced from 1.6 mV to 0.4 mV after the modification. The discussion above forms the major guideline for the design of AROM-1.

5.1.2 Pixel V2

In pixel V2 (recall Fig. 4.11), the reference V_{ref1} is set to 0.8 V and the switches transferring the reference voltages are driven into linear region when closed, exhibiting relatively low on-resistance. However, the circuit topology limits the noise performance. Firstly, the feedback switches add noise directly to the input nodes, in form of kTC noise sampled on the input offset storage capacitors. Secondly, due to the closed-loop

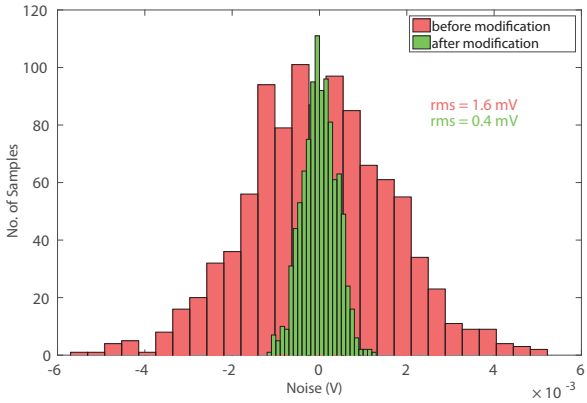


Figure 5.2: The simulated noise distribution, referred to the discriminator input, before (green) and after (red) the modification for AROM-0 V1.

operation in the auto-zeroing phase, its noise bandwidth is larger. Pixel V1 doesn't show these issues because the IOS is only employed for the second stage. The noise bandwidth issue can be explained by referring to Fig. 5.3, which gives the schematics of two circuits in the auto-zeroing phase employing OOS and IOS, respectively.

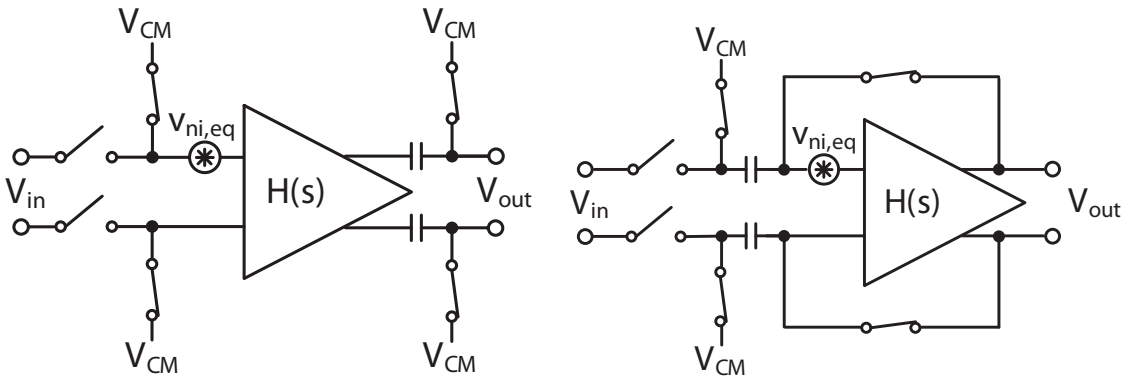


Figure 5.3: Schematics of the circuits employing (a) OOS and (b) IOS during the auto-zeroing phase.

It is first assumed that the amplifier has a first-order transfer function given by

$$H(s) = \frac{G_0}{1 + s\tau}. \tag{5.1}$$

where G_0 is the DC gain and τ is the time constant. Here we are concerned only by the thermal noise from the amplifier, which can be modeled by a voltage source $v_{ni,eq}$ with

a white spectrum $S_{ni}(f)$, present at the input of the amplifier. If the loading effects of the offset storage capacitors are neglected , the mean-squared (MS) values of the sampled noise, referred to the outputs of the circuits, after the auto-zeroing phase, are given by [128]

$$\overline{v_{no,oos}^2} = \int_0^\infty S_{ni}(f) \mid H(j2\pi f)) \mid^2 df = S_{ni}\frac{G_0^2}{4\tau}. \tag{5.2}$$

for Fig. 5.3(a) and

$$\overline{v_{no,ios}^2} = G_0^2 \int_0^\infty S_{ni}(f) \mid \frac{H(j2\pi f)}{1+H(j2\pi f)}) \mid^2 df = S_{ni}\frac{G_0^2}{4\tau}(\frac{G_0^2}{1+G_0}). \tag{5.3}$$

for Fig. 5.3(b). It can be seen that the total sampled noise power of using the IOS is greater by a factor of $G_0^2/(1+G_0)$. This phenomenon can be explained by the noise bandwidth. The OOS always works in open loop configuration and the noise is first filtered by $H(s)$ and then sampled on the offset storage capacitors. On the other hand, the IOS closes a unit gain feedback loop during the auto-zeroing phase. And the noise is shaped by the closed-loop transfer function $H(s)/(1+H(s))$, which has a larger bandwidth than the open-loop transfer function $H(s)$. It is noted that the noise of the IOS is sampled at the input nodes and it will be multiplied by the DC gain of the amplifier. Therefore, the output noise spectra for the IOS and the OOS have similar low-frequency magnitudes, but the IOS has a larger noise bandwidth.

If $H(s)$ is a second-order transfer function as in the V2 case, where two directly cascaded amplifiers form a two-stage high gain amplifier, to model the noise and make a calculation like (5.3) are much more complicated. However, similar conclusion can be drawn. In addition, due to the stability issue of V2, the close-loop transfer function shows a peak, as illustrated in Fig. 5.4. The noise component around the peak region will be augmented and sampled at the input, leading to a larger total noise. Simulation results showed that V2 has an input referred noise voltage 1.5 times larger than V1, if only the amplifier noise is considered.

Due to this structure limitation, it is very difficult to largely reduce the TN of V2. However, its simpler structure is still an advantage. Moreover, the noise issue can be compensated, to some extent, by optimizing the sensing system in the future, for lower RTS noise and a higher CVF. Therefore, a satisfactory SNR is still likely to be achieved with the discriminator V2.

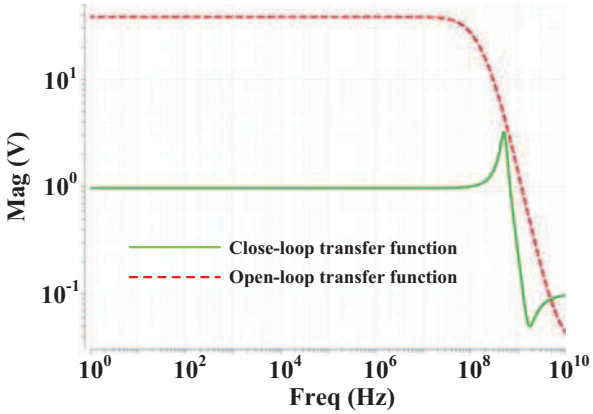


Figure 5.4: The simulated close-loop (green solid line) and open-loop (red dashed line) transfer functions for the two-stage amplifier in AROM-0 V2.

5.2 Design of AROM-1

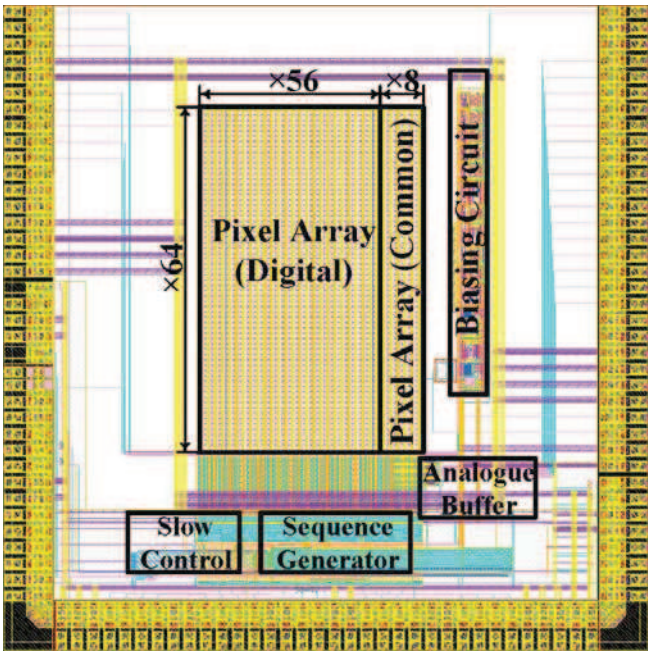


Figure 5.5: The layout of AROM-1.

Based on the experience from the AROM-0 prototype, a series of prototype chips, named AROM-1, were submitted in two separate MPW runs, in August 2013 and in November 2013. They conceive two main purposes: to verify the improvement of pixel performances, and to approach the final sensor architecture proposed for the ALICE-ITS upgrade. The AROM-1 prototypes were fabricated by using the high-resistivity

epitaxial wafers (> 1 kΩcm), provided by *TowerJazz*.

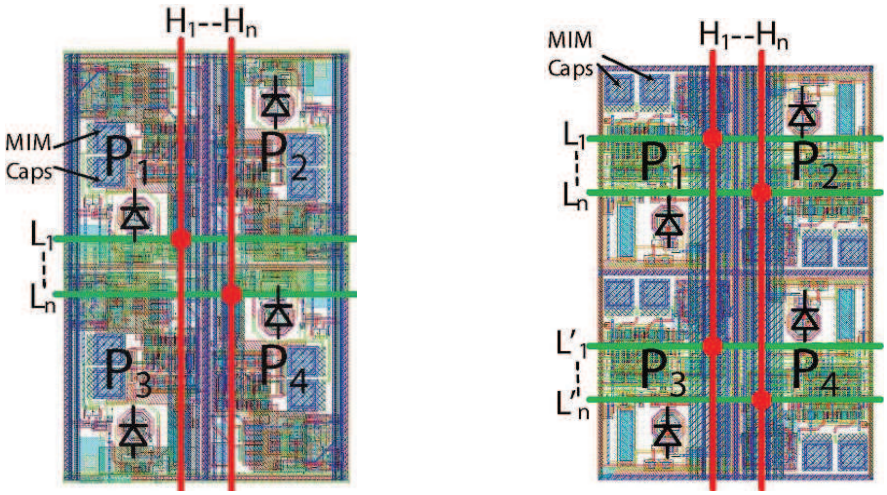
Fig. 5.5 gives the layout of an AROM-1 chip, with some of its main blocks located in the figure. The sensor is composed of a matrix with 64×64 pixels. The readout is based on the rolling shutter mode. At each time, two rows of pixels are read out simultaneously. The 128 (2×64) digital pixel outputs are multiplexed to 16 binary output pads. Eight columns, on the right side of the pixel matrix, are implemented with modified digital pixels to study the pixel analogue response, i.e., with a source follower inside each pixel to read out the analogue signal. On the chip level, the analogue signals are buffered to the 16 (2×8) output pads for the analogue test. As compared to AROM-0, the AROM-1 chip features an on-chip sequence generator, fully programmable by the slow control logic. In addition, the biasing circuit, which is also programmable by tuning the corresponding DACs, provides precisely the necessary biasing/reference for the pixel matrix. The AROM-1 series can be categorized into two chip groups, one contains AROM-1 A/B/C and the other includes AROM-1 E/F. In the following part of this section, the pixel design of the AROM-1 chips is described.

5.2.1 AROM-1 A/B/C

As mentioned in Section 5.1.2, the pixel V2 in AROM-0 is still likely to achieve satisfactory SNR, assuming the layout design is improved and the sensing system is further optimized. Due to the tight submission deadline and the fact that there already existed the double-row readout experience for the AROM-0 V2, the chip AROM-1 was first developed based on the pixel topology of AROM-0 V2. In the MPW run of August 2013, three different chip versions were submitted, with the names of AROM-1 A, AROM-1 B and AROM-1 C. The three chip versions distinguish each other by the pixel layout design or by the pixel pitch.

One major difference of the AROM-1 A/B/C, from the AROM-0 prototype, is the sensing system. In AROM-1 A/B/C, the length of the pre-amplifier's input transistor is 0.36 μm, twice of that in AROM-0. By doing this, the RTS noise, exhibited in the AROM-0 prototype, was expected to be largely mitigated (see Section 3.2.3 and Section 4.3.1).

In AROM-1 A, a similar layout of the pixel array, as the double-row readout pixels of AROM-0 V2, was used. But the routing of some signals was rearranged, hoping to mitigate the suspected cross coupling effect described in Section 4.3.2. The AROM-1 A was submitted as the reference chip, since its pixel design has no significant difference



(a) (b)

Figure 5.6: The layout comparison of (a) AROM-1 A and (b) AROM-1 B. The red lines represent the vertical metal lines (metal six) connecting the sequence generator at the bottom of pixel matrix, and the green lines represent the metal lines (metal five) distributing the control signals to the corresponding row (or rows).

from the AROM-0 double-row V2. The AROM-1 B incorporates a different layout for the pixel array, which is more symmetric and was expected to have less cross coupling. The AROM-1 C uses similar layout as the AROM-1 B, but the pixel pitch is extended slightly in one dimension from 22 μm to 24 μm. The larger dimension of AROM-1 C allows to explore if the cross coupling is highly dependent on the pixel pitch, while a proper spatial resolution is still maintained to meet the ALICE-ITS upgrade requirement.

Fig. 5.6 compares the layouts of AROM-1 A and AROM-1 B. In Fig. 5.6(a), the metal lines from L_1 to L_n, each distributing a corresponding control signal, are shared by two neighbouring rows. Due to staggered diode arrangement, the diodes of pixel P_1 and P_4 are very close to the horizontal signal lines, while the diodes of pixel P_2 and P_3 are relatively far from those lines. In addition, pixel P_1 and P_2 are more likely to be influenced by line L_1, whereas pixel P_3 and P_1 are more likely to be influenced by line L_n. As a result, the four pixels in Fig. 5.6(a) all have different signal distribution environments. In Fig. 5.6(b), each row has its own metal lines to distribute the control signals (e.g. L_1 and L'_1 distribute the same signal). So, the two pixels on the same side have the same signal distribution environment. The drawbacks of the former layout

also include that the MIM capacitors can only be placed in the middle of the pixel, which makes it impossible to lay out a circuit like the AROM-0 V1 for double-row readout, due to signal routing difficulties introduced by the additional MIM capacitor. However, the layout like Fig. 5.6(b) has the disadvantage of more parasitic capacitance on the signal lines, since two separate horizontal metal lines are used to distribute the same signal. When a very large pixel array is considered, careful simulation must be made to ensure the signal skewing and the sloping edges, caused by the large parasitic capacitance on signal lines, are acceptable.

5.2.2 AROM-1 E/F

In the MPW of November 2013, another two chip versions of the AROM-1 series were submitted, namely AROM-1 E/F. They are made of pixels derived from the AROM-0 V1. The pixel pitch for AROM-1 E is 22 μm $\times$ 33 μm, whereas that of AROM-1 F is 27 μm $\times$ 27 μm. The squared pixel of AROM-1 F facilitates the layout design, since the diode placement is not staggered anymore. In order to study the trade-off between noise and CVF of the sensing system, the gate width of the pre-amplifier's input transistor is further extended as compared to AROM-1 B, from 1 μm to 1.5 μm.

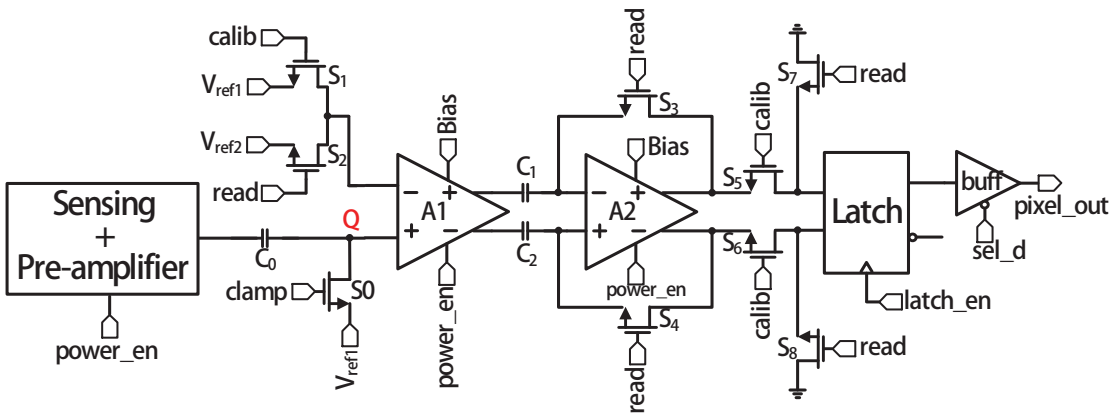


Figure 5.7: The simplified pixel schematic for the AROM-1 E and AROM-1 F.

Fig. 5.7 gives the pixel schematic that has been implemented in AROM-1 E/F. The main modification in the pixel schematic, as compared to the AROM-0 V1, is the removal of the source followers at the discriminator inputs, complying with the discussion in Section 5.1.1. The timing sequence is also modified, which is shown in Fig. 5.8. The working principle is slightly different from AROM-0 V1 and can be

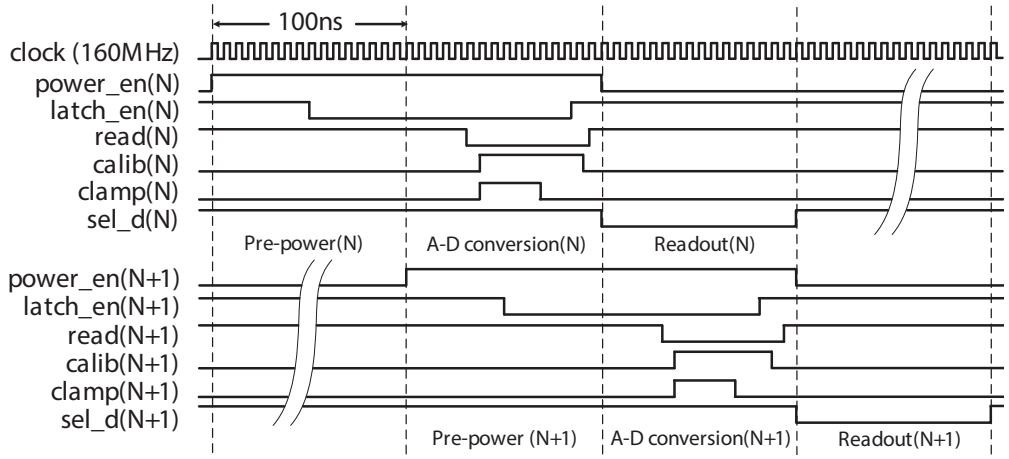


Figure 5.8: The timing diagram of the AROM-1 E and AROM-1 F.

described as follows. At the end of the *read* phase, the differential voltage memorized in the capacitors C_1 and C_2 is

$$V_{mem} = G_1(V_{ref2} - V_{Q,read} - V_{OSA1}) - \frac{V_{OSA2}}{1+G2} \tag{5.4}$$

where $V_{Q,read}$ is the voltage of the node "Q" by the end of the *read* phase; G_1, G_2 are the gains of the amplifier A_1 and A_2; and V_{OSA1} and V_{OSA2} are the offsets of A_1 and A_2. Then, the inputs of A_1 are connected to V_{ref1} by closing S_0 and S_2. The switch S_0 is open first and the voltage on the node "Q" becomes

$$V_{Q,base} = V_{ref1} - V_{charge} \tag{5.5}$$

where V_{charge} is due to the charge injection and clock feed-through of switch S_0. This voltage can be seen as the baseline voltage on the node "Q". Just before the end of *calib* phase, the rising edge of the *latch_en* signal activate the latch circuit, and the latch input voltage at this moment is

$$\begin{aligned} V_{latch,in} &= G_2[G_1(V_{ref1} - V_{Q,base} - V_{OSA1}) - V_{mem}] \\ &= G_1G_2[(V_{Q,read} - V_{Q,base}) - V_{th}] + \frac{G_2V_{OSA2}}{1+G_2} \end{aligned} \tag{5.6}$$

where V_{th} is the threshold voltage, defined by

$$V_{th} = V_{ref2} - V_{ref1} \tag{5.7}$$

Note that $V_{Q,read}$ includes the integrated signal during the read-out period, superimposed on the baseline voltage set from the previous read-out cycle. Therefore, the signal voltage is

$$V_{sig} = V_{Q,read} - V_{Q,base} \tag{5.8}$$

Substituting (5.8) in (5.6) gives

$$V_{latch,in} = G_1 G_2 (V_{sig} - V_{th}) + \frac{G_2 V_{OSA2}}{1 + G_2} \tag{5.9}$$

The last term results from the offset of A_2, that is not fully compensated by the IOS. Excluding this small remaining offset, the latch circuit senses the amplified difference between the signal voltage and the threshold voltage, and provides a CMOS level based on its input polarity. It is worth mentioning that the latch circuit is only connected to the output of A_2 during the *calib* phase by switching S_5 - S_8. In this way, the kick-back due to the reset of the latch circuit, on the falling edge of *latch_en* signal, is removed.

One of the advantages of this new timing sequence is that the bandwidth of the amplifier A_1 can be traded for the gain and power. The speed of the discriminator is mainly limited by the amplifier A_1 during the *read* phase, when it is directly loaded by the large offset storage capacitors. The new timing sequence leaves sufficient time for A_1 to settle in the *read* phase, thanks to the fact that the pixel is switched on 100 ns in advance (the first half of the *power_en* signal) for circuit settling. This is different from the AROM-0 V1, where very limited time duration (the length of the *calib* phase in Fig. 4.13) can be employed by the critical amplifier A_1 to settle (see Section 4.2.3).

Table 5.1: Simulation results for the amplifiers used in AROM-1 E/F.

Amplifier	Biasing current	Gain	Bandwidth
AROM-0 amplifier[a]	15 μA	6.9	35.2 MHz
A_1&A_2 in AROM-1 E[b]	7.3 μA	8.8	16.3 MHz
A_2 in AROM-1 F[c]	2.75 μA	6.0	48.4 MHz

[a]Simulated with 0.7 V DC input and 80 fF load capacitor.
[b]Simulated with 0.75 V DC input and 80 fF load capacitor.
[c]Simulated with 0.92 V DC input and 10 fF load capacitor.

For design simplicity, in AROM-1 E, the amplifier A_1 and A_2 use the same transistor parameters. Table 5.1 gives the simulated performances of the amplifier. As compared to the differential amplifier used in AROM-0, the new amplifier has a larger gain and

lower biasing current, sacrificing the bandwidth. The larger gain can further mitigate the offsets from the latch and the amplifier A_2. The total static current consumption is about 18 μA per pixel, which is less than half of that consumed by the AROM-0 V1. In AROM-1 F, the power consumption of the second amplifier A_2 is further reduced, since the speed and noise requirements of A_2 is not as critical as A_1. As a result, the static current consumption of AROM-1 F is about 13 μA per pixel. The simulation results of the amplifier A_2 in AROM-1 F is also summarized in Table 5.1.

By removing the source followers at the discriminator input nodes and using the new amplifiers, the discriminators of AROM-1 E/F have larger gain before the latch circuit, allowing for trading the latch random offset for less area. Thus, the area of the dynamic latch was decreased by 13 % in the layout, from 10 μm $\times$ 16.5 μm to 10 μm $\times$ 14.5 μm, by reducing the transistor size in the latch circuit. The simulated offset variation of the new latch is shown in Fig. 5.9. As compared to the former latch used in AROM-0, the offset variation is increased by about 50 %, reaching a value of 3.1 mV. The increased latch random offset can be compensated by the larger gain of the new amplifier, and a similar FPN value as the AROM-0 V1 was expected for the AROM-1 E/F.

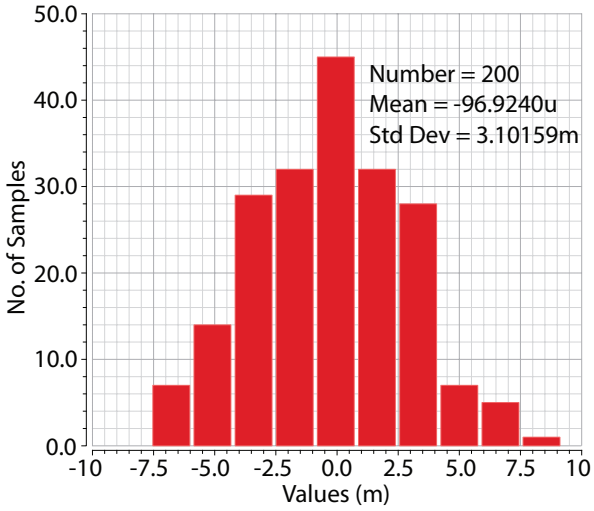


Figure 5.9: Simulated offset distribution of the dynamic latch used in AROM-1 E/F.

5.3 Laboratory measurement

The functionality as well as the noise performances of the AROM-1 chips were evaluated in laboratory. The data acquisition system used for AROM-1 economically reuses an existing system designed for the test of the MIMOSA 22 chips [129,130], which employ the column-level discrimination. The digital data acquisition board allows a maximal clock frequency of 100 MHz, leading to a read-out speed of 160 ns/2-rows. Despite this speed limitation, the measurements can still effectively estimate the chip performances. In this section, the experimental setup is briefly introduced. Then the measurement results for these AROM-1 chips are presented.

5.3.1 Experimental setup

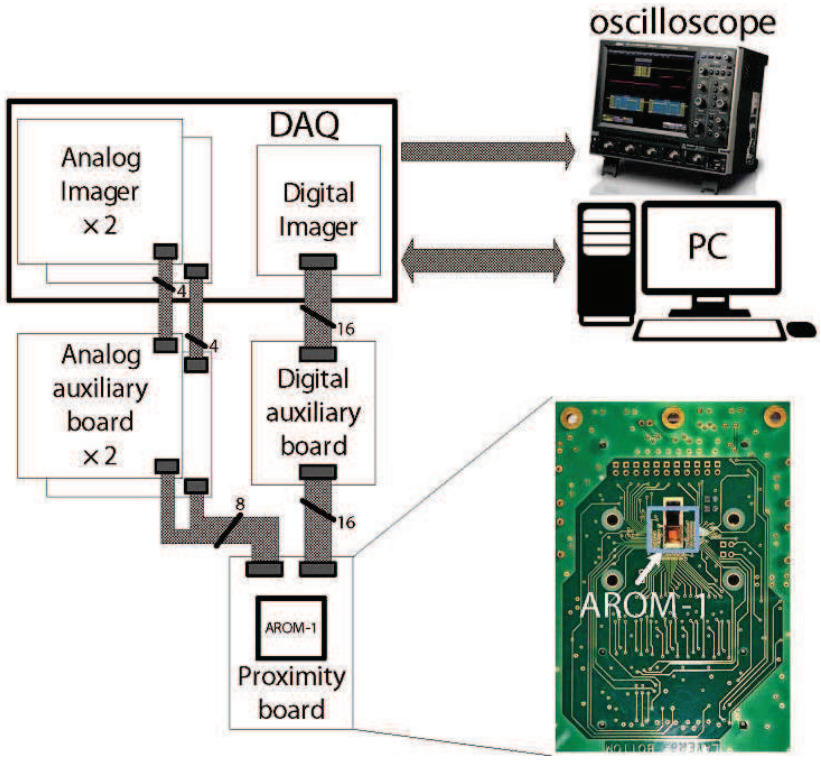


Figure 5.10: The experimental setup for the test of AROM-1.

The experimental setup for the test of AROM-1 is shown in Fig. 5.10. The sensor chip is wire-bonded to a small sized PCB board called proximity board. The board includes only the minimum front-end electronic, i.e., the buffering and amplification for the critical signals. The use of proximity board allows to adapt different DUTs

(device under test) to the existing system with minimum cost. The proximity board is interfaced with the data acquisition boards by two different kinds of auxiliary boards, one named analog auxiliary board and the other named digital auxiliary board. Two analog auxiliary boards are used to buffer up to 8 channels of analog signal from the chip in differential mode for long-distance (40 m) transmission. The digital auxiliary board generates the 100 MHz clock for the sensor chip. It also buffers all the digital communications between the data acquisition boards and the sensor chip in LVDS. In addition, it provides power supply for the chip and the proximity board. The data acquisition board, named Imager, is based on USB bus. It has the standard 6U VME[1] size and acquires the power supply from the VME crate. The USB 2.0 bus is used for board control and data transfer [131]. Each Imager board is equipped with four differential analog channels connected to fast 12-bit ADCs. The board contains banks of SRAM memory, used for temporary data storage. The on-board FPGA logic controls the data flow from ADCs to the RAM and then to the PC for storage. System control GUI, on-line monitoring, and data storage tasks are handled by a remote PC running Windows.

5.3.2 Measurements with an ^{55}Fe iron source

In order to obtain the analogue output of the sensing system for calibration, an NMOS source follower is placed inside each pixel of the eight analogue columns, buffering the analogue signal from the sensing system to the column line. An additional PMOS source follower is used at the chip periphery for each output channel, to effectively drive the signal to the outside of the chip. This is shown in Fig. 5.11. The NMOS source follower is biased at 50 μA and the PMOS source follower is biased at 500 μA.

The sensing calibration was performed by registering the responses of those analogue pixels to an ^{55}Fe iron source. The coolant temperature is 15 °C. Fig. 5.12 gives the measured analogue output spectra of AROM-1 B and AROM-1 E for the seed pixel, the set of 4 pixels and the set of 9 pixels in a cluster with the largest signal. The calibration peak was estimated by a Gaussian fit around the peaking area. For AROM-1 B, the calibration peak is located at 243 ADC units. And for AROM-1 E, the peak is located at 189 ADC units. Here, each ADC unit corresponds to $\sim$ 0.38 mV, when referred to the input of the in-pixel NMOS source follower. Thus, the CVF is calculated to be

[1]VMEbus (Versa Module Europa bus) is a computer bus standard.

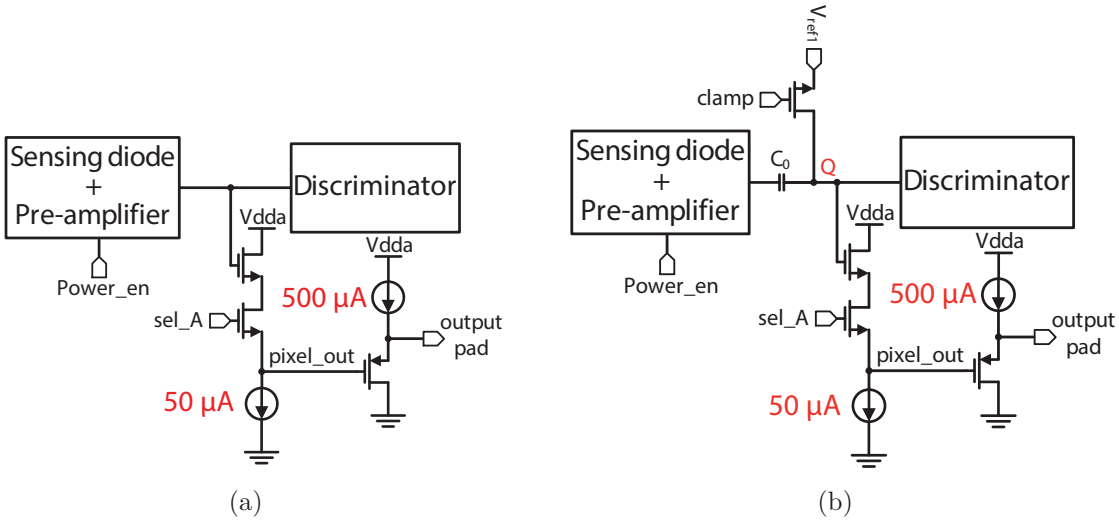


Figure 5.11: The analogue output configuration for the AROM-1 pixels: (a) AROM-1 A/B/C, (b) AROM-1 E/F.

56 μV/e$^-$ for AROM-1 B, and 44 μV/e$^-$ for AROM-1 E.

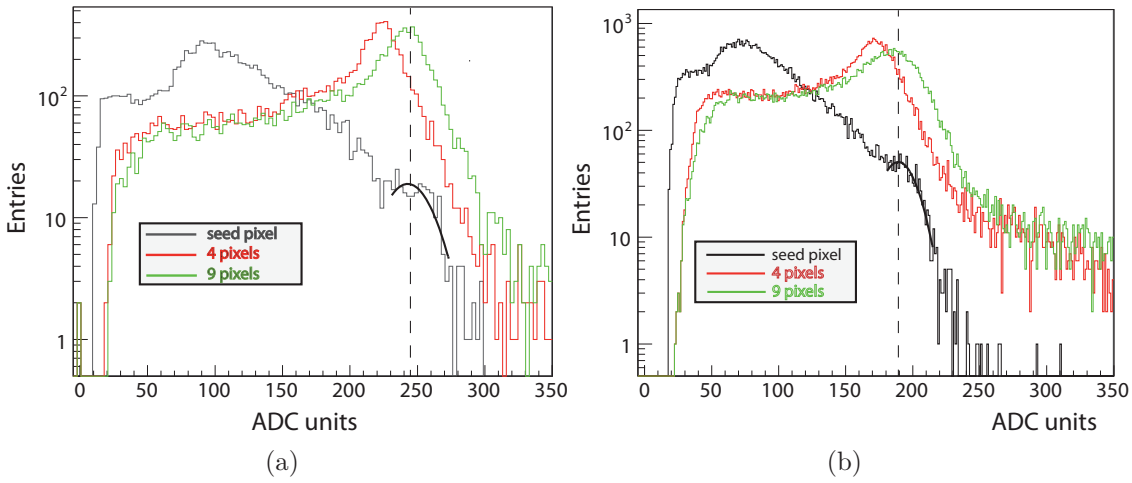


Figure 5.12: The responses of the analogue pixels to the ^{55}Fe iron source for (a) AROM-1 B and (b) AROM-1 E. Black line: seed pixel. Red line: the set of 4 pixels in a cluster with the largest signal. Green line: the set of 9 pixels in a cluster with the largest signal

On one hand, as compared to AROM-1 B, the AROM-1 E has a wider input transistor for its pre-amplifier, which tends to promote the amplifier gain. On the other hand, the larger input transistor increases the parasitic capacitance on the sensing

node. These two factors contradict with each other and the latter seems to overcome the former, resulting in a decreased overall CVF. The lower CVF for AROM-1 E is also partially attributed to the capacitive divider effect at the node Q in Fig. 5.11, similarly as the AROM-0 V1. From the discriminator point of view, a larger CVF for the sensing system is preferable. However, the RTS noise of the pre-amplifier, which depends highly on the dimension of its input transistor, should also be considered. An optimal dimension for the pre-amplifier is still to be explored, which is out of the scope of this thesis. The sensing calibration was also performed on the AROM-1 A and the AROM-1 F, and they exhibited very close CVFs to AROM-1 B and AROM-1 E, respectively. Hence, for simplicity reason, the measured CVFs for AROM-1 B and AROM-1 E are also used in the following part to estimate the pixel ENC values for the other chip versions with the same sensing systems.

From Fig. 5.12, one can also observe that the CCE for the AROM-1 chips is significantly improved as compared to AROM-0, thanks to the high-resistivity epitaxial layer. The seed pixel collects about 40 % of the total charge, and about 90 % of the total charge is collected by the cluster of 4 pixels. These values comply with the results with the traditional analogue pixels (see Section 3.2.2).

5.3.3 Characterization of the full in-pixel circuitry

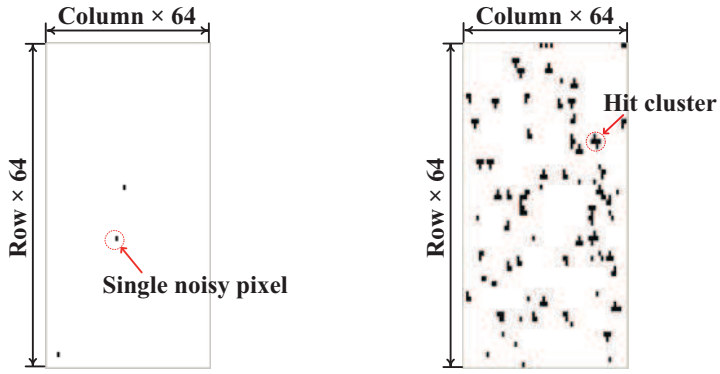


Figure 5.13: Accumulated hit events after 70 read-out frames for an AROM-1 E chip operating at 15 °C with 100 MHz clock. (a) without the radiation source; (b) with the radiation source.

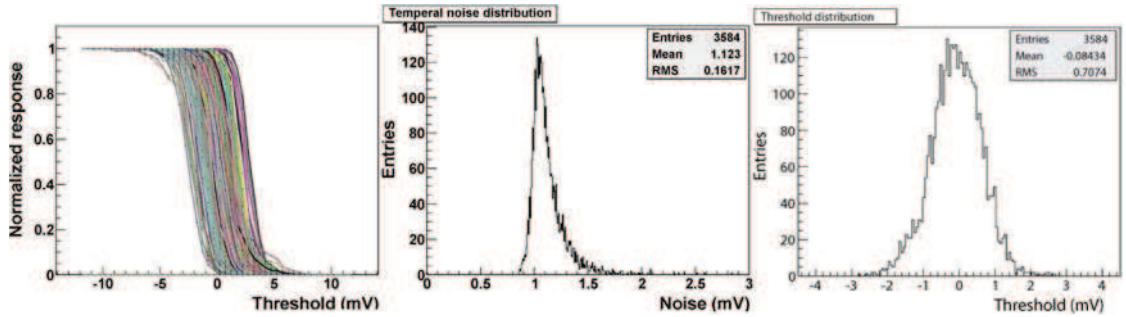
Before evaluating the noise performance of the full in-pixel circuitry, the digital

response of each measured chip to an ^{55}Fe source was monitored by using the data acquisition software in the Window environment, in order to verify the particle detection capability of the digital pixels. The monitoring proceeds as follows. First, an arbitrary threshold is set, so that the monitored hit events, due to noise fluctuation, are very rare. Then, the chip is illuminated by an ^{55}Fe source. If the chip is capable of detecting the impinging photons, a significant raise of hit event rate should be observed. Fig 5.13 gives the screen shots of the data acquisition software, which shows the accumulated fired pixels monitored for 70 read-out frames, in an AROM-1 E chip running with a 100 MHz clock at 15 °C. Fig. 5.13(a) is the monitoring run without the radiation source, where several single fired pixels caused by noise fluctuation can be seen. When irradiated by the ^{55}Fe source, as shown in Fig. 5.13(b), the number of accumulated fired pixels is obviously increased. And for most cases, a particle hit results in a cluster of fired pixels. After verifying the detection capability, the "S" curve method was used to evaluate the noise performance of the AROM-1 chips and the measurement results with the coolant temperature of 15 °C are given in the following.

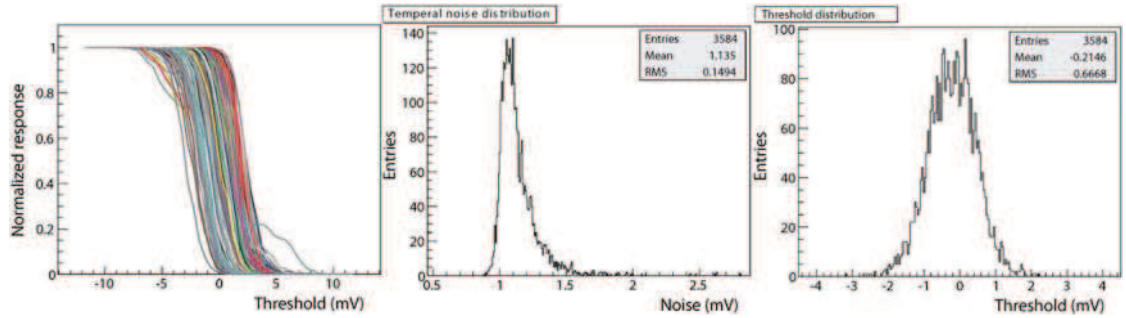
AROM-1 A/B/C

The measured "S" curves, noise distributions and the threshold distributions for the full in-pixel circuitry of AROM-1 B and AROM-1 C are shown in Fig. 5.14. The results given were measured with a 100 MHz clock frequency, translating into a read-out speed of 160 ns/2-rows. As for AROM-1 A, it seems that the modifications made in the layout, as compared to the AROM-0 double-row V2, have introduced more severe cross coupling. Only when the clock frequency is reduced to 10 MHz, the particle detection capability of the chip can be clearly monitored and all the measured "S" curves have smooth transition regions. Since the AROM-1 B and C were designed as the optimized versions, the coupling issues in AROM-1 A were not further investigated, and the chip was only characterized with 10 MHz clock to have an impression about its noise performance. The extracted noise values of AROM-1 A/B/C are summarized in Table. 5.2. In order to study the dependence of FPN on the read-out speed, AROM-1 B and AROM-1 C were also characterized with a 10 MHz clock, and the results are included in the table.

The noise performances of the three chip versions are very similar. It can be seen from the noise distributions (the middle graphs in Fig. 5.14) that the RTS like noise, exhibiting long tail towards the high noise value, is mitigated as compared to AROM-0,



(a)



(b)

Figure 5.14: "S" curves of the full in-pixel circuitry (left), the extracted TN distributions (middle) and threshold distributions (right) for (a) AROM-1 B, and (b) AROM-1 C. The readout speed is 160 ns/2-rows.

thanks to the increased gate length of the pre-amplifier's input transistor. As a result, the temporal noise of these AROM-1 chips is less than their ancestor, AROM-0 V2, but it still dominates over the FPN. The AROM-1 C has a slightly lower FPN value than AROM-1 B with the 100 MHz clock, which may be explained by the extended dimension of the AROM-1 C pixel. With a much lower clock frequency (10 MHz), the FPN values of AROM-1 B/C both reach about 0.6 mV, decreased by 14 % and 10 % respectively. The ENC values for all the three chip versions are about 24 e^-, estimated by using the CVF of AROM-1 B.

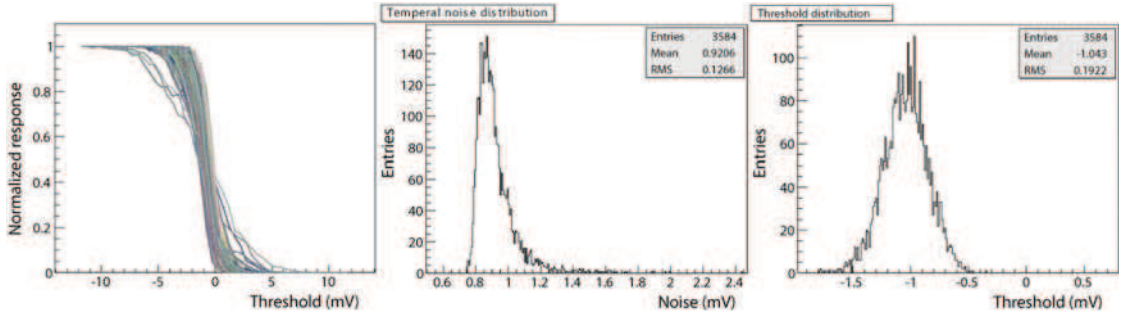
AROM-1 E/F

The measurement results of the full in-pixel circuitry in AROM-1 E and AROM-1 F, at the read-out speed of 160 ns/2-rows, are shown in Fig. 5.15. Table 5.3 summarizes their noise values. For AROM-1 E, the FPN value is only 0.19 mV, much lower than

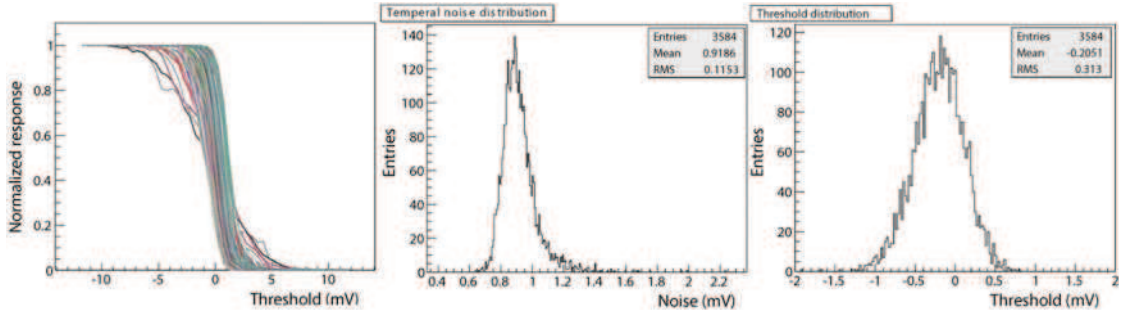
Table 5.2: Noise performance of the full in-pixel circuitry in AROM-1 A/B/C.

Chip version	Clock frequency (MHz)	TN (mV)	FPN (mV)	Total noise (mV)	ENC[a] (e^-)
AROM-1 B	100	1.12	0.71	1.33	23.8
	10	1.16	0.61	1.31	23.4
AROM-1 C	100	1.14	0.67	1.32	23.6
	10	1.16	0.60	1.31	23.4
AROM-1 A	10	1.10	0.74	1.33	23.8

[a]Calculated based on the measured CVF of AROM-1 B.



(a)



(b)

Figure 5.15: "S" curves of the full in-pixel circuitry (left), the extracted TN distributions (middle) and threshold distributions (right) for (a) AROM-1 E, and (b) AROM-1 F. The readout speed is 160 ns/2-rows.

those achieved by AROM-1 B/C. And for AROM-1 F, this value is 0.31 mV. One of the explanations for the larger FPN in AROM-1 F is its lower amplifying gain before the latch (see Section 5.2.2). These measurement results of FPN confirm the discussion in Section 4.3.2 that the topology of AROM-0 V1 has good potential for low FPN. As for the TN, both AROM-1 E and AROM-1 F have a value of 0.92 mV, which is also lower

Table 5.3: Noise performance of full in-pixel circuitry in AROM-1 E/F.

Chip version	TN (mV)	FPN (mV)	Total noise (mV)	ENC[a] (e^-)
AROM-1 E	0.92	0.19	0.94	21.4
AROM-1 F	0.92	0.31	0.97	22.0

[a]Calculated based on the measured CVF of AROM-1 E.

than those of AROM-1 B/C. Thus, despite the lower CVF for the AROM-1 E/F, their ENC values are better than AROM-1 B/C, slightly exceeding 20 e^-.

5.3.4 Characterization of the in-pixel discriminator

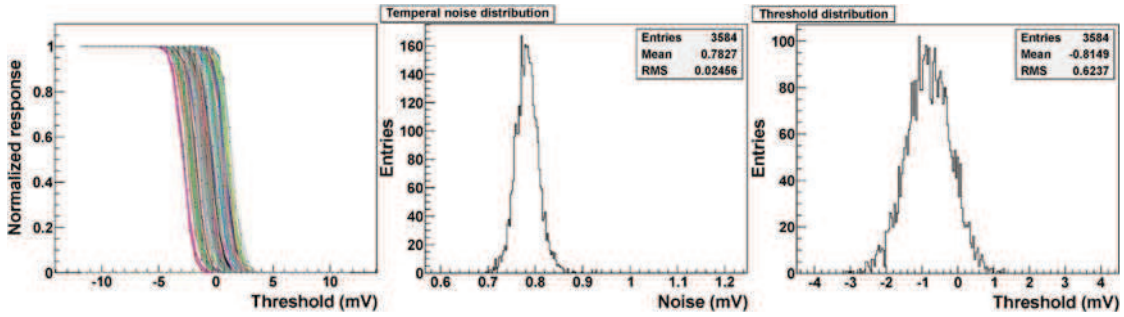
Similarly to AROM-0, the in-pixel discriminators of these AROM-1 chips were measured, in order to study their noise contributions.

AROM-1 B/C

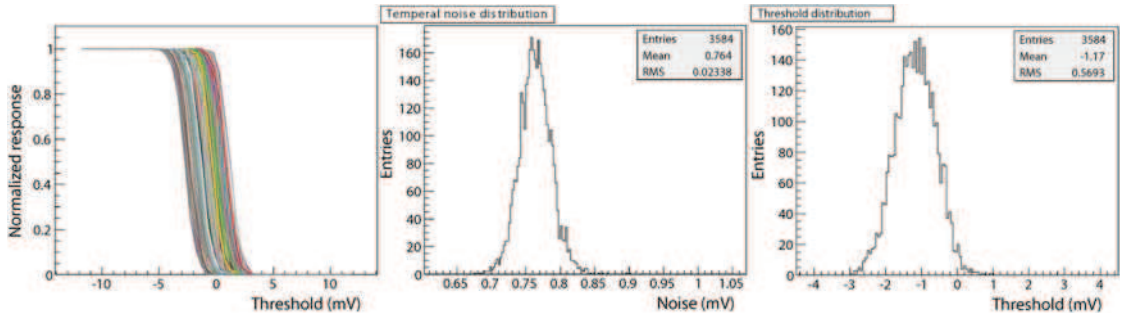
Fig. 5.16 gives the "S" curves, noise distributions and threshold distributions of the in-pixel discriminators in AROM-1 B/C, measured with the 100 MHz clock, and table 5.4 summarizes the extracted noise values. The discriminators of AROM-1 B and AROM-1 C have similar noise performance, with a TN of about 0.8 mV and an FPN of about 0.6 mV. These discriminators were also characterized at lower read-out speed, using 10 MHz clock, and the noise values stay almost the same. Combining the results of the full in-pixel circuitry given in table 5.2, one can conclude that the in-pixel discriminators of AROM-1 B/C contribute most of the total FPN, and their TN value is equivalent to that of the sensing system. In addition, the improvement of the ENC, as compared to AROM-0 V2, results mostly from the mitigated RTS noise from the sensing system.

Table 5.4: Noise performance of in-pixel discriminator in AROM-1 B/C.

Chip version	Clock frequency (MHz)	TN (mV)	FPN (mV)	Total noise (mV)
AROM-1 B	100	0.78	0.62	1.00
	10	0.78	0.61	0.99
AROM-1 C	100	0.76	0.57	0.95
	10	0.79	0.58	0.98



(a)

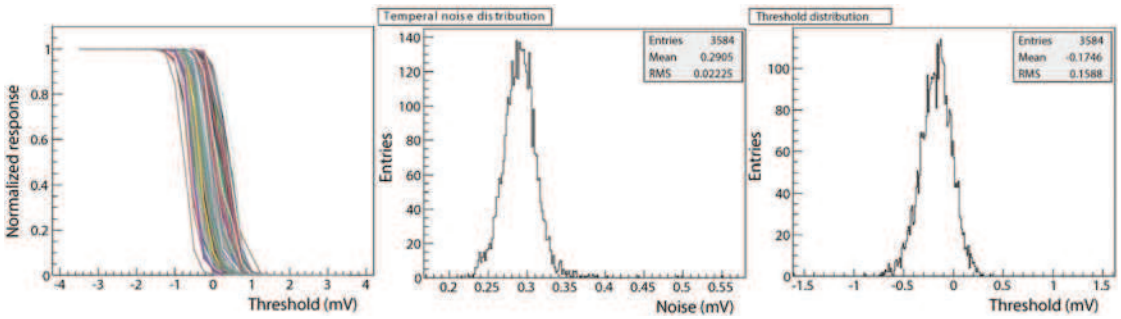


(b)

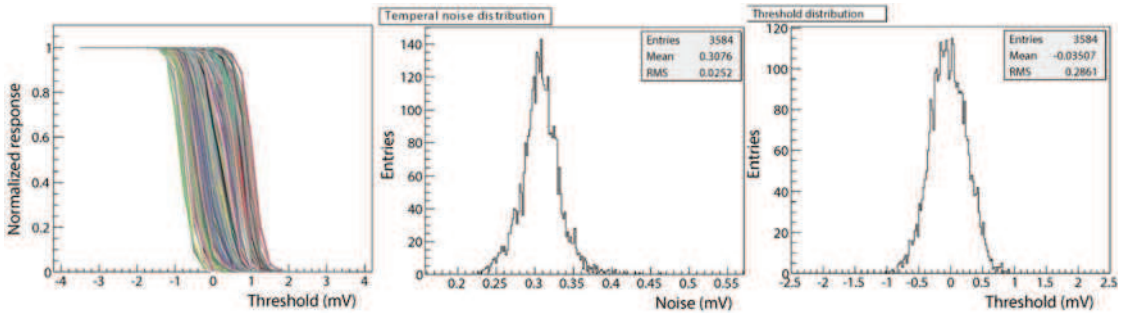
Figure 5.16: "S" curves of the in-pixel discriminators, the extracted TN distributions and threshold distributions for (a) AROM-1 B, and (b) AROM-1 C. The readout speed is 160 ns/2-rows.

AROM-1 E/F

The in-pixel discriminators of AROM-1 E/F were characterized with the 100 MHz clock, and the measurement results are shown in Fig. 5.17. From the extracted noise values given in table 5.5, it can be seen that the discriminator noise of AROM-1 E/F is significantly improved as compared to their ancestor, AROM-0 V1, in terms of both TN and FPN. The TN for the discriminators in AROM-1 E/F is about only 0.3 mV. As for the FPN, the AROM-1 E has a value of 0.16 mV, which is similar or even lower than that has been achieved by the much more complicated column-level discriminators [132]. The FPN value of the discriminators in AROM-1 F is about 0.3 mV, which is larger than that of AROM-1 E. Nevertheless, the discriminators in AROM-1 E/F both contribute marginally to the total noise of the full in-pixel circuitry, as compared to the sensing system.



(a)



(b)

Figure 5.17: "S" curves of the in-pixel discriminators, the extracted TN distributions and threshold distributions for (a) AROM-1 E, and (b) AROM-1 F. The readout speed is 160 ns/2-rows.

Table 5.5: Noise performance of in-pixel discriminator in AROM-1 E/F.

Chip version	TN (mV)	FPN (mV)	Total noise (mV)
AROM-1 E	0.29	0.16	0.33
AROM-1 F	0.31	0.29	0.42

5.4 Summary

This chapter began with the analysis of the temporal noise for AROM-0. It indicates that the noise performance of the pixel V1 in AROM-0 can be significantly improved, if slight modifications are made. And the pixel V2 in AROM-0 is also likely to achieve satisfactory noise performance if careful layout optimization is made and the sensing system is further optimized. Based on these two pixel versions in AROM-0, several modified pixels were integrated in the AROM-1 prototypes, which were manufactured by using a high-resistivity starting material. As compared to AROM-0, the AROM-1

chip includes a larger pixel array and more on-chip intelligence, approaching the final ASTRAL chip. The AROM-1 chip series is categorized into two groups. The former includes AROM-1 A/B/C, incorporating pixels derived from AROM-0 V2. The latter includes AROM-1 E/F, with pixels derived from AROM-0 V1.

These AROM-1 chips were characterized in laboratory. The measurements with an ^{55}Fe source indicate that the total signal charge is almost fully collected by a set of 4 pixels in a cluster, thanks to the high-resistivity epitaxial layer. The measured CVF is 56 μV/e$^-$ for the sensing system used in AROM-1 A/B/C and is 44 μV/e$^-$ for the sensing system in AROM-1 E/F. It is noted that the performance of the sensing system is still under optimization, which is out of the scope of this thesis.

Due to the limitation of the current data acquisition board, the digital characterization was performed with a 100 MHz clock, resulting in a read-out speed of 160 ns/2-rows. The measured ENC values of the AROM-1 B/C are about 24 e$^-$, which are better than their ancestor AROM-0 V2. The noise improvement is mainly attributed to the reduction of the RTS noise. The discriminator performance of these two chips are limited by the circuit topology and the total discriminator noise is about 1 mV. The highlight of the AROM-1 series comes from the in-pixel discriminators of AROM-1 E/F. The total noise voltage values for AROM-1 E and AROM-1 F are only 0.33 mV and 0.42 mV, respectively. The ENC values for AROM-1 E/F both exceed slightly 20 e$^-$, coming mainly from the sensing system.

Chapter 6

Summary and conclusions

The ALICE collaboration plans to upgrade its apparatus during the long shutdown of LHC in 2018/2019 in order to increase its physics capabilities. The proposed physics programs are motivated by new high-precision measurements on heavy flavour and low-mass dilepton production in heavy-ion collisions. These rely essentially on an upgraded Inner Tracking System (ITS) with significantly improved low-momentum tracking and vertexing capabilities.

CMOS pixel sensors, fabricated in a standard CMOS process, can provide a great balance between spatial resolution, read-out speed, radiation tolerance, material budget and power consumption. They are very attractive to the applications where measurements at low transverse momentum are crucial, thanks to their capabilities of high granularity and low material budget. The state-of-the-art ULTIMATE sensor, fabricated in a 0.35 μm CMOS process, has successfully equipped the STAR-PXL detector, which began to take physics data in early 2014. As compared to the STAR-PXL detector, the ALICE-ITS upgrade calls for some substantial improvements on the sensor performances, especially in terms of read-out speed and radiation tolerance. Therefore, a 0.18 μm CIS quadruple well process was assessed for CPS fabrication, in order to push forward the CPS potential to meet the challenges of the ALICE-ITS upgrade. This new process offers an epitaxial layer with a resistivity higher than 1 kΩ·cm and a gate oxide thickness below 4 nm, thus being more robust to radiation damages than the 0.35 μm technology. Another important feature of this technology is the possibility of using full CMOS inside the pixel by adding a special deep P-well to shield the N-well containing PMOS transistors. As a result, more intelligence can be integrated at the pixel level, potentially allowing for faster readout and less power consumption. By

exploiting this new process, the objective of this thesis is to develop a fast and power efficient CPS prototype, that could direct a full scale CPS design well adapted to the ALICE-ITS upgrade.

6.1 Work summary

In this thesis, the AROM sensors, incorporating the pixel-level discriminator, were prototyped as the forerunners of the ASTRAL sensor, which is the final sensor we have proposed for the ALICE-ITS upgrade. The study began with the AROM-0 chip, which includes various test structures to demonstrate the feasibility of in-pixel signal discrimination with small pixels (e.g., 22 μm $\times$ 33 μm) and to evaluate their performance. As compared to the column-level discrimination, the static current consumption per pixel can be reduced by at least a half with the AROM-0 pixels. The row processing time is also decreased from 200 ns/row to 100 ns/row. Laboratory test shows that all the three pixel versions function properly and have the ENC values of about 30 e^- for the full in-pixel circuitry. The discriminator alone contributes about 20 e^- of noise and has the noise voltage $\gtrsim$ 1 mV. The design issues of cross coupling in the layout and poorly biased MOS switches were analyzed and resolved in the next generation of prototype chips with the name of AROM-1. In addition, the sensing system was optimized for less RTS noise in AROM-1. These AROM-1 chips were fabricated by using a high-resistivity starting material ($>$ 1 kΩ·cm), and they are the intermediate prototypes towards the ASTRAL sensor. Two main purposes are addressed in AROM-1, one is to validate the optimization of the pixel designs and the other is to establish a scalable CPS architecture with necessary on-chip intelligence. Each AROM-1 chip contains a 64 $\times$ 64 pixel array, read out two rows by two rows. The reference DACs (Digital-to-Analog Converter) and the sequence generator are integrated at the chip periphery, all programmable with registers accessed via an embedded slow control JTAG interface. The AROM-1 series includes five chip versions, categorized into two groups: one includes AROM-1 A/B/C, with pixels derived from AROM-0 V2; and the other contains AROM-1 E/F, incorporating the pixels derived from AROM-0 V1. The different pixel versions in the same group are distinguished from each other by pixel pitch, as well as by device placement and signal routing in the pixel layout. These chips were measured in laboratory. Thanks to the high-resistivity starting material, higher charge collection efficiency than AROM-0 was observed. Another improvement, as compared

to the AROM-0, is the mitigation of RTS noise by using larger dimensions for the input transistors of the pre-amplifiers. As for the discriminator part, the AROM-1 E manifests a most promising discriminator design and has been chosen as the baseline for future development. The AROM-1 E is composed of pixels with the same pitch as that of AROM-0. Its discriminator inherited the topology of AROM-0 V1, and was optimized for low noise and low power. The total static current consumption is about 18 μA per pixel and is much less than that consumed by the pixels in AROM-0. The total discriminator noise of AROM-1 E is only 0.33 mV. The ENC value of the full in-pixel circuitry slightly exceeds 20 e^-, mainly contributed by the sensing system. The noise performance of all the AROM prototypes developed in this thesis is summarized in Appendix A.

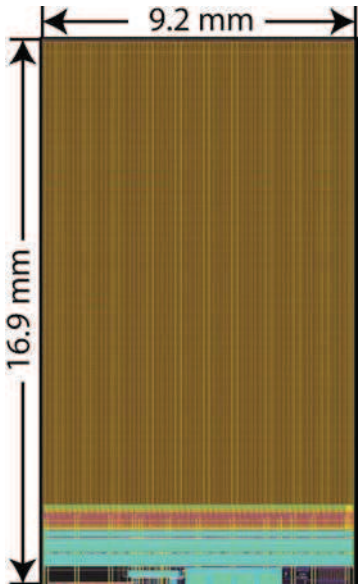


Figure 6.1: The layout of the FSBB-A0.

By extending the AROM-1 sensor to the full size pixel array and combining the zero-suppression logic, the FSBB-A0 sensor, which is the first prototype of the Full Scale Building Block for the ASTRAL sensor, was built. The FSBB-A0 sensor composes one third of the ASTRAL sensor. Fig. 6.1 gives the layout of the FSBB-A0, which has a chip area of 16.9 $\times$ 9.2 mm^2. The sensor utilizes the same pixel as the AROM-1 E. The active area is 13.7 $\times$ 9.2 mm^2, composed of a pixel array of 416 $\times$ 416. With the double-row rolling shutter readout, the integration time is about 20 μs. The SUZE-02 circuitry, including the zero-suppression logic and the output buffers, was integrated at the bottom of the pixel array. With a 160 MHz clock, the data flow at the two output

nodes is 320 Mbits/s for each. The chip was fabricated in early 2014. Unfortunately, due to the failure of the JTAG interface and the reference voltages, we were unable to characterize the FSBB-A0 properly. The reasons for the failure are still unraveled and have to be explored in the future beyond this thesis.

6.2 General conclusions and discussions

CMOS pixel sensors have been chosen to equip the ALICE-ITS upgrade and it will be the first time for CPS to equip a large area tracker ($\sim$ 10 m^2). The CPS with rolling shutter readout forms a mature sensor architecture, provided by its previous use in the STAR-PXL detector. By profiting from a more advanced CMOS process based on a 0.18 μm feature size, the signal discrimination, conventionally performed at the column level, can be implemented inside each pixel. In this way, the performance of the rolling shutter CPS can be greatly enhanced in terms of read-out speed and power consumption, meeting the requirements of the ALICE-ITS upgrade.

In this thesis, several prototypes of rolling shutter CMOS pixel sensors with in-pixel discrimination were developed. A promising in-pixel discriminator design, with a very low power consumption and excellent noise performance, was eventually achieved in the AROM-1 prototypes. Table 6.1 compares some selected discriminators among those prototyped.

Table 6.1: Performances of the discriminators in different chips.

Chip		Process (μm)	Static current (μA/discri.)	Avg. TN (mV)	FPN (mV)
AROM-1	E	0.18	15	0.3	0.2
	F		12	0.3	0.3
MIMOSA-22THRb		0.18	$\sim 70^a$	$\lesssim 0.4$	< 0.2
ULTIMATE		0.35	$\sim 70^a$	$\lesssim 0.4$	$\lesssim 0.3$

[a] $\sim$ 50 μA of additional current is needed for the analogue signal buffering in the pixel.

The chip MIMOSA-22THRb includes a series of prototypes in the 0.18 μm process, featuring a double-row rolling shutter readout and a column-level discrimination. The baseline discriminator design in these prototypes inherits the discriminator from the ULTIMATE sensor implemented in the STAR-PXL. As can be seen from the table, similar noise performances, as compared to the more complex column-level discriminators,

have been achieved with the AROM prototypes with much lower power consumption. However, large efforts, beyond this thesis, are still needed to verify the AROM concept in a large scale sensor (e.g. like ASTRAL).

The R&D of CMOS pixel sensors for the ALICE-ITS upgrade represents the frontier in the field of CPS design for charged particle detection. And it should be noted that the ASTRAL sensor is only one of several proposals for this application. Two other candidates, i.e. MISTRAL[1] and ALPIDE[2], are being developed in parallel. They feature different sensor architectures from ASTRAL. In the following sections, some discussions on the three development approaches are given.

6.2.1 The MISTRAL/ASTRAL development

The MISTRAL development employs the most mature CPS architecture: the rolling shutter readout with column level discrimination. It is derived from the ULTIMATE sensor, but two rows are read out at the same time to increase the read-out speed. As a result, two discriminators are required at each column end. The MISTRAL architecture only differs from the ASTRAL architecture in the discrimination stage. And the final MISTRAL sensor, proposed for the inner layers of the ALICE-ITS upgrade, will be optimized to achieve an integration time of about 30 μs, with an expected power consumption of $\sim$ 200 mW/cm^2 [112]. It should be noted that the MISTRAL sensor follows a conservative design strategy and will not be as fast and power efficient as the ASTRAL sensor, which features an integration time below 20 μs and a power consumption of $\sim$ 85 mW/cm^2. However, the MISTRAL development is based on a well established sensor architecture, and it has been validated on real scale via the FSBB-M0 sensor, which is a prototype of the full scale building block of the MISTRAL sensor. The FSBB-M0 contains a pixel array of 416 by 416, with pixel dimensions of 22 μm $\times$ 33 μm. The integration time is $\sim$ 40 μs. Beam tests, with 120 GeV negatively charged pions at SPS, showed a detection efficiency well above 99 %, with a fake hit rate below 10 $^{-5}$. The spatial resolution is about 4.5 μm [133, 134].

[1] MIMOSA Sensor for the inner TRacker of ALICE
[2] ALice PIxel DEtector

MISTRAL for the outer layers of the ALICE-ITS upgrade

Currently, large R&D efforts are focused on optimizing the MISTRAL architecture for the outer layers of the ALICE-ITS upgrade. Thanks to the relaxed spatial resolution requirement of the outer layers [16], an increased pixel area of 36×65 μ^2m was studied for MISTRAL. Such a pixel pitch will allow for a spatial resolution of ~ 10 μm, and an integration time of ~ 20 μs in the full scale sensor. The power consumption can also be reduced with the large pixel dimensions, and a power consumption below 100 mW/cm^2 is well achievable.

It is worth mentioning that the optimization of the power consumption for the MISTRAL sensor could benefit from the AROM development addressed in this thesis. In principle, the low-power in-pixel discriminator designs developed in this work can also be utilized for the column-level discrimination. However, for design safety, the current MISTRAL development still employs the well demonstrated discriminator design, which is the same as that from the MIMOSA-22THRb chip mentioned in table 6.1. In this PhD study, a new column-level discriminator circuit was designed for the MISTRAL development. It has a modest static current of ~ 40 μA, and the longitudinal dimension for two discriminators located at the same column end is reduced from 200 μm to 150 μm. This new discriminator circuit was integrated in a MIMOSA-22THRb prototype currently in fabrication, which will bridge the transition from the current conservative design to the aggressive AROM discriminator designs.

In order to reduce the fake hit rate, the final MISTRAL sensor is foreseen to include a pixel masking circuitry. It was observed that the fake hit rate could be improved by an order of magnitude by masking the 0.1 % noisiest pixels [134].

Pads over the pixel array

The current design strategy of the new ALICE-ITS detector involves implementing the interface pads over the sensor chip, so that the chip will be vertically interconnected with the flex PCB through laser soldering [134]. Each of these metal pads will cover an area of several pixels. Consequently, the top two metal layers in the pixel array should be reserved for the pad implementation, rather than for the capacitor and global signal routing. In this case, the MIM capacitors are prohibited in the pixel array, since their implementation requires the top two metal layers. In order to be compatible with this pad implementation, fully customized fringe capacitors, using the lowest two

metal layers, have been explored to replace the MIM capacitors for the MISTRAL development.

It should be noted that the AROM sensors developed in this work are still not compatible with the pads over the pixel array. The 1.8 V power supply leaves a limited voltage margin for the current AROM in-pixel circuitry to maintain a proper biasing ($\gtrsim$ 0.4mV) for MOS capacitors. As for the fringe capacitor, it has much less capacitance density than the currently used stacked MIM capacitor. Without increasing substantially the pixel pitch of the AROM sensor, using the fringe capacitor will result in an unaffordable capacitance loss.

Perspectives of the AROM sensor

Similarly to MISTRAL, the ASTRAL development could also profit from a relaxed spatial resolution requirement. With a large pixel pitch, e.g. 36 μm $\times$ 65 μm, the layout difficulties of the AROM pixels will be greatly alleviated. In addition, it will allow for more design flexibility. For example, the fringe capacitors, complying with the pads over the pixel array, could be used. As a result, an ASTRAL variant could be optimized for the outer layers of the new ALICE-ITS, achieving a power consumption below 60 mW/cm^2.

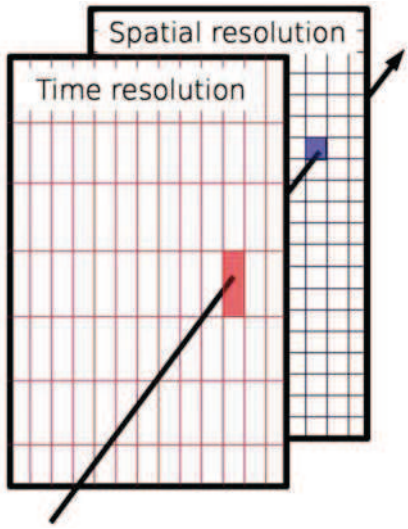


Figure 6.2: Illustration of a double-sided detector, with one side providing high spatial resolution and the other side providing time stamping.

It is also noted that the fast readout feature of the AROM sensor could benefit to the concept of a double-sided ladder, which consists of two CPS layers separated by

an ultra-light support structure. This ladder concept was developed by the PLUME[3] collaboration as a proof of principle for the ILD[4] vertex detector [135]. As illustrated in Fig. 6.2, a traversing particle produces two hits in the two sensor layers, which are optimized for different but complementary functionalities. One side of the ladder provides a high spatial resolution by using small pixels. Whereas the other side, aimed at a high time resolution, is equipped with elongated pixels for fast readout. The AROM sensor is particularly suitable for the latter. Unlike the MISTRAL architecture, where extra discriminators are required at the periphery when multiple rows are read out at the same time, the AROM sensor already has a discriminator exclusively serving for each pixel. And in principle, all the pixels in the AROM sensor could be read out in parallel. In practice, the read-out parallelism is limited by the power consumption constraint, by the available room in the layout to route the output channels, as well as by the capability of the downstream circuitry. By employing a more parallelized readout and optimizing the longitude dimension of the pixel, the AROM sensor may provide a time stamping in the μs level or even below.

6.2.2 The ALPIDE development

Besides the rolling shutter architecture, another CPS architecture with data-driven readout is being developed. This new read-out architecture of CPS is similar to that of the hybrid pixel detectors, thanks to the possibility of utilizing the full CMOS potential inside the pixels. The study of this CPS architecture is followed through the ALPIDE development [136, 137]. The in-pixel front-end electronics of the ALPIDE sensor is based on a current comparator circuit that works with a very low bias current, i.e. 20 nA. The integration time is defined by the pulse duration induced by a particle passage, which is about 4 μs. The in-matrix asynchronous priority encoder network generates directly the address of a hit pixel with the highest priority, and resets the storage element in the hit pixel once the digital periphery has read its address. The procedure is iterated until all hit pixels are read out. This sensor architecture allows for data sparsification at the time when the pixel array is read out. The read-out time, in this case, is proportional to the chip occupancy. With the multiplicities foreseen in the ALICE experiment, it is expected to have on average less than 1 hit/column, and

[3]PLUME stands for Pixelated Ladder with Ultra-Low Material Embedding

[4]International Large Detector a system of particle detectors which is being developed for the International Linear Collider (ILC)

the time needed to read out the full matrix is, on average, in the order of 10 μs, which is shorter than that of the rolling shutter CPS currently under development [138].

The performance of the low power front-end and the data-driven read-out circuitry was first investigated via the pALPIDE prototype, which has a pixel array of 512 rows by 64 columns with pixel dimensions of 22 μm $\times$ 22 μm. The measured average TN is about 7 e^- and the threshold dispersion is about 17 e^- standard deviation. The first full scale prototype, named pALPIDEfs, was then developed. It has overall dimensions of 30 mm $\times$ 15 mm and contains about 5 $\times$ 10^5 pixels of 28 μm $\times$ 28 μm. A detection efficiency of 99 % at a fake hit rate below 10^{-5} was measured. This result was obtained by masking the 20 noisiest pixels. The total power density of this prototype is 70 mW/cm^2, with the dominating contribution from the digital periphery. By implementing the low-power techniques, the targeted power density for the final prototype, excluding the off-chip data transmission, is about 30 mW/cm^2 [136,139,140]. The performance of the ALPIDE pixels is still under optimization and the most recent improvements on the ALPIDE pixel design include reducing the threshold dispersion by optimizing the front-end and using multi-event buffers inside the pixel in order to mitigate the dead time.

The achievements of ALPIDE have confirmed its architecture as a promising approach to build a fast CMOS pixel sensor with very low power consumption. However, due to the very low biasing current, all the transistors in the front-end operate in the sub-threshold region, which makes it difficult to control the behavior of the circuit, and the circuit performance is hardly predictable by simulation. In addition, the design margin of the front-end circuit is limited, and achieving a time resolution below the present one seems to be an arduous task. Another issue is the dead time generated by the matrix read-out procedure. Even though the dead time can be reduced by implementing multi-event in-pixel buffers, which conflicts with an improved spatial resolution, it is still questionable if the ALPIDE architecture is suitable to the environment with very high hit density.

6.2.3 Some perspectives for CPS

At the end of this thesis, it is noted that the CMOS pixel sensors haven't reached their full potential yet. They will keep gaining power from the evolutions in the CMOS technology, and will hopefully meet the extreme requirements driven both by the physics performances and by the running conditions of the next generation high energy physics

experiments. Following the ALICE-ITS upgrade, the next use of CMOS pixel sensors will be the Micro-Vertex Detector (MVD) of the Compressed Baryonic Matter (CBM) experiment at FAIR[5] [141]. And CMOS pixel sensors are also considered by other experiments like the ILD as one of the options for the vertexing and tracking subsystem [142]. Beyond the HEP experiments, CMOS pixel sensors are also drawing attentions from some other applications, like X-Ray detection and space dosimeter, where their added value is already established [143, 144]. Therefore, the development of CPS for a wide range of applications will steadily allow progresses in various research domains.

[5]Facility for Antiproton and Ion Research an international accelerator facility under construction for the research with antiprotons and ions.

Appendix A

Noise summary of the AROM prototypes

Table A.1: The AROM noise performance for the full in-pixel circuitry.

Chip version	Read-out speed	TN (mV)	FPN (mV)	Total noise (mV)	ENC (e^-)
AROM-0 V1	100 ns/row	1.43	0.66	1.57	30.2
	400 ns/row	1.66	0.34	1.69	32.5
AROM-0 V2	100 ns/row	1.55	0.49	1.62	28.4
	400 ns/row	1.70	0.58	1.79	31.4
AROM-0 V3	100 ns/row	5.77	2.50	6.29	32.5
	400 ns/row	6.70	1.83	6.95	35.9
AROM-0 V2 (2-row)	100 ns/2-rows	1.40	0.71	1.57	27.5
	400 ns/2-rows	1.67	0.67	1.80	31.6
AROM-1 A	160 ns/2-rows	−−	−−	−−	−−
	1.6 μs/2-rows	1.10	0.74	1.33	23.8
AROM-1 B	160 ns/2-rows	1.12	0.71	1.33	23.8
	1.6 μs/2-rows	1.16	0.61	1.31	23.4
AROM-1 C	160 ns/2-rows	1.14	0.67	1.32	23.6
	1.6 μs/2-rows	1.16	0.60	1.31	23.4
AROM-1 E	160 ns/2-rows	0.92	0.19	0.94	21.4
	1.6 μs/2-rows	−−	−−	−−	−−
AROM-1 F	160 ns/2-rows	0.92	0.31	0.97	22.0
	1.6 μs/2-rows	−−	−−	−−	−−

Table A.2: The AROM noise performance for the in-pixel discriminator.

Chip version	Read-out speed	TN (mV)	FPN (mV)	Total noise (mV)
AROM-0 V1	200 ns/row	1.03	0.60	1.19
	400 ns/row	0.97	0.25	1.00
AROM-0 V2	200 ns/row	0.81	0.65	1.04
	400 ns/row	0.85	0.41	0.95
AROM-0 V2 (2-row)	200 ns/2-rows	0.91	0.85	1.24
	400 ns/2-rows	0.85	0.55	1.01
AROM-1 B	160 ns/2-rows	0.78	0.62	1.00
	1.6 μs/2-rows	0.78	0.61	0.99
AROM-1 C	160 ns/2-rows	0.76	0.57	0.95
	1.6 μs/2-rows	0.79	0.58	0.98
AROM-1 E	160 ns/2-rows	0.29	0.16	0.33
	1.6 μs/2-rows	$--$	$--$	$--$
AROM-1 F	160 ns/2-rows	0.31	0.29	0.42
	1.6 μs/2-rows	$--$	$--$	$--$

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Développement des capteurs à pixels CMOS pour le nouveau trajectometre interne de l'expérience ALICE

Résumé

Ce travail contribue au programme de recherche et de développement d'un capteur CMOS à pixel qui pourrait satisfaire pleinement les spécifications du nouvel ITS (Inner Tracking System: trajectometre interne) de l'expérience ALICE. Afin de briser les limites de la CPS de pointe, une technologie CMOS 0.18 µm à quatre puits a été explorée. Les capteurs fabriqués dans cette nouvelle technologie ont montré une meilleure tolérance aux radiations que les capteurs réalisés dans une technologie CMOS 0.35 µm plus ancienne. En outre, cette nouvelle technologie offre la possibilité d'implémenter des transistors de type P dans chaque pixel sans dégrader la capacité de collection de la diode. Il devient donc possible d'intégrer un discriminateur dans chaque pixel et obtenir un pixel à sortie binaire. En conséquence, la consommation sera largement réduite. De plus, le temps de traitement de la ligne peut être potentiellement réduit. Un premier prototype de petite taille, intitulé AROM-0, a été conçu et fabriqué afin d'étudier la faisabilité de la discrimination de signal dans un petit pixel. Dans ce prototype, chaque pixel de surface 22 × 33 µm^2 contient une diode de détection, un préamplificateur et un discriminateur à tension d'offset compensée. La performance de bruit des différentes versions de pixels dans le capteur AROM-0 a été évaluée. Ensuite sera détaillé le développement des capteurs AROM-1. Ce sont les capteurs intermédiaires vers le capteur final proposé par notre group. Ils ont deux objectifs principaux, l'un est de valider les optimisations de conception du pixel et l'autre est de mettre en place une architecture du capteur évolutive intégrant l'intelligence nécessaire dans le circuit. Cette thèse présente en détail la conception et les résultats de mesure de ces capteurs AROM.

Mots-clés: ALICE, la mise à jour de l'ITS, les capteurs CMOS à pixel, détection de particules chargée, volet déroulant, discriminateur à l'intérieur du pixel

Résumé en anglais

This work is part of the R&D program aimed for a CMOS pixel sensor (CPS) complying with the requirements of the upgrade of the inner tracking system (ITS) of the ALICE experiment. In order break the limitations of the state-of-the-art CPS, a 0.18 µm quadruple-well CMOS process was explored. Besides an enhanced radiation tolerance, with respect to the former sensors fabricated in a 0.35 µm process, the sensor based on this new process allows for full CMOS capability inside the pixel without degradation of the detection efficiency. Therefore, the signal discrimination, which was formerly performed at the column level, can be integrated inside the pixel. As a result, the readout speed and power consumption can be greatly improved as compared to the CPS with column-level discrimination. This work addresses the feasibility study of achieving the signal discrimination within a small pixel (i.e. 22 × 33 µm^2), via the prototype named AROM-0. The pixel of AROM-0 contains a sensing diode, a pre-amplifier and an offset compensated discriminator. The noise performance of the various pixel versions implemented in AROM-0 was evaluated. The study was further pursued with the AROM-1 prototypes, incorporating the optimized pixel designs and the necessary on-chip intelligence to approach the final sensor we have proposed for the ALICE-ITS upgrade. This thesis presents in detail the design and the measurement results of these AROM sensors.

Keywords: ALICE, CMOS pixel sensor, charged particle detection, rolling shutter, in-pixel discriminator