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Laurent OSBERGER

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Etude de magnétomètres haute performance intégrés en technologie silicium

THÈSE dirigée par :

M. Vincent FRICK	Maître de conférences HDR, Université de Strasbourg, France

RAPPORTEURS :

M. Oliver PAUL	Professeur, Université Albert-Ludwigs, Freiburg, Allemagne
M. Thierry TARIS	Professeur, Institut Polytechnique INP de Bordeaux, France

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AUTRES MEMBRES DU JURY :

M. Laurent LATORRE	Professeur, POLYTECH Montpellier, France
M. Wilfried UHRING	Professeur, Université de Strasbourg, France

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Contents

Chapter 1

General introduction

Sensing is the entry point of any perception process. Now more than ever, this statement needs careful consideration. Indeed, with the ever-expanding amount of technological devices, perception is gradual shifting towards new paradigms of unprecedented amount and variety of information. From home to industry via health, transportation, security or environment, no domain sets apart from technological evolution. One blatant illustration of this context is the advent of the Internet of Things, which relies on ultra-low-power high-performance sensors to extract information from their physical environment in real-time. This evolution inevitably comes along with growing constraints, whether they be technical such as power consumption, accuracy, agility, reliability, compactness, or economic, and requires the developing of both new conception strategies and new devices with genuine breakthrough capabilities. This work addresses the points raised here. More specifically, this thesis is about high-performance integrated magnetic field sensors.

Integrated technologies probably constitute the most convenient way to co-integrate onto the same chip a sensitive element, usually called transducer, together with its conditioning electronics. This close, intrinsically intimate, combination enables the creating of smart sensors. Silicon-based technologies, and above all standard CMOS processes, are particularly well suited because they are mature, cost effective[1] , and offer great versatility, enhancing sensors with advanced signal processing and a large variety of complex functions, turning them into even smarter microsystems.

As an introduction to this thesis, the next two following sections report on magnetic sensors and transducers. Section 1.1 proposes a concise survey of representative state-of-the-art applications of integrated magnetic sensors. Section 1.2 then refocuses on the core element of any magnetic sensing system, i.e. the transducer that converts magnetic excitation into an electrical signal. The goal of this section is precisely to identify what principles are actually suitable for integration, particularly in silicon technology. The presentation of the motivations and objectives finally completes this general introduction and invites the reader to discover this work on silicon-based high-performance magnetic sensors.

[1] To some extent, considering large scale production volume.

1.1 Applications of magnetic field sensors

The demand for magnetic field sensor has been growing rapidly over the last decade [1]. Figure 1.1 illustrates the related market trend for north America. It shows that the global market has been almost linearly growing since 2012 and is dominated by Hall effect sensors. This trend is expected to consolidate in the next years due to emerging applications in all domains (consumer electronics, automotive, industry and health care...). In 2014, the magnetic field sensors market was evaluated of about USD 1.8 billion worldwide [2].

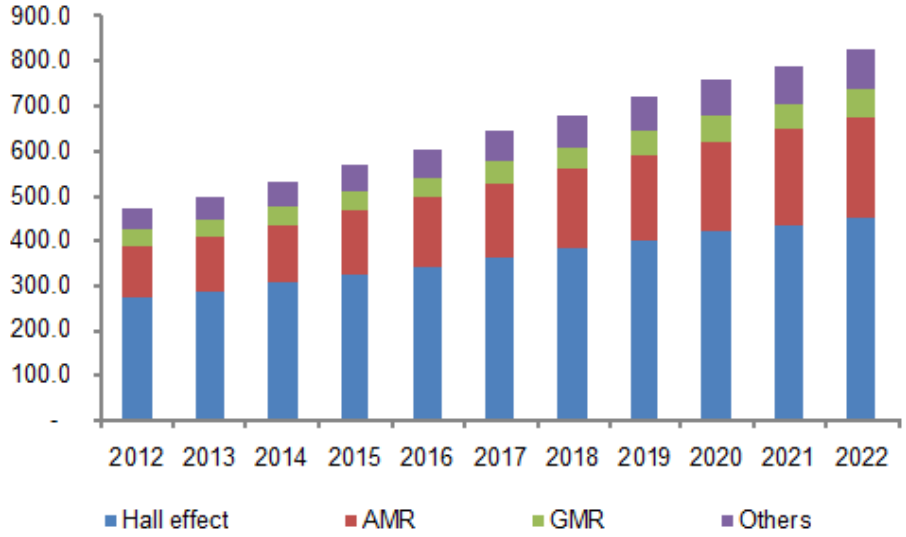
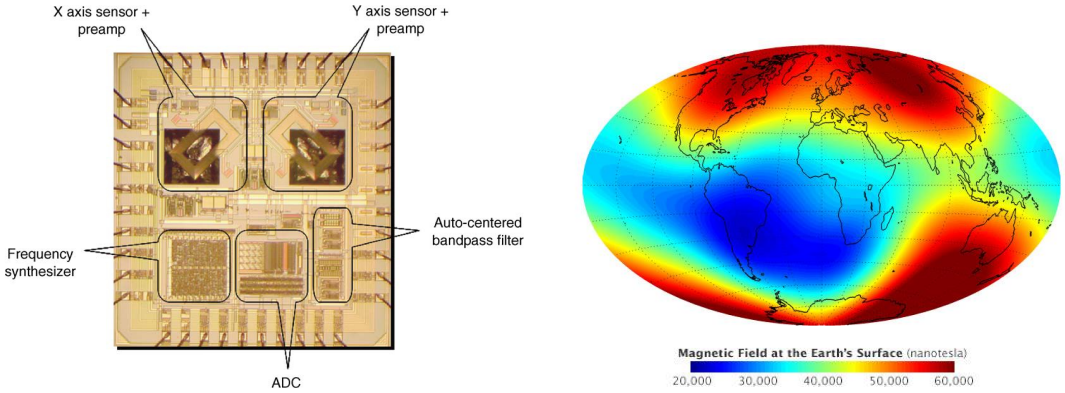


Figure 1.1 – North America magnetic sensors market by technology, 2012-2022, (USD Million). Reprinted from [2].

Of course, magnetic field sensors, also called magnetometers, can be used to provide direct measurement on the magnetic field itself. But most of the time, the magnetic field is an image or a consequence of other physical quantities such as mechanical displacement, electrical current... Magnetometers also represent promising approach in many bio-medical applications (immunoassay procedure [3, 4], micro-invasive surgery [5]).

1.1.1 Electronic compass

Electronic compass is a significant application of magnetic field sensors for consumer electronics (for example smartphones). It consists of a magnetometer with at least 2D capability (figure 1.2a), and accurate offset and gain calibration [6] that measures the horizontal component of the Earth's magnetic field in order to indicate the direction of the North pole. This application requires microtesla sensing capability since the Earth's horizontal magnetic field component is in the $20 - 60\,\mu T$ range (figure 1.2b).

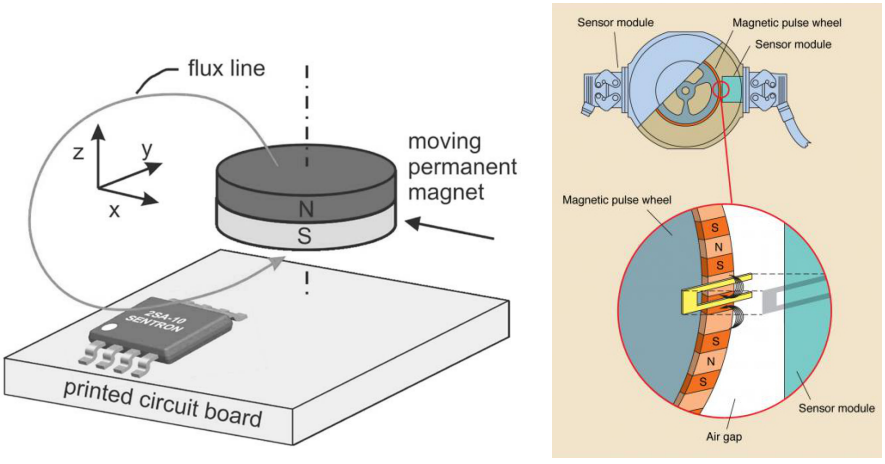


(a) (b)

Figure 1.2 – (a) 2D electronic compass based on resonant magnetic transducer, reprinted from [6], (b) Magnetic field at the Earth's surface, reprinted from [7].

1.1.2 Contactless linear and angular position sensors

Due to their massive use in automotive industry, displacement sensors probably constitute the largest application of magnetometers (rotary encoders, stirring wheels, active pedals, ...) [1]. Indeed, linear and angular position sensors consist of a magnetic field sensor combined to a permanent magnet (figure 1.3a) [8]. For example, the permanent magnet can be attached to a moving object such as a stirring wheel (figure 1.3b). In most position sensing applications, the magnetic field is in the micro to millitesla range.

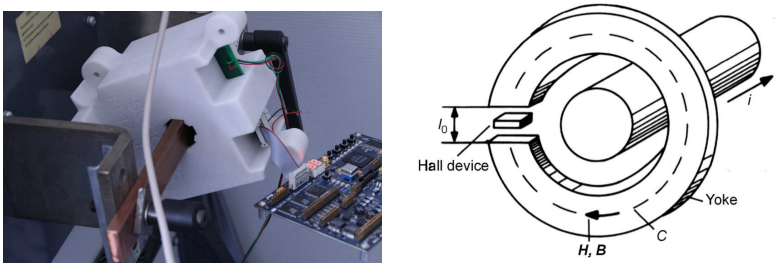


(a) (b)

Figure 1.3 – (a) linear position sensor, reprinted from [8] and (b) sensor system for stirring wheel, reprinted from [9].

1.1.3 Contactless current sensor

Contactless current sensor current sensors are based on the measurement of the magnetic field generated by an current flowing through a conductor [8]. The easiest way to perform this measurement is to place a magnetic field sensor close to the conductor [11]. The magnetometer can either be used as it is (figure 1.4a), or coupled to a ferromagnetic structure in



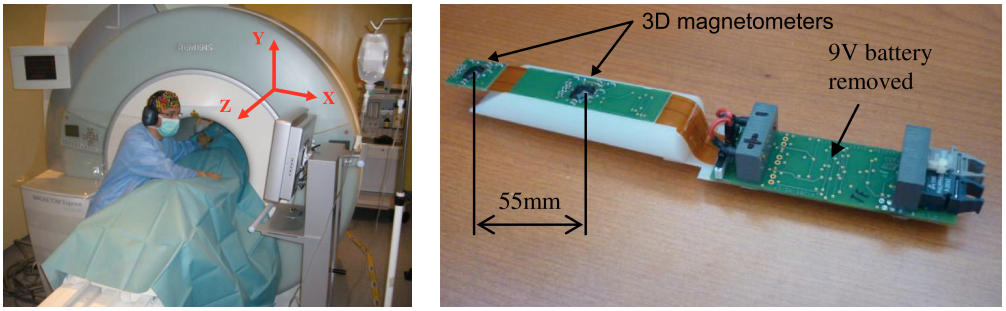
(a) (b)

Figure 1.4 – (a) Contactless current sensor, reprinted from [10], and (b) Hall device in magnetic yoke, reprinted from [8].

order to increase the magnetic flux density (figure 1.4b) [8, 11]. Depending on the sensor implementation and the amplitude of the current, this application requires magnetic field sensor resolution in the micro to millitesla range.

1.1.4 MRI surgical tool tracking

In MRI environment, high static magnetic field is applied together with magnetic gradients and radio-frequency electromagnetic stimulation in order to perform non-invasive imaging of living tissues [5]. There is a unique relationship between position within the MRI and the magnetic field gradients [5, 12, 13]. Attaching a micro-scale magnetometer to a surgical tool can thus be to assist micro-invasive surgery in MRI environment (figure 1.5). Two 3D magnetometers measure the gradients (i.e. around $20\,mT/m$) in order to provide high-accuracy on the tool's position [12]. This application requires magnetic field sensors able to achieve micro to millitesla range resolution within high static field (i.e. typically 1.5 or $3\,T$ for current clinical human MRI).



(a) (b)

Figure 1.5 – (a) MR-guided minimally-invasive surgery, (b) tracking device prototype. Reprinted from [5].

1.1.5 Magnetic microbeads detection

The magnetic microbeads detection is a promising approach in immunoassay procedure to provide low-cost and fast detection, for bio-medical analysis (tumor cells detection [14], DNA

analysis [15]...). Magnetic immunoassay procedure is illustrated in figure 1.6. The magnetic microbeads are functionalized with specific antibodies to ensure a biomolecular bonding with the analyte (antigens) [3, 4]. The substrate of the magnetometer is functionalized with antibody receptors that capture the analyte-bonded microbeads. Considering the close interaction between a single microbead and the magnetometer, this latter requires microtesla range resolution [16].

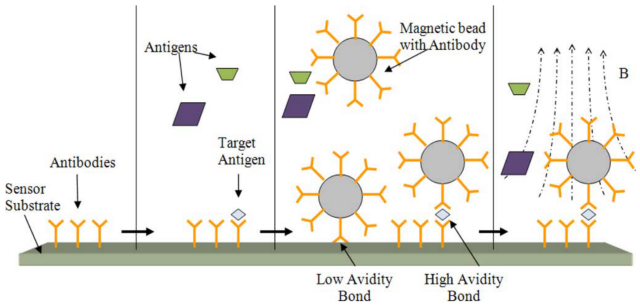


Figure 1.6 – Magnetic immunoassay procedure. Reprinted from [3].

1.2 Magnetic transducers

One should notice that most applications require vector magnetometers, which are able to measure the magnitude of the magnetic field along a specific axis. Their are many techniques and technologies to achieve vector magnetometers. There are presented in figure 1.7 and arranged as a function of the typical detectable magnetic field magnitude. Some of them can achieve very high accuracy (for example fluxgates and SQUIDs) while others cover wide range (inductive sensors). Unfortunately not all of them are suitable for integration (SQUIDs, inductive sensors...). This work addresses integrated magnetometers. Therefore, the following

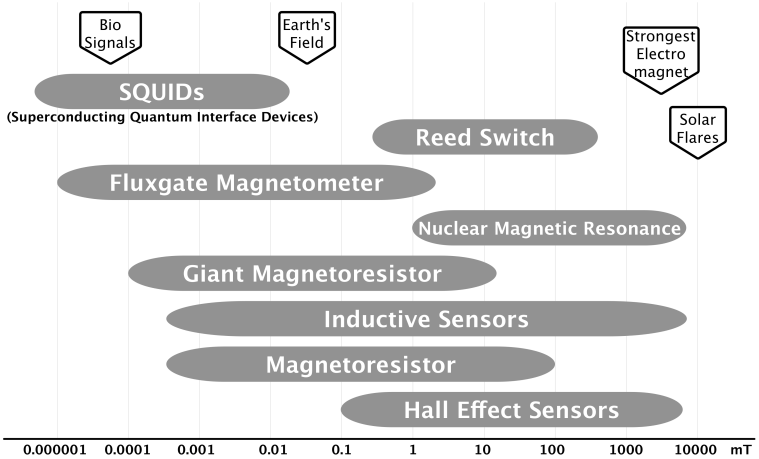


Figure 1.7 – Application range of the most prevalent magnetic field sensor. Reprinted from [17].

lines exclusively focus on transducers suitable for integration, i.e. magnetoresistor devices [18], fluxgates [19], Hall effect transducers, and other transducers based on the Lorentz force [8].

1.2.1 Giant magnetoresistors

In 2007, Albert Fert and Peter Grünberg received the Physics Nobel prize for the discovery of Giant MagnetoResistor (GMR) [20]. These transducers, also called spin-valves, are typically based on a four layers structure consisting of two ferromagnetic materials separated by a conductor, and an antiferromagnetic (AF) material layer (figure 1.8a). Simultaneous and parallel magnetization of both ferromagnetic layers changes the resistance of the device [1]. These transducers are able measure magnetic fields as low as $10\,nT$ and up to $1\,T$ (static to $10\,MHz$) [8, 21, 1]. They are suitable with integrated technologies by post-process layer deposition (figure 1.8b) [22, 23]. Unfortunately, GMR transducers are highly non-linear. Furthermore, exposure to high magnetic field can lead to irreversible damages of the pinned ferromagnetic layer [8]. One should also notice that, at lower frequency, GMR transducers suffer from 1/f noise issue (cf. section 3.3.1.3), which dramatically degrades their resolution [8, 23].

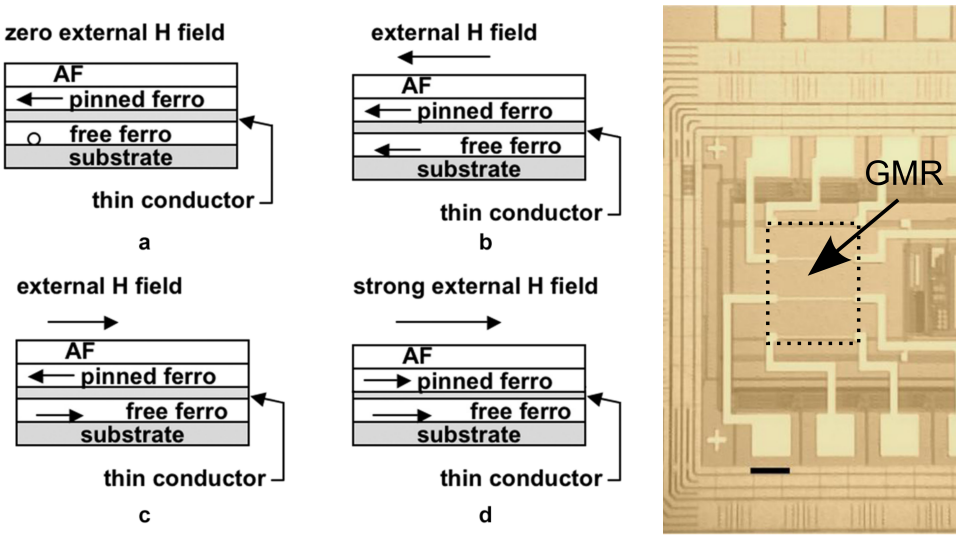
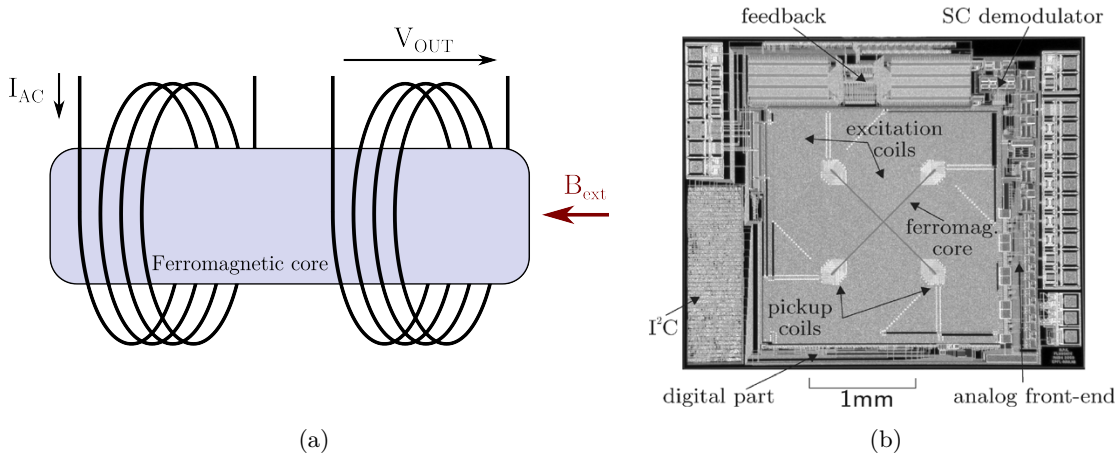


Figure 1.8 – (a) GMR structure with magnetization orientation, reprinted from [1]. (b) GMR deposition on AMS $0.35\,\mu m$ standard CMOS die, adapted from [23].

1.2.2 Fluxgate transducers

Figure 1.9a presents the typical structure of a fluxgate transducer. It consists of a ferromagnetic core surrounded by two coils. The magnetic material is periodically saturated by means of an excitation current flowing through the first coil. The second coil is used to pick up the voltage induced by magnetization variation in presence of an external magnetic field. Fluxgates transducers have been integrated on standard CMOS processes with additional post-processing steps (figure 1.9b) [1, 21]. They can measure magnetic fields in the nano to millitesla range. Nevertheless, their bandwidth is limited by the frequency of the excitation current (i.e. typically around $10\,kHz$) [1]. Moreover, they are liable to saturate at high-magnetic field because of the ferromagnetic core. Another drawback of fluxgate transducers



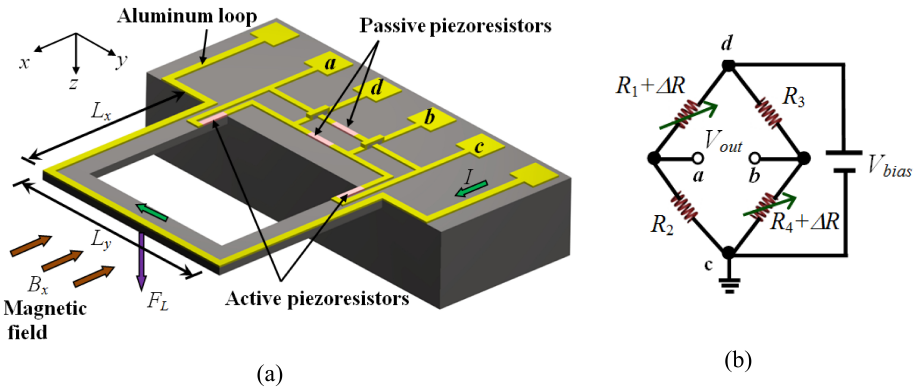
(a) (b)

Figure 1.9 – (a) Basic fluxgate principle. Redrawn from [21]. (b) Picture of an integrated 2-D fluxgate magnetometer [19].

is the degradation of their performances with core miniaturization. Therefore, their size is in the millimeter range, which can be an issue for spatial resolution and leads to high power consumption (high excitation coil current) [19, 21].

1.2.3 Resonant magnetic transducers

Resonant magnetic field transducers exploit the Lorentz force on vibrating mechanical structures. The magnetic signal amplifies the resonance. The mechanical deflection can be measured with either piezoresistive (figure 1.10), capacitive or optical techniques [24, 25]. These



(a) (b)

Figure 1.10 – (a) Schematic view of a resonant magnetic field sensor based on two U-shaped clamped-free microbeams and (b) its associated Wheatstone bridge. Reprinted from [24].

transducers are based on MEMS[2] technologies, some of which are compatible with CMOS process. For instance, a micro-beam can be fabricated with bulk micromachining [24]. These transducers can detect magnetic field up to $1\,T$ with a resolution in the nanotesla range [21]. The main issue MEMS-based magnetic transducers is their resonance frequency dependency

[2]MEMS: Micro-Electro-Mechanical System.

upon mechanical stress, temperature and pressure... Therefore, they require electronic compensation to ensure effective operation [21].

1.2.4 Hall effect transducers

The principle of Hall effect transducers is presented in section 2.1.1. Hall effect transducers probably have the lowest intrinsic performances of all integrated magnetic transducers. However, their performances can be dramatically improved by using dedicated signal processing techniques and conditioning electronics. One approach, consists in building hybrid Hall sensors, by combining transducers based on high-mobility semiconductors (i.e. In/Sb, In/Sa or GaAs) with silicon-based conditioning electronics on the same package [26]. It is also possible to apply post-processing in order to deposit magnetic flux concentrators that further increase their sensitivity [8, 27]. These hybrid-sensors achieve resolution in the nanotesla range at the expense of microsystem cost [21]. Another much more interesting solution consists in developing silicon Hall effect transducers because they can be co-integrated with their dedicated electronics onto the same substrate without any additional fabrication step, for instance in standard CMOS process. Silicon Hall effect transducers can detect magnetic fields up to $1\,T$ with microtesla range resolution (static up to $1\,MHz$).

Conventional Hall effect transducers sens magnetic fields in one dimension only. MEMS technology-based solutions have been proposed to implement 3D capability (figure 1.11) [28, 29]. MEMS technologies are yet not the only possibilities to achieve 3D Hall effect transducers (cf. section 4.1.2).

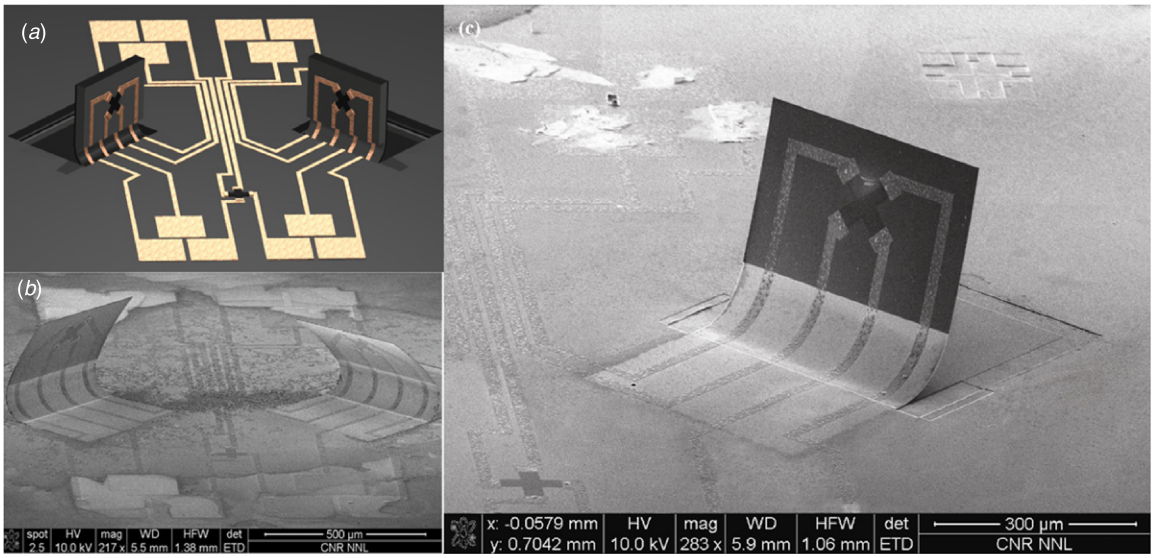


Figure 1.11 – (a) schematic view, (b) micrograph, and (c) close-up of both in-plane and out-of-plane Hall transducers. Reprinted from [28].

1.3 Thesis motivation and objectives

Silicon Hall sensors have been extensively studied in the last decades [30, 31, 32, 33]. Current modern magnetic field smart sensors provide advanced function such as auto calibration [34], temperature effects compensation [35], offset and low-frequency noise cancellation [32, 36]... Still, there is still plenty of room for improvement to push their limits and open to new applications.

In this thesis, we focus on magnetic transducers developed in low-cost low-power standard CMOS process. The optimizing of such post-processing-free silicon transducers is limited by the physical properties of the semiconductor itself (band structure, mobility...) and by the technological characteristics (doping concentration, well depth, design rules, geometry...). This requires accurate knowledge of the transducer's physical behavior and appropriate modeling in order to develop perfect match with its dedicated conditioning electronics.

In light of this purpose, the motivation of this thesis work is to explore two transducers with unexploited potential: the Low-Voltage Vertical Hall Device and a magneto-transistor called CHOPFET. We aim at pushing their limits in terms of resolution, offset and power consumption. Three levels of abstraction are considered:

- the transducer, its physics, model and optimization, the conditioning electronics and the system.
- the conditioning electronics dedicated to achieve optimal transducer operation
- the system consisting of the magnetic front-end and advanced signal processing.

This thesis is structured around three parts. The first part addresses the basics and state of the art of silicon magnetic sensors from the physics, to the transducer and its conditioning electronics. The two following parts, presents respectively the investigations dedicated to the Low-Voltage Vertical Hall Device and to the CHOPFET.

Part I

Silicon magnetic sensors: Basics and state of the art

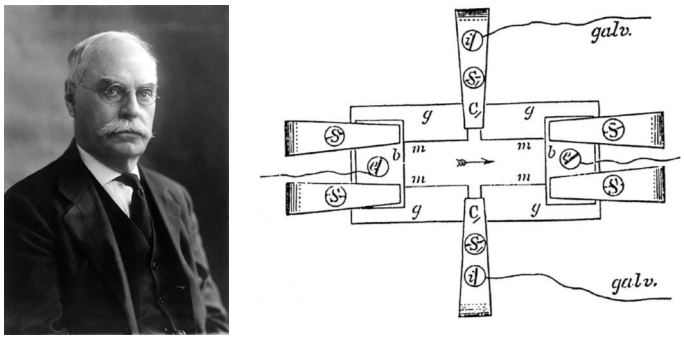
Chapter 2

Galvanomagnetic effect

Magnetic field transducer operation is based on the phenomena called galvanomagnetic effects, which are physical effects acting on electric current in the presence of a magnetic field. In the context of integrated magnetic transducers, Hall, current deflection, and magnetoresistance are the most significant effects. They are presented in the following sections.

2.1 Basic approach

2.1.1 Hall effect



(a) (b)

Figure 2.1 – (a) Edwin Herbert Hall 1855-1938. This photograph was taken around 40 years after the discovery of the Hall effect (reprinted from [37]). (b) Schematic of the very first Hall plate, the experimental device Mr Hall discovered the effect with. (Reprinted from [**?**]).

The Hall effect was discovered by American physicist Edwin Herbert Hall in 1879 (figure 2.1a). He proved that a magnetic field directly affects the current itself and not the wire bearing it as was first believed according to Maxwell's theory. Figure 2.1b) shows the original experiment conducted in 1819 [**?**]. A gold sheet biased with a fixed current was mounted on a glass plate and a galvanometer was connected across it at two nearly equipotential points. Hall highlighted that a transverse voltage appears when a magnetic field perpendicular to surface of the sheet is applied. This voltage has been known as the Hall voltage ever since.

Even though the Hall effect was first brought out on a sheet of metal, it appears on any conducting material exposed to a magnetic field[1]. In this study we will exclusively concentrate on semiconductor materials.

2.1.1.1 Lorentz force

Considering an infinitely long non-degenerated semiconductor plate with uniform doping, in presence of an electric field $\mathbf{E_e}$, the electric carriers are under the effect of an electrostatic force given by [38]:

$$\mathbf{F_e} = e \cdot \mathbf{E_e} \tag{2.1.1}$$

Here, e denotes the charge of a particle: for the electrons $e = -q$ and for holes $e = q$, where q is the elementary charge equal to $1.6 \cdot 10^{19}\, C$. This force leads to an electric current with the same direction as the electric field $\mathbf{E_e}$.

In presence of a magnetic field $\mathbf{B}$ a new force called magnetic force or Lorentz force appears [38]. It is given by:

$$\mathbf{F_m} = e\,(\mathbf{v_n} \times \mathbf{B}) \tag{2.1.2}$$

where $\mathbf{v_n}$ is the electron velocity vector. The direction of $\mathbf{F_m}$ is orthogonal to the electron displacement.

When both electric and magnetic fields are present, the total force, called electromagnetic force or Laplace force, is given by:

$$\mathbf{F_L} = e\,(\mathbf{E_e} + \mathbf{v_n} \times \mathbf{B}) \tag{2.1.3}$$

As illustrated in figure 2.2, the carriers trajectory is affected by the magnetic field, thus the displacement is no longer parallel to the electric field $\mathbf{E_e}$.

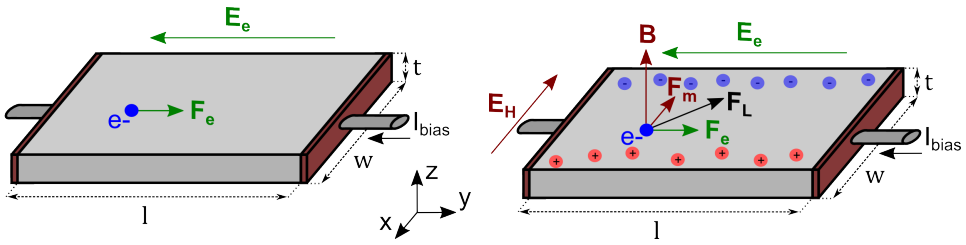


Figure 2.2 – (a) An electric field $\mathbf{E_e}$ is applied to a n-type plate. (b) An electric field $\mathbf{E_e}$ is applied concurrently with a magnetic field $\mathbf{B}$ to a a n-type plate: appearance of the Hall effect.

Considering an n-type plate, the expression of the the electron velocity vector $\mathbf{v_n}$ is given by [8]:

$$\mathbf{v_n} = \frac{\tau}{m^*} \cdot \mathbf{F_L} = -\frac{q \cdot \tau}{m^*} \cdot \mathbf{E_e} - \frac{q \cdot \tau}{m^*} \cdot (\mathbf{v_n} \times \mathbf{B}) \tag{2.1.4}$$

[1] including the human body!

where τ is the free transit time, i.e. the average time between two electron collisions with the crystal lattice, m^* is the effective electron weight. By solving equation 2.1.4 (cf Appendix B.1), the velocity vector $\mathbf{v_n}$ can be expressed according to the electric field $\mathbf{E_e}$ and to the magnetic field $\mathbf{B}$:

$$\mathbf{v_n} = \frac{-\frac{q\cdot\tau}{m^*}\cdot\mathbf{E_e} + \left(\frac{q\cdot\tau}{m^*}\right)^2\cdot\mathbf{E_e}\times\mathbf{B} - \left(\frac{q\cdot\tau}{m^*}\right)^3\cdot(\mathbf{E_e}\cdot\mathbf{B})\cdot\mathbf{B}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot\mathbf{B}^2} \tag{2.1.5}$$

Unlike to the free transit time, the charge carrier's effective mass does not vary significantly with the energy. Therefore we consider the mean free transit time $\langle\tau\rangle$ as a function of the energy E. This value is also called energy-weighted average free transit time [8] and is given by:

$$\langle\tau\rangle = \frac{\int_{E_C}^{E_{top}}\tau(E)\cdot E\cdot g(E)\cdot F(E)\,dE}{\int_{E_C}^{E_{top}} E\cdot g(E)\cdot F(E)\,dE} \tag{2.1.6}$$

Here, the angular brackets denote the energy-weighted average, $\tau(E)$ is the energy-dependent free transit time, $g(E)$ is the energy-dependent density of state, $F(E)$ is the energy-dependent distribution function. The integration is done over the conduction band.

The energy weighted average velocity vector can be written as

$$\begin{aligned}\langle\mathbf{v_n}\rangle = & -\left\langle\frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot\mathbf{E_e} + \left\langle\frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot\mathbf{E_e}\times\mathbf{B} \\ & -\left\langle\frac{\left(\frac{q\cdot\tau}{m^*}\right)^3}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot(\mathbf{E_e}\cdot\mathbf{B})\cdot\mathbf{B}\end{aligned} \tag{2.1.7}$$

The term $q\cdot\tau/m^*$ is consistent with the electron mobility μ_n, whose typical value for the n-well, for example in a standard $0.35\,\mu m$ CMOS process, is $1000\,cm^2.V^{-1}.s^{-1}$ [39]. Thus equation (2.1.7) can be simplified under the condition: $\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2 \ll 1$, which corresponds to:

$$B \ll \frac{m^*}{q\cdot\tau} = 2.89\,T \tag{2.1.8}$$

Equation 2.1.7 then becomes (cf Appendix B.1):

$$\langle\mathbf{v_n}\rangle = -\frac{q}{m^*}\cdot\langle\tau\rangle\cdot\mathbf{E_e} + \left(\frac{q}{m^*}\right)^2\cdot\left\langle\tau^2\right\rangle\cdot\mathbf{E_e}\times\mathbf{B} - \left(\frac{q\cdot}{m^*}\right)^3\cdot\left\langle\tau^3\right\rangle\cdot(\mathbf{E_e}\cdot\mathbf{B})\cdot\mathbf{B} \tag{2.1.9}$$

Note that this simplification makes sens for most silicon-transducer-based applications where the magnetic field is typically in the $100\,mT$ range. Yet, as will be discussed later (section 2.2.2), equation 2.1.7 should be consider for higher magnetic field operation condition (i.e. $B > 2.89\,T$).

The current density flowing in the plate is thus $\boldsymbol{J_n} = -n\cdot q\cdot\langle\mathbf{v_n}\rangle$, such as:

$$\begin{aligned}\boldsymbol{J_n} = & \; n\cdot q\cdot\Big(\frac{q}{m^*}\cdot\langle\tau\rangle\cdot\mathbf{E_e} - \left(\frac{q}{m^*}\right)^2\cdot\langle\tau^2\rangle\cdot\mathbf{E_e}\times\mathbf{B} \\ & + \left(\frac{q\cdot}{m^*}\right)^3\cdot\langle\tau^3\rangle\cdot(\mathbf{E_e}\cdot\mathbf{B})\cdot\mathbf{B}\Big)\end{aligned} \tag{2.1.10}$$

where n denotes the electron density. Assuming an n-type semiconductor, the hole current density $\boldsymbol{J_p}$ can be neglected compared to the electron current density $\boldsymbol{J_n}$. Consequently, the total current density $\boldsymbol{J}$ is assumed to be equal to $\boldsymbol{J_n}$. By reversing equation (2.1.10), a new expression of the electric field is obtained [8]:

$$\mathbf{E_e} = \frac{\boldsymbol{J}}{\sigma_n} - R_H \cdot \mathbf{J} \times \mathbf{B} + P_H \cdot (\mathbf{J} \cdot \mathbf{B}) \cdot \mathbf{B} \tag{2.1.11}$$

which can also be expressed with:

$$\sigma_n = n \cdot q \cdot \frac{q}{m^*} \cdot \langle \tau \rangle = n \cdot q \cdot \mu_n^* \tag{2.1.12}$$

$$R_H = -\frac{\frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2}}{n \cdot q} \tag{2.1.13}$$

$$P_H = \frac{\mu_n^*}{n \cdot q} \left(\frac{\langle \tau^2 \rangle^2}{\langle \tau \rangle^4} - \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \right) \tag{2.1.14}$$

Here, σ_n is the electric conductivity, $\mu_n^* = {}^{q}/_{m^*} \cdot \langle \tau \rangle$ is the energy-weighted equivalent mobility, R_H is the Hall coefficient and P_H is the planar Hall coefficient.

The presence of the magnetic field $\mathbf{B}$ diverts the current lines, which are no more parallel to the electric field $\mathbf{E_e}$. On the example of figure 2.2, the electric field E_e is along y-axis. This implies that, except the two faces parallel to the (Oxz) plane, all faces are in high impedance ($\boldsymbol{J_x} = \boldsymbol{J_z} = 0$). Given these conditions, equation (2.1.11) can be developed along each axis and leads to following equations:

$$E_x = -R_H \cdot J_y \cdot B_z + P_H \cdot J_y \cdot B_x \cdot B_y \tag{2.1.15}$$

$$E_y = \frac{J_y}{\sigma_n} + P_H \cdot J_y \cdot B_y^2 \tag{2.1.16}$$

$$E_z = R_H \cdot J_y \cdot B_x + P_H \cdot J_y \cdot B_y \cdot B_z \tag{2.1.17}$$

2.1.1.2 Hall voltage

The electric field component E_x, E_y, E_z leads to an equivalent voltage, which is obtained by integration over the respective axis:

$$V_x = -E_x \cdot w = \frac{R_H}{t} \cdot I_y \cdot B_z - \frac{P_H}{t} \cdot I_y \cdot B_x \cdot B_y \tag{2.1.18}$$

$$V_y = -E_y \cdot l = -\frac{l}{w \cdot t \cdot \sigma_n} \cdot I_y - \frac{l \cdot P_H}{w \cdot t} \cdot I_y \cdot B_y^2 \tag{2.1.19}$$

$$V_z = -E_z \cdot t = -\frac{R_H}{w} \cdot I_y \cdot B_x - \frac{P_H}{w} \cdot I_y \cdot B_y \cdot B_z \tag{2.1.20}$$

Let's now assume that the magnetic field is oriented along z-axis, which is perpendicular to plate surface. Therefore, $\mathbf{B} = B_z \cdot \boldsymbol{e_z}$. In this case, equations (2.1.18), (2.1.19) and (2.1.20) becomes:

$$V_x = \frac{R_H}{t} \cdot I_y \cdot B_z \tag{2.1.21}$$

$$V_y = -\frac{l}{w \cdot t \cdot \sigma_n} \cdot I_y \tag{2.1.22}$$

$$V_z = 0 \tag{2.1.23}$$

A new voltage, called the Hall voltage, appears along the x-axis. It varies linearly with the magnetic field B_z and the biasing current I_y:

$$V_H = V_x = \frac{R_H}{t} \cdot I_y \cdot B_z = \frac{\frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2}}{n \cdot q \cdot t} \cdot I_y \cdot B_z = \frac{r_H}{n \cdot q \cdot t} \cdot I_y \cdot B_z \tag{2.1.24}$$

where the Hall scattering factor r_H , is around 1.15 for silicon at room temperature [38]. Note that V_H only appears when the measurement faces are kept to high impedance. A phenomenological description will help understand this phenomenon.

When a magnetic field is applied along z-axis, the electrons are deflected by the magnetic force to the rear side (figure 2.2). As a consequence, the electron density is higher on the rear face compared to the front face on which the hole density is higher. This carrier imbalance induces a new transverse electric field $\boldsymbol{E_H}$, called the Hall electric field, which in turn leads to a new electrostatic force $\mathbf{F_H}$ called the Hall force and given by: $\mathbf{F_H} = e \cdot \mathbf{E_H}$. This force is opposite to the magnetic force $\boldsymbol{F_m}$ and restores the carrier displacement along y-axis. Furthermore, since the plate is considered as infinitely long, and when condition 2.1.8 is fulfilled , the magnetoresistance effects can be neglected. As can be noticed, in equation (2.1.21), the voltage across the plate in the y-axis is thus only described by Ohm's law. The voltage along the z-axis is equal to zero.

2.1.1.3 Hall angle

In presence of a magnetic induction, the total electric field $\boldsymbol{E}$ given in equation 2.1.11 is not collinear with the external electric field $\boldsymbol{E_e}$.

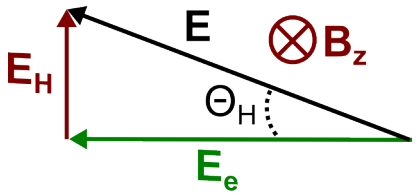


Figure 2.3 – The vector diagrams of electric field and current density.

According to figure 2.3, the Hall angle θ_H, defined as the angle of inclination of the current

density $\boldsymbol{J}$ with respect to the total electric field $\boldsymbol{E}$, is given by:

$$\tan\theta_H = \frac{|\boldsymbol{E_H}|}{|\boldsymbol{E_e}|} \tag{2.1.25}$$

According to the previous equations, the Hall angle can be expressed as:

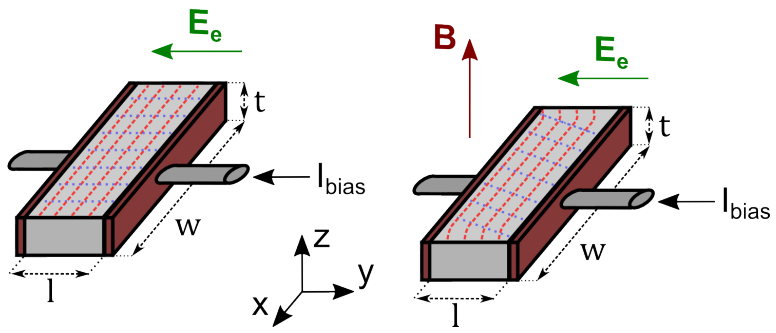
$$\theta_H = \arctan\left(\mu_H \cdot B_z\right) \tag{2.1.26}$$

The value of the Hall angle only depends on the magnetic induction and the Hall mobility $\mu_H = r_H \cdot \mu$. With r_H is the Hall scattering factor linked to the dispersion of the relaxation time and μ the mobility of the carriers.

2.1.2 Current deflection effect

The second galvanomagnetic manifestation is called current deflection. Rewriting equation 2.1.10 highlights the quantitative relation between the electric field and the current density:

$$\boldsymbol{J_n}(\mathbf{B}) = n \cdot q \cdot \mu_n \cdot \mathbf{E_e} - n \cdot q \cdot \mu_n^2 \cdot \frac{\langle\tau^2\rangle}{\langle\tau\rangle^2} \cdot (\mathbf{E_e} \times \mathbf{B}) + n \cdot q \cdot \mu_n^3 \cdot \frac{\langle\tau^3\rangle}{\langle\tau\rangle^3} \cdot (\mathbf{E_e} \cdot \mathbf{B}) \cdot \mathbf{B} \tag{2.1.27}$$



(a) (b)

Figure 2.4 – Short Hall plate, (a) without magnetic induction, (b) with magnetic induction. The current density lines are sketched in blue lines. The equipotential are sketched in red lines.

We shall again suppose the magnetic induction is oriented along z-axis (figure 2.2). Thus equation 2.1.27 can be simplified as:

$$\begin{aligned} \boldsymbol{J_n}(\mathbf{B}) &= n \cdot q \cdot \mu_n \cdot \mathbf{E_e} - n \cdot q \cdot \mu_n^2 \cdot \frac{\langle\tau^2\rangle}{\langle\tau\rangle^2} \cdot (\mathbf{E_e} \times \mathbf{B}) \\ &= \boldsymbol{J_n}(\mathbf{0}) - K \cdot (\mathbf{E_e} \times \mathbf{B}) \end{aligned} \tag{2.1.28}$$

Here, $\boldsymbol{J_n}(\mathbf{0}) = n \cdot q \cdot \mu_n \cdot \mathbf{E_e}$ is the drift current density for $B = 0$, K is given by $K = n \cdot q \cdot \mu_n^2 \cdot \langle\tau^2\rangle/\langle\tau\rangle^2$.

Figure 2.4 illustrates the current deflection effect on a very short Hall plate. The distance between the contacts is much smaller than the plate's width. In this case, the isolated boundaries, where the charge could accumulate, are very small. Therefore, the Hall effect that

counterbalances the charge deflection in a long plate, cannot settle. The Hall field, which is short-circuited by the large contacts, is thus negligible.

2.1.3 Geometrical magnetoresistance effect

The third galvanomagnetic effect is the geometrical magnetoresistance. This phenomenon occurs in short Hall plates and is directly linked to the the current deflection. According to equation 2.1.28, the current density is smaller in presence of a magnetic field. As a consequence, the current density lines are longer and the effective resistivity of the plate increases. Since this effect is a consequence of the geometrical change of the current lines, it is thus called the geometrical magnetoresistance effect.

2.2 Secondary effects

This section presents second order phenomena related to the galvanomagnetic effects.

2.2.1 Planar Hall effect

A "new" galvanomagnetic effect was reported by Goldberg and Davis in 1954 [40]. It is called planar Hall effect and occurs when the magnetic field is not purely along z-axis. It was first observed by measuring the induced voltage normal to the direction of the current flow but this effect can actually be observed in any direction. Considering the Hall plate presented in figure 2.2, equation 2.1.18 can be rewritten as a general expression of the Hall voltage:

$$\begin{aligned} V_x &= \frac{r_H}{n \cdot q \cdot t} \cdot I_y \cdot B_z - \frac{\mu_n^* \left(\frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} - \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \right)}{n \cdot q \cdot t} \cdot I_y \cdot B_x \cdot B_y \\ &= V_H\left(B_z\right) + V_{Pl}\left(B_x,\, B_y\right) \end{aligned} \tag{2.2.1}$$

where V_{Pl} denotes the planar Hall voltage.

The planar Hall effect is due to the mean free transit time, which depends on the electron's energy. Strictly speaking, equation 2.2.1 is considered as an approximation because of the anisotropic characteristics of silicon. It has been shown that V_{Pl} is minimal for a n-type Hall plate on a (100) direction wafer, with current flowing along (100) direction [41].

According to Schott et al. [42], for a standard Hall plate in CMOS process (100 wafer), at $B = 2\,T$ the ratio V_{Pl}/V_H is equal to 8.1 %. The significantly high value of V_{Pl} can have deleterious impact the magnetic induction measurement. Hopefully, it can be easily removed by applying appropriate signal processing techniques presented in section 4.2.1.2. Thus it is generally not considered when designing Hall-plate-based systems.

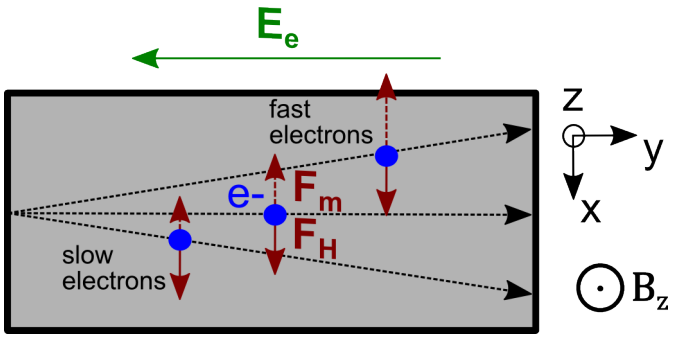


Figure 2.5 – Physical magnetoresistance effect on n-type Hall plate.

2.2.2 Physical magnetoresistance effect

The physical magnetoresistance effect also directly results from the carrier's mean free transit time depending on their energy. To highlight this phenomenon we shall reconsider equations 2.1.12, 2.1.13 and 2.1.14, i.e. $B > 2.89\,T$. At first order, the expressions of the electric conductivity, the Hall coefficient and the planar Hall coefficient become:

$$\sigma_n = n \cdot q \cdot \mu_n^* \cdot \left(1 + \mu_n^{*2} \cdot \left(\frac{\langle\tau^2\rangle^2}{\langle\tau\rangle^4} - \frac{\langle\tau^3\rangle}{\langle\tau\rangle^3}\right) \cdot B^2\right) \tag{2.2.2}$$

$$R_H = \frac{\frac{\langle\tau^2\rangle}{\langle\tau\rangle^2}}{n \cdot q} \cdot \left(1 - \mu_n^{*2} \cdot \left(\frac{\langle\tau^4\rangle}{\langle\tau^2\rangle \cdot \langle\tau\rangle^2} + \frac{\langle\tau^2\rangle^2}{\langle\tau\rangle^4} - 2\frac{\langle\tau^3\rangle}{\langle\tau\rangle^3}\right) \cdot B^2\right) \tag{2.2.3}$$

$$P_H = \frac{\left(\frac{q}{m^*}\right)^5 \cdot \frac{\langle\tau^2\rangle^2 \cdot \langle\tau^3\rangle}{\langle\tau\rangle^2} \left(1 + \left(\frac{q}{m^*}\right)^2 \cdot \left(\frac{\langle\tau^3\rangle}{\langle\tau\rangle} - 2 \cdot \frac{\langle\tau^4\rangle}{\langle\tau\rangle^2} - \frac{\langle\tau^5\rangle}{\langle\tau\rangle^3}\right) \cdot B^2\right)}{\frac{nq^2}{m^*} \cdot \langle\tau\rangle \left(1 + \left(\frac{q}{m^*}\right)^2 \cdot \left(\frac{\langle\tau^2\rangle^2}{\langle\tau\rangle^2} - \frac{\langle\tau^3\rangle}{\langle\tau\rangle}\right) \cdot B^2\right)} \tag{2.2.4}$$

According to equation 2.2.2, the input resistance R_{in}, i.e. the resistance between the biasing contacts is given by:

$$\begin{aligned} R_{in} &= \frac{1}{\sigma_n} \cdot \frac{l}{w \cdot t} = \frac{1}{n \cdot q \cdot \mu_n^* \cdot \left(1 + \mu_n^{*2} \cdot \left(\frac{\langle\tau^2\rangle^2}{\langle\tau\rangle^4} - \frac{\langle\tau^3\rangle}{\langle\tau\rangle^3}\right) \cdot B^2\right)} \cdot \frac{l}{w \cdot t} \\ &\simeq \frac{1}{n \cdot q \cdot \mu_n^*} \cdot \frac{l}{w \cdot t} \left(1 + \mu_n^{*2} \cdot \left(\frac{\langle\tau^2\rangle^2}{\langle\tau\rangle^4} - \frac{\langle\tau^3\rangle}{\langle\tau\rangle^3}\right) \cdot B^2\right) \\ &\simeq R_{in0} \left(1 + \mu_n^{*2} \cdot \left(\frac{\langle\tau^2\rangle^2}{\langle\tau\rangle^4} - \frac{\langle\tau^3\rangle}{\langle\tau\rangle^3}\right) \cdot B^2\right) \end{aligned} \tag{2.2.5}$$

here R_{in0} is the input resistance without magnetic induction. Equation 2.2.5 shows that the input resistance increases with respect to B^2. Slow electrons (i.e. with relaxation time lower than the mean relaxation time $\langle\tau\rangle$) are subject to the Lorentz force $\boldsymbol{F_m}$, which is not totally compensated by the transverse Hall force (figure 2.5). Their path is longer compared to the one of mean-velocity electrons for which $\boldsymbol{F_m} = -\boldsymbol{F_H}$. On the opposite, for fast electrons (i.e. with relaxation time higher than the the mean relaxation time $\langle\tau\rangle$), the Hall force is not compensated by the Lorentz force, which also leads to an equivalent longer path. Therefore,

under magnetic induction, the electron path is globally longer, which increases the input resistance. This phenomenon is linked to the dispersion of the carrier's mean velocity and is called physical magnetoresistance. It is worth noting this effect, varying with $\mu_n^{*2} \cdot B^2$, is very low and thus not exploited in silicon transducer. Furthermore, as discussed in section 3.3.1, a Hall plate should be biased with a constant current. Thus, the Hall voltage measurement is not affected by the input resistance variation.

2.2.3 Piezo-Hall effect

According to Popovic [8]: "The piezo-Hall effect, is the alteration of the Hall voltage upon the application of a mechanical force. The effect is best characterized by the mechanical stress dependence of the Hall coefficient R_H. The relative change in the Hall coefficient is proportional to the stress X.

$$\frac{\triangle R_H}{R_H} = P \cdot X \tag{2.2.6}$$

Where P denotes the piezo-Hall coefficient."

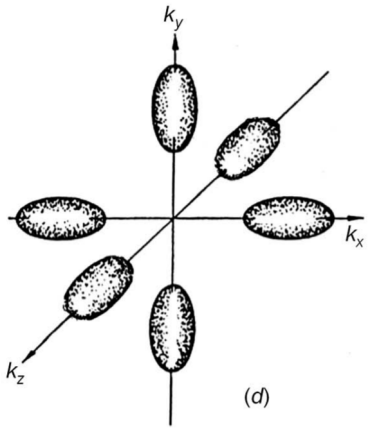


Figure 2.6 – Ellipsoidal constant energy surfaces in the k-space. (Reprinted from [8])

The piezo-Hall, as the piezo-resistive effect stem from the change of the the inter-atomic distance in a crystal under mechanical stress. In ellipsoidal constant energy surface semiconductor (figure 2.6) such as silicon, the mechanical stress affects the valley population [8]. Without stress the six valleys are on average equally populated with carriers [43]. If the crystal is stressed, the conduction band edge increases at some ellipsoids while it decreases at others. As a consequence, the lower valleys are more populated than the higher ones. This population variation affects the Hall coefficient (equation 2.2.6) and finally affects the sensitivity [8].

Chapter 3

Magnetic transducers study

In chapter 2, we considered the ideal case of either, infinitely long and infinitely short active zones. This chapter, focuses on the impact of technology and geometry related parameters on the transducer's behavior. In order to have a global view of the Hall transducer, we also have to study the impact of it biasing mode and the physical nature of its output signal.

3.1 Technological parameters

At this point, general allegations shall be replaced by the particular case of transducers fabricated in CMOS technology. This section sheds light on the key CMOS process parameters that influence the transducer and which may be potentially used to improve its performances.

Above all, we shall consider the physical limit achievable by the power supply. Equation 2.1.24 highlights that the Hall voltage increases with respect to the biasing current. The transducer's resistive behavior converts this current into an equivalent input voltage. Due to the CMOS gate thickness, the maximum input voltage is limited by technology[1] and thus limits the absolute sensitivity achievable.

The nature of the transducer's active zone is the second point to consider. It generally consists of a n-well region. The n-well profile type and doping concentration depends on the considered technology. In modern sub-micron technologies, the dose of impurities tends to increase when the transistor's minimum length decreases. Fortunately, the increase of the the doping level comes along with a reduction of the n-well's depth, which partially compensates the Hall voltage loss. Considering the $n \cdot t$ ratio, the technology evolution has minor influence on the Hall transducers sensitivity [11]. In this context, some works focused on the n-well optimization but this approach requires additional fabrication steps, which increases the final cost of the micro-system [44]. In this work, we will focus on low-cost standard CMOS process without any post-processing.

An alternative way to achieve the active zone consist in using the conduction channel of a n-MOS transistor. In this case, the depth of the active zone and the carrier concentration

[1] 3.3 V for AMS (Austria Micro-System) $0.35\,\mu m$ CMOS process

is modulated by the gate to source voltage V_{GS}. A very thin conduction layer is available at the cost of a loss of carrier conductivity loss. This alternative solution is very interesting for low power design, as will be discussed in part 11.

3.2 Geometrical parameters

So far, we considered ideal case Hall plates. We shall now analyze realistic devices with process-limited measurement contacts size (figure 3.1). As it is, geometric parameters, such for instance the n+ width, are imposed by the technological process.

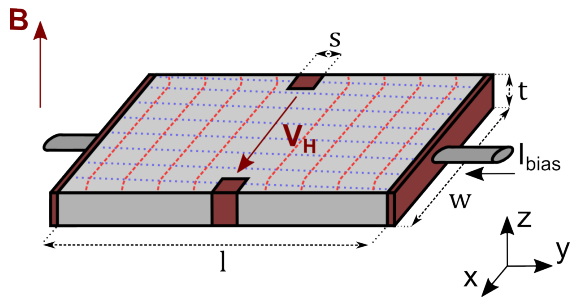


Figure 3.1 – Rectangular Hall plate with non-point-like measurement contacts. The current density lines are sketched in blue lines. The equipotential are sketched in red lines.

3.2.1 Geometrical factor of Hall voltage

The geometrical factor G_H describes the diminution of the Hall voltage in a realistic device compared to that of a corresponding infinity long plate with point-like contacts. The Hall geometrical factor of Hall voltage is defined by:

$$G_H = \frac{V_H}{V_{H\infty}} \tag{3.2.1}$$

Here V_H is the Hall voltage of a realistic Hall plate, and $V_{H\infty}$ the Hall voltage of a perfect Hall pate. Thus, the Hall voltage expressed in equation 2.1.24 becomes:

$$V_H = G_H \cdot \frac{r_H}{n \cdot q \cdot t} \cdot I_{bias} \cdot B_z \tag{3.2.2}$$

A part of the Hall geometrical factor can be attributed to the presence of the measurement contacts in the current flow. In integrated CMOS process, contacts are achieved by means of a high doping region (n+ for a n-type plate), in which the Hall effect is much lower (cf. section 2.1.1.2). A part of the total current flows through these regions causing a reduction of the Hall voltage. An other part of the geometrical factor comes from the short-circuit effect of the biasing contacts. This is due to the fact that the electric field lines are deviated in vicinity of the ohmic biasing contacts. Finally G_H depends on the transducer's geometry and all its dimensions (w, l, t, s).

For a relatively long rectangular Hall plate with small measurement contacts ($l/w >$

$1.5\,s/w < 0.18$), it was demonstrated through conformal mapping method [8] that:

$$G_H = \left[1 - \frac{16}{\pi^2} \cdot \exp\left(-\frac{\pi}{2} \cdot \frac{l}{w}\right) \cdot \frac{\theta_H}{\tan\theta_H}\right] \left(1 - \frac{2}{\pi} \cdot \frac{s}{w} \cdot \frac{\theta_H}{\tan\theta_H}\right) \tag{3.2.3}$$

3.2.2 Geometrical factor of magnetoresistance

Similarly, we can also define the geometrical factor of magnetoresistance as:

$$G_R = \frac{R(B)}{R_\infty(B)} \tag{3.2.4}$$

where $R(B)$ corresponds to the resistance of an actual device, while $R_\infty(B)$ denotes the resistance of an infinitely short device with large contacts.

3.3 Output operation mode

The transducer's operation mode denotes the physical nature of the output signal. As discussed below, this output signal can be either a voltage, or a current or even a resistive change. In case of integrated silicon Hall sensors, the magnetoresistance effect is very low and thus not worth exploiting [8, 45]. Next section details the characteristics of the voltage and current output mode of operation. Note that the output mode is independent of the biasing type which is achieved by constant current or voltage.

3.3.1 The Hall voltage mode of operation

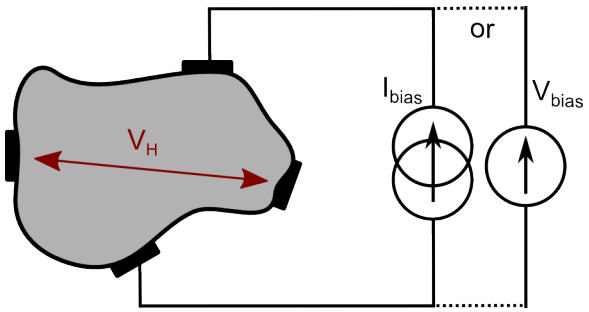


Figure 3.2 – Symbolic representation of a Hall plate with arbitrary shape operated in voltage mode of operation. The transducer is biased either with a constant current or with a constant voltage.

The Hall voltage mode of operation is characterized by the use of two non-neighboring contacts for the biasing (figure 3.2). In this mode, the Hall voltage is considered as the output signal. The Hall plate may either be biased with a constant current source or constant voltage source. Concerning the current biasing, the analysis has already been presented in section 2.1.1 (see equation 2.1.24).

In order to analyze the influence of voltage biasing on the Hall voltage, we shall consider the input resistance $R_{in}(B)$, i.e. the resistance between the biasing contacts as a function of

the magnetic field [8]:

$$R_{in}(B) = \rho(B) \cdot \frac{l}{w \cdot t} \cdot G_R \tag{3.3.1}$$

with $\rho(B)$ the magnetoresistivity.

The Hall voltage can be expressed:

$$V_H = \frac{G_H.R_H}{G_R \cdot \rho(B)} \cdot \frac{w}{l} \cdot V_{bias} \cdot B_z \tag{3.3.2}$$

Here, V_{bias} is the biasing voltage. For low magnetic field, this equation can be simplified as:

$$V_H \simeq \mu_H \cdot \frac{w}{l} \cdot G_H.V_{bias}.B_z \tag{3.3.3}$$

This equation clearly shows the direct relationship between the Hall voltage and the Hall mobility. Moreover, it also underlines the interest of using high carrier mobility materials for discrete Hall devices.

As demonstrated above, the Hall voltage depends on the biasing type. Therefore, its dependence upon temperature is also quite different. If the Hall plate is biased by a constant current, the temperature dependency of V_H appears through $R_H(T)$ (see section 2.1.24, and [46, 47]). However, if the Hall plate is biased by a constant voltage, the temperature dependency of V_H appears through $\mu_H(T)$. The influence of temperature is much stronger on $\mu_H(T)$ than $R_H(T)$ [8]. For that reason Hall plates are usually biased with a constant current. From now one, we will thus only consider current-biased transducers.

3.3.1.1 Sensitivity

The absolute sensitivity of the magnetic sensor is defined by :

$$S_A = \left|\frac{\partial V_H}{\partial B_z}\right|_c \tag{3.3.4}$$

Here, V_H is the Hall voltage given by equation 3.2.2, B_z is the normal component of the magnetic field, and c denotes a set of operating conditions such as temperature, biasing... S_A is expressed in volt per tesla ($V \cdot T^{-1}$). According to equation 3.2.2 and 3.3.4, the Hall plates absolute sensitivity is equal to:

$$S_A = G_H \cdot \frac{r_H}{n \cdot q \cdot t} \cdot I_{bias} \tag{3.3.5}$$

Another typical characteristic of magnetic transducers is their current-related sensitivity given in volt per ampere per tesla ($V \cdot A^{-1} \cdot T^{-1}$), called S_R and defined by:

$$S_R = \frac{1}{I_{bias}} \left|\frac{\partial V_H}{\partial B_z}\right|_c \tag{3.3.6}$$

which gives:

$$S_R = G_H \cdot \frac{r_H}{n \cdot q \cdot t} \tag{3.3.7}$$

3.3.1.2 Offset

The offset voltage voltage is a parasitic voltage, which adds to the transducer's output voltage:

$$V_{OUT} = V_H + V_{off} \tag{3.3.8}$$

This voltage is considered as constant for a set of environmental parameters such as temperature, mechanical stress, biasing... It is usually not precisely known and limits the static accuracy of the Hall voltage. The major causes of offset in real Hall transducer stem from imperfections during the fabrication process such as ohmic contacts misalignment and material non-uniformity [8]. Another significant offset cause is the modulation of the effective thickness of the transducer's active zone[2], which may break the symmetry of the transducer [48, 49].

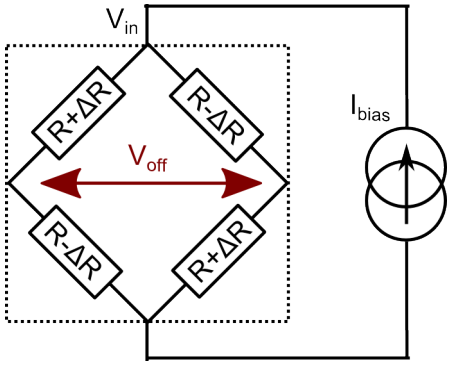


Figure 3.3 – Wheatstone bridge model of a Hall plate. Ideally, the four resistance should be identical but the variation $\triangle R$ leads to bridge asymmetry and hence to offset voltage.

A four ohmic contacts transducer such as the Hall plate can be represented as a Wheatstone bridge (figure 3.3). The offset voltage is modeled by the asymmetry of the bridge and given by:

$$V_{off} = \frac{\Delta R}{R} \cdot V_{in} \tag{3.3.9}$$

Here, V_{in} is the voltage across the biasing contacts. Due to the magnetoresistance effect, the offset also shows small dependence upon the magnetic field. This phenomenon is generally neglected and the offset is supposed independent of the magnetic field. Moreover, by applying signal processing techniques (section 4.2.1.2), the transducer's offset can be dramatically reduced[3].

[2]For instance, this can be the modulation of a depleted zone as will be seen in section 6.3.2.
[3]Typically by a factor around 100-1000.

It is sometimes useful to know the offset-equivalent magnetic field given by:

$$B_{off} = \frac{V_{off}}{S_a} \tag{3.3.10}$$

3.3.1.3 Noise

The noise voltage limits the dynamic precision of the output voltage (Hall voltage and offset voltage). A third term modeling the noise voltage $V_N(t)$ is now added to equation 3.3.8:

$$V_{OUT} = V_H + V_{off} + V_N(t) \tag{3.3.11}$$

In CMOS transducers, the dominating noise sources are the 1/f noise (also called flicker noise) and the thermal noise (also called Johnson noise). The total noise is described by the voltage noise spectral density [50]:

$$S_{NV}(f) \simeq S_{V\alpha}(f) + S_{VT}(f) \tag{3.3.12}$$

Here, $S_{v\alpha}$ and S_{VT} respectively denote the 1/f noise and the thermal noise spectral densities, f is the frequency. Figure 3.4 represents these different noise signals in time domain and their corresponding spectral densities.

The 1/f noise is named after its dependency upon frequency, $I^2 \cdot K/f^\alpha$, where I is the current, K is a constant and α is close to 1. The 1/f noise thus prevails at low frequencies. No further details are given here because the 1/f noise strongly depends on the type of device considered[4].

Two competing models have been developed to explain 1/f noise in silicon technologies:

- The McWhorter model proposed in 1955 [53] attributes the 1/f noise to surface effects. In this theory the 1/f is modeled by fluctuations in the number of carriers (Δn) due to charge trapping at the Si/SiO_2 interface.

- The Hooge model proposed in 1969 [54] attributes the flicker noise to a volume effect which takes its origin in random mobility fluctuations ($\Delta\mu$).

More recently, different combined models have been proposed to improve the noise level prediction [55, 56, 57]. Concerning Hall transducers, the origin of the 1/f noise depends on the type of the active region (n-well or MOS transistor conduction channel) [8].

[4]One can notice that the 1/f noise can be observed in any electronic device but also in mechanical, geological, biological processes [51]. 1/f phenomena can also be observed in acoustic systems [51]. No satisfactory explanation has been given until now but it appears that the origin of the flicker noise is very different depending on the considered area [52]. The actual origin of the 1/f mechanism comes from the memory of the system whose time constants are distributed evenly over logarithmic time [51, 52].

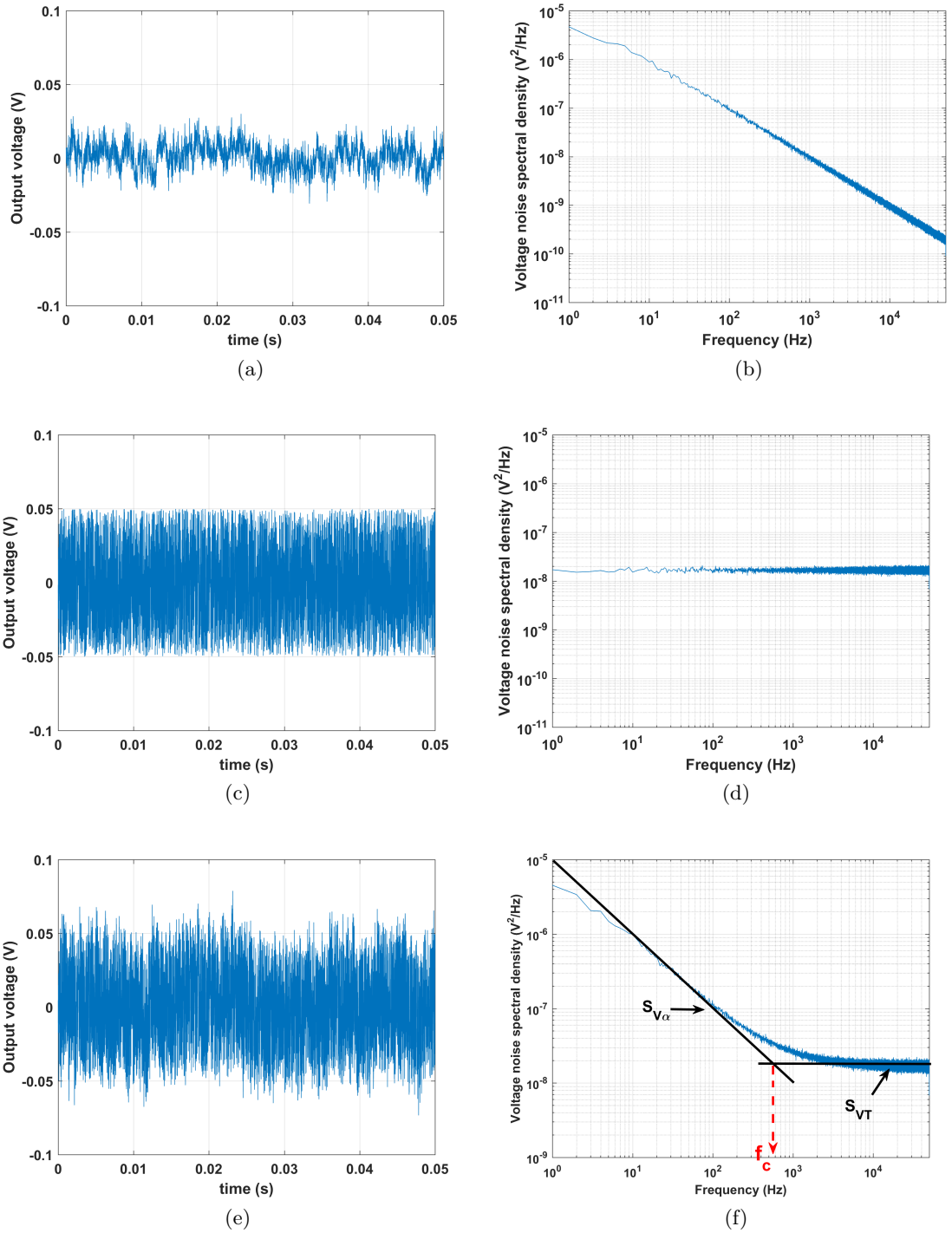


Figure 3.4 – Different noise types are represented in time domain (left column), and frequency domain (right column). Figures (a-b) , (c-d) and (e-f) respectively represent 1/f noise, thermal noise and total noise (i.e. including both noise types). In (f), f_c is the corner frequency.

The thermal noise S_{VT} is caused by the thermal agitation (brownian motion) of carriers in a resistive device. It is generally approximated by a white noise spectrum that extends to the microsystem's cut-off frequency. The noise voltage power spectral density across a resistance R is given by:

$$S_{VT} = 4 \cdot k_B \cdot T \cdot R \tag{3.3.13}$$

where k_B is is the Boltzmann constant. For a transducer, the resistance R corresponds to the output resistance, i.e. the resistance across the measurement contacts.

3.3.1.4 Resolution

Resolution is the smallest increment of magnetic field, B_{min}, which can be sensed for a given bandwidth $\Delta f = f_2 - f_1$. The resolution depends on the absolute sensitivity and on the total noise power spectral density:

$$B_{min} = \frac{1}{S_a}\sqrt{\int_{f_1}^{f_2} S_{NV}(f)\, df} \tag{3.3.14}$$

3.3.2 The current mode of operation

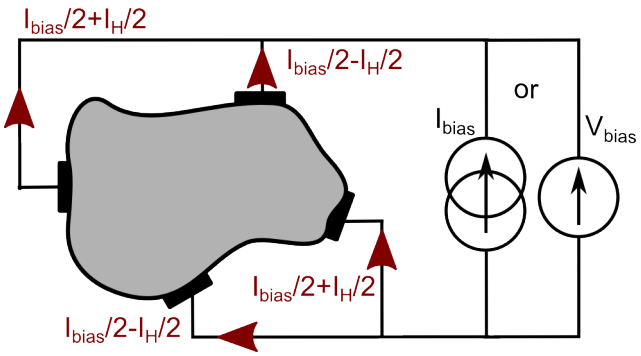


Figure 3.5 – Symbolic representation of a Hall plate with arbitrary shape operated in current mode. The transducer is biased either with a constant current or a constant voltage.

When the Hall plate is operated in Hall current mode (figure 3.5), the Hall current, i.e. the deflection current, can be regarded as the output signal. In this operating mode, infinitely large contacts are used in order to increase the short-circuit effect at the expense of the Hall voltage.

To further understand the Hall current we should use the geometrical similarities between the Hall voltage and Hall current modes of operation. As previously mentioned, the operation mode (output mode) is independent from the way the transducer is biased (voltage or current). Yet, for calculation purpose, in the following examples we will compare a voltage-biased voltage-mode operated transducer to a current-biased current-mode operated transducer. Figure 3.6 (a) shows a very long Hall plate with point-like measurement contacts operated in voltage mode (i.e. the output signal is the Hall voltage). The device is biased by the voltage V_{bias}. When no magnetic induction is applied, the equipotential lines are parallel to the

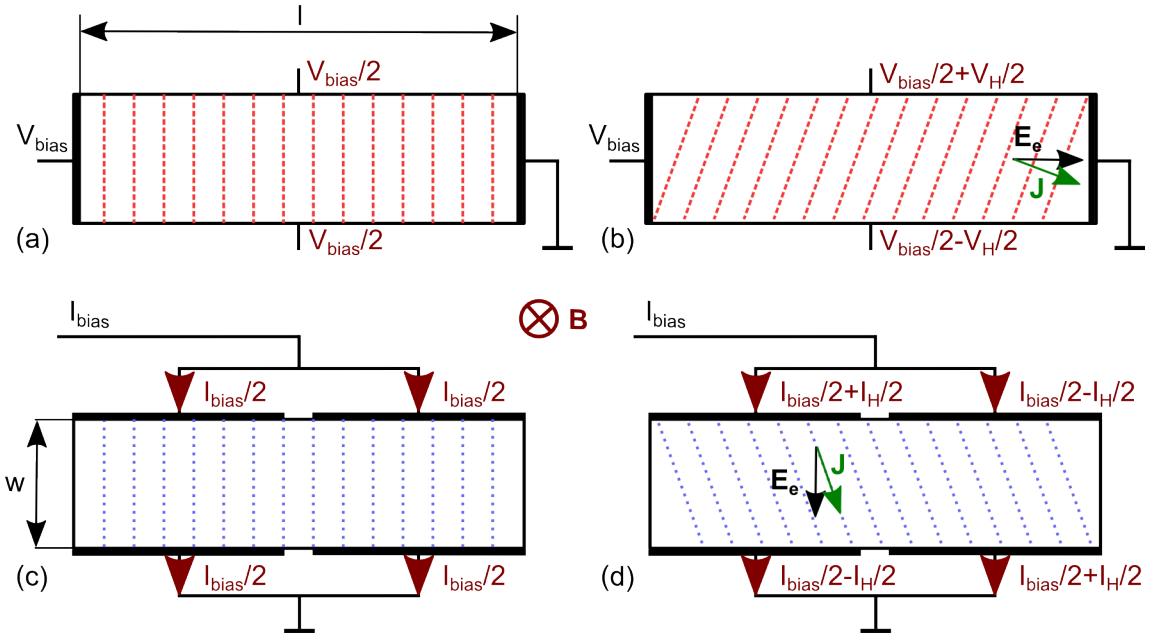


Figure 3.6 – Analogy between a long Hall device operating in the Hall voltage mode ((a) and (b)) and its dual device operating in the current mode ((c) and (d)). The broken lines in (a) and (b) are the equipotential lines; the similarly distributed doted lines in (c) and (d) are the current lines. A magnetic induction produces equal relative disturbances in the equipotential lines (c) and in the current lines (d). Therefore, $^{V_H}/_{V_{bias}} = {}^{I_H}/_{I_{bias}}$. Adapted from [8].

biasing contacts. Figure 3.6 (c) shows a very short Hall plate with large contacts operated in current mode. The device is biased by the current I_{bias}. In the absence of any magnetic induction, the current density lines are perpendicular to the contacts.

When a magnetic induction is applied, the equipotential lines of the voltage-mode operated transducer rotate by the Hall angle θ_H (figure 3.6(b)). Similarly, the current density lines of the current-mode operated transducer rotate by the same angle but in the opposite direction (figure 3.6(d)).

By considering the input resistance given in equation 3.3.1, the Hall voltage in figure 3.6(b) becomes:

$$V_H = \frac{G_H.R_H}{G_R \cdot \rho\,(B)} \cdot \frac{w}{l} \cdot V_{bias} \cdot B_z \tag{3.3.15}$$

According to figure 3.6 and equation 3.3.15, the equivalent transverse Hall current can be written as:

$$I_H = \frac{G_H.R_H}{G_R \cdot \rho\,(B)} \cdot \frac{w}{l} \cdot I_{bias} \cdot B_z \tag{3.3.16}$$

For low magnetic induction, equation 3.3.16 can be approximated by:

$$I_H \simeq \mu_H \cdot \frac{w}{l} \cdot G_H.I_{bias}.B_z \tag{3.3.17}$$

3.3.2.1 Sensitivity

In current mode of operation, the Hall current is the output signal. For low magnetic induction, the absolute sensitivity is then given by:

$$S_A = \left|\frac{\partial I_H}{\partial B_z}\right|_c \simeq \mu_H \cdot \frac{w}{l} \cdot G_H. \cdot I_{bias} \tag{3.3.18}$$

The corresponding unit is ampere per tesla $(A \cdot T^{-1})$.

The current-related sensitivity is thus given by:

$$S_R = \frac{1}{I_{bias}} \left|\frac{\partial I_H}{\partial B_z}\right|_c \simeq \mu_H \cdot \frac{w}{l} \cdot G_H \tag{3.3.19}$$

The corresponding unit is here ampere per ampere per tesla $(A \cdot A^{-1} \cdot T^{-1})$ and is sometimes expressed in percent per tesla $(\% \cdot T^{-1})$.

3.3.2.2 Offset

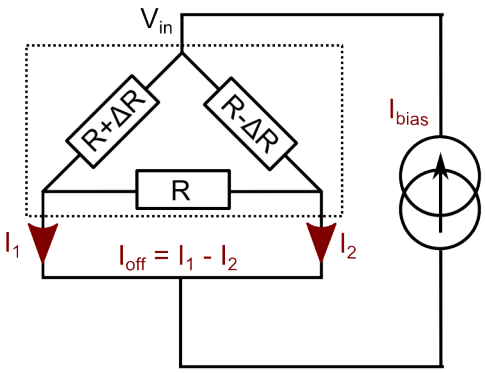


Figure 3.7 – Triangular bridge model of a Hall plate in current mode. Ideally, the three resistors should be equal to R but the variation $\triangle$R leads to bridge asymmetry and offset current I_{off}.

In current mode of operation, the transducer is modeled by a three-branch resistor network in delta configuration. Figure 3.7 shows the network representation in which two adjacent contacts are shorted to form the biasing contact. Thus, in current mode of operation the transducer becomes a three contacts device. The corresponding triangular resistive model with ΔR variation, is shown in figure 3.7 and leads to an offset current:

$$I_{off} = V_{biaseq} \cdot \left(\left(\frac{1}{R + \Delta R} - \frac{1}{R - \Delta R}\right)\right) \tag{3.3.20}$$

As previously, V_{in} is the voltage across the to biasing contacts.

This offset current adds as a second component to the output current:

$$I_{OUT} = I_H + I_{off} \tag{3.3.21}$$

3.3.2.3 Noise

In current mode, the noise current limits the dynamic precision with which we can determine the output current (Hall current and offset current). A third term, modeling the noise current $I_N(t)$, is added to the output current:

$$I_{OUT} = I_H + I_{off} + I_N(t) \tag{3.3.22}$$

As previously, the total noise current is described by the current noise spectral density:

$$S_{NI}(f) \simeq S_{i\alpha}(f) + S_{iT}(f) \tag{3.3.23}$$

Here $S_{i\alpha}$ and S_{iT} denote respectively the current noise spectral density due to the flicker noise and to the thermal noise, f is the frequency.

3.3.2.4 Resolution

The resolution is B_{min} , for $\Delta f = f_2 - f_1$ bandwidth, is now given by:

$$B_{min} = \frac{1}{S_a}\sqrt{\int_{f_1}^{f_2} S_{NI}(f)\, df} \tag{3.3.24}$$

According to Popovic [8], for the same transducer, no resolution difference is expected between current and voltage mode.

Chapter 4

Integrated magnetic field sensor

A great majority of integrated magnetic field sensors are fabricated in silicon [8]. Despite their relatively low mobility compared to InSb and GaAs, silicon technologies are a very attractive because they are versatile, extremely mature and low-cost. Indeed, standard CMOS processes allow the integrating of both the transducer and its conditioning electronics on a same chip without any post-processing and can be further extended to advanced functions such as noise reduction, thermal compensation, analog to digital conversion, digital signal processing... In this chapter we focus on the association of a silicon transducer with its conditioning electronics. This set is known as the front-end of integrated magnetic sensors.

4.1 Transducers

4.1.1 Horizontal Hall Device

The Horizontal Hall Device (HHD) is the simplest way to integrate a Hall plate in CMOS process. This transducer works in voltage mode and is preferably biased with a constant current source (see section 3.3.1).

The active region of the HHD is a n-type well, which is generally used to fabricate n-well resistors (figure 4.1). The Hall plates depth is determined by the thickness of the n-well, which is around $2\,\mu m$ for $0.35\,\mu m$ CMOS process [39]. Ohmic contacts for biasing and measurements are high-doped n+ region. The n-well is surrounded by p+ diffusion connected to the lowest potential and is used to bias the substrate. The p-substrate/n-well junction acts as a diode to isolate the transducer from the rest of the chip. As developed in section 2.1.1.2, the HHD is sensitive to the magnetic field perpendicular to surface of the chip (z-axis). In figure 4.1, contacts C_{b1} and C_{b2} are dedicated to the biasing, while C_{m1} and C_{m2} are used to measure the output voltage.

The voltage mode resolution, given by equation 3.3.1.4 depends on the ratio between the total noise power spectral density and the absolute sensitivity. To achieve high resolution, we need both low spectral density and high absolute sensitivity. According to equation 3.2.2, I_{Bias} should be as high as possible. Other parameters such as the doping level n and the n-well thickness t are imposed by the process.

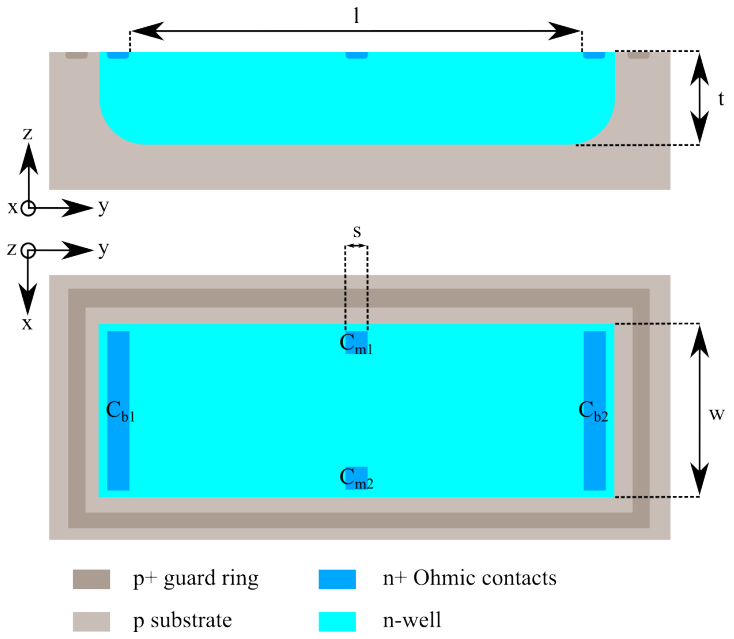


Figure 4.1 – Rectangular Horizontal Hall effect Device.

It is however possible to reduce the n-well depth by placing a gate (SiO2 and metal layers) upon the n-well. By applying appropriate gate biasing it is thus possible to create a depleted region, which pushes the current deeper in the n-well [58]. Frick et al. [58] highlight an increase of the relative sensitivity by 40% ($120\,V/AT$ against $80\,V/AT$ for $0.6\,\mu m$ CMOS process). Unfortunately, the transducers input resistance increases accordingly, thus limiting the maximum biasing current. Therefore, adding a gate does not actually improves the absolute sensitivity, yet it reduces the 1/f noise. As it is, according to Vandamne [55], the lattice defect density is higher at the n-well/SiO2 interface than in the n-well's bulk. As a consequence, the resolution is better for the same biasing current.

Furthermore, as presented in figure 4.2, modern HHD are designed to be symmetrical by rotation of 90°. This allows, further performance improvements by using specific signal processing presented in section 4.2.1 [8].

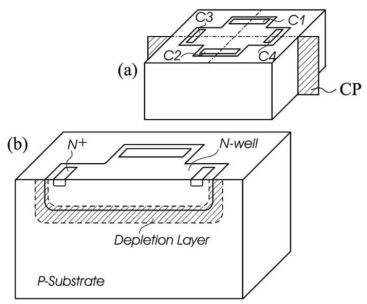


Figure 4.2 – Cross-shaped Hall device in bulk CMOS technology. (a) General view, CP denotes a crossing plane. (b) View along CP. Reprinted from [8].

4.1.2 Vertical Hall Device

The HHD only allows 1D magnetic field measurement (i.e. perpendicular to the surface of the chip). In some cases, it can be useful to have 2D and 3D measurement capabilities. This can be done by using two additional orthogonal-mounted HHD chips. ICs positioning yet requires expensive non-standard post-processing [59]. A more elegant and cost-effective solution is two integrate one HHD and two Vertical Hall Devices (VHDs) on the same chip. The five contacts VHD was proposed by Popovic in 1984 [60]. It is called "vertical" because the active region is perpendicular to the surface of the chip. The VHD is thus sensitive to the magnetic field perpendicular to the active region and parallel to the surface of the chip.

The VHD structure is obtained by conformal mapping applied on the HHD [8]. Figure 4.3 represents the VHD transformation steps. In figure 4.3 (a), the HHD is represented in the volume of the chip. The biasing contacts $C1/C5$ and the measurement contacts $C2/C4$ are in the substrate volume, thus they are not accessible in a planar CMOS process. In figure 4.3 (b), the conformal mapping is applied to the HHD. Finally, figure 4.3(c) shows the VHD obtained after conformal mapping. All the contacts are now located on the surface of the substrate and are thus accessible.

The first fabricated VHDs were discrete components using n-type substrate [32, 61]. This specific technology with constant doping provides sensitivities up to $400\,V/AT$ [60, 8]. The first five-contacts VHD (figure 4.3 (c)) suitable for CMOS process was proposed in 2002 [62]. This transducer is based on a deep high-voltage n-well integrated on p-substrate. The conventional VHD is actually not consistent with a standard shallow n-well. Due to the gaussian doping distribution with maximum level near the surface, the current flow is concentrated on the top of the n-well. Thus, the location of the measurement contacts, i.e. in the current flow, is responsible for short-circuit effect, which dramatically reduces the sensitivity (cf. section 3.2.1). To minimize this phenomena one has to use the high-voltage option available with some CMOS process.

The same teams as in [62] proposed to applies offset and noise reduction techniques to the VHD (cf. section 4.2.1.2), reducing offset form initially $30\,mT$ down to $1-4\,mT$. To further reduce the offset, they also proposed a four-contact VHD with lower initial offset leading to $0.2\,mT$ residual offset. Concerning the resolution, this four-contact VHD operated with noise reduction technique achieves $76\,\mu T$ resolution over $1.6\,kHz$ bandwidth ($1.9\,\mu T/\sqrt{Hz}$) [36]. This VHD's performance are yet poor compared to equivalent resolution achieved by the HHD [58].

More recently, Sander et all. proposed a new approach suitable with deep n-well, based on three-contact structure [63]. Four of such VHDs are coupled in series to form a four-contact transducer. It features $0.14\,mT$ offset and $11.6\,\mu T$ ($0.29\,\mu T//\sqrt{Hz}$) resolution over the reference bandwidth [63]. A second coupling method, combining 16 series and parallel connected VHDs has been proposed. This configuration yiels $0.04\,mT$ offset and $5.2\,\mu T$ ($0.13\,\mu T//\sqrt{Hz}$) resolution [64].

One reason of the performance gap between the HHD and the VHD has been highlighted

by Pascal et al. [65]. They demonstrated that a part of the Hall voltage appears at the bottom side of the chip and is thus lost since it cannot be accessed in planar technologies.

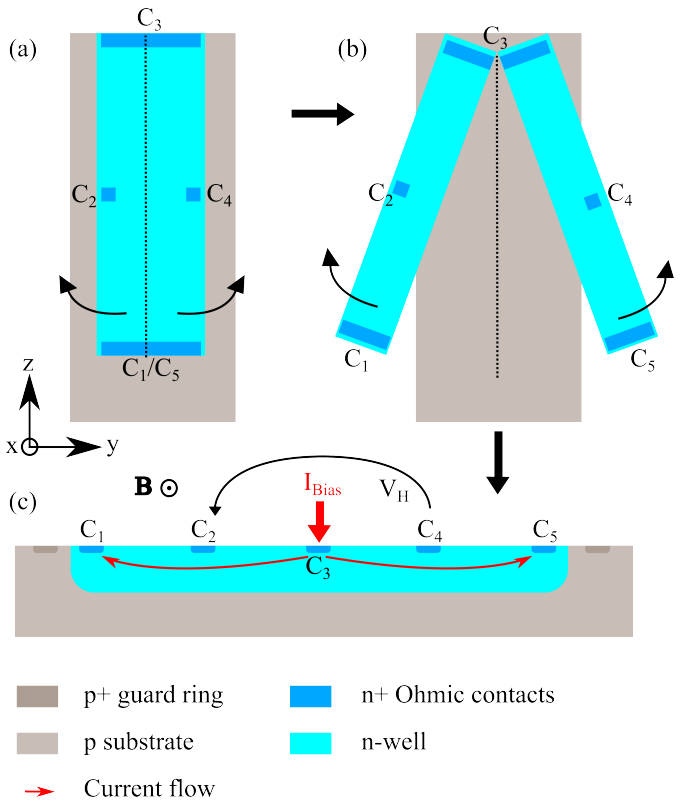


Figure 4.3 – (a) HHD oriented in the chip surface. (b) Principle of the conformal mapping. (c) VHD structure obtained by conformal mapping applied on the HHD

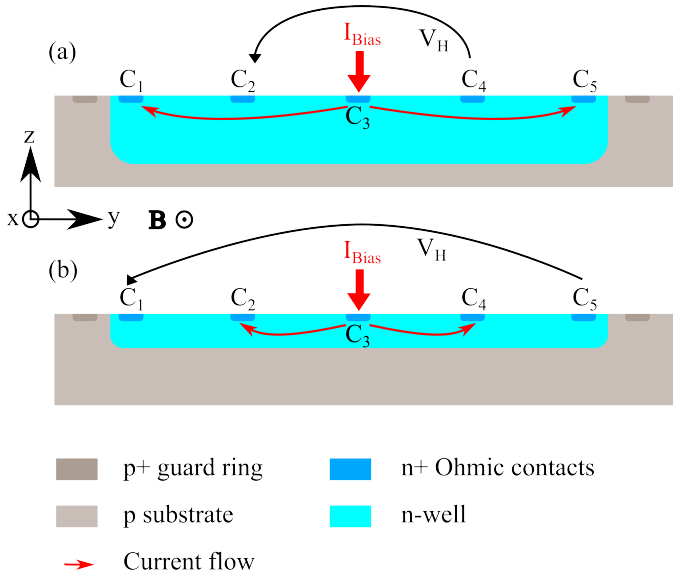


Figure 4.4 – (a) HV-VHD with HV option and deep n-well. (b) LV-VHD with shallow n-well.

As a consequence, the Hall voltage is lower for a VHD compared to its equivalent HHD.

In order to to take this effect into account, a new coefficient G_v is added to equation 3.2.2:

$$V_H = G_v \cdot G_H \cdot \frac{r_H}{n \cdot q \cdot t} \cdot I_0 \cdot B_x \tag{4.1.1}$$

Here, the Hall voltage depends on the magnetic field along x-axis. The coefficient G_v models the intrinsic limitation of the VHD sensitivity. It has been showed by FEM simulations that the highest value for G_v is around 0.75 [65].

In order to further reduce the fabrication costs, Pascal et al. proposed a LV-VHD suitable with a standard shallow n-well [33] (figure 4.4 (b)). The measurement contacts $C1/C5$ are located outside the current flow. As can be seen in figure 4.5 (a), this change of location is made to the detriment of the sensitivity. However, since the measurement contacts are placed in a low-current density region, the 1/f noise (figure 4.5 (b)) as well as the offset are dramatically reduced. The LV-VHD achieves around 100 µT resolution without any signal processing technique [33]. This results is comparable with the resolution achieved by the HV-VHD with noise and offset reduction technique (cf. 4.2.1.2) [36].

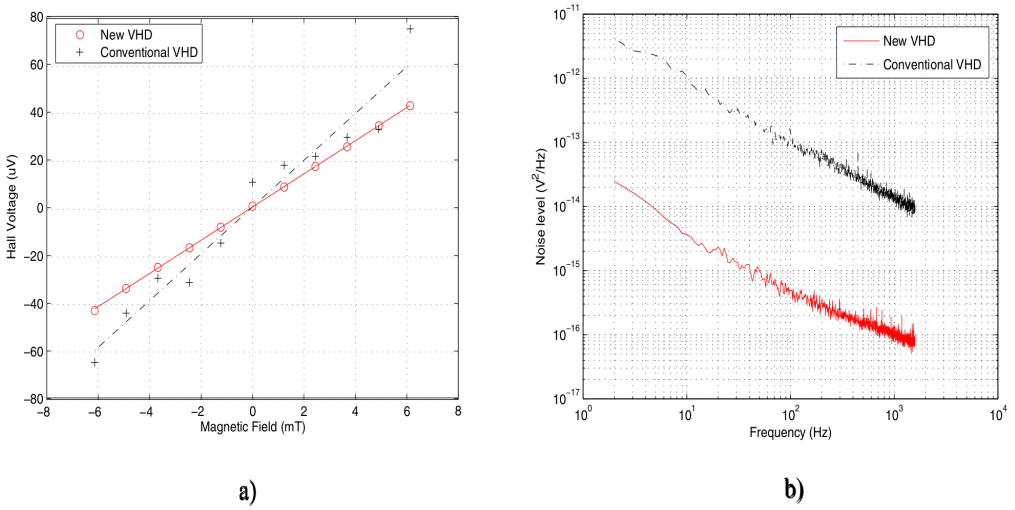


Figure 4.5 – (a) Measured sensitivity for conventional and LV-VHD. (b) Output noise for conventional and LV-VHD. Both measurements are done on a shallow n-well VHD with 1.12 mA biasing current. Here, the LV-VHD exhibits 79 µT resolution over 1.6 kHz bandwidth, while the conventional VHD exhibits only 710 µT resolution over the same bandwidth. Reprinted from [33].

4.1.3 MagFET

The MagFET transducer is based on a MOS transistor (either n or p-type) with two or more drains replacing the conventional single drain (figure 4.6). The transduction principle is based on the current deflection effect (cf. section 2.1.2). When no magnetic field is applied to the transducer, considering a device with n identical drains, the current in the drains is given by:

$$I_{D1} = I_{D2} = ... = I_{Dn} = I_{DS}/n \tag{4.1.2}$$

Here I_{DS} is the total current flowing between the two-drain and the source. I_{D1}, I_{D2}, ..., I_{Dn} denote the currents flowing respectively between the MagFET's *Source* and $Drain_1$, $Drain_2$, ..., $Drain_n$.

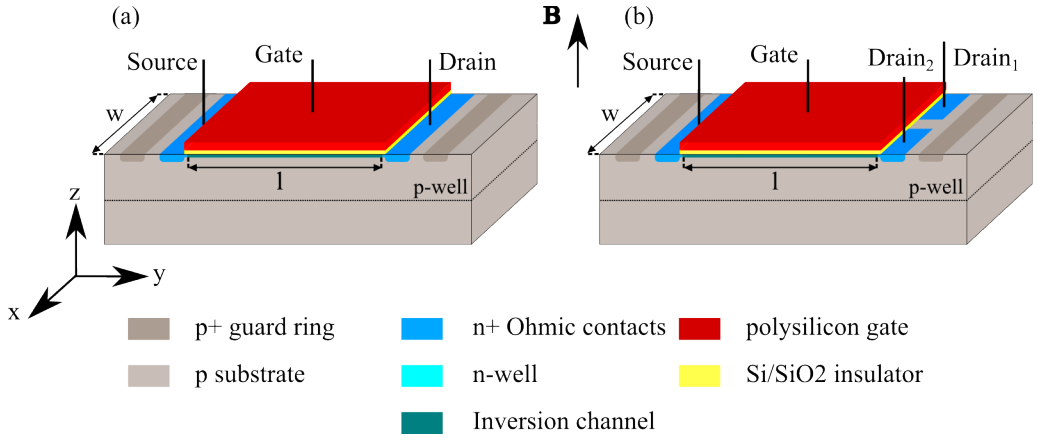


Figure 4.6 – 3D view of (a) a conventional NMOS transistor and of (b) a dual-drain MagFET.

In the presence of a magnetic field perpendicular to active region of the MagFET (i.e. transistor channel), the carriers are deviated along x-axis, leading to a current imbalance ΔI between the drains. In the example of figure 4.6, considering dual-drain MagFET, this imbalance, ΔI, can be written:

$$\Delta I = I_{D1} - I_{D2} \tag{4.1.3}$$

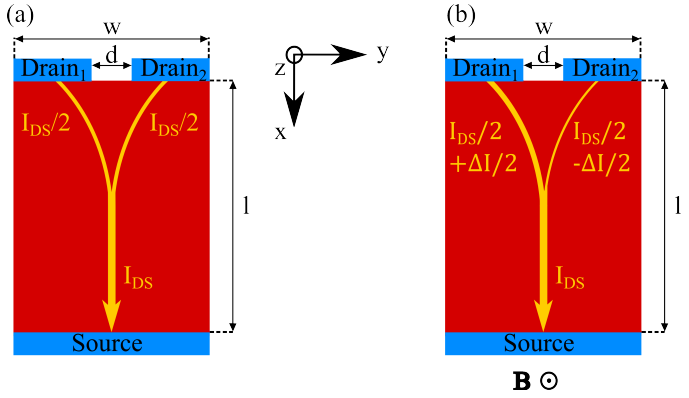


Figure 4.7 – Schematic view of a dual-drain MagFET device with (a) $B_z = 0\,T$ and (a) $B_z > 0\,T$.

The current deflection expressed in equation 3.3.17 here becomes:

$$I_H \simeq \mu_{Ch} \cdot \frac{L}{W} \cdot G_H . I_{DS} . B_z \tag{4.1.4}$$

μ_{Ch} denotes the Hall mobility of the carriers in the transistors channel. It is important to notice that W and L are inverted compared to figure 3.6, hence the inversion in equation 4.1.4 compared to equation 3.3.17. Also note that the previous developments are only valid when the MagFET operates the linear region. In saturation region the expression of I_H cannot be analytically expressed [8].

4.2 Conditioning electronics

4.2.1 Offset / Noise reduction techniques

This section presents the offset and 1/f noise reduction techniques mentioned in section 3.3. By definition, 1/f noise prevails at low-frequencies and can be considered as a slowly-varying offset. Therefore, under some conditions detailed bellow, the offset cancellation techniques will also remove the 1/f noise.

The first way to deal with the offset is the Correlated Double Sampling (CDS). This sampling based technique, is generally used in switched capacitor amplifiers [66] and CMOS cameras [67]. Unfortunately, it increases the noise floor and is thus rarely applied to integrated magnetic field transducers [68]. The most common offset and 1/f noise reduction techniques for integrated magnetic sensors are: the Spinning Current Technique (SCT) for the transducer and the Chopper Stabilization (CS) for the conditioning electronics (biasing and amplification).

We now first consider the CS applied to the conditioning electronics associated to the transducer.

4.2.1.1 Chopper stabilization

The CS technique was proposed about 50 years ago to provide high-precision DC amplifier with vacuum tubes and mechanical relay choppers [66]. Nowadays, many integrated amplifiers feature this technique to reduce 1/f noise and offset [69, 70, 71].

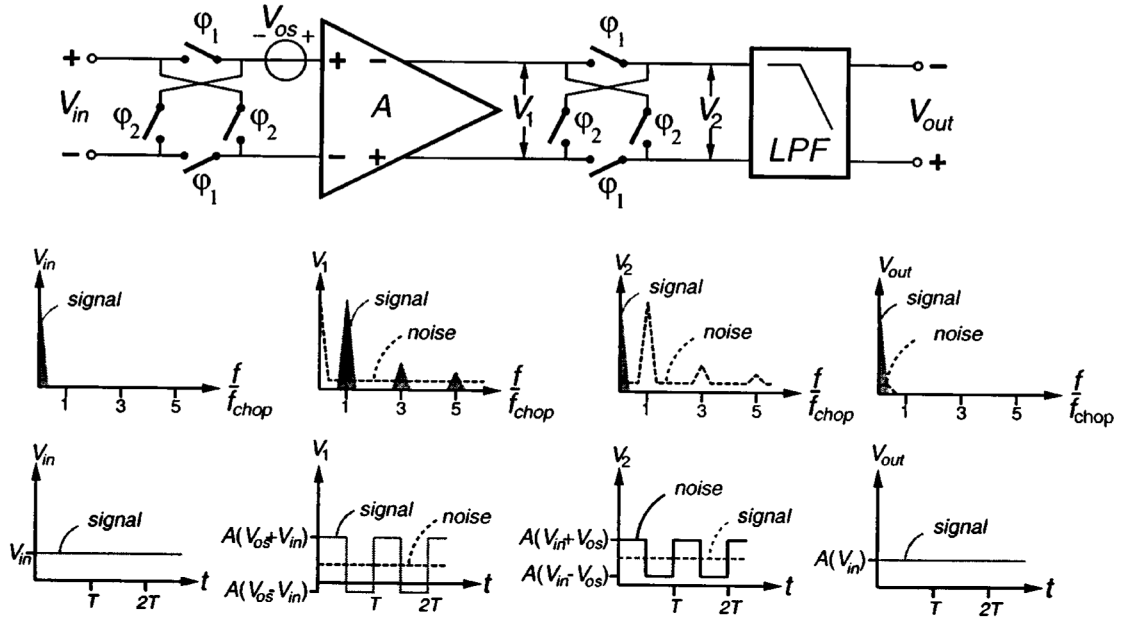


Figure 4.8 – Chopper Stabilized amplifier including signals in frequency and time domain (reprinted from [30]).

Figure 4.8 shows the structure of a CS amplifier [30]. It consists of modulator switches, referred to as "chopper". The chopper structure inverts the signal periodically at the frequency

f_{chop}. The switching process requires to two opposite clock signals. The CS amplifier also feature an ideal fully-differential gain stage (with gain A). The offset is represented as a voltage source at the input of this gain stage. The modulated signal is filtered by means of a low-pass filter (LPF).

As far as 1/f noise is concerned, the chopping frequency should be two-times higher than the corner frequency (cf. section 3.3.1.3). In this case, considering an ideal amplifier with infinite bandwidth, ideal switches and infinite order filter, the CS technique allows to completely remove the amplifier's offset and 1/f noise.

Yet, in practice, the limited amplifier's bandwidth is responsible for glitches, which limits the CS technique's efficiency. This effect can be limited with careful amplifier design. Also, residual offset can occur because of charge injection due to non-ideal switches and clock signals. These shortcomings can be minimized by applying specific signal processing techniques such as spike filtering, nested chopper and guard band [72]. For instance, the nested-chopper instrumentation amplifier developed in [30] achieves $100\,nV$ residual offset and $27\,nV/\sqrt{Hz}$ noise floor.

4.2.1.2 Spinning current technique

The Spinning Current Technique (SCT) was first proposed and patented by Toromow in 1973 [73]. This technique is used to reduce the transducer's offset and 1/f noise. Basically, the SCT is dedicated to four-contact magnetic transducers operating in voltage mode. This technique relies on the offset sign change according to the current direction, while the Hall voltage remains constant. The principle consists in biasing the transducer alternatively into two orthogonal modes called phases. Figure 4.9 illustrates the biasing diagram in phase $\phi 1$ and phase $\phi 2$.

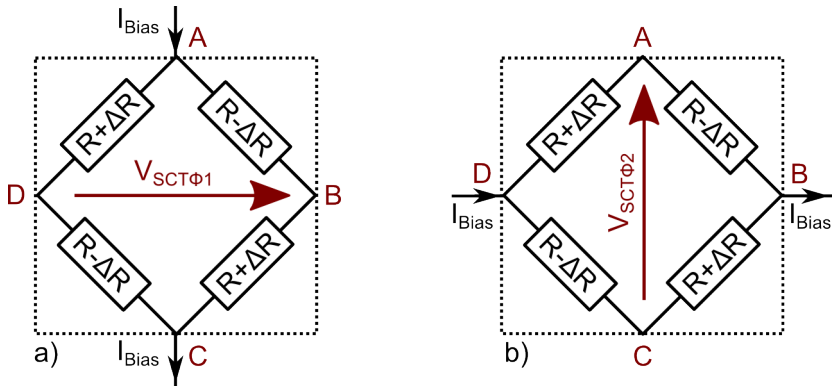


Figure 4.9 – Two-phase spinning current method applied on a four-contact magnetic transducer; (a) phase $\phi 1$ and (b) phase $\phi 2$.

Considering the Hall voltage and the offset, the output voltage in phase $\phi 1$ and $\phi 2$ is given by:

$$\begin{aligned} V_{SCT\phi 1} &= V_H\left(B_z\right) + V_{off} \\ V_{SCT\phi 2} &= V_H\left(B_z\right) - V_{off} \end{aligned} \tag{4.2.1}$$

The spinning current modulates the transducer's offset at the spinning frequency. Thereafter, it can be easily removed by applying adequate low-pass filtering, i.e. with cut-off frequency lower than spinning frequency. In first approximation, the output voltage becomes:

$$V_{SCT} \simeq \frac{V_{SCT\phi1} + V_{SCT\phi2}}{2} = V_H\left(B_z\right) \tag{4.2.2}$$

To complete this analysis, we should also consider other relevant phenomena such noise and planar Hall voltage:

$$\begin{aligned} V_{SCT\phi1} &= V_H\left(B_z\right) + V_{pl}\left(B_x,\, B_y\right) + V_{off} + V_{th} + V_{1/f} \\ V_{SCT\phi2} &= V_H\left(B_z\right) - V_{pl}\left(B_x,\, B_y\right) - V_{off} + V_{th} - V_{1/f} \end{aligned} \tag{4.2.3}$$

Here $V_{pl}\left(B_x,\, B_y\right)$ is the planar Hall voltage depending on the magnetic field along x and y-axis (cf. section 2.2.1), V_{th} is the thermal noise contribution and $V_{1/f}$ is the 1/f noise contribution (cf. section 3.3.1.3). We notice that the sign of V_{pl}, V_{off} and $V_{1/f}$ changes according to the spinning phase. Thus, V_{SCT} becomes:

$$V_{SCT} \simeq \frac{V_{SCT\phi1} + V_{SCT\phi2}}{2} = V_H\left(B_z\right) + V_{th} \tag{4.2.4}$$

As shown in equation 4.2.4, the SCT simultaneously removes the offset, the 1/f noise and planar Hall voltage. Note that to avoid aliasing and thus efficiently remove 1/f, the spinning frequency should be higher than twice the corner frequency ($f_{SCT} > 2 \cdot f_{corner}$).

Figure 4.10 represents the spinning current carried out by a switch box which alternatively switches the transducer's contacts in the corresponding phases.

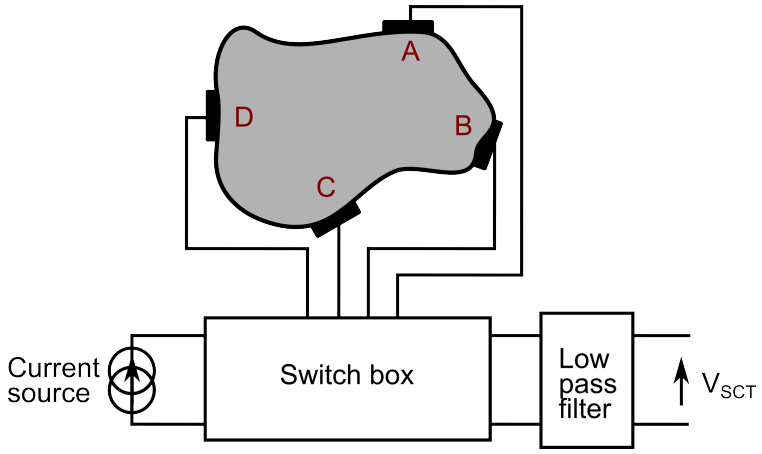


Figure 4.10 – The four-contact magnetic transducer and its associated SCT switch box.

The switch box consists of integrated switches (basically T-gates). There are two ways to perform the spinning current:

- The first one consists in direct demodulation as presented above. In that case, the sign of the Hall voltage is kept constant.
- The second mode is presented in figure 4.11. Here, the Hall voltage is modulated while the offset sign is kept constant. This mode allows to remove the 1/f noise together with

the amplification stage A prior to demodulation. Here, the SCT is combined with the chopper stabilization (CS) technique to remove the offset and 1/f noise of the whole instrumental chain (i.e. sensor).

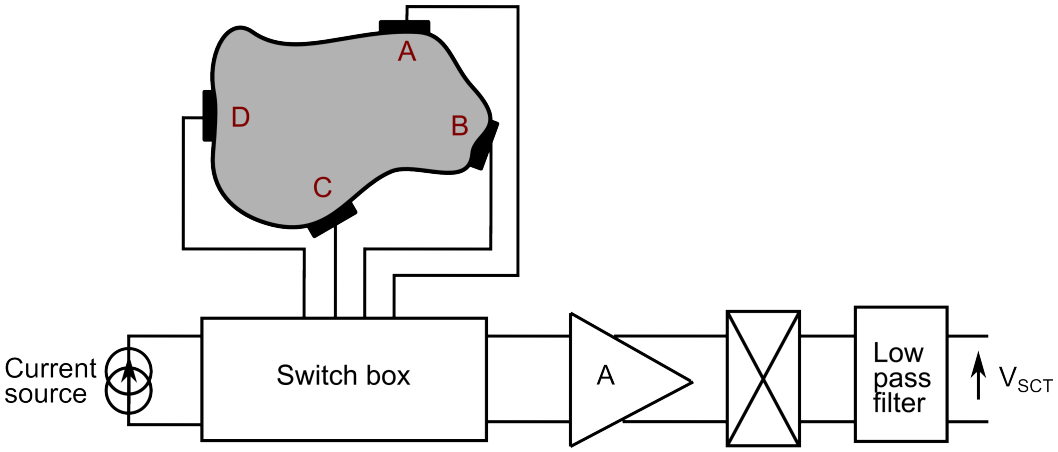


Figure 4.11 – Instrumental chain with amplification prior to demodulation.

It was first thought that the SCT is only efficient on 90° symmetric devices, but Cornils [74] showed in 2008 that two-phase SCT perfectly removes the offset of any arbitrary-shaped linear device (i.e. respecting $\mathbf{J} = \sigma\mathbf{E}$).

In a real device with non negligible second order effects, such as depleted zone effect and carrier velocity saturation, higher-order (more than two phases[1]) spinning current is necessary. With typical CMOS-integrated Hall transducers, two or four-phases SCT is generally used, which leads to a residual offset around several hundreds of microteslas. The residual offset is mainly due to clock charge injection by the switching electronics [66].

4.2.2 Thermal drift compensation

Regarding industrial applications, thermal effect is significant in Hall sensors. Temperature variation will induce electrical parameters fluctuations such as input resistance. In most applications, it is not possible to implement temperature regulation. Therefore, it is important to ensure the sensor's characteristics remain within the acceptable range imposed by the application's specifications. In this section we only consider the effect of temperature on the sensor's sensitivity. Furthermore, since temperature phenomena are slow, the offset drift related to it is removed by SCT.

One can address temperature compensation with two strategies. The first strategy is to apply passive compensation. Its purpose is to bias the transducer and its electronics with thermal-invariant current source. This approach is illustrated in figure 4.12. A band-gap current source, based on lateral bipolar transistor is used to control the required current sources. It also necessary to use cascoded current source (T_{n1} to T_{n4}) because simple current source are temperature dependent [76].

[1] Continuous time SCT is also possible [75].

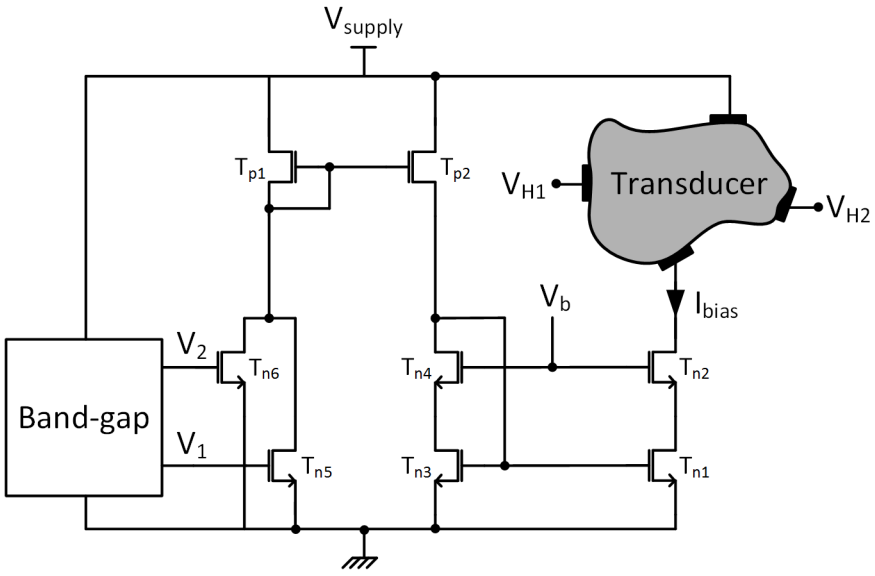


Figure 4.12 – Transducer biased with a cascoded current source and band gap current source.

The second approach is active. It is based on the passive approach combined to active sensitivity compensation. The temperature is real-time monitored and the biasing dynamically adapted to compensate the sensitivity drift. This technique requires preliminary calibration of the instrumental chain. Considering the thermal effect on the transducer operated in voltage mode, the current-related sensitivity is:

$$S_R(T) = G_H \cdot \frac{r_H(T)}{n(T) \cdot q \cdot t_{eff}(T)} \tag{4.2.5}$$

Here, $r_H(T)$, $n(T)$, $t_{eff}(T)$ denotes the thermal dependence of respectively the Hall scattering factor, the electron density and the effective thickness of the active zone. The thermal drift of current-related sensitivity is therefore given by:

$$\frac{\partial S_R}{\partial T} = \frac{\partial S_R}{\partial r_H} \cdot \frac{\partial r_H}{\partial T} + \frac{\partial S_R}{\partial n} \cdot \frac{\partial n}{\partial T} + \frac{\partial S_R}{\partial t_{eff}} \cdot \frac{\partial t_{eff}}{\partial T} \tag{4.2.6}$$

From equation 4.2.5, we obtain:

$$\frac{\partial S_R}{\partial r_H} = \frac{G}{n \cdot q.t_{eff}} \tag{4.2.7}$$

$$\frac{\partial S_R}{\partial n} = -\frac{S_R}{n} \tag{4.2.8}$$

$$\frac{\partial S_R}{\partial t_{eff}} = -\frac{S_R}{t_{eff}} \tag{4.2.9}$$

Thus equation 4.2.6 becomes:

$$\frac{\partial S_R}{\partial T} = S_R \cdot \left(\frac{1}{r_H} \cdot \frac{\partial r_H}{\partial T}\right) - S_R \cdot \left(\frac{1}{n} \cdot \frac{\partial n}{\partial T}\right) - S_R \cdot \left(\frac{1}{t_{eff}} \cdot \frac{\partial t_{eff}}{\partial T}\right) \tag{4.2.10}$$

As published by [8, 47, 46], the effective thickness t_{eff} is considered constant with the tem-

perature when the substrate voltage is constant. Thus, equation 4.2.10 can be simplified as:

$$\frac{\partial S_R}{\partial T} = S_R \cdot \left(\frac{1}{r_H} \cdot \frac{\partial r_H}{\partial T}\right) - S_R \cdot \left(\frac{1}{n} \cdot \frac{\partial n}{\partial T}\right) \tag{4.2.11}$$

The temperature coefficient α_{S_R} of the current related sensitivity is defined as follows:

$$\alpha_{S_R} = \alpha_{r_H} - \alpha_n \tag{4.2.12}$$

Here, α_{r_H} and α_n are the temperature coefficients of respectively the Hall scattering factor and the electron density., with the temperature coefficient of a quantity Q defined as:

$$\alpha_Q = \frac{1}{Q_0} \cdot \frac{\partial Q}{\partial T} \tag{4.2.13}$$

with Q_0 the quantity's value at room temperature [47]. Note that α_n tends to decrease with temperature due to the freeze-out effect while α_{r_H} tends to increase [46].

A second-order expansion Taylor series of $S_R = S_R(T)$ around room temperature T_0 gives:

$$S_R(T) \simeq S_R(T_0) + \alpha_I (T - T_0) + \beta_I (T - T_0)^2 \tag{4.2.14}$$

with α_I the first-order coefficient of the current related sensitivity used for linear compensation, and β_I the second-order coefficient of the current related sensitivity used for second-order compensation. Due to the complexity, higher-order compensation is rarely achieved with analog-only electronics. Digital implementation is preferred [77].

Part II

Vertical Hall Device

Chapter 5

Introduction to the LV-VHD

The Vertical Hall Device (VHD), especially the LV-VHD suitable with low-voltage standard CMOS process, has already been presented in section 4.1.2. This part is dedicated to an extensive study of the LV-VHD.

In order to further understand the physical background of this transducer, we propose an a 2D Finite Element Method (FEM) modeling approach in chapter 6. The models eventually allows to take second order effects into account. Also, one should expect the model to match real device behavior. Therefore, this chapter also presents comparative study of simulations versus experimental results.

The LV-VHD performances are dramatically affected by its 1/f noise and its offset. Therefore, chapter 7 is dedicated to the implementation of the Spinning Current Technique (SCT) to remove this drawbacks. A new, so called bi-current SCT, is proposed. The bi-current technique consists in biasing the LV-VHD with maximum current in each phases. Conventional and bi-current SCT performances are compared through analytical development based on sensitivity and thermal noise analysis.

In order to complete this analysis, chapter 8 is dedicated to conventional and bi-current SCT validation by FEM simulations and experimental results. A new FEM model's version, extended to the 1/f noise, as well as experimental results are proposed.

Chapter 6

FEM modeling

An accurate analytical analysis of the LV-VHD with second order effects is overly complex and not suitable for straightforward implementation in CAD simulation tools. Therefore, we need to use appropriate solving approach such as the Finite Element Method (FEM), which is a numerical method for solving physical problems based on partial differential equations. In this chapter we propose to present a self-consistent 2D FEM COMSOL Multiphysics® model. Solutions to implement the main second order effect such as the junction field effects and the carrier velocity saturation are also proposed.

6.1 Principle

This section presents LV-VHD model principle. The analytical equations used in FEM model are first presented. Then, these equations are implemented in COMSOL Multiphysics®.

6.1.1 Electrical model

In a semiconductor device, the electron and hole current densities (respectively $\mathbf{J_n}$ and $\mathbf{J_p}$) include the conduction and diffusion mechanisms. They are expressed in equation 6.1.1 [8]:

$$\begin{cases} \mathbf{J_n} = -q \cdot n \cdot \mu_n \cdot \boldsymbol{\nabla}\psi + q \cdot D_n \cdot \boldsymbol{\nabla} n \\ \mathbf{J_p} = -q \cdot n \cdot \mu_p \cdot \boldsymbol{\nabla}\psi - q \cdot D_p \cdot \boldsymbol{\nabla} n \end{cases} \tag{6.1.1}$$

where μ_n and μ_p represent the electrons and holes mobilities respectively, D_n and D_p represent the electrons and holes diffusivities respectively, $\boldsymbol{\nabla}\psi$ the electrostatic potential gradient, q the elementary charge, n and p the electrons and holes intrinsic concentrations respectively ($\boldsymbol{\nabla} n$ and $\boldsymbol{\nabla} p$) their respective gradients, k the Boltzmann constant, T the temperature in Kelvin. Note that, in order to have a full electrical model, we assume p and n obey Maxwell-Boltzmann's statistics, and thus the Gauss law gives [8]:

$$-\boldsymbol{\nabla}\left(\epsilon_{Si} \cdot \boldsymbol{\nabla}\psi\right) = q \cdot (p - n + N) \tag{6.1.2}$$

Besides, we use the convection-diffusion expression to model the continuity equations for electrons and holes:

$$\begin{cases} -\boldsymbol{\nabla} \cdot \mathbf{J_n} = -q \cdot R_{SRH} \\ -\boldsymbol{\nabla} \cdot \mathbf{J_p} = q \cdot R_{SRH} \end{cases} \tag{6.1.3}$$

In these equations, ϵ_{Si} is the silicon relative permittivity, N the ionized doping donors' concentration, i.e. the doping profile. R_{SRH} is the Shockley-Read-Hall recombination model [38].

Furthermore, due to the small size of the VHD, the electric fields within it can be high. Therefore, it is important to take the carrier velocity saturation into account in the expression of the mobility, for both the electrons and the holes [78, 79]. According to [78] a power law mobility function, $\mu_{sat_{n/p}}$, is used to replace the constant mobility $\mu_{n/p}$:

$$\mu_{sat_{n/p}} = \frac{\mu_{n/p}}{\left(1 + \left(\frac{\mu_{n/p} \cdot \|\boldsymbol{\nabla}\psi\|}{V_{sat_{n/p}}}\right)^{\beta}\right)^{1/\beta}} \tag{6.1.4}$$

$V_{sat_{n/p}}$ is the saturation velocity, i.e. $10^7\, cm \centerdot s^{-1}$ for electrons and $8 \centerdot 10^6\, cm \centerdot s^{-1}$) for holes, and β is a fitting parameter, which value has been determined in [78], i.e. 1.30 for electrons and 1.21 for holes.

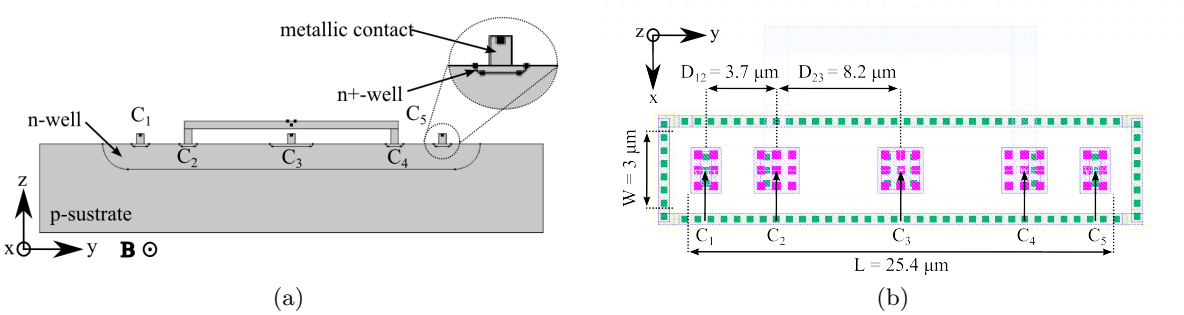
6.1.2 COMSOL® implementation

Since the LV-VHD is symmetric along x-axis and almost no current flows in this axis, we assumed a two dimensional model should allow faithful modeling of the device. Thus, we neglected the lateral junction field effect on the n-well / p-substrate junction, along x-axis. As a consequence, the effect of the junction modulation will be slightly underestimated. Furthermore, while this assumption does not affects global model accuracy, it also has the positive impact to dramatically reduces computation time.

Based on the p-n junction application note [80], we used COMSOL multiphysics® capabilities to model the physical equations given in section 6.1.1. Theses equations are combined through the electrostatic module and the transport of diluted species (i.e. electrons and the holes) module. The transport of diluted species module is used to describe the conduction/diffusion mechanism described in section 6.1.1.

According to measurements performed by Dimitripopoulos at al. [39], we chose Gaussian approximation to model the doping profile. The n-well maximum doping level was initially set to $5 \cdot 10^{16}\, cm^{-3}$ [80]. The n-well depth, i.e. the depth at which the silicon has intrinsic properties, was set to $2\,\mu m$ [39]. Finally, the n+ junction depth was set to $200\,nm$ [39].

The metallic contact to access the n+ well and the link between C_2 and C_4 were modeled as n+ silicon with artificially high mobility. Figure 6.1 (a) represents a view of the model geometry. All geometrical parameters are fitted to the VHD prototype fabricated with AMS $0.35\,\mu m$ process [79].



(a) (b)

Figure 6.1 – (a) View of the 2D LV-VHD COMSOL model geometry, and (b) its corresponding layout.

6.2 Model validation

A LV-VHD prototype, presented in figure 6.1 (b), has been fabricated with AMS 0.35 μm process.

Figure 6.2 shows the IV characteristics across each contacts pairs. The measurements were preformed with an Agilent® 4156C parameter analyzer. The measured characteristics are not perfectly superimposed because the distance between $C_1 - C_2$ and $C_4 - C_5$ is relatively small (3.2 μm). This is due to fabrication process dispersion and to package stress. The model was fitted to the corresponding average measurements by reducing the n-well maximum doping to $4.6 \cdot 10^{-16}\, cm^{-3}$.

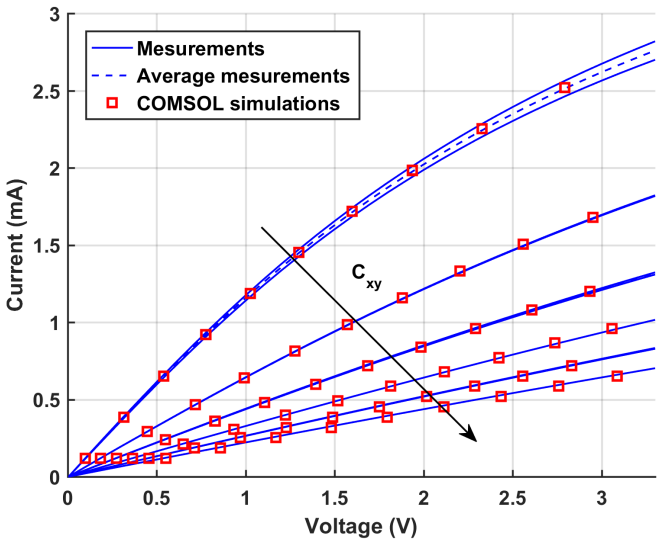


Figure 6.2 – I/V measurement and COMSOL simulations along each contacts pair combination. C_{xy} corresponds to the measurement between contacts x and y. In order of appearance, C_{xy} is respectively $C_1{-}C_2/C_4{-}C_5$, $C_2{-}C_3/C_3{-}C_4$, $C_1{-}C_3/C_3{-}C_5$, $C_2{-}C_4$, $C_1{-}C_4/C_2{-}C_5$, $C_1 - C_5$.

6.3 FEM SCT modeling

6.3.1 Principle

The Spinning Current Technique (SCT) principle to reduce the offset and 1/f noise has already been presented in section 4.2.1.2. We now apply it to the LV-VHD. Contacts C_2 and C_4 are shorted to form a four contacts device compatible with the SCT. The four corresponding biasing phases are presented in figure 6.3.

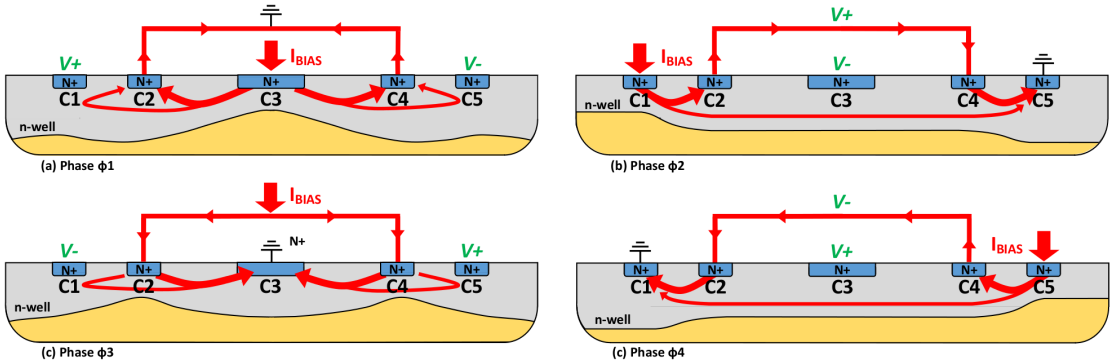


Figure 6.3 – Four-phases spinning current technique applied to the LV-VHD: (a) phase $\phi 1$, (b) phase $\phi 2$, (c) phase $\phi 3$, (d) phase $\phi 4$. The red arrows corresponds to the current flow. The green annotations denote the Hall voltage terminals. The shape of the voltage dependent depleted zone is represented in yellow.

In phase $\phi 1$, the current is injected from contact $C3$ to contacts $C2/C4$, while the Hall voltage is picked out between $C1$ and $C5$. This phase corresponds to the conventional biasing way of the LV-VHD, as applied in [33]. Phase $\phi 3$ is symmetric to phase $\phi 1$, but the current flow direction and the sign of the Hall voltage is inverted. In phase $\phi 2$, the current is injected from contact $C1$ to $C5$, while the Hall voltage is picked out on contacts $C3$ and $C24$. Finally, phase $\phi 4$ is symmetric to phase $\phi 2$, i.e. the current flow direction and the sign of the Hall voltage is inverted.

Figure 6.4 shows the simulated electric potential into the device of figure 6.1, with $550\,\mu A$ biasing current. The input resistance is not constant between phases $\phi 1/\phi 3$ and $\phi 2/\phi 4$ because of the asymmetrical structure of the LV-VHD. In phases $\phi 2/\phi 4$, $I_{24} = 550\,\mu A$ corresponds to the highest achievable biasing current, i.e. the current corresponding to the maximum biasing voltage applied to the transducer. Here, the maximum voltage corresponds to the difference between the maximum allowed supply voltage of the AMS $0.35\,\mu m$ process ($3.3\,V$) and the voltage drop across the current source. Here, the maximum biasing voltage is $V_{max} = 3\,V$. In phases $\phi 1/\phi 3$, the maximum biasing current is $I_{13} = 1100\,\mu A$. Therefore, considering the SCT biasing conditions as stated in section 4.2.1.2, the biasing current should be fixed to the lower value of either I_{13} or I_{24}, i.e. $I_{13} = I_{24} = 550\,\mu A$. Yet, as will be discussed later, alternative operating condition can be proposed.

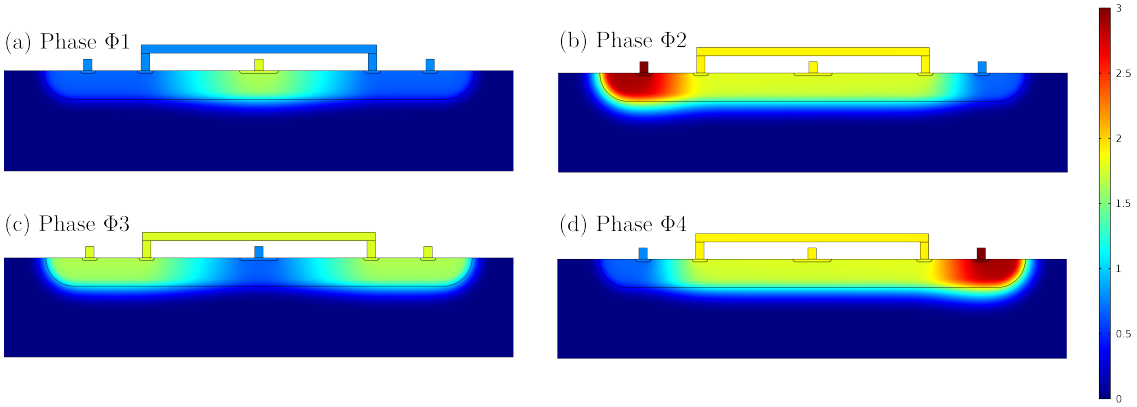


Figure 6.4 – Simulation of the electric potential with $550\,\mu A$ biasing current.

6.3.2 Offset

Figure 6.5 shows the output voltage $V_{out} = V_+ - V_-$ extracted from the simulations. The biasing current was swept from 0 to $550\,\mu A$ in each biasing phases.

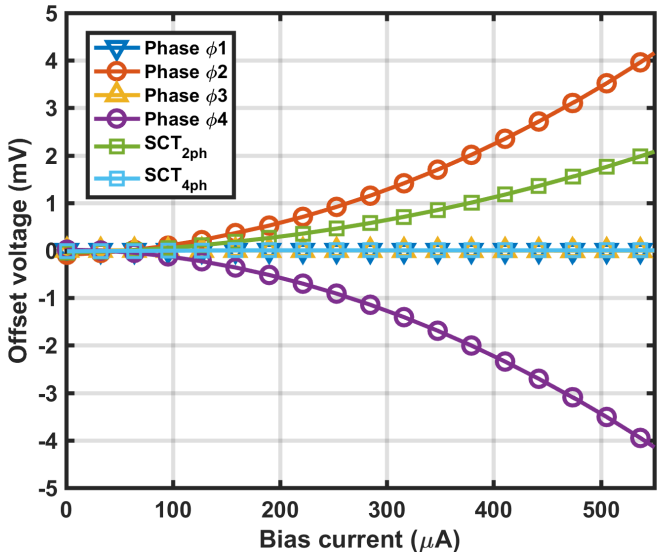


Figure 6.5 – LV-VHD simulated offset without misalignment.

The results are very similar to the ones proposed for the HV-VHD [48]. Considering a device with no fabrication imperfection or mechanical stress, there is no offset in phases $\phi 1/\phi 3$. On the contrary, phases $\phi 2/\phi 4$ exhibit quadratic offset due to the modulation of the depleted zone.

Figure 6.6 shows the simulated depleted zone density expressed as $\rho_V = q\,(N - n + p)$, where N is the doping profile, n the electron density, p the hole density.

In phases $\phi 1/\phi 3$, the depleted zone modulation is symmetrical with respect to the central contact $C3$. Since the output voltage is measured between $C1$ and $C5$, it is not affected by the depleted zone. In phases $\phi 2/\phi 4$, the depleted zone modulation is not symmetrical anymore

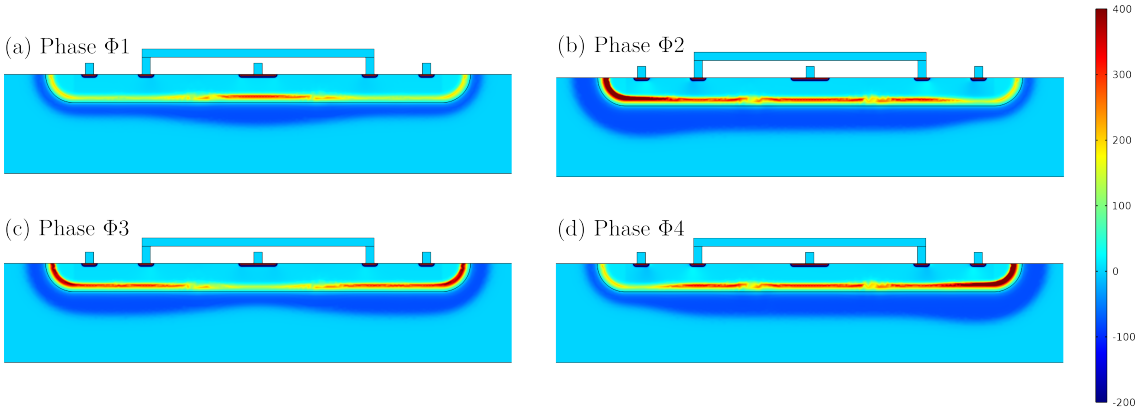


Figure 6.6 – Simulation of the depleted zone density in $C \cdot m^{-3}$ with $550\,\mu A$ biasing current.

and leads to systematic offset. Because of this non-linearity, the two-phase spinning current[1] does not remove efficiently the offset. We recall that, as demonstrated by Cornils and Paul [74], the offset of linear devices is completely removed by two-phase spinning current. Here, the LV-VHD is highly non-linear due to the asymmetry induced by the modulation of the depleted-zone (illustrated in figure 6.3). Figure 6.5 clearly shows that four phases are needed to remove the quadratic offset component.

In order to make the model more realistic, a random offset component was also added. Madec et al. [81] showed that the random offset may be modeled as an equivalent contact misalignment. According to this model, a shift of $100\,nm$ was applied on contact $C3$. The simulated offset is presented in figure 6.7.

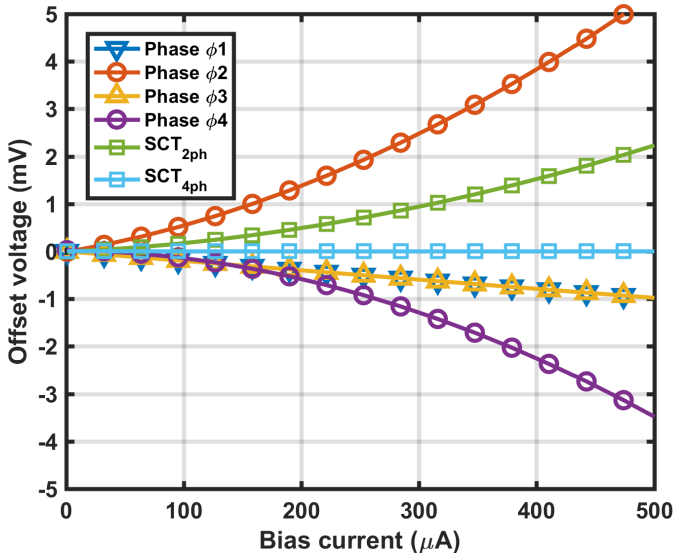


Figure 6.7 – LV-VHD simulated offset with $100\,nm$ shift applied on contact $C3$.

It appears that phases $\phi 1/\phi 3$ exhibit linear offset due to the contact shift. In phases

[1] Here $\phi 1/\phi 2$, but it also applies to $\phi 3/\phi 4$.

$\phi 2/\phi 4$, linear offset is respectively added or subtracted to the quadratic component. The same trend was observed on HV-VHD by Paul et al. [49]. Here also, four-phase spinning current is necessary to remove the offset. Therefore, only four-phase spinning current will be considered in the following chapters.

Chapter 7

LV-VHD Spinning current technique

The spinning current technique applied to the HHD has proven efficient to dramatically reduce its offset and 1/f noise [8, 32]. With the single-current (i.e. "conventional") SCT, the biasing current in all phases is kept constant. This technique is sub-optimal for the LV-VHD with non-constant input resistance. In this chapter we propose an analytical study dedicated to the single-current and the optimized bi-current SCT. We suppose that SCT completely removes the 1/f noise and offset (this assumption is discussed in chapter 8.1). Thus, in this chapter we consider resolution is limited by the sensitivity and thermal noise floor. We compare the efficiency of both SCT techniques through analytical methods.

7.1 Principle

A simplified LV-VHD linear resistive model is presented in figure 7.1.

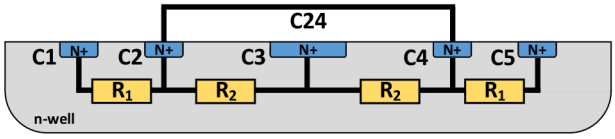


Figure 7.1 – Resistive model of the LV-VHD

According to this model, we can estimate the maximum biasing current in each phase. The maximum theoretical biasing currents in phases $\phi 1/\phi 3$ and phases $\phi 2/\phi 4$ are respectively called I_{13max} and I_{24max} . They are expressed by:

$$\begin{aligned} I_{13max} &= \frac{V_{supply}}{\frac{R_2}{2}} \\ I_{24max} &= \frac{V_{supply}}{2 \cdot R_1} \end{aligned} \tag{7.1.1}$$

Here, V_{supply} is the maximum supply voltage allowed by the technology, R_1 is the resistance of contact pairs $C1/C2$ and $C4/C5$, and R_2 is the resistance or contact pairs $C2/C3$ and $C3/C4$.

Assuming R_1 and R_2 have close values, $I_{24max} \simeq {}^{I_{13max}}/_{4}$, as stated in chapter 6, we must choose the smallest current, i.e. I_{24max}, in order to apply the conventional four phases single-current SCT. Since the Hall voltage is proportional to the biasing current (equation 4.1.1), i.e. $V_H = S_i \cdot I_{24max} \cdot B$, the single-current SCT dramatically limits the LV-VHD sensitivity and resolution. Therefore, it is not the most appropriate technique for LV-VHD operation.

7.2 Bi-current SCT

In a linear transducer the offset varies linearly with the biasing current and is reversed from phases $\phi1/\phi3$ to phases $\phi2/\phi4$ [8]. Considering a realistic device with non-linearities, the depleted zone modulation, represented in figure 6.3, engenders an asymmetry on phases $\phi2$ and $\phi4$, which leads to systematic offset. This offset varies quadratically with the biasing current and is reversed from phases $\phi2$ to $\phi4$ [49, 48]. In the analysis below, we will neglect the depleted zone effect because its related offset is removed with SCT.

In a linear device, the Hall voltage as well as the random offset, coming from fabrication imperfections, varies linearly with the biasing current [49, 48]. Thus, $V_{off} = R_{off} \cdot I$, with R_{off} introducing the current-related offset resistance. Furthermore, the 1/f noise may be considered as a slow-varying random offset. Its magnitude at the sensing contacts is also proportional to the biasing current [8]. Thus, $V_{1/f} = R_{1/f} \cdot I$ with $R_{1/f}$ introducing the current-related 1/f noise resistance.

The bi-current SCT consists of biasing the LV-VHD with the maximum biasing current in each phases, i.e. I_{13max} in phases $\phi1/\phi3$ and I_{24max} in phases $\phi2/\phi4$. The LV-VHD output voltage in phases $\phi1/\phi3$ and $\phi2/\phi4$ is thus:

$$\begin{aligned} V_{13}\left(I_{13max}\right) &= V_{13H} + V_{13off-1/f} + \sqrt{\langle V_{13th}^2 \rangle} \\ &= S_i \cdot I_{13max} \cdot B + \left(R_{off} \cdot I_{13max} + R_{1/f} \cdot I_{13max}\right) + \sqrt{\langle V_{13th}^2 \rangle} \end{aligned} \tag{7.2.1}$$

and

$$\begin{aligned} V_{24}\left(I_{24max}\right) &= V_{24H} + V_{24off-1/f} + \sqrt{\langle V_{24th}^2 \rangle} \\ &= S_i \cdot I_{24max} \cdot B - \left(R_{off} \cdot I_{24max} + R_{1/f} \cdot I_{24max}\right) + \sqrt{\langle V_{24th}^2 \rangle} \end{aligned} \tag{7.2.2}$$

Here, $\left\langle V_{xyth}^2 \right\rangle$ denotes the power spectral density of thermal noise in phase x or y, $V_{xyoff-1/f}$ denotes the addition of the offset with the flicker noise voltage in phase x or y.

Since the current is different between phases $\phi1/\phi3$ and $\phi2/\phi4$, the resulting modulated offset and 1/f noise voltage is no longer symmetric around $0\,V$. Therefore, in order to restore balance between all phases, the LV-VHD output voltage in phases $\phi2/\phi4$ has to be amplified by the current ratio called G_{max}:

$$G_{max} = \frac{I_{13max}}{I_{24max}} = \frac{4 \cdot R_1}{R_2} \tag{7.2.3}$$

The switched gain amplification restores the symmetry of the offset and 1/f noise voltage around 0V. Thus, the output voltages in phases $\phi1/\phi3$ and $\phi2/\phi4$ become:

$$\begin{aligned} V_{13-bi-SCT} &= V_{13}\left(I_{13max}\right) \\ V_{24-bi-SCT} &= G_{max} \cdot V_{24}\left(I_{24max}\right) \end{aligned} \tag{7.2.4}$$

Hence:

$$V_{24-bi-SCT} = S_i \cdot I_{13max} \cdot B - \left(R_{off} \cdot I_{13max} + R_{1/f} \cdot I_{13max}\right) + \sqrt{\left\langle V_{24th-bi-SCT}^2 \right\rangle} \tag{7.2.5}$$

with

$$\left\langle V_{24th-bi-SCT}^2 \right\rangle = G_{max}^2 \left\langle V_{24th-bi-SCT}^2 \right\rangle \tag{7.2.6}$$

The resulting voltage with bi-current SCT, called V_{bi-SCT} is obtained by averaging $V_{13-bi-SCT}$ and $V_{24-bi-SCT}$:

$$V_{bi-SCT} = S_i \cdot I_{13max} + \frac{\sqrt{\left\langle V_{13th}^2 \right\rangle} + \sqrt{\left\langle V_{24th-bi-SCT}^2 \right\rangle}}{2} \tag{7.2.7}$$

Equation 7.2.7 shows offset and 1/f noise voltage are removed by the bi-current SCT. As initially stated, one can notice that the resolution is only limited by the sensitivity and the thermal noise.

7.3 Resolution comparison

As discussed above, both single-current and bi-current SCT efficiently remove the offset and the 1/f noise voltage on a linear device. The following lines are dedicated to compare the efficiency of both techniques.

7.3.1 Single-current SCT

When applying SCT, each phase is picked out during one quarter of the spinning period. As a consequence, the contribution of each phase on the total thermal noise power a quarter of the thermal noise present on that phase.

On phases $\phi1/\phi3$, the resistance across the measurement contacts is $2 \cdot R_1$ (see figure 7.1). Therefore, the mean thermal noise power on phases $\phi1/\phi3$ is:

$$\left\langle V_{13th}^2 \right\rangle = \frac{1}{4} \cdot \left(4 \cdot k_B \cdot T \cdot \left(2 \cdot R_1\right) \cdot BW\right) = 2 \cdot k_B \cdot T \cdot R_1 \cdot BW \tag{7.3.1}$$

Here, BW corresponds to the system bandwidth, i.e. the cut-off frequency f_c of the low-pass filter (cf. section 4.2.1.2) if its order is high enough.

Similarly, the resistance across the measurement contacts, on phases $\phi2/\phi4$ is $R_2/2$. Thus,

the corresponding mean thermal noise power is given by:

$$\left\langle V_{24th-sc-SCT}^2 \right\rangle = \frac{1}{4} \cdot \left(4 \cdot k_B \cdot T \cdot \left(\frac{R_2}{2} \right) \cdot BW \right) = \frac{1}{2} \cdot k_B \cdot T \cdot R_2 \cdot BW \tag{7.3.2}$$

Here, notation $\left\langle V_{24th-sc-SCT}^2 \right\rangle$ denotes the single-current-SCT-related (sc-SCT) thermal noise.

Finally, after low-pass filtering, the mean thermal noise power $\left\langle V_{th-sc-SCT}^2 \right\rangle$ is obtained by summing each phase noise contribution:

$$\left\langle V_{th-sc-SCT}^2 \right\rangle = k_B \cdot T \cdot (4 \cdot R_1 + R_2) \cdot BW \tag{7.3.3}$$

Since the biasing current is limited to I_{24max}, the resolution (defined in section 3.3.1.4) yields:

$$\sigma_{sc-SCT} = \frac{\sqrt{k_B \cdot T \cdot (4 \cdot R_1 + R_2) \cdot BW}}{S_i \cdot I_{24max}} \tag{7.3.4}$$

7.3.2 Bi-current SCT

Concerning the bi-current SCT, the signal is picked out at the output of a switched gain amplifier. The gain is unitary on phases $\phi 1/\phi 3$ and equal to G_{max} on phases $\phi 2/\phi 4$. Assuming the amplifier noise is negligible compared to the transducer's noise[1], the mean thermal noise power on phases $\phi 1/\phi 3$ is the same whatever single-current or bi-current technique is used. However on phases $\phi 2/\phi 4$, the signal is amplified by the power gain G_{max}^2:

$$\left\langle V_{24th-bi-SCT}^2 \right\rangle = \left(4 \cdot \frac{R_1}{R_2} \right)^2 \cdot \left(\frac{1}{2} \cdot k_B \cdot T \cdot R_2 \cdot BW \right) \tag{7.3.5}$$

As previously stated, the output of the low pass-filter yields:

$$\left\langle V_{th-bi-SCT}^2 \right\rangle = k_B \cdot T \cdot \left(4 \cdot R_1 + \left(4 \cdot \frac{R_1}{R_2} \right)^2 \cdot R_2 \right) \cdot BW \tag{7.3.6}$$

The resolution of the LV-VHD operated with bi-current SCT thus becomes:

$$\sigma_{bi-SCT} = \frac{\sqrt{k_B \cdot T \cdot \left(4 \cdot R_1 + \left(4 \cdot \frac{R_1}{R_2} \right)^2 \cdot R_2 \right) \cdot BW}}{S_i \cdot I_{13max}} \tag{7.3.7}$$

This equation corresponds to a resolution improvement gained by the use of the bi-current technique given by:

$$\frac{\sigma_{bi-SCT}}{\sigma_{sc-SCT}} = \sqrt{\frac{R_2}{4 \cdot R_1}} = \frac{1}{\sqrt{G_{max}}} \tag{7.3.8}$$

The above result shows resolution improvement by a factor $\sqrt{G_{max}}$ when applying bi-current SCT instead of single-current SCT. It is always theoretically possible to increase G_{max} by adjusting the R_1/R_2 ratio. Yet, this increase, should not be performed to the detriment of the

[1] This is actually possible by using appropriate low-noise amplifier architecture.

maximum achievable current in phase $\phi 2/\phi 4$, since this might degrade the effective resolution. Indeed, for instance, increasing R_1 too much would lead to dramatically reduce I_{24max}, and thus lower the resolution. Notice that equation 7.3.8 is always true, i.e. whatever the value of the biasing current. Therefore, in order the achieve maximal resolution, the most efficient procedure consists in defining $R_1$and R_2 so as to maximize I_{24max} as would be done for single-current SCT.

At this point of the study it is important to notice that switched gain amplifier with extremely accurate gain ratio can be achieved with standard CMOS process. In practical implementation of the bi-current SCT, both biasing currents are delivered by current mirrors in order to ensure good control of the current ratio. Due to the voltage drop across these current mirrors, the maximum current as defined in equation 7.1.1 is not achievable. Therefore, I_{13max} and I_{24max} may be replaced by $I_{13} < I_{13max}$ and $I_{24} < I_{24max}$:

$$\begin{aligned} I_{13max} &= \frac{V_{supply}-V_{sat}}{\frac{R_2}{2}} \\ I_{24max} &= \frac{V_{supply}-V_{sat}}{2 \cdot R_1} \end{aligned} \tag{7.3.9}$$

Where V_{sat} is the lowest achievable voltage drop across the current mirror in order to keep the transistors in the saturation region.

Therefore, the current ratio becomes:

$$G = \frac{I_{13}}{I_{24}} \tag{7.3.10}$$

G could be set higher than G_{max}, for instance with $I_{24} \ll I_{24max}$ and $I_{13} \simeq I_{13max}$. But as stated above, this would again impact the effective resolution. As a consequence I_{13} and I_{24} should be chosen as high as possible, i.e. close to I_{13max} and I_{24max}, to get the best resolution.

Chapter 8

Concept validation

This chapter is dedicated to the presenting the FEM model and experimental results of the single and bi-current SCT applied to the LV-VHD. Special attention is given to the offset and 1/f noise.

8.1 FEM concept validation

In the following lines we explain how we used the FEM model proposed in chapter 6 to emulate the 1/f noise, and thus assess the efficiency of the SCT.

8.1.1 Noise simulation

According to the Hooge model [54] that applies to bulky devices such as the VHD, 1/f noise can be attributed to a quasi-static random variation of the carrier mobility, which is comparable to a slow-varying offset. Therefore, 1/f noise can be emulated by substituting the constant mobility by random mobility maps. From this point forward, a set of thirty linear interpolated random mobility maps was generated with a 0.1 % standard deviation around the nominal mobility $\mu_n = 1100\,cm^2/(V \cdot s)$. Figure 8.1 shows one sample of these thirty maps. The red areas correspond to high mobility, and the blue ones with low mobility. Simulations, using COMSOL® LiveLink® for MATLAB®, were performed on the same device as the one presented in section 6.3.1 (i.e. $3\,\mu m$ width LV-VHD presented in figure 6.1) for each of the thirty mobility maps in each phase. The voltage across the sensing contacts was then extracted.

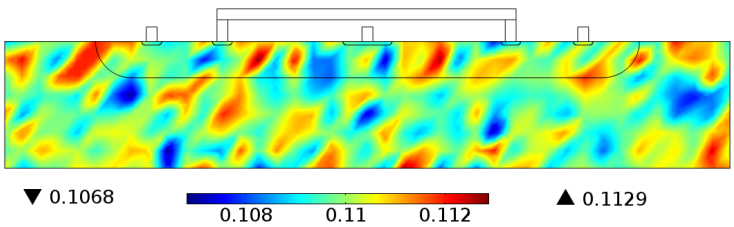


Figure 8.1 – One sample of the thirty random mobility map with $500\,nm$ step grid (in $m^2 \cdot V^{-1} \cdot s^{-1}$).

Due to the carrier velocity saturation, the highest achievable current in phases $\phi1/\phi3$ is around $1100\,\mu A$ while it is $550\,\mu A$ in phases $\phi2/\phi4$ (cf. section 6.3.1). In the considered device, $G = 2$.

Furthermore, the simulations were performed under different biasing configurations:

1. in single-current biasing mode, with $550\,\mu A$ constant biasing current and $1100\,cm^2 \cdot V^{-1} \cdot s^{-1}$ constant mobility. This configuration is necessary in order to assess computation-accuracy-related residual offset is negligible. The transducer output voltage is amplified by G to normalize the signal in all simulations.

2. in single-current biasing mode, with $550\,\mu A$ constant current and random mobility maps, in order to assess the single-current SCT. The output voltage is also amplified by G.

3. in bi-current biasing mode, with $1100\,\mu A$ biasing current in phases $\phi1/\phi3$, and $550\,\mu A$ in phases $\phi2/\phi4$, in order to assess the bi-current SCT. The transducer output voltage on phases $\phi2/\phi4$ is multiplied by G.

8.1.2 Simulations results

From configuration 1, the computation accuracy was estimated to $5.53\,nV$. This value is related to the $COMSOL^{®}$ convergence criteria, which had been set to 10^{-91}. This is three decades below the device's actual residual noise extracted from configurations 2 and 3.

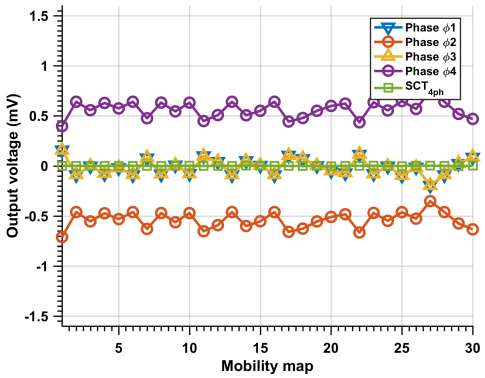
The simulated transducer output voltage is shown without amplification (figure 8.2a), and with amplification by gain G on each phase (figure 8.2b).

Considering these results, the noise level is the same on all phases. It appears also that on phases $\phi2/\phi4$, the 1/f noise is superimposed with the systematic offset due to the modulation of the depleted zone (cf. section 6.3.2). We can also notice the symmetry of the 1/f noise between phases $\phi1/\phi2$ and $\phi3/\phi4$. Therefore, two-phase SCT could be used to reduce the 1/f noise but the offset still remains relatively high. These observations apply for both the transducer's output and after amplification because the gain is the same on all phases.

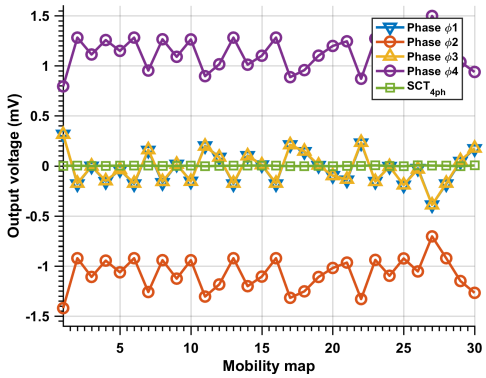
Things are not quite the same when considering bi-current SCT. Indeed, before amplification (figure 8.2c), the noise level on phases $\phi1/\phi3$ is higher than for single-current SCT. This is due to the higher biasing current, which is two times higher in theses phases (cf. section 3.3.1.3). Note that the offset and noise remain unchanged in phases $\phi2/\phi4$, since the biasing current is the same as for single-current SCT. Yet, after switched -amplification (figure 8.2d), the noise level appears similar to the single-current SCT configuration. Nevertheless, in order to quantify the 1/f noise cancellation efficiency of the bi-current SCT, standard deviation has been computed, first on each phase of the thirty output voltages individually, and then on the average. All these results are presented in table 8.1.

As expected, the 1/f noise level linearly varies with the biasing current [49, 48]. Thus, as can be seen on table 8.1, the noise is the same whatever the biasing current/gain couple used.

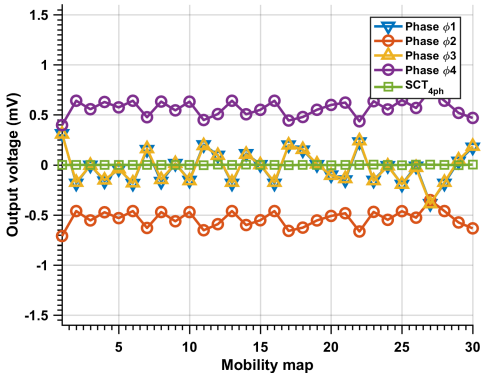
[1]The convergence criteria defines the acceptable simulation error.



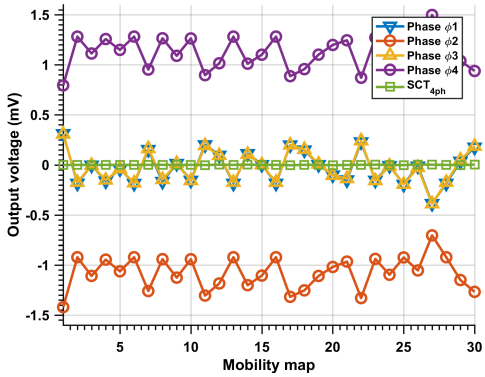
(a) Simulated single-current SCT at the transducer output.



(b) Simulated single-current SCT with amplification.



(c) Simulated bi-current SCT at the transducer output.



(d) Simulated bi-current SCT with switched gain amplification.

Figure 8.2 – Simulated noise.

Mode	I_{bias} (μA)	Gain	Output noise standard deviation (μV)
Phase ϕ1	550	2	165.6
	1100	1	166.3
Phase ϕ2	550	2	166.4
Phase ϕ3	550	2	164.7
	1100	1	166.1
Phase ϕ4	550	2	166.1
Single-current SCT	550	2	1.3
Bi-current SCT	825 (average current)	2 with ϕ2/ϕ4, 1 with ϕ1/ϕ3	1.7

Table 8.1 – Noise standard deviation

For both modes the 1/f is drastically reduced by a ratio around 100. One can thus safely assess that the LV-VHD resolution is almost only limited by the thermal noise with either single-current or bi-current mode.

The residual noise of the bi-current SCT ($1.7\,\mu V$) is slightly higher than for single-current SCT ($1.3\,\mu V$), which could make appear single-current SCT more interesting than bi-current SCT. Nevertheless, as demonstrated in chapter 7, one should keep in mind that the thermal noise/sensitivity ratio is much better for the bi-current SCT. Therefore, the bi-current SCT stands for the most appropriate technique to achieve best resolution of an LV-VHD.

8.2 Experimental validation

The single-current and the bi-current SCT was implemented on a LV-VHD fabricated in AMS $0.35\mu m$ standard CMOS technology.

8.2.1 Instrumental chain

For this prototype, we used the same $3\,\mu m$ width LV-VHD as the one considered in section 6.1.2 (cf. figure 6.1). The LV-VHD is co-integrated with two current sources in order to provide $I_{min} = 550$ and $I_{max} = 1100\,\mu A$ biasing currents. These current sources are externally trimmed by I_{ext}. The switch box allows to select the appropriate single or bi-current biasing. Although, amplification can easily be integrated together with the LV-VHD on the same chip[2], for experimentation purpose, it is achieved by an external switched gain instrumentation amplifier (IA). For the single-current SCT the gain is fixed to 200 and for the bi-current SCT it switches from 100 to 200. An FPGA[3] provides the different $10\,kHz$ clock signals needed for single and bi-current SCT. A schematic view of the system is proposed in figure 8.3.

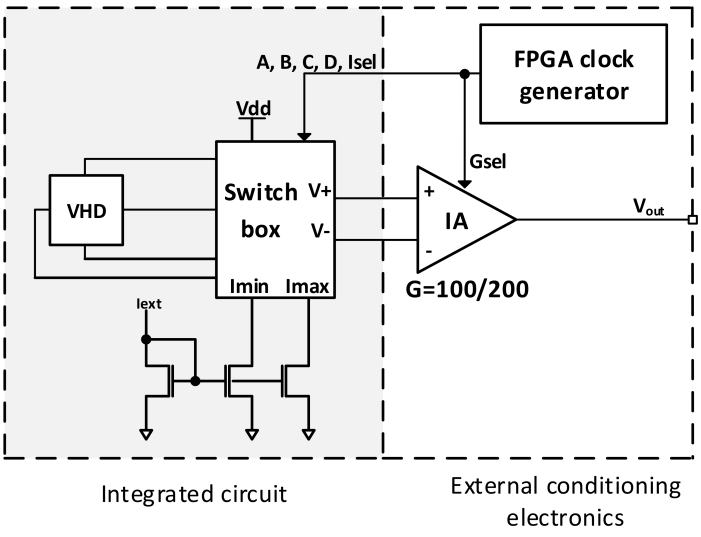


Figure 8.3 – Schematic view of the LV-VHD experimental system.

[2]Accurate gain ratio can be achieved by using common-centroid topology resistors.This is a major advantage of standard CMOS technology.

[3]FPGA: Field-Programmable Gate Array.

The switch box (figure 8.4) achieves SCT modulation and demodulation according to the switching pattern proposed in table 8.2.

	C1	C24	C3	C5
phase $\phi 1$	$V+$	I_{min}	Vdd	$V-$
phase $\phi 2$	Vdd	$V+$	$V-$	I_{min}
phase $\phi 3$	$V-$	Vdd	I_{min}	$V-$
phase $\phi 4$	I_{min}	$V-$	$V+$	Vdd

(a)

	C1	C24	C3	C5
phase $\phi 1$	$V+$	I_{max}	Vdd	$V-$
phase $\phi 2$	Vdd	$V+$	$V-$	I_{min}
phase $\phi 3$	$V-$	Vdd	I_{max}	$V-$
phase $\phi 4$	I_{min}	$V-$	$V+$	Vdd

(b)

Table 8.2 – LV-VHD (a) single-current and (b) bi-current switching pattern. C1 to C5 are the LV-VHD contacts. $V+$ and $V-$ are the positive and negative integrated circuit outputs.

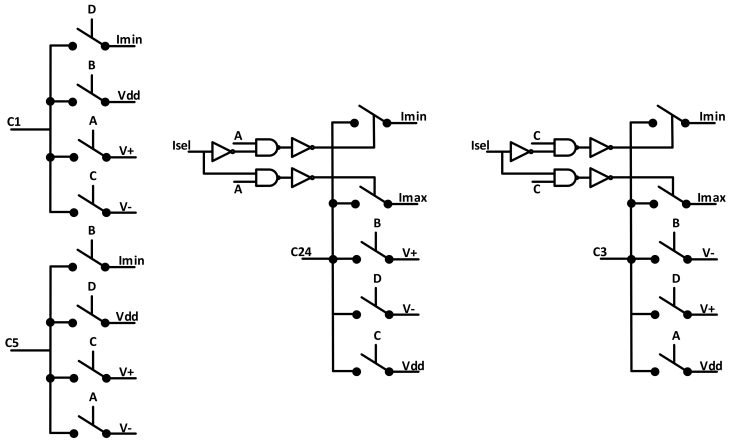
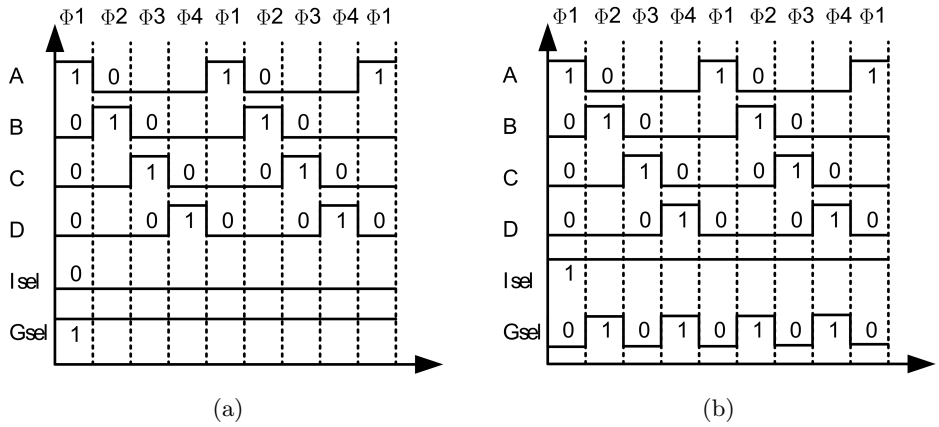


Figure 8.4 – Single-current and bi-current switch box. A, B, C, D and $Isel$ are the SCT clocks.



(a) (b)

Figure 8.5 – (a) Single-current and (b) bi-current SCT clocking sequence.

The single or bi-current mode is selected by $Isel$ terminal and the amplifier gain by $Gsel$. When single-current mode is selected the biasing current is set to $I_{min} = 550\,\mu A$. Conversely,

when the bi-current mode is selected the current switches from $I_{min} = 550\,\mu A$ in phases $\phi 2/\phi 4$ to $I_{max} = 1100\,\mu A$ in phases $\phi 1/\phi 3$. The SCT clocking sequence is presented in figure 8.5.

8.2.2 Experimental setup

The experimental setup is presented in figure 8.6.

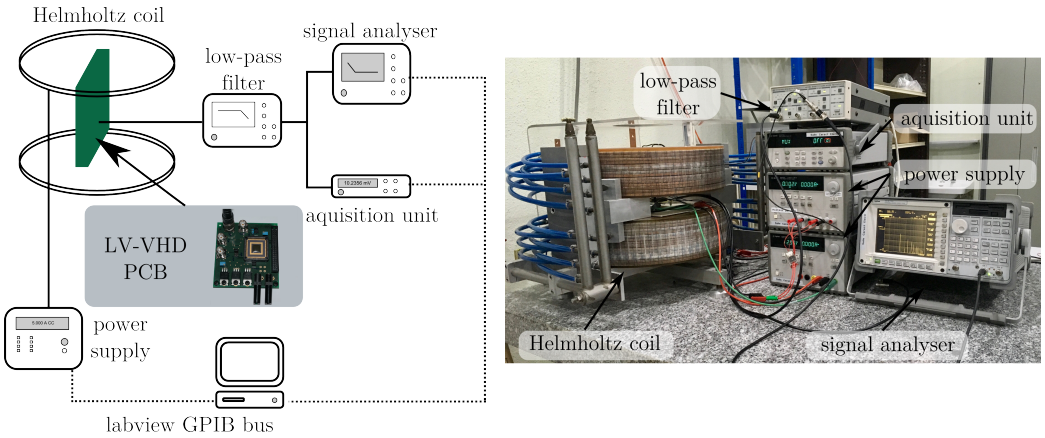


Figure 8.6 – (a) Block diagram and (b) picture of the experimental setup.

Sensitivity measurements are performed by mean of calibrated[4] Helmholtz coil ($1.227 \cdot 10^{-3}\,T/A$). The coil is driven by a power supply (Agilent® 3631A) in short-circuit mode. The demodulated output voltage is low-pass filtered by a low-noise configurable Stanford® filter. It is configured in second-order low-pass filter with $3\,kHz$ cut-off frequency. The filtered voltage is digitized by a data acquisition unit (Agilent® 34970A/34901A). Noise measurements are performed by a dynamic signal analyzer (Agilent® 35670A). The power spectral density is used to calculate the total noise over a $[5\,Hz - 1.6\,kHz]$ bandwidth, which is the reference bandwidth used in many publications dedicated to the HHD and the VHD [58, 82, 33]. The whole test bench is controlled by a labVIEW® interface in order to perform automatic measurement.

8.2.3 Experimental results

The measured biasing currents are $I_{min} = 554\,\mu A$ and $I_{max} = 1101\,\mu A$.

Figure 8.7a shows the system's offset as a function of the LV-VHD biasing current in single-current mode. One should notice that, except for the gain of the instrumentation amplifier, the results are very similar to FEM simulation. This proves once again the necessity to apply four-phase SCT in order to efficiently remove the offset. Figure 8.7b shows the system's offset as a function of the LV-VHD biasing current in bi-current mode.

Figure 8.7c shows the transfer characteristic of the system. The red line represents the linear regression used to extract the absolute sensitivity. As can be seen on table 8.3, due to

[4]Nanotesla accuracy.

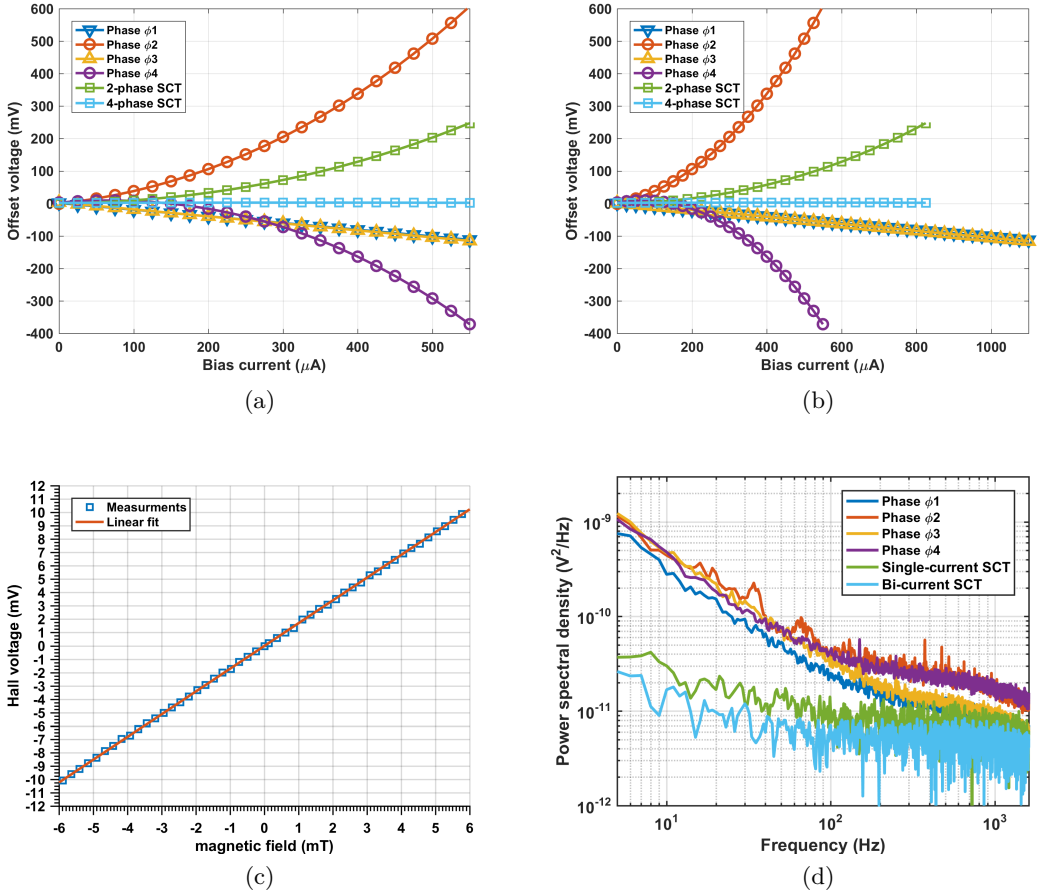


Figure 8.7 – VHDspin2 microsystem measurement results: (a) Single-current offset as a function of the biasing current. (b) Bi-current offset as a function of the biasing current (average current in two-phase and four-phase SCT). (c) LV-VHD-based sensor system transfer characteristic (bi-current SCT). The offset is mathematically nullified. For visibility purpose, only one point out of five is printed. (d) Power spectral density. The $50\,Hz$ harmonics have been mathematically suppressed.

the gain switching, the sensitivity remains almost the same (1.65 to $1.72\,V/T$)[5] whatever the considered phase or SCT mode.

Figure 8.7d shows the output power spectral density according to the different biasing modes.

It comes as no surprise that 1/f noise prevails in phase ϕ1 to ϕ4 (i.e. without SCT). We also notice that the noise level is higher in phases ϕ2/ϕ4 compared to phases ϕ1/ϕ3. This difference is neither due to thermal noise (which by the way is higher in phases ϕ1/ϕ3 than ϕ2/ϕ4, cf. section 7.1), nor is it related to 1/f noise of the transducer (which should be equivalent on every phase according to FEM simulations, cf. section 8.1). Actually, the difference is due to the 1/f noise contribution from the biasing current source. Let's remind that phases ϕ2/ϕ4 suffer from quadratic systematic offset coming from the depleted zone modulation. In addition, all phases have linear random offset. These offsets, which vary with

[5]The difference is due to 1/f noise.

the biasing current, are modulated by the 1/f noise of the current source and thus increase the noise levels. As shown in figure 8.7a, the amplitude of the offset in phases $\phi 2/\phi 4$ is higher than in phases $\phi 1/\phi 3$. Therefore, this noise related to offset-modulation is higher in phases $\phi 2/\phi 4$ than in $\phi 1/\phi 3$. One usually admits that the common mode noise of transducers or amplifiers is rejected and does thus not affect the output signal. This assumption is actually wrong if the offset is not negligible. Fortunately this low-frequency noise, is considered as a slow time-varying offset and can therefore be removed by four-phase single or bi-current SCT[6].

Concerning the single and bi-current SCT, we observe that both techniques are efficient to remove the 1/f noise. According to the theory, at the output of the instrumental chain, the thermal noise floor is lower with bi-current SCT. The remaining 1/f noise comes from the relatively low spinning frequency used, i.e. $10\,kHz$, which was chosen because of the limited bandwidth of the external amplifier. It can easily be increased by using an ad-hoc integrated switched gain amplifier.

The microsystem achieves $64\,\mu T$ and $51\,\mu T$ resolution respectively with the single-current and bi-current SCT over $[5\,Hz - 1.6\,kHz]$ bandwidth. This corresponds to 20 % resolution improvement. Theoretically, the resolution ratio should be equal to $1/\sqrt{G} = \sqrt{554/1101} \simeq 0.7$, corresponding to 30 % resolution improvement. This is due to the fact that the actual maximum achievable current in phases $\phi 1/\phi 3$ has been underestimated in the model. Experiments showed that I_{max} should be about $1300\,\mu A$ instead of $1100\,\mu A$.

Table 8.3 gathers the measurement results.

[6]Under the condition that the SCT frequency is higher than the 1/f noise corner frequency.

Mode	I_{bias} (μA)	Gain	Sensitivity (V/T)	Offset (mV)	Offset (mT)	Output noise (μV_{RMS})	Resolution (μT)
Phase $\phi 1$	554	200	1.72	−111.9	−65.1	221	128
	1101	100	1.66	−112.7	−67.9	154	90
Phase $\phi 2$	554	200	1.65	607.1	368.0	213	129
Phase $\phi 3$	554	200	1.67	−115.1	−68.9	233	139
	1101	100	1.65	−116.7	−70.7	174	105
Phase $\phi 4$	554	200	1.70	−371.9	−218.7	206	121
Sc-current	554	200	1.68	3.1	1.8	107	64
Bi-current	828	200 with $\phi 2/\phi 4$, 100 with $\phi 1/\phi 3$	1.67	2.7	1.6	82.2	51

Table 8.3 – Summary of the experimental results.

Chapter 9

Conclusion on the LV-VHD

This part was dedicated to the study of the LV-VHD (Vertical Hall Device suited for low-voltage CMOS process) and its offset and 1/f noise reduction techniques. The LV-VHD is a magnetic transducer sensitive to the magnetic field in the plane of the chip.

Chapter 6 was dedicated to present a 2D FEM COMSOL® model, which was experimentally validated. The model was used to evaluate the offset reduction with two-phase and four-phase SCT. Results confirm that 4-phase SCT is necessary to remove efficiently the offset.

In chapter 7, we presented bi-current SCT. This technique allows to operate the LV-VHD at the highest achievable biasing current whatever its phase. Theoretical analysis has shown that bi-current SCT dramatically improves the resolution of the LV-VHD compared to single-current SCT.

Chapter 8, was dedicated to validate the single and bi-current SCT through FEM simulations and experiments. As expected, best performance is achieved by bi-current SCT, with no less than $51\,\mu T$ resolution over $[5\,Hz - 1.6\,kHz]$ bandwidth and $1.6\,mT$ residual offset.

Based on the simulation tool proposed in this work, one should consider LV-VHD optimization within the framework of the further bi-current SCT study. Even though VHD transducers will never compete with HHD transducers in terms of performances, because of their intrinsic technology-related limitations [65], we are yet convinced there is still room for improvement. Indeed, according to our estimations, around $25\,\mu T$ resolution should be achieved with a $6\,\mu m$-wide LV-VHD [83] operated with bi-current SCT. Also, integrating the switched gain amplification together with the LV-VHD and its switch box on the same chip should help dramatically reducing residual offset.

Part III

CHOPFET

Chapter 10

Introduction on the CHOPFET

This introduction aims at laying the foundation of the CHOPFET, and the SCT adapted to this current-mode transducer.

Chapter 11 addresses the questions related to the CHOPFET transducer's design and optimal implementation. This comes in an extensive study of 2D and 3D FEM models, biasing modes and temperature behavior.

Finally, in chapter 12, we investigate on the CHOPFET's conditioning electronics. We present an improved version, with fully differential output, of the concept introduced by Vincent Frick in 2010 [82]. A new architecture, based on a Magnetic Operational Amplifier (MOP) to provide a low-noise functionalizable instrumental chain, is proposed.

10.1 CHOPFET principle

A split-drain MagFET (cf. section 4.1.3) is a current-mode transducer based on a MOS transistor with one source and at least two drains. Several MagFET shapes have been proposed (rectangular [84, 85, 86], circular [3],...) but only the rectangular one, illustrated in figure 10.1a, respects the design rules of most standard CMOS processes. While its principle has been known for decades[31], it never really hit the magnetic field sensors market because it suffers from noise and offset issues. Indeed, the nature of its active region (i.e. inversion channel of a MOS transistor), located at the $Si-SiO_2$ interface, is the home of many defects, which leads to high 1/f noise level [55]. Furthermore, this transducer is very sensitive to process variations (masks misalignment, doping inhomogeneity...), which induces high current imbalance between the drains, leading to random offset [8]. Even though noise and offset may be minimized by increasing the transducer's surface, they still limit the low-frequency performances of the MagFET.

As previously developed, the SCT is a good solution to remove the 1/f noise and the offset of Hall devices. A first attempt to adapt the SCT to current-mode transducers was proposed by Doyle [87]. He proposed to use an octal ring MagFET, symmetrical by rotation. Un-

fortunately, this unconventional asymmetrical shape greatly limits geometrical optimization (width/length ratio), which is yet a major feature in CMOS transistor-based analog design.

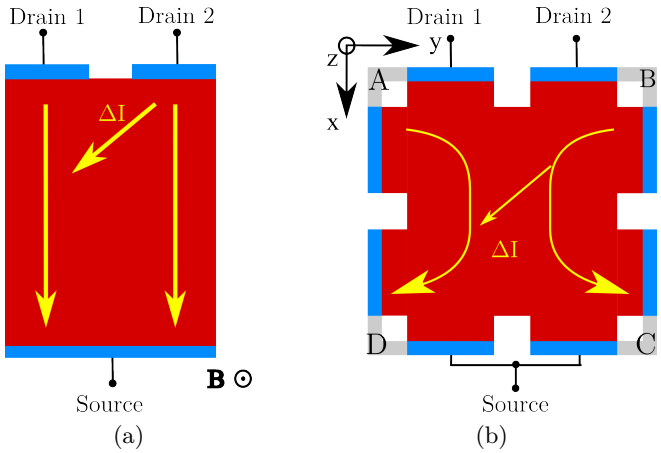


Figure 10.1 – View of (a) a MagFET and (b) a CHOPFET transducer

Frick et al. proposed a new MagFET shape, called CHOPFET, presented in figure 10.1b [82]. This new structure is compatible with the SCT and standard CMOS process. It is based on the superimposition of four MOS transistors arranged in two parallel pairs crossing each other in order to form a pattern inscribed in a square [82]. The two perpendicular n+ wells are linked to form a four contacts transducer (A, B, C and D). In the example of figure 10.1b, contacts A and B are the split drains, while contacts C and D are shorted to form the source. One can thus create four identical perpendicular MagFET by adequate interconnection.

10.2 Application of the SCT to the CHOPFET

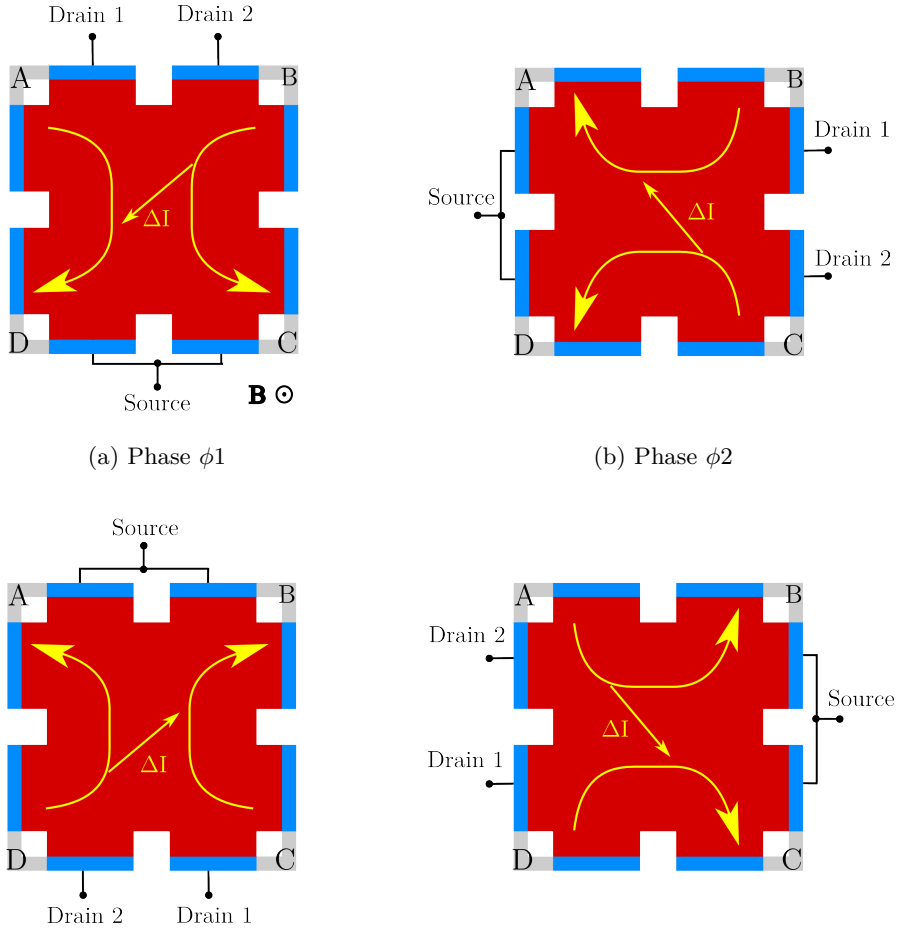
The CHOPFET is a current mode transducer (i.e. the output signal is a current). It can yet be understood by the fact that MagFET transducers are based on current imbalance (i.e. between the drains). Even though one could intuitively expect that the spinning current technique also applies to current mode transducers, this statement is yet not obvious and has never been addressed before in literature. Therefore, we propose to further investigate this topic.

Figure 10.2 shows the CHOPFET in its four biasing phases. For instance in phase $\phi 1$ (figure 10.2a), the source is obtained by shorting contacts C and D. The output signal is the difference between the currents in drain 1 and drain 2:

$$\Delta I_{\phi i} = I_{D1} - I_{D2} \tag{10.2.1}$$

where i corresponds to the phase. Thus, $\Delta I_{\phi 1} = I_A - I_B$ in phase 1, and similarly, $\Delta I_{\phi 2} = I_B - I_C$, $\Delta I_{\phi 3} = I_C - I_D$ and $\Delta I_{\phi 4} = I_D - I_A$ for respectively phase $\phi 2$ to $\phi 4$.

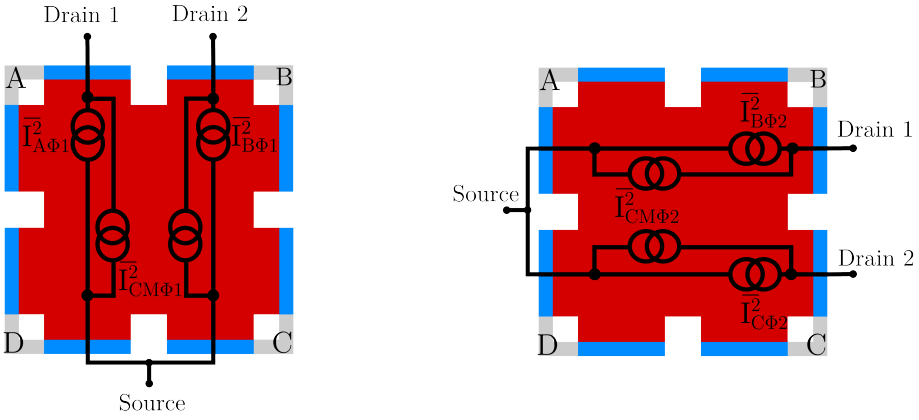
Figure 10.3 shows the CHOPFET noise model in phases $\phi 1$ and $\phi 2$. The spinning current is dedicated to 1/f noise reduction, thus for this analysis we neglect the thermal noise contribution. Note that the technique to minimize the thermal noise is discussed in section 11.3.



(a) Phase $\phi 1$ (b) Phase $\phi 2$

(c) Phase $\phi 3$ (d) Phase $\phi 4$

Figure 10.2 – Spinning current technique applied to the CHOPFET.



(a) (b)

Figure 10.3 – CHOPFET noise model on (a) phase $\phi 1$ and (b) phase $\phi 2$.

Lets introduce the 1/f noise current power spectral densities $\overline{I^2_{D1\phi i}}$ and $\overline{I^2_{D2\phi i}}$ corresponding to drain 1 and drain 2 in phase i. They can be separated into two noise contributions: the common mode noise $\overline{I^2_{CM\phi i}}$ and the uncorrelated noise associated to each contact ($\overline{I^2_{A\phi i}}$, $\overline{I^2_{B\phi i}}$, $\overline{I^2_{C\phi i}}$ and $\overline{I^2_{D\phi i}}$). The common mode and uncorrelated noise distribution vary with the transducer operating point [88].

For instance, in phase $\phi 1$, $\overline{I^2_{D1\phi 1}}$ and $\overline{I^2_{D2\phi 1}}$ are given respectively by:

$$\overline{I^2_{D1\phi 1}} = \overline{I^2_{CM\phi 1}} + \overline{I^2_{A\phi 1}} \tag{10.2.2}$$

$$\overline{I^2_{D2\phi 1}} = \overline{I^2_{CM\phi 1}} + \overline{I^2_{B\phi 1}} \tag{10.2.3}$$

$\overline{I^2_{A\phi 1}}$ and $\overline{I^2_{B\phi 1}}$ are totally uncorrelated noise contributions from contacts A and B (during phase $\phi 1$). Any correlation between these contacts is rejected to $\overline{I^2_{CM\phi 1}}$. This common mode noise is assumed to be totally removed by differential measurement. [1]. As for $\overline{I^2_{A\phi 1}}$ and $\overline{I^2_{B\phi 1}}$, these uncorrelated noise contributions are removed by SCT according to the following analysis.

At time t, the current differences in phase $\phi 1$ and $\phi 2$, are given by:

$$\Delta I_{\phi 1}(t) = I_{A\phi 1}(t) - I_{B\phi 1}(t) \tag{10.2.4}$$

$$\Delta I_{\phi 2}(t) = I_{B\phi 2}(t) - I_{C\phi 2}(t) \tag{10.2.5}$$

where $I_{A\phi 1}(t)$, $I_{B\phi 1}(t)$ contain the current noise contribution of contacts A and B in phase $\phi 1$. And $I_{B\phi 2}(t)$, $I_{C\phi 2}(t)$ are the current noise contribution of contacts B and C in phase $\phi 2$. When the CHOPFET is alternatively switched between phase $\phi 1$ and $\phi 2$, the average current difference corresponds to:

$$\Delta I_{\phi 1/\phi 2}(t) = \frac{\Delta I_{\phi 1}(t) + \Delta I_{\phi 2}(t)}{2} = \frac{1}{2} \cdot (I_{A\phi 1}(t) - I_{B\phi 1}(t) + I_{B\phi 2}(t) - I_{C\phi 2}(t)) \tag{10.2.6}$$

As discussed in section 12.1.2, $I_{B\phi 1}(t)$ and $I_{B\phi 2}(t)$ are related to the same contact and are thus highly correlated. Therefore, these noise currents are removed[2] and $\Delta I_{\phi 1/\phi 2}(t)$ becomes:

$$\Delta I_{\phi 1/\phi 2}(t) = \frac{1}{2} \cdot (I_{A\phi 1}(t) - I_{C\phi 2}(t)) \tag{10.2.7}$$

This means the 1/f noise contribution of the common contact is removed by switching from one phase to the next. One may conclude that n-phase SCT is necessary to remove the 1/f noise for an n-contact current mode transducer[3].

This introduction, dealing with CHOPFET's 1/f noise and the way to deal with, shows the validity of the following extensive study dedicated to this promising device. The CHOPFET is, above all, a transistor, which is inserted in a electronic circuit. Thus, we first need to investigate on its dimensioning and implementation, as presented in the next chapter.

[1] Of course it is also the case of $\overline{I^2_{A\phi i}}$, $\overline{I^2_{B\phi i}}$, $\overline{I^2_{C\phi i}}$ and $\overline{I^2_{D\phi i}}$, which are totally uncorrelated.

[2] I.e. up to the SCT frequency.

[3] One should notice that this reasoning also applies to the offset, according to the FEM simulations proposed by Heidari [17, 89].

Chapter 11

CHOPFET behavior

This chapter is dedicated to the extensive study of the CHOPFET transducer. Previous studies have investigated the effect of the MagFET parameters on its sensitivity [90, 91, 85]. Nevertheless, some contradictions appears in the conclusions [88]. Xinyu [90] and Ning [91] reported that the sensitivity is higher for square shaped MagFET, while Kluge [85] noted that the sensitivity increases with respect to the L/W ratio. The purpose of this chapter is to deeply explore the CHOPFET behavior by means of FEM simulations and experimental measurements.

The MagFET is a transistor. Therefore, its electrical behavior is ruled by standard FET[1] transistors laws [38]. In a first time, based on the state of the art, we rapidly built a 2D COMSOL® FEM model limited to the MagFET linear region[2]. Previous studies reported that the MagFET has best sensitivities in linear region [60, 85] but the CHOPFET's geometry differs from the conventional MagFET. Thus, in a second time, we proposed an improved 3D COMSOL® FEM model dedicated to the CHOPFET.

11.1 2D FEM model

The CHOPFET's channel is modeled by an equivalent resistive plate. The modeling principle was already presented in chapter 6. The constant mobility is replaced by a an anisotropic mobility tensor in order to model the effect of the magnetic field. In order to simplify the analysis, lets assume the magnetic field is oriented perpendicularly to the CHOPFET and its value is sufficiently low to neglect the physical-magnetoresistive effect (i.e. $B_z < 2.89\,T$, $B_x = B_y = 0\,T$, cf. section 2.1.1.1). Appendix B.3 contains the detailed calculations[3] Therefore, the anisotropic mobility tensor is expressed as:

$$\mu_n\left(B_z\right) = \begin{pmatrix} \mu_n \cdot E_x + \left(-\mu_n^2 \frac{\langle\tau^2\rangle}{\langle\tau\rangle^2} B_z\right) E_y \\ \left(\mu_n^2 \frac{\langle\tau^2\rangle}{\langle\tau\rangle^2} B_z\right) E_x + \mu_n \cdot E_y \end{pmatrix} \tag{11.1.1}$$

[1] FET: Field Effect Transistor.

[2] $V_{DS} \ll V_{DSsat}$

[3] The z-axis is not taken into account in this 2D model. Thus, the electric field along this axis is neglected.

with E_x and E_y are the electric fields along x and y, and $\langle\tau^2\rangle/\langle\tau\rangle^2 = r_{Hn}$ is the Hall scattering factor in the channel, set to 0.8 [84]. In the following analysis, the galvanomagnetic effects on the holes are neglected since magnetic transducers are generally based on n-type active zones. Let us recall that according to equation 6.1.1, in a semiconductor magnetic transducer, the electron and hole current densities (respectively $\mathbf{J_n}$ and $\mathbf{J_p}$) based on the conduction and diffusion mechanisms are given by:

$$\begin{cases} \mathbf{J_n}\left(B_z\right) = -q \cdot n \cdot \mu_n\left(B_z\right) \cdot \boldsymbol{\nabla}\psi + q \cdot D_n\left(B_z\right) \cdot \boldsymbol{\nabla} n \\ \mathbf{J_p} = -q \cdot p \cdot \mu_p \cdot \boldsymbol{\nabla}\psi - q \cdot D_p \cdot \boldsymbol{\nabla} p \end{cases} \tag{11.1.2}$$

where $D_n\left(B_z\right)$ and D_p represents respectively the electrons' diffusivity tensor and the holes' diffusivity. To ensure balance between the conduction/diffusion mechanisms, we need to modify the Einstein diffusivity-mobility equation as a function of the mobility tensor:

$$D_n(B_z) = {}^{k \cdot T}/_{q} \cdot \mu_n(B_z) \tag{11.1.3}$$

11.1.1 Validation on a standard MagFET

The model was first tested on a rectangular MagFET shape presented in figure 11.1a. The n+ contacts and the channel are respectively modeled by a constant doping level of $10^{19}\,cm^{-3}$ and $10^{17}\,cm^{-3}$. The biasing current was arbitrary fixed to $150\,\mu A$. Figure 11.1b shows the electric potential simulation[4]. In the results presented in figure 11.2, the MagFET has been simulated with $5\,mT$ magnetic field and various conditions: (a) with a constant width W and different lengths L, (b) with a constant L and different W, (c) W and L fixed and different drain notches d. The effect of H_o, which denotes the gap depth, has also been investigated.

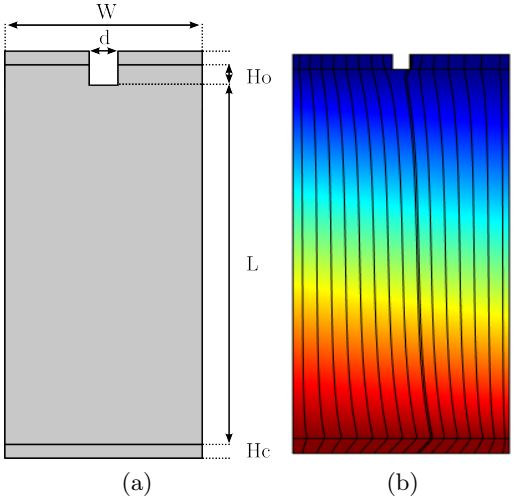


Figure 11.1 – 2D MagFET (a) geometry and (b) electric potential and current density lines with $B_z = 5\,T$. Here, H_o is set to $0\,\mu m$. For display purpose, an unrealistic high value of the magnetic field was chosen in order to highlight the current deflection.

Figures 11.2a and 11.2b show the simulated current-related sensitivity as a function of the

[4]For display purpose, an unrealistic high value of the magnetic field was chosen in order to highlight the current deflection

channel length L and width W, while the drain gap distance d is kept constant at 1 μm. The sensitivity increase is sharper with W small, and reaches the highest value when $L/W > 2$. According to these simulations, L should be as long as possible to achieve maximum sensitivity.

Figure 11.2c shows that the relative sensitivity decreases linearly with the drain gap width d. Here, the length and the width are kept constant, to 50 μm and 25 μm respectively. The optimal MagFET parameters, in terms of current-related sensitivity, are $L/W > 2$ and d as small as possible. Furthermore, figure 11.2d also shows that the drain depth H_o does not affect the sensitivity. This can be easily understood since this parameter has no impact on the magnetically active region (i.e. the region where the current deflection occurs). These results are consistent with previous studies based on analytical modeling [85] and 3D FEM simulation [84].

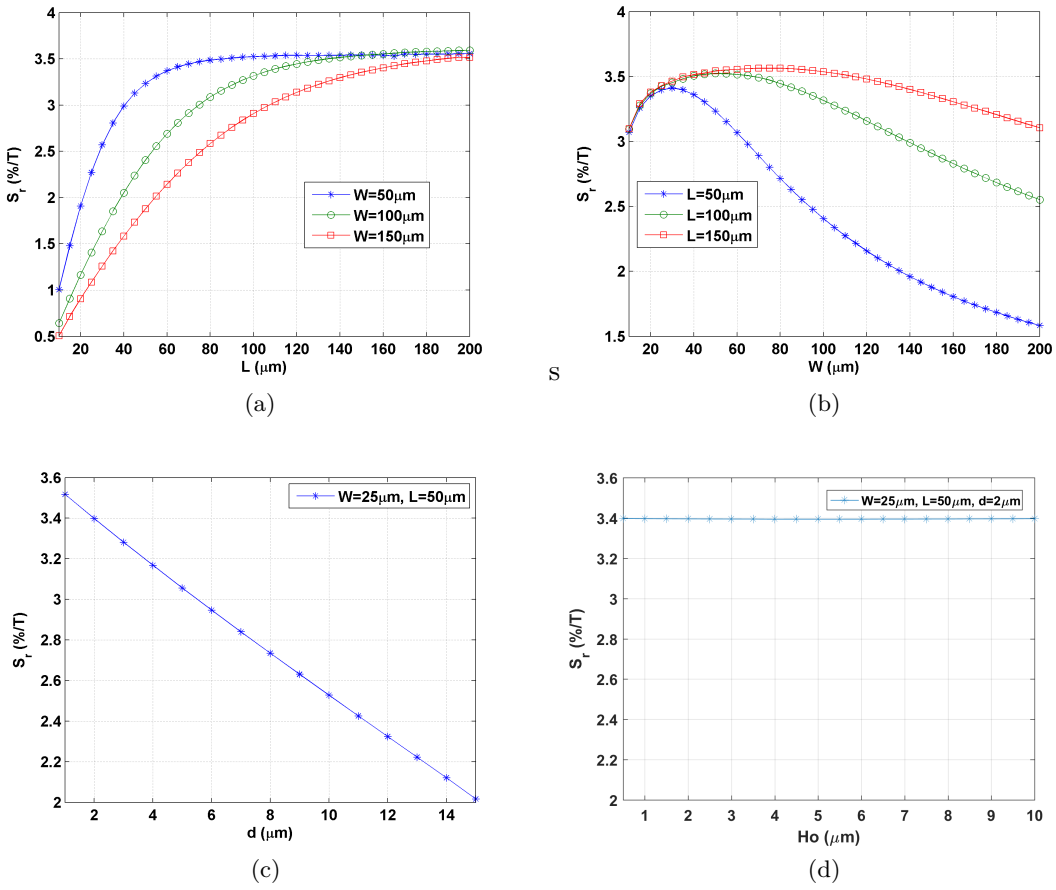
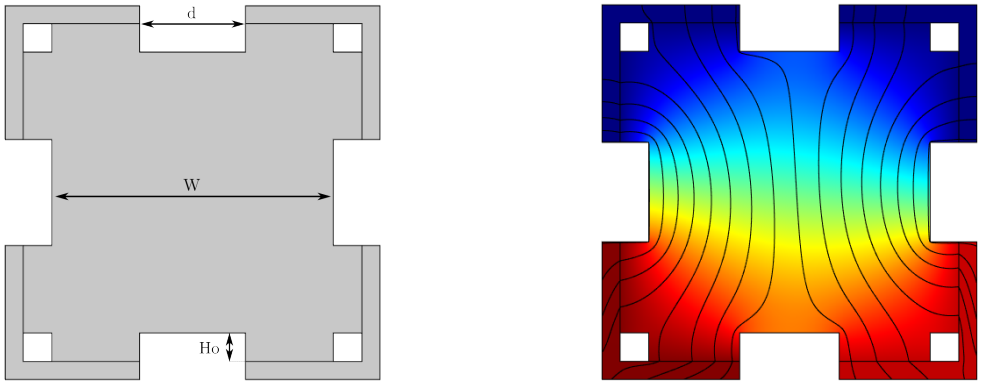


Figure 11.2 – 2D COMSOL simulations of the current-related sensitivity as a function of (a) the length L, (b) the width W, (c) the drain notch d and the drain overlap H_o.

11.1.2 Application to the CHOPFET

The previous model is now applied to the CHOPFET shape. Figure 11.3a represents the CHOPFET's 2D model. As previously stated, d denotes the drain notch, H_o denotes the drain overlap and W is the active zone width. As a consequence of the square shape, the width W is equal to the length L (hence not represented in this figure). The geometrical

parameters have been chosen to fit the CHOPFET of a first prototype in AMS $0.35\,\mu m$ CMOS process [82]. Therefore, $W = 13.3\,\mu m$, $d = 4.7\,\mu m$ and $Ho = 1.35\,\mu m$. According to figure 10.1, contacts C and D are shorted to form the source, while contacts A and B are the drains. The biasing conditions have been chosen to match the biasing point proposed in [82], i.e. $I_{DS} = 275\,\mu A$ and V_{GS} around $3.0\,V$. The channel doping level was slightly reduced to $0.78 \cdot 10^{17}\,cm^{-3}$ in order to fit the measured value of $V_{DS} = 1.05\,V$. The parameter r_{Hn} was set to 0.4 in order to fit the measured current-related sensitivity. This value might seem low compared to the one of standard Hall plates, usually around 1.15[8], but lower values have been reported for MagFET transducers, and depend on the channel characteristics [84].



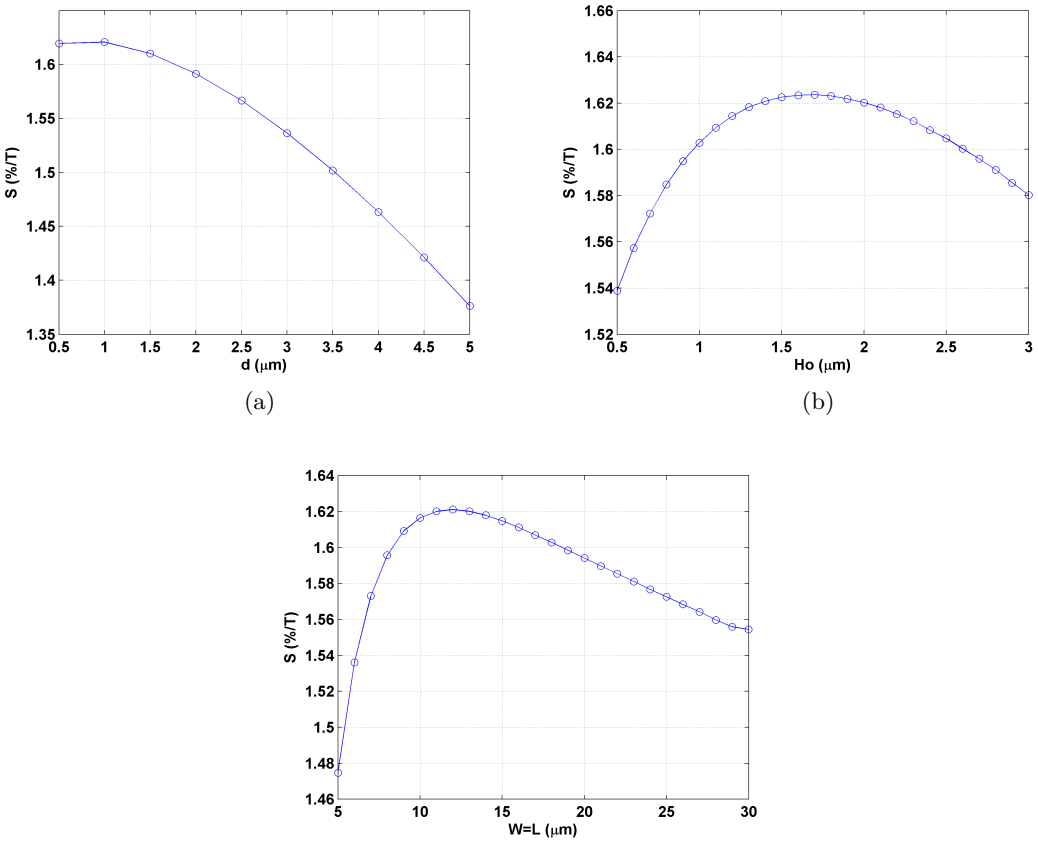
(a) (b)

Figure 11.3 – (a) CHOPFET 2D geometry. (b) Electrical potential and current density lines with $B_z = 5\,T$.

Figure 11.3b shows the simulation results of the electrical potential and the current density lines. The vertical drains force the current lines to bend, and thus increase the effective length compared an equivalent MagFET. Furthermore, the electrical potential simulation clearly shows that, due to strong short-circuit effect in the drain contacts, the Hall effect can not settle in the CHOPFET except in the region near the lateral notches.

Figure 11.4a presents the evolution of the sensitivity as a function of the drain notch d. The results indicate that d should be as small as possible. The sensitivity saturation for low d values is due to two concomitant phenomena. First, decreasing d affects the sensitivity in the same way as the MagFET, but it also affects the current distribution between the vertical and horizontal drain. A part of the current, which flows between the vertical drains, and increases when lowering d, does not participate in the current deflection. Therefore, the current distribution between the lateral and vertical drain varies with d and limits the sensitivity. One might think that the presence of the vertical drains has negative impact on the CHOPFET sensitivity. Nevertheless, it is not case due to the effective length increase, which also increases the sensitivity.

Figure 11.4b shows the sensitivity as a function of the drain overlap H_o. This region does not participate to the total current deflection ΔI and is not in the magnetically active region. The absolute sensitivity is maximum for H_o around $1.5\,\mu m$. It decreases around this value due to the current distribution between the lateral and horizontal contacts. Similarly, in figure



(a) (b) (c)

Figure 11.4 – COMSOL 2D simulations of the current-related sensitivity as a function of (a) the drain notch d, (b) the drain overlap H_o and (c) the active region width W.

11.4c we can see that the width W of the active region affects the equivalent length. For $H_o = 1.35\,\mu m$, the maximum relative sensitivity is achieved with W around $13\,\mu m$. Theses results clearly show that all parameters are tightly coupled. Considering the current-related sensitivity (in AMS $0.35\,\mu m$ CMOS process), the best choice seems to be:

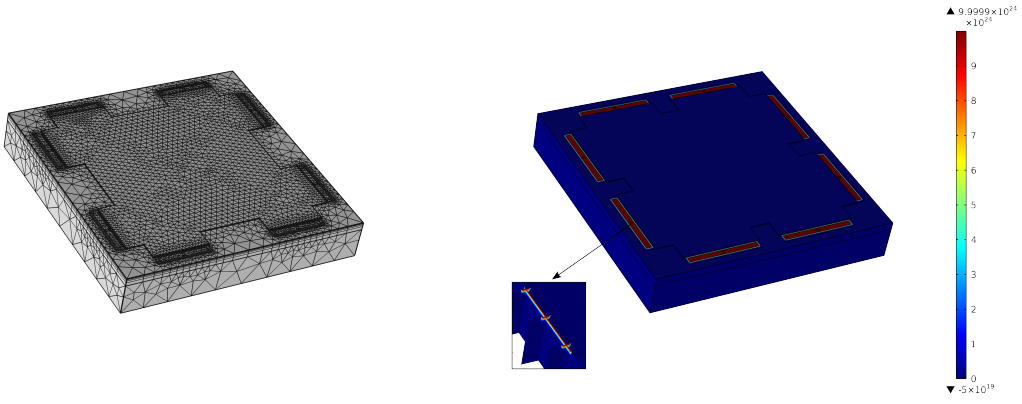
- d as short as possible,
- H_o around $1.5\,\mu m$,
- W around $13\,\mu m$.

11.2 3D FEM model

The 2D model is interesting as a first approach but it is not sufficient to understand the CHOPFET's transistor behavior. A 3D FEM model is necessary to model the channel whatever the biasing used. The principle of this model is based on the COMSOL® application note "DC characteristics of a MOS Transistor" (2D) [80], which has been extended to 3D. As for the 2D model, the physics of the 3D model is also based on the electrostatic module coupled with the conduction/diffusion module. Since implementation of the 3D model is not a straightforward process, particular attention has been paid to the geometry and meshing. The following model stems from an iterative process dedicated to highlighted the key parameters of the simulation. It is the best trade-off between model accuracy and computation time.

11.2.1 Implementation

The CHOPFET geometry is dynamically built as a function of several parameters such as the width, the drain notch... Figure 11.5a shows the mesh used for the following simulations. The SiO_2 insulator thickness was set $7.6\,nm$ according to the AMS $0.35\,\mu m$ process parameters [92]. Particular attention was paid to the insulator meshing, which could dramatically increase the number of elements and thus have strong impact on the computation time. The insulator surface is meshed with triangles, then it is swiped in the insulator volume with one element to form prisms. The silicon top layer is completed by other triangles, whose sizes were adapted in the n+ contacts in order to have sufficient precision on the doping profile. All these triangles are swiped in the CHOPFET depth up to the end of the n+ contacts. A geometric sequence distribution is used to increase the number of elements in the active region. Finally, the mesh is completed with tetrahedrons in the bulk.



(a) (b)

Figure 11.5 – 3D COMSOL® model implementation: (a) mesh and (b) doping level in m^{-3}.

Figure 11.5b shows the three dimensional gaussian function used to achieve realistic approximation of the n+ doping profile [39]. The maximum doping level was set to $5.10^{18}\,cm^{-3}$, while the junction depth (i.e. the depth at which the silicon is intrinsic) was set to $100\,nm$. In order to further enhance realism, the lateral junction length was set to $20\,nm$. The p-type

substrate doping level was set to a constant value, $N_a = 5 \cdot 10^{13}\, cm^{-3}$. The technological parameters, i.e. n+ contacts doping level, n+ contacts junction depth, silicon oxide thickness, etc., have been fixed to the values given in [92, 93].

11.2.2 Transistor characteristics

Preliminary simulations were performed in order to check the physical validity of the model. The simulation plots of figures 11.6 and 11.7 confirms the MOS behavior of our structure. Figure 11.6 shows the electric potential together with the current lines in the channel at the interface between the bulk silicon and the silicon oxide. Figure 11.7 shows the free carrier density at various depths of the channel ranging from 0 to $3\,nm$. The carrier gradient in a same plane is due to V_{DS}, according to conventional MOS transistor behavior.

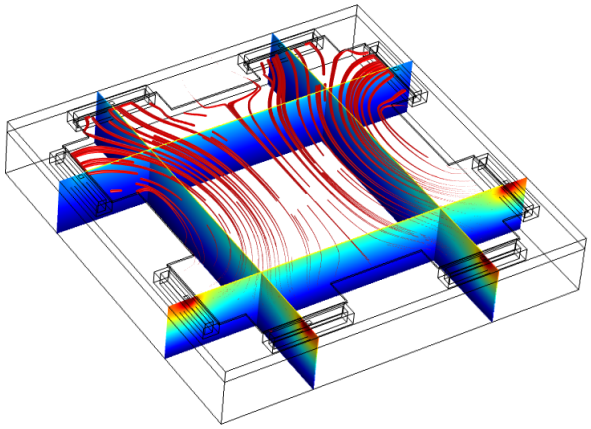


Figure 11.6 – Simulated electric potential and current lines density map, $V_{GS} = 1\,V$, $V_{DS} = 1\,V$.

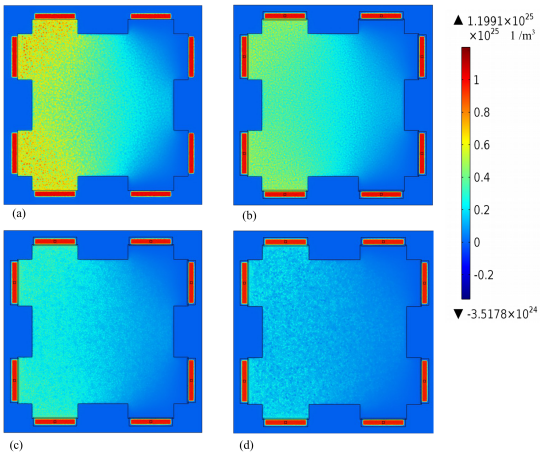
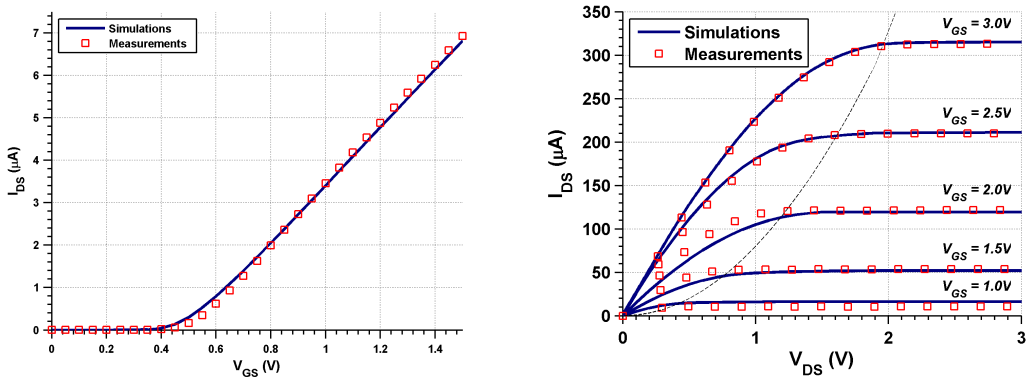


Figure 11.7 – Simulated electron density with drain to source voltage $V_{DS} = 1\,V$ and gate to source voltage $V_{GS} = 1\,V$, (a) depth $0\,nm$, (b) $1\,nm$, (c) $2\,nm$, (d) $3\,nm$.

In order to validate the 3D model, a set of CHOPFET devices with different gap values ($d = 4.7,\ 3.5,\ 2.5,\ 1.5,\ 0.5\,\mu m$) was fabricated in standard technology AMS $0.35\,\mu m$ (cf. section D.2). Electrical measurements were performed with an Agilent® 4156C precision

semiconductor analyzer, and compared to the simulation results. Unless otherwise stated, the results presented in the next figures are obtained from a CHOPFET with $W = 13.3\,\mu m$ and $d = 4.7\,\mu m$, which is our reference device.



(a) (b)

Figure 11.8 – 3D COMSOL simulations: (a) I_{DS} as a function of V_{GS} for V_{DS} fixed to $100\,mV$ and (b) I_{DS} current as a function of V_{DS}. V_{DSsat} is also sketched (dotted line).

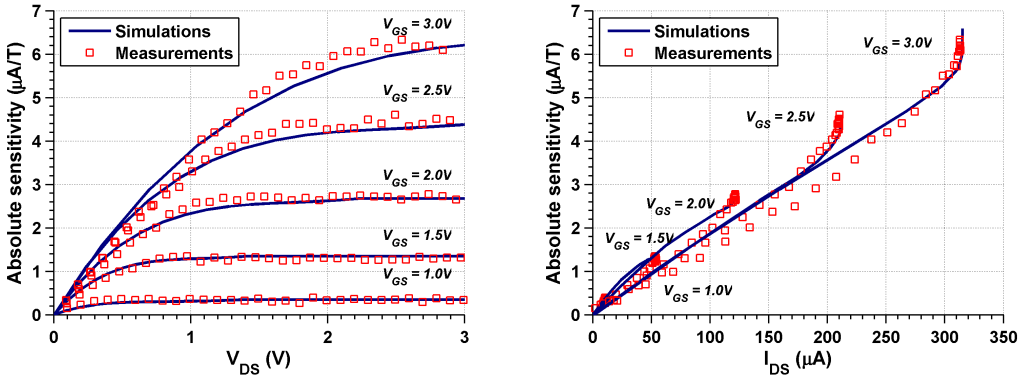
In order to extract the transistor characteristics, V_{DS} was set to $100\,mV$ and the drain to source current, I_{DS}, was measured according to V_{GS}. The CHOPFET is assumed to be in linear region in this case. Thus, the carrier velocity saturation phenomena can be neglected. The simulated characteristics were fitted to the experimental measurements by adjusting the low-field mobility μ_n to $300\,cm^2/(V.s)$ (figure 11.8a). Then the I-V curves were simulated and measured (figure 11.8b). The carrier velocity saturation parameter was thus adjusted to $\beta_n = 1.1$. The CHOPFET is simulated for different biasing condition and shows very good agreement with measurements. This validates the modeling approach for the electrical behavior, i.e. without magnetic field, and thus gives a go to further extend the study to the magnetic part of the model.

11.2.3 Magnetic response

The external magnetic field was set to $10\,mT$ along axis z. The drain current imbalance ΔI is extracted from I-V characteristics to evaluate the absolute sensitivity. Concomitantly, sensitivity measurements were performed with a calibrated Helmholtz coil (with the same magnetic field orientation as in the simulations) and Agilent® 34970A data acquisition unit . The Hall coefficient R_H was adjusted $131\,m^3/C$ in order to fit the simulation to the measured sensitivity. Figure 11.9a shows the absolute sensitivity of the CHOPFET according to V_{DS}. As for the transistor characteristics, simulations and measurements are in good agreement for the magnetic model.

11.2.4 Discussion

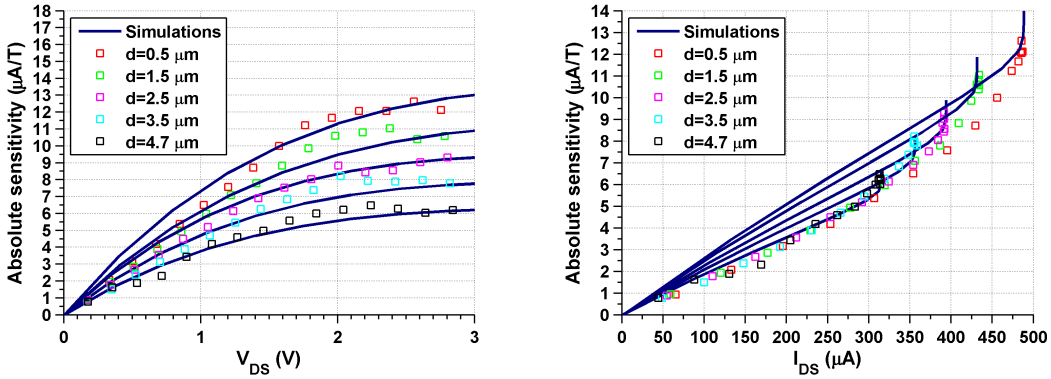
The overall good match between simulations and experiments is crucial for sensor system designers since it allows to assert confident predictions on the CHOPFET's behavior (electrical



(a) (b)

Figure 11.9 – 3D COMSOL simulations: (a) sensitivity as a function the drain source voltage V_{DS} and (b) sensitivity as a function of the drain source current I_{DS}.

and magnetic) according to its parameters.



(a) (b)

Figure 11.10 – 3D COMSOL simulations: (a) sensitivity as a function the drain-source voltage V_{DS} for different values of d ($V_{GS} = 3\,V$) and (b) sensitivity as a function of the drain-source current I_{DS} for different values of d ($V_{GS} = 3\,V$).

Concerning the results shown in figure 11.10a, one can notice that the sensitivity increases with V_{DS} and V_{GS} in the same way as I_{DS} (i.e. I-V characteristics of figure 11.8b). Therefore, the sensitivity reaches a saturation limit, and it comes as no surprise that in order to achieve maximum absolute sensitivity, the CHOPFET should be biased with maximum V_{DS}, V_{GS} and I_{DS}. Yet, this is not necessarily the most interesting operation configuration. As shown in figure 11.9b, the absolute sensitivity can also be represented as a function of I_{DS} (extracted from figure 11.8b). Here, one can notice that the operation configuration has a great impact on the CHOPFET's performance since a same sensitivity value can be reached for different I_{DS} currents corresponding to different V_{GS}. The advantage of using lower V_{GS} values for a targeted sensitivity is twofold: first, the current (i.e. power) consumption can be dramatically reduced without sensitivity loss, and second a lower V_{GS} value gives more flexibility for conditioning electronics design (cf. chapter 12), provided, for instance, the CHOPFET is used as

an input pair in an amplifier [82, 87].

It is also important to notice (cf. figures 11.10a and 11.10b) that the sensitivity keeps on increasing slightly with V_{DS} once the saturation has been reached, i.e. when I_{DS} becomes constant.

As previously demonstrated, the parameter Ho has an impact on the effective channel length but minor effect on the sensitivity (cf. section 11.1). Therefore, it has been fixed to the optimum value of $1.35\,\mu m$, as in [94]. Thus, this work concentrates more specifically on the parameter d, which significantly affects the magnetically active region. Figure 11.10a shows that for a given set of V_{DS} and V_{GS} the sensitivity increases when d is reduced. As shown in figure 11.10b, reducing d increases the maximum biasing current but has minor impact on the measured sensitivity for a given value of I_{DS}. The difference between measurements and simulations in the linear region is as yet not explained. One explanation could be drifting accumulation of errors during recursive computation process, due to the I/V characteristics which is more sensitive in linear region, leading to the noticeable difference in figure 11.10b.

11.3 Optimal operation point

The previous sections were dedicated to optimize the CHOPFET sensitivity through electrical and geometrical parameters. To complete this analysis one should not omit to consider sensitivity versus noise, i.e. resolution. Thus, we now focus on the CHOPFET resolution depending on its absolute sensitivity and its thermal noise floor[5].

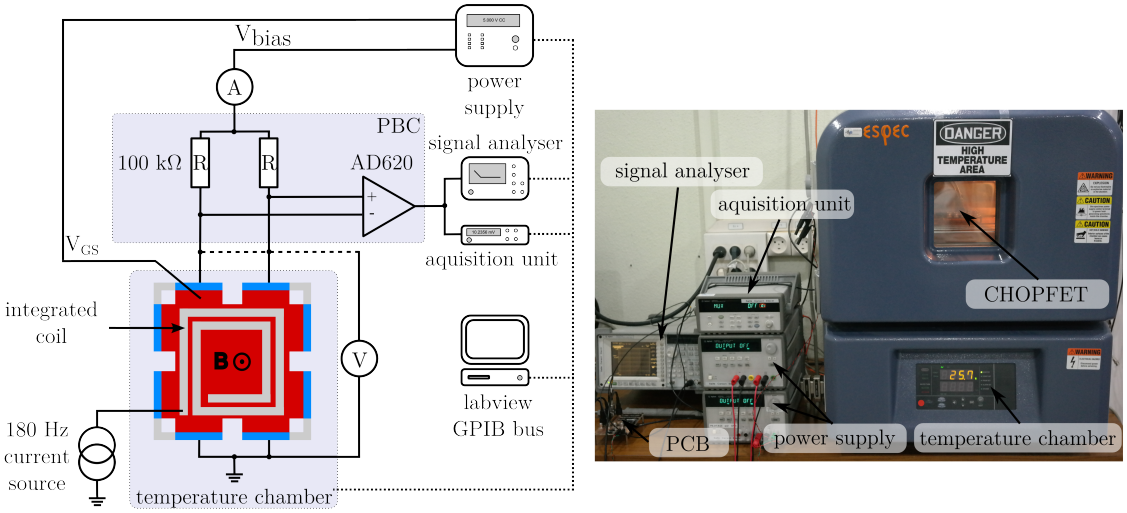
11.3.1 Experimental setup

This study could have been performed on the previously mentioned AMS $0.35\,\mu m$ prototype. Yet, at some point during this thesis, decision was made to upgrade the designs to the newer AMS $180\,nm$ process (also used to develop the conditioning electronics associated to the CHOPFET, presented in the next chapter). Therefore, the following results have been extracted from a CHOPFET device fabricated in the AMS $180\,nm$ standard CMOS technology (figure D.4) using $5\,V$ medium-oxide transistors layers. Note that the CHOPFET dimensioning was chosen to fit the one fabricated in the AMS $0.35\,\mu m$ process (cf. section 11.1.2).

The experimental setup is presented in figure 11.11. A pair of matched high-value resistances, i.e $R = 100\,k\Omega$, was used to perform the current-to-voltage conversion of drain currents. The advantage of using high-value resistances is twofold: the current-to-voltage gain increases, and the corresponding noise current decreases accordingly. The noise contribution of the resistors to the total noise (resistors and CHOPFET and amplifier) is thus negligible. A low noise instrumentation amplifier (AD620), with a gain of $A_v = 40.4$ was chosen to convert the differential signal into a single-ended signal. The total conversion gain is thus defined as $G = R \cdot A_V$. Its input-referred noise is negligible compared to the estimated noise of the CHOPFET-resistors couple. Due to the high resistors' value, the biasing requires

[5]We recall that 1/f noise and offset are removed by SCT (cf. chapter 12).

voltage up to $40\,V$ to achieve a drain-source voltage around $5\,V$. Particular care, such as specific wiring, power supply filtering, and above $200\,kHz$ sampling frequency, was taken to minimize the environmental influence (parasitic sources). An ESPEC® temperature chamber was used to keep the temperature constant at 25°C throughout the experimental session.



(a) (b)

Figure 11.11 – (a) Schematic and (b) picture of the CHOPFET characterization experimental setup.

A coil was integrated over the CHOPFET with the lowest metal layer[6]. It has been calibrated with our Helmholtz coil and achieves $332.9\,mT/A$. With excitation current in the range of milliampere, the integrated coil generates a magnetic field in the millitesla range. The coil was driven with an AC current source, which injects an $180\,Hz$ sinusoidal current. The instrumental chain's harmonic voltage was measured with a dynamic signal analyzer (Agilent® 35670A).

The CHOPFET's V_{DS} and I_{DS} as well as the output voltage was measured with a data acquisition unit (Agilent® 34970A/34901A). V_{GS} and V_{bias} were provided by an Agilent® 3631A power supply.

The noise figures were extracted from the power spectral density by the current-to-voltage conversion, and which was measured with a dynamic signal analyzer (Agilent® 35670A). The noise measurement reference frequency was set to $100\,kHz$, which is above the corner frequency of the fabricated device[7].

The whole test bench was controlled by a labVIEW® interface in order to perform automatic measurements.

11.3.2 Results and discussion

All measurements presented in the following lines are referred to the current output of the CHOPFET.

[6] Metal 1: closest to the substrate.
[7] The corner frequency is in the $10 - 50\,kHz$ range depending on the biasing current in the CHOPFET.

11.3.2.1 Transistor characteristics

Figure 11.12 shows the I/V characteristics extracted by short-circuiting the two drains D1 and D2, i.e. by configuring the CHOPFET as a conventional MOS transistor. One can identify two main regions: the triode region ($V_{DS} < V_{GS} - V_T$, with V_T the threshold voltage) and the saturation region ($V_{DS} > V_{GS} - V_T$). The triode region can also be separated into two zones: the resistive zone, where the I/V characteristic is approximately linear, and the non-linear zone with V_{DS} close to $V_{GS} - V_T$. One should also notice that the current I_{DS}, with same V_{GS}, is near the one obtained in the $0.35\,\mu m$ process CHOPFET. The maximum gate voltage, and thus the maximum current is increased due to higher insulator thickness.

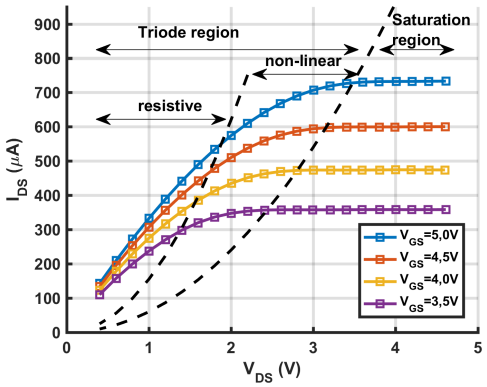


Figure 11.12 – I_{DS} as a function of V_{DS}. The dashed lines separate the various operation modes.

11.3.2.2 Sensitivity

Since no spinning current was applied in this experiment, a set of 64 measurements was performed and averaged to increase the signal-to-noise ratio. The absolute sensitivity at the output of the test bench, obtained at $180\,Hz$, is divided by the overall gain to obtain the CHOPFET sensitivity:

$$S_a = \frac{S_{out}}{G} \tag{11.3.1}$$

Figure 11.13a shows the absolute sensitivity with respect to the biasing current I_{DS}. It comes as no surprise that the highest sensitivity is achieved with the highest biasing current ($I_{DS} = 750\,\mu A$) and the highest gate voltage ($V_{GS} = 5\,V$). As previously mentioned, one can notice that a given sensitivity can be achieved with various I_{DS}/V_{GS} combinations, which can be useful for low-power operation.

Figure 11.13b shows the absolute sensitivity with respect to the drain-source voltage V_{DS}. The sensitivity increases linearly with V_{DS} until saturation is reached, and then remains constant. One can thus notice that strong saturation (i.e. $V_{DS} \gg V_{GS} - V_{th}$) is not compulsory to achieve maximum sensitivity.

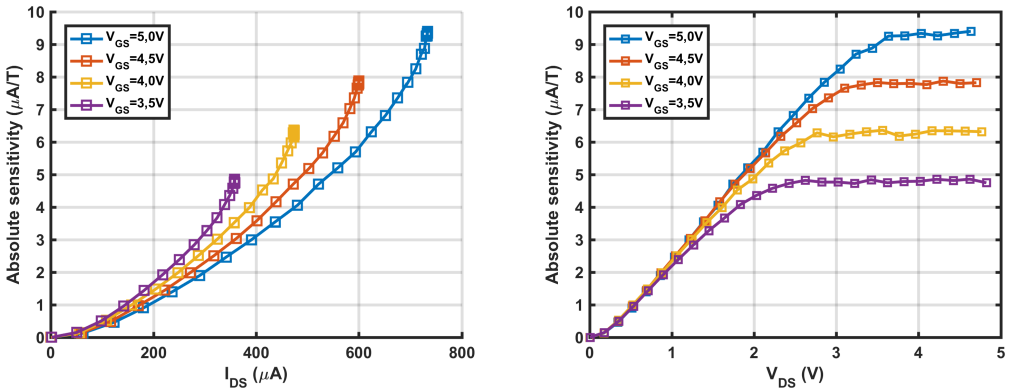


Figure 11.13 – Absolute sensitivity as a function of (a) I_{DS} and (b) V_{DS} .

11.3.2.3 Noise

Figure 11.14a shows the current power spectral density $S_{NI} = S_{NV}/G^2$ at $100\,kHz$ as a function of I_{DS}. Here, S_{NV} is the voltage power spectral density at the output of the instrumental chain. S_{NI} has been used to estimate the RMS thermal noise current, i.e. when removing the 1/f noise by applying the spinning current [82]. One can notice that in the resistive zone of the triode region (i.e. $V_{DS} < V_{GS} - V_{Th}$), the noise hardly varies with I_{DS} and is independent from V_{GS}. This is due to the fact that the transverse electric field related to V_{DS} has only limited effect on the shape of the conduction channel. Therefore, the resistance between the two drains, and thus the thermal noise, can be considered as constant.

When the biasing current increases and the non-linear zone of the triode region is reached, the noise increases dramatically. Here, the effect of V_{DS} cannot be neglected because it affects the resistance between the two drains. As a corollary, note that for a given current, the total noise is inversely proportional to V_{GS} (figure 11.14a). Yet, when the saturation zone is reached the increase of the noise is not as steep anymore. This can be seen in figure 11.14b, which shows the power spectral density at $100\,kHz$ as a function of V_{DS}.

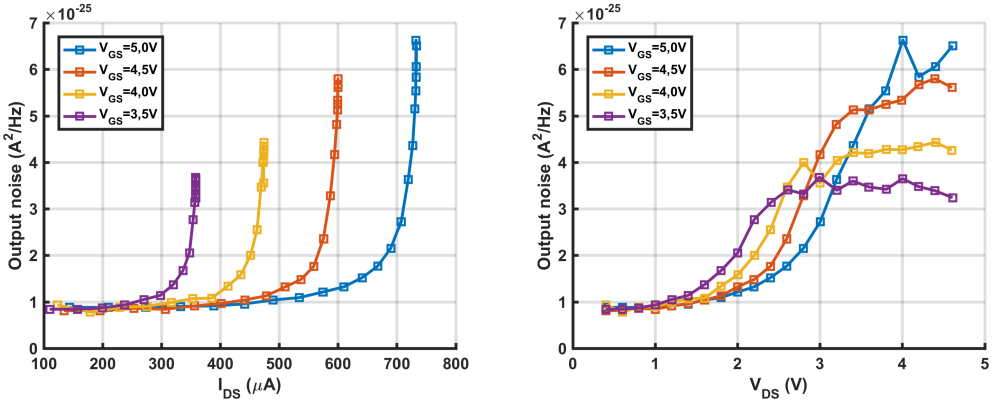
In order to define the device's operating point that satisfies the best trade-off between noise, sensitivity and power consumption, it is thus important to study the resolution.

11.3.2.4 Resolution

The RMS resolution as a function of the biasing current, presented in figure 11.15a, is obtained by the ratio $^{(S_{NI}\cdot BW)^{1/2}}/_{S_a}$.

In the linear zone of the triode region, the resolution is mainly related to the strong sensitivity variation. One can notice that best resolutions are achieved when the non-linear zone of the triode region is reached despite the strong evolution of the noise around that operating point (cf. figure 11.14a). The resolution deteriorates in saturation region because the noise increases while the sensitivity remains constant.

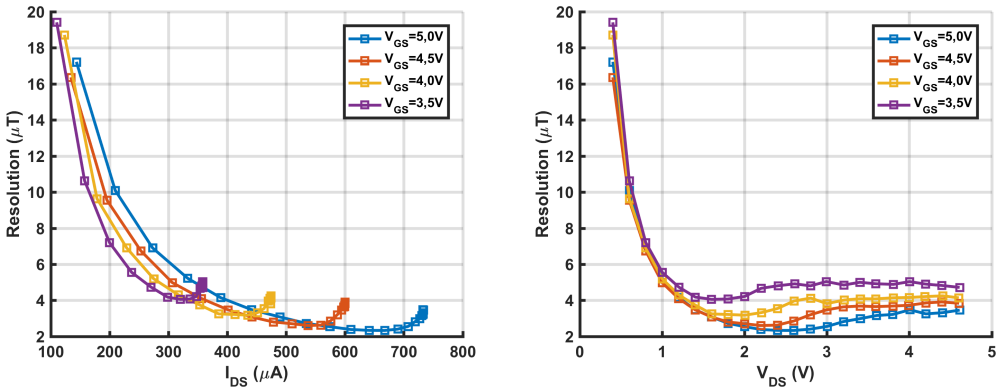
The best resolution, which is $2.3\,\mu T$ (calculated over $BW = [5\,Hz - 1.6\,kHz]$), is achieved with the highest V_{GS} (i.e. $5\,V$) and $I_{DS} \simeq 670\,\mu A \simeq 0.9 \cdot I_{DSsat}$. One should notice that this



(a) (b)

Figure 11.14 – Output noise at $100\,kHz$ as a function of (a) I_{DS} and (b) V_{DS}.

resolution denotes extremely promising results, since it is two times better than the HHD's one achieved with AMS $0.35\,\mu m$ process [58]. Yet, if the biasing current is limited, for example in case of low-power application, fixing V_{GS} to a lower value (i.e. that sets the CHOPFET in the non-linear zone of the triode region) is the best choice. For example, if I_{DS} is set to $250\,\mu A$, the gate voltage should be around $3.5\,V$. This yields around $5\,\mu T$ resolution, which is a typical value for conventional silicon Hall effect devices operating at $1\,mA$ biasing current [58].



(a) (b)

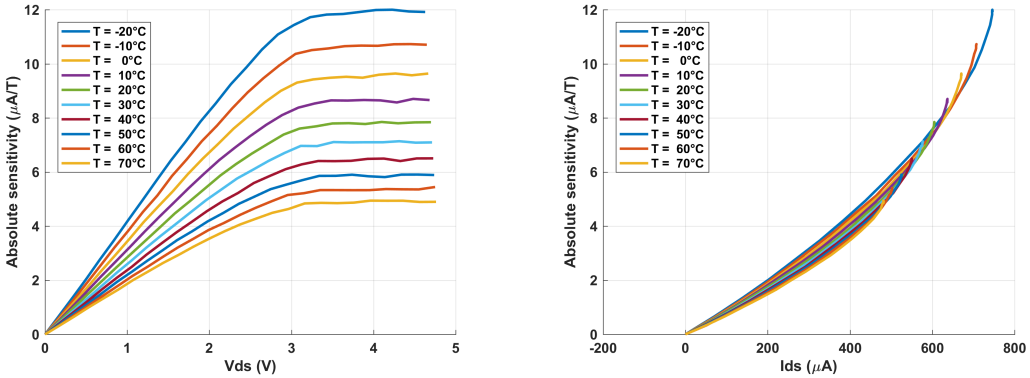
Figure 11.15 – Transducer resolution as a function of (a) I_{DS} and (b) V_{DS} .

11.4 Temperature

In actual applications, it is important to consider the evolution of the absolute sensitivity and maximum biasing current as a function of the temperature. Unfortunately, as discussed in section 4.1.3, there is no complete analytical expression for the sensitivity of a MagFET-type transducer. Therefore, in this section we explore these phenomena through experimental measurements.

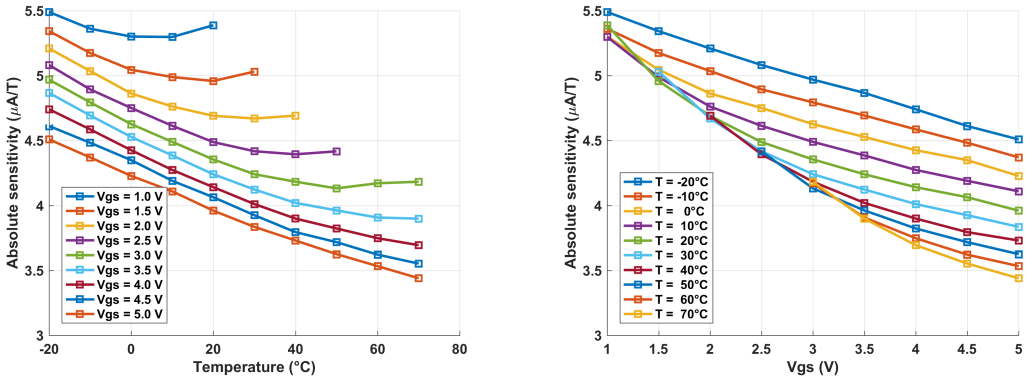
The CHOPFET was placed in an ESPEC® temperature chamber and connected to an external PCB for biasing and amplification. The experimental setup is the same as presented in section 11.3.1.

Figures 11.16a and 11.16b show the absolute sensitivity respectively as a function of V_{DS} and I_{DS} for different temperature varying from -20 to 70°C and V_{GS} fixed to $5\,V$. It appears that the saturation current I_{DSsat} increases at low temperature. Furthermore, for a given I_{DS} or V_{DS}, best sensitivity is achieved at low-temperature due to the mobility increase. The usual active compensation strategy consists in dynamically adapting the biasing current I_{DS} to keep the sensitivity constant as a function of the temperature. Nevertheless, if the transducer is meant to be used in an application where the temperature is liable to change, a sensitivity achievable over the whole temperature range should be chosen.



(a) (b)

Figure 11.16 – Absolute sensitivity as a function of (a) V_{DS} and (b) I_{DS} with $V_{GS} = 5\,V$.



(a) (b)

Figure 11.17 – Absolute sensitivity as a function of (a) temperature and (b) V_{GS} with $I_{DS} = 400\,\mu A$.

Figure 11.17a shows the absolute sensitivity as a function of the temperature with $I_{DS} = 400\,\mu A$. As previously stated, for a fixed current, the highest sensitivity is achieved with V_{GS}

as low as possible. Due to the temperature effect on I_{DS}, it is yet not possible maintain a constant current with low V_{GS} and high temperature. For V_{GS} around $5\,V$ the sensitivity decreases almost linearly with temperature. Figure 11.17b shows the absolute sensitivity as a function of V_{GS} with $I_{DS} = 400\,\mu A$. It appears that a chosen sensitivity can also be achieved with various V_{GS}. This result takes on prime importance because it shows that it is possible to maintain constant sensitivity by controlling V_{GS}. Now, integrated CMOS technologies allow to efficiently integrate advanced conditioning electronics and smart signal processing, which is the subject of the next chapter.

Chapter 12

Dedicated electronics

This chapter addresses the CHOPFET's dedicated electronics. Co-integrating the transducer together with its conditioning electronics and signal processing creates great opportunities to achieve high-performance versatile sensors. One can advantageously use the potential of integrated electronics to design low-noise amplifiers, sensitivity feedback control over temperature, analog-to-digital conversion, and many other features... In this context, the CHOPFET-based sensor performances considerably depend on the appropriate choice of its conditioning electronics. Indeed, the CHOPFET is a current mode transducer and thus requires specific signal handling and processing.

12.1 CHOPFET conditioning and signal processing

In this section, we propose an example of conditioning and signal processing dedicated to the CHOPFET's 1/f noise reduction. Note that we deliberately do not address the question of offset here, because it is a more common issue in integrated electronics for which efficient solutions already exist in the state of the art (cf. section 12.2). The following architecture consists in a differential version of the microsystem developed by Vincent Frick [82]. In particular, the purpose of this microsystem is to confirm the noise correlation statement of section 12.1.2 and thus to confirm the capability of the SCT to remove the 1/f noise of the CHOPFET.

12.1.1 Instrumental chain

Figure 12.1 presents a schematic view of an example of instrumental chain associated to the CHOPFET. The switch box modulates the useful signal (i.e. magnetic signal) around the spinning frequency and keeps the CHOPFET's 1/f noise and offset in the base band, according to the switching pattern illustrated and table 12.1 and figure 12.2 (further details are given in appendix D.1). The split-drains are connected to a differential load (transistors M6, M7) and a chopper stage, while the CHOPFET is biased by a current mirror (M1, M3). The chopper demodulates the magnetic signal in the base-band and rejects the 1/f noise and the offset around the spinning frequency. They can thus easily be removed by low-pass filtering. The differential load is biased by a stage equivalent to half the differential

stage. That is, transistor M5 is identical to M6 and M7, M4 is electrically equivalent to half a CHOPFET, and M2 provides half the biasing current (i.e. $I_{bias}/2$) of the differential stage. The common mode is imposed by a reference voltage applied by two I/V converters. Therefore, the differential current is forced to flow through the chopper and is amplified by the I/V converter. The differential voltage, at the I/V converters' output is optionally converted into single-ended signal in order to facilitate measurements (useful for sensitivity and noise measurements described in section 12.1.3).

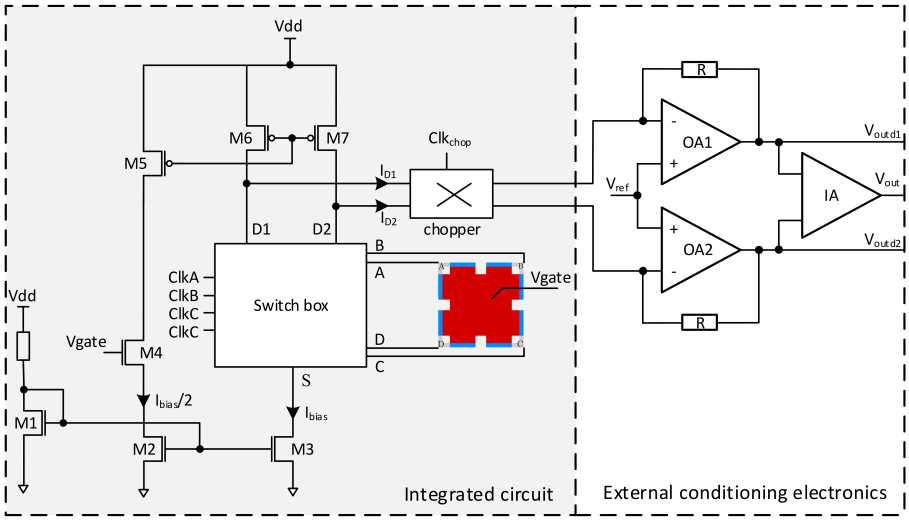
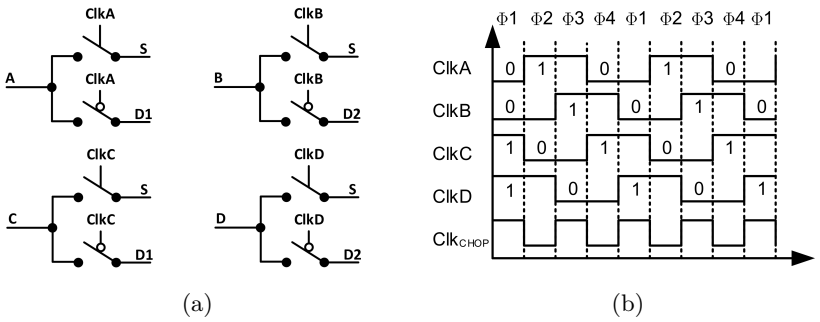


Figure 12.1 – Schematic view of the CHOPFET differential instrumental chain.

	CHOPFET contacts			
	A	B	C	D
phase $\phi 1$	$D1$	$D2$	S	S
phase $\phi 2$	S	$D2$	$D1$	S
phase $\phi 3$	S	S	$D1$	$D2$
phase $\phi 4$	$D1$	S	S	$D2$

Table 12.1 – CHOPFET modulation switching pattern.



(a) (b)

Figure 12.2 – (a) Switch box structure and SCT clocking sequence. ClkA, ClkB, ClkC and ClkD are the SCT clocks and Clk_{CHOP} is the chopping clock.

12.1.2 Noise correlation

As assessed in the introduction of this part (cf. section 10.2) the whole CHOPFET concept relies on the assumption that the noise on a given contact is correlated between two consecutive phases. The instrumental chain (figure 12.1) was designed to enable experiments on the noise correlation within the CHOPFET. The switching sequence has been tweaked to alternatively switch the CHOPFET between phases $\phi 1$ and $\phi 2$. When the chopper is deactivated, the drain current I_{D2} (corresponding to contact B in phases $\phi 1$ and $\phi 2$) flows in the same chopper's transistor[1] and amplification channel[2]. When no magnetic field is applied, I_{D1} and I_{D2} corresponds to offset and noise currents, which are negligible compared to the CHOPFET's biasing current[3]. Thus, both the chopper's transistors and amplification channel add negligible correlated noise contribution.

The experimental setup was battery-powered in order to reduce parasitic environmental effects on the experiment. The voltage signal at the I/V converters output was digitized by a two-channel PXI 24bit resolution analog-to-digital converter. The sampling frequency was set sufficiently high ($f_s = 250\,kHz$) so the measurements between channel 1 and 2 can be considered as instantaneous up to $1.8\,kHz$[4] Furthermore, in order to have good estimation of the 1/f noise at very low frequency (i.e. below 5 Hz), we need sufficiently long acquisition time. We set the acquisition time to $1\,s$.

The data of the channel corresponding to I_{D1} alternatively contains the current related to contact A in phase $\phi 1$, and to contact C in phase $\phi 2$ ($I_{A\phi 1}$ and $I_{C\phi 2}$). Similarly, I_{D2} contains alternatively the current related to contact B in phase $\phi 1$ and phase $\phi 2$ ($I_{B\phi 1}$ and $I_{B\phi 2}$). Since no magnetic field is applied, [$I_{A\phi 1}$, $I_{B\phi 1}$], and [$I_{C\phi 2}$, $I_{B\phi 2}$] are thus the noise contributions of the contacts [A, B] and [C, B] respectively in phases $\phi 1$ and $\phi 2$. In order to make the data exploitable, we first needed to isolate the contribution of each contact in each phase. Therefore, the first step of the data analysis, presented in figure 12.3, consisted in reconstructing $I_{A\phi 1}$, $I_{C\phi 2}$, $I_{B\phi 1}$ and $I_{B\phi 2}$. The experimental setup features only two fast-acquisition channels. Therefore, we reconstructed the spinning clock from the data by means of a PLL[5]. The reconstructed clock signals (Clk and $\overline{Clk}$) were then used to extract $I_{A\phi 1}$, $I_{C\phi 2}$, $I_{B\phi 1}$ and $I_{B\phi 2}$. We then applied high-order low-pass filtering on $I_{A\phi 1}$, $I_{C\phi 2}$, $I_{B\phi 1}$ and $I_{B\phi 2}$ in order to remove the high-frequency commutation spikes and the thermal noise above $1.8\,kHz$. Let us recall that $I_{A\phi 1}$, $I_{B\phi 2}$ and $I_{B\phi 1}$, $I_{C\phi 2}$ are uncorrelated and the common mode noise is removed by differential measurements. These signals are thus used to calculate $\Delta I_{\phi 1} = I_{B\phi 1} - I_{A\phi 1}$ and $\Delta I_{\phi 2} = I_{B\phi 2} - I_{C\phi 2}$ in order to evaluate the noise correlation.

Figure 12.4a shows the temporal plots of $\Delta I_{\phi 1}$ and $\Delta I_{\phi 2}$. It appears clearly that the curves are very similar, thus high correlation level should be expected. Figure 12.4b represents the normalized cross correlation between $\Delta I_{\phi 1}$ and $\Delta I_{\phi 2}$ as a function of the time. The high correlation level (around 0.79) at $t = 0$ confirms the correlation hypothesis on a given

[1] Let us recall that 1/f noise in a transistor is proportional to its I_{DS} current [54].

[2] The input-refereed noise of external amplifiers is negligible compared to the integrated circuit noise.

[3] Estimated to be below 10^{-9} A, cf. figure 12.6b.

[4] The CHOPFET operates at non-optimized biasing point, which causes the thermal noise contribution to be high. This leads to around $1.8\,kHz$ corner frequency.

[5] PLL: Phase-Locked Loop, carried out with MATLAB® Simulink®

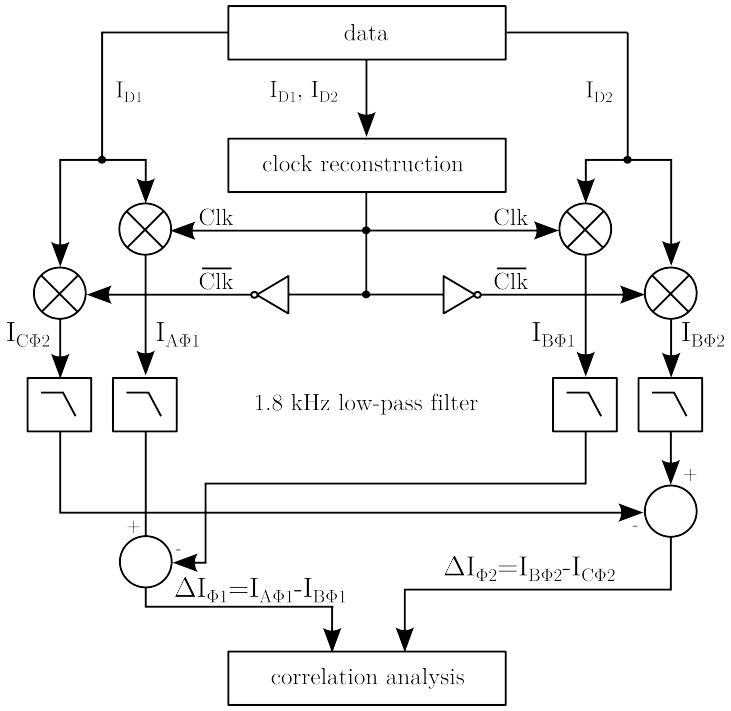
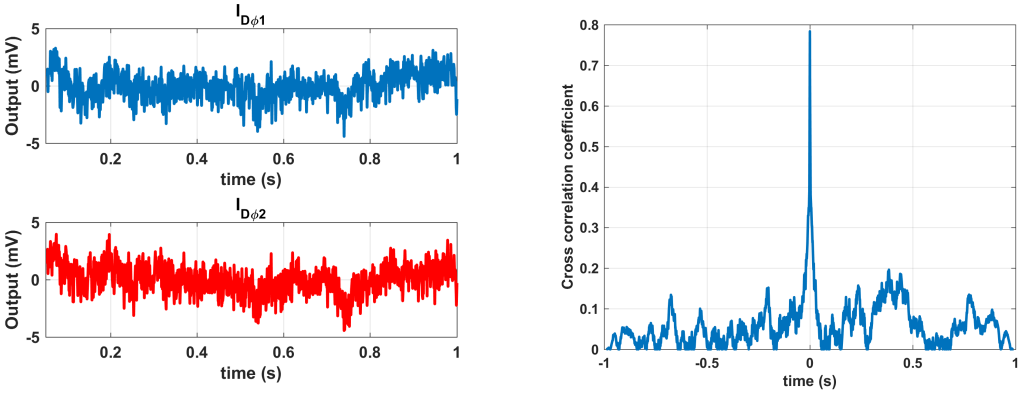


Figure 12.3 – $I_{D\phi1}$ and $I_{D\phi2}$ signals reconstruction.

CHOPFET's contact (and, of course, its corresponding load transistor) between two successive phases. Note that correlation coefficient is lower than 1 (maximum value), this is due the fact that contacts A and C add thus uncorrelated contribution to $\Delta I_{\phi1}$ and $\Delta I_{\phi2}$, which confirms that four-phase SCT is necessary to totally remove the 1/f noise of the CHOPFET.

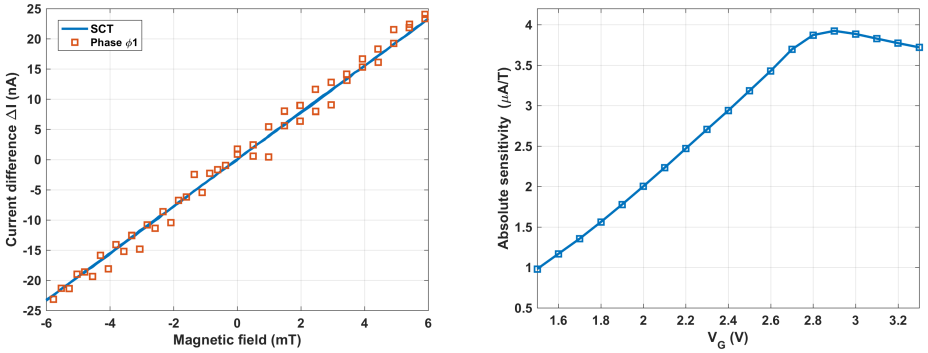


(a) (b)

Figure 12.4 – (a)Temporal plot of $I_{D\phi1}$ and $I_{D\phi2}$, (b) normalized cross-correlation between $I_{D\phi1}$ and $I_{D\phi2}$.

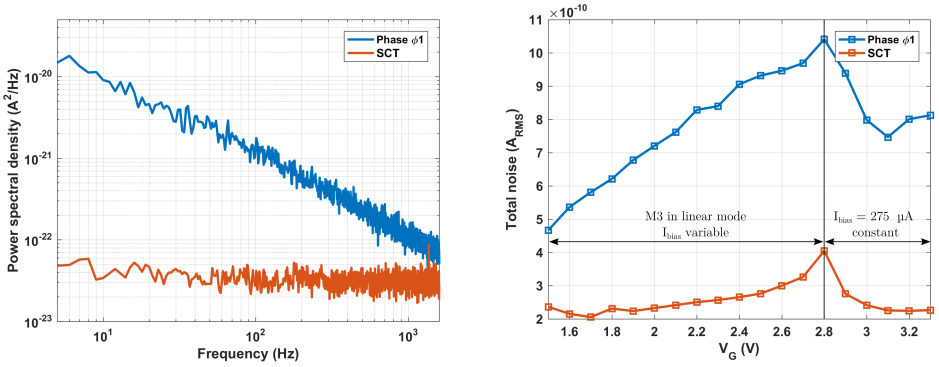
12.1.3 Sensitivity and resolution

The previous section confirmed the noise correlation on a given contact between two consecutive phases, which gives a go for the actual implementation of the SCT according to the configuration proposed in section 12.1.1.



(a) (b)

Figure 12.5 – Measurements of (a) the current difference as a function of the magnetic field (the offset has been nullified), (b) the absolute sensitivity as a function of the gate voltage.



(a) (b)

Figure 12.6 – Measurements of (a) the power spectral density, (b) the total noise as a function of the gate voltage.

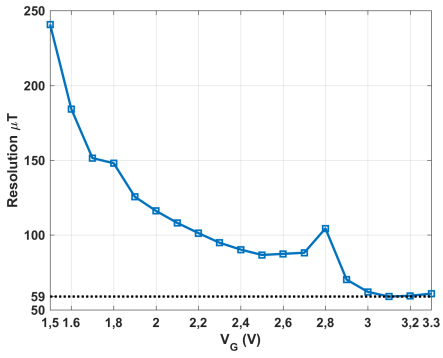


Figure 12.7 – Resolution as a function of the gate voltage.

The sensitivity measurements are presented in figure 12.5[6]. Figure 12.5a shows the current difference as a function of the magnetic field with and without SCT. Figure 12.5b shows the evolution of the absolute sensitivity as a function of the gate voltage. The biasing current was

[6]The experimental setup is identical to the one dedicated to the LV-VHD (cf. section 8.2.2).

initially set to $275\,\mu A$ with $V_G = 3.3\,V$. As long as the current can be maintained to its value, the absolute sensitivity increases when V_G is lowered (cf. section 11.2). Below $V_G = 2.8\,V$ it is no longer possible to maintain the biasing current to $275\,\mu A$, because transistor M3 is no longer saturated ($V_{GSM3} - V_{ThM3} < V_{DSsatM3}$), and the sensitivity thus decreases linearly.

Figure 12.6a shows the noise power spectral density in phase $\phi 1$ only, and with SCT. It clearly appears that the SCT completely removes the 1/f noise. Figure 12.6b shows the total noise over the reference bandwidth ($[5\,Hz - 1.6\,kHz]$) as a function of the gate voltage. Without SCT, the total noise increases linearly with V_G as long as M3 is in linear mode (I_{bias} increases). When $V_G > 2.8\,V$ ($I_{bias} = 275\,\mu A$, constant), the total noise starts to decrease (cf. figure 11.14a and section 11.3.2.3).

Figure 12.7 shows the resolution as a function of V_G. The best resolution achieved by this microsystem is $59\,\mu T$, withV_G higher than $3.0\,V$. This non-optimum resolution (compared to the CHOPFET's transducer resolution, cf. section 11.3) is due to both the inappropriate CHOPFET operation point and loads thermal noise contribution. Moreover, this architecture based on external voltage reference is not suited for offset reduction (cf. section 12.1.1). Considering these issues, an improved ultra-low-noise architecture with offset and 1/f noise cancellation capability should be investigated. This architecture is addressed in section 12.2. Nevertheless, the presented results confirm the capability of the four-phase SCT to efficiently remove the 1/f noise of the CHOPFET and its associated differential load.

Chapter 13

Conclusion on the CHOPFET

This part was dedicated to the study of the CHOPFET and its conditioning electronics. The CHOPFET is a current-mode MagFET-based transducer, suitable with the SCT and a very promising candidate for replacing the conventional Hall sensor for future low-power high-resolution applications.

Chapter 10 was dedicated to, first introduce the principle of the CHOPFET, and then SCT applied to current mode transducers. In particular, we demonstrated that n-phase SCT is necessary to remove the 1/f noise and offset of n-contact current mode transducers.

In chapter 11, we focused on the behavior of the CHOPFET. 2D and 3D FEM model have been proposed and validated with experimental measurements. Simulations highlighted the impact of geometry and biasing on its performances. Sensitivity and noise measurements have been performed to identify the optimum-resolution biasing point. Experiments revealed that, with optimum biasing conditions, the CHOPFET could achieve $2.3\,\mu T$ resolution over $[5\,Hz - 1.6\,kHz]$ bandwidth with SCT (estimated at $100\,kHz$). These performances are globally better than the one announced for conventional Hall sensors in silicon technology.

Chapter 12 was first dedicated to verify the hypothesis of noise correlation within the CHOPFET through experimental measurements. Further experiments allowed to successfully validate the concept of SCT to current mode transducer. This chapter was also dedicated to present the implementation of the CHOPFET within an advanced instrumental chain, based on a Magneto-OPerational amplifier (MOP). This structure can be adapted to achieve specific functionalities (amplification, integration, filtering, sensitivity feedback control over temperature,...), and is thus very interesting to build smart sensors. Two MOP prototypes have been designed. The first prototype validated the concept of the MOP for magnetic signal amplification, and 1/f noise cancellation of the full instrumental chain. The second version, with improved characteristics, is currently under fabrication. It should achieve resolution below ten microteslas.

This study revealed that some significant aspects of the MagFET have been omitted in lit-

erature. For example, the impact of mechanical stress, high magnetic field, cross sensitivities on MagFETs characteristics should be investigating before considering actual applications. The MOP's performances could be further improved by using more specific amplifier architectures. The functionalization also deserved to be explored in order to provide smart sensors featuring advanced functions such as temperature compensation, eventually low-pass filtering of the 1/f noise and offset, ADC...

Chapter 14

General conclusion

Time has now come to draw the conclusion from this PhD thesis dedicated to high-performances magnetic field sensors integrated in silicon technologies. The integration of a transducer together with its dedicated conditioning electronics can be advantageously used to build high-performances smart sensors. The purpose of the conditioning electronics is not only to amplify the transducer's signal, but also to improve the performances of the microsystem.

In light of this purpose, the first part described the state-of-the-art of silicon magnetic field sensors, starting from the Physics, to the transducer and finally to the sensor with advanced functions. This study highlights the differences between transducers providing voltage and current output mode in terms of sensitivity, offset and noise. In particular, the expression of the sensitivity highly depends on the output mode, and thus requires specific optimization approach. The short-circuit effect due to the measurement and biasing contacts is a good example since it should be minimized in voltage mode and maximized in current mode.

The second part was dedicated to the LV-VHD together with its offset and 1/f noise reduction techniques. Advanced modeling work has been carried out to model the transducer, using an approach that can be adapted to any silicon transducer. A 2D model was built with a view to simulating 1/f noise and offset within the transducer. Results confirm that four-phase SCT is necessary to remove efficiently the offset. A new dedicated signal processing technique, called bi-current SCT, has been proposed. This technique allows to operate the LV-VHD at the highest achievable biasing current whatever its phase. The single and bi-current SCT have been validated through FEM simulation and experimental results. As expected, best performance is achieved by bi-current SCT, with $51\,\mu T$ resolution over $[5\,Hz - 1.6\,kHz]$ bandwidth and $1.6\,mT$ residual offset.

The third part was dedicated to study a very promising transducer, the CHOPFET. The behavior of the CHOPFET was studied through 2D and 3D FEM models and experimentation. Based on the results, we proposed optimization and biasing strategies for high-sensitivity or low-power operation. The models allow the analog designer to extract the transducer's most important characteristics and imagine its best adapted conditioning electronics.

Measurements have been performed to identify the optimum-resolution biasing point of the CHOPFET. The measured resolution on the CHOPFET is $2.3\mu T$ over $[5\,Hz - 1.6\,kHz]$ bandwidth estimated at $100\,kHz$, which is globally better than the one announced for conventional Hall sensors in standard CMOS process.

The SCT has been adapted to the CHOPFET on the basis of the noise correlation hypothesis that has been experimentally verified. We proved that n-phase SCT is necessary to remove the 1/f noise (and offset) of an n-contact current mode transducer.

The CHOPFET has been implemented in an instrumental chain based on a Magneto-OPerational amplifier (MOP). A European and International patent dedicated to the instrumental chain is currently pending. The concept of the MOP for magnetic signal amplification, and 1/f noise cancellation of the full instrumental chain has been validated experimentally.

We are getting close to the end of this manuscript. Several solutions to push the limits of the LV-VHD and the CHOPFET have been proposed. The thrilling part of Research is that each results open doors to further exciting perspectives.

In the short term, we will focus on the second MOP prototype characterization. We will investigate, in particular, the effects of the temperature on the MOP's characteristics. Based on these measurements, we will propose actual implementation for sensitivity drift compensation. Concerning the LV-VHD, we will consider developing fully integrated 3D magnetic field sensors by combining two LV-VHDs with bi-current SCT and a HDD with SCT.

Looking further ahead, we could develop smart ultra-low-power magnetic field sensor based on CHOPFET operating at low V_{GS} voltage and biasing current. The MOP could be implemented in a Delta-Sigma ADC as an integrator. We could imagine combining the magnetometer to energy harvesting and wireless communication, thus paving the way to autonomous high-performance magnetic field sensors networks.

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Appendices

Appendix A

List of publications

Journal

- L. Osberger, V. Frick, L. Hébrard, "High resolution shallow vertical Hall sensor operated with four-phase bi-current spinning current", Sensors and Actuators A: Physical, Volume 244, 15 June 2016, Pages 270-276.

Patent

- L. Osberger, V. Frick, "Magnetic operational amplifier". European and international patent pending (EP16169019.3).

International conferences

- L. Osberger, J. B. Schell, V. Frick, "On optimal operation of the CHOPFET magnetic field transducer" 2017 IEEE 15th International New Circuits and Systems Conference (NEWCAS), Strasbourg, 2017.

- L. Osberger, V. Frick, "3D FEM Modelling of a New Magnetic Field Sensor: The CHOPFET", Procedia Engineering, Volume 120, 2015, Pages 410-413.

- L. Osberger, V. Frick, L. Hébrard, "Four-phase Bi-current Spinning Current on Shallow Vertical Hall Sensor", Procedia Engineering, Volume 120, 2015, Pages 120-123.

- L. Osberger, V. Frick, M. Madec and L. Hébrard, "High resolution, low offset Vertical Hall device in low-voltage CMOS technology" 2015 IEEE 13th International New Circuits and Systems Conference (NEWCAS), Grenoble, 2015, pp. 1-4.

- M. Madec, L. Osberger, J. B. Schell, J. B. Kammerer, C. Lallement and L. Hebrard, "Compact modeling of offset sources in vertical hall-effect devices" 2014 IEEE 12th International New Circuits and Systems Conference (NEWCAS), Trois-Rivieres, QC, 2014, pp. 253-256.

- L. Osberger and V. Frick, “2D MAGFET-type sensors modeling: Application to a new device design, the CHOPFET” 2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS), Marseille, 2014, pp. 355-358.
- M. Madec, L. Osberger and L. Hébrard, “Assessment of the spinning-current efficiency in cancelling the 1/f noise of Vertical Hall Devices through accurate FEM modeling” 2013 IEEE SENSORS, Baltimore, MD, 2013, pp. 1-4.

National conferences

- L. Osberger, V. Frick, “Modélisation 3D d’un capteur de champ magnétique : le CHOPFET”, JNRDM TOULOUSE 2016, Toulouse, France, mai 2016.
- L. Osberger, V. Frick, L. Hébrard, “Four-phase bi-current spinning current on shallow vertical Hall sensor”, Colloque national du GdR SoC-SiP, Nantes, France, juin 2016.
- L. Osberger, V. Frick, “Modélisation 3D d’un nouveau capteur de champ magnétique : le CHOPFET”, JNRDM 2015, Bordeaux, France, avril 2015.
- L. Osberger, V. Frick, L. Hébrard, “Etude de la technique du courant tournant pour la réduction du bruit en 1/f des capteurs à effet Hall verticaux par simulation FEM”, JNRDM14, Lille, France, mai 2014.

Appendix B

Hall effect

B.1 Equations without physical magnetoresistive effect

Equation 2.1.4 resolution:

$$\boldsymbol{v_n} = -\frac{q \cdot \tau}{m^*} \cdot \boldsymbol{E_e} - \frac{q \cdot \tau}{m^*} \cdot (\boldsymbol{v_n} \times \boldsymbol{B}) \tag{B.1.1}$$

Our aim is to express $\boldsymbol{v_n}$ as a function of $\boldsymbol{E_e}$ and $\boldsymbol{B}$. Thus, we calculate $\boldsymbol{v_n} \times \boldsymbol{B}$:

$$\boldsymbol{v}_n \times \boldsymbol{B} = -\frac{q \cdot \tau}{m^*} \cdot \boldsymbol{E}_e \times \boldsymbol{B} - \frac{q \cdot \tau}{m^*} \cdot (\boldsymbol{v}_n \times \boldsymbol{B}) \times \boldsymbol{B} \tag{B.1.2}$$

By using the expression $(\boldsymbol{a} \times \boldsymbol{b}) \times \boldsymbol{c} = (\boldsymbol{a}.\boldsymbol{c}) \cdot \boldsymbol{b} - (\boldsymbol{b}.\boldsymbol{c}) \cdot \boldsymbol{a}$, we get:

$$\boldsymbol{v}_n \times \boldsymbol{B} = -\frac{q \cdot \tau}{m^*} \cdot \boldsymbol{E}_e \times \boldsymbol{B} - \frac{q \cdot \tau}{m^*} \cdot ((\boldsymbol{v}_n.\boldsymbol{B}) \cdot \boldsymbol{B} - (\boldsymbol{B}.\boldsymbol{B}) \cdot \boldsymbol{v}_n) \tag{B.1.3}$$

We also have to calculate $\boldsymbol{v}_n.\boldsymbol{B}$:

$$\begin{aligned} \boldsymbol{v}_n.\boldsymbol{B} &= -\frac{q \cdot \tau}{m^*} \cdot \boldsymbol{E}_e.\boldsymbol{B} - \frac{q \cdot \tau}{m^*} \cdot (\boldsymbol{v}_n \times \boldsymbol{B}).\boldsymbol{B} \\ &= -\frac{q \cdot \tau}{m^*} \cdot \boldsymbol{E}_e.\boldsymbol{B} \end{aligned} \tag{B.1.4}$$

Thus equation B.1.3 becomes:

$$\boldsymbol{v}_n \times \boldsymbol{B} = -\frac{q \cdot \tau}{m^*} \cdot \boldsymbol{E}_e \times \boldsymbol{B} - \frac{q \cdot \tau}{m^*} \cdot \left(-\frac{q \cdot \tau}{m^*} \cdot (\boldsymbol{E}_e.\boldsymbol{B}) \cdot \boldsymbol{B} - B^2 \cdot \boldsymbol{v}_n \right) \tag{B.1.5}$$

We replace $\boldsymbol{v}_n \times \boldsymbol{B}$ by equation (B.1.5) in equation (B.1.1), therefore:

$$\boldsymbol{v}_n = -\frac{q \cdot \tau}{m^*} \cdot \boldsymbol{E}_e - \frac{q \cdot \tau}{m^*} \cdot \left(-\frac{q \cdot \tau}{m^*} \cdot \boldsymbol{E}_e \times \boldsymbol{B} - \frac{q \cdot \tau}{m^*} \cdot \left(-\frac{q \cdot \tau}{m^*} \cdot (\boldsymbol{E}_e.\boldsymbol{B}) \cdot \boldsymbol{B} - B^2 \cdot \boldsymbol{v}_n \right) \right)$$

$$\boldsymbol{v}_n \left(1 + \frac{q \cdot \tau}{m^*} \cdot B^2 \right) = -\frac{q \cdot \tau}{m^*} \cdot \boldsymbol{E}_e + \left(\frac{q \cdot \tau}{m^*} \right)^2 \cdot \boldsymbol{E}_e \times \boldsymbol{B} - \left(\frac{q \cdot \tau}{m^*} \right)^3 \cdot (\boldsymbol{E}_e.\boldsymbol{B}) \cdot \boldsymbol{B}$$

Finally:

$$\boldsymbol{v}_n = \frac{-\frac{q\cdot\tau}{m^*}\cdot\boldsymbol{E}_e + \left(\frac{q\cdot\tau}{m^*}\right)^2\cdot\boldsymbol{E}_e\times\boldsymbol{B} - \left(\frac{q\cdot\tau}{m^*}\right)^3\cdot(\boldsymbol{E}_e.\boldsymbol{B})\cdot\boldsymbol{B}}{\left(1+\frac{q\cdot\tau}{m^*}\cdot B^2\right)} \tag{B.1.6}$$

Inverting equation (2.1.10) to obtain the electric field as a function of the magnetic field $\boldsymbol{B}$ and the current density $\boldsymbol{J}$.

$$\boldsymbol{J} = n\cdot q\cdot\left(\frac{q}{m^*}\cdot\langle\tau\rangle\cdot\boldsymbol{E}_e - \left(\frac{q}{m^*}\right)^2\cdot\langle\tau^2\rangle\cdot\boldsymbol{E}_e\times\boldsymbol{B} + \left(\frac{q}{m^*}\right)^3\cdot\langle\tau^3\rangle\cdot(\boldsymbol{E}_e.\boldsymbol{B})\cdot\boldsymbol{B}\right) \tag{B.1.7}$$

Rewriting $\boldsymbol{J}\times\boldsymbol{B}$ and $\boldsymbol{J}.\boldsymbol{B}$ gives:

$$\begin{aligned}\boldsymbol{J}\times\boldsymbol{B} &= n\cdot q\cdot\left(\frac{q}{m^*}\cdot\langle\tau\rangle\cdot\boldsymbol{E}_e\times\boldsymbol{B} - \left(\frac{q}{m^*}\right)^2\cdot\langle\tau^2\rangle\cdot(\boldsymbol{E}_e\times\boldsymbol{B})\times\boldsymbol{B}\right)\\ &= n\cdot q\cdot\left(\frac{q}{m^*}\cdot\langle\tau\rangle\cdot\boldsymbol{E}_e\times\boldsymbol{B} - \left(\frac{q}{m^*}\right)^2\cdot\langle\tau^2\rangle\cdot\Big((\boldsymbol{E}_e.\boldsymbol{B})\cdot\boldsymbol{B} - B^2\cdot\boldsymbol{E}_e\Big)\right)\end{aligned} \tag{B.1.8}$$

Thus:

$$\boldsymbol{E}_e\times\boldsymbol{B} = \frac{\boldsymbol{J}\times\boldsymbol{B} + n\cdot q\cdot\left(\frac{q}{m^*}\right)^2\cdot\langle\tau^2\rangle\cdot\big((\boldsymbol{E}_e.\boldsymbol{B})\cdot\boldsymbol{B} - B^2\cdot\boldsymbol{E}_e\big)}{n\cdot q\cdot\frac{q}{m^*}\cdot\langle\tau\rangle} \tag{B.1.9}$$

Moreover:

$$\begin{aligned}\boldsymbol{J}.\boldsymbol{B} &= n\cdot q\cdot\left(\frac{q}{m^*}\cdot\langle\tau\rangle\cdot\boldsymbol{E}_e.\boldsymbol{B} + \left(\frac{q}{m^*}\right)^3\cdot\langle\tau^3\rangle\cdot(\boldsymbol{E}_e.\boldsymbol{B})\cdot B^2\right)\\ &= n\cdot q\cdot\frac{q}{m^*}\cdot\langle\tau\rangle\cdot(\boldsymbol{E}_e.\boldsymbol{B})\left(1+\frac{\langle\tau^3\rangle}{\langle\tau\rangle^3}\cdot\left(\frac{q\cdot\langle\tau\rangle}{m^*}\right)^2\cdot B^2\right)\end{aligned} \tag{B.1.10}$$

We assumed that the expression $\left(\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2\right)$ can be neglected compared to 1 (cf. equation 2.1.8). Therefore:

$$\boldsymbol{J}.\boldsymbol{B} = n\cdot q\cdot\frac{q}{m^*}\cdot\langle\tau\rangle\cdot(\boldsymbol{E}_e.\boldsymbol{B}) \tag{B.1.11}$$

from which:

$$\boldsymbol{E}_e.\boldsymbol{B} = \frac{\boldsymbol{J}.\boldsymbol{B}}{n\cdot q\cdot\frac{q}{m^*}\cdot\langle\tau\rangle} \tag{B.1.12}$$

Replacing equation (B.1.9) into (B.1.7) gives:

$$\begin{aligned}\boldsymbol{J} &= n\cdot q\cdot\frac{q}{m^*}\cdot\langle\tau\rangle\cdot\boldsymbol{E}_e + n\cdot q\cdot\left(\frac{q}{m^*}\right)^3\cdot\langle\tau^3\rangle\cdot(\boldsymbol{E}_e.\boldsymbol{B})\cdot\boldsymbol{B}\\ &\quad -n\cdot q\cdot\left(\frac{q}{m^*}\right)^2\cdot\langle\tau^2\rangle\cdot\frac{\boldsymbol{J}\times\boldsymbol{B} + n\cdot q\cdot\left(\frac{q}{m^*}\right)^2\cdot\langle\tau^2\rangle\cdot\big((\boldsymbol{E}_e.\boldsymbol{B})\cdot\boldsymbol{B} - B^2\cdot\boldsymbol{E}_e\big)}{n\cdot q\cdot\frac{q}{m^*}\cdot\langle\tau\rangle}\end{aligned} \tag{B.1.13}$$

from which:

$$n \cdot q \cdot \frac{q}{m^*} \cdot \langle \tau \rangle \cdot \left(1 + \frac{\langle \tau^2 \rangle^2}{\langle \tau \rangle^4} \cdot \left(\frac{q \cdot \langle \tau \rangle}{m^*}\right)^2 \cdot B^2\right) \cdot \boldsymbol{E}_e = \boldsymbol{J} + \frac{n \cdot q \cdot \left(\frac{q}{m^*}\right)^2 \cdot \langle \tau^2 \rangle}{n \cdot q \cdot \frac{q}{m^*} \cdot \langle \tau \rangle} \cdot \boldsymbol{J} \times \boldsymbol{B} + \left(n \cdot q \cdot \frac{\left(\frac{q}{m^*}\right)^4 \cdot \langle \tau^2 \rangle^2}{\frac{q}{m^*} \cdot \langle \tau \rangle} - n \cdot q \cdot \left(\frac{q}{m^*}\right)^3 \cdot \langle \tau^3 \rangle\right) \cdot (\boldsymbol{E}_e.\boldsymbol{B}) \cdot \boldsymbol{B} \quad \text{(B.1.14)}$$

According to equation 2.1.8, equation (B.1.14) can be rewritten as:

$$\begin{aligned} \boldsymbol{E}_e &= \frac{\boldsymbol{J}}{n \cdot q \cdot \frac{q}{m^*} \cdot \langle \tau \rangle} + \frac{1}{n \cdot q} \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot \boldsymbol{J} \times \boldsymbol{B} \\ &+ \frac{n \cdot q \cdot \frac{\left(\frac{q}{m^*}\right)^4 \cdot \langle \tau^2 \rangle^2}{\frac{q}{m^*} \cdot \langle \tau \rangle} - n \cdot q \cdot \left(\frac{q}{m^*}\right)^3 \cdot \langle \tau^3 \rangle}{n \cdot q \cdot \frac{q}{m^*} \cdot \langle \tau \rangle} \cdot (\boldsymbol{E}_e.\boldsymbol{B}) \cdot \boldsymbol{B} \end{aligned} \quad \text{(B.1.15)}$$

Finally by inserting equation (B.1.12) in (B.1.15), we obtain:

$$\boldsymbol{E}_e = \frac{\boldsymbol{J}}{n \cdot q \cdot \frac{q}{m^*} \cdot \langle \tau \rangle} + \frac{1}{n \cdot q} \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot \boldsymbol{J} \times \boldsymbol{B} + \frac{\frac{q}{m^*} \cdot \langle \tau \rangle}{n \cdot q} \cdot \left(\frac{\langle \tau^2 \rangle^2}{\langle \tau \rangle^4} - \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3}\right) \cdot (\boldsymbol{J}.\boldsymbol{B}) \cdot \boldsymbol{B} \quad \text{(B.1.16)}$$

which is simplified as:

$$\boldsymbol{E}_e = \frac{\boldsymbol{J}}{\sigma_n} - R_H \cdot \boldsymbol{J} \times \boldsymbol{B} + P_H \cdot (\boldsymbol{J}.\boldsymbol{B}) \cdot \boldsymbol{B} \quad \text{(B.1.17)}$$

with:

$$\sigma_n = n \cdot q \cdot \frac{q}{m^*} \cdot \langle \tau \rangle \quad \text{(B.1.18)}$$

$$R_H = -\frac{1}{n \cdot q} \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \quad \text{(B.1.19)}$$

$$P_H = \frac{\frac{q}{m^*} \cdot \langle \tau \rangle}{n \cdot q} \cdot \left(\frac{\langle \tau^2 \rangle^2}{\langle \tau \rangle^4} - \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3}\right) \quad \text{(B.1.20)}$$

B.2 Equations with physical magnetoresistive effect

Expression of σ_n, $\mathbf{R}_H$ and $\mathbf{P}_H$ for any magnetic field

The general expression of the current $\boldsymbol{J}$ is:

$$\begin{aligned}\boldsymbol{J} &= n\cdot q\cdot\left\langle\frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot\boldsymbol{E}_e - n\cdot q\cdot\left\langle\frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot\boldsymbol{E}_e\times\boldsymbol{B}\\ &\quad + n\cdot q\cdot\left\langle\frac{\left(\frac{q\cdot\tau}{m^*}\right)^3}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot(\boldsymbol{E}_e.\boldsymbol{B})\cdot\boldsymbol{B}\end{aligned}\tag{B.2.1}$$

As before we calculate $\boldsymbol{J}.\boldsymbol{B}$ and $\boldsymbol{J}\times\boldsymbol{B}$:

$$\boldsymbol{J}.\boldsymbol{B} = n\cdot q\cdot\left\langle\frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot\boldsymbol{E}_e.\boldsymbol{B} + n\cdot q\cdot\left\langle\frac{\left(\frac{q\cdot\tau}{m^*}\right)^3}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot B^2\cdot(\boldsymbol{E}_e.\boldsymbol{B})\tag{B.2.2}$$

thus

$$\boldsymbol{E}_e.\boldsymbol{B} = \frac{\boldsymbol{J}.\boldsymbol{B}}{n\cdot q\cdot\left\langle\frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle + n\cdot q\cdot\left\langle\frac{\left(\frac{q\cdot\tau}{m^*}\right)^3}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot B^2}\tag{B.2.3}$$

and

$$\begin{aligned}&= n\cdot q\cdot\left\langle\frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot\boldsymbol{E}_e\times\boldsymbol{B}\\ &\quad -n\cdot q\cdot\left\langle\frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot\Big((\boldsymbol{E}_e.\boldsymbol{B})\cdot\boldsymbol{B} - B^2\cdot\boldsymbol{E}_e\Big)\end{aligned}\tag{B.2.4}$$

Therefore:

$$\boldsymbol{E}\times\boldsymbol{B} = \frac{\boldsymbol{J}\times\boldsymbol{B} + n\cdot q\cdot\left\langle\frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot\big((\boldsymbol{E}_e.\boldsymbol{B})\cdot\boldsymbol{B} - B^2\cdot\boldsymbol{E}_e\big)}{n\cdot q\cdot\left\langle\frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle}\tag{B.2.5}$$

Inserting equation (B.2.5) in (B.2.1) gives:

$$\begin{aligned}\boldsymbol{J} &= n\cdot q\cdot\left\langle\frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot\boldsymbol{E}_e + n\cdot q\cdot\left\langle\frac{\left(\frac{q\cdot\tau}{m^*}\right)^3}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot(\boldsymbol{E}_e.\boldsymbol{B})\cdot\boldsymbol{B}\\ &\quad -n\cdot q\cdot\left\langle\frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot\frac{\boldsymbol{J}\times\boldsymbol{B} + n\cdot q\cdot\left\langle\frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot\big((\boldsymbol{E}_e.\boldsymbol{B})\cdot\boldsymbol{B} - B^2\cdot\boldsymbol{E}_e\big)}{n\cdot q\cdot\left\langle\frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle}\end{aligned}\tag{B.2.6}$$

Therefore:

$$n \cdot q \cdot \left(\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle + \frac{\left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle^2}{\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle} \cdot B^2 \right) \cdot \boldsymbol{E}_e = \boldsymbol{J} + \frac{\left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle}{\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle} \cdot \boldsymbol{J} \times \boldsymbol{B}$$
$$+ \left(n \cdot q \cdot \frac{\left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle^2}{\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle} - n \cdot q \cdot \left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^3}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle \right) \cdot (\boldsymbol{E}_e.\boldsymbol{B}) \cdot \boldsymbol{B} \tag{B.2.7}$$

Inserting equation (B.2.3) in (B.2.7) gives:

$$n \cdot q \cdot \left(\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle + \frac{\left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle^2}{\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle} \cdot B^2 \right) \cdot \boldsymbol{E}_e = \boldsymbol{J} + \frac{\left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle}{\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle} \cdot \boldsymbol{J} \times \boldsymbol{B}$$
$$+ \left(\frac{\left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle^2}{\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle} - \left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^3}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle \right) \cdot \frac{(\boldsymbol{J}.\boldsymbol{B}) \cdot \boldsymbol{B}}{\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle + \left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^3}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle \cdot B^2} \tag{B.2.8}$$

By identification with equation (B.1.17), we can express σ_n, R_H and P_H:

$$\sigma_n = n \cdot q \cdot \left(\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle + \frac{\left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle^2}{\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle} \cdot B^2 \right) \tag{B.2.9}$$

$$R_H = -\frac{1}{n \cdot q} \cdot \frac{\left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle}{\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle^2 + \left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2 \cdot B^2} \right\rangle^2 \cdot B^2} \tag{B.2.10}$$

$$P_H = \frac{\frac{\left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle^2}{\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle} - \left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^3}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle}{\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle + \left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^3}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle \cdot B^2} \cdot \frac{1}{n\cdot q\cdot\left(\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle + \frac{\left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle^2}{\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle}\cdot B^2\right)} \tag{B.2.11}$$

First order Taylor development of σ_n, $\mathbf{R}_H$ et $\mathbf{P}_H$ for any magnetic field

- First order expression of σ_n:

$$\sigma_n = n\cdot q\cdot\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle\cdot\left(1+\frac{\left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle^2}{\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle^2}\cdot B^2\right) \tag{B.2.12}$$

As seen in section 2.1.1 $(q\cdot\tau)/\mathrm{m}^* \approx 0{,}1\ m^2\cdot V^{-1}\cdot s^{-1}$, as a consequence:

$$\begin{aligned}\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle &\simeq \left\langle \frac{q\cdot\tau}{m^*}\left(1-\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2\right)\right\rangle \\ &\simeq \frac{q}{m^*}\cdot\langle\tau\rangle - \left(\frac{q}{m^*}\right)^3\cdot\langle\tau^3\rangle\cdot B^2\end{aligned} \tag{B.2.13}$$

Similarly,

$$\begin{aligned}\frac{\left\langle \frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle^2}{\left\langle \frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle^2} &\simeq \frac{\left\langle \left(\frac{q\cdot\tau}{m^*}\right)^2\cdot\left(1-\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2\right)\right\rangle^2}{\left\langle \frac{q\cdot\tau}{m^*}\cdot\left(1-\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2\right)\right\rangle^2} \\ &\simeq \frac{\left(\left(\frac{q}{m^*}\right)^2\cdot\langle\tau^2\rangle - \left(\frac{q}{m^*}\right)^4\cdot\langle\tau^4\rangle\cdot B^2\right)^2}{\left(\frac{q}{m^*}\cdot\langle\tau\rangle - \left(\frac{q}{m^*}\right)^3\cdot\langle\tau^3\rangle\cdot B^2\right)^2} \\ &\simeq \frac{\left(\frac{q}{m^*}\right)^4\cdot\langle\tau^2\rangle^2 - 2\left(\frac{q}{m^*}\right)^6\cdot\langle\tau^2\rangle\cdot\langle\tau^4\rangle\cdot B^2 + \left(\frac{q}{m^*}\right)^8\cdot\langle\tau^4\rangle^2\cdot B^4}{\left(\frac{q}{m^*}\right)^2\cdot\langle\tau\rangle^2 - 2\left(\frac{q}{m^*}\right)^4\cdot\langle\tau\rangle\cdot\langle\tau^3\rangle\cdot B^2 + \left(\frac{q}{m^*}\right)^6\cdot\langle\tau^3\rangle^2\cdot B^4} \\ &\simeq \left(\frac{q}{m^*}\right)^2\cdot\frac{\langle\tau^2\rangle^2}{\langle\tau\rangle^2}\end{aligned} \tag{B.2.14}$$

We can thus evaluate σ_n in equation (B.2.12) with (B.2.13) and (B.2.14), thus:

$$\begin{aligned}
\sigma_n &\simeq n\cdot q\cdot\frac{q}{m^*}\cdot\langle\tau\rangle\cdot\left(1-\left(\frac{q}{m^*}\right)^2\cdot\frac{\langle\tau^3\rangle}{\langle\tau\rangle}\cdot B^2\right)\cdot\left(1+\left(\frac{q}{m^*}\right)^2\cdot\frac{\langle\tau^2\rangle^2}{\langle\tau\rangle^2}\cdot B^2\right)\\
&\simeq n\cdot q\cdot\frac{q}{m^*}\cdot\langle\tau\rangle\cdot\left(1+\left(\frac{q}{m^*}\cdot\langle\tau\rangle\right)^2\cdot B^2\cdot\left(\frac{\langle\tau^2\rangle^2}{\langle\tau\rangle^4}-\frac{\langle\tau^3\rangle}{\langle\tau\rangle^3}\right)\right)\\
&\simeq n\cdot q\cdot\mu_n^*\cdot\left(1+{\mu_n^*}^2\cdot B^2\cdot\left(\frac{\langle\tau^2\rangle^2}{\langle\tau\rangle^4}-\frac{\langle\tau^3\rangle}{\langle\tau\rangle^3}\right)\right) \qquad \text{(B.2.15)}
\end{aligned}$$

- First order expression of $\mathbf{R}_H$:

$$R_H = -\frac{1}{n\cdot q}\cdot\frac{\left\langle\frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle}{\left\langle\frac{\frac{q\cdot\tau}{m^*}}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle^2+\left\langle\frac{\left(\frac{q\cdot\tau}{m^*}\right)^2}{1+\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2}\right\rangle^2\cdot B^2}=-\frac{1}{n\cdot q}\cdot\frac{N_{R_H}}{D_{R_H}} \qquad \text{(B.2.16)}$$

Taking each expression separately gives:

$$\begin{aligned}
N_{R_H} &\simeq \left\langle\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot\left(1-\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2\right)\right\rangle\\
&\simeq \left(\frac{q}{m^*}\right)^2\cdot\langle\tau^2\rangle-\left(\frac{q}{m^*}\right)^4\cdot\langle\tau^4\rangle\cdot B^2 \qquad \text{(B.2.17)}
\end{aligned}$$

and

$$\begin{aligned}
D_{R_H} &\simeq \left\langle\frac{q\cdot\tau}{m^*}\cdot\left(1-\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2\right)\right\rangle^2+\left\langle\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot\left(1-\left(\frac{q\cdot\tau}{m^*}\right)^2\cdot B^2\right)\right\rangle^2\cdot B^2\\
&\simeq \left(\frac{q}{m^*}\cdot\langle\tau\rangle-\left(\frac{q}{m^*}\right)^3\cdot\langle\tau^3\rangle\cdot B^2\right)^2\\
&\quad+\left(\left(\frac{q}{m^*}\right)^2\cdot\langle\tau^2\rangle-\left(\frac{q}{m^*}\right)^4\cdot\langle\tau^4\rangle\cdot B^2\right)^2\cdot B^2 \qquad \text{(B.2.18)}
\end{aligned}$$

Neglecting high-order magnetic field terms (higher than 2), the above equation becomes:

$$D_{R_H} \simeq \left(\frac{q}{m^*}\right)^2\cdot\langle\tau\rangle^2-2\left(\frac{q}{m^*}\right)^4\cdot\langle\tau\rangle\cdot\langle\tau^3\rangle\cdot B^2+\left(\frac{q}{m^*}\right)^4\cdot\langle\tau^2\rangle^2\cdot B^2 \qquad \text{(B.2.19)}$$

Thus equation (B.2.16) of parameter R_H can be rewritten:

$$\begin{aligned}
R_H &\simeq -\frac{1}{n\cdot q}\cdot\frac{\left(\frac{q}{m^*}\right)^2\cdot\langle\tau^2\rangle-\left(\frac{q}{m^*}\right)^4\cdot\langle\tau^4\rangle\cdot B^2}{\left(\frac{q}{m^*}\right)^2\cdot\langle\tau\rangle^2+\left(\left(\frac{q}{m^*}\right)^4\cdot\langle\tau^2\rangle^2-2\left(\frac{q}{m^*}\right)^4\cdot\langle\tau\rangle\cdot\langle\tau^3\rangle\right)\cdot B^2}\\
&\simeq -\frac{1}{n\cdot q}\cdot\frac{\langle\tau^2\rangle}{\langle\tau\rangle^2}\cdot\frac{1-\left(\frac{q}{m^*}\right)^2\cdot\frac{\langle\tau^4\rangle}{\langle\tau^2\rangle}\cdot B^2}{1+\frac{\left(\frac{q}{m^*}\right)^2\cdot\langle\tau^2\rangle^2-2\left(\frac{q}{m^*}\right)^2\cdot\langle\tau\rangle\cdot\langle\tau^3\rangle}{\langle\tau\rangle^2}\cdot B^2}\\
&\simeq -\frac{1}{n\cdot q}\cdot\frac{\langle\tau^2\rangle}{\langle\tau\rangle^2}\cdot\left(1-\left(\frac{q}{m^*}\right)^2\cdot\frac{\langle\tau^4\rangle}{\langle\tau^2\rangle}\cdot B^2\right)\cdot\left(1-\frac{\left(\frac{q}{m^*}\right)^2\cdot\langle\tau^2\rangle^2-2\left(\frac{q}{m^*}\right)^2\cdot\langle\tau\rangle\cdot\langle\tau^3\rangle}{\langle\tau\rangle^2}\cdot B^2\right)\\
&\simeq -\frac{1}{n\cdot q}\cdot\frac{\langle\tau^2\rangle}{\langle\tau\rangle^2}\cdot\left(1-\left(\left(\frac{q}{m^*}\right)^2\cdot\frac{\langle\tau^4\rangle}{\langle\tau^2\rangle}+\frac{\left(\frac{q}{m^*}\right)^2\cdot\langle\tau^2\rangle^2-2\left(\frac{q}{m^*}\right)^2\cdot\langle\tau\rangle\cdot\langle\tau^3\rangle}{\langle\tau\rangle^2}\right)\cdot B^2\right)\\
&\simeq -\frac{1}{n\cdot q}\cdot\frac{\langle\tau^2\rangle}{\langle\tau\rangle^2}\cdot\left(1-\left(\frac{q\cdot\langle\tau\rangle}{m^*}\right)^2\cdot\left(\frac{\langle\tau^4\rangle}{\langle\tau^2\rangle\cdot\langle\tau\rangle^2}+\frac{\langle\tau^2\rangle^2}{\langle\tau\rangle^4}-2\frac{\langle\tau^3\rangle}{\langle\tau\rangle^3}\right)\cdot B^2\right) \qquad \text{(B.2.20)}
\end{aligned}$$

Finally:

$$R_H \simeq -\frac{1}{n\cdot q}\cdot\frac{\langle\tau^2\rangle}{\langle\tau\rangle^2}\cdot\left(1-\mu_n^{*2}\cdot\left(\frac{\langle\tau^4\rangle}{\langle\tau^2\rangle\cdot\langle\tau\rangle^2}+\frac{\langle\tau^2\rangle^2}{\langle\tau\rangle^4}-2\frac{\langle\tau^3\rangle}{\langle\tau\rangle^3}\right)\cdot B^2\right) \qquad \text{(B.2.21)}$$

B.3 COMSOL Multiphysics® implementation

As expressed in equation 2.1.10, the electron current density is given by:

$$\boldsymbol{J_n} = n \cdot q \cdot \left(\frac{q}{m^*} \cdot \langle \tau \rangle \cdot \mathbf{E_e} - \left(\frac{q}{m^*} \right)^2 \cdot \left\langle \tau^2 \right\rangle \cdot \mathbf{E_e} \times \mathbf{B} + \left(\frac{q \cdot}{m^*} \right)^3 \cdot \left\langle \tau^3 \right\rangle \cdot (\mathbf{E_e} \cdot \mathbf{B}) \cdot \mathbf{B} \right) \tag{B.3.1}$$

The electron mobility μ_n is defined as:

$$\mu_n = \frac{q}{m^*} \langle \tau \rangle \tag{B.3.2}$$

Thus, equation B.3.1 can be rewritten as:

$$\boldsymbol{J_n} = n \cdot q \cdot \left(\mu_n \cdot \mathbf{E_e} - \mu_n^2 \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot \mathbf{E_e} \times \mathbf{B} + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot (\mathbf{E_e} \cdot \mathbf{B}) \cdot \mathbf{B} \right) \tag{B.3.3}$$

Furthermore $-q \cdot n \cdot \langle \boldsymbol{\nu_n} \rangle$, thus:

$$\langle \boldsymbol{\nu_n} \rangle = -\mu_n \cdot \mathbf{E_e} + \mu_n^2 \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot \mathbf{E_e} \times \mathbf{B} - \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot (\mathbf{E_e} \cdot \mathbf{B}) \cdot \mathbf{B} \tag{B.3.4}$$

After developing along each axis, the previous equation becomes:

$$\begin{aligned} \begin{pmatrix} \langle \nu_{nx} \rangle \\ \langle \nu_{ny} \rangle \\ \langle \nu_{nz} \rangle \end{pmatrix} = & -\mu_n \cdot \begin{pmatrix} E_x \\ E_y \\ E_z \end{pmatrix} + \mu_n^2 \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot \begin{pmatrix} B_z \cdot E_y - B_y \cdot E_z \\ B_x \cdot E_z - B_z \cdot E_x \\ B_y \cdot E_x - B_x \cdot E_y \end{pmatrix} - \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \\ & -\mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot \begin{pmatrix} B_x^2 \cdot E_x - B_x \cdot B_y \cdot E_y + B_x \cdot B_z \cdot E_z \\ B_x \cdot B_y \cdot E_x - B_y^2 \cdot E_y + B_y \cdot B_z \cdot E_z \\ B_x \cdot B_z \cdot E_x - B_y \cdot B_z \cdot E_y + B_z^2 \cdot E_z \end{pmatrix} \end{aligned} \tag{B.3.5}$$

which can be rewritten as:

$$\begin{aligned} \begin{pmatrix} \langle \nu_{nx} \rangle \\ \langle \nu_{ny} \rangle \\ \langle \nu_{nz} \rangle \end{pmatrix} = - & \left[\begin{array}{l} \left(\mu_n + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_x^2 \right) \cdot E_x + \left(-\mu_n^2 \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot B_z + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_x \cdot B_y \right) \cdot E_y \\ \left(\mu_n^2 \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot B_z + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_x \cdot B_y \right) \cdot E_x + \left(\mu_n + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_y^2 \right) \cdot E_y \\ \left(-\mu_n^2 \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot B_y + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_x \cdot B_z \right) \cdot E_x + \left(\mu_n^2 \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot B_x + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \right. \end{array} \right. \\ & \left. \begin{array}{l} + \left(\mu_n^2 \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot B_y + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_x \cdot B_z \right) \cdot E_z \\ + \left(-\mu_n^2 \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot B_x + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_y \cdot B_z \right) \cdot E_z \\ \cdot B_y \cdot B_z) \cdot E_y + \left(\mu_n + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_z^2 \right) \cdot E_z \end{array} \right] \end{aligned} \tag{B.3.6}$$

with:

$$\frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} = -n \cdot q \cdot R_H \tag{B.3.7}$$

and

$$\frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} = (n \cdot q \cdot R_H)^2 - \frac{n \cdot q}{\mu_n} \cdot P_H \tag{B.3.8}$$

Here R_H and P_H are respectively the Hall coefficient and the planar Hall coefficient [8].

In COMSOL Multiphysics® the relevant parameter is the mobility linked to the drift velocity by $\boldsymbol{\nu_n} = \mu_n \cdot \boldsymbol{E}$. Thus an equivalent electron mobility tensor can be identified from equation B.3.6:

$$\mu_n(B) = \begin{pmatrix} \left(\mu_n + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_x^2\right) & \left(-\mu_n^2 \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot B_z + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_x \cdot B_y\right) & \left(\mu_n^2 \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot B_y + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_x \cdot B_z\right) \\ \left(\mu_n^2 \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot B_z + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_x \cdot B_y\right) & \left(\mu_n + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_y^2\right) & \left(-\mu_n^2 \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot B_x + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_y \cdot B_z\right) \\ \left(-\mu_n^2 \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot B_y + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_x \cdot B_z\right) & \left(\mu_n^2 \cdot \frac{\langle \tau^2 \rangle}{\langle \tau \rangle^2} \cdot B_x + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_y \cdot B_z\right) & \left(\mu_n + \mu_n^3 \cdot \frac{\langle \tau^3 \rangle}{\langle \tau \rangle^3} \cdot B_z^2\right) \end{pmatrix} \tag{B.3.9}$$

Appendix C

Single- and bi-current SCT integrated circuits

C.1 Single and bi-current SCT circuit

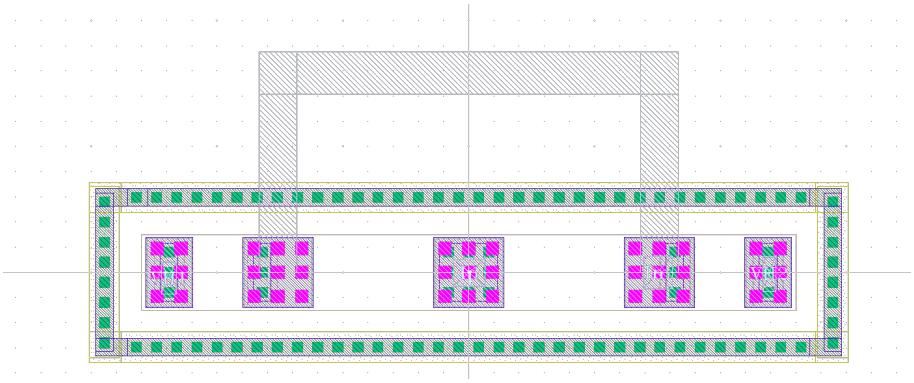


Figure C.1 – Layout plot of the $3\mu m$ width LV-VHD transducer.

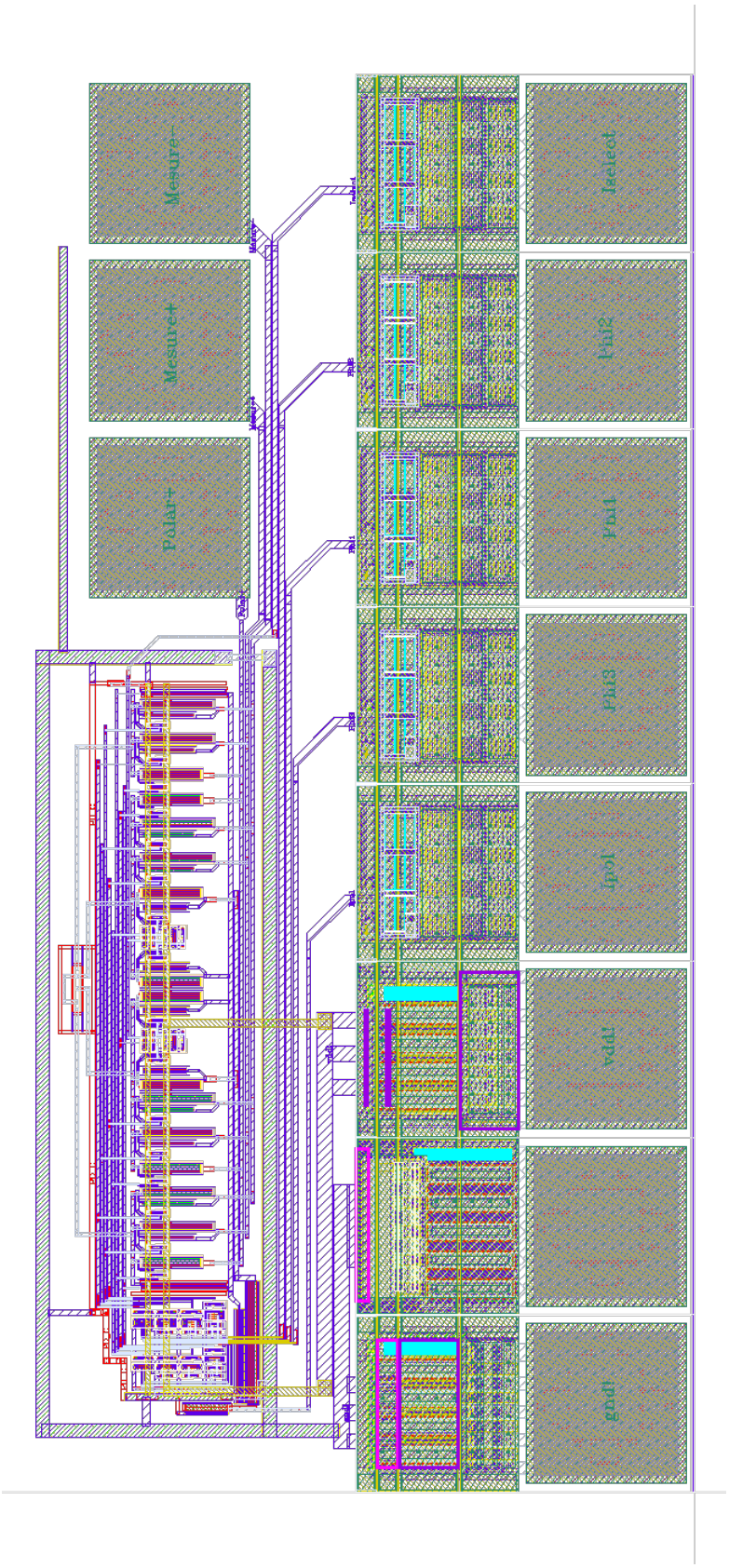
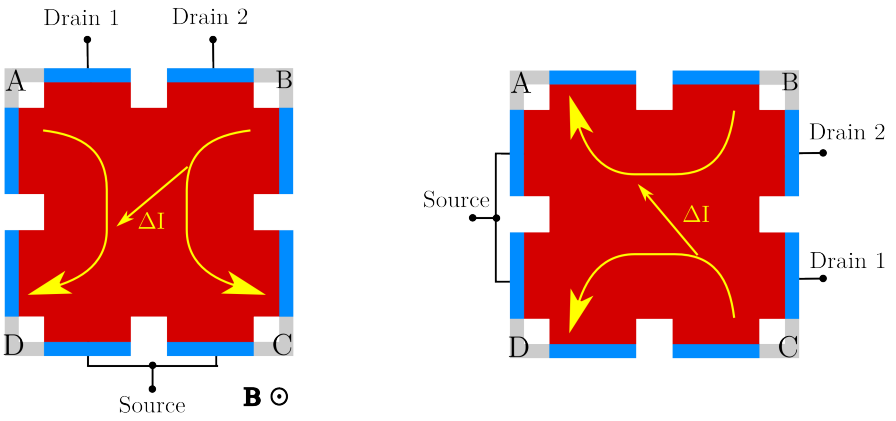


Figure C.2 – Full layout plot of the integrated circuit with single and bi-current SCT.

Appendix D

CHOPFET

D.1 Modulation switching pattern



(a) Phase $\phi 1$

(b) Phase $\phi 2$

(c) Phase $\phi 3$

(d) Phase $\phi 4$

Figure D.1 – Spinning current technique applied to the CHOPFET.

D.2 CHOPFET layout

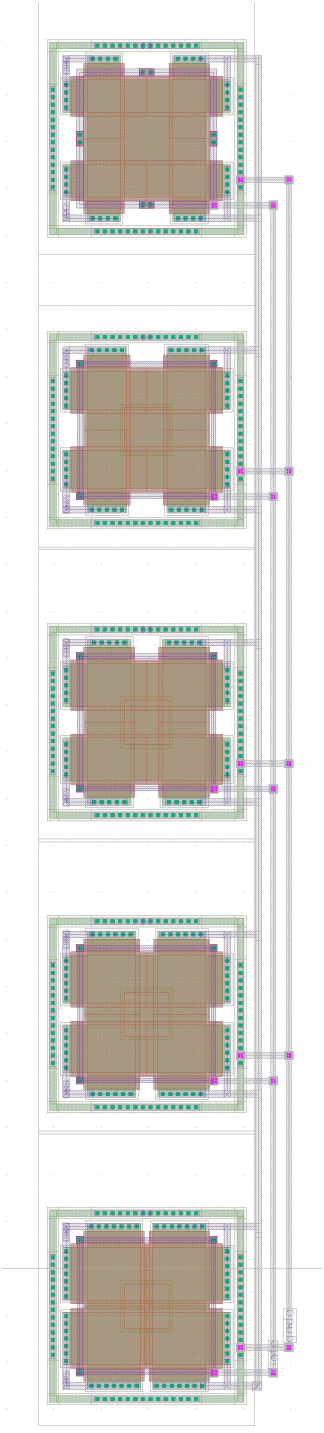


Figure D.2 – Layout plot of a set of CHOPFETs with different drain gap d from $4.7\,\mu m$ to $0.5\,\mu m$ in AMS $0.35\,\mu m$ process.

D.3 CHOPFET conditioning and signal processing

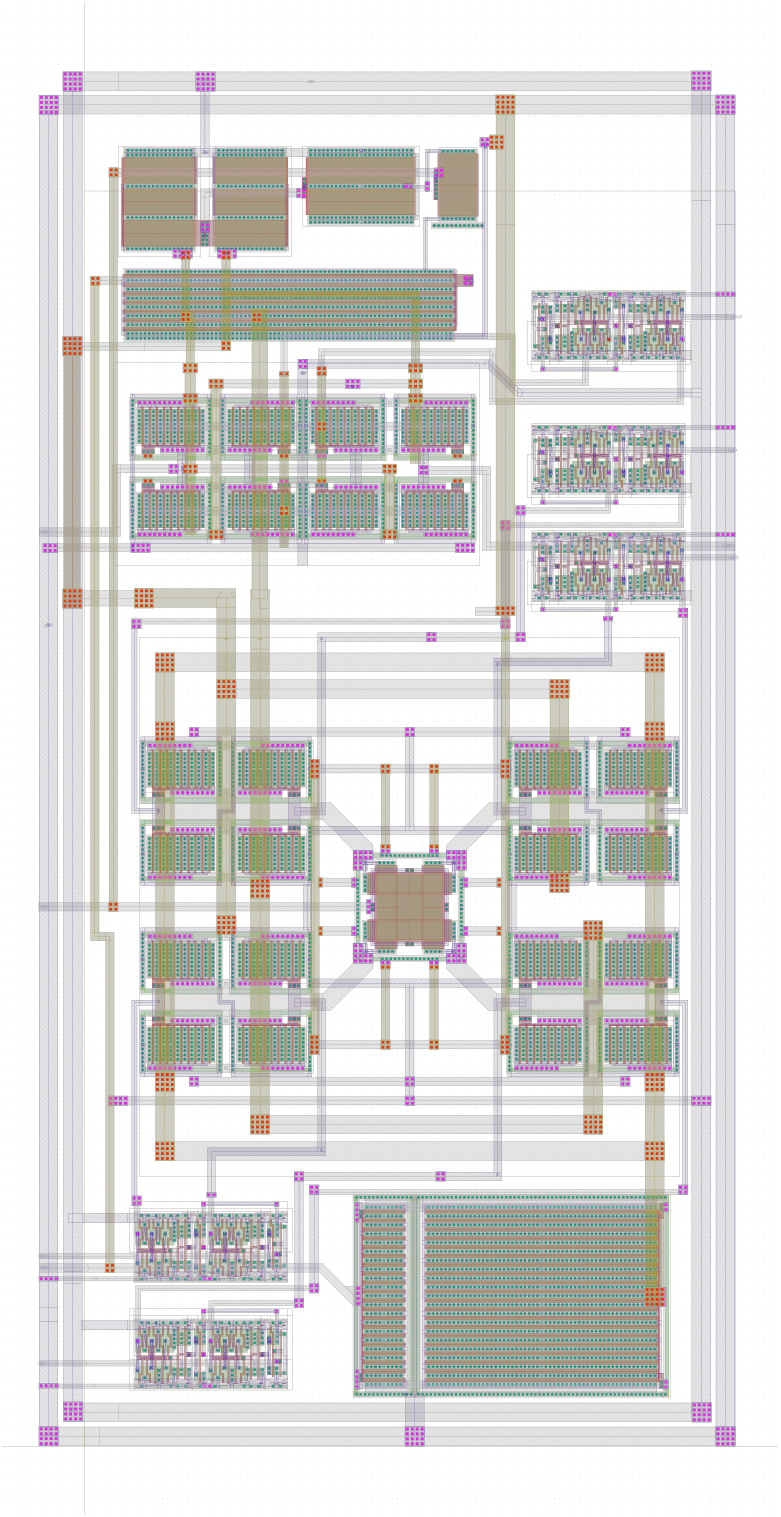


Figure D.3 – Layout plot of the differential CHOPFET-based integrated circuit in AMS $0.35\mu m$ CMOS process.

D.4 First MOP prototype: MOP018_1 CORALIE

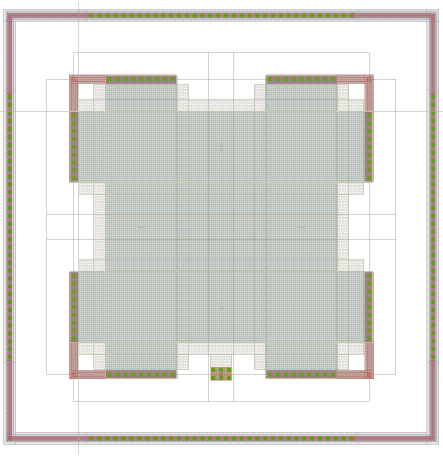


Figure D.4 – Layout plot of the CHOPFET in AMS 0.18 μm CMOS process.

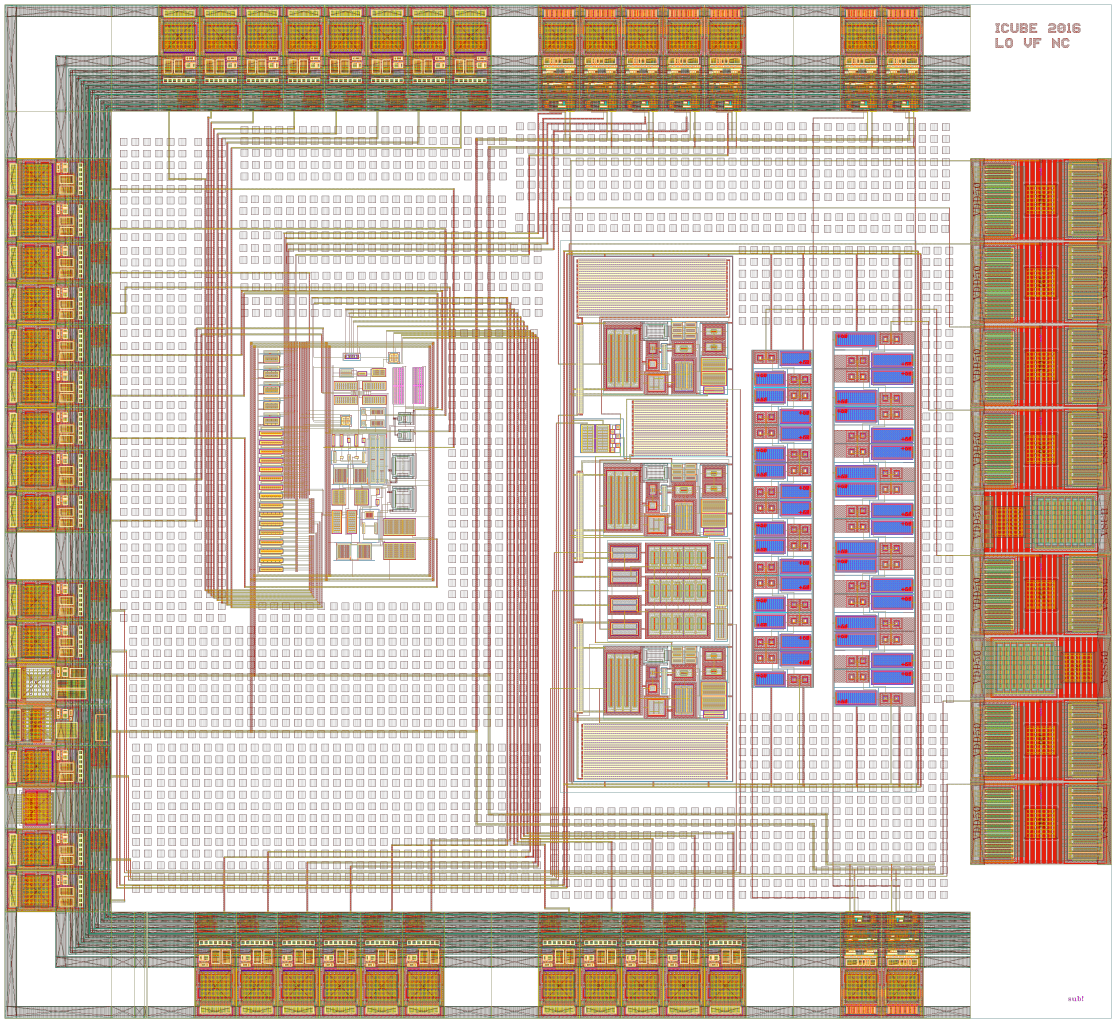


Figure D.5 – Layout plot of the integrated circuit MOP018_1 CORALIE in AMS 0.18 μm CMOS process.

D.5 Second MOP prototype: MOP018_2 VITTORIA

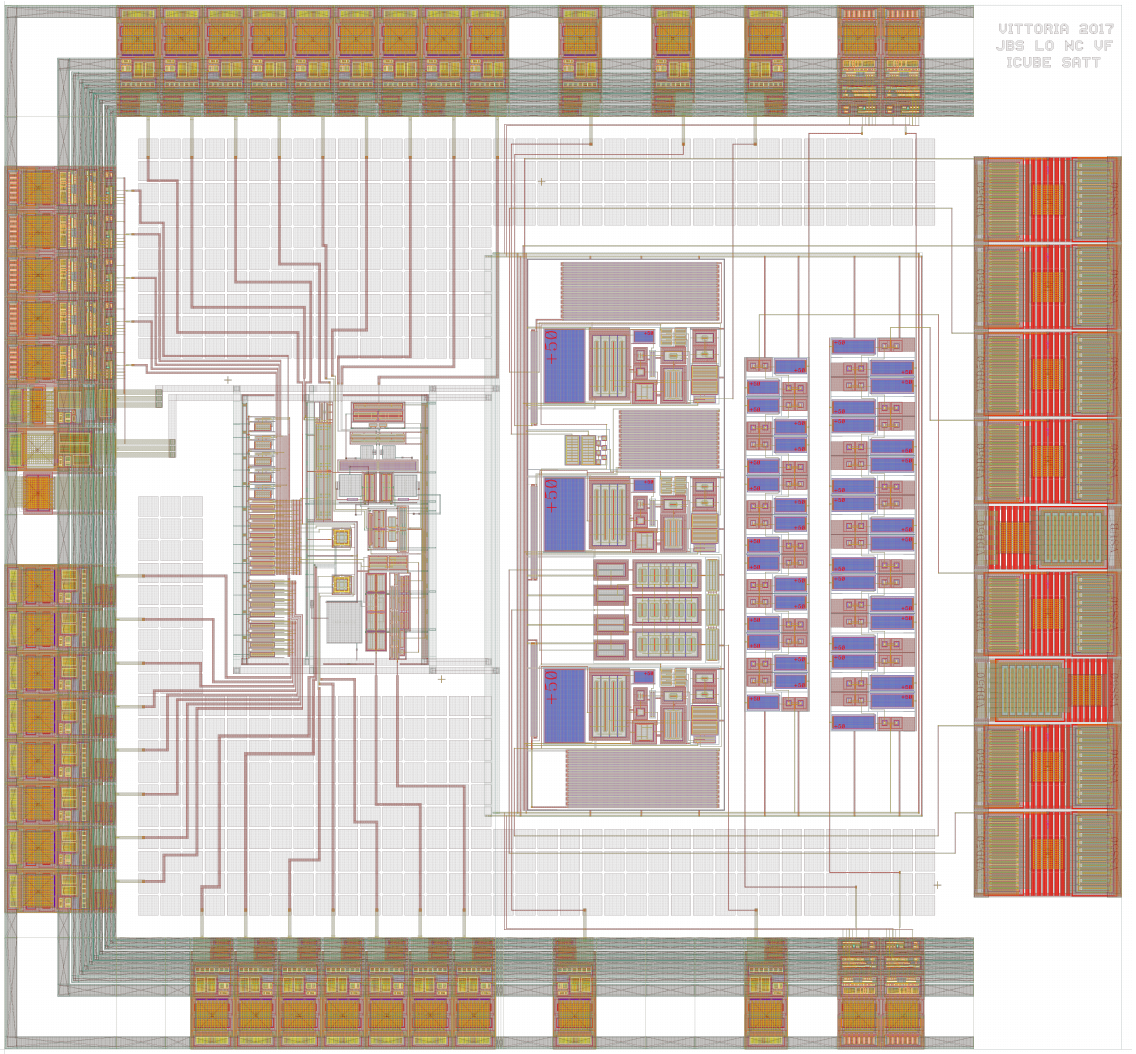


Figure D.6 – Layout plot of the integrated circuit MOP018_2 VITTORIA in AMS 0.18 μm CMOS process.

Appendix E

Résumé

Titre : Étude des magnétomètres haute performance intégrés en technologie silicium.

Doctorant : Laurent Osberger
Directeur de thèse : Vincent Frick
Laboratoire ICube / Université de Strasbourg

La thématique de mon sujet de thèse porte sur l'étude des capteurs de champ magnétique intégrés en technologie silicium. Ce type de capteur, utilisant les procédés standards de la microélectronique, est très répandu dans de nombreux secteurs tels que l'industrie automobile, les applications grand public, la médecine, etc. Outre la mesure de champs magnétiques, ils permettent de mesurer d'autres grandeurs telles que le courant électrique, la position, les angles ou la vitesse. Dans ce travail nous avons fait le choix de nous concentrer uniquement sur les technologies CMOS standard, c'est à dire permettant la réalisation de capteurs magnétiques sans étapes de fabrication particulières. Les technologies CMOS offrent de nombreux avantages. En l'occurrence, elles permettent d'intégrer sur un même substrat, à la fois, le transducteur magnétique (l'élément sensible qui transforme le champ magnétique en une grandeur électrique) et son électronique de conditionnement afin de former un capteur magnétique. Cette co-intégration permet, via l'utilisation de techniques spécifiques, d'améliorer significativement les performances du capteur telles que sa résolution, son offset ou encore sa stabilité en température. En outre, le coût de production à l'échelle industrielle des circuits en technologie CMOS est très faible. Les travaux présentés dans cette thèse portent plus particulièrement sur deux types de transducteur, le transducteur à effet Hall dit « vertical » (LV-VHD) et le un magnéto-transistor appelé « CHOPFET ».

E.1 LV-VHD

Les transducteurs à effet Hall peuvent être de type horizontal (sensible au champ magnétique perpendiculaire à la surface du circuit intégré) ou vertical (sensible au champ parallèle, figure E.1). Si la connaissance du premier est maîtrisée depuis de nombreuses années, celle du second reste en revanche largement perfectible. En l'occurrence, de par sa structure particulière, ses

performances sont plus faibles que celles du transducteur horizontal. La figure E.1 illustre l'intégration du transducteur à effet Hall vertical en technologie CMOS (a) haute tension (HV-VHD) et (b) basse tension (LV-VHD). La première partie de cette thèse a donc été consacrée à l'étude approfondie du transducteur vertical compatible avec les technologies CMOS standards basse-tension, le LV-VHD.

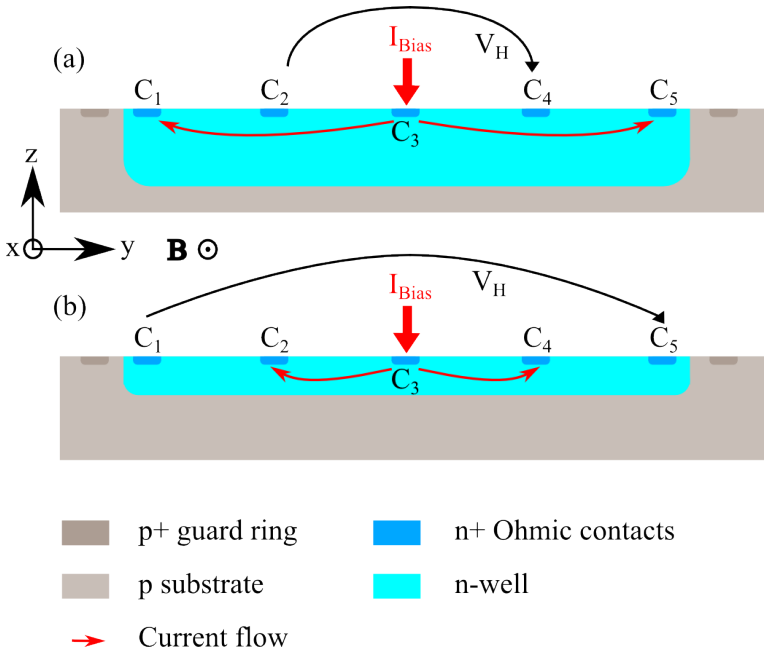


FIGURE E.1 – (a) HV-VHD avec option haute-tension et caisson profond, (b) LV-VHD intégré dans un caisson peu profond.

Dans un premier temps, des travaux de modélisation par éléments finis (FEM) à deux dimensions ont été réalisés afin d'optimiser le LV-VHD et d'approfondir la compréhension de son comportement. Un modèle tenant compte des phénomènes de conduction et de diffusion des porteurs de charges a été développé. Il a été enrichit par la prise en compte des principaux effets de second ordre tels que la modulation de la zone de charge d'espace et la saturation de la vitesse des porteurs. L'ajustement des paramètres du modèle à la technologie CMOS AMS 0,35 µm ont permis sa comparaison à des LV-VHD prototypes fabriqués dans cette même technologie, ce qui a conduit à sa validation (figure E.2).

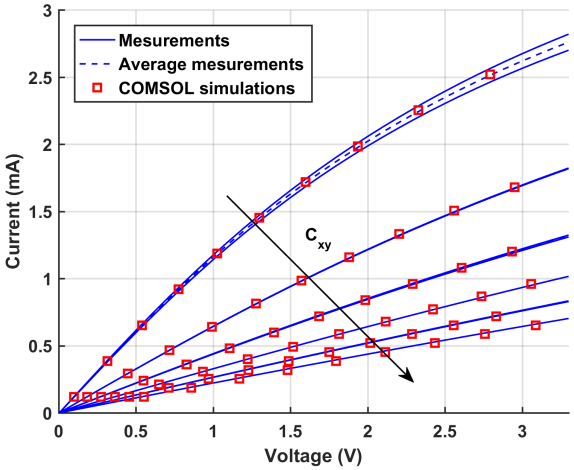


FIGURE E.2 – Mesures et simulations des caractéristiques courant/tension entre toutes les paires de contacts C_{xy}.

Dans un second temps nous sommes intéressés aux techniques de conditionnement du LV-VHD. Dans la plupart des applications, la bande passante est généralement limitée à quelques kilohertz. Dans ce cas, le principal facteur limitant la résolution du transducteur est le bruit en 1/f. Une technique classique, appelée « spinning current », permettant d'éliminer efficacement ce bruit ainsi que l'offset, consiste à inverser périodiquement les contacts de mesures et de polarisations du transducteur (figure E.3). Cette technique, généralement appliquée aux

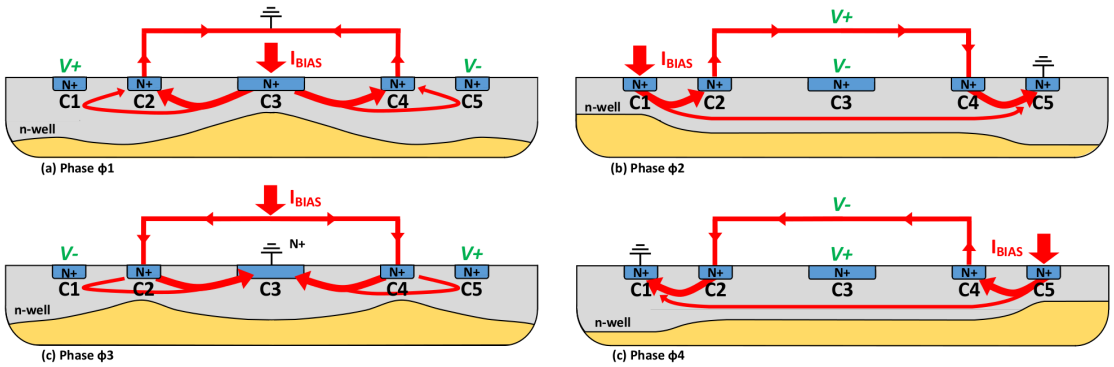
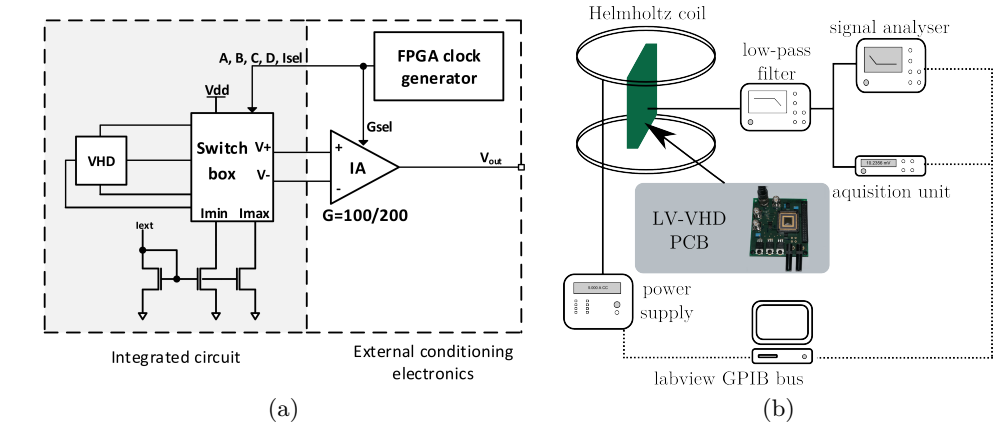


FIGURE E.3 – Technique du « spinning current » à adapté au LV-VHD.

transducteurs horizontaux a été adaptée au LV-VHD en tenant compte des particularités propres à ce transducteur. En effet, contrairement au transducteur à effet Hall horizontal, la résistance d'entrée (résistance mesurée entre les contacts de polarisation) varie selon les modes d'utilisation du transducteur. Nous avons donc proposé de polariser le transducteur à courant maximum quel que soit son mode de polarisation ($I_{min} = 550\,\mu A$ en phase $\phi 2/\phi 4$, et $I_{max} = 1100\,\mu A$ en phase $\phi 1/\phi 3$) afin d'augmenter le rapport signal à bruit. Ce nouveau concept a d'abord été évalué analytiquement puis par simulation FEM. Le bruit en 1/f a été modélisé afin d'évaluer l'efficacité de cette technique.

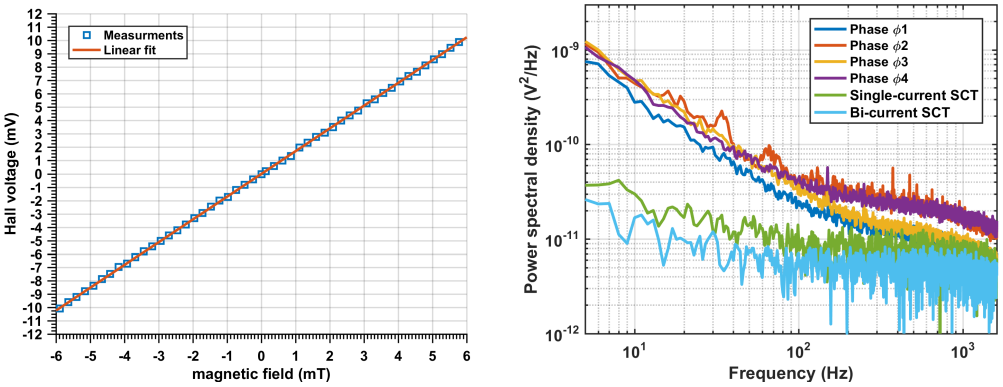
Les résultats prometteurs ont mené à la fabrication de deux prototypes de circuits intégrés (figure E.4). Les caractérisations de ces circuits ont permis de mettre en évidence une



(a) (b)

FIGURE E.4 – (a) Chaine instrumentale et (b) banc de test.

amélioration significative de la résolution, de 100 µT à 20 µT (figure E.5).



(a) (b)

FIGURE E.5 – (a) Caractéristique de transfert du capteur et (b) densité spectrale de puissance de bruit.

E.2 CHOPFET

Le second type de transducteur étudié, nommé CHOPFET, est une évolution d'un transducteur de type MagFET (figure E.6a) dont la structure a été modifiée afin de le rendre compatible avec les techniques de réductions du bruit. Un MagFET est un transistor MOS (généralement de type n) dont le drain a été séparé en plusieurs parties. Sous l'effet du champ magnétique, les électrons circulant dans le canal du transistor sont déviés vers l'un ou de l'autre drain. Ce phénomène induit une différence de courant, variant linéairement avec le champ magnétique, entre les drains. Le CHOPFET (inventé par Vincent Frick en 2010, cf. figure E.6b) est un MagFET symétrisé par rotation de 90°. Si le concept de compatibilité avec la technique du « spinning current » avait initialement été vérifié dans sa globalité (transducteur et électronique de conditionnement associée), il était néanmoins primordial de pouvoir vérifier le degré de corrélation du bruit en 1/f sur le transducteur seul. Dans ce but, nous

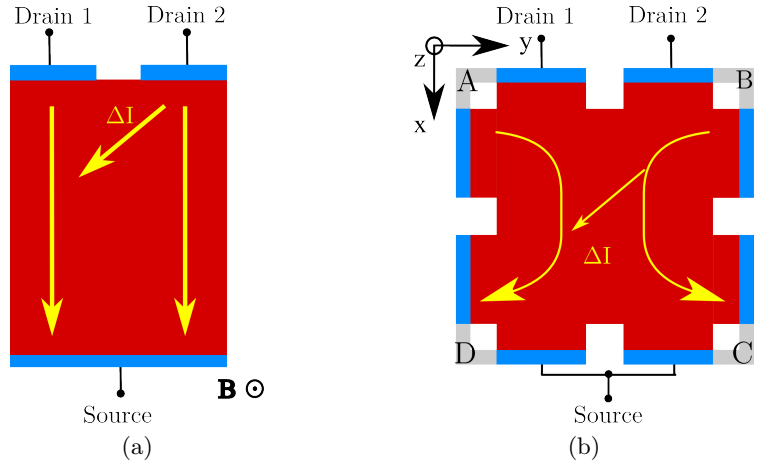


FIGURE E.6 – Transducteur (a) MagFET et (b) CHOPFET.

avons réalisé un circuit prototype qui a permis de vérifier cette hypothèse.

Les travaux ont alors porté sur la modélisation du CHOPFET afin d'en explorer les possibilités optimisation. Un premier modèle 2D FEM a été réalisé et confronté à des mesures expérimentales. Ce modèle, intégrant les effets galvano-magnétiques, a permis de simuler le fonctionnement du CHOPFET pour une polarisation donnée et d'en évaluer la sensibilité. Il ne permettait cependant pas de modéliser le transducteur en régime linéaire et n'était donc pas suffisant pour décrire avec précision le CHOPFET.

Un modèle 3D a alors été développé afin d'optimiser à la fois la géométrie du capteur et son mode de polarisation (figure E.7). Ce modèle 3D permet aujourd'hui de simuler le CHOPFET quelle que soit sa polarisation et d'obtenir une estimation fidèle de sa sensibilité. Le modèle a été validé par comparaison avec un jeu de cinq CHOPFETs caractérisés expérimentalement. Il a notamment permis d'identifier la géométrie et la polarisation optimale du CHOPFET afin d'en maximiser sa sensibilité.

En outre, la résolution d'un capteur étant limitée à la fois par sa sensibilité et son niveau de bruit, une étude complémentaire portant sur le bruit du CHOPFET a été menée (figure E.8). En partant du postulat selon lequel le bruit en 1/f est éliminé par la technique du « spinning-current », la principale source de bruit ayant un impact sur la résolution est de nature thermique (indépendante de la fréquence). Nous avons donc étudié l'évolution du bruit thermique en fonction de la polarisation du CHOPFET. Des mesures ont permis d'identifier deux stratégies de polarisation : une première permettant d'avoir la meilleure résolution possible (autour de 3 µT) et une seconde permettant de réduire significativement la consommation électrique pour une résolution donnée.

Afin de permette la réalisation de capteurs magnétiques haute-résolution à base de CHOPFET, il a été nécessaire d'entreprendre une réflexion approfondie sur les différentes architectures de conditionnement bas-bruit adjointes. Le CHOPFET étant avant tout un transistor, nous avons proposé de l'intégrer dans une architecture d'amplificateur opérationnel, appelée MOP (Magneto-Operational Amplifier). La sortie du MOP dépend de la tension d'entrée mais

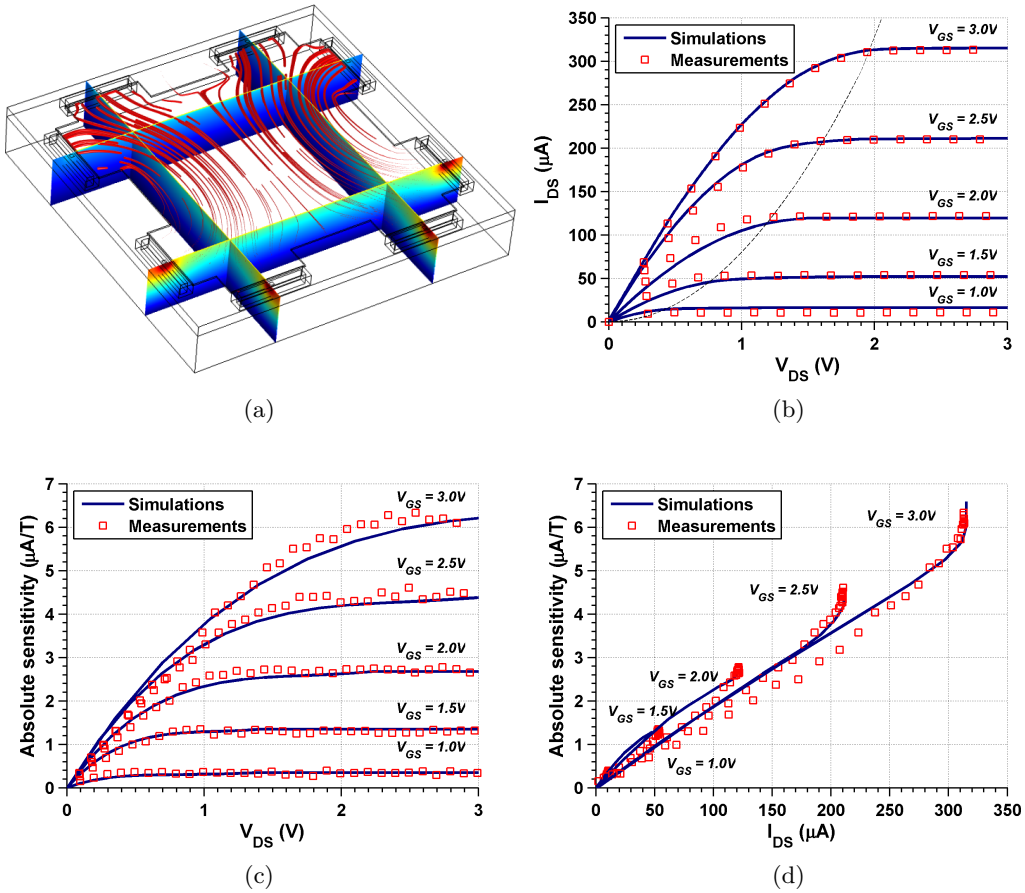


FIGURE E.7 – Simulations FEM 3D : (a) Potentiel électrique et lignes de courant, (b) caractéristiques courant/tension, (c) et (d) sensibilité respectivement en fonction de I_{DS} et V_{DS}.

également du champ magnétique. Une réflexion a été mené afin de déterminer l'emplacement du CHOPFET dans le MOP permettant de pouvoir régler le transducteur et indépendamment du reste de l'architecture (ces travaux font actuellement l'objet d'un dépôt de brevet européen et international). L'architecture du MOP a également été adaptée pour permettre la suppression du bruit en 1/f et de l'offset du CHOPFET mais aussi de l'électronique adjointe. Un premier prototype de MOP réalisé en technologie CMOS AMS 0,18 µm a été envoyé en fabrication. Ce prototype a permis de valider le concept du MOP mais en raison d'un défaut dans l'étage d'asservissement du mode commun il n'a pas permis d'atteindre les performances attendues (figure E.9). Un second prototype, corrigeant ce défaut, a été conçu et envoyé en fabrication. Sa caractérisation est prévue pour le mois de juin 2017.

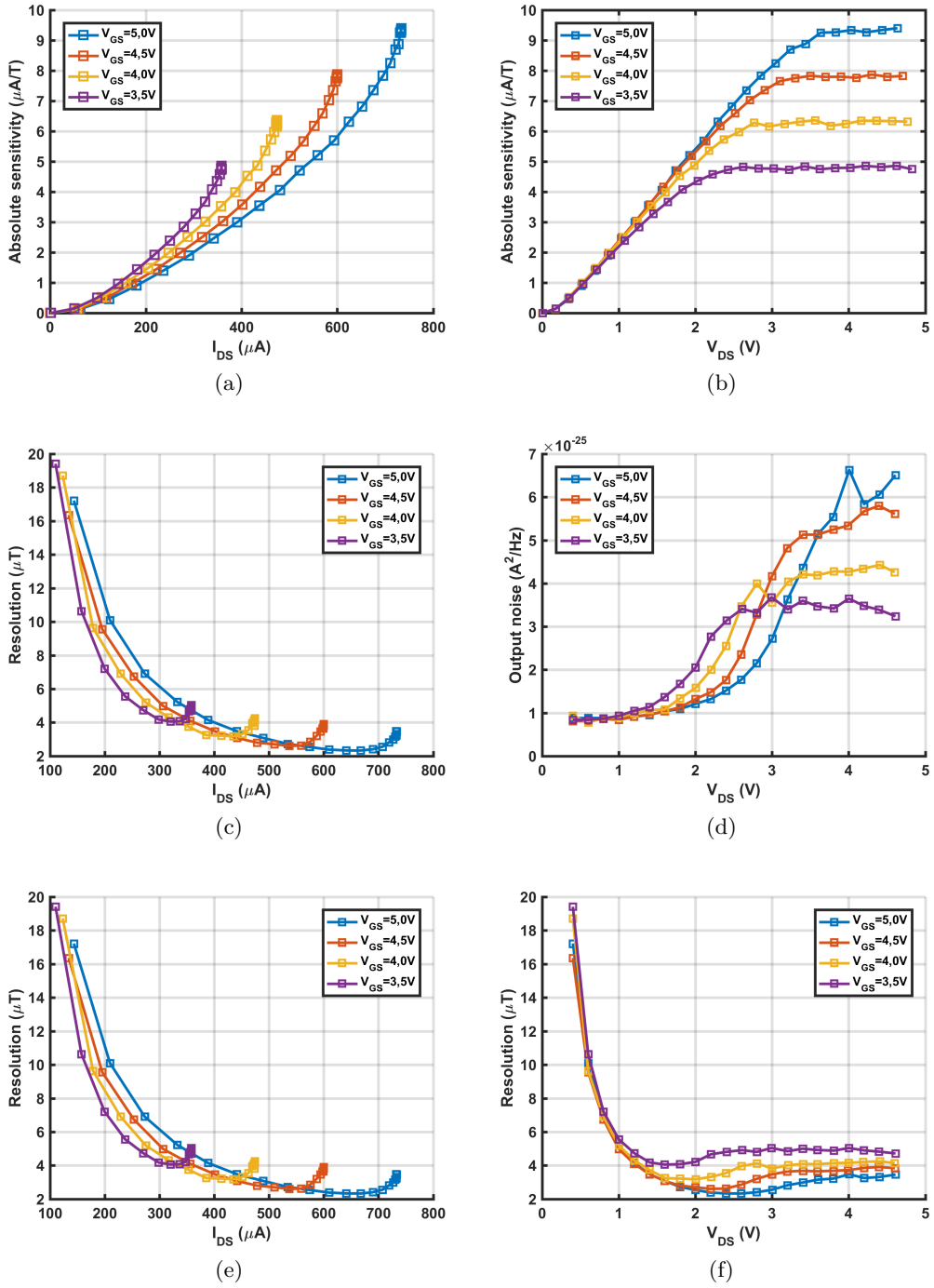
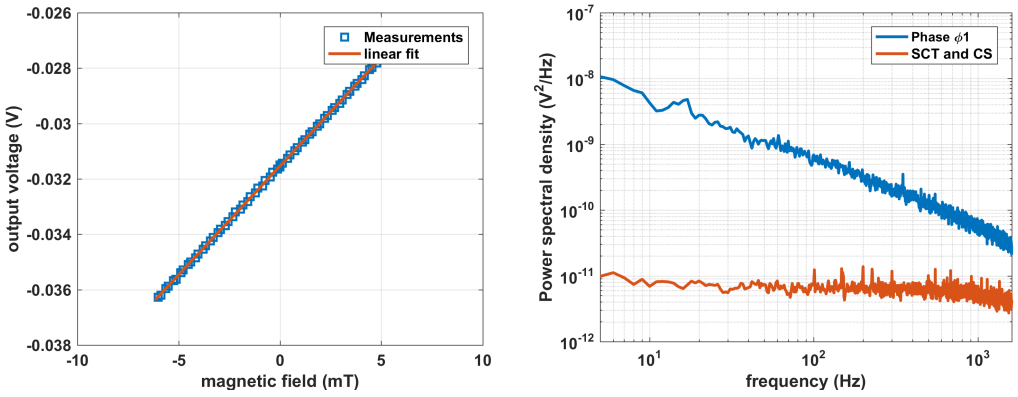


FIGURE E.8 – (a) et (b) sensibilité respectivement en fonction de I_{DS} et V_{DS}, (c) et (d) densité spectrale de puissance de bruit à $100\,kHz$ respectivement en fonction de I_{DS} et V_{DS}, (e) et (f) estimation de la résolution sur une bande passante de $[5\,Hz - 1.6\,kHz]$ respectivement en fonction de I_{DS} et V_{DS}.



(a) (b)

FIGURE E.9 – Résultats expérimentaux du premier prototype de MOP : (a) caractéristique de transfert, et (b) densité spectrale de puissance de bruit en phase ϕ1 et en appliquant le « spinning current » associé à la stabilisation par découpage.

Laurent OSBERGER

Etude de magnétomètres haute performance intégrés en technologie silicium

Résumé

La thématique de ce sujet de thèse porte sur l'étude des capteurs de champ magnétique intégrés en technologie CMOS standard basse tension sans étapes de fabrication supplémentaires. La co-intégration du transducteur (l'élément sensible qui transforme le champ magnétique en une grandeur électrique) et de son électronique de conditionnement du signal sur la même puce permet réaliser des fonctions spécifiques qui améliorent significativement les performances du capteur. Les travaux présentés dans cette thèse portent plus particulièrement sur deux types de transducteur : le transducteur à effet Hall dit vertical et un magnéto-transistor particulier appelé « CHOPFET ». Nous avons développé des modèles numériques de ces transducteurs afin d'analyser finement leurs comportement mais aussi d'optimiser leurs performances. En nous basant sur ces résultats, nous avons adapté des techniques de traitement du signal et proposé plusieurs architectures originales dédiées au conditionnement du signal magnétique. Cela a permis d'améliorer significativement les performances de ces capteurs en termes de résolution, d'offset et de consommation électrique.

Mots clefs : capteur de champ magnétique, technologie CMOS, transducteur à effet Hall vertical, CHOPFET.

Abstract

The subject of thesis subject concerns the study of magnetic field sensors integrated in low-voltage standard CMOS process without additional post-processing steps. Co-integrating the magnetic transducer (the sensitive element transforming the magnetic field into an electrical quantity) together with its conditioning electronics onto a same chip allows to implement specific features, which dramatically improve the sensor performances. This work particularly focuses on two types of transducer: the vertical Hall device and a specific magneto-transistor called "CHOPFET". We developed numerical simulation models in order to predict and optimize the behavior of these transducers. Based on the results, we adapted dedicated signal processing techniques and proposed several innovative magnetic signal conditioning architectures. This led to significant improvement in terms of resolution, offset and power consumption.

Keywords: magnetic field sensor, CMOS technology, vertical Hall device, CHOPFET.