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# UTBB FDSOI MOSFET DYNAMIC BEHAVIOR STUDY AND MODELING FOR ULTRA-LOW POWER RF and mm-WAVE IC DESIGN

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بِسْمِ اللَّهِ الرَّحْمَنِ الرَّحِيمِ

﴿وَمَا يُلَقَّاهَا إِلَّا الَّذِينَ صَبَرُوا وَمَا يُلَقَّاهَا إِلَّا ذُو حَظٍّ عَظِيمٍ﴾

"And no one will be granted such goodness except those who exercise patience and self-restraint, none but persons of the greatest good fortune."
Quran, Surat 41, Ver. 35.

To my parents, my wife and my son

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# Abstract

This research work has been motivated primarily by the significant advantages brought about by the UTBB FDSOI technology to the Low power Analog and RF applications. The main goal is to study the dynamic behavior of the UTBB FDSOI MOSFET in light of the recent technology advances and to propose predictive models and useful recommendations for RF IC design with particular emphasis on Moderate Inversion regime. After a brief review of progress in MOSFET architectures introduced in the semiconductor industry, a state-of-the-art UTBB FDSOI MOSFET modeling status is compiled. The main physical effects involved in the double gate transistor with a 7 nm thick film are reviewed, particularly the back gate impact, using measurements and TCAD. For better insight into the Weak Inversion and Moderate Inversion operations, both the low frequency $g_m/I_D$ FoM and the proposed high frequency $y_m/I_D$ FoM are studied and also used in an efficient first-cut analog design. Finally, a high frequency NQS model is developed and compared to DC and S-parameters measurements. The results show excellent agreement across all modes of operation including very low bias conditions and up to 110 GHz.

Key words: Analog and RF, Double-gate FETs, Fully Depleted Silicon-on-Insulator (FDSOI), UTBB, Inversion Coefficient, Transconductance efficiency, $g_m$ over $I_D$, Transadmittance efficiency, Low-Power, Low-Voltage, HF, mm-Wave, NQS, LNA, LNA-MIXER.

# Résumé

Ce travail de recherche a été principalement motivé par les avantages importants apportés par la technologie UTBB FDSOI aux applications analogiques et RF de faible puissance. L'objectif principal est d'étudier le comportement dynamique du transistor MOSFET du type UTBB FDSOI et de proposer des modèles prédictifs et des recommandations pour la conception de circuits intégrés RF, en mettant un accent particulier sur le régime d'inversion modérée. Après une brève analyse des progrès réalisés au niveau des architectures du transistor MOSFET, un état de l'art de la modélisation du transistor MOSFET UTBB FDSOI est établi. Les principaux effets physiques impliqués dans le transistor à double grille avec une épaisseur du film de 7 nm sont passés en revue, en particulier l'impact de la grille arrière, à l'aide de mesures et de simulations TCAD. La caractéristique $g_m/I_D$ en basse fréquence et la caractéristique $y_m/I_D$ proposée pour la haute fréquence sont étudiées et utilisées dans une conception analogique efficace. Enfin, le modèle NQS haute fréquence proposé reproduit les mesures dans toutes les conditions de polarisation y compris l'inversion modérée jusqu'à 110 GHz.

Mots-clés : Analogique et RF, Double Grille, FDSOI, UTBB, Coefficient d'inversion, Efficacité de la transconductance, $g_m$ sur $I_D$, Efficacité de la transadmittance, faible puissance, faible tension, HF, spectre millimétrique, NQS, LNA, LNA-MIXER.

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# Acronyms and Abbreviations

| | |
|---|---|
| A/D | Analog to digital |
| BSIM | Berkeley Short-channel IGFET Model |
| GBW | Gain-Bandwidth |
| CLM | Channel Length Modulation |
| CMOS | Complementary Metal-Oxide-Semiconductor |
| CS | Common-Source |
| DIBL | Drain Induced Barrier Lowering |
| DUT | Device under Test |
| FDSOI | Fully Depleted Silicon on Insulator |
| FET | Field Effect Transistor |
| FinFET | Fin Field Effect Transistor |
| FoM | Figure-of-Merit |
| GIDL | Gate Induced Drain Leakage |
| GISL | Gate Induced Source Leakage |
| IC | Integrated Circuit |
| MI | Moderate Inversion |
| MOS | Metal-Oxide-Semiconductor |
| MOSFET | Metal-Oxide-Semiconductor Field-Effect-Transistor |
| mm-Wave | Millimeter-Wave |
| LNA | Low noise amplifier |
| NMOS | N-type Metal-Oxide-Semiconductor |
| NQS | Non-Quasi-Static |
| OP | Operation Point |
| PMOS | P-type Metal-Oxide-Semiconductor |
| PSD | Power Spectral Density |
| QS | Quasi-Static |
| RF | Radio Frequencies |
| SCE | Sort-Channel Effects |

| | |
|---|---|
| SEM | Scanning Electron Microscope |
| SH | Self-Heating |
| SI | Strong Inversion |
| SOI | Silicon on Insulator |
| T | Temperature |
| TCAD | Technology Computer Aided Design |
| TEM | Transmission electron microscopy |
| UTBB | Ultra-Thin-Body and Box |
| UTSOI | Ultra-Thin SOI |
| VSAT | Velocity Saturation |
| WI | Weak Inversion |

# List of Symbols

**Physical constants**

| | |
|---|---|
| $k$ | Boltzmann's Constant in [$J.K^{-1}$] |
| T | Absolute Temperature in [K] |
| $\mu_0$ | Low-field mobility in [$m^2.V^{-1}.s^{-1}$] |

**Geometry**

| | |
|---|---|
| L | Channel length in [m] |
| W | Total channel width in [m] |
| $W_f$ | Single gate finger width in [m] |
| $N_f$ | Number of gate fingers |
| M | Number of devices in parallel |
| $T_{ox}$ | Front gate oxide thickness in [m] |
| $T_{si}$ | Silicon film thickness in [m] |
| $T_{BOX}$ | Back gate oxide thickness (BOX thickness) (= $T_{ox2}$) in [m] |

**Voltages**

| | |
|---|---|
| $U_T$ | Thermodynamic Voltage in (= $k$T/q) in [V] |
| $V_D$ | DC drain to source voltage (= $V_{DS}$) in [V] |
| $V_G$ | DC gate to source voltage (= $V_{GS}$) in [V] |
| $V_{bG}$ | DC back gate to source voltage in [V] |
| $V_{TH}$ | Threshold voltage in [V] |
| $V_{DSAT}$ | Drain to source saturation voltage in [V] |
| $V_{ov}$ | Gate to source voltage overdrive (= $V_G$ - $V_{TH}$) in [V] |

**Currents**

| | |
|---|---|
| $I_D$ | Static drain current flowing into the drain terminal in [A] |
| $I_d$ | Normalized drain current (= $I_D$/(W/L)) in [A] |
| IC | Inversion Coefficient which is also a drain current normalization |

| | |
|---|---|
| $I_1$ | Technology characteristic current for the front gate (= $I_{spec}$) in [A] |
| $I_2$ | Technology characteristic current for the back gate in [A] |
| $I_{\square}$ | Square shape drain current in [A] |
| $I_{ON}$ | MOSFET ON current (digital applications FoM) in [A] |
| $I_{OFF}$ | MOSFET OFF current (digital applications FoM) in [A] |

**Conductances and Transconductances**

| | |
|---|---|
| $g_{m1}$ or $g_m$ | Front gate transconductance in [S] |
| $g_{m2}$ or $g_{mb}$ | Back gate transconductance in [S] |
| $g_{ds}$ | Output conductance (= $g_d$) in [S] |

**Charges**

| | |
|---|---|
| $Q_{inv}$ | Inversion mobile charge density (= $Q_i$) in [$C.m^{-2}$] |
| $Q_I$ | Inversion charge in [C] |
| $Q_G$ | front gate charge (= $Q_{g1}$) in [C] |
| $Q_D$ | Drain charge in [C] |
| $Q_S$ | Source charge in [C] |
| $Q_{bG}$ | Back gate charge for UTBB FDSOI MOSFET (= $Q_{g2}$) in [C] |
| $Q_B$ | Bulk charge for bulk MOSFETs in [C] |

**Gains in [dB]**

| | |
|---|---|
| $H_{DG}$ | Current gain |
| U | Unilateral gain or Mason's gain |
| $A_v$ | Voltage gain |

**Admittances and Transadmittances**

| | |
|---|---|
| $y_m$ | Intrinsic mutual front gate transadmittance in [S] |
| $y_{xy}$ | Admittance (x = y) or transadmittance (x ≠ y) in [S] where x and y are taking the following values: 1 for drain, 2 for gate, 3 for source and 4 for back gate |

**Capacitances and Transcapacitances**

| | |
|---|---|
| $C_{ox}$ | Oxide capacitance per unit area in [$F.m^{-2}$] |

| | |
|---|---|
| $C_{gs}$ | Total gate to source capacitance in [F] |
| $C_{gsi}$ | Intrinsic gate to source capacitance in [F] |
| $C_{gse}$ | Extrinsic gate to source capacitance in [F] |
| $C_{gd}$ | Gate to drain capacitance in [F] |
| $C_{gdi}$ | Intrinsic gate to drain capacitance in [F] |
| $C_{gde}$ | Extrinsic gate to drain capacitance in [F] |
| $C_{sb}$ | Source to back gate capacitance in [F] |
| $C_{gb}$ | Total gate to back gate capacitance in [F] |
| $C_{gbi}$ | Intrinsic gate to back gate capacitance in [F] |
| $C_{gbe}$ | Extrinsic gate to back gate capacitance in [F] |
| $C_{db}$ | Drain to back gate capacitance in [F] |
| $C_{ds}$ | Drain to source capacitances in [F] |
| $C_{dg}$ | Drain to gate capacitance in [F] |
| $C_{sg}$ | Source to gate capacitance in [F] |
| $C_{sd}$ | Source to drain capacitance in [F] |
| $C_{bd}$ | Back gate to drain capacitance in [F] |
| $C_{bg}$ | Back gate to gate capacitance in [F] |
| $C_{bs}$ | Back gate to source capacitance in [F] |
| $C_{gg}$ | Gate capacitance, including overlap capacitances in [F] |
| $C_{dd}$ | Drain capacitance in [F] |
| $C_{ss}$ | Source capacitance in [F] |
| $C_{bb}$ | Total back gate capacitance in [F] |
| $C_{m}$ | Intrinsic mutual capacitance related to front gate in [F] |

**Resistances**

| | |
|---|---|
| $R_G$ | Gate resistance in [Ω] |
| $R_S$ | Source series resistance in [Ω] |
| $R_D$ | Drain series resistance in [Ω] |
| $R_{bG}$ | Back gate resistance in [Ω] |
| $R_{contact}$ | Contact resistance in [Ω] |

**Times and Frequencies**

| | |
|---|---|
| $f_T$ | Transit frequency in [Hz] |

| | |
|---|---|
| $\tau_T$ | Transit time in [s] |
| $f_{max}$ | Maximum oscillation frequency in [Hz] |

**Other**

| | |
|---|---|
| $n_1$ | Front gate slope factor |
| $n_2$ | Back gate slope factor |

# Introduction

Wireless portable devices improve life by providing quick tracking and diagnostics, and have become ubiquitous over the last few years. The main reasons of this spectacular spread are the low price and high performance. Still, the power-consumption remains one of the major barriers somehow preventing the complete achievement of the wider Network of Things. With the emergence of the Internet of Things (IoT), there has been rising interest in fast, low-cost and low-power Systems-On-Chip (SoCs) to satisfy the thirst for sensing and communicating in a continuous and unnoticeable way. The popularity of these devices and things is due mainly to advances in the semiconductor industry which have promoted low-cost, low-power and high speed Integrated Circuits (ICs) through aggressive scaling [1].

## Background and Motivation

Silicon technology has been driven for years by downscaling dictated by the high-performance integrated digital circuits. Today, further reduction of transistor dimensions is critical due to intrinsic limitations such as short channel effects. To overcome these challenges, semiconductor industry strategies include the use of new materials and revolutionary device architectures such as Multiple-Gate (MG). Moreover, shrinking the thickness of the silicon body is proposed in the case of planar ultra-thin Body and Box (UTBB) fully depleted (FD) Silicon-on-Insulator (SOI) double-gate (DG) MOSFET, and vertical FinFET [2][3][4][5].

The UTBB FDSOI MOSFET is considered as a planar low-cost and a straightforward solution to continue shrinking the CMOS transistor for low power and high-speed Very-Large-Scale Integration (VLSI) circuits [6]. The advantages of the UTBB FDSOI MOSFETs include: steep subthreshold slope (close to the room temperature Boltzmann limit of 60 mV/dec for long channels) thanks to the better control of the channel potential [7], low channel doping and excellent control of short-channel effects (SCE). Both FinFET and UTBB FDSOI MOSFETs allow excellent

channel control for high digital performances [8][9][10]. However, analog and RF performances are affected unevenly.

Because of a crowded up-to-5 GHz spectrum with many interferers, some applications such as automotive radar started to tackle the mm-Wave spectrum looking for more bandwidth [11]. Other applications are under active investigation and design in mm-Wave spectrum such as low-power portable radars demonstrated in [12] and high data rate Wireless USB-like communication prospected in [13]. The aforementioned nanoscale CMOS device architectures display very high transit frequencies practically beyond the Millimeter-Wave (mm-Wave) spectrum and can be clearly used for these mm-Wave applications [14][15]. To be ready to take full advantage of the advanced nanoscale CMOS devices, the computer-aided design (CAD) tools have to be updated with accurate descriptions of their behavior in all operation conditions. Therefore, FinFET and UTBB FDSOI MOSFET models for high frequency (HF) and low-voltage (LV) applications are required. The simulation of advanced high precision mixed-mode analog circuits including A/D converters, switched-capacitor circuits, and RF amplifiers requires accurate device models in a large frequency spectrum including mm-Wave. Actually, at high frequency operation, the input signal may have rise or fall times comparable or smaller than the transit time of the transistor. Though all standard compact models, including the advanced Leti-UTSOI2 model, are mainly low frequency quasi-static models with no or simplified high frequency effects.

As mentioned above, low power consumption is one of the main challenges for IoT widespread especially at high frequency operation for RF or mm-Wave communication. High performance rechargeable batteries have already granted a certain degree of autonomy. Moreover, CMOS technology evolution has allowed substantial reduction of power consumption needs in the digital part of the Integrated Circuits (ICs) [16][17]. To further reduce power consumption in the light battery powered devices, high frequency front-end subsystems design has to take into consideration power consumption. Particularly, with the increasing off leakage current that determines the systems stand-by power consumption, power management techniques have to be used and bias conditions have to be lowered. Furthermore, with the very high transit frequencies achieved today in submicron CMOS technologies, the

operating point can be moved towards Weak Inversion (WI) and Moderate Inversion (MI) regimes in order to achieve low drive currents, higher gains and still acceptable operation frequencies [18]. Moderate Inversion operation is increasingly important for low-voltage and low-power CMOS applications since it allows for high transconductance efficiency and low $V_{DSAT}$ while maintaining high bandwidth. However, operating MOSFET in MI greatly complicates analog CMOS design as no physically based simple model is available for hand calculation.

This research work has been motivated primarily by the significant advantages brought about by the UTBB FDSOI technology to the Low power Analog and RF applications on the one hand and the interesting physical phenomena occurring in the thin silicon film under the impact of the two independent gates on the other hand. The main goal is to study the dynamic behavior of the UTBB FDSOI MOSFET in light of the recent technology advances and propose predictive models and useful recommendations for RF IC design with particular emphasis on Moderate Inversion regime.

## Thesis Outline

After a brief review of progress in MOSFET architectures introduced in the semiconductor industry, in **Chapter 1** we go through the list of the advantages of the state-of-the-art UTBB FDSOI technology. We also present two modeling approaches as a basis of our research work. We then describe the existing compact models for quasi-static UTBB FDSOI MOSFET.

**Chapter 2** describes the static and low frequency behavior of the UTBB FDSOI MOSFET. The main involved physical effects are reviewed, particularly the back gate impact, using measured data and technology computer-aided design (TCAD) simulations. A threshold based long channel model is compared to the classical bulk model, and a small signal low frequency equivalent circuit is proposed. Two modeling approaches are investigated: the simple enhanced equivalent circuit and an industrial recently proposed compact model namely Leti-UTSOI2 model. The important low frequency Figures-of-Merit are assessed using both models. An enhancement of the classical MOSFET Operating Point Information feature is finally proposed. The

classical feature is intensively used in Analog and RF design CAD despite the severe discussed limitations.

For better insight into the Weak Inversion and Moderate Inversion MOSFET operation, the $g_m$ over $I_D$ figure of merit namely the transconductance efficiency is studied in **Chapter 3.** Transconductance efficiency is an essential design synthesis tool for low-power analog and RF applications. The invariance of $g_m/I_D$ versus normalized drain current curve is analyzed in UTBB FDSOI asymmetric double gate (DG) MOSFET. The Chapter studies the breakdown of this invariance versus back gate voltage, transistor length, temperature, drain to source voltage and process variations. The unforeseeable invariance is emphasized by measurements of a commercial 28 nm UTBB FDSOI CMOS technology, thus supporting the $g_m/I_D$ based design methodologies usage in double gate UTBB FDSOI transistors sizing.

**Chapter 4** discusses RF and mm-Wave characterization and modeling of the UTBB FDSOI MOSFET high frequency behavior up to 110 GHz. Various model enhancements are proposed to capture high frequency effects including Non-Quasi-Static (NQS) effect and gate distributed effect. The high frequency UTBB FDSOI model is extended using front and back gates networks. Simulated high frequency figures of merit are assessed and compared to measured data.

**Chapter 5** provides a study of the NQS behavior of the UTBB FDSOI MOSFET with a special focus on moderate inversion. Frequency dependence of small signal characteristics derived from experimental S-parameters are analyzed and reveal that the transconductance efficiency ($g_m/I_D$) concept, studied in Chapter 3 and already adopted as a low frequency Analog figure-of-merit (FoM), can be generalized to high frequency. We report that the normalized frequency dependence of the generalized FoM transadmittance efficiency ($y_m/I_D$) only depends on the mobility and inversion coefficient (IC). In addition, we used this novel approach to extract essential parameters such as the mobility, the critical NQS frequency $f_{NQS}$ and the transit frequency $f_T$.

**Chapter 6** discusses a sizing methodology where the previously developed charts and models are used in a simple 35 GHz LNA circuit design. The goal is to

provide with an application example where operation in MI is profitable as long as both high frequency performance and power consumption matters.

Finally, an overall summary of this dissertation is presented along with future research suggestions in the **Conclusion**.

# Chapter 1
# State of the Art

## 1.1 Introduction

In the last five decades, semi-conductor industry is mainly governed by Moore's law with a main focus on scaling IC components geometry gradually down to the nanoscale. Moore’s law is mainly about cost reduction, and the economic aspect resulted in electronics widespread. Recently, new materials and architectures are used to overcome short channel effects limitations and DIBL caused by the close proximity between the source and the drain. Therefore, new solutions become inevitable particularly below the 20 nm technology node.

In order to overcome MOSFET off-state leakage current, the gate control over the channel potential distribution has to be enhanced. High-k materials were introduced since 45 nm technology node to help increasing the gate capacitance with less tunneling leakage and consequently enhance Gate control [19]. All enhancement techniques that were used in previous nodes hit their limit when approaching the 20 nm technology node. The mobility degradation due to scattering limited the doping concentration in the channel and the lattice maximum stress limited the mobility enhancement in strained channels [20][21]. With above limitations, novel device architectures with multiple gates were foreseen to continue device scaling. The first published work on the double-gate MOSFET, [2], shows significant SCE reduction in FDSOI MOSFETs while adding a bottom or back gate. With this architecture, the influence of the drain electric field on the channel is reduced. However, the first manufactured double-gate MOSFET was the fully depleted lean-channel transistor (DELTA) which is similar to FinFET but without the top hard mask [4]. Two leading technology contenders have been adopted and are in production today: the symmetric DG FinFET and the asymmetric DG UTBB FDSOI. The two basic differences between

the two technological solutions are the gates and the channel orientation, and the two gates connection. FinFET is basically a double-gate in which the two gates are connected together. However, in a UTBB FDSOI MOSFET, the two gates are not connected and can be bias differently. Otherwise FinFET and UTBB FDSOI look the same as depicted in Fig. 1.1 and provide comparable digital performances [22]. The RF behavior of FinFET is however affected by a large level of parasitic elements [23][24][25][14]. Fig. 1.2 shows a benchmarking of the transit frequency $f_T$ of various state-of-the-art MOSFETs versus gate length. UTBB FDSOI shows higher $f_T$ versus FinFET thanks to the reduced parasitic resistance and capacitance elements. Moreover, the ITRS (International Technology Roadmap for Semiconductors) expectations are met by UTBB FDSOI and confirmed by our measurements of a nominal L = 30 nm length NMOS and PMOS devices as depicted in Fig. 1.3.

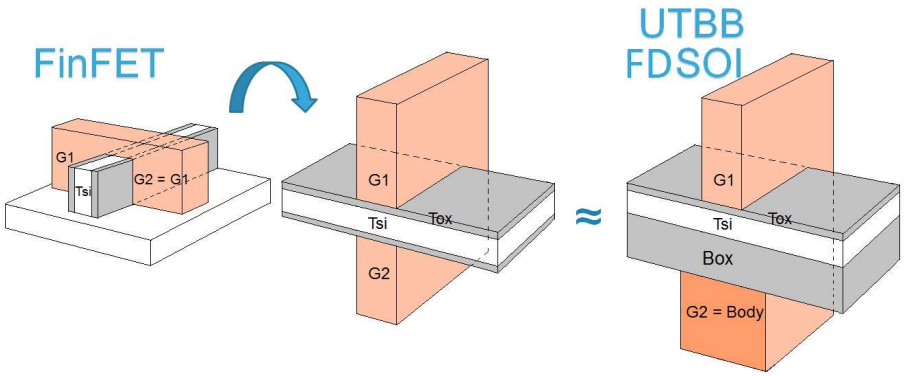



Fig. 1.1 FinFET (left) and UTBB FDSOI (right) similarity.

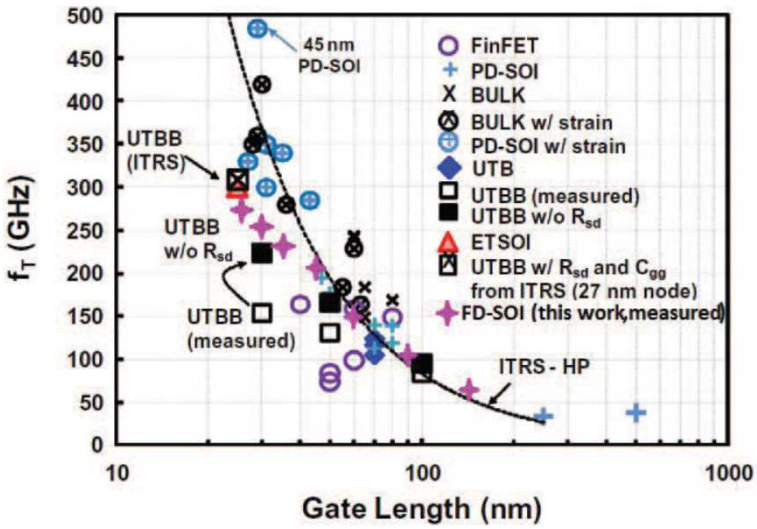



Fig. 1.2 Benchmarking transit frequency $f_T$ for various state-of-the-art MOSFETs versus gate length [14].

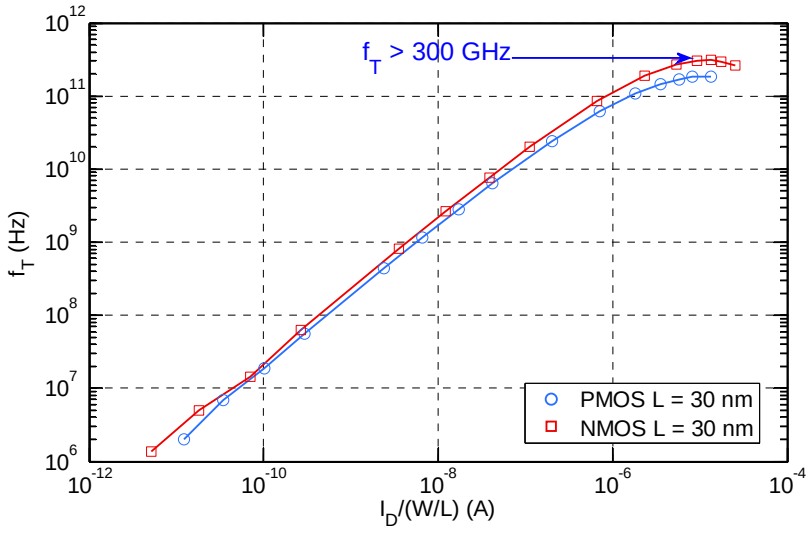



Fig. 1.3 Measured $f_T$ versus normalized drain current $I_D$/(W/L) for UTBB FDSOI NMOS and PMOS (L = 30 nm, Nf = 20, $W_f$ = 1µm, $V_{DS}$ = 1 V).

An important propriety of DG MOSFETs (i.e. FinFET, UTBB FDSOI, etc.) namely volume inversion (VI) has been discovered in 1987 [26]. Volume inversion occurs in very thin silicon films controlled by two gates which is the case for a UTBB FDSOI MOSFET where inversion carriers are not confined in the Si/SiO2 interface, as predicted by classical semiconductor physics, but rather in all volume of the silicon film. This phenomena will be illustrated using our TCAD simulations in Chapter 2 and evidenced using our measured data in Chapters 2, 3, and 5. The quantum confinement in the thin Si film is at the origin of the VI effect [27]. Although volume inversion phenomena is demonstrated, its modeling is frequently overlooked and charge-sheet approximation is forced [28][29]. Accurate results are obtained with modeling the quantum confinement effect using offsets applied on gates voltages or vertical dimensions in [30] and [31], and using the concept of inversion layer centroid in [32]. Moreover, multiple inversion charges (front and back) and vertically variant carrier mobility are considered to retrieve the total charge and the effective mobility [30][33]. Actually the calculation of the electron concentration in the presence of confinement needs to solve Poisson's and Schrödinger's equation self-consistently but this is frequently ignored. Fig. 1.4 shows our simulated electron density in the 7 nm silicon film of a UTBB FDSOI MOSFET for different back gate voltages $V_{bG}$ and fixed front gate voltage $V_{GS}$ = 1 V using Synopsys Sentaurus TCAD [34]. The various $V_{bG}$ values generate a variant vertical electrical field in the film that controls the volume inversion

intensity, and consequently the vertical charge carrier concentration. For $V_{bG}$ = 2 V, the electron density is almost constant far from the two Si/Oxide interfaces.

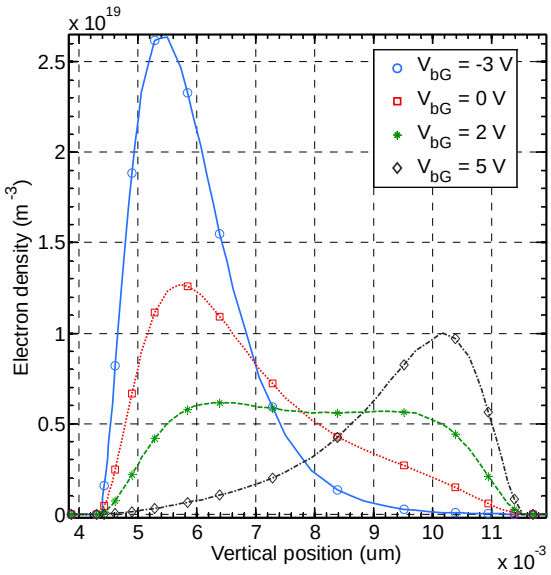



Fig. 1.4 Simulated electron density in the silicon film at different back gate voltages $V_{bG}$ for a UTBB FDSOI NMOS (L = 1 µm & W = 1 µm) in saturation $V_{DS}$ = 1 V and strong inversion (at constant $V_{GS}$ = 1 V).

## 1.2 UTBB FDSOI technology

FDSOI technology started to draw attention in the middle of the 80s because of its multiple advantages over the partially-depleted SOI [7]. Several SOI wafers fabrication processes were developed and used for SOI CMOS such as the Separation by IMplanted OXygen (SIMOX) and ELTRAN [35][36]. In our research work, the UTBB FDSOI wafers are fabricated using a UNIBOND substrate made with Smart Cut technology reported by LETI in 1995 [37]. The UNIBOND process involves several steps as shown in Fig. 1.5. After oxidation, hydrogen is implanted into a Si donor wafer. The donor wafer is bonded to another wafer to form the future BOX. Smart Cut step is the operation of splitting off the donor wafer at a temperature of 500 to 600 °C. Planarization of the surface ends this process and results in a UTBB FDSOI wafer where the MOSFET will be formed and a recycled donor wafer.

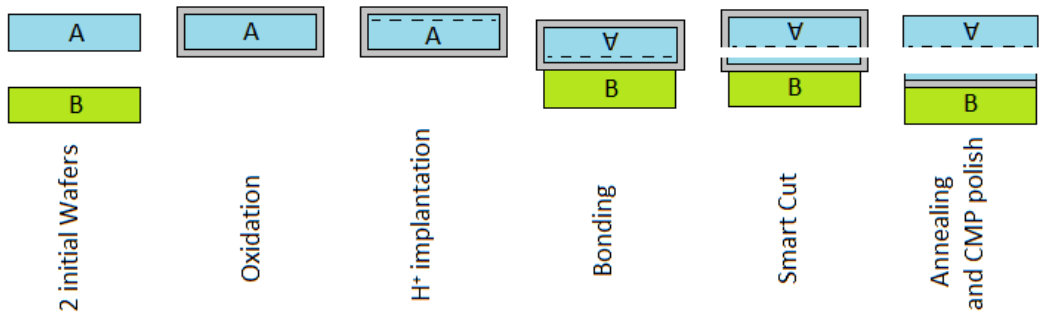



Fig. 1.5 UNIBOND fabrication process with Smart Cut

In the UTBB FDSOI technology, MOSFET channel is formed in a thin silicon film separated from the substrate by an oxide film called Buried OXide (BOX) as depicted in Fig. 1.6. In 28 nm FDSOI technology from STMicroelectronics, final silicon film is 7 nm thick and BOX is 25 nm thick after a few process steps [3]. This architecture provides with multiple advantages for high performance and low power applications. In addition of the well-known SOI technology advantages [38][39], UTBB FDSOI technology features lower parasitic capacitances as depicted in Fig. 1.7, and consequently high-speed operation. The harmful parasitic substrate coupling is avoided in the UTBB FDSOI by the introduction of the Ground Plane (GP) which is a highly doped region underneath the thin BOX [40]. The ground-plane implantation under the BOX is well-type in the structures studied in this research work. This highly doped layer underneath the BOX opens various possibilities to tune the device threshold Voltage ($V_{TH}$) [41] and extends the usage of the MOSFET back biasing to dynamically optimize the power consumption [42].

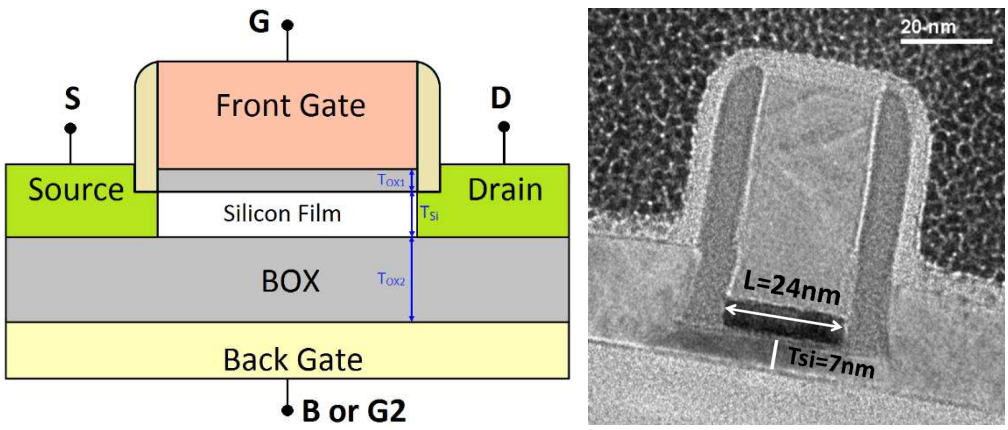



Fig. 1.6 Cross section (left) and TEM (right [3]) of the UTBB FDSOI MOSFET

The channel is rotated by 45° from the <100> plane [43]. FDSOI technology allows co-integration of both bulk and SOI devices on the same die thanks to BOX opening for the bulk parts with a dedicated mask [44]. Carrier mobility is enhanced due to weaker surface electric field and low doping concentration in the Si film. With thin Si film, no punch-through current exists and consequently MOSFETs can be made shorter with no need to dope the Si film, and with the inherited advantage of higher electron mobility.

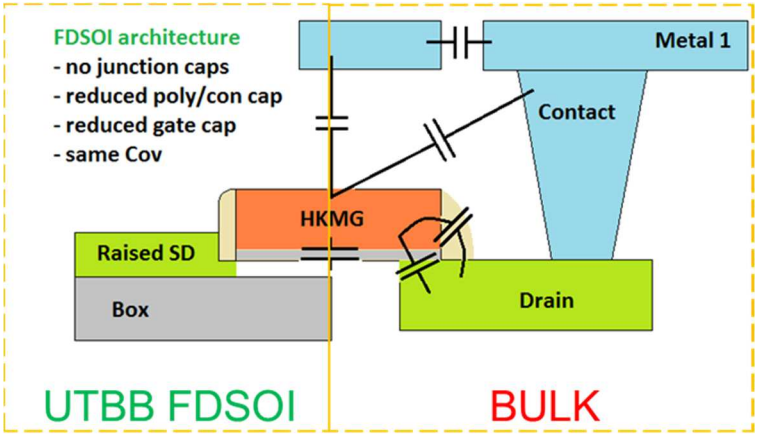



Fig. 1.7 Cross section comparison between bulk MOSFET (right) and UTBB FDSOI (left)

The UTBB FDSOI MOSFET is first introduced at the 28 nm technology node [3], and demonstrated using efficient ARM processor architecture based chips operating at high frequency [45]. Scaling of the UTBB FDSOI technology to the 14 nm technology node is also demonstrated [46]. The key feature of a FDSOI MOSFET in comparison to the partially depleted SOI (PDSOI) is that the depletion region occupies the whole thickness of the silicon film all the way to the Si/BOX interface. Consequently, the floating-body effects of the PDSOI are bypassed in the FDSOI devices.

One major advantage UTBB FDSOI has in comparison to bulk technology is the possibility to control the threshold voltage ($V_{TH}$) using the back gate voltage for both N- and P-type MOSFETs with a modulation factor of ~80 mV / 1V [47]. Fig. 1.8 shows our measured drain current versus the front gate voltage $V_{GS}$ for various back gate voltages $V_{bG}$. The transfer characteristic $I_D$-$V_{GS}$ shifts towards lower $V_{GS}$ while increasing $V_{bG}$, which indicates that the threshold voltage $V_{TH}$ shifts towards lower

values. The increase of $V_{bG}$ is commonly called forward back biasing (FBB), and lowering $V_{bG}$ is called reverse back biasing (RBB).

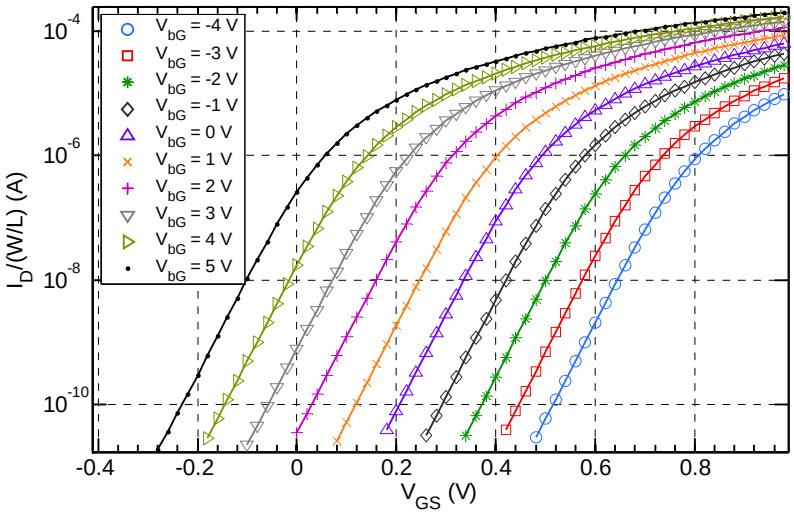



Fig. 1.8 Measured and normalized drain current $I_D$/(W/L) versus front gate voltage $V_{GS}$ for various back gate voltages $V_{bG}$ in semi logarithmic scale for L = 1 µm, W = 10 µm at $V_{DS}$ = 1 V.

Moreover, same bulk technology design flows are applicable to UTBB FDSOI as both technologies are planar [48]. Fig. 1.9 shows the difference between the UTBB FDSOI MOSFET and an advanced bulk MOSFET cross sections. Halos and channel implants are no more required in UTBB FDSOI thanks to the BOX isolation.

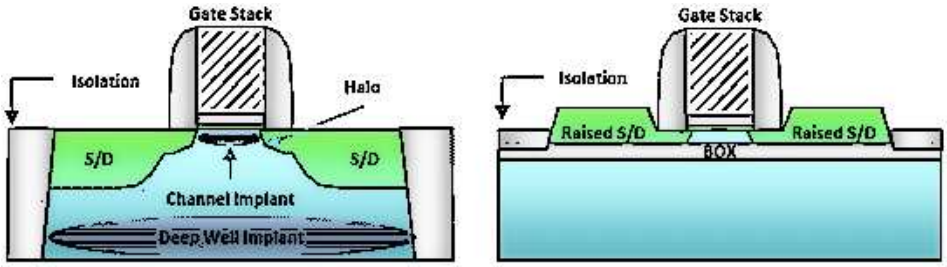



Fig. 1.9 Bulk MOSFET (left) versus UTBB FDSOI MOSFET (right).

Unlike bulk MOSFET, UTBB FDSOI is not subject to the turn on of parasitic p-n-p-n (or n-p-n-p) thyristors causing latch-up in bulk. As UTBB FDSOI has no parasitic thyristors, consequently there is no need for special circuit layout or process to prevent latch-up. Moreover, UTBB FDSOI are ideally isolated from the substrate thanks to the BOX and laterally from each other using shallow-trench-isolation (STI) as shown in Fig. 1.9. The MOSFETs can be put close to each other and gain in density.

In comparison to advanced bulk technologies, FDSOI presents lower DIBL with an enhancement of more than 40 mV/V in short channels as shown in Fig. 1.10.

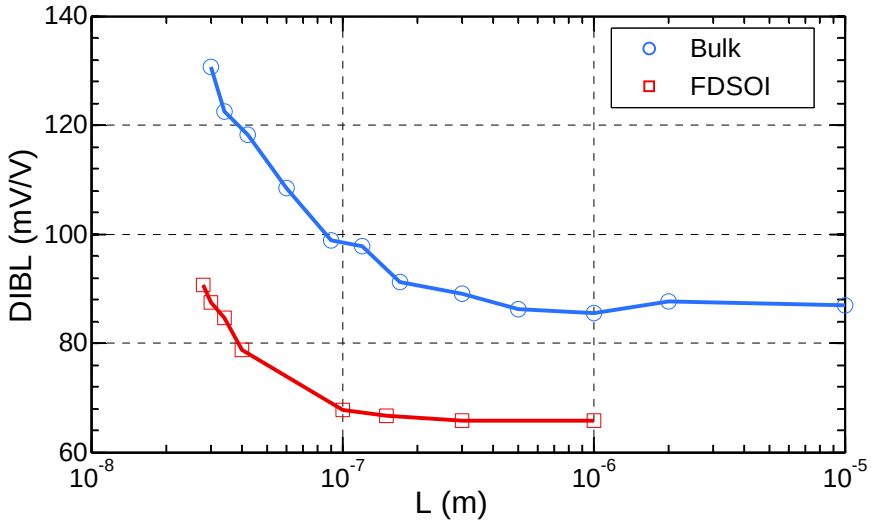



Fig. 1.10 Comparison of DIBL between FDSOI 28 nm and bulk 28nm technologies in saturation ($V_{DS}$ = 1 V) and $V_{bG}$ = 0 V.

One of the key features of SOI CMOS structures is the smaller junction capacitances in comparison to bulk CMOS structures. The junction capacitances in UTBB FDSOI, with thin silicon film, are negligibly small. Moreover, in UTBB FDSOI MOSFET, the capacitance between the drain (source) and the substrate is negligibly small thanks to the thickness of the BOX, and the dielectric constant of the BOX SiO2, which is lower than that of Si.

With less parasitic capacitances as shown in Fig. 1.7, supply voltage can be lowered for reduced power consumption with still high speed operation. Other advantages of UTBB FDSOI are reduced SCE, and tolerance for high temperatures and voltages. With a steep subthreshold slope, lower threshold voltages are obtained in comparison to bulk. Consequently, the gate voltage overdrive $V_{GS}$ - $V_{TH}$ can be made larger to achieve higher speed or lower power dissipation. Furthermore, thanks to the raised source and drain regions, UTBB FDSOI MOSFET exhibits lower series resistances [49][50]. The industry transition from bulk to FDSOI in the last decade as is illustrated in Fig. 1.11 using the MOSFET transconductance efficiency ($g_m/I_D$). The transconductance efficiency is an interesting figure of merit that will be studied in next

Chapters. This FoM can be used to gain insight into the transfer characteristic of a MOSFET in its semi logarithmic form for all levels of inversion as it is expressed as:

$$\frac{g_m}{I_D} = \frac{\partial \ln I_D}{\partial V_{GS}} \tag{1.1}$$

The plateau of the $g_m/I_D$ plots (i.e. maximum $g_m/I_D$), which represents the weak inversion region, is inversely proportional to the subthreshold slope. The 28 nm FDSOI technology provides near ideal subthreshold slope (1.07) versus 65 nm bulk (1.13) and 28 nm bulk (1.17). The downscaling from 65 nm to 28 nm bulk clearly shows the electrostatic control issue, which results in higher leakage. Moreover, the short channel effects, responsible of the departure from the ideal square law current expression are worst for 28 nm bulk as shown in the inset of Fig. 1.11. The velocity saturation and series resistances are responsible for the decrease of $g_m/I_D$ at high current density and departure from the ~$1/\sqrt{I_D}$ trend. The main advantage of 28 nm bulk versus 65 nm bulk is the higher $g_m/I_D$ in strong inversion region thanks to a higher $C_{ox}.\mu_0$, which results into a lower current for same transconductance value (analog applications), and a higher $I_{ON}$ current (digital applications). Besides a better subthreshold slope, the 28 nm FDSOI is less subject to SCE, and the $I_D$-$V_{GS}$ is closer to the classical square law as shown in the inset of Fig. 1.11. The goal of all the research work in semiconductor industry in the last decades is to keep the subthreshold slope as high as possible in Weak Inversion and the square law trend as long as possible in SI. The UTBB FDSOI seems to be near to the ultimate technology. For short channel devices, all the aforementioned short channel effects are more amplified in bulk in comparison to UTBB FDSOI.

Buried oxide isolation is known to give birth to temperature increase because of self-heating effect [51], however, thanks to a thinner BOX in the UTBB FDSOI, thermal effects influence on device parameters are limited in comparison with standard SOI [52]. Similar to SOI devices, UTBB FDSOI MOSFET displays excellent radiation hardness to the detrimental alpha particles, neutrons, and other particles that generate electron-hole pairs after Si penetration [53].

The several advantages of the UTBB FDSOI technology make it possible to implement high performance MOSFETs operating at a low voltage. An understanding of the fundamental behavior of the UTBB FDSOI MOSFETs is essential for circuit design and an accurate model is a must.

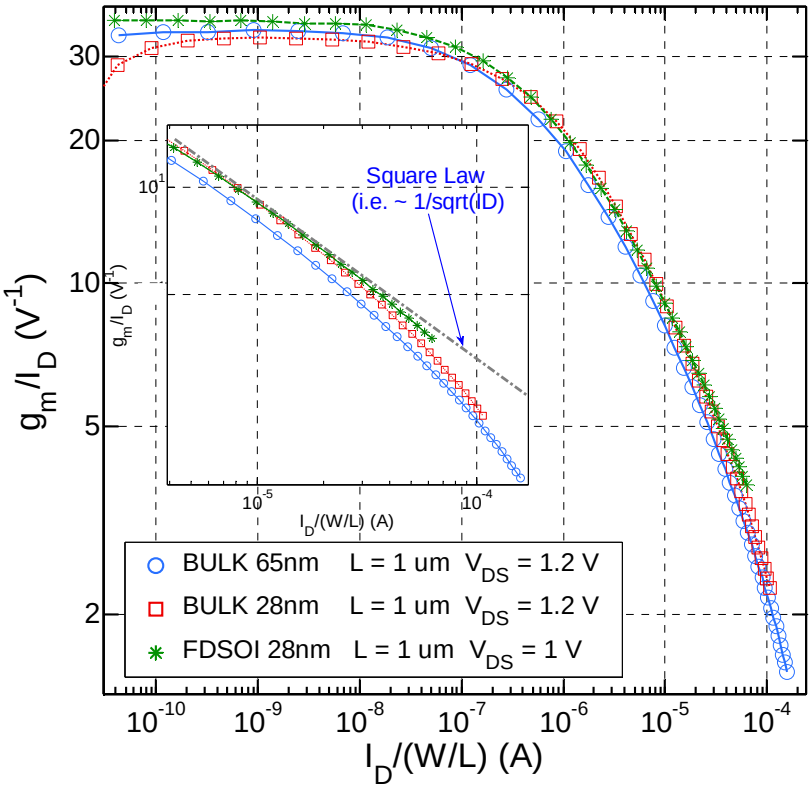



Fig. 1.11 Transconductance efficiency $g_m/I_D$ versus normalized drain current $I_D/(W/L)$ for long channels in saturation for bulk 65 nm, bulk 28 nm, and UTBB FDSOI 28 nm.

## 1.3 Device modeling approaches

Several MOSFET modeling approaches coexist. We will focus on two of them: equivalent circuit based approach and compact modeling approach. Both of the aforementioned approaches are somehow physically based. Modeling of MOSFETs started mainly using the simple equivalent circuit approach because of the lack of physical knowledge of the MOSFET device and the limited computing power. One of the frequently used MOSFET equivalent circuit is the Meyer (1971) model based on reciprocal capacitances ($C_{gs}$, $C_{gd}$, and $C_{gb}$). Besides the problem with the charge conservation, this model is still acceptable for hand calculation with small errors at low

frequency operation. An augmented version of the Meyer model is shown in Fig. 1.12 where additional elements are added such as source to drain capacitance. Actually, this equivalent circuit is used for small-signal simulations where linear relations between current and voltage are assumed, and is called the small-signal equivalent circuit.

With better understanding of the MOSFET physics along with higher computing power availability, compact modeling became a more efficient alternative and an important research area. Years later, the equivalent circuit approach is still inevitable for two main reasons. On the one hand simple lumped element circuits are helpful for analog hand calculation based design and for a better insight into MOSFET physics. On the other hand, equivalent circuits are used to complement and augment low frequency compact models by describing external parasitic elements or complex distributed effects. Though, because of the several nodes in an equivalent circuit and the large SPICE simulator computation time involved, scalable compact models are the industry models of choice for the device core.

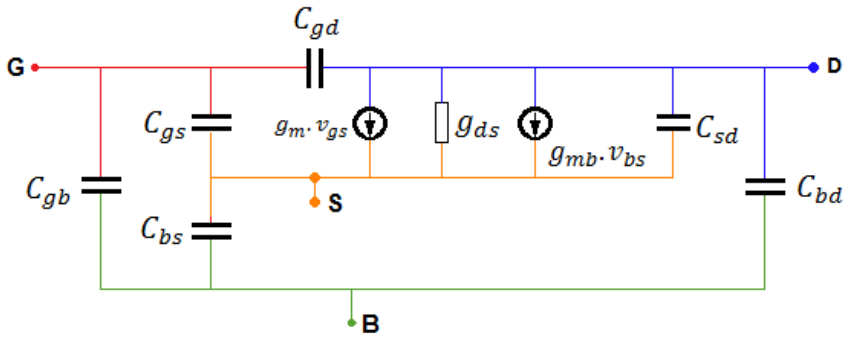



Fig. 1.12 Modified Meyer equivalent circuit.

Compact models of semiconductor devices are mathematical descriptions of their complex behavior, and usually implemented in a computer language such as Verilog-A. Compact models simulations are fast despite the complex and lengthy codes, and are systematically used for IC simulation earlier to an expensive production process. Moreover, compact models are flexible enough to describe MOSFETs fabricated in different foundries. Standard compact models go through extensive qualification within semiconductor foundries and fabless industrials that are organized into an industry consortium, namely Compact Model Coalition (CMC). It should be

noted that the valuable contributions from universities are key for innovative compact modeling solutions.

A practical modeling approach in semiconductor industry is the simultaneous use of the two approaches in RF modeling. Sub-circuits are built using passive elements network on top of intrinsic or core MOSFET models that have been qualified for DC and low frequency operation. The high frequency behavior of MOSFETs is captured using additional lumped elements to end up with complex sub-circuits. Lumped elements are commonly added to each MOSFET terminal. The gate and substrate are modeled using passive RC network while simple series resistances are added to the source and drain. In general, this approach takes advantage of industry standards, such as the threshold voltage ($V_{TH}$) based BSIM4 model from UC Berkeley and the surface potential based PSP model originated from Philips and Pennsylvania State University (currently supported by LETI and NXP), as far as bulk MOSFETs are concerned. The aforementioned approach will be adopted in addition to an equivalent circuit in our work for its efficiency in an industrial usage. The equivalent circuit will be proposed as an alternative for the core compact model in order to gain practical insight into the contributors to the small signal behavior.

For UTBB FDSOI MOSFET, several core models have been proposed but four main industry level compact models exist.

## 1.4 UTBB FDSOI compact models

Early compact models assume a depleted back interface with huge limitations when back gate voltage is high (forward back gate bias or FBB). In an asymmetric double gate MOSFET, the resolution of Poisson equation with boundary conditions is not an easy task. Depending on the number of the introduced boundary conditions, numerical resolution of one [54] or two [55] coupled equations is used after a calculation to separate between hyperbolic (i.e. zero potential) and trigonometric (i.e. zero field) possible modes. Fig. 1.13 shows the regions of the front and back gates voltages plane where the equations to be solved are trigonometric or hyperbolic [56]. This calculation relies on Lambert functions usage [57]. The problem has been also

written in a more suitable formulation of three coupled complex equations [58], but this does not lead to an analytical solution for the surface potentials in the film and box interfaces. A summary of the surface potential calculation models for an asymmetric DG MOSFET is given in Table 1-1.

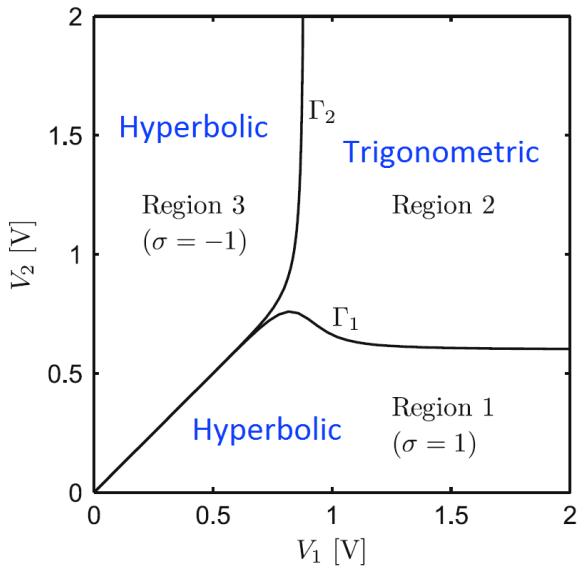



Fig. 1.13 Regions of operation on the front and back gates voltages plane for an imref splitting Vc = 0.5V, $T_{si}$ = 20 nm, $T_{ox1}$ = 2 nm, and $T_{ox2}$ = 40 nm. $V_1$ and $V_2$ are the front and back gate voltages respectively [57].

Table 1-1 Summary of surface potential calculation models in a DG MOSFET [59].

| Reference | Interpolation functions | Approx. on potential vertical profile | Numerical resolution | Comput. Of boundaries between modes | Use of Lambert functions |
|---|---|---|---|---|---|
| H. Lu et al. IEEE TED 2006 [60] | No | No | Yes | Yes | No |
| A.S. Roy et al. SSE 2006 [61] | Yes | No | No | No | No |
| Z. Zhu et al. JJAP 2007 [62] | Yes | No | No | No | Yes |
| F. Liu et al. IEEE TED 2008 [63] | No | No | Yes | Yes | No |
| H. Abebe et al. Jour. Semi. Tech. Sc. 2009 [64] | No | Yes | No | No | No |

| | | | | | |
|---|---|---|---|---|---|
| A. Sahoo et al. IEEE TED 2010 [54] | No | No | Yes | Yes | Yes |
| S. Jandhyala et al. IEEE TED 2011 [65] | No | No | Yes | Yes | No |
| F. Lime et al. SSE 2011 [66] | Yes | No | No | No | No |
| A. Abraham et al. IEEE TED 2012 [67] | No | No | Yes | Yes | No |
| T. Poiroux et al. IEEE IEDM 2013 [59] | Yes | Yes | Yes | Yes | Yes |

Four compact models are available for UTBB FDSOI MOSFET simulation: BSIM-IMG [31], HISIMSOTB [29], UFDG [68], and Leti-UTSOI2 [59]. Three models are standards or candidates for standardization in the semiconductor industry: BSIM-IMG, HISIMSOTB, and Leti-UTSOI2. All models are claimed to be physics based, scalable and efficient for circuit simulations. All these compact models are incorporating several physical effects, such as short channel effects (SCE), mobility degradation, velocity saturation, velocity overshoot, series resistance, channel length modulation (CLM), quantum mechanical effects, gate tunneling current, gate-induced-drain-leakage (DIBL), and parasitic capacitances.

### 1.4.1 BSIM IMG

The Berkeley BSIM IMG (independent multi-gate) model is a CMC (e.g. Compact Model Coalition) standard model for asymmetric double gate MOSFETs. It is a surface potential based model supporting asymmetric oxide thicknesses, dielectric constants and work-functions [31]. Early versions of BSIM-IMG didn’t support channel inversion at the back interface of the silicon film. Today, official versions of BSIM-IMG still have limited support of the back gate voltage impact. Surface potentials and charge densities at the source and drain ends are calculated by solving the Poisson's equation in a fully-depleted, lightly doped film and using analytical approximations. Consequently, model is claimed to capture volume inversion effects at least for low back gate voltages [69]. The back gate effect on long channel front gate threshold voltage is inherently captured while two inversion charge models are proposed using CHARGEMOD switch parameter. The model is continuous and symmetrical at $V_{DS}$ = 0 V. The standard BSIM-IMG was not considered here to model UTBB FDSOI

in 28 nm technology node because of the early versions limitations such as a limited support of the back gate control.

### 1.4.2 HISIMSOTB

The Hiroshima University STARC IGFET model-silicon on thin buried oxide (HiSIM-SOTB) has been developed for ultrathin SOI and buried oxide (BOX) layers by Hiroshima University's HiSIM research center in collaboration with its partners. This model is selected as an international industry standard by the CMC and is open to the public. The surface potentials at three positions are calculated by solving the Poisson equation [29]. The three positions are the upper and lower sides of the silicon film, and the lower side of the BOX. The potential distribution is numerically solved using Newton iteration method. Under the gradual-channel approximation, the potential distribution in the channel is described by the potential at the source side and the drain side. Consequently, the charges at the source and drain sides are obtained. Surprisingly, the charge-sheet approximation is claimed to be valid even with thin silicon films where carriers are distributed within all the volume of the silicon film. The total charges are calculated by the integration of the charge distribution along the channel. Current is then deduced from the integrated inversion charge using a bulk-like mobility model with three scattering effects: Coulomb, Phonon, and Surface Roughness. Capacitances are then determined by a charge derivation.

### 1.4.3 UFDG

UFDG model from university of Florida is claimed to be physically based and generic model for symmetric (e.g. FinFET) or asymmetric (e.g. UTBB FDSOI) DG MOSFETs [68]. The model can also be used for single gate MOSFETs with thick BOX [70]. 2D Poisson's equation in the channel region is solved while assuming a second-order polynomial function for the electric potential and using four bias dependent boundary conditions [71]. The carrier-energy quantization is then taken into account using a potential offset [72]. The diffusion current in WI is then calculated by integrating the electron density in the Si film. In Strong Inversion (SI), where the quantum effect is more important, an iterative and self-consistent solution of the 1D Schrodinger's and

Poisson's equations is developed. Spline polynomial functions are used in MI to continuously link the physically based WI and SI models. Quantum confinement in the thin Si film and volume inversion are taken into account for thin Si films [73]. The transport is modeled as quasi-ballistic using velocity overshoot derived from Boltzmann transport equation and its moments [74]. Main parasitic elements are included. Terminal charges are calculated by an integration of the channel current. Short channel effects are modeled and main parasitic elements such as series resistances, overlap capacitances, and gate resistance are included. Self-heating effect is also proposed in UFDG model.

### 1.4.4 Leti-UTSOI2

Leti-UTSOI2 (or UTSOI2) is a surface potential based compact model describing the ultra-thin fully depleted SOI MOSFET with a lightly doped silicon film [59]. UTSOI2 physical core is suitable for any independent double gate transistor with low-doped channel, and in particular for UTBB-FDSOI architectures.

In UTSOI2, explicit formulations of the front and back surface potentials ($\psi_{s1}$, $\psi_{s2}$) are used to calculate the drain current ($I_D$) and the intrinsic mobile charge ($Q_{inv}$). While iterative resolution of Poisson's equation is used in HISIM STOB, in UTSOI2 an accurate and direct calculation of interface potentials is used. As in [58] and after integration of Poisson's equation along with the boundary condition, three coupled equations are obtained [59]. The key point in UTSOI2 is that to solve the three equations there is no need to know a priori if the solution is in the hyperbolic or trigonometric mode depicted in Fig. 1.13. The three equations are transformed into one equation that is solved analytically using three successive corrections based on 2$^{nd}$ order Taylor development as for PSP bulk model.

Partitioning of inversion charge between source and drain is classically calculated using front interface potential. However, for asymmetric DG MOSFET where more than one interface is available, the classical way is not relevant. In UTSOI2, following the solution proposed in [57], charges are obtained from the drain current calculation. Short and narrow channel effects, series resistance, overlap capacitance,

fringing capacitance and backplane related parasitic capacitances are all accounted for.

The UTSOI2 satisfies continuity requirements for currents and capacitances as well as for their higher order derivatives. It is compliant with all MOSFET standard models criteria such as DC and AC symmetry and robustness in all operation conditions [75].

## 1.5 Conclusion

This Chapter briefly reviews the evolution of the MOSFET architecture from single-gate to double-gate in the last few decades. In order to mitigate the short channel effects that result from advanced MOSFET downscaling, two gates control of the channel appears to be a straight-forward solution. DG UTBB FDSOI architecture exhibits several advantages for digital applications and outperforms bulk and FinFET in Analog and RF applications thanks to the reduced parasitic elements [76][47][14]. In this research work, focus is limited to the UTBB FDSOI MOSFET manufactured in 28 nm and 14 nm technology nodes.

In Section 1.3, two main modeling approaches are discussed. The combination of a core, based on either a compact model or an equivalent circuit, along with lumped extrinsic elements within a sub-circuit is the most accurate approach for an industrial usage [77][78]. This approach is used in this work.

The last Section of this Chapter describes the existing compact models for DG UTBB FDSOI MOSFET. The list is limited to the compact models that are ready for an industrial usage and that include all important physical effects. Leti-UTSOI2 is the first compact model that accurately and completely supports the back gate voltage control within the time frame of this research work, and has been chosen to model the intrinsic behavior of the UTBB FDSOI MOSFET in parallel to the proposed equivalent circuit.

# Part I

# DC and Small Signal Low Frequency Operation

# Chapter 2
# DC and Low Frequency description and modeling

## 2.1 Introduction

High frequency operation of a MOSFET is closely linked to its bias condition, and consequently to its DC operation. The high frequency quasi-static operation can be seen as an assessment of the multiple derivations of the DC operation, in that it scans a part of the I-V characteristic and “senses” its variations. When terminal voltage variations are sufficiently small, the small-signal assumption can be considered, and linear relations between produced current variations and input voltage variations can be used. Consequently, only one derivation of the I-V characteristic is sufficient to predict the behavior of the MOSFET in small-signal assumption. Acceptable prediction of the derivatives of the DC characteristic obviously relies on very accurate DC model. Therefore, an accurate model for DC operation of UTBB FDSOI is a must.

A compact model serves as a bridge between process and circuit design. It is a compact mathematical description of the complex device physics with a trade-off between accuracy and calculation efficiency and induced CPU time. A physically based compact model allows both technology engineers and circuit designers to predict device behavior beyond the measured data used to extract the model. As for the single gate MOSFET models, available compact models for DG MOSFET rely on long-channel core on the top of which various physical effects are added such as short channel effect (SCE), mobility degradation, velocity saturation, and quantum mechanical effect (QME).

Both FinFET and planar Fully Depleted SOI (FDSOI) technologies fulfill the International Technology Roadmap for Semiconductors (ITRS) requirements for

device downscaling. As has been stated in Chapter 1, the two architectures allow excellent channel control for high digital performances thanks to the two gates control and thin silicon film [8][9][10]. However, thanks to fewer parasitic elements, It has been demonstrated that planar FDSOI technology with ultra-thin Body and BOX (UTBB) transistors exhibits excellent analog and RF performances and outperforms bulk and FinFET technologies on various RF aspects [79][80]. Furthermore, UTBB FDSOI MOSFET is claimed to outperform FinFET in terms of cutoff frequencies as shown in Fig. 1.2 [14]. The UTBB FDSOI MOSFET is consequently a good candidate for low power and low voltage applications.

In recent low power and high performance circuits such as those implemented in FDSOI for IoT market, one needs to operate MOSFETs from weak to strong inversion levels [81]. It is worth pointing that moderate inversion region has been found to be a good compromise while power consumption and speed are valued equally [82][25][15]. The MI provides higher transconductance for lower current, and still acceptable bandwidth for low power and low voltage applications. The importance of the moderate inversion region and the related modeling issues are pointed out for bulk earlier in [83].

In order to fully benefit from the advantages of the FDSOI technology, MOSFET compact models should accurately reproduce transistor behavior in all regions of operation especially in low inversion. For hand calculations, although classical WI exponential law and SI square law models can be carefully used, the $g_m/I_D$ charts developed in the next Chapter are more convenient to predict UTBB FDSOI MOSFET capability in all levels of inversion. Moreover, for an industrial usage and as seen in the previous Chapter, UTSOI2 is the first available independent double-gate compact model able to describe accurately the UTBB MOSFET in all bias conditions, including strong forward back bias [84]. UTSOI2 model was validated against numerical simulations and measurements for DC operation showing excellent predictability and scalability properties [30]. However, its RF capabilities have been only highlighted in [85] and clearly ask for more in depth analysis. Noting that digital FoMs such as $I_{ON}$ and $I_{OFF}$ are not sufficient to assess analog behavior of a MOSFET. Moreover, analog

applications such as amplification need accurate prediction of continuous and higher order MOSFET metrics and FoMs in all levels of inversion.

Therefore, two different quasi-static models will be considered for low frequency operation and will be both used as starting blocks for the augmented high frequency non-quasi-static model: (1) an equivalent small signal circuit, and (2) UTSOI2 model.

This Chapter will focus on the description and modeling of the DC and low frequency behavior of the UTBB FDSOI MOSFET. In particular, the special double gate operation will be presented and compared to the bulk single gate operation using measured data. The ability of the proposed models to describe the DC and the small signal low to medium frequency operation will be studied with a focus on low voltage bias conditions.

TCAD simulations will also be performed on two different decks using Sentaurus standard process and device simulator from Synopsys, Inc. : (1) a simple deck without the raised source and drain and using a constant carrier mobility in order to capture first order effects, and (2) a calibrated deck with raised source and drain, and advanced thin layer mobility model with enhanced carrier effective mass [86]. The 28 nm FDSOI technology calibrated TCAD deck will be crucial for back gate impact assessment in both low frequency and high frequency operations.

Synopsys Sentaurus TCAD tool is calibrated at a temperature of 300 K. NMOS and PMOS measurements of four lengths (e.g. L = 30 nm, 40 nm, 100 nm, and 1 µm) and of a 210 nm width are used for calibration. C-V characteristics are used to set the dielectric material properties as well as the work function of the back gate. Mobility model calibration is taken care of using transconductance $g_m$ in linear mode and including doping dependence, Philips unified mobility, remote Coulomb and Phonon scattering, and ballistic transport. The transconductance calibration at high field is taking into account the self-heating effect. Moreover, doping and temperature dependent Shockley-Read-Hall (SRH) recombination model are all accounted for as well.

In order to match $g_m$ in Moderate Inversion, fixed charge traps (Nhk = 5 × 1012 $cm^{-2}$) on the shared interface between high-k HfO2 dielectric and the interfacial oxide layer (SiO2) are considered.

The Chapter is organized as follows. In Section 2.2, the DC and low frequency operation of the UTBB FDSOI MOSFET is described using measurements and TCAD simulations, especially for low inversion levels. In Section 2.3, the simple bulk long channel model is compared to the DG counterpart showing deep similarities, and a small signal equivalent circuit is proposed for simple device assessment. In the same Section, the measured structures are described along with the characterization steps. Having in mind an industrial usage, in Section 2.4, the modeling of the DC and low to medium frequency operation is presented aiming at accurate IC simulations. Simulated analog MOSFET metrics and figures of merit are compared to measurements with emphasis on moderate inversion. Finally, in Section 2.5, the important analog design feature namely DC Operating Point information (DC OP info) is reviewed along with its limitations, and an enhancement is proposed for analog design usage.

## 2.2 UTBB FDSOI MOSFET description and DC operation

Fig. 2.1 shows the cross-section of the UTBB FDSOI MOSFET studied in this work. The silicon film thickness $T_{si}$ is 7 nm on top of a buried oxide (BOX) which isolates the channel from the substrate. The BOX thickness (referred to as $T_{ox2}$ or $T_{BOX}$) is 25 nm, and the equivalent front oxide thickness (referred to as $T_{ox}$ or $T_{ox1}$) is 1.3 nm. A thin BOX is used to reduce coupling between source and drain, and reduce SCE. High k/Metal gate (HkMG) process is used and adjusted to control the threshold voltage for both thin and thick oxide devices. In the gate stack, a single mid-gap metal gate (TiN) is used to adjust simultaneously the threshold voltage of the N and P types MOSFETs while keeping the channel undoped [87]. The source and drain regions are raised using epitaxial step in order to reduce series resistance. A heavily doped Si layer underneath the BOX is introduced in order to suppress the depleted zone under the BOX, further to reduce the coupling between the source and the drain regions, which eliminates

high frequency analog performance degradation, and finally to allow $V_{TH}$ control [40][88][89]. Well-type implantation is used for the ground-plane or back gate region under the BOX and the ground plane [3].

For the 28 nm UTBB FDSOI technology the maximum front gate voltage that is recommended for thin oxide MOSFETs is $V_{DD}$ = 1 V. The minimal recommended length is 30 nm and commonly called nominal length, while minimum possible length is 28 nm and also characterized in this research work.

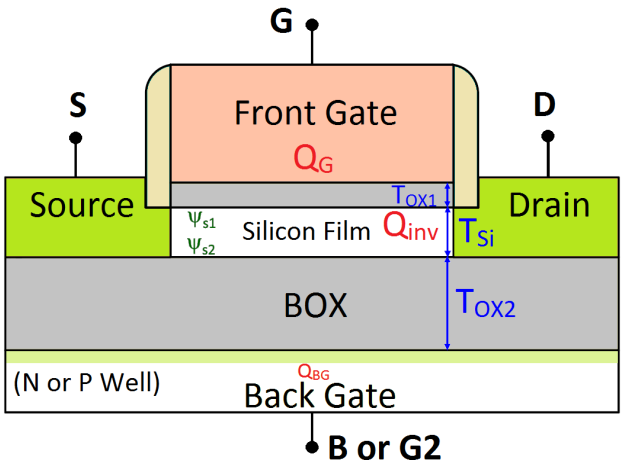



Fig. 2.1 UTBB transistor architecture (cross-section) with modeled charges as well as front and back surface potentials.

## 2.2.1 C-V characteristic

Fig. 2.2 shows the measured front gate to channel capacitance $C_{gc}$ normalized using the front oxide capacitance $C_{ox}$ with respect to the front gate voltage $V_{GS}$ for various back gate voltages $V_{bG}$, and for N type MOSFET. The first observation is that $C_{gc}$ characteristic shifts towards negative $V_{GS}$ when $V_{bG}$ is increased. This is evidencing the impact of the back gate voltage on the threshold voltage. Same observation, in absolute values, applies to the P type MOSFET as depicted in Fig. 2.3. It should be noted that, thanks to a thick buried oxide (BOX), higher voltages can be applied to the back gate ($V_{bG}$ is covering a very large -10 V to 10 V range).

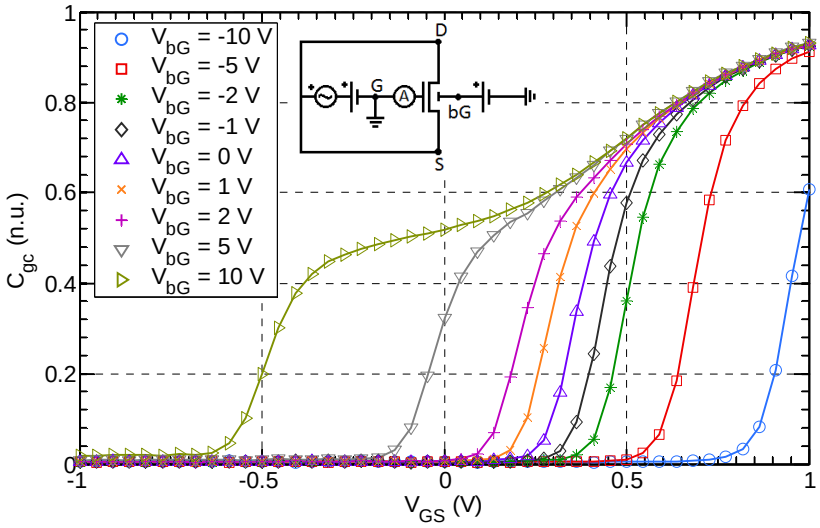



Fig. 2.2 Measured and normalized front gate capacitance versus front gate voltage for various back gate voltages for NMOS and at $V_{DS}$ = 0 V (L = 10 µm, W = 2 µm, MULT = 30). Inset: diagram showing C-V measurement procedure.

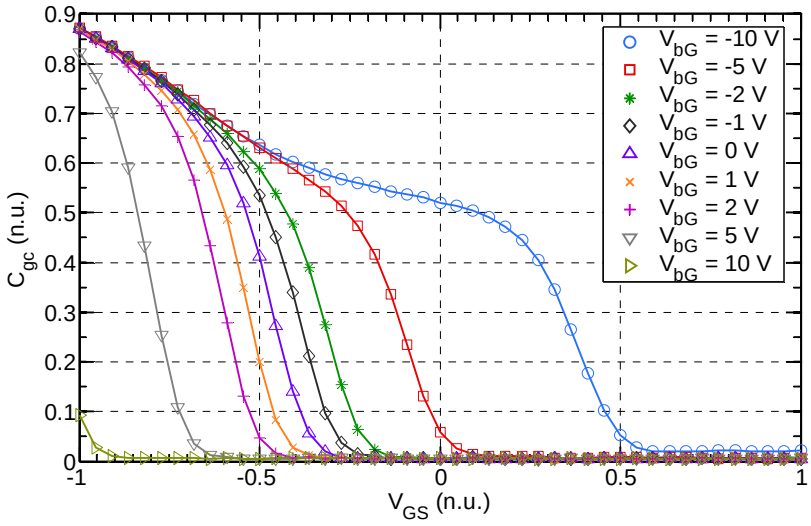



Fig. 2.3 Measured and normalized front gate capacitance versus front gate voltage for various back gate voltages for PMOS and at $V_{DS}$ = 0 V (L = 10 µm, W = 2 µm, MULT = 30).

In [90], the derivative of the gate to channel capacitance $C_{gc}$ with respect to $V_{GS}$ is used to extract a threshold voltage. Actually, in bulk, we have the following relation:

$$C_{gc} \equiv \frac{\partial Q_{inv}}{\partial V_{GS}} = \frac{\partial (C_{ox} \cdot V_{ox})}{\partial V_{GS}} = C_{ox} \frac{\partial V_{ox}}{\partial V_{GS}} = C_{ox} \frac{\partial (V_{GS} - \Psi_s)}{\partial V_{GS}} = C_{ox} \left(1 - \frac{\partial \Psi_s}{\partial V_{GS}}\right) \quad (2.1)$$

where $Q_{inv}$, $C_{ox}$, $V_{ox}$, and $\psi_s$ are respectively the inversion charge, the oxide capacitance, the oxide voltage drop, and the surface potential. If we derive (2.1) with respect to $V_{GS}$, we get:

$$\frac{\partial C_{gc}}{\partial V_{GS}} = -C_{ox}\frac{\partial^2 \Psi_s}{\partial V_{GS}^2} \tag{2.2}$$

This quantity becomes equal to zero at the inflection point of the surface potential plot with respect to $V_{GS}$ and corresponds to the inversion charge rise. Therefore, the maximum of the $C_{gc}$ derivative determines the $V_{GS}$ at which an accelerated increase of the capacitance occurs, which is in turn a consequence of the inversion start in the channel. The derivative of $C_{gc}$ for a UTBB FDSOI MOSFET is shown in Fig. 2.4 for an NMOS case. For high $V_{bG}$, two local maximums are observed, which cannot be observed in bulk, where no back interface is available, and bulk voltage range is limited because of the source and the drain to bulk junctions. The two local maximums can be explained by the existence of two “inversions” that are taking place at two different $V_{GS}$ values. Similar $C_{gc}$ plots are reproduced using TCAD simulations on a simplified deck (no raised source and drain, constant mobility, and $T_{si}$ = 6 nm) for three $V_{bG}$ values in Fig. 2.5 along with the corresponding carriers concentration evolution in the silicon film with respect to $V_{GS}$ for $V_{bG}$ = 7 V in Fig. 2.6. For higher $V_{bG}$, the back interface is inverted first, which corresponds to the local maximum of the capacitance derivative at low $V_{GS}$. A cross section view for this situation is shown in Fig. 2.7 (b) where carrier’s concentration near the back interface is higher. The second local maximum occurs when the front interface is inverted at $V_{GS} \approx 0.6$ V. This is evidenced in Fig. 2.6 where carrier concentration is almost constant in the volume of the silicon film with a local maximum near the front gate for $V_{GS}$ = 1 V. In Fig. 2.7, the electrons concentration at $V_{GS}$ = 0 V (a) is very low as the channel is not inverted. The concentration is maximum close to the back interface at lower $V_{GS}$ = 0.3 V (b) and maximum at the front interface for $V_{GS}$ = 1 V (c). Actually, the carriers occupy all the thickness of the silicon film. The concentration of the carriers is maximizing locally based on the applied gate voltage. This is a demonstration of the volume inversion in the silicon film of the UTBB FDOI.

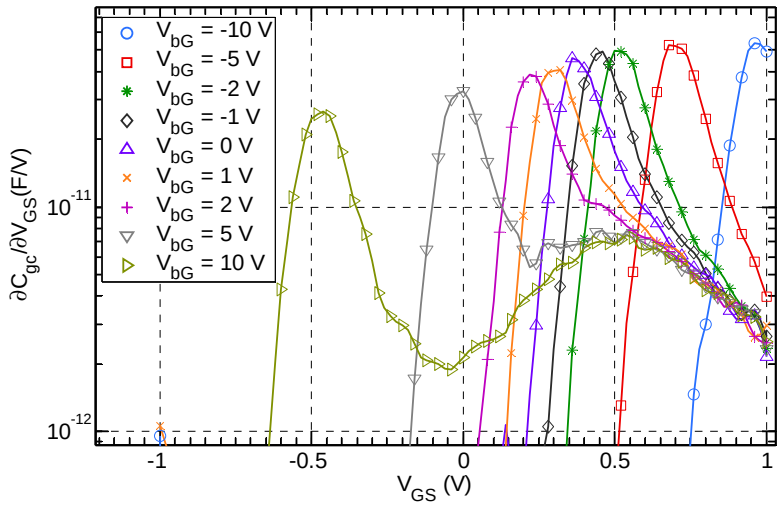



Fig. 2.4 Measured gate capacitance derivatives versus $V_{GS}$ for various back gate voltages for NMOS (L = 10 µm, W = 2 µm, MULT = 30).

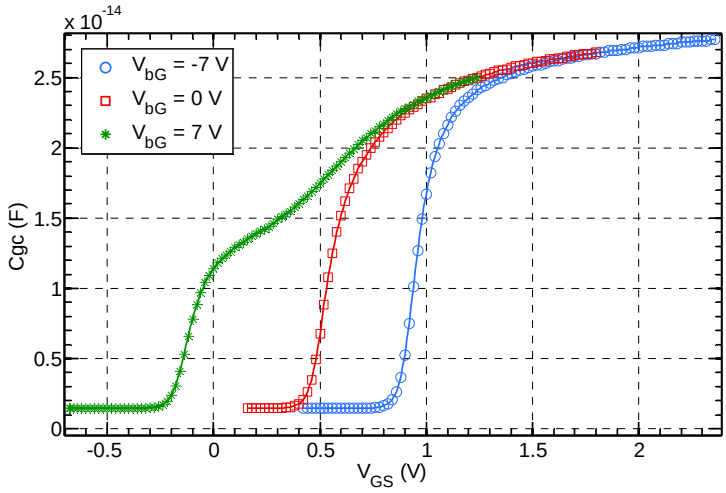



Fig. 2.5 TCAD simulations of the gate capacitance versus $V_{GS}$ for three $V_{bG}$ values (-7 V, 0 V, and 7 V) for L = 1 µm and $V_{DS}$ = 1 V.

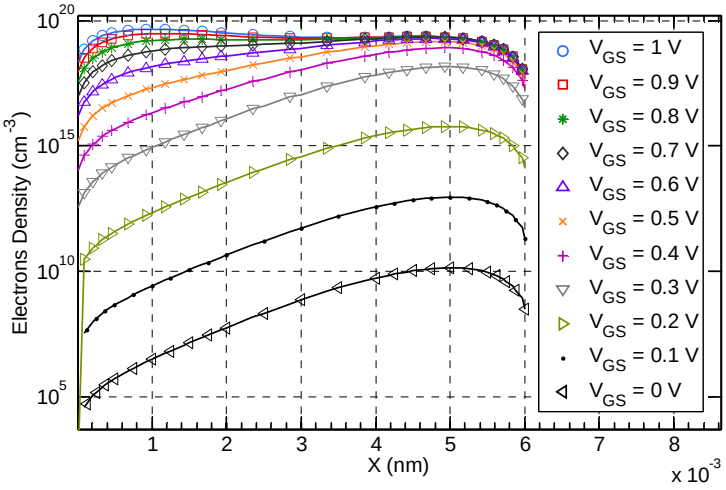



Fig. 2.6 Electron concentration versus position in the silicon film for various $V_{GS}$ values and fixed $V_{bG}$ = 7 V for L = 1 µm and $V_{DS}$ = 1 V.

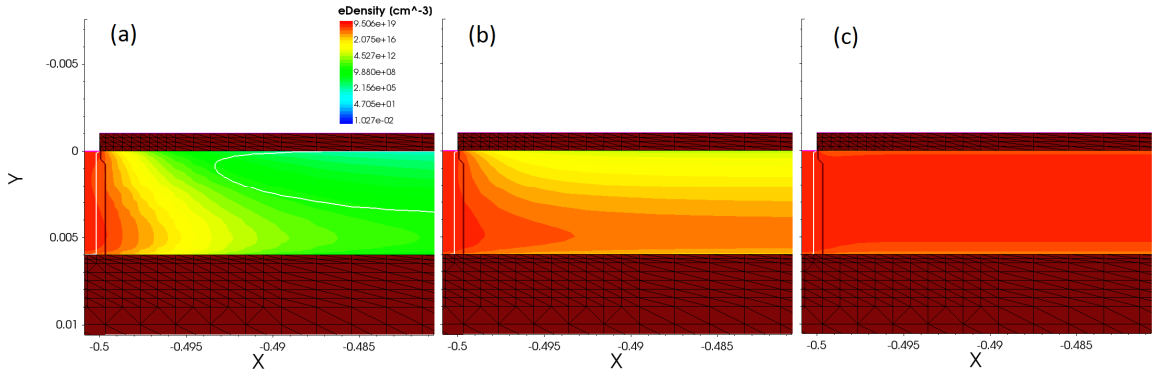



Fig. 2.7 Electron concentration using TCAD simulations for fixed $V_{bG}$ = 7 V, and (a) $V_{GS}$ =0 V, (b) at threshold $V_{GS}$ = 0.3 V and (c) $V_{GS}$ = 1 V for L = 1 µm and $V_{DS}$ = 1 V.

Based on Fig. 2.4, front gate threshold voltage values are extracted for the different $V_{bG}$ cases. For high $V_{bG}$ cases, the local maximum for lower $V_{GS}$ is considered. The result is plot in Fig. 2.8. A slope of approximately 80 mV/V is extracted for $V_{bG} > 0$ V and approximately 65 mV/V for $V_{bG} < 0$ V.

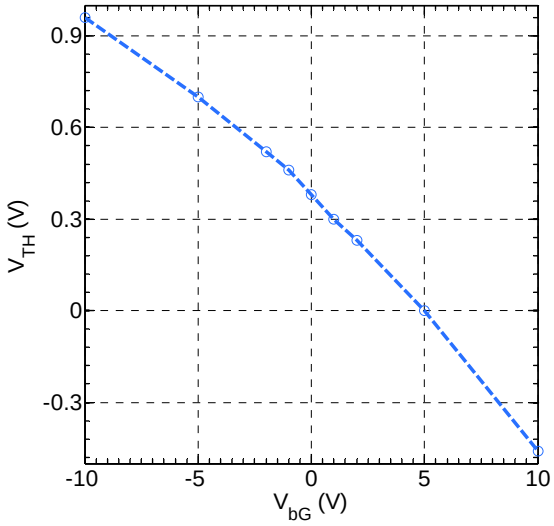



Fig. 2.8 Front gate threshold voltage $V_{TH}$ versus back gate voltage $V_{bG}$ for NMOS (L = 10 µm, W = 2 µm, MULT = 30)

## 2.2.2 I-V characteristic

The C-V characteristic at low or zero $V_{DS}$ provides insight into the device electrostatic. However, for DC operation, a positive $V_{DS}$ is applied between the drain and source of the MOSFET to produce a lateral electrical field that enhances the current through the channel. Fig. 2.9 shows measured input characteristics $I_D$-$V_{GS}$ for various back gate voltages $V_{bG}$ in a logarithmic scale. The logarithmic scale is convenient to highlight the operation in the weak and moderate inversion regimes. The first observation is that all $I_D$-$V_{GS}$ plots have similar shapes with a shift towards negative $V_{GS}$ values while $V_{bG}$ is increased. An important figure of merit is the slope of this input characteristic in its logarithmic scale, which is nothing other than the $g_m$ over $I_D$ as we have:

$$FoM = \frac{\delta \ln I_D}{\delta V_{GS}} = \frac{1}{I_D}\frac{\partial I_D}{\partial V_{GS}} = \frac{g_m}{I_D} \qquad (2.3)$$

If we plot the $g_m$ over $I_D$ characteristic with respect to the normalized current $I_D$.L/W for various $V_{bG}$ in a log-log scale, we get the interesting invariance property shown in Fig. 2.10. This property will be assessed in Chapter 3 using measurements with respect to geometry, back gate voltage, temperature, drain to source voltage, and process variations. For SI, all the plots tend to the square law characteristic which varies as the inverse of the square root of the current. For WI, a plateau is measured with a level as

high as 36 $V^{-1}$, which corresponds to a near ideal slope factor of 1.08. The fixed value in WI corroborated the exponential evolution of the drain current with respect to $V_{GS}$.

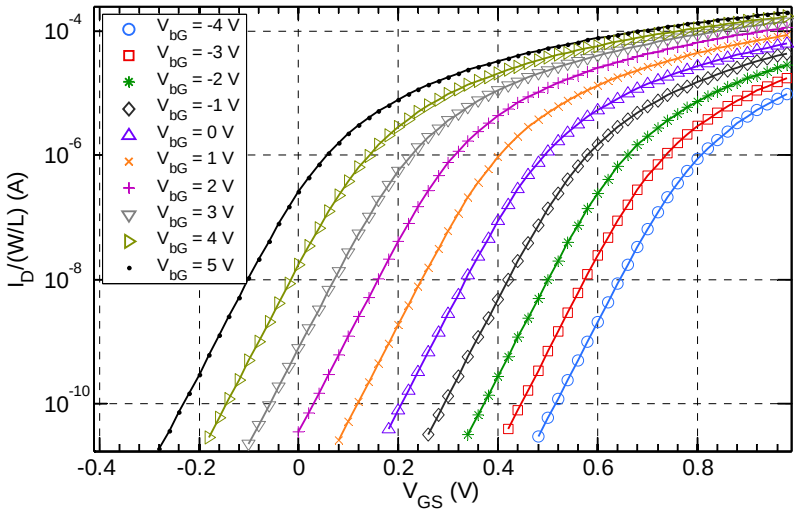



Fig. 2.9 Measured and normalized drain current (i.e. $I_D/(W/L)$) versus front gate voltage $V_{GS}$ for $V_{DS}$ = 1 V and various back gate voltages for NMOS (L = 1 µm, W = 1 µm).

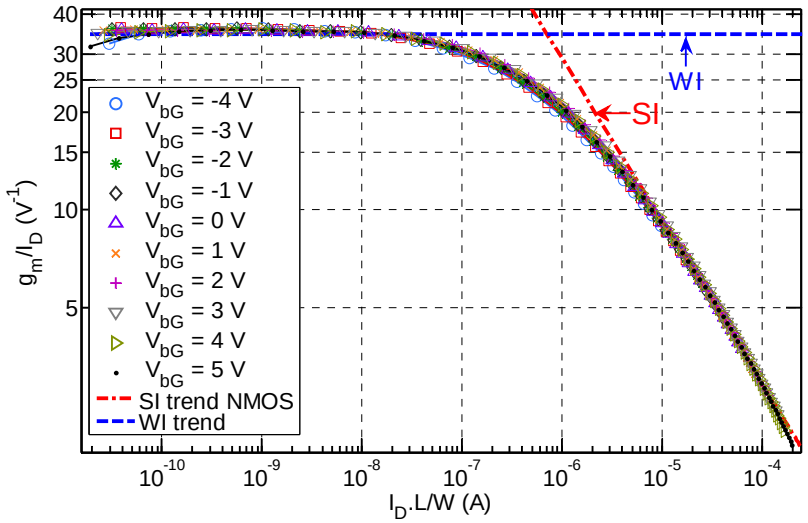



Fig. 2.10 Measured $g_m$ over $I_D$ characteristics versus normalized drain current $I_D/(W/L)$ for various back gate voltages $V_{bG}$ along with the WI and SI trends for NMOS (L = 1 µm, W = 1 µm, $V_{DS}$ = 1 V).

Apparently, similar observations can be made as for the C-V characteristics exploitation regarding the impact of the back gate voltage. In order to have a closer insight into the threshold voltage evolution based on I-V characteristics, the $g_m$ over $I_D$ is used as in [91]. In bulk, the derivative of the $g_m$ over $I_D$ is used to extract a threshold voltage noting that we have in WI and using (2.2):

$$I_D = I_0 e^{\left(\frac{\Psi_s}{U_T}\right)}$$
$$\frac{g_m}{I_D} = \frac{\delta \ln I_D}{\delta V_{GS}} = \frac{1}{U_T}\frac{\partial \Psi_s}{\partial V_{GS}} \quad (2.4)$$

Consequently we get:

$$\frac{\partial\left(\frac{g_m}{I_D}\right)}{\partial V_{GS}} = \frac{1}{U_T}\frac{\partial^2 \Psi_s}{\partial V_{GS}^2} \quad (2.5)$$

In bulk, this quantity is proportional to the quantity expressed in (2.2), and also determines the inversion charge rise when set to 0. The derivatives of the $g_m$ over $I_D$ with respect to $V_{GS}$ are shown in Fig. 2.11. Surprisingly, we don't observe two local maximums for high $V_{bG}$ as observed in Fig. 2.4, and the extracted threshold voltages are not exactly the same as those extracted using the capacitance derivatives (i.e. up to 90 mV mismatch as reported in Table 2-1 knowing that DIBL cannot be the root cause of this difference at $V_{DS}$ = 50 mV). It should be noted that, for low $V_{bG}$ (particularly for $V_{bG} \leq 0$ V) and based on (2.2) and (2.5), the following equality is verified:

$$U_T \cdot \frac{\partial\left(\frac{g_m}{I_D}\right)}{\partial V_{GS}} = -\frac{1}{C_{ox}} \cdot \frac{\partial C_{gc}}{\partial V_{GS}} \quad (2.6)$$

Therefore, this demonstrates that the $V_{TH}$ extraction methodology proposed by Flandre [91] for advanced MOSFETs cannot be applied to an asymmetric DG MOSFET especially at positive back gate voltages where apparent mobility is highly affected by the front and back gates control.

For low $V_{bG}$, where the inversion charge is closer to the front interface like in the bulk case, the inflexion point of the surface potential is rather closely tied to the electrostatic behavior of the device. However, for high $V_{bG}$ with a stronger volume inversion phenomena, the equality in (2.6) is no more valid and the mobility contributes also to the observed difference in the threshold voltage values extracted using the C-V derivative based method with respect to the $g_m/I_D$ derivative based method.

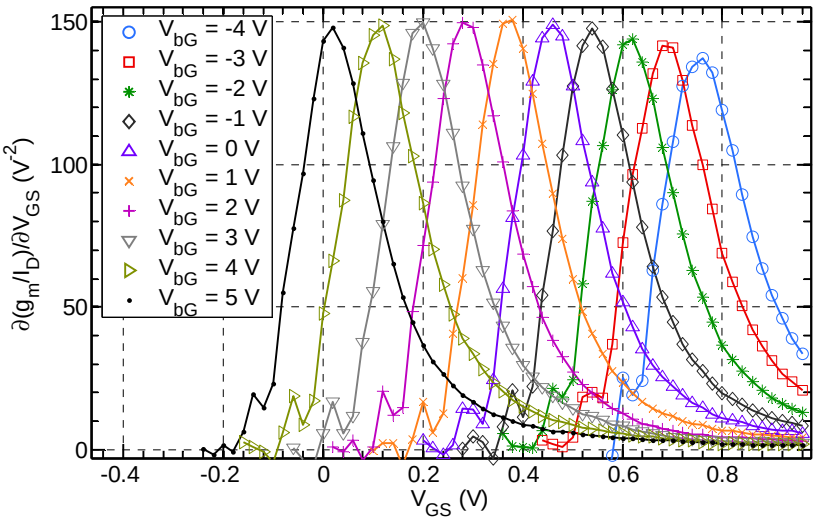



Fig. 2.11 Measured $g_m$ over $I_D$ derivative versus front gate voltage for $V_{DS}$ = 0.05 V and various back gate voltages for NMOS (L = 1 µm, W = 1 µm).

Table 2-1 Threshold voltage comparison between the C-V derivative based and $g_m/I_D$ derivative based methods.

| **$V_{bG}$ (V)** | -2 | -1 | 0 | 1 | 2 | 5 |
|---|---|---|---|---|---|---|
| C-V derivative based method | 0.52 | 0.46 | 0.38 | 0.3 | 0.22 | 0 |
| **$g_m/I_D$ derivative based method** | 0.61 | 0.54 | 0.46 | 0.37 | 0.29 | 0.017 |
| Delta (V) | 0.09 | 0.08 | 0.08 | 0.07 | 0.07 | 0.017 |

TCAD simulations on a calibrated deck (raised source and drain for lower series resistance, $T_{si}$ = 7 nm, and advanced mobility model using the thin layer mobility with enhanced carrier effective mass [86]) are run and the results are shown in Fig. 2.12 and Fig. 2.13. As expected, the inversion charge concentration depicted in Fig. 2.12 (b)-(d) is higher at the front of the Si film for low $V_{bG}$ and higher at the back of the Si film for high $V_{bG}$. At some specific front and back gates voltages, the volume inversion phenomena is enhanced. The $I_D$-$V_{GS}$ is also reproduced accurately in Fig. 2.12 (a). The extraction of the threshold voltage using both the $C_{gc}$ and $g_m/I_D$ derivatives provided similar conclusions than those based on measurement data. This is depicted in Fig. 2.13 where capacitance and $g_m/I_D$ based threshold voltages are close for $V_{bG}$ = 5 V in (a) and (b). At $V_{bG}$ = 10 V, the negative threshold voltage result is close to the

measured one. However, as illustrated in Fig. 3.1, the $g_m$ over $I_D$ invariance evidenced using measurement data in Fig. 2.10 is not reproduced using TCAD simulations most probably because of the TCAD transport model limitations. The $g_m$ over $I_D$ invariance is studied in detail in Chapter 3.

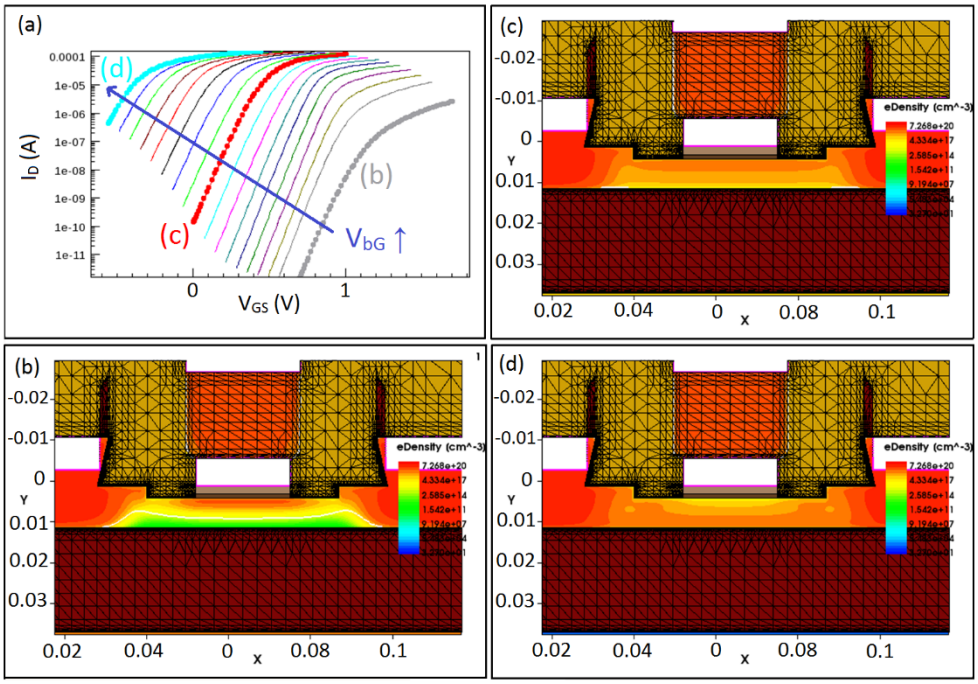



Fig. 2.12 TCAD simulations showing the impact of the back gate voltage on carriers concentration and consequently on input characteristic $I_D$ - $V_{GS}$. (a) $I_D$ - $V_{GS}$ for various $V_{bG}$ from -10 V to 8 V. (b) channel inversion at the front for negative $V_{bG}$ = -10 V (c) channel inversion in silicon film volume at $V_{bG}$ = 0 V, and (d) channel inversion local maximum near the back interface for $V_{bG}$ = 8 V. Distance unit is µm.

Both electrostatic and transport contribute to the $g_m$ over $I_D$ characteristic as:

$$\frac{g_m}{I_D} = \frac{\partial \ln I_D}{\partial V_{GS}} = \frac{1}{Q_{inv}} \frac{\partial Q_{inv}}{\partial V_{GS}} + \frac{1}{v} \frac{\partial v}{\partial V_{GS}} \tag{2.7}$$

noting that $I_D = Q_{inv} \cdot v$, where $v$ is the average velocity of the charge carrier. In order to assess the transport contribution to the $g_m$ over $I_D$ characteristic, we propose to use a simple mathematical expression based on (2.7) and given as:

$$\frac{1}{v} \frac{\partial v}{\partial V_{GS}} = \frac{g_m}{I_D} - \frac{1}{Q_{inv}} \frac{\partial Q_{inv}}{\partial V_{GS}} \tag{2.8}$$

This mathematical operation is applied to measured data for various $V_{bG}$ values. Inversion charge $Q_{inv}$ is extracted using a careful integration of the $C_{gc}$–$V_{GS}$ characteristics.

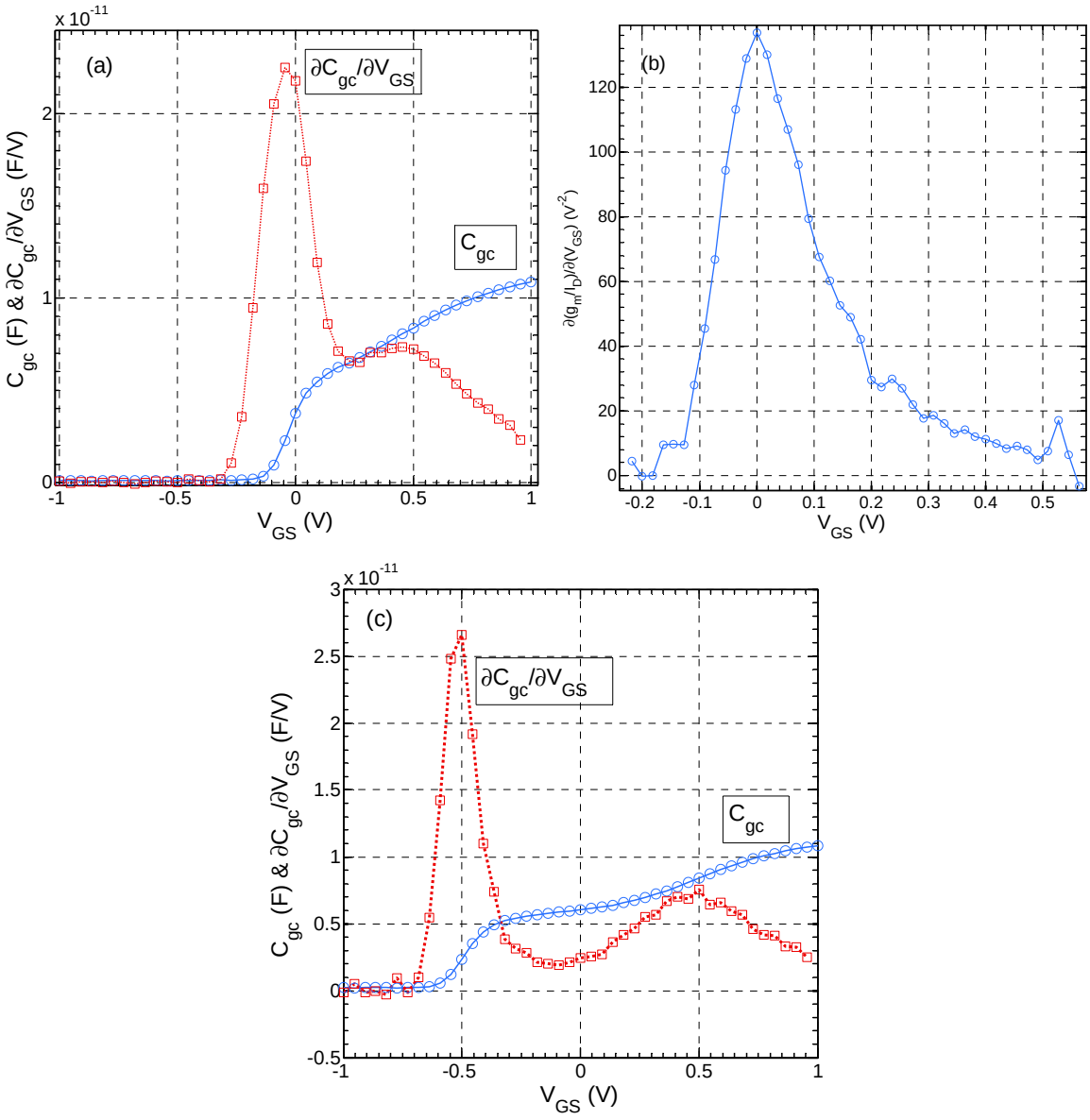



Fig. 2.13 TCAD simulations showing (a) $C_{gc}$ and its derivative for $V_{bG}$ = 5 V (b) derivative of $g_m/I_D$ for $V_{bG}$ = 5 V, and (c) $C_{gc}$ and its derivative for $V_{bG}$ = 10 V, L = 1 µm and $V_{DS}$ = 1 V

The electrostatic part of (2.8) is shown in Fig. 2.14 (b) with respect to the normalized drain current. The $g_m$ over $I_D$ is measured in linear mode ($V_{DS}$ = 0.05 V) to be as close as possible to the $C_{gc}$-$V_{GS}$ bias conditions. The $g_m$ over $I_D$ plots are shown in Fig. 2.14 (a) where the invariance is evidenced for linear mode too. The transport contribution to the $g_m$ over $I_D$ is finally depicted in Fig. 2.15 with respect to both $V_{GS}$ in (a) and $I_D$.L/W

in (b). We clearly observe the impact of the $V_{bG}$ on carrier velocity. As for the $g_m$ over $I_D$ at high currents, the transport quantity which is equal to the derivative of ln(*v*) with respect to $V_{GS}$ has its minimum at higher velocities. Therefore, for intermediate $V_{bG}$ values, thanks to the volume inversion strength, the maximum apparent carrier velocity is higher. The term “apparent” stands for the fact that the transport metrics we extract (i.e. carrier velocity or mobility) using drain current characteristic represents an average on all carriers in the silicon film (i.e. in all its volume). Thanks to a lower vertical field, while volume inversion is taking place, more carriers in the Si volume are contributing to the transport and this is observed as an increase of the mobility in various publications such as in Ohata [92] and Rudenko [93]. Moreover, we will demonstrate using a novel method based on high frequency NQS effect that mobility is practically unchanged over all levels of inversion (cf. Section 5.7). Our interpretation is also corroborated in Chapter 3 while studying the invariance of the transconductance efficiency (cf. Fig. 3.6).

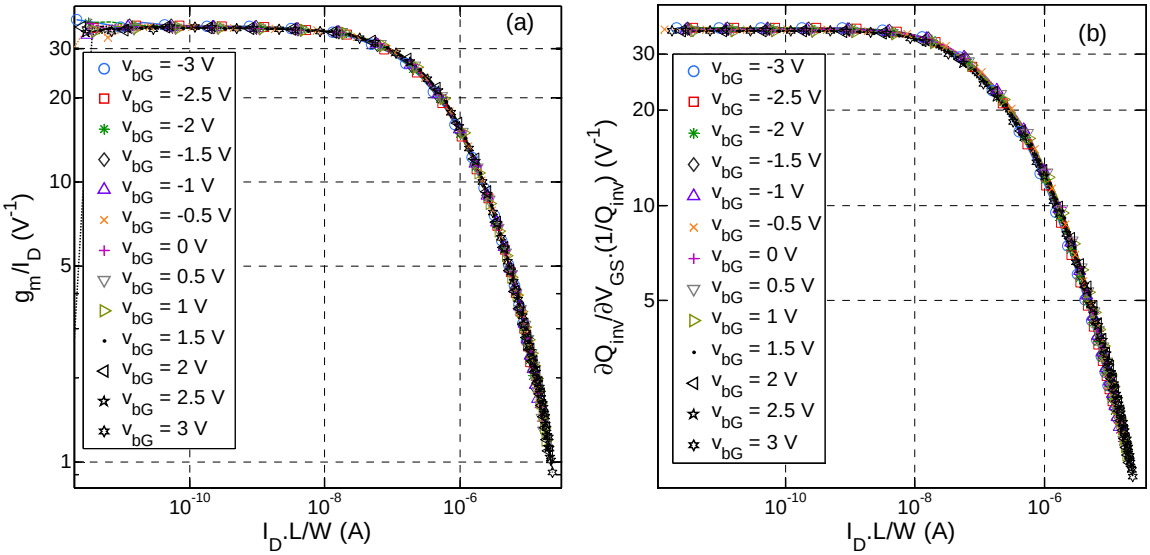



Fig. 2.14 Measurements showing (a) $g_m$ over $I_D$ and (b) $\partial(\ln(Q_{inv})/\partial V_{GS}$ versus normalized drain current for various $V_{bG}$ values (from -3 V to 3 V) in linear mode ($V_{DS}$ = 50 mV).

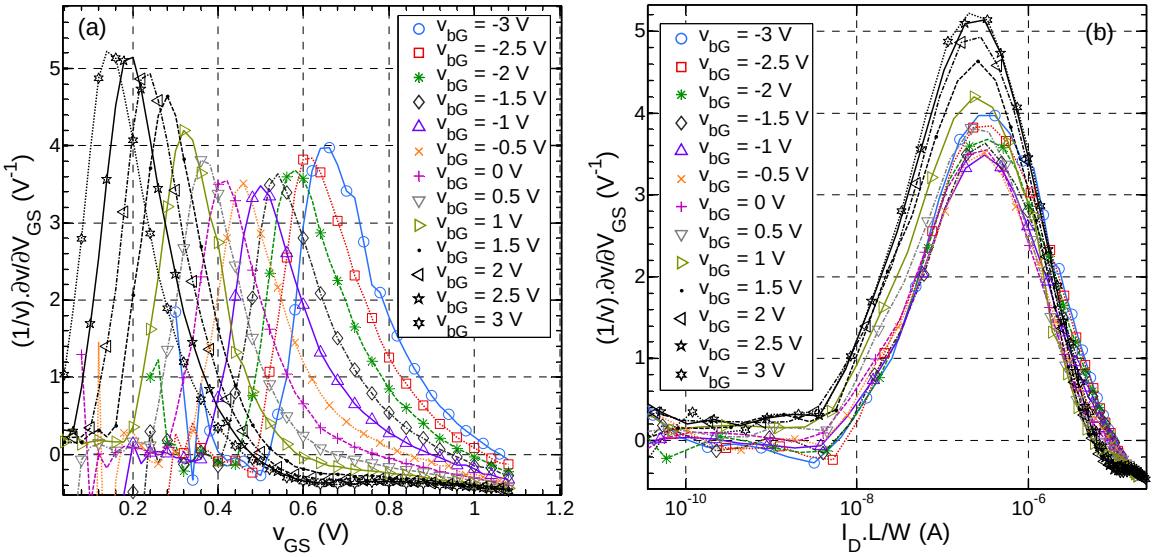



Fig. 2.15 Measurements showing the transport term $\partial \ln(v)/\partial V_{GS}$ versus gate voltage $V_{GS}$ in (a) and normalized drain current in (b) for various $V_{bG}$ values (from -3 V to 3 V) in linear mode (L = 1 µm, W = 1 µm).

## 2.3 DC and low frequency small-signal operation modeling and characterization

The accuracy of circuit simulations mainly depend on the quality of the involved models. High quality models are physics based and verified against measurements for various geometries and bias conditions. For DC and low frequency operation of the UTBB FDSOI MOSFET, two modeling approaches are used in this work. On the one hand simple hand calculation expressions or charts along with an equivalent small signal circuit are used to predict main bias currents/voltages, and small signal FoMs of the transistor, and on the other hand the newly proposed UTSOI2 compact model, which is suitable for an industrial usage. The advantage of the first approach is its simplicity and suitability for analog design context, in that it helps to get insight into the behavior of the MOSFET without the complexity of a compact model. However, this simple approach is not adapted for large circuit simulations where scalability and variability models are required. The second approach is the most adapted for an industrial usage provided that the quasi-static compact model is augmented and completed for high frequency accuracy. This second approach is proposed and validated in our work, while the first approach is used for simplicity when relevant.

In this Section, first the long channel DC model is discussed to pave the road towards the dynamic small signal model using equivalent circuits. Next, the main physical effects involved are briefly described. Finally, the DC and low frequency operation is assessed through several MOSFET metrics and FoMs.

### 2.3.1 Long channel DC modeling – a threshold voltage based approach

In Fig. 2.10, UTBB FDSOI I-V characteristic in SI is shown to be very close to the square law derived for early bulk technologies in the case of a long channel for which mobility reduction, velocity saturation, and series resistance have lower impact. In WI, I-V characteristic follows an ideal exponential law with constant slope in logarithmic scale. Having these observations in mind, we propose to re-derive the square law I-V model for the bulk case using a special mathematical approach. Then the validity of the square law is discussed for the UTBB FDSOI case. In particular, we show that the square law model is valid in SI provided that the threshold voltage expression is adapted for a double gate architecture.

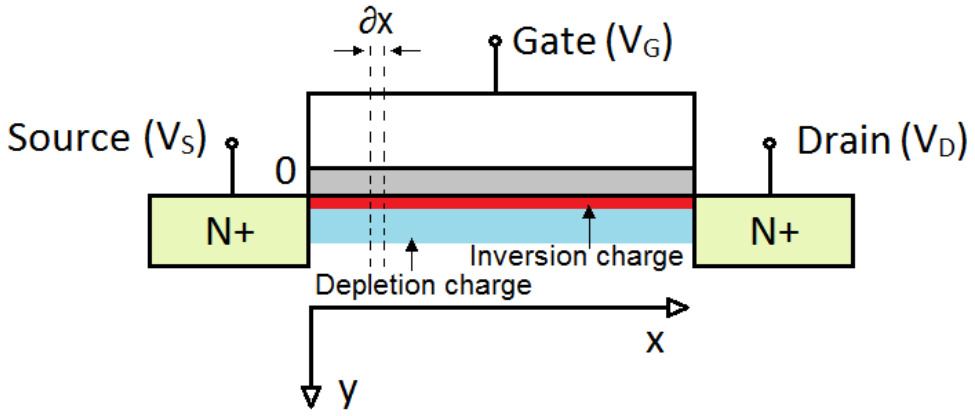



Fig. 2.16 Cross section of the bulk MOSFET for $V_D = V_S$ (N-type)

In the case of the bulk N-type MOSFET shown in Fig. 2.16, which is somehow comparable to the case of FDSOI with infinite silicon film thickness, the drain current is expressed using the drift and diffusion contributions as [94]:

$$I_D = W\left(-\mu . Q_i . \frac{\partial \psi_s}{\partial x} + \mu U_T \frac{\partial Q_i}{\partial x}\right) = -\mu W Q_i \frac{\partial V}{\partial x} \qquad (2.9)$$

where

μ is the carrier mobility at x (x = 0 at the source side).

$Q_i$ is the inversion charge at x

$\Psi_s$ is the surface potential at x

$U_T$ is the thermal voltage

V is the quasi-Fermi level

Since $I_D$ is constant at any location x along the channel, deriving (2.9) one obtains:

$$\frac{\partial I_D}{\partial x} = \frac{\partial Q_i}{\partial x}.\mu.\frac{\partial V}{\partial x} + Q_i.\frac{\partial \mu}{\partial x}.\frac{\partial V}{\partial x} + Q_i.\mu.\frac{\partial^2 V}{\partial x^2} = 0 \qquad (2.10)$$

If we consider a constant mobility in the channel, the differential equation (2.10) becomes:

$$\frac{\partial Q_i}{\partial x}.\frac{\partial V}{\partial x} + Q_i.\frac{\partial^2 V}{\partial x^2} = 0 \qquad (2.11)$$

The inversion charge $Q_i$, which is the algebraic sum of the gate and depletion charges, can be obtained by linearizing the maximum depth of the depletion region as a function of the quasi-Fermi level V(x) [95]. The inversion charge is given in SI by:

$$Q_i = Q_i(x) = -C_{ox}\big(V_G - V_{TH} - n.V(x)\big) \qquad (2.12)$$

where $C_{ox}$ and $V_{TH}$ are respectively the oxide capacitance per unit area and the threshold voltage, and n is the slope factor approximated using the capacitive divider based expression:

$$n = 1 + \frac{C_{dep}}{C_{ox}} \qquad (2.13)$$

where $C_{dep}$ is the depletion capacitance.

The inversion charge expression (2.12) can be derived using Gauss's law at the interface and from the interface to a region deep in the Si bulk, and assuming the thickness of the inversion layer is negligible (charge sheet approximation).

Using (2.12) in (2.11), we obtain the following differential equation:

$$-n.\left(\frac{\partial V}{\partial x}\right)^2 + (V_G - V_{TH} - n.V).\frac{\partial^2 V}{\partial x^2} = 0 \qquad (2.14)$$

If we define: $X = V_G - V_{TH} - n.V$, (2.14) becomes:

$$(X')^2 + X.X'' = 0 \qquad (2.15)$$

This linear second order differential equation can be solved using a new variable defined as:

$$U = X' = \frac{dX}{dx} \qquad (2.16)$$

Deriving (2.16) gives:

$$X'' = \frac{dU}{dX}U \qquad (2.17)$$

The differential equation (2.15) becomes:

$$\frac{dU}{U} = -\frac{dX}{X} \qquad (2.18)$$

After integration one obtains:

$$U = \frac{1}{X}.e^{K_1} = \frac{dX}{dx} \qquad (2.19)$$

where $K_1$ is an integration constant which is determined using the following boundary conditions: $V(x=0) = V_S = 0$ and $V(x=L) = V_D$, where L is the channel length. Using the boundary conditions, a second integration of (2.19) (steps are not shown) provides the expression of X as a function of the location x, which leads to:

$$V(x) = \frac{V_G - V_{TH}}{n}\left[1 - \sqrt{1 - \frac{x}{L}\left[1 - \left(1 - \frac{n.V_D}{V_G - V_{TH}}\right)^2\right]}\right] \quad (2.20)$$

Same expression is obtained if one choses, as a solution for (2.15), the following expression:

$$X = \alpha \cdot \sqrt{1 - \beta x} \quad (2.21)$$

Using (2.20) for x = 0 (at the source side), the drain current expression (2.9) becomes:

$$I_D = \frac{W}{L} C_{ox} \mu \left[(V_G - V_{TH}) - \frac{n.V_D}{2}\right] V_D \quad (2.22)$$

The latter equation describes the linear region operation of the MOSFET, which is a parabolic dependence of the drain current on the drain voltage. $I_D$ reaches a maximum when the drain voltage is equal to $V_{DSAT}$. Using $\partial I_D/\partial V_D = 0$ and assuming that $V_S = 0$, $V_{DSAT}$ is given by:

$$V_{DSAT} = \frac{V_G - V_{TH}}{n} \quad (2.23)$$

And replacing $V_{DSAT}$ in (2.22) gives the drain saturation current commonly known as the square law:

$$I_D = \frac{W}{L} C_{ox} \mu \frac{(V_G - V_{TH})^2}{2n} \quad (2.24)$$

The previous bulk inversion charge derivation cannot be applied as such to an asymmetric double gate such as UTBB FDSOI MOSFET, where the buried oxide capacitance and the back Si/SiO2 interface state can have a considerable impact on the front inversion charge. Moreover, in the state of the art UTBB FDSOI technology, the silicon film is undoped or lightly doped while in bulk the channel is doped. Actually even the charge sheet approximation is no more relevant if we consider a thin silicon film as stated earlier in Chapter 1.

In the following, we will show that similar WI and SI bulk models can be derived in the case of UTBB FDSOI, provided that the threshold voltage is adapted to the asymmetric double gate architecture.

Fig. 2.17 shows a cross section of the UTBB FDSOI under study. This structure has different front and back oxide thicknesses and different gate work-functions. A lightly-doped silicon film is assumed. Using the gradual channel approximation, the potential in the silicon film is obtained by solving the 1-D Poisson's equation and taking Gauss's law at the front and back surfaces as the boundary conditions. Then, front and back inversion charges are derived using the calculated front and back surface potentials. The details on the calculations based on [96] are given in Appendix A.

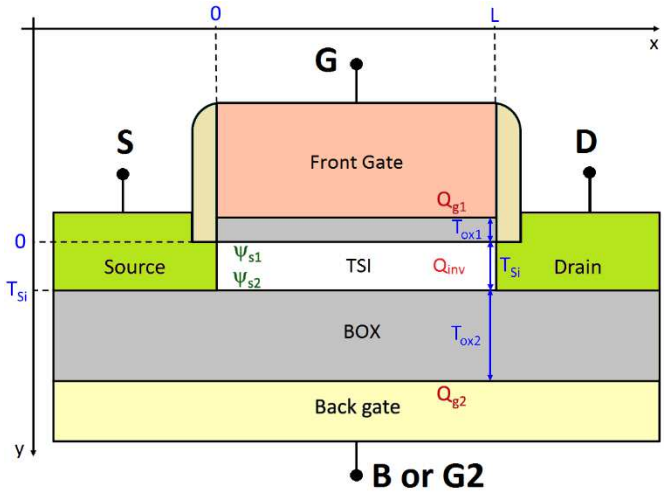



Fig. 2.17 FDSOI UTBB transistor architecture (cross-section) with involved charges as well as front and back surface potentials.

Inversion charges formulations using equivalent threshold voltages, comparable to the bulk case, are finally retrieved. The front and back threshold voltages expressions using physical dimensions, capacitances, and applied voltages are given as:

$$V'_{TH1} = n_{s1} \cdot U_T \cdot \ln\left(\frac{2 \cdot n_{s1} \cdot C_{ox1} \cdot U_T}{q \cdot n_i \cdot t_{Si}}\right) - (n_{s1} - 1) \cdot V'_{bG} - n_{s1} \cdot U_T \cdot \ln\left(\frac{\tanh\left(\frac{C_{eq}}{C_{Si}} \cdot \frac{V'_{bG} - V'_G}{2 \cdot U_T}\right)}{\frac{C_{eq}}{C_{Si}} \cdot \frac{V'_{bG} - V'_G}{2 \cdot U_T}}\right) \quad (2.25)$$

$$V'_{TH2} = n_{s2} \cdot U_T \cdot \ln\left(\frac{2 \cdot n_{s2} \cdot C_{ox2} \cdot U_T}{q \cdot n_i \cdot t_{Si}}\right) - (n_{s2} - 1) \cdot V'_G - n_{s2} \cdot U_T \cdot \ln\left(\frac{\tanh\left(\frac{C_{eq}}{C_{Si}} \cdot \frac{V'_{bG} - V'_G}{2 \cdot U_T}\right)}{\frac{C_{eq}}{C_{Si}} \cdot \frac{V'_{bG} - V'_G}{2 \cdot U_T}}\right) \quad (2.26)$$

where:

$V_G$' ($V_{bG}$') is the voltage difference between the front (back) gate voltage and the corresponding front (back) flat band voltage.

$n_{s1}$ and $n_{s2}$ are coupling factors equivalent to front and back slope factors, respectively.

$C_{ox1}$ and $C_{ox2}$ are the front and back oxide capacitances per unit area.

$t_{si}$ is the silicon film thickness.

q and $n_i$ are the electron charge and the intrinsic doping, respectively.

$C_{si}$ is the silicon film capacitance per unit area.

$C_{eq}$ is the equivalent capacitance per unit area of the series $C_{ox1}$, $C_{si}$, and $C_{ox2}$.

Refer to Appendix A for the expressions of the involved parameters.

The derivation in Appendix A and the threshold voltage expressions reproduced above show that a threshold voltage based approach is still valid at least at certain bias conditions. Threshold voltage expressions (2.25) and (2.26) are valid when the other interface is still in WI. When the other interface is strongly inverted, the threshold voltage is no more dependent on the other gate voltage as the other interface screens this effect. The case of both front and back interfaces inversion can be handled using coupling effects between the two interfaces. The generalization of this coupling effects is used by Lime [66], with a coupling charge expression given as:

$$Q_0 = C_{Si} \cdot (\Psi_{s1} - \Psi_{s2}) \tag{2.27}$$

The drain current is calculated using same general expression as in (2.9). The only difference is that the inversion charge has two components: front and back.

The above approach is proposed in [96] along with some modeling and physical limitations. Moreover, the WI and SI assumptions considered in above derivations are not valid in Moderate Inversion. Alternatives to this approach, using the surface potential or the inversion charge, are proposed in the literature as discussed in Chapter 1. For an industrial usage, UTSOI2 model is the first proposed compact model with a complete support of the back gate biasing, and therefore selected for large circuits simulations. A summary of the UTSOI2 model derivation is given in Appendix B. The several involved physical effects modeled in the quasi-static UTSOI2 are summarized in the table of Appendix C.

The drain current expression is complex in an asymmetric double gate MOSFET, and cannot be easily used for hand calculations in analog and RF design. However, we have shown that a threshold voltage based approach similar to bulk can be used to get a first insight, especially in SI and WI regimes. In MI where the simple models fail or for the case of short channels, measured charts (cf. Chapter 3) can be used to estimate the analog performance of the device. In particular, the UTBB FDSOI transconductance efficiency charts are shown to be predictable and generally invariant. This invariance, discussed in Chapter 3, can be used to predict the transconductance provided that W/L and level of inversion (i.e. IC) are given. Moreover, with the additional chart of IC with respect to the gate voltage overdrive $V_{GS}$ - $V_{TH}$ noting that a bijective relation exists between the two inversion metrics, one can predict drain current provided that W/L, $V_{TH}$, and gate voltage are provided. This can allow designers to predict MOSFET DC properties without the need of an analytical model including in MI which is difficult to capture.

For accurate integrated circuits simulations, model extraction is first based on I-V and C-V characteristics. Analog FoMs are compared with respect to measurements in DC and small signal low frequency operation. At the same time, in order to allow a simpler access to the different contributors to the small signal frequency operation,

equivalent circuits are proposed. For higher frequency operation, the core device using either UTSOI2 model or the lumped small-signal equivalent circuit is gradually enriched to capture new parasitic and distribution / delay effects.

### 2.3.2 Equivalent low frequency small signal circuit

UTBB FDSOI small-signal equivalent schematic valid in low-frequency operation is depicted in Fig. 2.18. It includes intrinsic MOSFET components such as the front transconductance $g_{m1}$ and extrinsic elements such as source and drain series resistances (i.e. $R_S$ and $R_D$, respectively). The explicit series resistances shown in Fig. 2.18 are taken into account in UTSOI2 implicitly in the mobility reduction saving some CPU time during circuit simulations as two circuit nodes are skipped. Gate-to-source ($C_{gs}$), gate-to-drain ($C_{gd}$) and front-to-back gates ($C_{gb}$) capacitances are also included as shown in Fig. 2.18. It should be noted that the equivalent circuit elements (i.e. capacitances and resistances) include both intrinsic and extrinsic parts. It is important to distinguish between the intrinsic (denoted by 'i') and extrinsic (denoted by 'e') contributions that have different origins. The intrinsic part is related to the device itself and mainly useful for channel current modulation, while the extrinsic part is related to parasitic elements unnecessary for the device operation. The extrinsic part can be optimized using proper layout technics such as multi-finger layout but cannot be completely removed. At high frequency operation the extrinsic elements gain particular importance and must be carefully modeled. At mm-Wave operation, these parasitic elements can even dominate the device performance.

The small-signal equivalent circuit depicted in Fig. 2.18 is frequently used in the literature to model small-signal operation of the MOSFET. This circuit was first proposed by Meyer in early semiconductor modeling life and enriched gradually. It represents the main channel modulation effect through $g_m$ along with the coupling effects of other terminals on MOSFET gate terminal through the three capacitances $C_{gs}$, $C_{gd}$ and $C_{gb}$. All the coupling effects represented in this equivalent circuit are extracted and validated under quasi-static operation. The quasi-static operation is defined when an applied small signal varies sufficiently slowly that the carriers in the channel can follow the variation simultaneously.

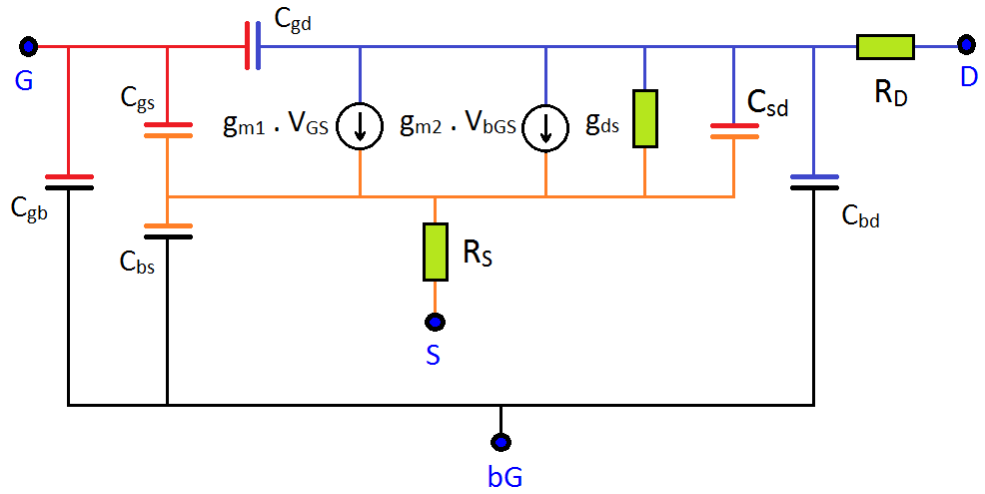



Fig. 2.18 Equivalent schematic for small signal and low-frequency operation of the UTBB FDSOI including series resistances $R_S$ and $R_D$ ($C_{gd} = C_{gdi} + C_{gde}$ and $C_{gs} = C_{gsi} + C_{gse}$).

One should be careful while using this simple equivalent circuit. Besides the lack of charge conservation in this equivalent circuit, it is only valid within the following assumptions:

- Transistor is used for amplification with the input signal entering to the gate terminal. The equivalent circuit cannot and should not be used to model a switch operation.
- The transistor configuration is common-source (CS).
- The coupling effect between drain and gate terminals is reciprocal which is rarely verified in saturation. In other words, one should verify that:

$$\frac{\partial Q_g}{\partial V_D} = \frac{\partial Q_d}{\partial V_G} \tag{2.28}$$

The last assumption is equivalent to assuming $C_{gdi} = C_{dgi}$ and it is important but not always verified even at low frequency operation as shown in Fig. 2.19. In saturation for example, a variation of the drain terminal voltage will not produce any change on the gate terminal charge because of pinch-off and consequently the intrinsic capacitance is equal to zero $C_{dgi} = 0$. However, a variation of the gate terminal voltage will produce a variation on the channel charge, which will produce a variation on drain charge through channel conduction, and thus $C_{dgi} \neq 0$. Fig. 2.19 shows the gate to drain

transadmittance $Y_{21}$ defined as the ratio of the two complex phasors representing the small current at the drain terminal and the small voltage at the gate terminal. $Y_{21}$ expression is given by:

$$Y_{21} \equiv \left.\frac{\widehat{I_D}}{\widehat{V_G}}\right|_{V_i=0, i\neq G} \tag{2.29}$$

Because of the reciprocal drain-gate capacitance in Fig. 2.18, the simple equivalent circuit provides different results compared to a compact model where charge conservation is verified. The difference is even observed at low frequency and is maximum at high frequency. Therefore, the difference between the two capacitances $C_{gdi}$ and $C_{dgi}$ must be taken into account and modeled. At high frequency operation the reciprocal $C_{gdi}$ and $C_{dgi}$ assumption is no more valid and these two coupling quantities diverge more because of non-quasi-static effects. This will be discussed in Chapter 4.

In general, the electrostatic couplings between the MOSFET terminals are not reciprocal, and for the dynamic operation modeling, 16 transcapacitances are required to agree with the charge conservation rule. Recent MOSFET compact models such as UTSOI2 account for the charge conservation, and the 16 transcapacitances are provided as part of the simulators DC OP information as discussed in Section 2.5.

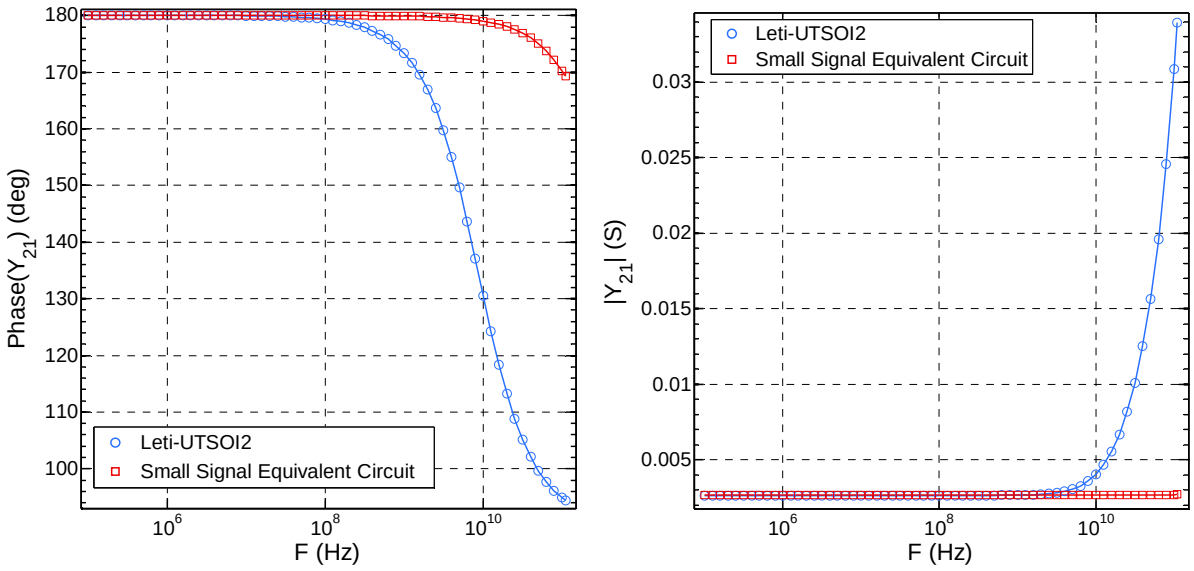



Fig. 2.19 NMOS gate to drain transadmittance phase (left) and modulus (right) simulated using Leti-UTSOI2 and the small signal equivalent circuit in Fig. 2.18. L = 1 µm, W = 10 µm, $N_F$ = 10, and $V_{GS}$ = $V_{DS}$ = 1 V.

The modeling of the non-reciprocal $C_{gd}$ and $C_{dg}$ capacitances effect can be done by adding an imaginary part $C_m$ to the transconductance $g_m$ (i.e. in parallel to it in an equivalent circuit). The proposed equivalent circuit is augmented using a mutual capacitance between the drain and the source terminals. The mutual capacitance is defined as [97]:

$$C_m = \frac{\partial Q_d}{\partial V_G} - \frac{\partial Q_g}{\partial V_D} = C_{dg} - C_{gd} \tag{2.30}$$

The new quasi static equivalent circuit is shown in Fig. 2.20 including series drain and source resistors. It should be noted that $C_{sd}$ is included when required in particular for short channels. In saturation, the new equivalent circuit provides strictly the same results as the Leti-UTSOI2 model as shown in Fig. 2.21.

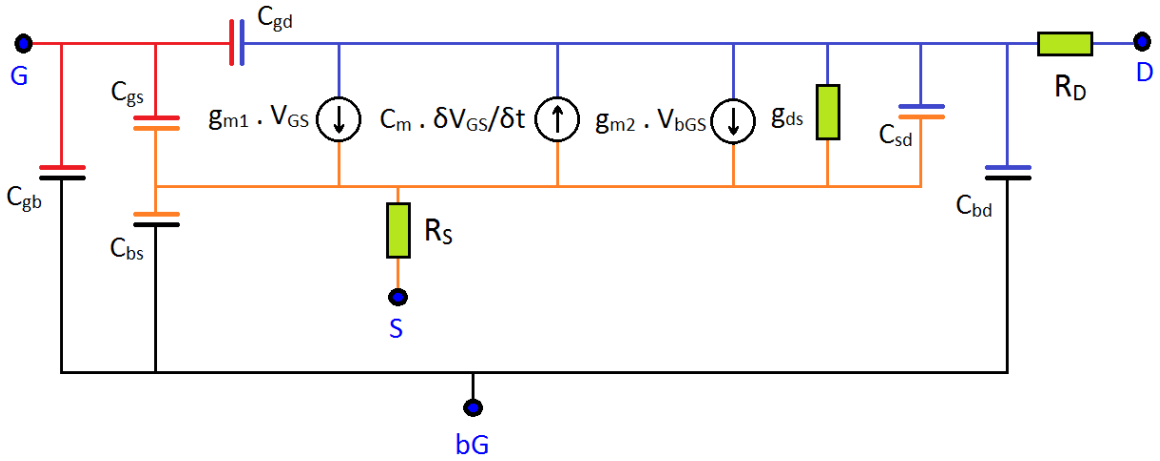



Fig. 2.20 Equivalent schematic for small signal and quasi-static operation of the UTBB FDSOI MOSFET including series resistances $R_S$ and $R_D$ ($C_{gd} = C_{gdi} + C_{gde}$ and $C_{gs} = C_{gsi} + C_{gse}$).

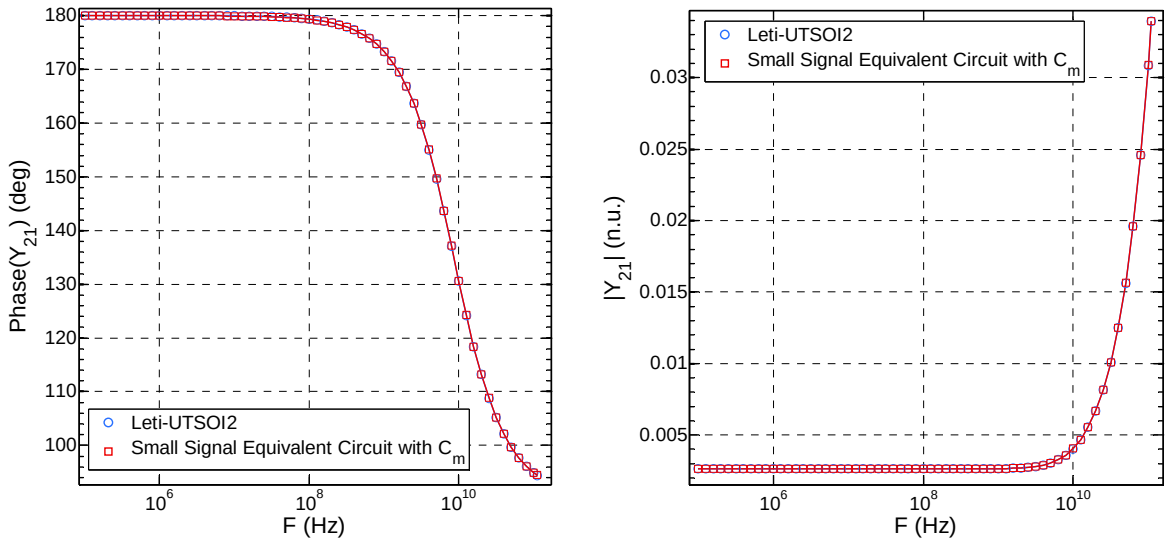



Fig. 2.21 NMOS gate to drain transadmittance phase (left) and modulus (right) simulated using Leti-UTSOI2 and the quasi-static small signal equivalent circuit in Fig. 2.20. L = 1 µm, W = 10 µm, $N_F$ = 10, and $V_{GS}$ = $V_{DS}$ = 1 V.

The parameters of the equivalent circuit in Fig. 2.18 are extracted using measurements and compared with the calculated Leti-UTSOI2 counterparts as a first model validation step. This allows a quick sanity check of the Leti-UTSOI2 extracted parameters, and a verification of the consistency between the equivalent circuit parameters and Leti-UTSOI2 parameters. The equivalent circuit parameters are extracted using two measurement sets and compared:

- The $I_D$-$V_G$ and $I_D$-$V_D$ characteristics derivatives are used to extract the transconductances $g_{m1}$ and $g_{m2}$ as well as the conductance $g_{ds}$, and C-V measurements are used to extract the required capacitances.

- The S-parameters measurements discussed in Chapter 4 are de-embedded and transformed into Y-parameters before parameters extraction using the simple analytical expressions summarized in Table 4-1.

The comparison between the two last characterization sets helps to validate the measurements and to assess the dynamic operation through basic model parameters. In particular the transconductance is compared based on DC (i.e. derivative if I-V characteristic) and S-parameters measurements (i.e. real part of $Y_{21}$-$Y_{12}$ at low frequency).

### 2.3.3 DC and low frequency characterization

DC and C-V operations accuracy is a prerequisite for analog and RF modeling. All model parameters are extracted based on dedicated structures and following pre-defined flows. Two different structures are characterized in this work. First, the simple DC structures generally adapted to digital or low frequency analog applications. An example of this type of structures is shown in Fig. 2.22. These simple structures are used for scalable core model extraction. Several other variants of this type of structures are adapted to extract advanced effects such as mismatch, STI stress, and Well-Proximity effect (WPE). The other type of structures (usually called RF structures) is dedicated to high frequency characterization using scattering parameters (S-parameters) measurement. This type of structures is depicted in Fig. 2.23, where multiple fingers are used to increase the device width (bias current) and optimize the dynamic behavior without degrading the gate resistance, which is detrimental at high frequency operation. These structures are optimized to have higher gain and higher transit frequency at the cost of increased footprint and layout complexity.

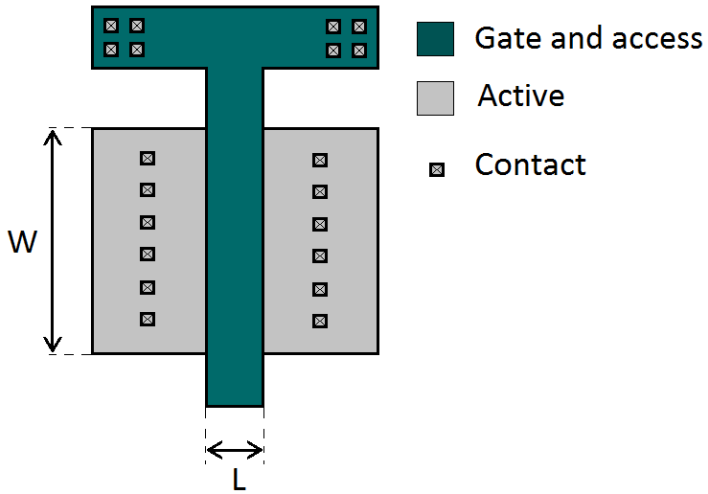



Fig. 2.22 DC structure illustration.

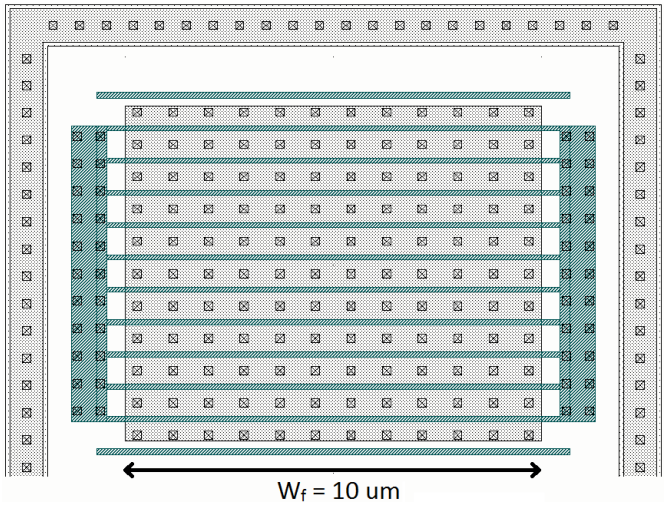



Fig. 2.23 RF multi-finger structure with a finger length of $W_f$ = 10 µm.

I-V measurement and characterization is done on both aforementioned types of structures (i.e. DC structures and RF structures). In our work, external connections related resistances (series resistances) are extracted before proceeding to a standard extraction flow similar to the one described in [98]. The advantage of the I-V characterization using RF structures is the availability of SHORT structures to extract series resistances. We propose to extract parasitic series resistances using both DC and S-parameters measurements of the dedicated RF “SHORT” structures shown in Fig. 4.2. The SHORT structure represents the measured Device Under Test (DUT) where gate, drain and common source and back gate are all shorted. The SHORT equivalent small signal circuit is implemented as illustrated in Fig. 2.24 (top) and corresponding resistances are optimized using measured data: the series DC resistors (Rg_ext, Rd_ext, and Rsb_ext) are encountered during DC measurements. Series HF resistors (Rg_hf, Rd_hf, and Rsb_hf) are encountered during DC & S-parameters measurements. Finally, shunt high capacitances (C = 1 F) are used to short the DC resistors in high frequency simulations. An illustration of the performed optimization is given in Fig. 2.24 (bottom) where input and output currents, respectively, $I_G$ and $I_D$ are plot with respect to input voltage $V_G$ for several output voltages $V_D$ ranging from -50 mV to 50 mV.

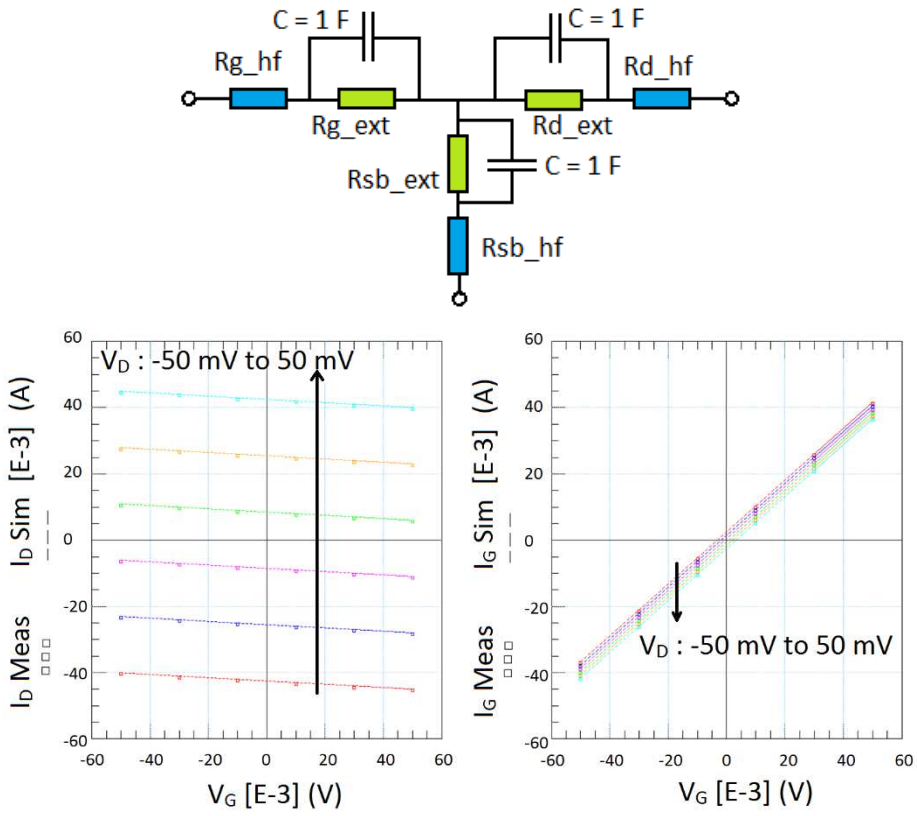
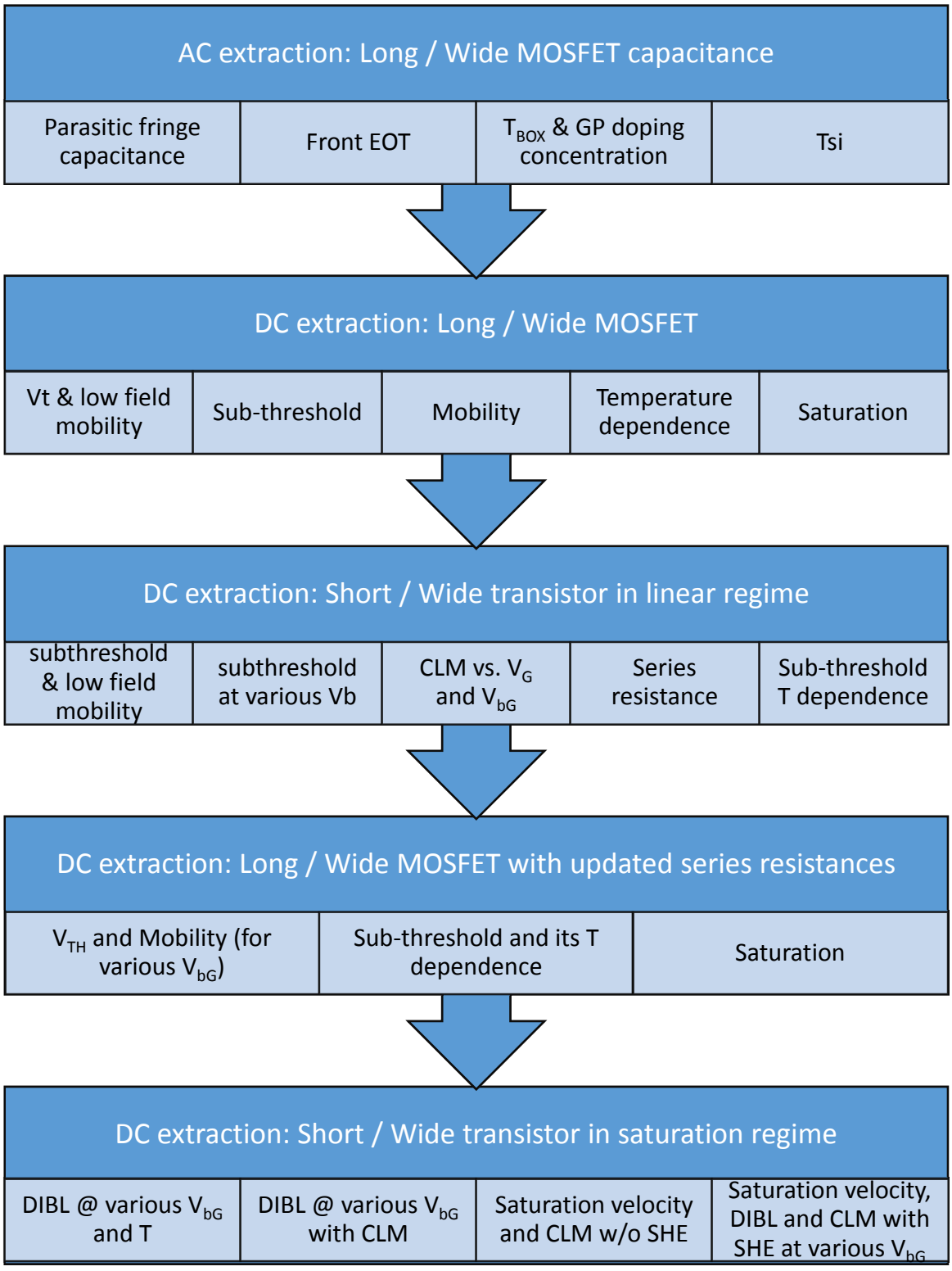



Fig. 2.24 (Top) SHORT structure equivalent schematic used to extract parasitic external resistances Rg_ext, Rd_ext and Rsb_ext (gate, drain and common source and back gate terminals series resistances respectively, source and back gate being shorted). (Bottom) an illustration of the performed optimization.

Several gate lengths and widths are measured and used for DC parameters extraction purpose. Long and wide structures are first used to extract main model parameters such as front oxide and BOX thicknesses, gates work-functions, effective and saturated mobility parameters and gate leakage. Short and narrow devices are then used to extract small geometry effects parameters. The minimal characterized MOSFET length and width are respectively 28 nm and 80 nm.

In saturation, the model fine tuning requires an estimate of the structure environment thermal resistance in order to account for the self-heating effects that is inevitable in DC operation besides its low effect in comparison to classical SOI technologies. A summary diagram of the proposed extraction steps for DC and AC is given in Table 2-2. Some of the listed steps (i.e. related to long channel) are executed twice to take into account the interaction between the several effects such as the impact of the series resistance on the mobility. Low field mobility is extracted using

Table 2-2 Summary of the extraction steps.




both $\log(I_D(V_{GS}))$ and $I_D(V_{GS})$ in non-saturation mode and refined using $g_m$ and $g_m$ derivative with respect to $V_{GS}$.

### 2.3.4 Normalization

In the following Section, when convenient, measured and simulated quantities are normalized as described in Table 2-3, unless otherwise stated.

Table 2-3 Normalization.

| Quantity | Normalization |
|---|---|
| Drain Current | $I_d = I_D/(I_{spec}.W/L)$ |
| Capacitance | $C/(C_{ox}.W.L)$ |
| Gate Voltage | Overdrive: $V_{gt} = (V_{GS} - V_{TH})$ |
| Transconductance | $g_m = G_m .U_T/(I_{spec}.W/L)$ |
| Transconductance derivative | $g_{m2} = G_{m2}.U_T^2/(I_{spec}.W/L)$ |
| Conductance | $g_{ds} = G_{ds}.U_T/(I_{spec}.W/L)$ |
| Conductance derivative | $g_{ds2} = G_{ds2}.U_T^2/(I_{spec}.W/L)$ |

where W is the total width ($W = N_f.W_f$), $W_f$ is a one finger length, $C_{ox}$ is the front oxide capacitance per unit area, $V_{TH}$ is the threshold voltage, TYPE is 1 for NMOS and -1 for PMOS, and $V_{gt}$ is the gate voltage overdrive. $I_{spec}$ is a technology current extracted in Chapter 3 and equal, for the front gate, to $I_1 \approx 0.7$ µA.

The validation of the extracted models is achieved through the comparison between the simulated MOSFET characteristics, and the measured counterparts. As stated earlier, several geometries and structures are characterized to validate the model scalability and all physical effects listed in Table C. 1. However, for an illustration purpose, only some geometries are shown in this document.

## 2.4 I-V and C-V operations assessment

The DC and C-V operation is compared against measurements of short and long (L = 30 nm and 2 µm respectively) NMOS and PMOS devices. To be consistent with RF operation assessment, multi-finger structures are used. When convenient, such as in the case of capacitances plots, NMOS convention gate voltage overdrive $V_{gt} = TYPE.(V_{GS} – V_{TH})$ is used.

### 2.4.1 I-V operation assessment

Accurate transfer characteristic $I_D$-$V_{GS}$ simulation is a critical condition for rigorous analog and RF modeling. Not only is the drain current accuracy required but also its first (transconductance) and second derivatives to estimate parasitic signal distortions in RF operation. Fig. 2.25 shows the transfer characteristic for NMOS and PMOS considering short and long channels. The normalized drain current in logarithmic scale is convenient to capture weak and moderate inversion behaviors while the linear scale highlights the strong inversion region as shown in Fig. 2.26. Subthreshold slope is accurately captured in weak inversion for both long and short channels. In strong inversion, series resistance impact, length modulation as well as mobility saturation effects (noticeable even at low $|V_{DS}|$) are correctly reproduced. Model is also correctly describing the complex moderate inversion region.

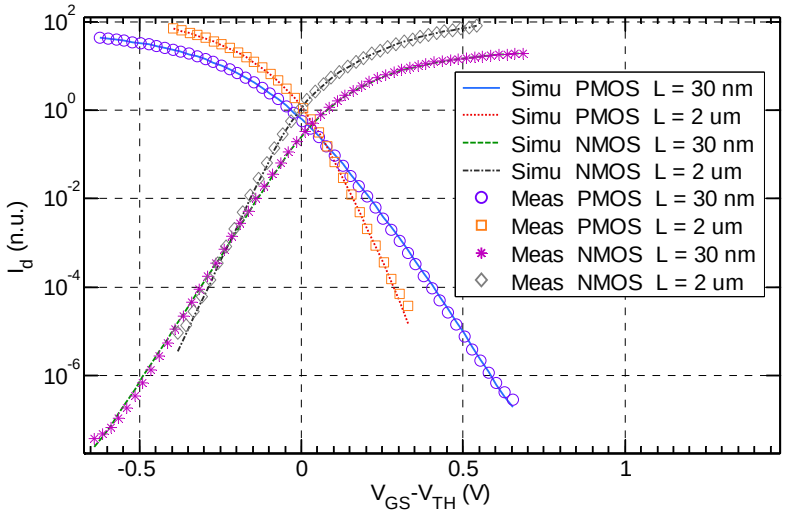



Fig. 2.25 Normalized drain current $I_d$ vs. gate voltage overdrive in linear operation $|V_{DS}|$ = 0.3 V for two NMOS and PMOS lengths (L = 30 nm and 2 µm), $W_f$ = 2 µm and $N_f$ = 10 at T = 25°C.

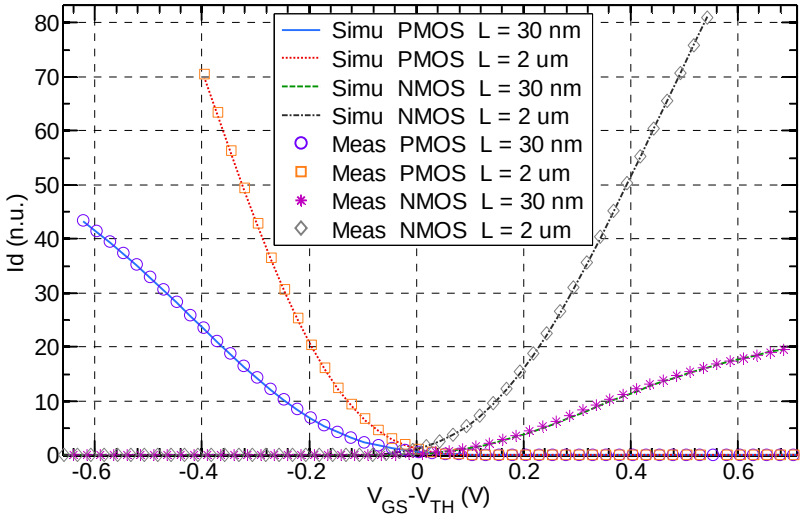



Fig. 2.26 Normalized drain current $I_d$ vs. $V_{GS}$ - $V_{TH}$ in linear operation $|V_{DS}|$ = 0.3 V for two NMOS and PMOS lengths (L = 30 nm and 2 µm), $W_f$ = 2 µm and $N_f$ = 10 at T = 25°C.

Normalized transconductance $g_m$ is shown in logarithmic and linear scales in Fig. 2.27 and Fig. 2.28 (left), respectively. In Fig. 2.28 (right), the second order derivative of the current is shown vs. overdrive voltage (in linear scale) for short and long channel NMOS and PMOS. An excellent matching with the measured transconductance and its derivative in weak, moderate and strong inversion is observed.

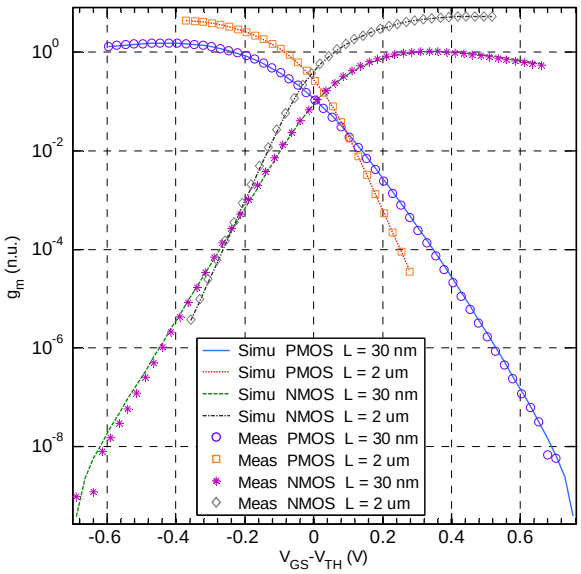



Fig. 2.27 Normalized transconductance vs. overdrive $V_{GS} – V_{TH}$ in linear operation $|V_{DS}|$ = 0.3 V for two NMOS and PMOS lengths (L = 30 nm and 2 µm), $W_f$ = 2 µm and $N_f$ = 10 at T = 25°C.

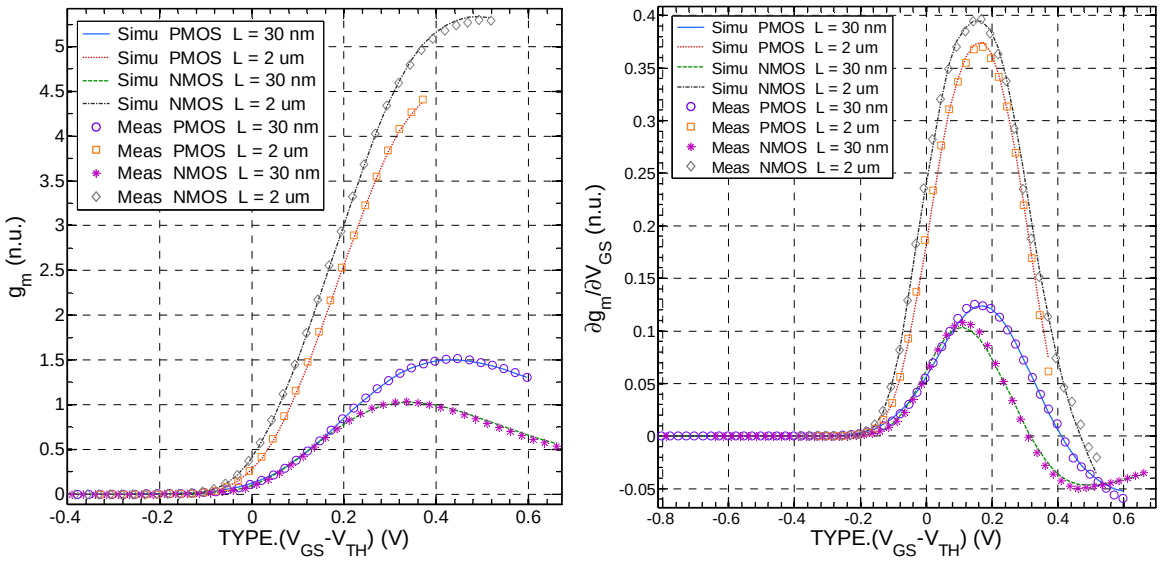



Fig. 2.28 Normalized transconductance (left) and its derivative (right) vs. gate overdrive in linear operation $|V_{DS}|$ = 0.3 V for two NMOS and PMOS lengths (L = 30 nm and 2 µm), $W_f$ = 2 µm and $N_f$ = 10 at T = 25°C.

In Appendix D, more model and measurement correlation results are shown. For instance, the dependence of the input characteristic on drain to source voltage $V_{DS}$ is validated for long and short channels. All characteristics are accurately predicted for all levels of inversion from WI to SI. In particular, DIBL effects are accurately captured in WI and higher current derivatives are also correctly reproduced. The DC quasi-static nonlinearities are decently captured and this is important for analog and high frequency operation. Moreover, the output characteristic and its dependence on gate to source voltage $V_{GS}$ are also accurately reproduced including conductance derivative for long and short devices from WI to SI.

The normalized transconductance efficiency FoM $g_m/I_D$ is depicted in Fig. 2.29 vs. the normalized drain current. This FoM is important for low-power analog and RF design [99]. Transconductance efficiency chart allows accurate hand calculation in all MOSFET inversion regions including moderate inversion that is complex to model and no analytical model is required. All the I-V based characteristics show model capability to accurately reproduce the UTBB FDSOI MOSFET DC behavior.

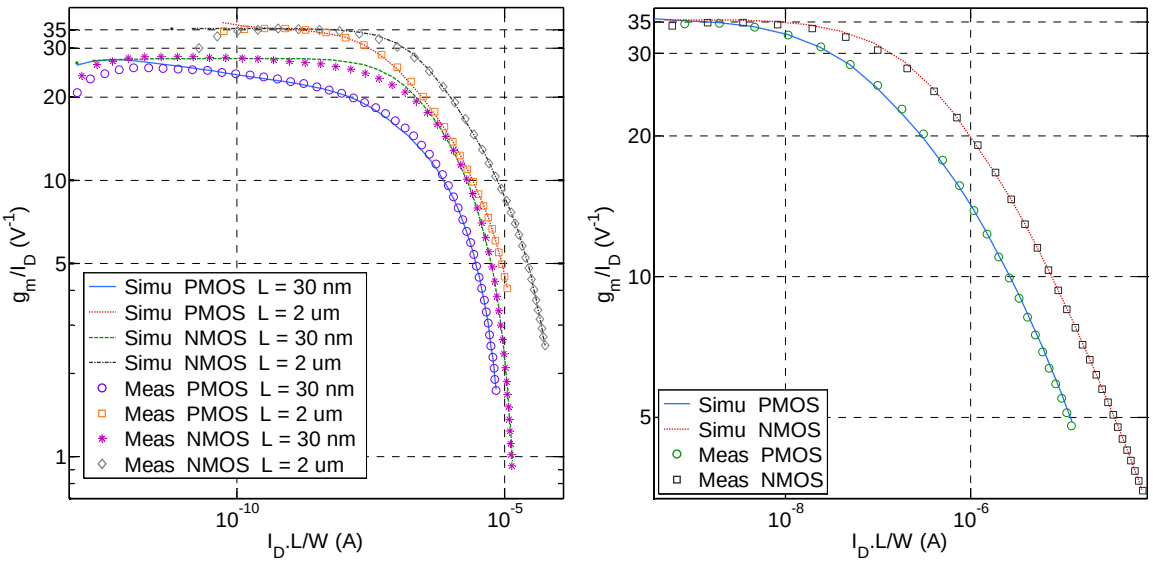



Fig. 2.29 Transconductance efficiency vs. normalized drain current $I_d = I_D.L/W$ in linear operation $|V_{DS}| = 0.3$ V for NMOS and PMOS (L = 30 nm, $W_f = 2$ µm and $N_f = 10$ at T = 25°C) (left). Same for NMOS and PMOS with L = 2 µm in saturation is given (right).

## 2.4.2 C-V operation assessment

For accurate low-voltage analog and RF modeling, MOSFET capacitances should be predicted in all operating conditions including moderate and weak inversion regions. In Fig. 2.30 and Fig. 2.31 normalized total gate capacitance $C_{gg}$ and gate to drain capacitance $C_{gd}$ are displayed vs. gate voltage overdrive at $|V_D| = 0.3$ V and source and back gate terminals grounded. $C_{gg}$ and $C_{gd}$ capacitances are correctly captured despite possible strong fringing capacitances impact.

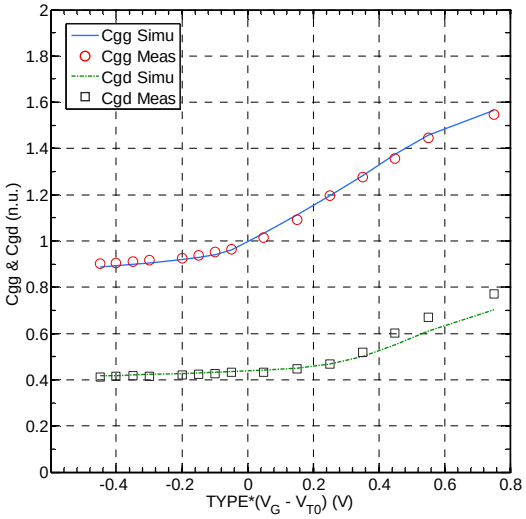



Fig. 2.30 Normalized $C_{gg}$ and $C_{gd}$ vs. gate voltage overdrive TYPE.($V_G$ – $V_{TH}$) in linear mode $|V_D|$ = 0.3 V for NMOS (L = 30 nm, $W_f$ = 2 µm and $N_f$ = 10) at T = 25°C and frequency = 100 MHz.

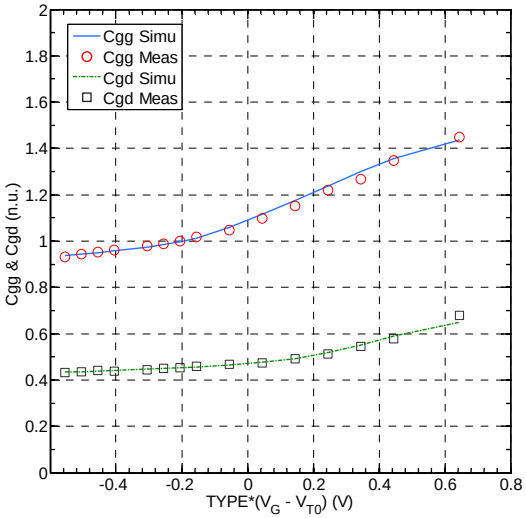



Fig. 2.31 Normalized $C_{gg}$ and $C_{gd}$ vs. gate voltage overdrive TYPE.($V_G$ – $V_{TH}$) in linear mode $|V_D|$ = 0.3 V for PMOS (L = 30 nm, $W_f$ = 2 µm and $N_f$ = 10) at T = 25°C and frequency = 100 MHz.

### 2.4.3 Dynamic operation assessment using UTSOI2 and the equivalent circuit

Using I-V and C-V measurements, quasi-static parameters are extracted separately for the small signal equivalent circuit model proposed in Fig. 2.18 and for the UTSOI2 model following the proposed flow in Table 2-2. Both models are simulated over a wide frequency range from 100MHz up to 500 GHz and compared. In Fig. 2.32 and Fig. 2.33, simulated S-parameters of a 1 µm NMOS are shown respectively in a

Smith chart and polar chart. The S-parameters are converted into Y-parameters and shown in Fig. 2.34 with respect to frequency. Both the proposed equivalent circuit and UTSOI2 provided comparable results. Considering the quasi-static assumption, both models are equivalent provided that intrinsic and extrinsic elements are extracted and accurately accounted for. The equivalent circuit parameters can be retrieved using measurements and can also be predicted using invariant charts that will be assessed in next Chapters. The comparison of the simulation of both equivalent circuit and UTSOI2 models to measured data shows a huge discrepancy at high frequency as discussed in the following.

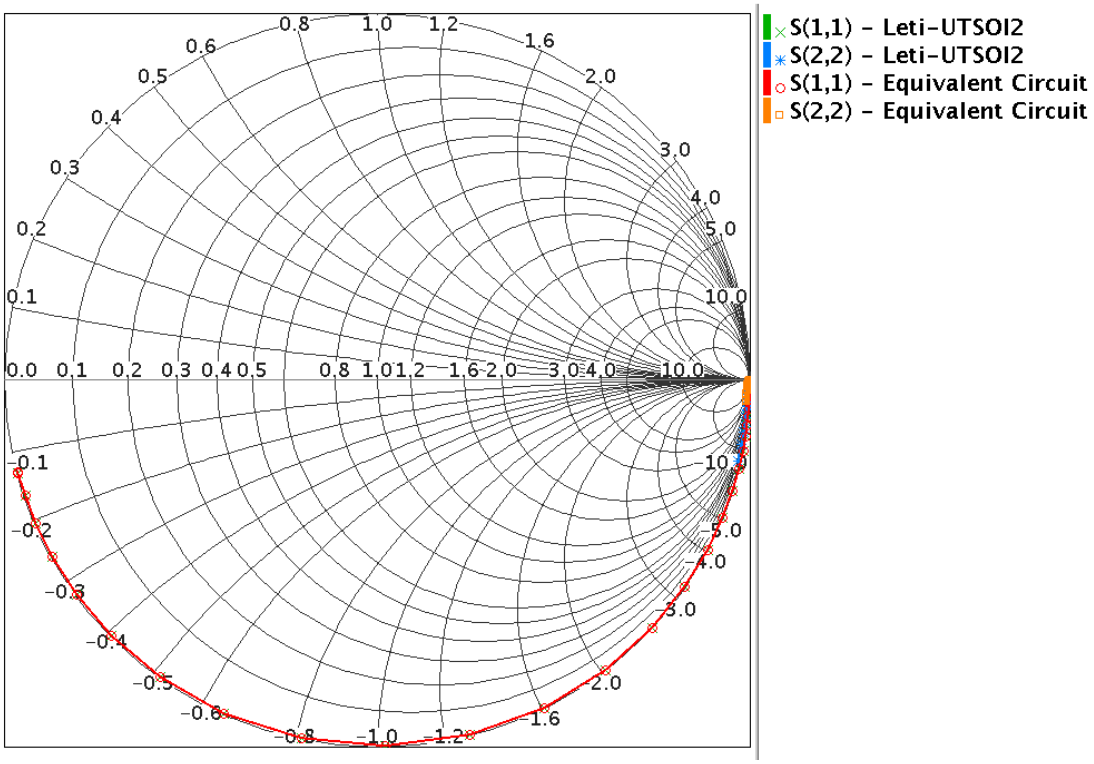



Fig. 2.32 Smith chart showing the input and output S-parameters simulated using the proposed equivalent circuit in Fig. 2.18 and the Leti-UTSOI2 of L = 1 µm NMOS in saturation ($V_{DS}$ = 1 V).

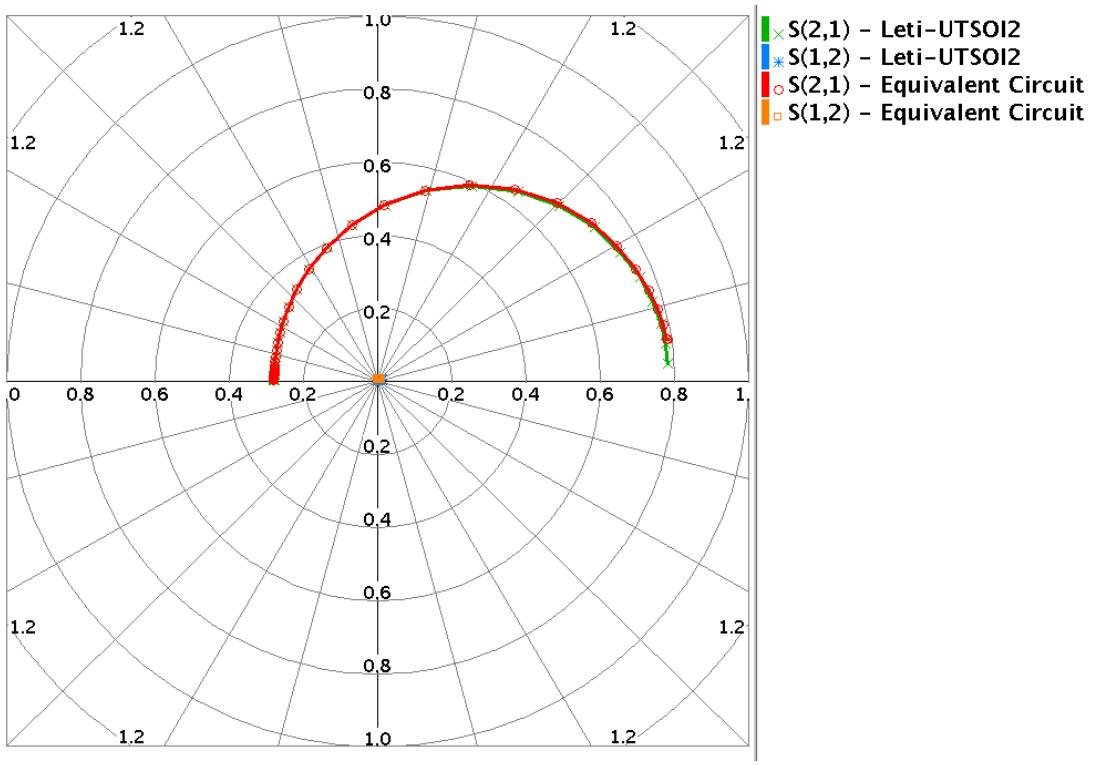



Fig. 2.33 Polar chart showing the input to output and output to input S-parameters simulated using the proposed equivalent circuit in Fig. 2.18 and the Leti-UTSOI2 of L = 1 µm NMOS in saturation ($V_{DS}$ = 1 V).

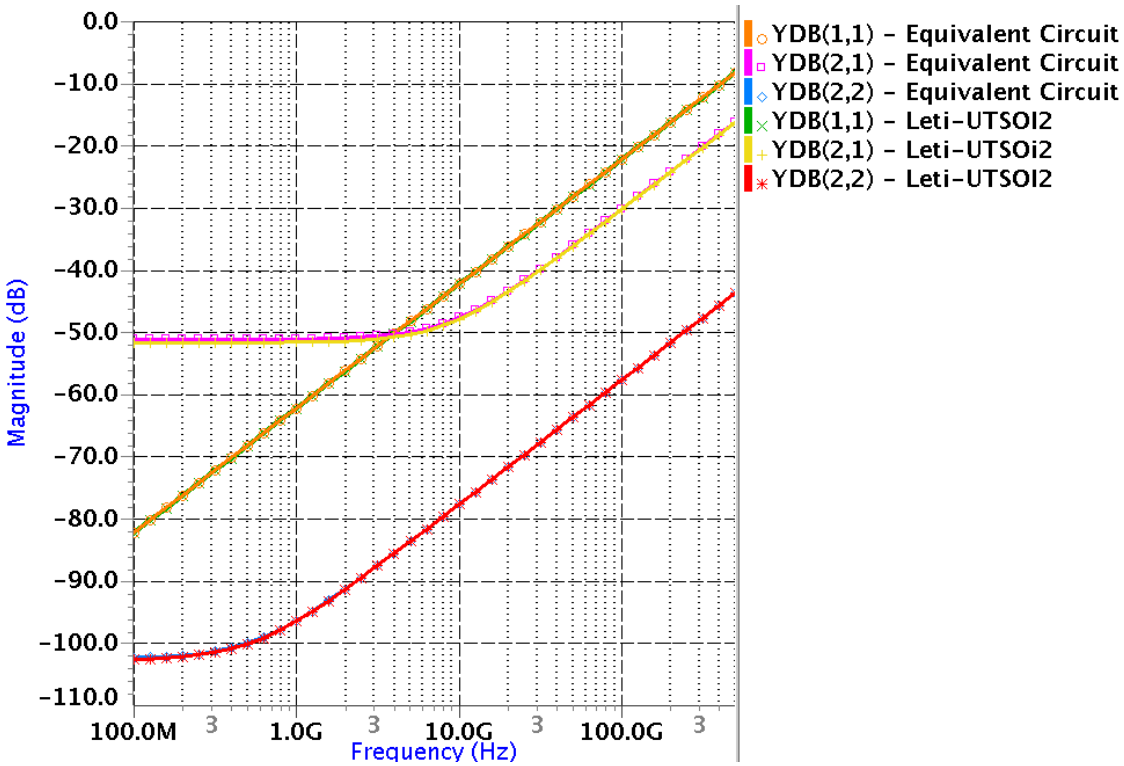



Fig. 2.34 Y-parameters simulated using the proposed equivalent circuit in Fig. 2.18 and the Leti-UTSOI2 of L = 1 µm NMOS in saturation ($V_{DS}$ = 1 V).

The DC and low frequency models are used to assess the high frequency behavior through Y-parameters. An equivalent of the transconductance at high frequency is the mutual transadmittance defined as:

$$y_m = Y_{21} - Y_{12} \tag{2.31}$$

where $Y_{21}$ and $Y_{12}$ are respectively the gate to drain transadmittance and the drain to gate transadmittance. At low frequency, the imaginary part of the complex $y_m$ tends to zero. Consequently, the modulus or the real part of $y_m$ is equal to the transconductance $g_m$ at low frequency. Fig. 2.35 shows the measured mutual transadmittance for a long channel MOSFET compared with the quasi-static UTSOI2 model simulations, which provides same results as the proposed equivalent circuit. Both models are clearly valid only up to 1 GHz and do not reproduce the performance degradation (i.e. 'transconductance' decrease) at high frequency.

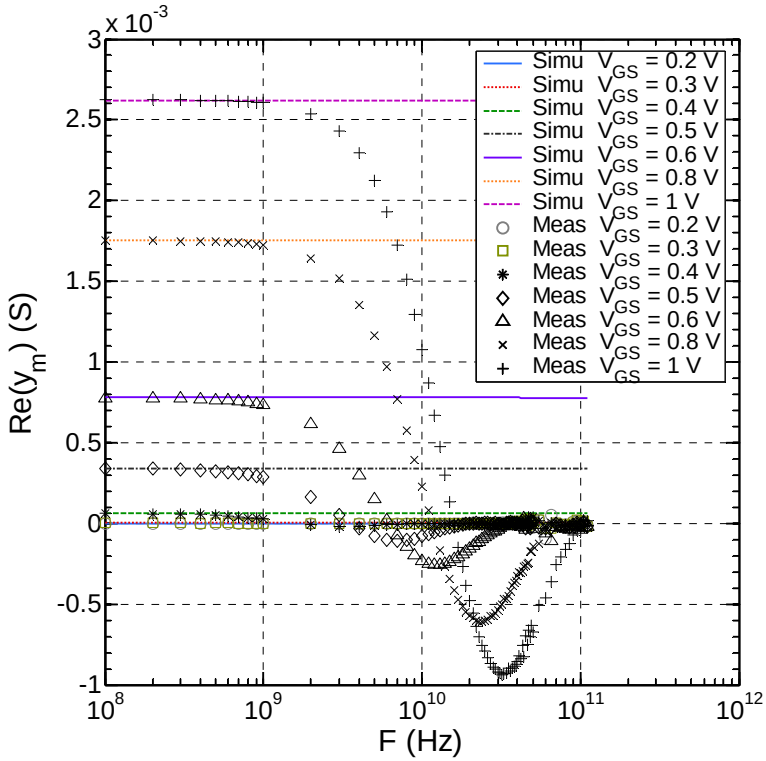



Fig. 2.35 The real part of the measured and simulated mutual transadmittance $y_m$ of a long channel L = 1 µm for various gate to source voltages from WI to SI in saturation ($V_{DS}$ = 1 V)

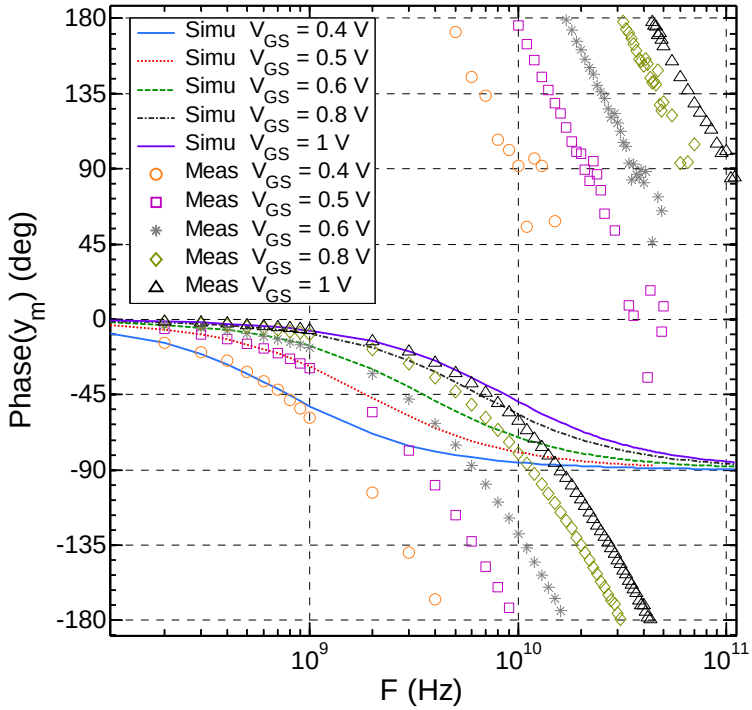



Fig. 2.36 The phase of the measured and simulated mutual transadmittance $y_m$ of a long channel L = 1 µm for various gate to source voltages from WI to SI in saturation ($V_{DS}$ = 1 V)

Measurements show negative real part of the transadmittance at high frequency, which means that the phase shift is greater than 90°. This is confirmed in Fig. 2.36 where $y_m$ phase is shown versus frequency. The quasi-static model is valid up to 1 GHz for $V_{GS}$ = 0.4 V (i.e. IC = 0.3) and up to 8 GHz for $V_{GS}$ = 1 V (i.e. IC = 109). The simulated phase tends to -90° for WI and SI while measurements show a clear antiphase phenomena. An enhancement of the model will be proposed in Chapter 4 for high frequency operation.

## 2.5 Operating point information

Operating Point (OP) information is a set of parameters usually provided by SPICE simulators describing a device in steady-state condition. For a MOSFET, the information represents the unique equilibrium state at which the transistor settles when related bias conditions (i.e. DC voltages or currents) are held constant. The OP information is including terminal voltages and currents as well as small signal low frequency parameters (e.g. $g_m$, $g_{ds}$, $C_{gd}$ and $C_{gs}$). The DC OP analysis is an intermediate step towards further simulator analysis (e.g. AC, Transient, and Noise).

The DC OP information is used by analog designers for sizing purposes, in particular to know the state of the transistor and its operation regime. The feature is convenient in providing quickly the required information within the circuit context, without the need for characterizing the device separately. The OP Info feature was proposed in early SPICE simulators and has not changed since.

### 2.5.1 OP information inaccuracy for sub-circuit based MOSFETs

In this Section, we will present our proposal to enhance the simulators DC OP information feature. This proposal is already adopted by major EDA vendors.

Today, in a DC simulation, the OP information provided by circuit simulators only represents elementary components (i.e. intrinsic or core MOSFET, parasitic resistors and capacitors, etc.) separately. As the majority of RF MOSFET models are implemented using sub-circuits with various elements, almost no accurate information is retrieved for such complex RF devices based on simulators outputs. Moreover, simulators provide some parameters such as $C_{gs}$ broken down into its components (i.e. overlap capacitance, fringe capacitance, etc.). For bulk PSP standard model for instance, simulators provide more than 200 parameters as the OP information while executing a simple operating point analysis. The majority of these parameters are useless for analog designers and most likely important for model developers. Therefore, designers run separate simulations to extract reliable information regarding steady-state conditions while working with RF MOSFETs. These attempts to find accurate OP information most likely distract designers from their design job.

Fig. 2.37 shows a simplified sub-circuit example of a RF MOSFET device with an external front gate resistor, series source and drain resistors and extrinsic capacitors. If DC $V_{GS}$ and $V_{DS}$ voltages are applied to the gate and drain terminals respectively while source and bulk or back gate are grounded, SPICE simulator provides OP information regarding all sub-circuit components separately (i.e. $C_{gs}$ and $V_{TH}$ of MOSFET M1, $R_S$, $C_{gse}$, etc.). The voltage drop between the internal MOSFET terminals $G_i$ and $S_i$ is different from the real $V_{GS}$ applied to the device. Thus, the threshold voltage provided by existing simulators for $M_1$ at the given $V_{DS}$ voltage is not accurate. Moreover, the $C_{gs}$ capacitance of the real device is not retrieved by a sum of

the intrinsic and the extrinsic capacitance, as the $R_s$ resistor is separating the two capacitors even at low frequency. Fig. 2.38 shows an example of comparison between the DC OP information $C_{gs}$ provided by major SPICE simulators (namely ELDO from Mentor Graphics, SPECTRE from Cadence, HSPICE from Synopsys, and ADS from Keysight), compared to the extracted one using AC simulations and taking the imaginary part of the impedenace. If the device is biased in same conditions within a circuit, the impedance between the gate and source terminals will have an imaginary part equal to the extracted values, and using the simulators information the designer is misled.

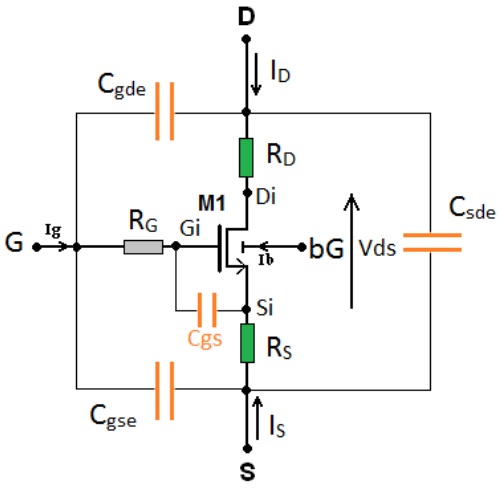



Fig. 2.37 A sub-circuit example of a RF MOSFET (B instead of bG in bulk).

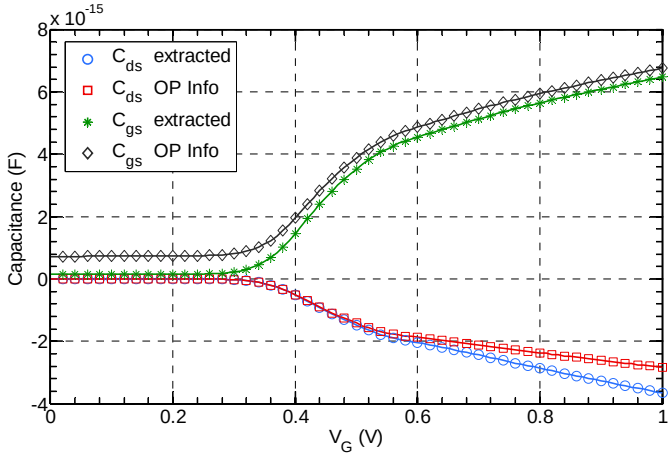



Fig. 2.38 Comparison of OP Info capacitances and extracted counterparts in saturation $V_{DS}$=1V for NMOS (L = 1 µm and W = 0.5 µm).

We propose a practical solution in the simulator side for all MOSFET types in such a way that the standard elementary information is replaced by the accurate equivalent one.

### 2.5.2 Enhancement proposal

We have worked on a proposal to help the simulator retrieve the required information for real devices. This solution is also used in our work to quickly assess high frequency MOSFET FoMs while simulating a Low Noise Amplifier (LNA) circuit (c.f Chapter 6).

A survey of various design groups within STMicroelectronics was carried out in order to define the required information for analog design. We came out with a specification, which is proposed to CMC for standardization. The proposed list is shown in Table 2-4, and includes a restricted set of MOSFET FoMs. This specification can be applied to various existing logic and analog MOSFETs with 4 terminals (i.e. a source, a drain, a front gate, and a back gate or a bulk terminal) in several technologies (i.e. bulk, SOI, etc.). The NMOS convention is chosen to display PMOS related information (i.e. the $V_{TH}$ of a PMOS for instance is positive in SI and saturation when equivalent bias conditions provide a positive $V_{TH}$ for NMOS). The source and drain are determined based on $V_{DS}$ voltage sign as in bulk PSP model. All parameters include temperature effect and self-heating effect (DC thermal voltage part).

Table 2-4 Operating Point information restricted list proposal for analog design (B = bG).

| Name | Unit | Formulation | Description |
|---|---|---|---|
| Total currents | | | |
| $I_D$ | A | - | Total DC drain current:<br>- flowing into drain terminal for NMOS<br>- flowing out of drain terminal for PMOS |
| $I_G$ | A | - | Total DC gate current:<br>- flowing into gate terminal for NMOS<br>- flowing out of gate terminal for PMOS |
| $I_S$ | A | - | Total DC source current:<br>- flowing into source terminal for NMOS<br>- flowing out of source terminal for PMOS |
| $I_B$ | A | - | Total DC bulk current:<br>- flowing into bulk terminal for NMOS |

| | | | |
|---|---|---|---|
| | | | - flowing out of bulk terminal for PMOS |
| Applied DC voltages | | | |
| $V_{GS}$ | V | NMOS: $V_{GS} = V_G - V_S$<br>PMOS: $V_{GS} = V_S - V_G$ | External gate-source DC voltage (with NMOS convention) |
| $V_{DS}$ | V | NMOS: $V_{DS} = V_D - V_S$<br>PMOS: $V_{DS} = V_S - V_D$ | External drain-source DC voltage (with NMOS convention) |
| $V_{SB}$ | V | NMOS: $V_{SB} = Vs - V_B$<br>PMOS: $V_{SB} = V_B - V_S$ | External source-bulk DC voltage (with NMOS convention) |
| Transconductances & MOSFET Conductance | | | |
| $g_m$ | A/V | $\partial(I_D)/\partial(V_G)$ | DC transconductance |
| $g_{mb}$ | A/V | $\partial(I_D)/\partial(V_B)$ | DC bulk or back gate transconductance |
| $g_{ds}$ | A/V | $\partial(I_D)/\partial(V_D)$ | DC output conductance |
| MOSFET Transcapacitances | | | |
| $C_{gd}$ | F | $-\partial(Q_G)/\partial(V_D)$ | AC Gate-Drain transcapacitance, including overlap capacitances |
| $C_{gs}$ | F | $-\partial(Q_G)/\partial(V_S)$ | AC Gate-Source transcapacitance, including overlap capacitances |
| $C_{gb}$ | F | $-\partial(Q_G)/\partial(V_B)$ | AC Gate-Bulk transcapacitance |
| $C_{ds}$ | F | $-\partial(Q_D)/\partial(V_S)$ | AC Drain-Source transcapacitance |
| $C_{dg}$ | F | $-\partial(Q_D)/\partial(V_G)$ | AC Drain-Gate transcapacitance |
| $C_{db}$ | F | $-\partial(Q_D)/\partial(V_B)$ | AC Drain-Bulk transcapacitance |
| $C_{sd}$ | F | $-\partial(Q_S)/\partial(V_D)$ | AC Source-Drain transcapacitance |
| $C_{sg}$ | F | $-\partial(Q_S)/\partial(V_G)$ | AC Source-Gate transcapacitance |
| $C_{sb}$ | F | $-\partial(Q_S)/\partial(V_B)$ | AC Source-Bulk transcapacitance |
| $C_{bd}$ | F | $-\partial(Q_B)/\partial(V_D)$ | AC Bulk-Drain transcapacitance |
| $C_{bg}$ | F | $-\partial(Q_B)/\partial(V_G)$ | AC Bulk-Gate transcapacitance |
| $C_{bs}$ | F | $-\partial(Q_B)/\partial(V_S)$ | AC Bulk-Source transcapacitance |
| MOSFET Capacitances | | | |
| $C_{gg}$ | F | $\partial(Q_G)/\partial(V_G)$ | AC Gate capacitance (including overlap) |
| $C_{dd}$ | F | $\partial(Q_D)/\partial(V_D)$ | AC Drain capacitance |
| $C_{ss}$ | F | $\partial(Q_S)/\partial(V_S)$ | AC Source capacitance |
| $C_{bb}$ | F | $\partial(Q_B)/\partial(V_B)$ | AC Bulk capacitance |
| Derived parameters | | | |
| $V_{TH}$ | V | - | Threshold voltage: should represent $V_{GS}$ at the onset of strong inversion in the MOSFET channel taking into account self-heating. |
| $V_{TH\_drive}$ | V | $V_{GS} - V_{TH}$ | Effective gate drive voltage including back bias, drain bias effects and self-heating. |
| $V_{DSAT}$ | V | $2/ (g_m/I_D)$ | Drain saturation voltage |
| $V_{DSAT\_marg}$ | V | $V_{DS} - V_{DSAT}$ | $V_{DS}$ voltage margin |
| Self_gain | - | $g_m/g_{ds}$ | MOSFET self-gain |
| $R_{out}$ | Ohm | $1/g_{ds}$ | AC output resistance |
| $B_{eff}$ | A/(V*V) | $2*abs(I_D)/(V_{TH\_drive})^2$ | Gain factor in saturation |

| | | | |
|---|---|---|---|
| $f_T$ | Hz | $g_m/[2*\pi*C_{gg}]$ | Transit frequency or unity current gain frequency |
| $R_{gate}$ | Ohm | - | Total MOSFET gate resistance |
| Gmoverid | 1/V | $g_m/I_D$ | $g_m$ over $I_D$ |
| $V_{EARLY}$ | V | $abs(I_D)/g_{ds}$ | Equivalent Early voltage |
| Tk | K | - | MOSFET device temperature |
| Dtsh | K | - | MOSFET device temperature increase due to self-heating |
| $R_{source}$ | Ohm | - | MOSFET source series resistance |
| $R_{drain}$ | Ohm | - | MOSFET drain series resistance |

Having the specification of the OP information defined, the issues regarding sub-circuit based devices can be tackled conveniently. We propose to consider the sub-circuit device as a black box MOSFET with 4 terminals. The simulator isolates the device from its context (i.e. original circuit) and runs, in background, specific simulations on it, while keeping same bias conditions. Then, simulator provides the extracted FoMs (i.e. list of Table 2-4) as a replacement of the detailed classical FoMs in the same output files and formats.

The cost of the proposed solution is some additional simulation CPU time (tens of milliseconds per device). However, the feature is only required in analog circuits where only a few devices need to be sized and their OP information to be accurately known. Consequently, in classical analog circuits, the additional CPU time is negligible and acceptable as a cost for accurate OP information.

The background specific simulation involves DC and AC analysis types, and is run using the isolated device. The DC simulation is a simple sweep of $V_{GS}$ in order to extract the threshold voltage at a constant predefined current density. Three other $V_{TH}$ definitions are also used:

- $g_{m\_max}$ based method where a linear extrapolation on $I_D$-$V_{GS}$ characteristic from the maximum $g_m$ location is used.
- maximum $\delta C_{gs}/\delta V_{gs}$ based method originating from a unified charge-control MOSFET model [90].
- maximum $\delta(g_m/I_D)/\delta V_{gs}$ based method proposed in [91] for bulk case.

The small signal AC simulation, with an applied small signal having a unit magnitude, is run at a default low frequency of 100 kHz, which can be modified by the user. Four instances of the same device are used with a small signal applied on each terminal in order to retrieve the 16 capacitances, the conductance, and the transconductance. The corresponding formulations are:

$$C_{xy} = \frac{\partial Q_x}{\partial V_y} = \frac{Im(i_x)}{|v_y|} = Im(i_x), \;\; x \neq y$$
$$C_{xx} = -\frac{\partial Q_x}{\partial V_x} = -\frac{Im(i_x)}{|v_x|} = -Im(i_x), \;\; x = y \tag{2.32}$$

where $C_{xy}$ and $C_{xx}$ are, respectively, the transcapacitances between x and y terminals and capacitance at terminal x. $Im(i_x)$ is the imaginary part of the AC current at terminal x, and $v_y$ is the AC voltage applied at terminal y with a magnitude of 1.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = -\frac{real(i_d)}{|v_g|} = -real(i_d), \qquad AC\ applied\ to\ gate$$
$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = -\frac{real(i_d)}{|v_b|} = -real(i_d), \tag{2.33}$$
$$AC\ applied\ to\ bulk\ or\ back\ gate$$

where $V_{BS} = V_{bG}$ in the case of DG MOSFET.

$$g_{ds} = \frac{\partial I_D}{\partial V_{GS}} = -\frac{real(i_d)}{|v_d|} = -real(i_d), \qquad AC\ applied\ to\ drain \tag{2.34}$$

In SI, the saturation voltage is estimated using:

$$V_{DSATSI} = \frac{2}{\left(\frac{g_m}{I_D}\right)} \tag{2.35}$$

(2.35) is used to estimate $V_{DSAT}$ for two geometries L = 2 µm and L = 100 nm. The result is shown in Fig. 2.39 and Fig. 2.41, respectively. For the long channel with less velocity saturation (e.g. L = 2 µm), the expression provides close results in SI to the definition of $V_{DSAT}$ proposed by Leti-UTSOI2. This is also evidenced in Fig. 2.40 using

$I_D$-$V_{DS}$ output characteristic. For WI, the expression underestimates the $V_{DSAT}$, and a correction can be proposed in this region of operation:

$$V_{DSATWI} = \frac{3}{\left(\frac{g_m}{I_D}\right)} \approx 3U_T \tag{2.36}$$

For short channel (e.g. L = 100 nm), the proposed SI expression provides lower $V_{DSAT}$ values as shown in Fig. 2.41. However, the values provided by Leti-UTSOI2 are too high to be defined as a threshold for current saturation. Actually the current already saturated at the values provided by Leti-UTSOI2 as depicted in Fig. 2.42. Expression (2.35) provides acceptable values for onset of saturation region.

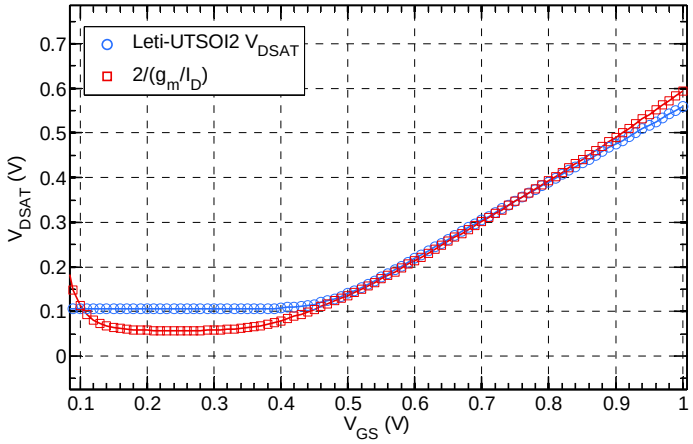



Fig. 2.39 Comparison of the Leti-UTSOI2 and $2/(g_m/I_D)$ expression $V_{DSAT}$ values versus $V_{GS}$ in saturation for NMOS and L = 2µm.

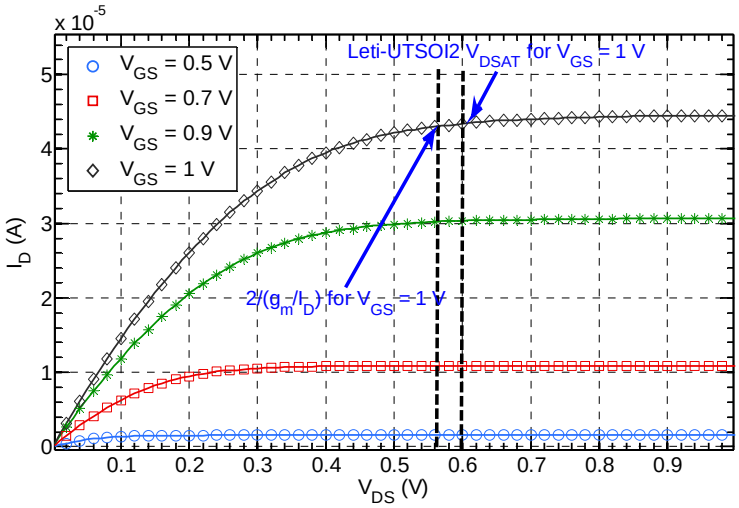



Fig. 2.40 $I_D$ – $V_{DS}$ characteristics for various $V_{GS}$ and L = 2 µm showing two $V_{DSAT}$ definitions (Leti-UTSOI2 and $2/(g_m/I_D)$ expression).

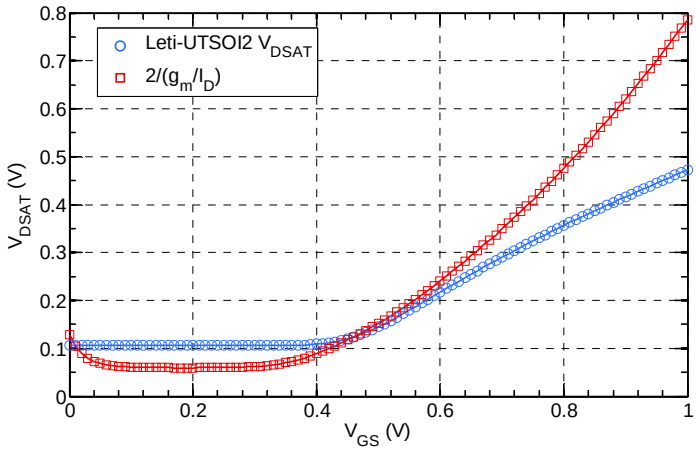



Fig. 2.41 Comparison of the Leti-UTSOI2 and $2/(g_m/I_D)$ expression $V_{DSAT}$ values versus $V_{GS}$ in saturation for NMOS and L = 100 nm.

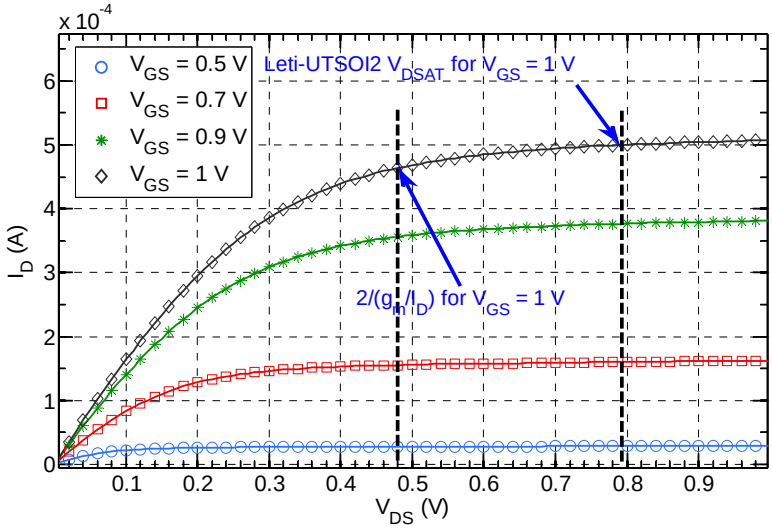



Fig. 2.42 $I_D$ – $V_{DS}$ characteristics for various $V_{GS}$ and for L = 100 nm showing two $V_{DSAT}$ definitions (Leti-UTSOI2 and $2/(g_m/I_D)$ expression).

## 2.6 Conclusion

The measured I-V and C-V characteristics of the UTBB FDSOI MOSFET have helped to gain more insight into the operation of an asymmetric double gate MOSFET. In particular, the impact of the back gate voltage on the threshold voltage is assessed using both characteristics. Volume inversion phenomena is evidenced using measurements and reproduced using TCAD simulations on a simple and optimized decks. The electrostatic behavior, assessed through C-V simulations, is reproduced accurately using both simple and optimized decks. However, the transport model (i.e.

mobility) is questionable as the invariance of the $g_m$ over $I_D$ characteristic is not reproduced using TCAD simulations. In the following, measurements will be our main reference and source of observation. TCAD simulations will be used carefully and compared with measurements.

The long channel I-V model of the UTBB FDSOI MOSFET showed deep similarities with bulk counterpart. In particular, the WI and SI trends are identical provided short channel effects are neglected. The DG MOSFET SI square law model, which is still in use in advanced technologies besides multiple limitations, is assessed through the threshold voltage parameter derivation for a long channel. The bulk square law model can be re-used provided that $V_{TH}$ dependence on $V_{bG}$ is correctly modeled. However, for production circuit simulation, the proposed charts in next Chapters and UTSOI2 model should be used as both account for all involved physical effects in a UTBB FDSOI MOSFET.

For small signal dynamic operation, a simple model is proposed for the core of the UTBB FDSOI MOSFET. The proposed model should be carefully used and the corresponding assumptions are verified.

In order to obtain the parameters of the small signal equivalent circuit or the UTSOI2 model, DC and low frequency characterization is carried out using DC and RF structures. RF structures along with the de-embeding structures are helpful to gain insight into the DC characterization as the series parasitics are extracted accurately and accounted for in the simulation.

The comparison between the extracted model and the measurements validates the capabilities of the model to accurately reproduce the DC and low frequency behavior of the UTBB FDSOI MOSFET. Both NMOS and PMOS are extracted and compared for several bias conditions with a focus on moderate inversion. Both UTSOI2 and the equivalent circuit based models are able to accurately capture the low frequency behavior over more than seven decades of current from WI to SI. However, the high frequency measured data are not captured at high frequency by both quasi-static models as shown in Fig. 2.35 and Fig. 2.36 because of non-quasi-static effects. A non-quasi-static model will be developed in Chapter 4.

The operating point information feature provided by the main SPICE simulators today is subject to several limitations that are discussed. In particular, the information provided to analog designers for advanced sub-circuit based RF models is inaccurate. The reason for this inaccuracy is the fact that all simulators rely on the information specified for individual lumped elements and ignore the complexity of parasitic aware models. An enhancement of this important feature has been proposed to the main EDA vendors, namely Mentor Graphics, Synopsys and Cadence, and is already implemented in recent simulators versions. Attempts to standardize the DC OP information are ongoing within CMC organization (DC OP Info subcommittee and PSP subcommittee).

# Chapter 3

# $g_m$ over $I_D$ invariance assessment

## 3.1 Introduction

Double gate fully depleted MOSFETs exhibit a large inherent immunity to short channel effects, a steeper subthreshold slope and a higher drive current [26]. The independent double gate architecture is further enlarging circuit design space as the two gates can be independently controlled. These advanced structures, as discussed in Chapter 1, are chosen to continue the aggressive CMOS technology down-scaling and demonstrate excellent digital and analog performances especially in low-power applications [10][14].

In recent low power and high performance circuits, it is crucial to operate MOSFET transistors all the way from weak to strong inversion levels [81]. Furthermore, moderate inversion region has been found to be a good compromise while power consumption and speed are valued equally [82][25][15]. To benefit from the full potential of recent technologies especially in deep weak and strong inversion, efficient analog first-cut designs still rely on hand calculations. The traditional hand calculations involve simplified MOSFET transistor models that are assumed to be valid in the weak and the strong inversion regimes.

Unfortunately, the usual strong and weak inversion approximations fail to predict drain current ($I_D$) in moderate inversion and there is no similar model that is simple enough for hand analysis and satisfactorily predictive in particular for multiple gate transistors [100][101]. The situation is becoming worse with advanced and down-scaled technologies where effective mobility, velocity saturation and series resistances are dominant at lower inversion levels. Consequently, the classical saturation and strong inversion approximation square law is only valid near to the onset of strong

inversion and inappropriate elsewhere. The transistors are therefore operated with less efficiency when traditional methods are used and this might lead to overdesign [102].

The above out-of-date hand calculations practices are preventing analog designers from taking full advantage of modern technologies (high transconductance efficiency and low $V_{DSAT}$). In order to address the weakness of the traditional procedures, where questionable concepts such as the early voltage, the gate voltage overdrive and the classical square law are used, the transconductance efficiency ($g_m/I_D$) based design methodology has been proposed [99]. The $g_m$ over $I_D$ approach relies on the fundamental and universal aspect of the transconductance efficiency versus normalized drain current curve in single gate MOSFETs. Such a plot is considered to be invariant regardless of threshold voltage and length considering short channel effects are negligible [99][103]. Should one be wary of taking the invariance assumption at face value while working with double gate MOSFETs?

The objective of this Chapter is to check the extent to which the $g_m$ over $I_D$ based design methodology referred to above is valid for advanced asymmetric double gate transistors such as the Fully Depleted SOI (FDSOI) Ultra-Thin Body and Box (UTBB) MOSFETs. The $g_m$ over $I_D$ design methodology is briefly explained in Section 3.2. In Section 3.3, TCAD simulations remind the back gate effect on the front gate transconductance efficiency already discussed in Chapter 2. The normalization of both transconductance efficiency and current for a double gate transistor is described in Section 3.4. In Section 3.5 the experimental setup is described and the transconductance efficiency versus the inversion coefficient (IC) chart invariance is assessed using obtained experimental data. Finally, a discussion on $g_m$ over $I_D$ invariance is presented in Section 3.6.

## 3.2 $g_m$ over $I_D$ based design methodology

The concept of transconductance efficiency ($g_m/I_D$) was introduced by Pullen [104] and used in the context of the EKV MOST model [105][106]. The low-power design methodology using $g_m$ over $I_D$ versus normalized drain current was first

demonstrated for an analog circuit design in [99]. The $g_m$ over $I_D$ analog design procedures were promoted by Binkley and other researchers since then [102][107].

$g_m/I_D$ is strongly related to analog circuits performances (e.g. common source amplifier gain is directly linked to $g_m/I_D$). It is also an indication of the device operating region as it is equal to the derivative $\partial \ln(I_D)/\partial V_G$ which is constant in weak inversion and decreasing in moderate inversion and strong inversion. Finally, $g_m/I_D$ vs. normalized DC drain current curve is a tool for transistor dimensions calculation.

Using $g_m$ over $I_D$ based charts, the methodology allows accurate hand calculations in all MOSFET inversion levels including moderate inversion that is complex to model. The transistor geometry ratio (W/L) is determined once two values of the triplet ($g_m/I_D$, $g_m$, $I_D$) are calculated. $I_D$, $g_m$ and Length are first chosen based on circuit design specifications (power consumption, higher gain or speed). In this first step, dedicated intrinsic gain and transit frequency versus normalized drain current charts with length as a parameter may be used as guides. Then $g_m$ over $I_D$ versus normalized drain current chart is used to determine the inversion level and calculate the required width. The $g_m/I_D$ vs. gate voltage overdrive $V_G$-$V_T$ curve is used to ensure MOSFET is in saturation.

The optimum inversion coefficient determined using recently proposed figure of merit $g_m.f_T/I_D$ can be used for an acceptable tradeoff between performance, power consumption, and speed [82][15]. The $g_m$ over $I_D$ methodology allows de facto the designer to consider level of inversion as an input rather than a consequence of the sizing.

## 3.3 Invariance unpredictability using TCAD

To assess the invariance of the transconductance efficiency versus normalized current chart, electrical $I_D$-$V_G$ and $C_{gg}$-$V_G$ characteristics have been first obtained using TCAD simulations based on constant mobility model. The simulated N-channel MOSFET device is an UTBB FDSOI MOSFET. Si body, BOX and equivalent gate oxide thicknesses are 7 nm, 25 nm and 1.3 nm, respectively. $I_D$-$V_G$ and $C_{gg}$-$V_G$ characteristics

are simulated in saturation for various back gate voltages $V_{bG}$ while source is grounded (all voltages in this Chapter are referred to the source). Fig. 3.1 shows the $g_{m1}/I_D$ as a function of the normalized drain current $I_D.L/W$ with back gate voltage $V_{bG}$ as a parameter ($g_{m1}$ is the front gate transconductance, W and L are width and length of the device respectively) and a focus on MI and SI. As current increases for high forward back gate voltage ($V_{bG}$ = 5 V), the back-channel inversion occurs first and results in a lower transconductance efficiency and lower subthreshold slope (i.e. higher “body effect”), corresponding to a lower equivalent front capacitance (front gate oxide capacitance in series with the silicon film capacitance). The transconductance efficiency for $V_{bG}$ = 5 V tends towards the $V_{bG}$ = 0 V curve at higher current (higher $V_G$) when the front channel inversion occurs. It should be noted that transconductance efficiency behavior at constant mobility is related to the $C_{gg}$ capacitance (electrostatic) shown in Fig. 3.2. Indeed, $C_{gg}$-$V_G$ curve at high forward back gate voltage $V_{bG}$ = 5 V reveals the two interfaces (back and front) activation corresponding to the two pronounced peaks of the $C_{gg}$ derivative (inset in Fig. 3.2). The $g_{m1}/I_D$ versus normalized drain current curves for $V_{bG}$ = 5 V and $V_{bG}$ = 0 V do not superpose (delta is greater than 15%) and hence TCAD simulations with constant mobility model do not unambiguously comfort/demonstrate the sought invariance for an asymmetric double gate MOSFET.

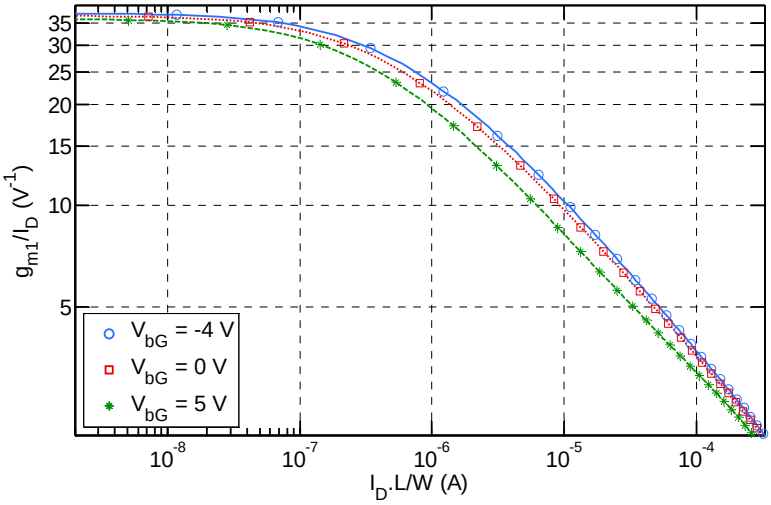



Fig. 3.1 $g_{m1}$ over $I_D$ versus normalized drain current ($I_D.L/W$) of NMOS (L = 1 µm) in saturation at $V_{bG}$ = {-4 V, 0 V, 5 V} and T = 25°C.

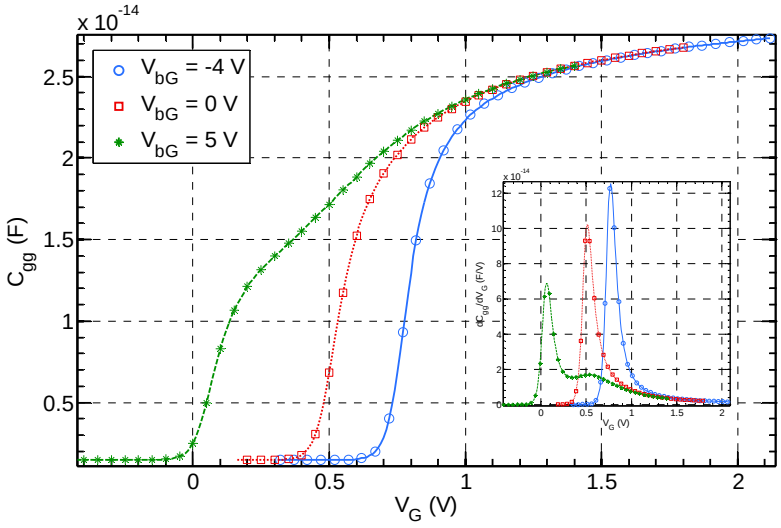



Fig. 3.2 Gate capacitance $C_{gg}$ versus front gate voltage $V_G$ of NMOS (L = 1 µm) in saturation at $V_{bG}$ = {-4 V, 0 V, 5 V} and T = 25 °C. Inset shows capacitance derivative $\partial C_{gg}/\partial V_G$.

To gain further insight into the special behavior of the $g_{m1}/I_D$ for a UTBB MOSFET, experimental data will be used in Section 3.5. The observed gradient mobility from front to back channel reported in [92][93] brings about additional ingredient to check out as $g_m/I_D$ is linked to both electrostatic and transport according to:

$$\frac{g_m}{I_D} = \frac{\partial \ln I_D}{\partial V_G} = \frac{1}{Q_{inv}}\frac{\partial Q_{inv}}{\partial V_G} + \frac{1}{v}\frac{\partial v}{\partial V_G} \tag{3.1}$$

where $Q_{inv}$ and $v$ are the mobile charge density and mobile velocity respectively. Moreover, the invariance demonstrated using the model proposed in [108] for the case of a symmetric DG MOSFET calls for a generalization to the asymmetric DG MOSFET studied here.

## 3.4 Transconductance efficiency and current normalizations

In this Chapter, the drain current is normalized to get an inversion coefficient (IC). The latter is defined as the square shape DC drain current $I_{\square}$ normalized by a technology current $I_i$ comparable to the process dependent current defined in [107]:

$$IC = \frac{I_{\square}}{I_i} = \frac{I_D/(W/L)}{I_i} \tag{3.2}$$

where $I_{\square}$ is the square shape drain current $I_D/(W/L)$, i = 1 for the front gate technology current and i = 2 for the back gate technology current. Indeed, two technology currents can be defined for an asymmetric double gate MOSFET. IC will be used as the x-axis of the normalized MOSFET transconductance efficiency plots presented in Section 3.5. The inversion coefficient concept was introduced by Vittoz [105] and used in EKV model context [106]. In the transconductance efficiency versus normalized current $I_{\square}$ chart, as depicted in Fig. 3.3, the technology current $I_i$ is located at the intersection of the weak inversion asymptote (Boltzmann limit) and the saturation strong inversion square law asymptote for a long MOSFET [105]. Inversion coefficient concept is helpful to easily identify the MOSFET operating level of inversion.

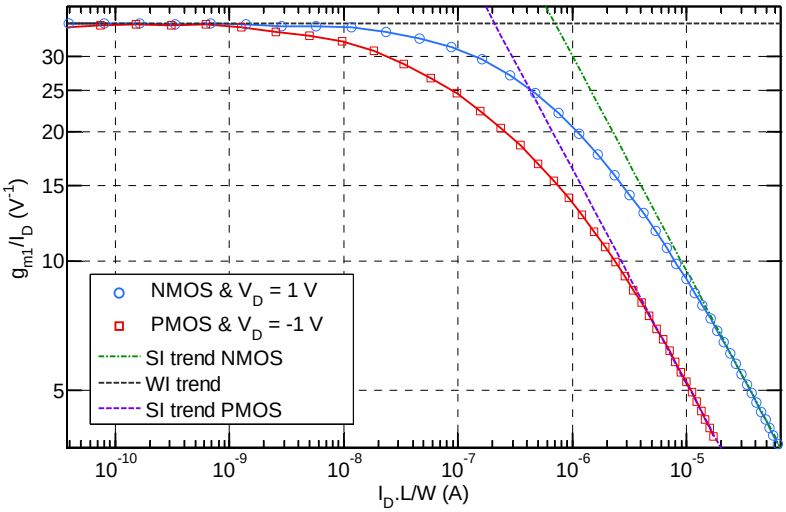



Fig. 3.3 Measured $g_{m1}$ over $I_D$ versus square shape drain current ($I_D$.L/W) of NMOS and PMOS (L = 1 µm) in saturation at $V_{bG}$ = 0 V and T = 25 °C.

An analytical expression for the technology current similar to the one given in [107] cannot straightforwardly be derived for a double gate MOSFET as mobility, subthreshold slope and gate capacitance vary significantly with front and back gate voltages. Indeed, as has been proposed in [96], the mobility is dependent on a coupling field, which in turn depends on front and back gate voltages. In the same model, the two ideality factors or namely front and back coupling factors $n_1$ and $n_2$ depend on the front or back channels activation. The explicit threshold based $I_D$ model considers two

inversion charges and a coupling charge associated to the coupling electrical field. An equivalent gate capacitance cannot be explicitly derived since two channels coexist. In [109] an equivalent gate capacitance is determined given the location of the effective conductive path, which in turn depends on front and back gate voltages. We propose to define an equivalent expression of the technology current which is related to both gates:

$$I_i = 2 \cdot \beta_i(V_G, V_{bG}) \cdot U_T^2 \tag{3.3}$$

where $\beta_i$ (i = 1 or i = 2) are two functions of both front and back gate voltages. In saturation and in the case of front channel inversion with back channel in weak inversion the $\beta_1$ becomes equal to $n_1.C_{ox1}.\mu_1$ provided that the front coupling factor $n_1$ in [96] is rather considered in strong inversion too. $C_{ox1}$ and $\mu_1$ are front oxide capacitance and front channel mobility respectively.

In asymmetric double gate transistors, two transconductance efficiencies can be defined according to the gate used for the input signal. Consequently, for a long channel, front and back transconductance efficiencies are normalized to their maximum values $1/(n_1.U_T)$ and $1/(n_2.U_T)$ respectively, which is reached in weak inversion. The analyzed figure of merit becomes: $FoM_i = n_i.U_T.g_{mi}/I_D$ where $g_{mi}$ is front or back transconductance. Although $g_m/I_D$ ratio reaches its maximum in deep weak inversion, the normalization factor (and consequently $n_i$ value) is extracted at a higher level of current just before the onset of the moderate inversion. $I_i$ is defined as the square shape current where the strong inversion asymptote and the weak inversion plateau intersect.

The normalization parameters for each gate $I_i$ and $n_i$ are taken to be intrinsic and unvarying constants for a MOSFET type. Consequently, the transconductance efficiency and $I_D$ can simply be obtained from the normalized charts by multiplying the corresponding normalized quantities (values on y-axis and x-axis) by $1/(n_i.U_T)$ and $I_i.(W/L)$ respectively.

## 3.5 Experimental results

This work was carried out using UTBB FDSOI MOSFETs implemented in a commercial 28 nm technology processed at STMicroelectronics. More details on the process can be found in [3]. The gate length and gate width of both measured N-channel and P-channel MOSFETs range from 28 nm to 4 µm and from 80 nm to 5 µm respectively. Drain current versus gate voltage $I_D$-$V_G$ curves are measured at different drain voltages $V_D$ (linear 50 mV to saturation 1 V), different back gate voltages $V_{bG}$ (from -4V to 5V) and different temperatures (-40 ºC, 0 ºC, 25 ºC, 80 ºC and 125 ºC).

As shown in Fig. 3.3, at a temperature of 25°C, the high subthreshold slope of the UTBB FDSOI transistors provides a maximum value of $g_{m1}/I_D$ of about 36 $V^{-1}$ for both NMOS and PMOS which corresponds to a near ideal subthreshold slope.

The extracted $n_1$ and $I_1$ values for long NMOS and PMOS in saturation with grounded back gate are given in Table 3-1. It should be noted that $I_1$ is not located in the center of the moderate inversion but rather in its upper part at one decade before the strong inversion region. The ratio of NMOS and PMOS technology currents compares to the ratio of electron and hole mobility. Both weak and strong inversion asymptotes overpredict transconductance efficiency at the technology current $I_1$ by more than 60%.

Table 3-1 $n_1$ factor and $I_1$ for N-MOSFET and P-MOSFET in saturation and at 25 ºC

| | $n_1$ | $I_1$ |
|---|---|---|
| NMOS | 1.086 | 7.028e-7 A |
| PMOS | 1.094 | 2.152e-7 A |

Following the normalization explained in the previous section, Fig. 3.4 shows the normalized $g_{m1}$ over $I_D$ as a function of the inversion coefficient IC. NMOS and PMOS curves overlap in strong and weak inversion regions while a maximum of 7% difference is encountered in moderate inversion as charge carriers nature influences mobility behavior mostly in this region. In the following Sections, we will analyze the dependence of the normalized $g_m/I_D$ versus inversion coefficient chart on transistor

back or opposite gate voltage, temperature, geometry, drain to source voltage and process variability.

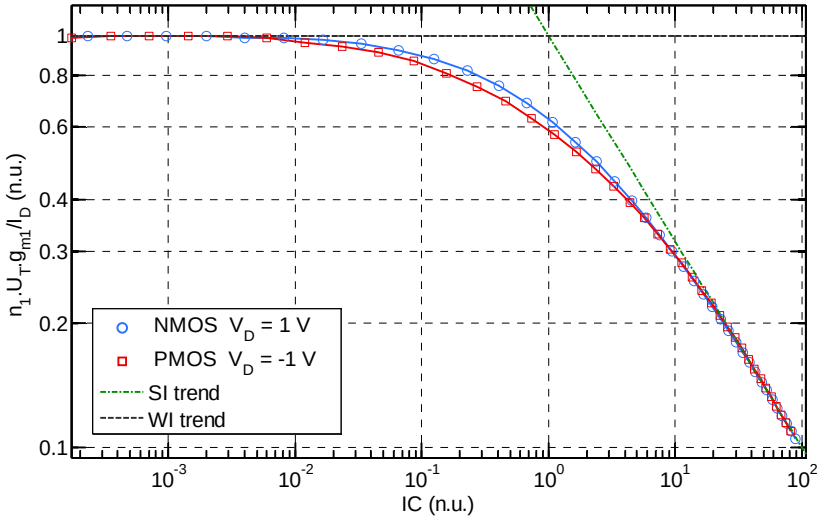



Fig. 3.4 Normalized transconductance efficiency versus IC of a NMOS and PMOS (L = 1 µm) in saturation at $V_{bG}$ = 0 V and T = 25 °C.

## 3.5.1 Back gate voltage impact

- **Front gate transconductance efficiency**

It is not evident at first sight that the universal aspect of the $g_{m1}/I_D$ versus IC chart should be somehow conserved when setting the back gate voltage at different values, i.e. could it be that the so called $g_m/I_D$ invariance will exhibit different shapes upon $V_{bG}$ as observed in TCAD simulations in Section 3.3. Fig. 3.5 shows normalized $g_{m1}$ over $I_D$ vs. inversion coefficient curves experimentally obtained with 1 µm-long FDSOI UTBB N type MOSFET under different back gate voltage conditions. Fig. 3.7 shows normalized $g_{m1}$ over $I_D$ vs. inversion coefficient curves experimentally obtained with 1 µm-long FDSOI UTBB P type MOSFET for various back gate voltages.

For long channel MOSFETs, the normalized $g_{m1}$ over $I_D$ behavior is within 6% from weak to strong inversion across the entire range of shown back gate voltage conditions (from -4 V to 5 V). Difference of non-zero back gate voltage cases versus the grounded back gate ($V_{bG}$ = 0 V) case for N type MOSFET are depicted in Fig. 3.6. Maximum transconductance efficiency is obtained for $V_{bG}$ = 2 V in Fig. 3.6 corresponding to a weak transverse field, or in other words to a pronounced volume

inversion shown in TCAD simulations in Fig. 1.4. This optimum condition takes place in the upper part of the moderate inversion region at IC = 4. Back gate voltage does not have great control on the volume inversion phenomena and consequently the front technology current does not vary too much. An error of less than 4 % is made in the prediction of the transconductance efficiency while assuming invariance over the wide back gate voltage range from -2 V to 2 V.

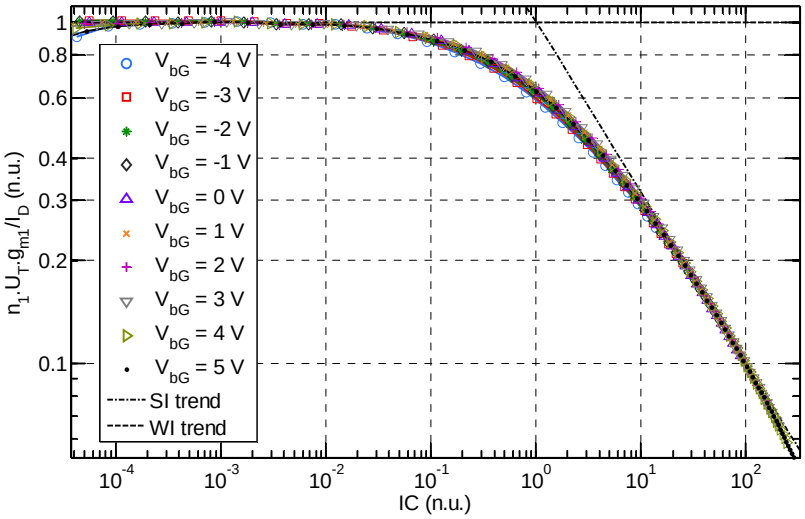



Fig. 3.5 Normalized $g_{m1}$ over $I_D$ as a function of the inversion coefficient at different $V_{bG}$ for NMOS (L = 1 µm & W = 1 µm) in saturation ($V_D$ = 1V) at T = 25 °C.

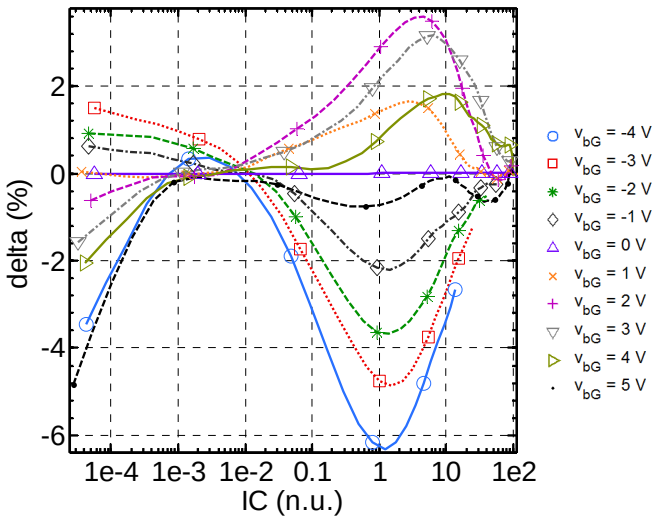



Fig. 3.6 Transconductance efficiency curves delta versus $V_{bG}$ = 0V curve.

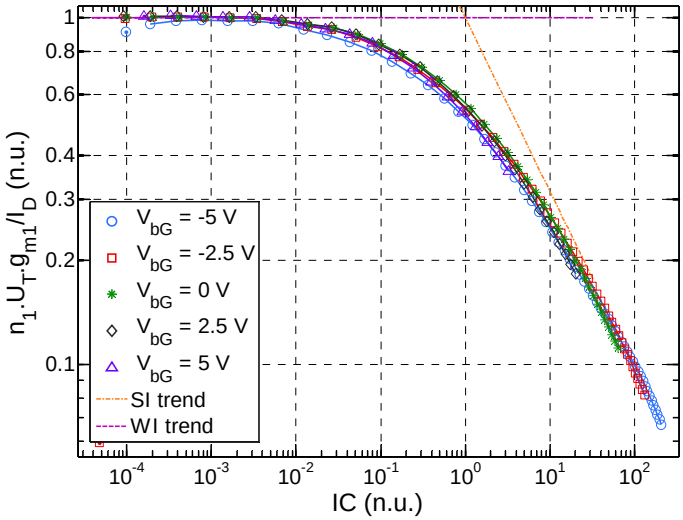



Fig. 3.7 Normalized $g_{m1}$ over $I_D$ as a function of the inversion coefficient at different $V_{bG}$ for PMOS (L = 1 µm & W = 1 µm) in saturation ($V_D$ = -1 V) at T = 25 °C

- **Back gate transconductance efficiency**

In addition to the current modulation from the front gate, which is the most 'regular' approach, the back gate transconductance efficiency ($g_{m2}/I_D$) for different front gate $V_G$ voltage conditions must also be analyzed since the IC concept should only depend on the current, independently how this current is generated, i.e. from the front or the back-gate voltage. This characteristic is shown in Fig. 3.8. In the case of front channel inversion with back channel in weak inversion (high front gate voltage), the extracted back gate slope factor is $n_2$ = 12.6 which agrees with the expression $n_1/(n_1 - 1)$ used in bulk technology except that depletion capacitance is replaced by box capacitance in series with silicon film capacitance.

The extracted technology current $I_2$ corresponding to back channel activation (low front gate voltage) is approximately 0.35 µA which supports a rather comparable mobility between front and back channels according to:

$$\frac{\mu_2}{\mu_1} = \frac{C_{ox1} + C_{si}}{C_{ox2} + C_{si}} \cdot \frac{I_2}{I_1} \approx 2 \cdot \frac{I_2}{I_1} = 1 \qquad (3.4)$$

where $C_{si}$, $C_{ox2}$ and $\mu_2$ are silicon film capacitance, back oxide or box capacitance and back channel mobility respectively. Unlike the front transconductance efficiency case, the front gate voltage has a considerable impact on the volume inversion and

consequently on the back technology current $I_2$. The technology current $I_2$ varies between 0.3 µA and 1.3 µA while front gate voltage $V_G$ is varied from -0.3 V to 0.6 V. Considering an invariant chart of the back transconductance efficiency $g_{m2}/I_D$ vs. IC generates a less than 20 % error in weak and moderate inversion.

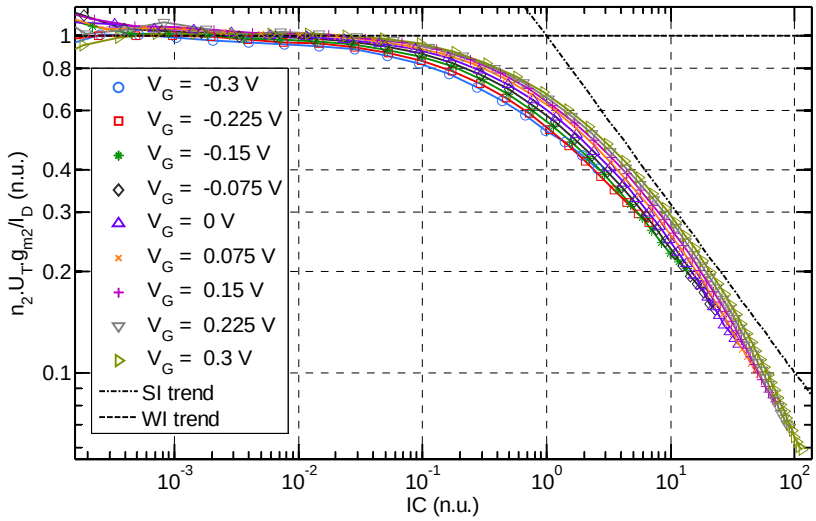



Fig. 3.8 Normalized $g_{m2}$ over $I_D$ as a function of the inversion coefficient at different $V_G$ for NMOS (L = 1 µm) in saturation ($V_D$ = 1V) at T = 25°C.

Front gate and back gate transconductance efficiency curves support that transconductance efficiency is maximized when charge carriers are not confined near the two interfaces but rather occupy the silicon film volume with a weaker transversal electrical field. This optimistic condition is obtained for certain combinations of front and back gate voltages ($V_G$, $V_{bG}$). In order to sustain this convenient state, front and back gates are swept simultaneously with a fixed voltage offset. This configuration can more easily be realized in design rather than sweeping the gates with a multiplication factor. Fig. 3.9 shows experimental transconductance efficiency curves where an ideal subthreshold slope is achieved for all offset values.

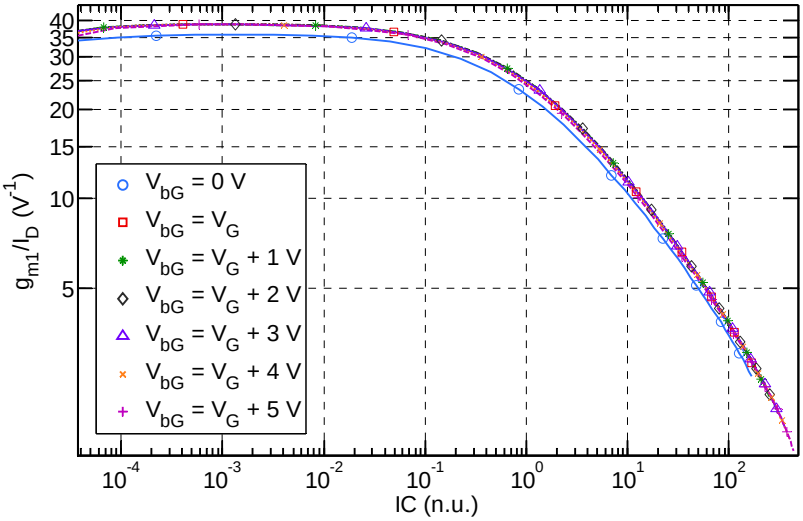



Fig. 3.9 Measured $g_{m1}$ over $I_D$ as a function of IC for fixed $V_{bG}$ and simultaneous front and back gates sweep with an offset for NMOS (L = 1 µm) in saturation ($V_D$ = 1V) at T = 25°C.

## 3.5.2 Temperature impact

The normalized $g_{m1}$ over $I_D$ characteristics measured at different temperatures for transistor length of 300 nm are shown in Fig. 3.10 and compared in the inset. In the comparison plots, most pessimistic case with regard to transconductance efficiency (i.e. T = 125 ºC) is taken as a reference. Normalization is using the unique $I_1$ and $n_1$ parameters extracted at 25 ºC (Table 3-1). Thermal voltage $U_T$ considers the measurements temperature. Less than 0.06 % error per degree Celsius is expected when considering $g_{m1}$ over $I_D$ versus IC characteristic invariance overall inversion levels. Maximum delta is obtained in the second half of the moderate inversion where charge carriers sensitivity is higher. It can be seen from Fig. 3.10 that transistor length of 300 nm slightly departs from strong inversion square law trend for high IC values (deep strong inversion). Such behavior is not significant for longer devices. The short channel impact will be assessed in the following section.

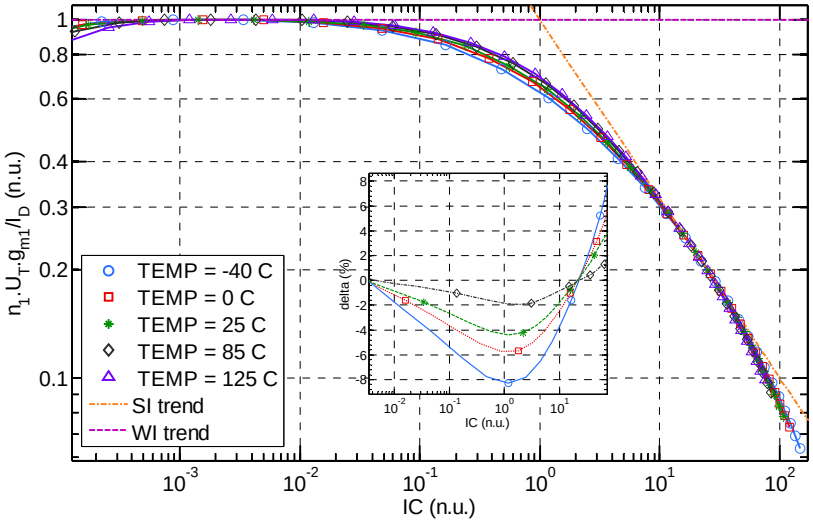



Fig. 3.10 $n_1.U_T.g_{m1}/I_D$ as a function of the inversion coefficient at different temperatures for NMOS (L = 300 nm & W = 1 µm) in saturation ($V_D$ = 1V) and $V_{bG}$ = 0 V; inset shows delta versus T = 125 ºC case.

### 3.5.3 Short channels

As shown in the previous plots for long transistors, transconductance efficiency is constant and maximum in weak inversion, decreases rather slowly in moderate inversion, and decreases as the inverse square-root of IC in strong inversion.

At the onset of strong inversion, transconductance efficiency is 70 % lower than its maximum value. Fig. 3.11 shows normalized transconductance efficiency as a function of IC for different transistor lengths for N type MOSFET. Equivalently, for P type MOSFET, Fig. 3.12 shows normalized transconductance efficiency as a function of IC for different transistor lengths. Short channel transistors depart from the strong inversion asymptotic behavior because of mobility reduction, velocity saturation effects and series resistance. The departure from SI trend is more important for N type than P type because of the carrier type difference. Transconductance efficiency curves overlay in weak and moderate inversion for the 120 nm to 4 µm range of channel lengths. For lengths below 120 nm, short channel effects lower subthreshold slope and enhance degradation (roll-off) of transconductance efficiency in strong inversion.

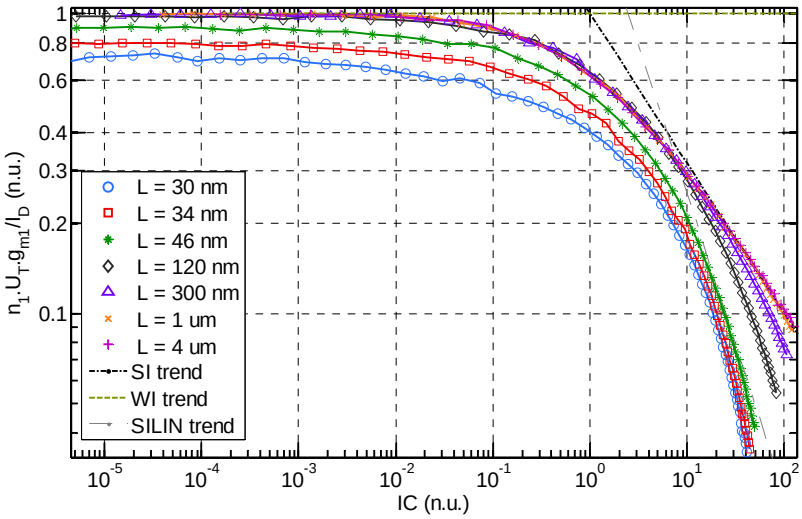



Fig. 3.11 Normalized $g_{m1}$ over $I_D$ as a function of the inversion coefficient for different lengths for NMOS (W = 1 µm) in saturation ($V_D$ = 1V) at T = 25°C.

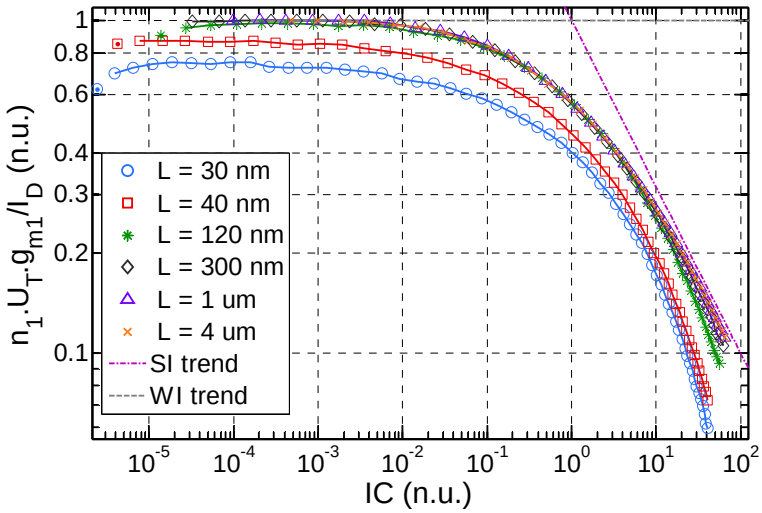



Fig. 3.12 Normalized $g_{m1}$ over $I_D$ as a function of the inversion coefficient for different lengths for PMOS (W = 1 µm) in saturation ($V_D$ = 1V) at T = 25°C.

Strong inversion degradation ceases when carrier's velocity saturates completely and a ~1/IC dependence is obtained. An additional degradation with respect to the linear asymptote (~1/IC) occurs when series resistance and mobility degradation add to velocity saturation for short channel transistors.

The long transistor unique chart can be used in weak and moderate inversion to predict transconductance efficiency for all transistors with a length greater than 120 nm while error is kept lower than 5 %.

To assess back gate voltage effect for a short channel MOSFET, the normalized $g_{m1}$ over $I_D$ is shown in Fig. 3.13 for L = 30 nm. The transconductance efficiency in weak inversion varies within 20 % across the entire range of back gate voltage conditions (from -4 V to 5 V). This spread is due to the short channel effects and the relative sensitivity of the subthreshold slope to back gate voltage. In Fig. 3.14, transconductance efficiency versus IC chart is measured for different temperatures. For short channel MOSFET, the chart varies with a low rate (less than 0.1 % per degree Celsius).

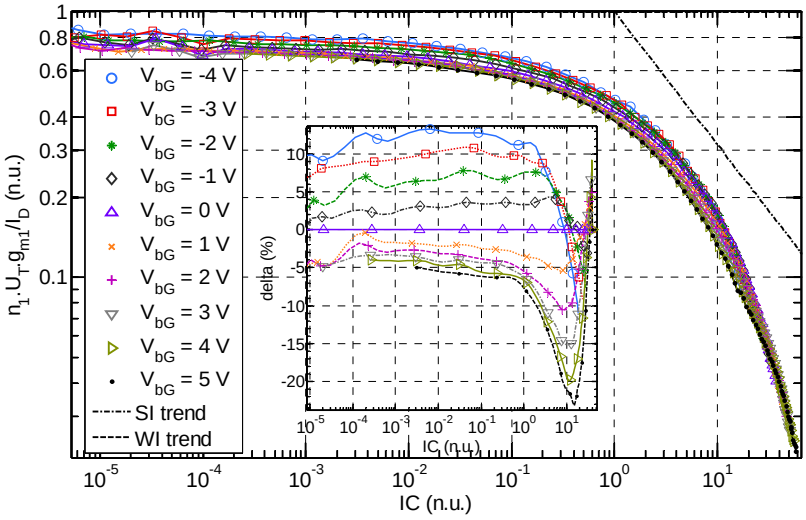



Fig. 3.13 Normalized $g_{m1}$ over $I_D$ as a function of the inversion coefficient at different $V_{bG}$ for NMOS (L = 30 nm & W = 1 µm) in saturation ($V_D$ = 1 V) at T = 25 °C.

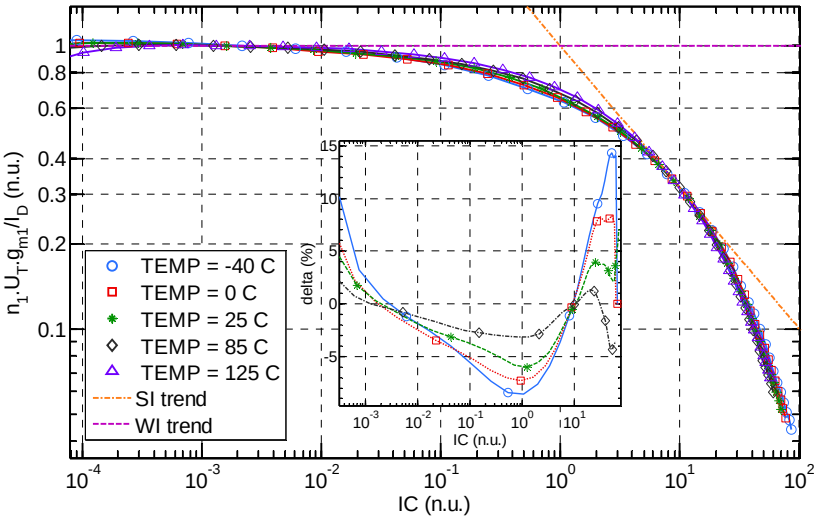



Fig. 3.14 $n_1.U_T.g_{m1}/I_D$ as a function of the inversion coefficient at different temperatures for NMOS (L = 30 nm & W = 1 µm) in saturation ($V_D$ = 1V) and $V_{bG}$ = 0 V; inset shows delta versus T = 125 ºC case.

### 3.5.4 Drain to source voltage

The concept of $g_m/I_D$ invariance should only be used in saturation regime and it is worth assessing the limit of drain potential below which the invariant breaks down in the onset of strong inversion. This information is useful in modern low-voltage low-power design since high transconductance efficiency is obtained in moderate inversion with lower drain to source saturation voltage $V_{DSAT}$.

Fig. 3.15 shows normalized transconductance efficiency versus IC for different drain to source voltages. In linear regime, the $g_{m1}/I_D$ curve departs from the saturation and strong inversion asymptotic behavior and follows the 1/IC asymptote instead (also shown in Fig. 3.15). The transconductance efficiency chart defined at $V_D$ = 1 V can be used for lower drain to source voltages down to $V_D$ = 250 mV in weak and moderate inversion (with an error of less than 4%).

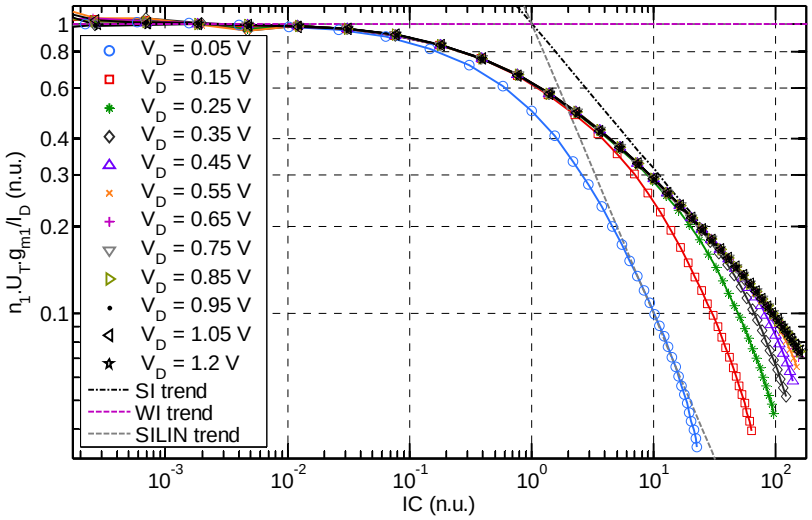



Fig. 3.15 Normalized $g_{m1}$ over $I_D$ as a function of the inversion coefficient for different $V_D$ for NMOS (W = 1 µm and L = 1 µm) at T=25°C.

#### 3.5.4.1 Sensitivity to manufacturing process variations

To check how sensitive transconductance efficiency versus inversion coefficient chart is to manufacturing process variations, foundry process based UTSOI model [110], has been used to plot three normalized transconductance efficiency characteristics versus IC. The characteristics correspond to the typical (TT), fast (FF) and slow (SS) corners. As shown in Fig. 3.16, the three corners charts practically

overlay and a maximum error of 4.5 % is obtained in deep strong inversion and less than 1.6 % error is made across the range of weak and moderate inversion (inset in Fig. 3.16).

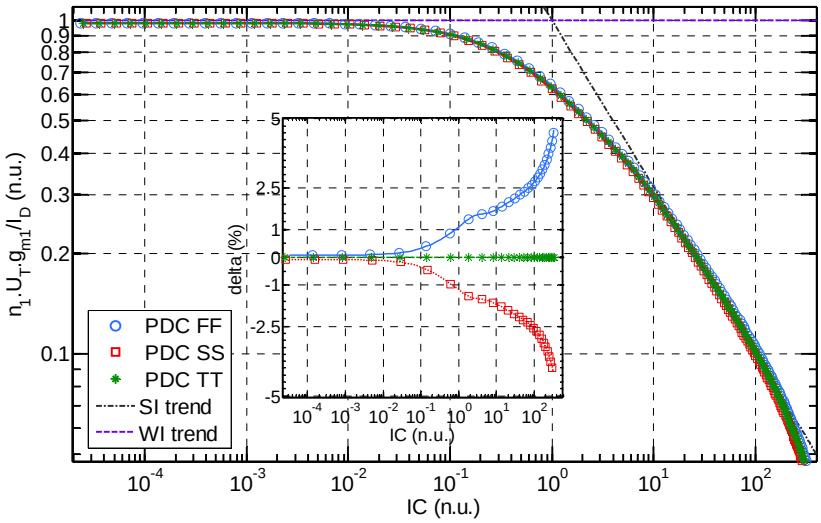



Fig. 3.16 NMOS transconductance efficiency as a function of the inversion coefficient for different process corners (L = 1 µm & W = 1 µm) in saturation ($V_D$ = 1V) and $V_{bG}$ = 0 V; inset shows delta versus typical corner case.

## 3.6 Discussion on $g_m$ over $I_D$ invariance

The transconductance efficiency clearly benefits from volume inversion apparent mobility comprehended as enhanced back channel mobility in [92] [93]. The optimum transconductance efficiency for a double gate MOSFET is obtained thanks to an enhanced mobility at low transverse field corresponding to a pronounced volume inversion. This is characterized by a higher carrier density in the center of the silicon film and a weak transverse electrical field. In this case, both effective mobility and gate capacitance are high and the corresponding technology current is boosted. For a back gate voltage of 2 V, a maximum transconductance efficiency is obtained at IC = 4 in Fig. 3.6 where $f_T.g_m/I_D$ figure of merit found to be optimal [82][110]. On the one hand, enhanced volume mobility helps to regain transconductance efficiency when back channel is inverted first (high $V_{bG}$) with lower front capacitance. On the other hand, the high capacitance, when only front channel inversion occurs, helps to partially recover the effect of degraded mobility on transconductance efficiency (low $V_{bG}$).

Consequently, $g_m/I_D$ vs. IC charts for different back gate voltages (from $V_{bG}$ = -2 V to 2 V) can be approximated using a universal chart with an acceptable error of 4%. The back gate voltage degree of freedom offered in asymmetric double gate transistors does not prevent design using $g_{m1}/I_D$ vs. IC chart especially in moderate inversion.

The transconductance efficiency versus IC chart determined using a typical long channel MOSFET at 25 ºC shows negligible sensitivity to temperature and process variations. The chart is invariant and rather insensitive to drain to source voltage as long as the transistor is in saturation. The minimum channel length for the chart invariance assumption is L = 120 nm. For NMOS, velocity saturation effects become significant in moderate inversion for L < 100 nm and chart cannot be used. However, a short channel chart might be considered as back gate voltage and temperature still have a relatively low impact at shorter MOSFETs. For PMOS, less subject to velocity saturation effects, shorter transistors can be sized using a unique PMOS chart.

## 3.7 Conclusion

In this Chapter, the universal aspect of the relationship between the transconductance efficiency ($g_m/I_D$) and the inversion coefficient (IC) has been investigated. We have shown that a unique chart can be exploited for the asymmetric double gate FDSOI transistors of the same type (N or P) with negligible errors in moderate inversion, thus of great interest for low-voltage and low-power applications. Sensitivity has been assessed in terms of back gate voltage, temperature, process corners, drain to source voltage and length. We have experimentally shown that $g_m$ over $I_D$ versus inversion coefficient chart can be considered as a fundamental characteristic of UTBB FDSOI technology transistors and thus be used in $g_m$ over $I_D$ based analog design sizing procedures.

# Part II

# High frequency Operation

# Chapter 4

# High Frequency Operation

## 4.1 Introduction

Today we can have access to information from everywhere thanks to wireless technology. Outstanding progress has been achieved to meet different range requirements from short-range Bluetooth to long-range cellular and satellite networks. According to Shannon's Theorem, the channel capacity and consequently the communication data rate depends on bandwidth and signal-to-noise ratio. Evidently, one way to increase the data rate is to move towards higher frequencies where more bandwidth is available [111]. With the tremendous high frequency capabilities in the latest technology nodes, CMOS based low cost millimeter Wave (mm-Wave) applications are now possible despite the fact that CMOS is not optimized for mm-Wave performance. However, implementing mm-Wave applications using CMOS technologies means operating at very high frequencies and close to the transistors "limits" (i.e. $f_T$ and $f_{max}$). Various applications are today operating in the mm-Wave band such as the 77 GHz automotive long-range automatic cruise control application and other applications such as the 60 GHz Wireless USB are still to come [11][13]. With such applications, CMOS circuits have new opportunities to operate above 60 GHz and consequently accurate MOSFET RF and mm-Wave models are required. Though both characterization and modeling are challenging for MOSFET high frequency operation.

As previously shown in Fig. 2.35, at high frequency operation the amplification capability of the transistor tends to decrease and the quasi-static models are enable to reproduce this behavior. Not only the mutual transadmittance $y_m$ acquire an imaginary part, but also the real and imaginary parts decrease in magnitude and the phase shift increases. This phenomena is observed for all geometries and bias conditions, in particular for long channel devices. The phase shift of $y_m$ means that the voltage

excitation at the gate terminal lags behind the generated current at the drain terminal. This delay is due to the distributed effects that are taking place in the MOSFET structure and that are not modeled neither in the equivalent circuit of Fig. 2.20 nor in Leti-UTSOI2 compact model. In this Chapter, the RF and mm-Wave characterization method is briefly described and modeling solutions are proposed for the intrinsic and extrinsic parts of the UTBB FDSOI structures. The proposed model is finally validated using measurements up to 110 GHz.

## 4.2 RF and mm-Wave characterization

Only DC-based extraction leads to RF performance overestimation therefore RF extraction is required to mitigate high frequency operation real performances. The characterization using S-parameters measurements and de-embedding procedures is a method of choice for mm-Wave spectrum operation assessment. Accurate characterization needs several correction steps to get rid of the measurement setup and pads related parasitic elements, and consequently set the reference plan close enough to the intrinsic DUT.

Model parameters are determined using extraction routines applied to measured characteristics. Dedicated test structures are measured in order to assess the different properties of the device and the several effects involved. Measurements are performed under various bias conditions, temperatures, and frequencies. As presented in Chapter 2, MOSFET characterization starts with DC and low frequency C-V measurements of several MOSFET geometries using voltmeter, ammeter, and LCR meter. For high frequency RF small-signal characterization in particular up to the mm-Wave spectrum, scattering (S-) parameters of dedicated structures are measured using a vector network analyzer (VNA), which measures the vector ratio of reflected and transmitted wave energy components in regard to incident energy component. Multi-finger MOSFET structures are embedded in Coplanar Waveguide (CPW) pads for high frequency characterization. Multi-finger and wide structures are used to obtain higher RF gain since $g_m \sim N_f.W/L$. S-parameters are measured in a frequency range from 100 MHz up to 110 GHz (i.e. up to the beginning of the Terahertz spectrum) in

linear, saturation and for all channel inversion levels: weak, moderate and strong. The test structures used for RF and mm-Wave measurements follow specific design rules to minimize the impact of coupling paths between probe-heads and the adjacent area of the measured structure [112][113].

In the high frequency measurements, a network is referred to as an n-port structure where a port means an electrical connection allowing power to be transmitted, and every port is terminated by a certain impedance. In practice all ports are terminated using 50 Ω resistors. 2-port measurements are more common mainly for economic reasons. In the last years, multi-port VNA along with multi-port test sets were introduced for multi-port DUT characterization [114].

In this work, the standard 2-port measurement setup shown in Fig. 4.1 is used where gate and drain represent respectively port 1 (v1) and 2 (v2), source and back gate being shorted and grounded. Mainly 2-port measurements are used while 4-port measurements are undertaken when required, in particular to set back gate voltage and source voltage independently.

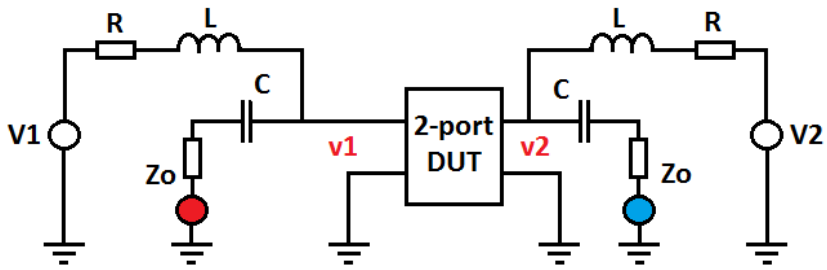



Fig. 4.1 2-port RF structures setup for S-parameters measurement.

On-wafer high frequency measurements using G-S-G (ground-signal-ground) probes are sensitive to parasitic elements that degrade the performance of the inner DUT (device-under-test). Parasitic elements originate from the measurement setup or from the G-S-G probe pads attached to the DUT as shown in Fig. 4.2. The parasitic capacitive and resistive extrinsic elements must be characterized and excluded carefully. In order to get rid of these parasitic contributions, RF measurements are de-embedded using dedicated OPEN and SHORT structures for each measured device as shown in Fig. 4.2. DC-extraction flow undergone in Chapter 2 is a prerequisite for

RF extraction. No fine-tuning is required for DC extracted capacitances and series resistances, SHORT structure being used for parasitic resistances extraction before DC-extraction flow. In summary, the effect of the surrounding parasitic elements are removed using two correction steps:

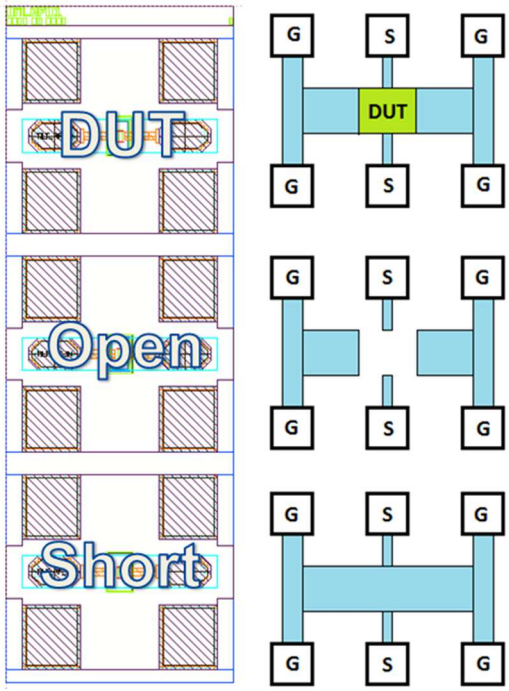



Fig. 4.2 2-port test structures using Ground-Signal-Ground probe pads

1. **Calibration**:

   The goal is to define the electrical boundary where the measurement system ends and the DUT starts in the setup. This boundary is usually called the reference plane and set at the structure pads. The definition of a reference plane for S-parameters measurements is done by measuring patterns with known electrical characteristics. This operation is called calibration and different standard techniques exist to achieve this calibration. The calibration using short, open, matched load, and through (SOLT) is the main technique used in this work. Other more advanced techniques also exist such as TRL and LRM techniques. The patterns used for calibration can be processed on wafer with the DUT or on a separate high-precision substrate called the impedance standard substrate (ISS).

2. **De-embedding**:

In order to get rid of the detrimental structure pad parasitic elements and extend the reference plane to the inner DUT, another important operation is executed after measurements. This operation is called de-embedding and is taking the measured S-parameters as a starting point for mainly two mathematical operations. The main pad parasitic elements are in parallel with the pads as depicted in Fig. 4.3 and stripped off first. S-parameters from the DUT and the OPEN structures shown in Fig. 4.2 are converted into Y-parameters, and subtracted in order to de-embed the parallel pad parasitic elements and leave the DUT along with the series parasitic elements. A second operation is executed to remove the series parasitic elements using the SHORT structure, and the operation uses the converted Z-parameters.

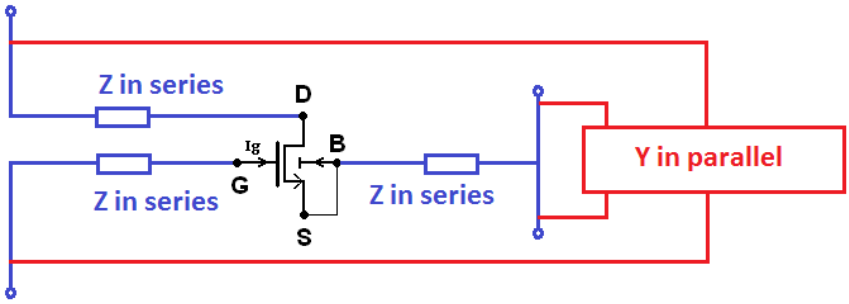



Fig. 4.3 Schematics representing the DUT with parallel and series parasitic elements (B = bG).

The calibration and de-embedding procedures do not get rid of the extrinsic parasitic elements of the DUT itself such as the gate resistance, the series source and drain resistances, the overlap and inner fringing capacitances, and the bulk or back gate resistance. All these series and parallel parasitic elements have detrimental impact on the MOSFET high frequency performance, especially gate resistance [115]. All these remaining parasitic elements need to be modeled carefully.

In order to extract the equivalent circuit parameters, the following expressions are used:

Table 4-1 Summary of the expressions used for equivalent circuit parameters extraction from Y-parameters (source and back gate being tight together in a 2-port).

| Small signal component | Expression |
|---|---|
| Gate resistance in SI ($R_G$) | $R_G = Re(Y_{11}^{-1})$ |
| Gate to drain capacitance ($C_{gd}$) | $C_{gd} = -\frac{Im(Y_{12})}{\omega}$ |
| Drain to gate capacitance ($C_{dg}$) | $C_{dg} = -\frac{Im(Y_{21})}{\omega}$ |
| Transconductance at low frequency $g_m$ | $g_m = Re[Y_{21} - Y_{12}] = \lvert Y_{21} - Y_{12} \rvert$ |
| Front gate to source and bulk capacitance ($C_{gs}$+$C_{gb}$) | $C_{gs} + C_{gb} = \frac{Im[Y_{11}]}{\omega} - C_{gd}$ |
| Output conductance ($g_{ds}$) | $g_{ds} = Re[Y_{22} + Y_{12}]$ |
| Drain to source and back gate capacitance ($C_{sd}$+$C_{bd}$) | $C_{sd} + C_{bd} = \frac{Im(Y_{22})}{\omega} - C_{gd}$ |
| Mutual capacitance ($C_m$) | $C_m = C_{dg} - C_{gd}$ |

## 4.3 High frequency operation modeling

Fig. 4.4 shows the mutual transadmittance with respect to frequency of a long channel MOSFET. The modulus, which is equal to the transconductance $g_m$ at low frequency, starts to decrease beyond a critical frequency $F_{crit}$. The phase shift decreases faster than the modulus from initial value of zero up to more than 270° (i.e. 180°+90° noting that phase continues to decrease even beyond the -180° and discontinuities in the plots are only due to the phase axis unit convention). The critical frequency depends on $V_{GS}$ and consequently on the channel inversion level. For long channel devices, the critical frequency is lower for lower inversion levels. However, for short channel devices, the $y_m$ phase decreases faster for stronger levels of inversion (i.e. $F_{crit}$ is lower for SI) as shown in Fig. 4.5 although subtle. Two distribution effects are competing in a MOSFET structure: (1) the non-quasi-static (NQS) effect due to the longer channel [116], and (2) the longitudinal distribution effect due to the longer gate fingers [117]. These two effects are represented in Fig. 4.6.

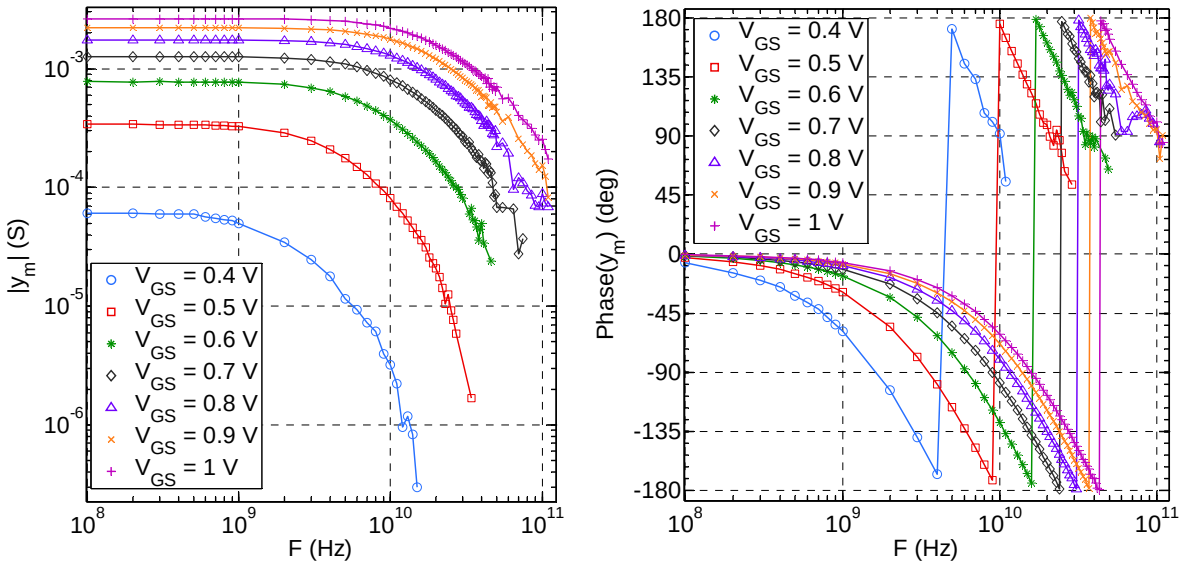



Fig. 4.4 Measured modulus (left) and phase (right) of the mutual transadmittance of an N Type MOSFET with L = 1 µm in saturation ($V_{DS}$ = 1 V).

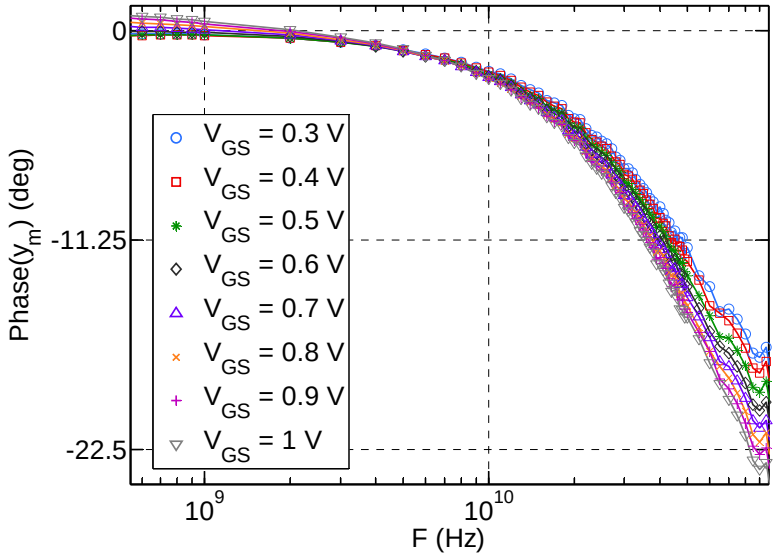



Fig. 4.5 Measured phase of the mutual transadmittance of an N-Type MOSFET with L = 28 nm in saturation ($V_{DS}$ = 1 V).

The two competing effects (1) and (2) will be modeled gradually in the following Sections.

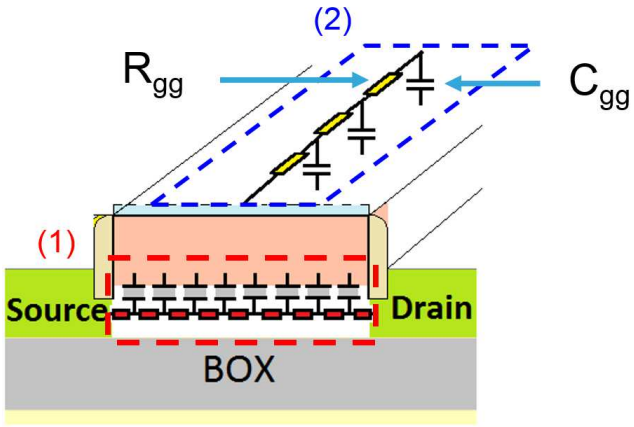



Fig. 4.6 A representation of the two distribution effects in the channel (1) and in the gate finger (2).

For DC and low frequency operation, no gate resistance is required as the gate leakage current is very low (i.e. typically lower than 10 nA/µm$^2$). However, for high frequency operation, the gate resistance should be taken into account, noting that high dynamic (AC) current is generated at the gate terminal. Moreover, the gate resistance in series with the gate capacitance will contribute a pole in the transadmittance function, and this will decrease the transadmittance modulus as shown in Fig. 4.4.

### 4.3.1 Simplified front and back Gates models

For high frequency operation, it is required to have a scalable model for the front gate resistance $R_G$ similar to the PSP standard model [98] and for the back gate resistance $R_{bG}$. Front gate resistance $R_G$ takes into account several contributions shown in Fig. 4.7: (a) the contact resistances, (b) the horizontal gate sheet resistance and finally (c) the vertical gate resistance related to the processed gate stack. The augmented model is shown in Fig. 4.8 (bottom) where series resistors $R_S$ and $R_D$ as well as gates resistors are added on top of the core model. Two models are proposed for the core part: (1) the equivalent circuit in Fig. 4.8 (top), and (2) the UTSOI2 compact model with implicit series resistances. The gate resistance $R_G$ is calculated as:

$$R_G = \frac{1}{N_f}\left(R_{contact} + R_{sh}.\frac{W_f}{\eta \times L} + R_{int}.\frac{1}{L \times W_f}\right) = \frac{1}{N_f}\left(R_{contact} + R_{shT} + R_{intT}\right) \quad (4.1)$$

where $R_{contact}$ is the one side gate finger access contacts resistance, $R_{sh}$ is the horizontal sheet resistance and $R_{int}$ is the interface vertical resistance. $W_f$ and $N_f$ are the gate finger width and the number of fingers, respectively. η is equal to 3 for a single-side connected gate and is equal to 12 for a double-side connected gate.

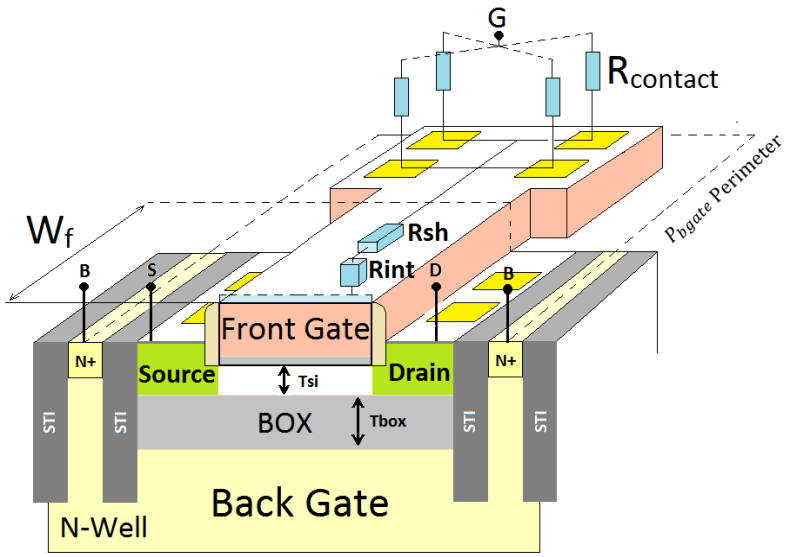



Fig. 4.7 UTBB FDSOI transistor architecture (3D).

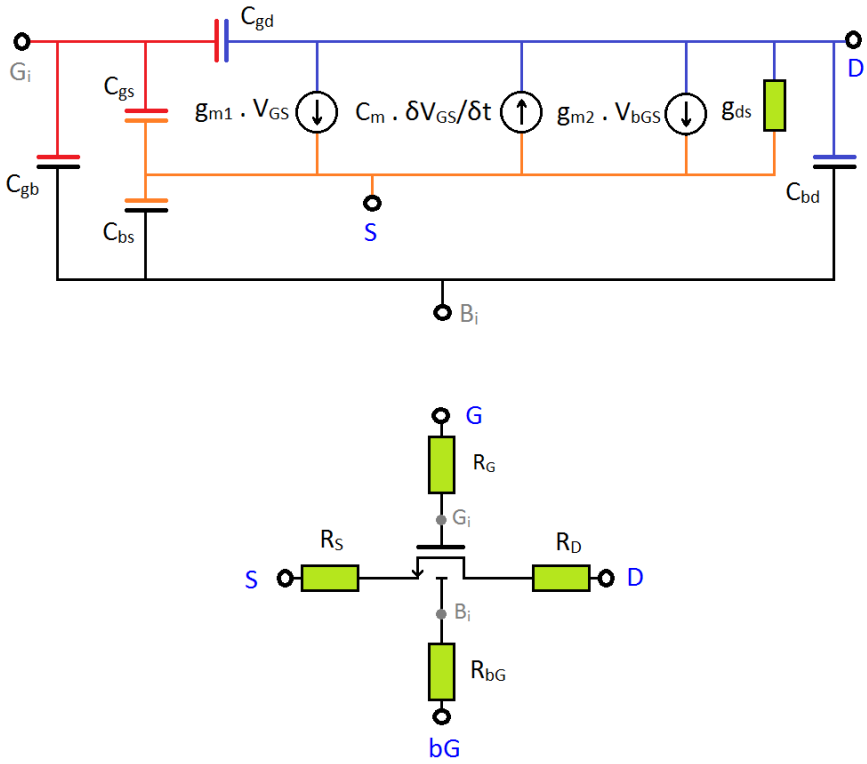



Fig. 4.8 RF equivalent schematic proposal with additional front-gate ($R_g$) and back-gate ($R_{bG}$) resistances. Top: the core model. Bottom: the complete quasi-static model.

Back gate resistance $R_{bG}$ describes the resistive access to the ground plane underneath the BOX. $R_{bG}$ resistance takes into account the structure layout in a simple manner using access perimeter $P_{bgate}$. In the following $R_{bG}$ expression, the horizontal resistive path under the box is considered to be negligible in comparison to the vertical strap access represented by the resistance per unit perimeter $R_{bsh}$ and including the effect of the N+ access zone and vertical N-Well path.

$$R_{bG} = R_{bsh} \times \frac{1}{P_{bgate}} \tag{4.2}$$

In order to extract $R_G$ and $R_{bG}$ related parameters, de-embedded S-parameters are transformed into Y-parameters and the two expressions (4.3) and (4.4) are used in high frequency operation:

$$R_G = Re(Y_{11}^{-1}) \tag{4.3}$$

On the one hand (4.3) is used to calculate the effective high frequency front gate resistance. On the other hand the following expression is used to extract the back gate

resistance. The expression is the well-known Mason's Unilateral Gain that is sensitive to $R_{bG}$:

$$U = \frac{|Y_{21} - Y_{12}|^2}{4.(Real(Y_{11}).Real(Y_{22}) - Real(Y_{12}).Real(Y_{21}))} \quad (4.4)$$

Transconductance is extracted in DC using drain current derivative and also in RF using the modulus or real part of the mutual transadmittance $y_m = Y_{21}$-$Y_{12}$. It is important to point out that in low-frequency, the two quantities must be equal and should diverge at high frequency operation as the effective transconductance and consequently gain decreases with frequency increase.

Although the proposed model in Fig. 4.8 reproduces accurately the high frequency behavior for short channel devices with mitigated NQS effects, the model fails to reproduce high frequency measurements for a long channel device. Fig. 4.9 shows the measured and simulated real part of the transadmittance with respect to frequency. The gate resistance in series with $C_{gg}$ adds a pole to the transadmittance but the critical frequency dependence on $V_{GS}$ is not captured correctly. The gate resistance tuning provides enhanced trend only for a given inversion level as shown in Fig. 4.10 where SI decrease is captured up to 10 GHz but not predicted for lower inversion levels. Moreover, the modulus of the current gain $H_{DG}$ shown in Fig. 4.11 is not predicted with a quasi-static model for high frequency operation although the transit frequency extracted using the slope at low frequency is correctly captured using same curves. A model valid for non-quasi-static operation is therefore required. In particular, the NQS effect will add poles and zeros to the transadmittance characteristic and thus will mitigate the accelerated decrease observed in the simulations shown in Fig. 4.9 [116].

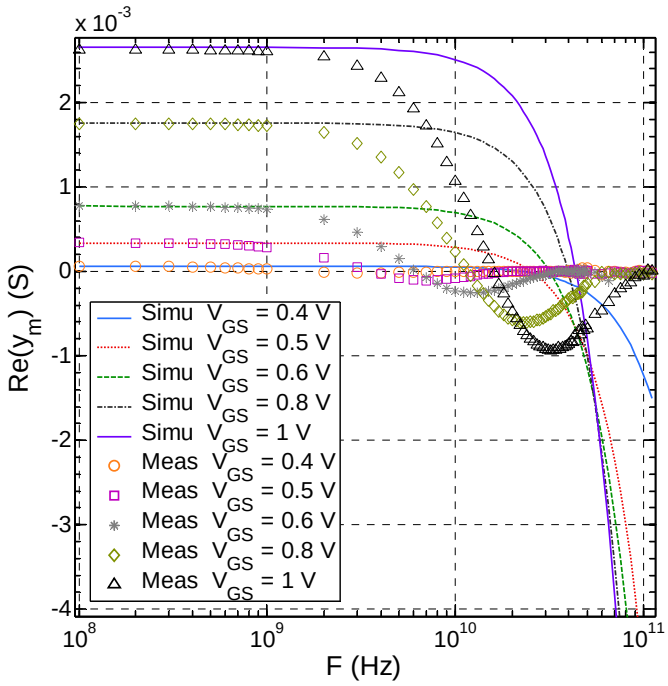



Fig. 4.9 The real part of the measured and simulated mutual transadmittance $y_m$ of a long channel L = 1 µm for various gate to source voltages from WI to SI in saturation ($V_{DS}$ = 1 V). Model includes simplified front and back gates resistances and ignores NQS effect.

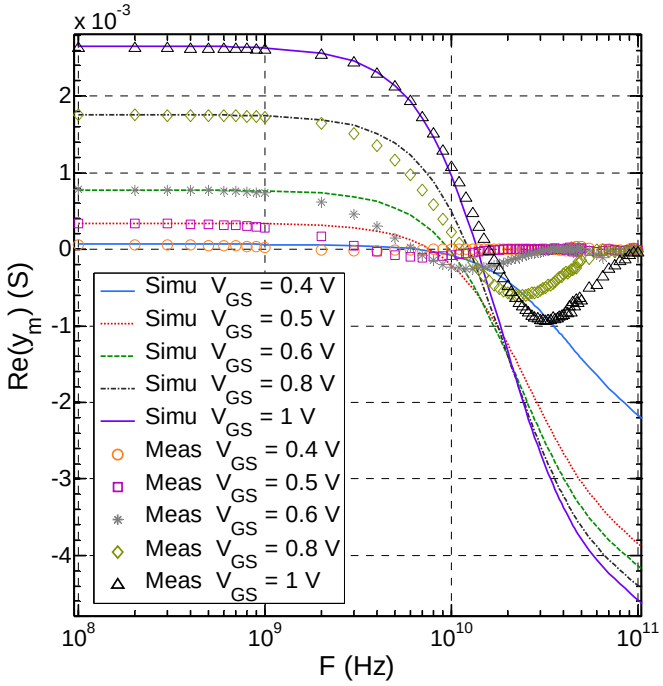



Fig. 4.10 The real part of the measured and simulated mutual transadmittance $y_m$ of a long channel L = 1 µm for various gate to source voltages from WI to SI in saturation ($V_{DS}$ = 1 V). Model includes front and back gates simplified resistances. Front gate resistance is tuned for SI.

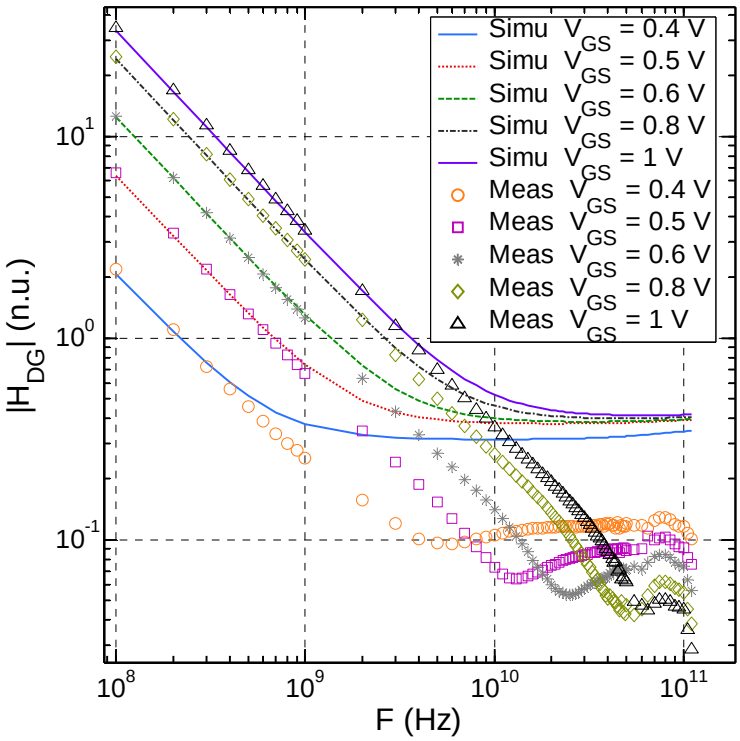



Fig. 4.11 The modulus of the measured and simulated current gain $H_{DG}$ of a long channel L = 1 µm for various gate to source voltages from WI to SI in saturation ($V_{DS}$ = 1 V). Model includes front and back gates simplified resistances and ignores NQS effect.

## 4.3.2 Channel segmentation

At high frequency operation, charge carriers inertia in a long channel limits the device performance and induces admittance and transadmittance phase shifts. The channel can be viewed as a transmission line at high frequency and should be modeled accordingly. An accurate and physically based charge model for NQS effects has been proposed by Sallese [116] based on Bessel functions. Other NQS formulations based on spline collation method are also proposed [118][119]. However, the proposed models are valid for small signal analysis only (i.e. no time domain transient) or difficult to efficiently implement on top of the proposed models unless a simplification is used (need of additional nodes). Several simplified NQS models are also proposed in the literature to capture the first order and used in standard models such as the relaxation time approximation (RTA) based method or the widely used Elmore model [120][121]. However, these simplified models are only valid up to a maximum of 1 to 2 $f_T$. The segmentation of the channel proposed in [122] is adapted to the UTBB FDSOI architecture and used for NQS modeling. The method is valid for small signal as well

as large signal analysis, in frequency and time domains. The MOSFET device channel is split into several segments. Each segment is modeled using UTSOI2 or the equivalent quasi-static circuit. Only 5 elements provided accurate results with respect to measurements and chosen as a tradeoff between accuracy and computational time. The decomposition is shown in Fig. 4.12 where all segments have same model parameters. Segmented model parameters extraction follows same procedure described in Table 2-2 with a special care being given to the saturation mode. In comparison to the quasi-static model, only saturation parameters are tuned provided that short channel effects related parameters are scaled in order to avoid any overestimation of these effects. The intermediate segments (i.e. $M_2$, $M_3$ and $M_4$) do not include series resistances, DIBL effect, and overlap and fringe capacitances. The outer segments (i.e. $M_1$ and $M_5$) do not include DIBL effect, and overlap and fringe capacitances but include source and drain series resistances.

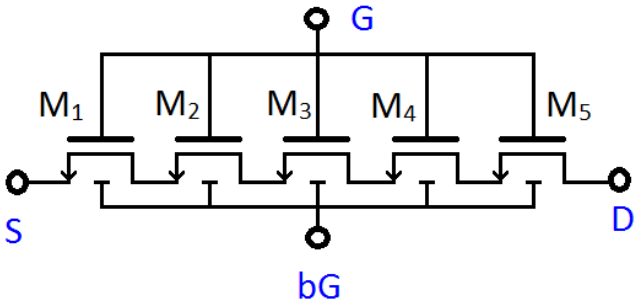



Fig. 4.12 Channel segmentation using 5 series MOSFETs.

In order to model the DIBL effect, two voltage dependent voltage sources are added in series with the two gate terminals. The DIBL is implemented as a threshold voltage shift. The overlap and fringe capacitances are modeled using a fifth parallel MOSFET with a mobility set to zero. The advantage of using a MOSFET shell for parasitic capacitances is the compatibility with the quasi-static model parameters in particular the overlap capacitance term. The model is shown in Fig. 4.13 along with the simplified front and back gates lumped models.

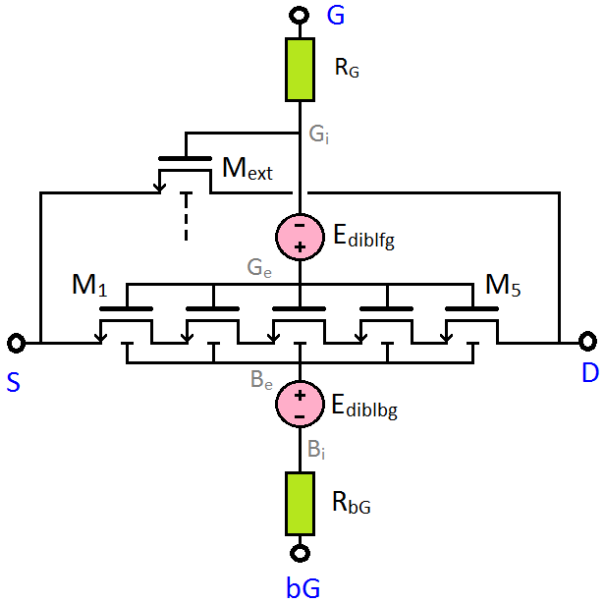



Fig. 4.13 Non-quasi-static model with simplified gates models.

### 4.3.3 Complete front and back gates model

Clearly, low and high frequency MOSFET behavior is strongly impacted by its parasitic elements. Unfortunately, the majority of standard models of CMOS MOSFET including UTSOI2 do not completely include extrinsic elements such as gate and substrate resistances required for high frequency operation. Only simplified and fixed parasitic elements are occasionally used but inappropriate in a scalable MOSFET layout. The augmented model in Fig. 4.13 predicts correctly MOSFET behavior of UTBB FDSOI MOSFET provided that fringe capacitance in series with the gate resistance are both tuned in order to reproduce an additional pole to the transadmittance function. In Chapter 5, it is evidenced that the two distribution phenomena represented in Fig. 4.6 are competing and should be modeled. The two phenomena namely channel NQS and gate distribution effect are confused in some research works noting that the consequence of the two effects on the Y-parameters are comparable. On the one hand the NQS effect adds zeros and poles to the transadmittance characteristic as demonstrated in [116]. On the other hand, according to Fig. 4.7, the gate contacts resistance and the horizontal salicide resistance (i.e. $R_{contact}$ + $R_{shT}$) in series with the top fringing capacitance (i.e. from gate salicide top area to the source and drain contacts) form a series RC circuit and consequently contributes a pole in the transadmittance characteristic. Another pole is also added by

the series combination of the physical gate resistance $R_G$ (i.e. $R_{contact}$ + $R_{shT}$ + $R_{intT}$) and the gate capacitance $C_{gg}$. This explains why channel NQS effect is sometimes modeled using an RC gate network provided that a parallel RC circuit is added to emulate the NQS zeros [123].

The model in Fig. 4.13 reproduces correctly the low frequency gate capacitance $C_{gg}$ (i.e. $Im(Y_{11})/2\pi F$)and gate resistance $R_{gg}$ (i.e. $Re(1/Y_{11})$) especially in SI for a long channel as depicted in Fig. 4.14. However, at high frequency, an additional pole is required to capture the $R_{gg}$ decrease especially for WI regime. Moreover, an additional gate capacitance contribution is required in order to capture the capacitance increase at high frequency. The constant additional capacitance will be also beneficial for the WI regime where extrinsic capacitors dominate. This additional pole is generated using an extrinsic fringing finger-length dependent capacitance $C_{frls}$+$C_{frld}$ between the top salicided area of the gate and source/drain contacts. Based on the measured $R_{gg}$ and $C_{gg}$ characteristics in Fig. 4.14, the decrease in the gate time constant $R_{gg}.C_{gg}$ tends to saturate because of a pole-zero compensation phenomena at high frequency.

The additional modeled pole (i.e. the one generated with the additional $C_{frls}$+$C_{frld}$ capacitance) will be compensated using a parallel RC circuit. A capacitance $C_{dge}$ will be added in parallel to the $R_{contact}$ + $R_{shT}$ resistance. Another parallel RC circuit is also added to mitigate the pole generated by the series $R_g$ and $C_{gg}$.

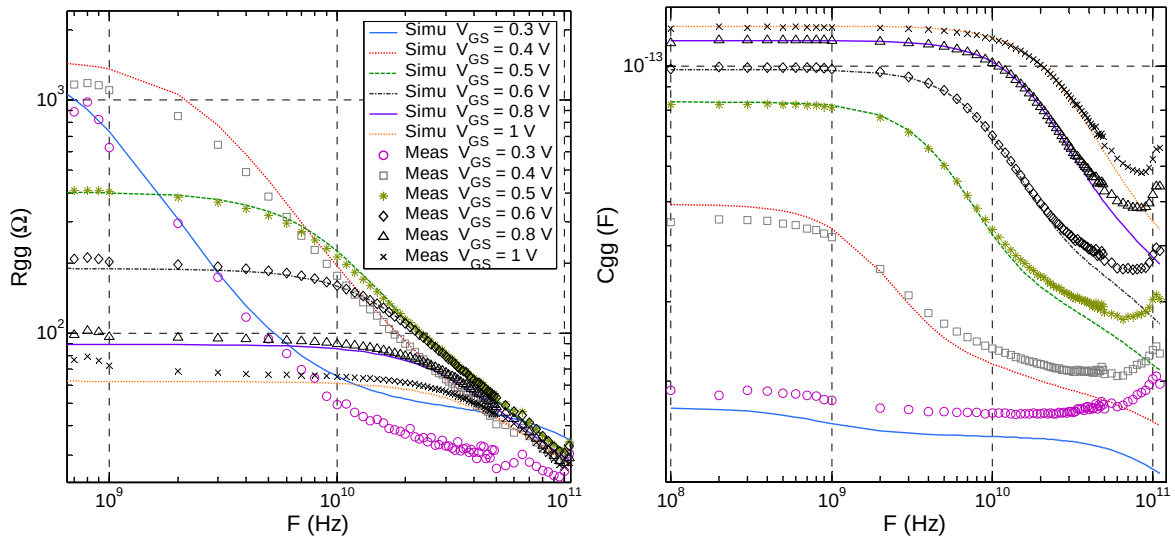



Fig. 4.14 Gate resistance (left) and gate capacitance (right) vs. frequency for L = 1 µm and Wf = 1 µm.

The series and parallel RC based front gate network developed using the pole-zero compensation technique is also convenient to model the gate distribution effect of short channels where the channel NQS effect contribution is mitigated. In summary, besides the NQS effect modeled using segmentation of the channel, the gate distributed effect must be modeled using series and parallel RC network. The front gate network is summarized in Fig. 4.15. In addition to the overlap capacitances included in the core MOSFET model, the gate network accounts for the lateral fringing capacitance (i.e. $C_{frwS}$+$C_{frwD}$) which is mainly dependent on the MOSFET width (i.e. finger length) [124].

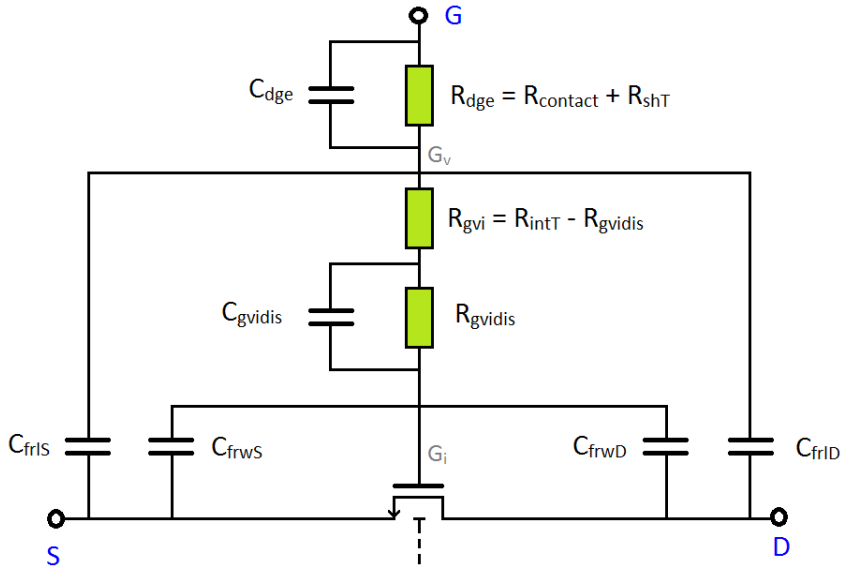



Fig. 4.15 Front gate network with series and parallel RC lumped circuits.

In order to account for the diode formed between the Well under the BOX and the substrate, a simple lumped circuit is added to the model for the comparison with the measured data. The final proposed model is shown in Fig. 4.16. A summary of the model parameters extraction flow is given in Appendix E, while the model validation is presented in the next Section.

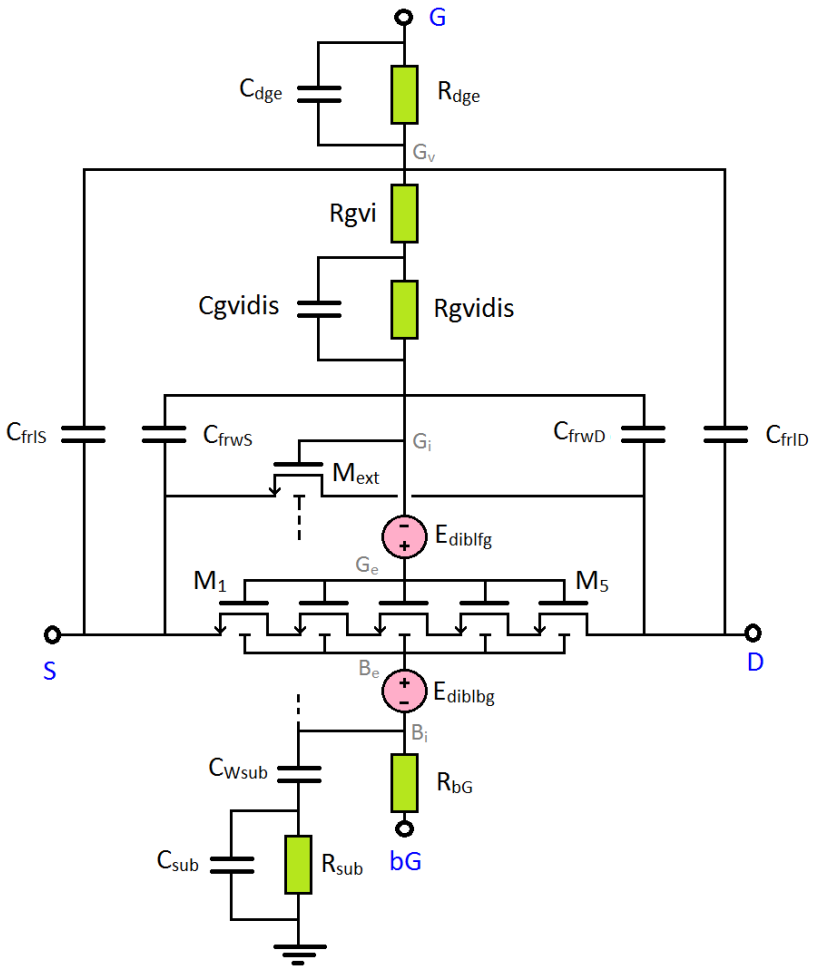



Fig. 4.16 Complete Non-Quasi-Static model.

## 4.4 RF and mm-Wave FoMs assessment

In order to validate the proposed model in Fig. 4.16, characterization based on DC and HF measurements has been performed starting with the flow described in Chapter 2 for a DC and low frequency model with a simplified front and back gates as shown in Fig. 4.13. The front and back gates networks parameters are then optimized on several geometries with various form factors ($W_f$/L). The gate network also accounts for the number of the access sides (1 or 2) depicted in Fig. 4.17 as it highly impacts the gate distributed effect. In particular, connection to the gate terminal from two opposite sides tremendously reduces the gate distribution effect and this is taken into account. Device performance is also impacted by device layout. In particular, the number of

fingers and the back gate access through dedicated straps are also accounted for as seen in the previous section.

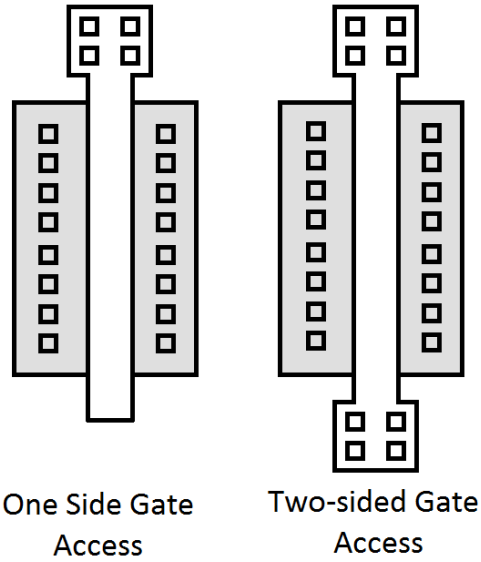



Fig. 4.17 One side and two side gate access configurations.

### 4.4.1 Y-parameters

S-parameters are practical metrics and are frequently used by microwave engineers and RF designers as the open or short circuit assumptions are not required. Instead, adapted terminations are used. However, S-parameters are generic and generally not practical to gain a deeper insight into the MOSFET physics. The measured S-parameters are transformed into Y-parameters and compared with the simulated counterparts for several inversion levels from WI to SI.

Fig. 4.18 shows the real and imaginary parts of the input and transfer Y-parameters for a short device (i.e. L = 30 nm) with respect to frequency in saturation ($V_{DS}$ = 1 V). Fig. 4.19 shows the equivalent metrics for a long channel device (L = 1 µm). The proposed model predicts accurately the Y-parameters over the wide frequency range from 100 MHz up to 110 GHz. The excellent accuracy over a wide frequency band of the simulations compared to measurements verifies that the topology of our model is correct and complete.

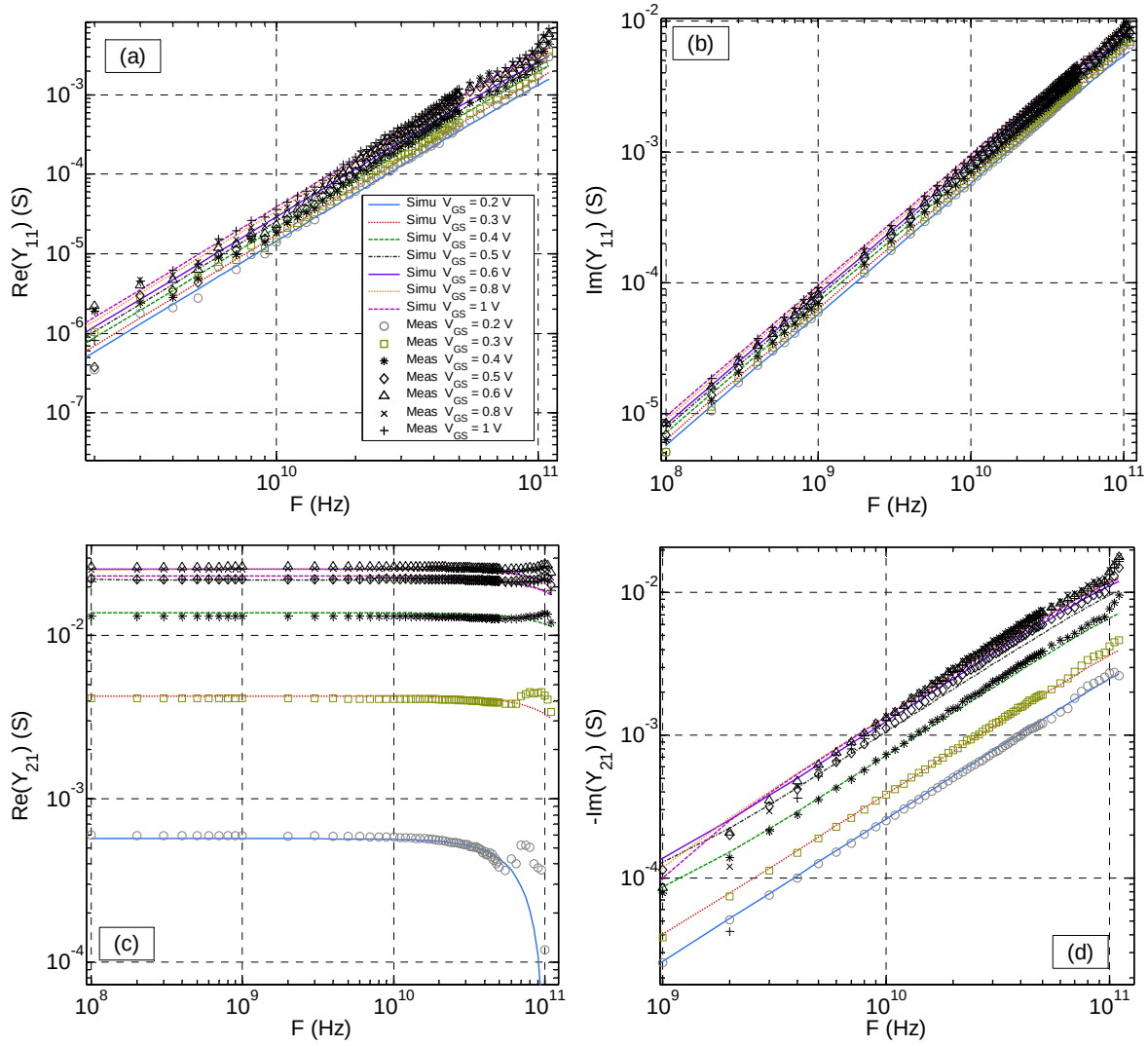



Fig. 4.18 Simulation and measurements of the input admittance $Y_{11}$ and input to output transadmittance $Y_{21}$ of a 30 nm long NMOS vs. frequency for various gate to source voltages from WI to SI in saturation ($V_{DS}$ = 1 V).

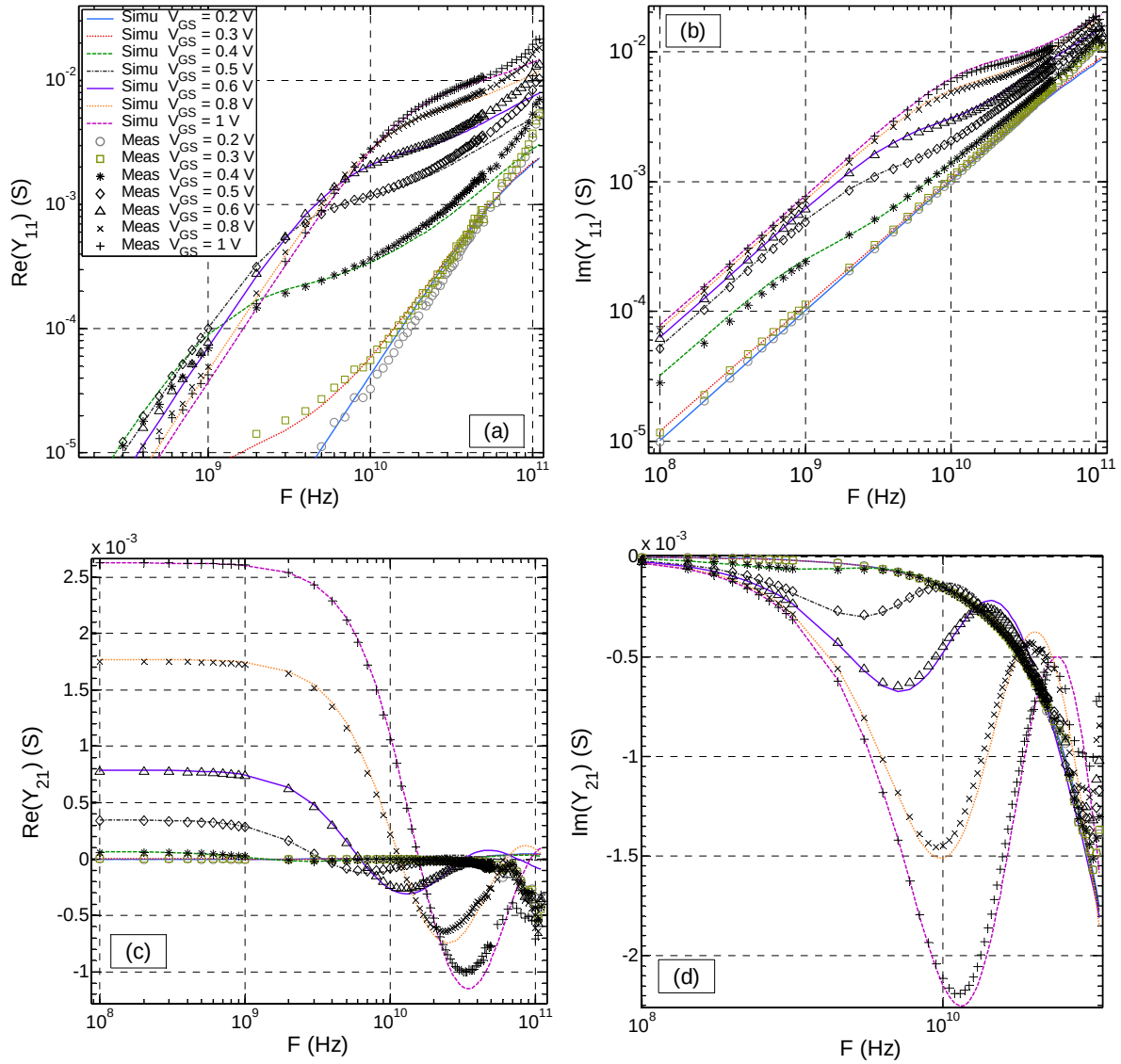



Fig. 4.19 Simulation and measurements of the input transadmittance $Y_{11}$ and input to output transadmittance $Y_{21}$ of 1 µm long NMOS vs. frequency for various gate to source voltages from WI to SI in saturation ($V_{DS}$ = 1 V).

Fig. 4.20 shows the real and imaginary part of the mutual transadmittance of a 1 µm long device with respect to frequency. The non-quasi-static effect is accurately reproduced including the antiphase phenomena. This is also evidenced in Fig. 4.21 where the phase shift is shown with respect to frequency although the gate distribution effect, optimized for a larger width, is overestimating the phase shift in WI. However starting from the MI, the phase shift is accurately predicted even beyond the antiphase shift (i.e. phase < -180°).

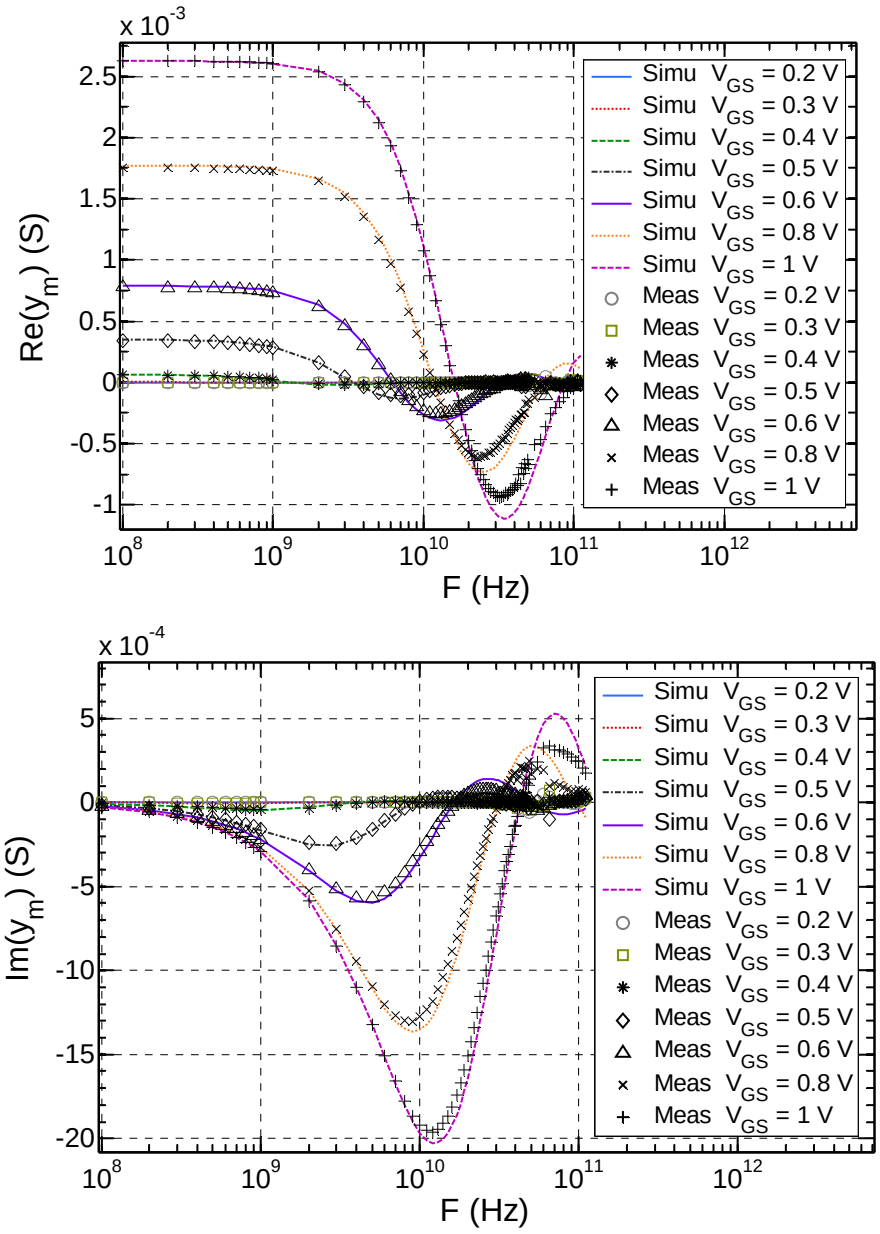



Fig. 4.20 Mutual transadmittance $y_m = Y_{21}$-$Y_{12}$ of a 1 µm long NMOS vs. frequency for various gate to source voltages from WI to SI in saturation ($V_{DS}$ = 1 V).

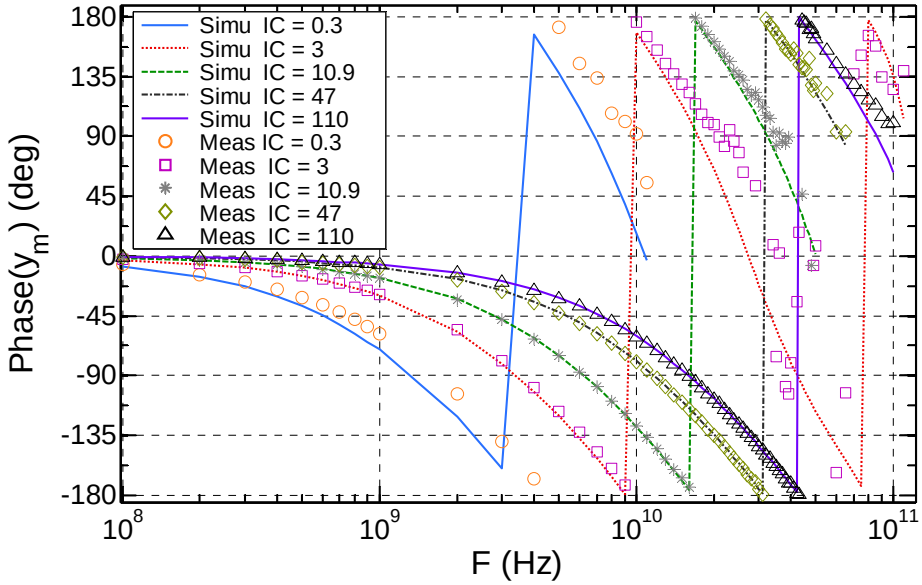



Fig. 4.21 Measured and simulated mutual transadmittance phase of a 1 µm long NMOS vs. frequency for various Inversion Coefficients IC from WI to SI in saturation ($V_{DS}$ = 1 V).

Derived from Y-parameters, two important RF Figures of Merit (FoMs) are the Transit Frequency of the current gain and the maximum oscillation frequency or cut-off frequency of the Mason's unilateral power gain. These two FoMs will be assessed in the following two sections. The FoM representing the tradeoff between the transconductance efficiency and the high frequency performance will be also assessed next.

## 4.4.2 Current gain and Transit Frequency FoM

The first quantity denoted $f_T$ is an interesting FoM for high-speed digital applications where speed and high swing are required. It is extracted at 0 dB current gain $|H_{DG}|_{dB}$ (or $|H_{DG}|$ = 1). Fig. 4.22 shows the current gain plots for several inversion levels in linear mode (i.e. $V_{DS}$ = 0.3 V). Fig. 4.23 shows the modulus of the current gain in saturation ($V_{DS}$ = 1 V) for short (left) and long (right) devices. We notice that gain becomes practically constant for low levels of inversion. This occurs at higher frequencies and $f_T$ extraction at $|H_{DG}|$ = 1 is still valid provided a suitable -20 dB asymptote is used. Current gain $|H_{DG}|$ vs. frequency presented in Fig. 4.22 and Fig. 4.23 as well as the normalized $f_T$ (using maximum $f_T$ value) vs. normalized drain current $I_d = I_D/(W/L)$ shown in Fig. 4.24 are accurately reproduced with the proposed model.

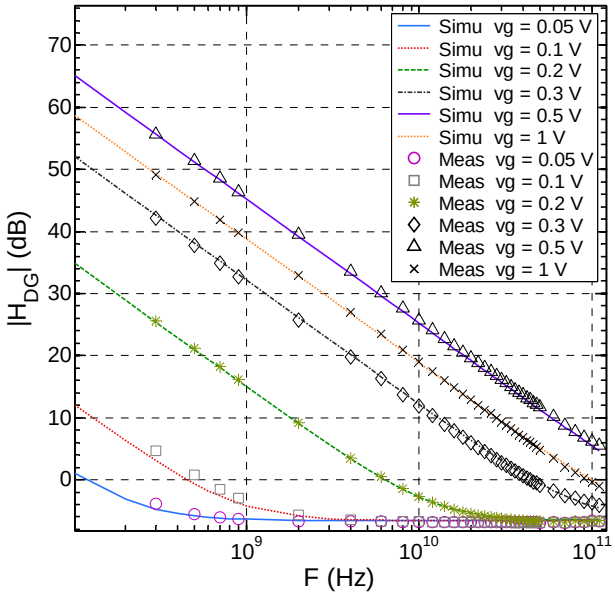



Fig. 4.22 Small signal current gain ($|H_{DG}|$) vs. frequency (F) in linear mode $V_{DS}$ = 0.3 V for NMOS (L = 30 nm, $W_f$ = 2 µm and $N_f$ = 10) at T = 25°C.

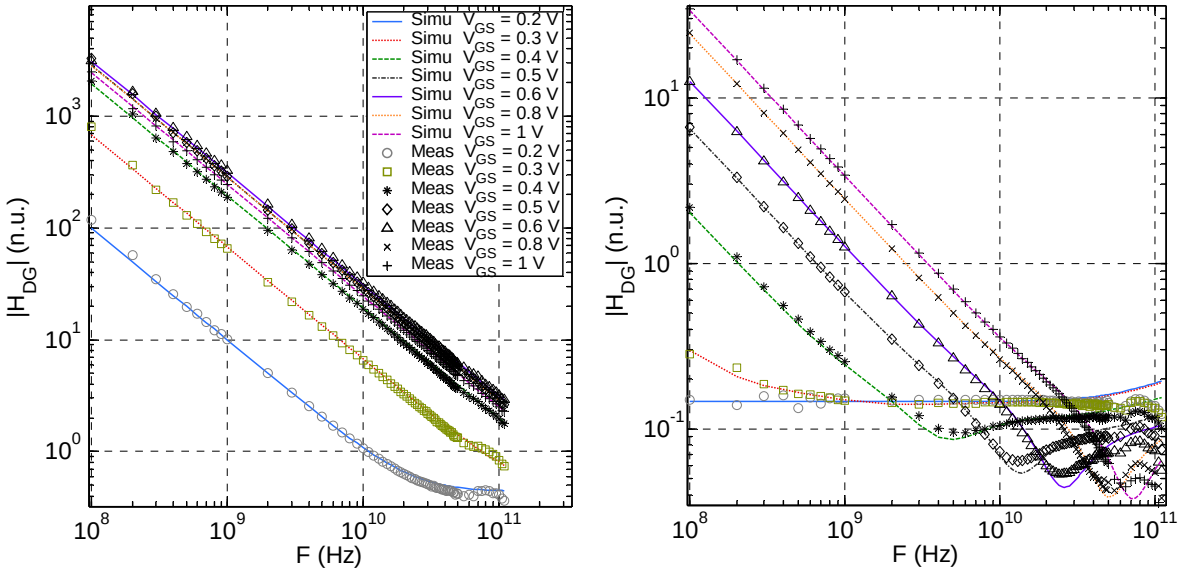



Fig. 4.23 Current gain $|H_{DG}|$ of a 30 nm long (left) and 1 µm long (right) N-type MOSFETs for various gate to source voltages $V_{GS}$ from WI to SI in saturation ($V_{DS}$ = 1 V).

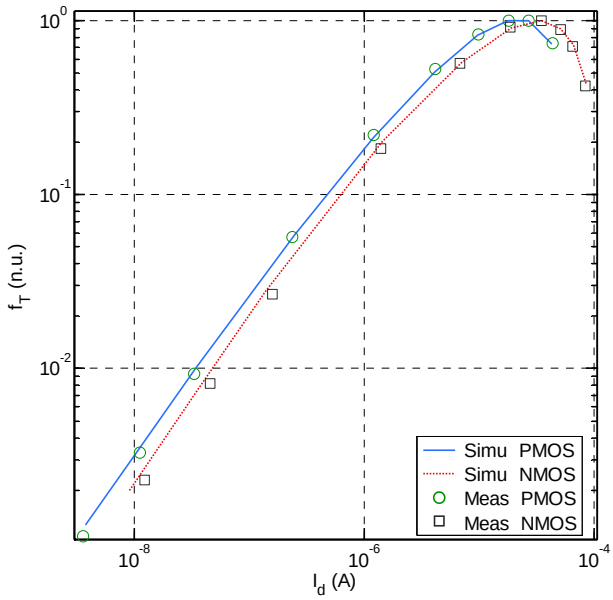



Fig. 4.24 Normalized transit frequency ($f_T$) vs. normalized drain current $I_d = I_D /(W/L)$ in linear mode $|V_{DS}| = 0.3$ V for NMOS and PMOS (L = 30 nm, $W_f$ = 2 µm and $N_f$ = 10) at T = 25°C.

Moreover, the transit frequency $f_T$ is correctly captured in saturation mode for both long and short channels as shown in Fig. 4.25 with respect to the inversion coefficient IC defined in the previous Chapter. The high frequency performance is reproduced for all levels of inversion in particular for L < 1 µm although, for L = 1 µm the performance in WI is decently captured but not useful for RF applications.

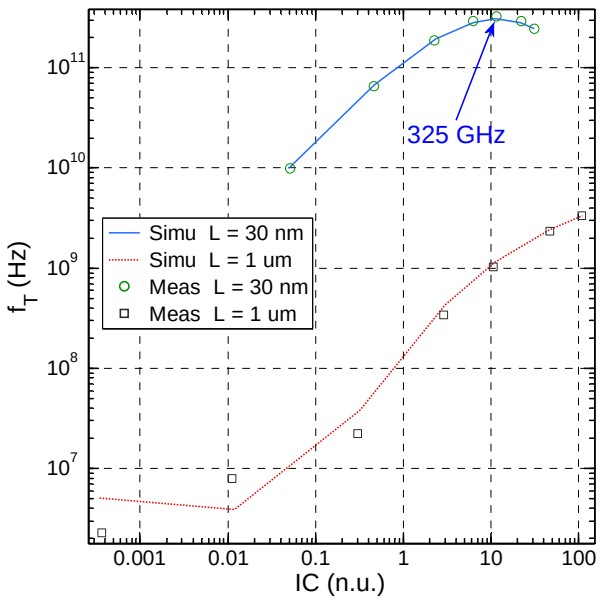



Fig. 4.25 Transit frequency $f_T$ versus IC of a short (L = 30 nm) and long (L = 1 µm) N-type MOSFETs in saturation ($V_{DS}$ = 1 V).

### 4.4.3 Mason's gain and maximum oscillation frequency FoM

$f_T$ alone is not sufficient to assess MOSFET performance at high frequency operation as it does not account for the impact of some important parasitic elements such as the gate resistance. $f_{max}$ however, defined as the frequency at which the extrapolated Mason's gain given by expression (4.4) drops to unity, is a more suitable FoM for RF analog applications such as microwave amplifiers. Both front gate and back gate resistances impact is accounted for and evidenced using $f_{max}$ FoM vs. $I_d$.

Fig. 4.26 shows Mason's gain modulus with respect to frequency for a short channel (i.e. L = 30 nm) in linear mode (i.e. $V_{DS}$ = 0.25 V) and for various gate to source voltages covering WI to SI regimes. Mason's gain is correctly reproduced for all levels of inversion although back gate resistance can be tuned to capture the high frequency slope for WI regime. Fig. 4.27 (left) shows Mason's gain simulated without the gates networks to illustrate the importance and accuracy of the proposed topology. The Mason's gain is reproduced correctly in saturation (i.e. $V_{DS}$ = 1 V) while accounting for the gates networks (right).

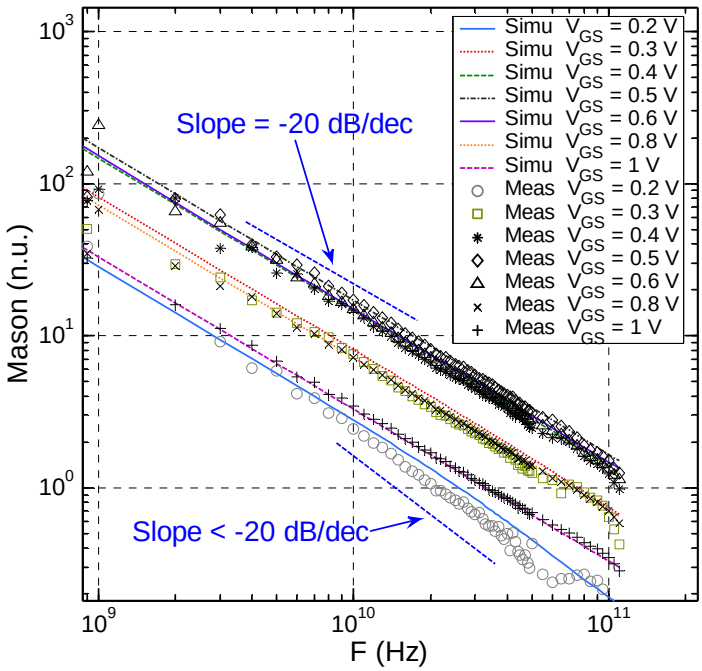



Fig. 4.26 Mason gain vs. frequency (F) of NMOS (L = 30 nm) for various gate to source voltages in linear mode $V_{DS}$ = 0.25 V.

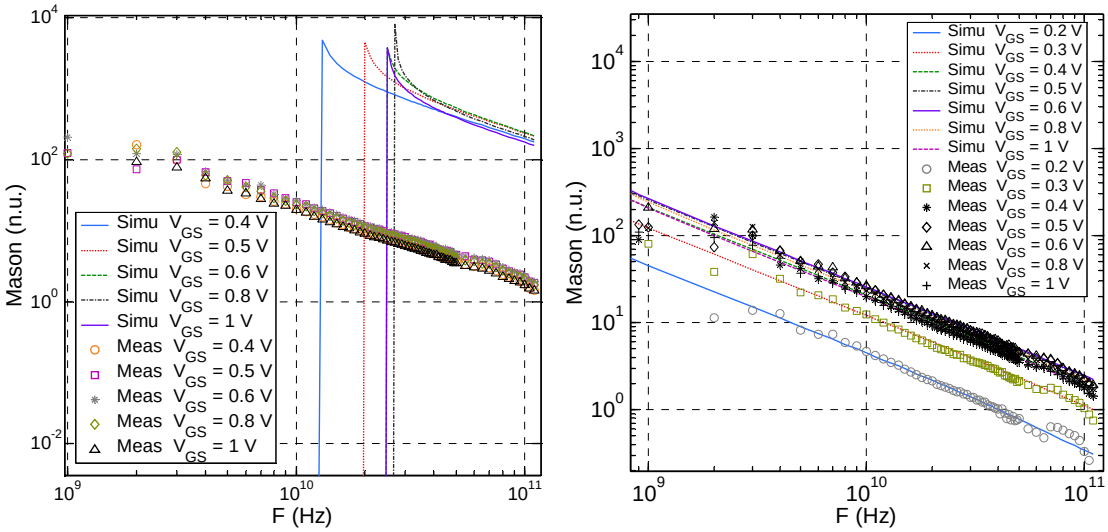



Fig. 4.27 Mason gain vs. frequency (F) of NMOS (L = 30 nm) for various gate to source voltages in saturation mode $V_{DS}$ = 1 V. Model w/o gates resistances (left) and with the gates networks (right).

Fig. 4.28 shows the simulated and measured $f_{max}$ normalized using maximum $f_{max}$ vs. $I_d$ demonstrating the model accuracy at high frequency operation. In weak inversion, Mason's gain slope decreases with frequency (as shown in Fig. 4.26), and this behavior is captured with a tuned $R_{bG}$ resistance [125]. Back gate resistance $R_{bG}$ impact is revealed and correctly reproduced in the frequency dependence of $f_{max}$ vs. $I_d$ curves particularly in weak inversion up to 80 GHz (Fig. 4.29). $f_{max}$ is reproduced in linear and saturation for all levels of inversion from WI to SI as shown in Fig. 4.30.

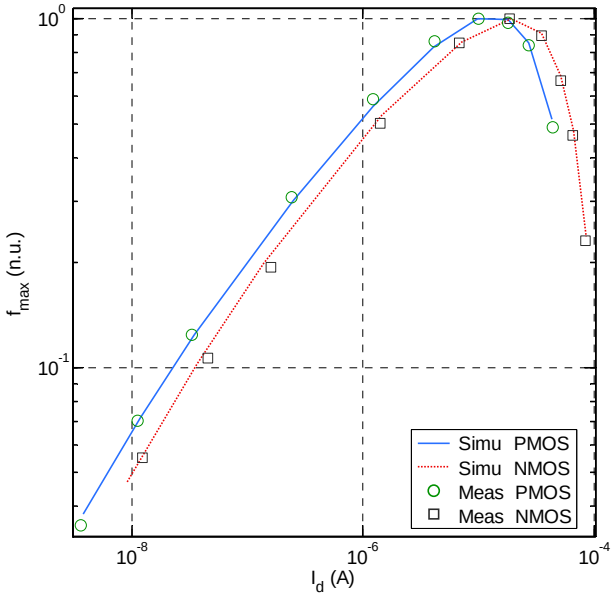



Fig. 4.28 Normalized $f_{max}$ vs. the normalized drain current $I_d$ in linear mode $|V_{DS}|$ = 0.3 V for NMOS and PMOS (L = 30 nm, $W_f$ = 2 µm and $N_f$ = 10) at T = 25°C.

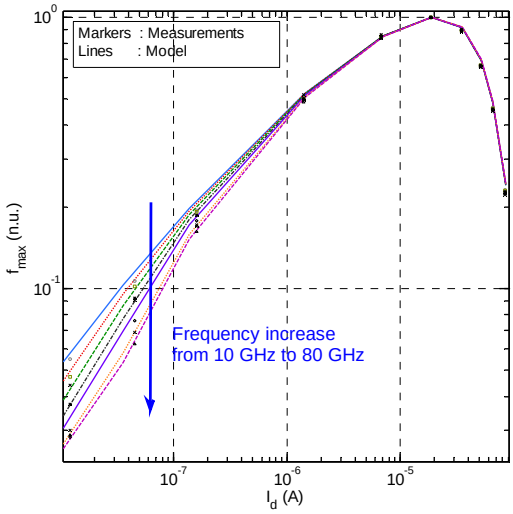



Fig. 4.29 Normalized $f_{max}$ vs. drain current $I_d$ in linear mode (i.e. $|V_{DS}|$ = 0.3 V) for NMOS and for following frequencies: 10 GHz, 20 GHz, 30 GHz, 40 GHz, 50 GHz, 70 GHz and 80 GHz (L = 30 nm, $W_f$ = 2 µm and $N_f$ = 10) at T = 25°C.

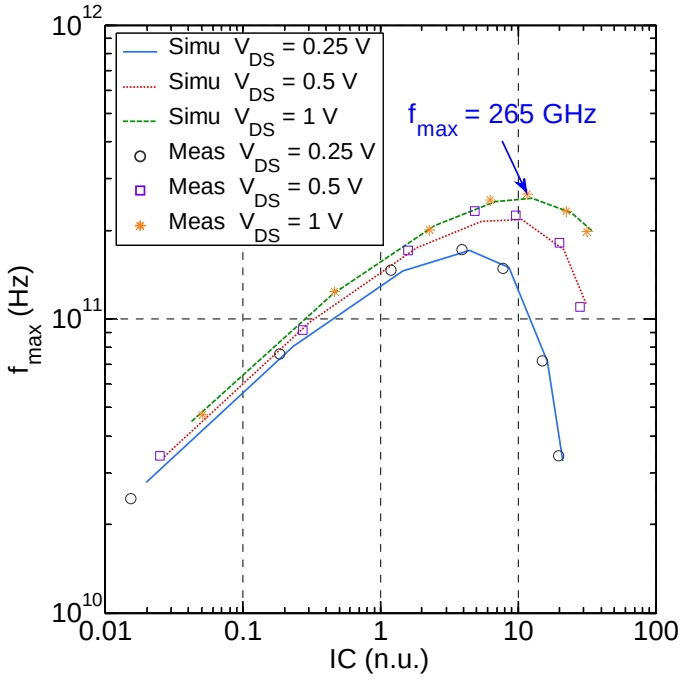



Fig. 4.30 $f_{max}$ vs. IC for NMOS L = 30 nm for various $V_{DS}$ from linear to saturation.

## 4.4.4 Performance and power consumption tradeoff FoM

$f_T$ and $f_{max}$ figures of merit are suitable for applications where only speed/performance is valued. The maximum value of these FoMs is obtained in strong inversion where transconductance efficiency ($g_m/I_D$) is low. Consequently, these FoMs are not suitable for low-voltage RF applications where performance and power

consumption are valued equally. The more convenient FoM for such low power consumption and high speed applications is the one introduced in [126] and given as:

$$FOM_{RF} = f_T \cdot \frac{g_m}{I_D} \tag{4.5}$$

Although a more generalized FoM will be proposed in next Chapter, this FoM captures decently both the transconductance efficiency and RF performance. The maximum value of this RF FoM represents the best tradeoff between power consumption and speed. In Fig. 4.31, $FoM_{RF}$ vs. normalized drain current $I_d = I_D/(W/L)$ is shown for NMOS and PMOS. Both MOSFET types present a maximum and consequently an optimum trade-off in moderate inversion region. Our model is accurately reproducing this RF FoM measurements too.

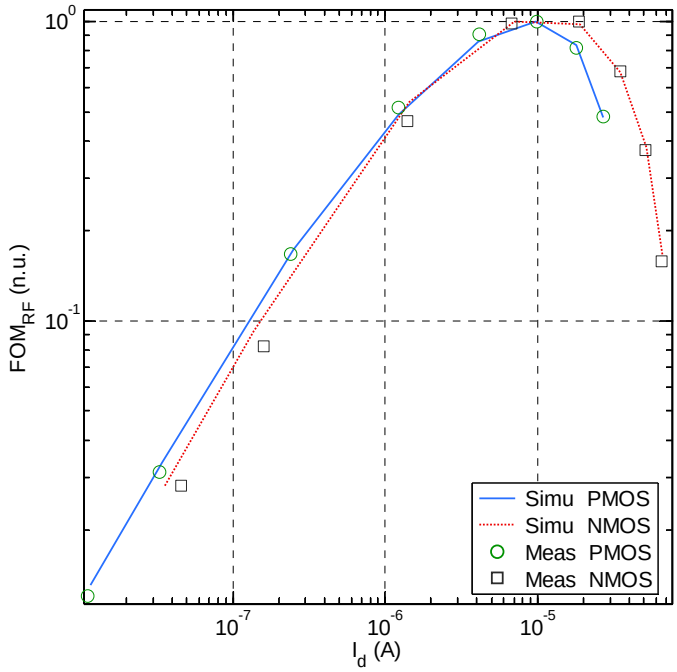



Fig. 4.31 $FoM_{RF}$ vs. $I_d$ in linear operation $|V_{DS}|$ = 0.3 V for NMOS and PMOS (L = 30 nm, $W_f$ = 2 µm and $N_f$ = 10) at T = 25°C.

## 4.5 Conclusion

In this Chapter we demonstrate that the proposed high frequency non-quasi-static model is well-suited for modeling UTBB FDSOI NMOS and PMOS RF and mm-Wave devices. Characterization conditions include length scaling down to nominal

value, a wide frequency range up to 110 GHz, and operation under different channel inversion levels down to low current and low voltage regime. An excellent agreement is shown over more than eight decades of current density for DC and four decades for RF and mm-Wave. The optimum operating point for low-power RF lies in the moderate inversion where our model is very well-suited. In particular, this Chapter demonstrates the accuracy of the proposed high frequency non-quasi-static model to enable RF/mm-Wave and Low Power circuit design applications in UTBB FDSOI technology.

# Chapter 5
# Transadmittance efficiency in presence of NQS effects

## 5.1 Introduction

RF CMOS based MOSFETs have been widely used in RF integrated circuits (RFIC) thanks to the geometry down-scaling. As seen in Chapter 1, critical issues related to short-channel effects have been mitigated using innovative architectures coupled with new materials [14]. The new architectures allow for higher level of integration and higher frequency operation of the CMOS technology. For analog and RF applications, the UTBB FDSOI technology has proven to be relevant, especially when power consumption matters [127]. UTBB FDSOI MOSFETs exhibit high analog and RF performances thanks to the reduced parasitic capacitances and resistances. Moreover, the independent back gate allows threshold voltage and channel mobility controls [41][127].

In this Chapter, the UTBB FDSOI MOSFET transconductance efficiency is generalized and studied at high frequency for different channel inversion levels. The main attention is paid to the impact of Non-Quasi-Static (NQS) effect on the transadmittance efficiency, and in particular how a proper choice of the normalization factors ends with simple representation of this fundamental figure of merit, with special focus on low-moderate inversion levels. The Chapter is organized as follows. The device architecture along with the high frequency characterization are described in Section 5.2. Next in Section 5.3 we discuss and validate experimentally the generalization of the transconductance efficiency (TE) concept in UTBB FDSOI MOSFETs derived at low frequency in Chapter 3 and published in [127]. The gate distribution effect is assessed and compared to channel NQS effect in Section 5.4, and an onset frequency of the channel NQS effect is defined and compared with transit

frequency in Section 5.5. The mobility in the silicon film is assessed using a novel method based on high frequency measurements after the compensation of the distributed gate effects in Section 5.7. Finally, discussion and conclusion are presented in Section 5.8 and 5.9, respectively.

## 5.2 Device description and characterization

Measured UTBB FDSOI MOSFETs were processed at STMicroelectronics. Si film, BOX and equivalent gate oxide thicknesses are 7 nm, 25 nm and 1.3 nm, respectively. More details on the process can be found in [127]. DC and C-V measurements are carried out to extract the device electrical parameters (e.g. threshold voltage $V_{TH}$, $K_p$, $C_{ox}$, etc.). In particular, the Inversion Coefficient (IC) is derived following the method proposed in Chapter 3. Multi-finger MOSFETs are embedded into CPW (Coplanar-Waveguide) transmission lines for high frequency characterization. After a standard short, open, matched load, and through (SOLT) calibration for reference plan definition, S-parameters are measured using ground-signal-ground (GSG) configuration probes up to a frequency of 110 GHz under several DC bias conditions. All transistor modes of operation are covered: non-saturation, saturation, weak inversion, moderate inversion and strong inversion. Measurements are de-embedded using Open-Short method. The gate lengths of the measured NMOS devices range from 28 nm to 1 µm while gate widths range from 200 nm to 5 µm.

## 5.3 Frequency dependence of the Transadmittance efficiency in long channel UTBB FD SOI MOSFETs

In [127], we have shown that the invariance of the transconductance efficiency, a well-known feature of bulk MOSFETs, remains valid for UTBB FD SOI MOSFETs despite these devices are controlled by two independent gates. This finding was not expected and constituted a major result per se. Besides the detrimental impact of the high channel inversion level upon the transconductance efficiency, this trend is amplified

with NQS operation, as shown in reporting the measured transadmittance efficiency modulus versus IC and operation frequency (F) (cf. Fig. 5.1).

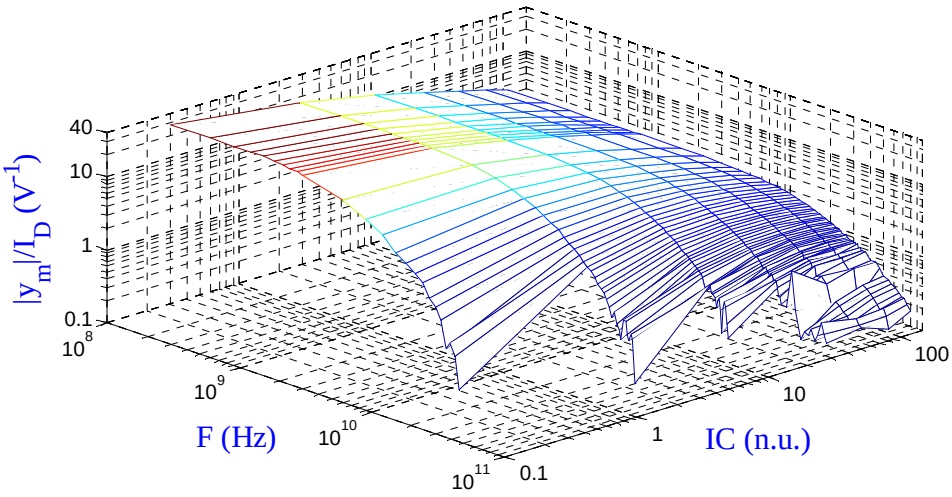



Fig. 5.1 3-D plot of the measured transadmittance efficiency modulus versus the frequency and inversion coefficient IC for L = 1 µm at $V_{DS}$ = 1 V.

On the other hand, a compact modeling approach to NQS operation of bulk MOSFETs was derived in [116], and a full dimensionless representation of a normalized transadmittance with respect to a normalized frequency led to a unique curve in the frequency domain [128] that could be used as a powerful abacus.

In this respect, we propose to investigate the front and back gates high frequency NQS behavior, and verify if this fundamental result still holds for UTBB FDSOI MOSFETs. As for the $g_m/I_D$ figure of merit [127], we define the transadmittance efficiency as:

$$TE_i = \frac{y_{mi}}{I_D} = \frac{y_{DG} - y_{GD}}{I_D} \tag{5.1}$$

where $y_{mi}$ is the mutual transadmittance defined as the difference between the gate-to-drain and drain-to-gate transadmittances, i.e. $y_{dg}$ and $y_{gd}$ respectively, $I_D$ is the DC drain current and IC is the inversion coefficient defined as [127]:

$$IC = \frac{I_D}{\frac{W}{L} \cdot I_{spec}} \tag{5.2}$$

where L, W and $I_{spec}$ are respectively the MOSFET length, width, and the 28 nm FDSOI technology current estimated for the front gate at $I_{spec} = I_1 = 0.7028$ µA when assuming W=L [127].

The transadmittance efficiency is a generalization of the transconductance efficiency defined at low frequency operation. At high frequency, the front or back gate transconductance is an imaginary number with a magnitude and phase. Since $g_{mi}$ represents the mutual interaction between the gate and drain [127], $y_{mi}$ keeps the same meaning even for high frequency (note that $y_{mi}$ reverts to $g_{mi}$ at low frequency). It should be noted that the capacitive coupling attributed to $C_{gd}$, which dominates $y_{DG}$ at high frequency, is ignored in the definition of $y_{mi}$, as $y_{GD} \approx -j\omega C_{gd}$ [97] in the low frequency limit. Then, $g_{mi}$ and $y_{mi}$ assess the gate control of the intrinsic MOSFET channel. At low frequency (quasi-static operation) we have [97]:

$$g_{mi} = real(y_{mi}) = |y_{mi}| \tag{5.3}$$

At any frequency, the $y_{mi}/I_D$ FoM determines the gain and phase shift for a given DC current $I_D$. The evolution of the Transadmittance efficiency versus frequency provides a very valuable insight in terms of power performances and efficiency at high frequency in presence of NQS effects.

As shown in Fig. 5.1, at high frequency, the NQS operation degrades the efficiency expected at low frequency, and in particular for weak and moderate inversion (IC < 10). This is also illustrated in Fig. 5.2, a side view of Fig. 5.1. The higher efficiency of the moderate and weak inversion modes (i.e. $g_{m1}/I_D > 10$) does not hold anymore beyond F = 4 GHz for L = 1 µm. Moreover, beyond 13 GHz and unlike low frequency operation, the strong inversion performs better with regards to the transadmittance efficiency. Plotting the integral of each curve in Fig. 5.2 over the interval [0, $F_{NQS}$] versus IC where $F_{NQS}$ is an onset frequency of NQS effect defined in (5.19) or (5.20), the maximum is found in SI (IC > 10) for L = 1 µm, while it is located in MI for L = 300 nm. This integral is a new FoM that we propose for the tradeoff between performance, power consumption, and speed.

$$FOM_{HF} = \int_0^{F_{NQS}} \frac{|y_{mi}|}{I_D} dF \tag{5.4}$$

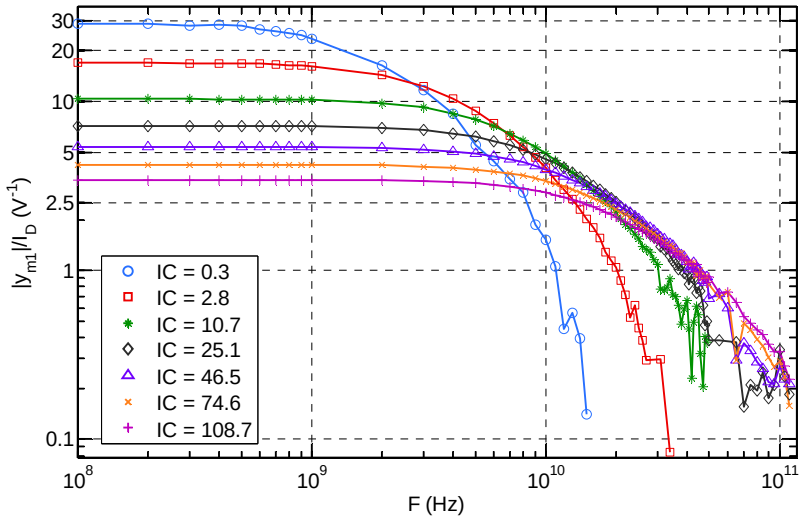



Fig. 5.2 Measured transadmittance efficiency modulus versus the frequency for different IC for a NMOS (L = 1 µm) in saturation ($V_{DS}$ = 1 V) and $V_{bG}$ = 0 V.

This FoM is more realistic than the previously defined $f_T.g_m/I_D$ in [126] since it does not assume that the transconductance vanishes beyond $f_T$ and does not underestimate performance in WI. In WI, $f_T$ is underestimating the onset of non-quasi static operation, i.e. the high frequency capability, since $F_{NQS}$ is a NQS critical frequency defined in Section 5.5. Actually, if we replace $f_T$ by the NQS critical frequency $F_{NQS}$ defined either in relations (5.19) or (5.20), the resulting FoM is higher in WI. Moreover, in contradiction to the previously reported conclusions such as in [126], the optimum is now located in SI for long channels, and no longer in moderate inversion. For shorter devices, the optimum is still located in MI, as already reported using the $f_T.g_m/I_D$ FoM. Fig. 5.3 shows the phase of the transadmittance efficiency versus frequency for various IC values. With respect to the modulus, the phase is more sensitive to NQS effects and particularly in weak inversion. At lower frequency (F < 500 MHz) and for IC = 0.3, the phase delay is more than 31° while the magnitude remains almost unaffected, i.e. 97 % of its DC value. For PMOS with lower carrier mobility, the phase shift degrades earlier with respect to frequency as observed for two PMOS lengths (i.e. L = 1 µm and L = 300 nm) shown in Fig. 5.4. Fig. 5.2 to Fig. 5.4 reveal that the effect of NQS transport on the transadmittance efficiency is gradual and depends on the channel inversion coefficient (IC). Having a clear definition for the onset frequency of NQS operation is

needed to provide a more realistic insight into the high frequency performance of MOSFETs.

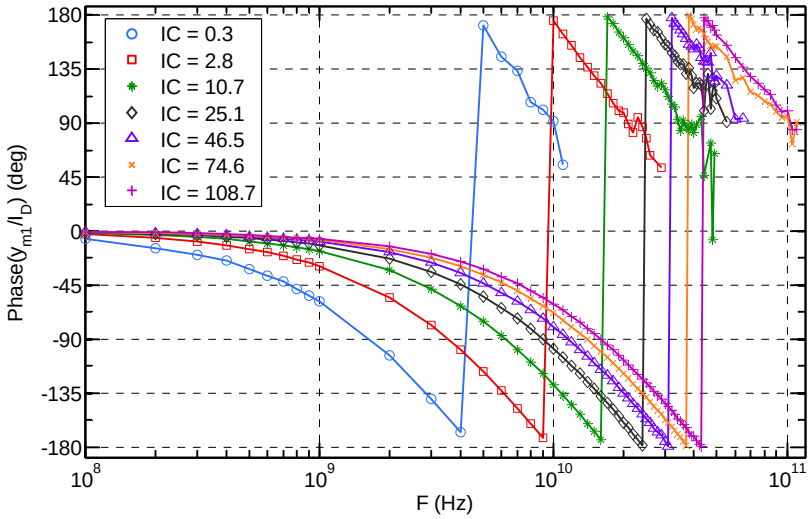



Fig. 5.3 Measured phase of the transadmittance over $I_D$ versus frequency at different IC for NMOS (L = 1 µm) in saturation ($V_{DS}$ = 1 V) and $V_{bG}$ = 0 V.

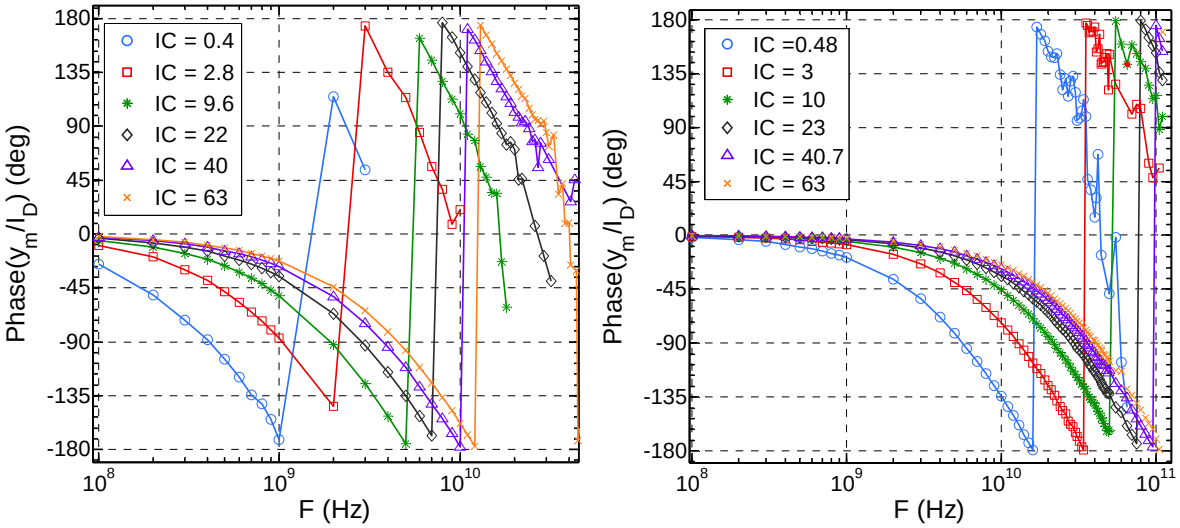



Fig. 5.4 Measured phase of the transadmittance over $I_D$ versus frequency at different IC for PMOS L = 1 µm (left) and L = 300 nm (right) in saturation ($V_{DS}$ = -1 V) and $V_{bG}$ = 0 V.

Exact small signal analytical expressions for NQS operation are presented in [116] for single gate bulk MOSFETs and simplified in [128] to derive a compact model. The critical frequency $F_{crit}$ expression, which corresponds to the first pole of the

frequency characteristic of the device, as a function of the inversion coefficient IC concept redefined in [127] for a DG UTBB FDSOI MOSFET is:

$$\mathrm{F}_{crit} = \frac{1}{2\pi}\frac{15}{4}\cdot\frac{\mu U_T}{L^2}\cdot\frac{2+6\,IC+3\sqrt{IC+\frac{1}{4}}+4\left(\sqrt{IC+\frac{1}{4}}\right)^3}{1+2\,IC+3\sqrt{IC+\frac{1}{4}}} \tag{5.5}$$

$$\approx \frac{15}{4\pi}\times\frac{\mu U_T}{L^2}\cdot\sqrt{IC}\ \ (\text{in SI}) \tag{5.6}$$

where μ and $U_T$ are respectively the effective mobility and the thermal voltage. (5.6) is an approximation of (5.5) while neglecting smaller terms in strong inversion, with less than 1 % error on $F_{crit}$ for IC > 2.

The model reported in [128] proposed a frequency normalization scheme using the first pole obtained from the first order approximation of the NQS model of bulk MOSFETs.

It should be noted that $F_{crit}$ is proportional to the effective mobility and $U_T$, inversely proportional to the square of gate length and accounts for the dependence of NQS on the inversion coefficient IC. This critical NQS frequency will be used for frequency normalization hereafter.

The transadmittance efficiency in saturation is derived from [128] as :

$$\frac{y_{m1}}{I_D} = \frac{g_{m1}}{I_D}\xi_m\left(\frac{F}{F_{crit}}, IC\right) \tag{5.7}$$

where $g_{m1}$ is the low frequency front gate transconductance, $I_D$ is the DC drain current, F is the operation frequency, $F_{crit}$ is given in (5.5), and $\xi_m$ is a NQS small-signal function based on the first kind Bessel functions. Defining the critical time as:

$$\tau_{crit} = \frac{1}{2\pi\cdot F_{crit}} \tag{5.8}$$

An approximation of (5.7) using the first pole of $\xi_m$ becomes:

$$\frac{y_{m1}}{I_D} = \frac{g_{m1}}{I_D}\frac{1}{(1+j\omega\tau_{crit})} \tag{5.9}$$

where ω is the angular frequency (=2πF).

In Fig. 5.5, a normalized magnitude of the transadmittance efficiency $(|y_{m1}|/I_D)_{norm}$ is shown for various values of IC versus the normalized frequency $F_{norm1}$:

$$F_{norm1} = \frac{F}{F_{crit}} \tag{5.10}$$

In addition, a further normalization of $|y_{m1}|/I_D$ is applied using the low frequency transconductance efficiency $g_{m1}/I_D$ as follows:

$$\left(\frac{|y_{m1}|}{I_D}\right)_{norm} = \left(\frac{|y_{m1}|}{I_D}\right)/(g_{m1}/I_D) \tag{5.11}$$

All normalized moduli plotted in Fig. 5.5 from weak to strong inversion are almost superposed as a result of the frequency normalization in (5.10) (despite the very high frequency disturbance of the parasitic elements). The invariance is also evidenced for the phase in Fig. 5.6 up to a phase shift as large as 270°.

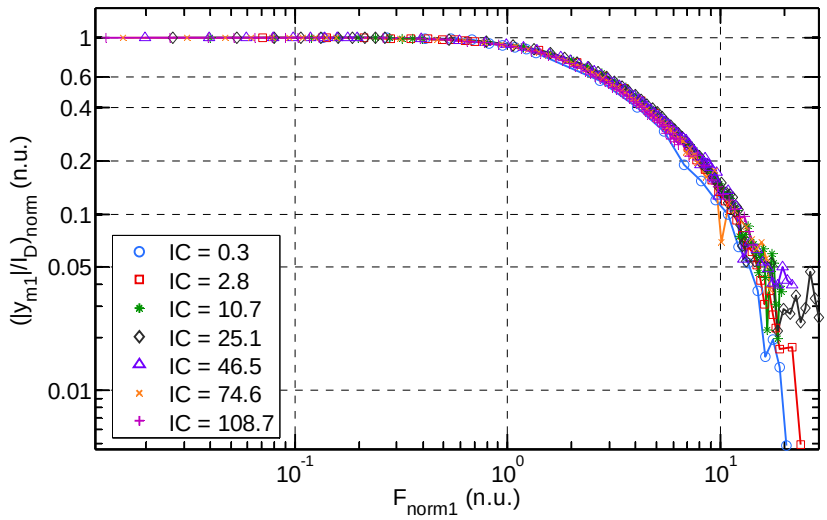



Fig. 5.5 Normalized transadmittance magnitude over $I_D$ versus normalized frequency $F_{norm1}$ at different IC for NMOS (L = 1 µm & W = 1 µm) in saturation ($V_{DS}$ = 1 V) and $V_{bG}$ = 0 V (Measurements).

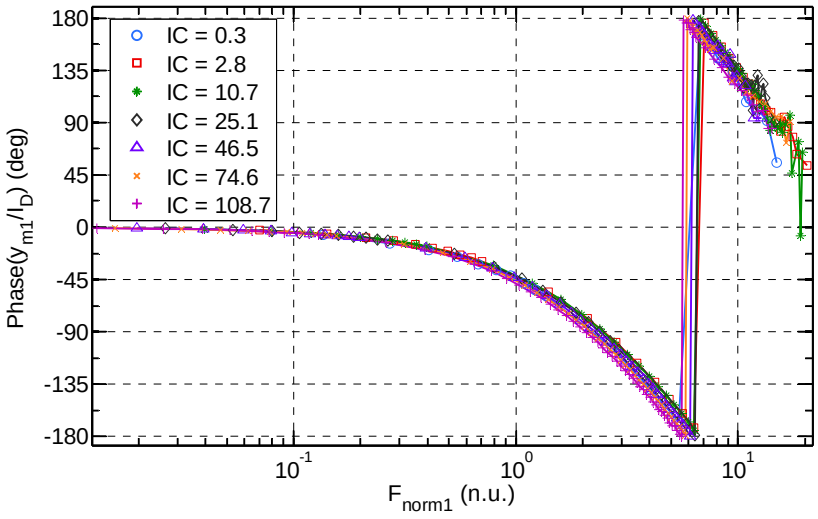



Fig. 5.6 Phase of the transadmittance over $I_D$ versus normalized frequency $F_{norm1}$ at different IC for NMOS (L = 1 µm & W = 1 µm) in saturation ($V_{DS}$ = 1 V) and $V_{bG}$ = 0 V (Measurements).

These results are of prime importance for modeling NQS effects in UTBB SOI FETs. For the first time, a simple but powerful analytical model can predict the gate transconductance, magnitude and phase, during highly non static operation of the intrinsic channel and in all the regions of operation. Additional normalizations in terms of the inversion coefficient and critical frequency were used to derive a kind of abacus, paving the way to a simple and efficient HF design methodology where device parameters, biasing conditions and frequency are treated on the same ground.

## 5.4 Impact of distributed effects along the gate on NQS

In this Section and Section 5.5, we will investigate the breakdown of the normalized transadmittance efficiency invariance shown in Section 5.3. In particular, we will study the impact of both the distributed effects along the gate and mobility variation (Section 5.7) on the critical frequency $F_{crit}$ used for normalization.

A closer look at the curves in the constant mobility normalization depicted in Fig. 5.6 reveals that in SI regime the transadmittance efficiency decreases earlier than in WI while frequency increases. This means that the transadmittance efficiency lags behind the gate voltage excitation in an enhanced manner. This enhanced phase shift in SI can be explained by a decrease in the mobility or an additional delay caused by

the gate distributed effect. In our previous normalizations (Fig. 5.5 and Fig. 5.6), the delay generated by the 1 µm gate finger length (gate width) was not taken into account.

At high frequency, the gate can be considered as a transmission line because of the limited electromagnetic wave velocity along the gate finger length. An estimation of the time constant of the distributed gate finger is given by [129]:

$$\tau_g = R_{gg} C_{gg} \tag{5.12}$$

where $R_{gg}$ and $C_{gg}$ are gate resistance and average gate capacitance respectively. It should be noted that $C_{gg}$ depends on the level of inversion, which could explain the lower critical frequency in SI case when gate distributed effect is important. Conversely, in weak inversion $C_{gg}$ is lower and a higher critical frequency is expected. According to [130][117], we have:

$$R_{gg} = \frac{R_g}{\eta} \tag{5.13}$$

where η is equal to 3 for a single-side connected gate and is equal to 12 for a double-side connected gate. $R_g$ is the resistance of the MOSFET finger at low frequency (i.e. without the distributed effect) and extracted in SI. If we consider the additional pole due to the gate distributed effect, the total time constant can be expressed as:

$$\tau_{tot} = \tau_{crit} + \tau_g \tag{5.14}$$

This time constant includes both distributed effects occurring along the channel (i.e. NQS) and through the gate. Thus, the new critical frequency is given by:

$$F_{tot} = \frac{1}{2\pi \cdot (\tau_{crit} + \tau_g)} \tag{5.15}$$

Finally, neglecting the higher order term in the denominator and using the same approach, the transadmittance efficiency expression given in (5.9) becomes:

$$\frac{y_{m1}}{I_D} \approx \frac{g_{m0}}{I_D} \frac{1}{1 + j\omega(\tau_{crit} + \tau_g)} \tag{5.16}$$

In order to include the distributed gate delay in the normalization scheme, a new frequency normalization is also used, still considering a constant mobility. The normalized frequency considering both non static transport (channel and distributed gate) is now given by:

$$F_{norm2} = \frac{F}{F_{tot}} \tag{5.17}$$

Considering the error on the frequency prediction at a given phase shift, for L = 1 µm, the normalization using $F_{norm2}$ (not shown here) results in a discrepancy of the predicted frequency for a 45° phase shift of less than 15 % (5 % enhancement versus Fig. 5.6) as gate distributed effects are less important in comparison to NQS effect. This residual discrepancy could be explained by a mobility varying versus IC, which would be estimated at about 15 % between WI and SI for a long channel (i.e. L = 1 µm). Conversely, the error on the phase shift prediction for a given frequency is less than 6 %.

For L = 300 nm, the normalization using either $F_{crit}$ or $F_{tot}$ leads to similar conclusions as for the L = 1 µm case. Fig. 5.7 shows the phase shift for L = 300 nm MOSFET versus frequency. Based on the apparent critical frequency, the dominant distributed effect is the channel NQS. In Fig. 5.8, the frequency is normalized using $F_{norm1}$ to account for the channel NQS effect. Clearly, the gate distributed effect is evidenced since a higher inversion coefficient is responsible for earlier more pronounced phase shift. This behavior cannot be attributed to the channel where higher IC moves the phase shift to higher frequencies.

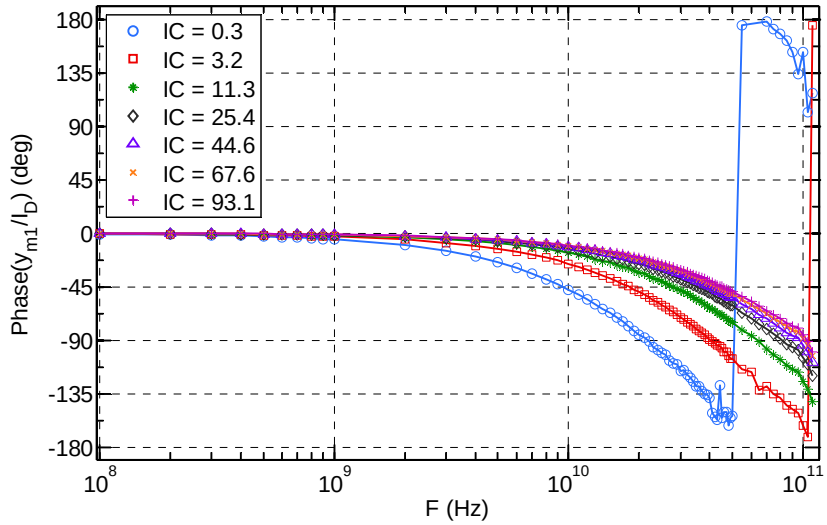



Fig. 5.7 Phase of the transadmittance over $I_D$ versus frequency at different IC for NMOS (L = 300 nm & W = 1 µm) in saturation ($V_{DS}$ = 1 V) and $V_{bG}$ = 0 V (Measurements).

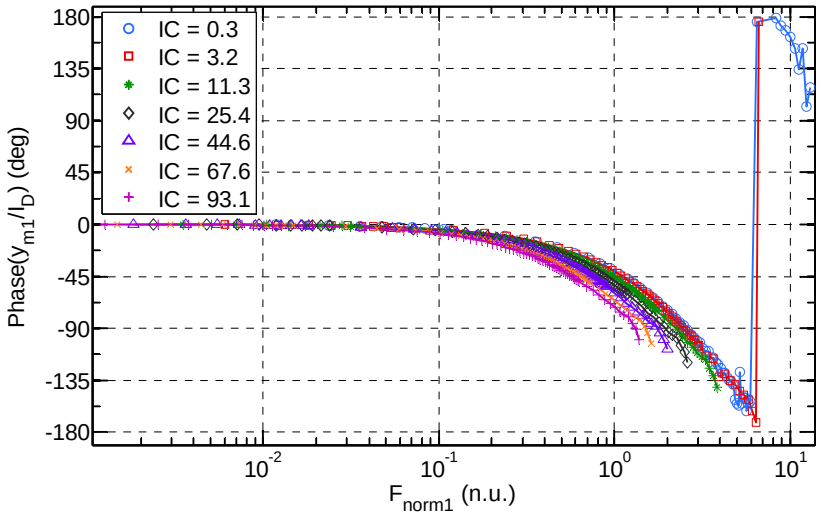



Fig. 5.8 Phase of the transadmittance over $I_D$ versus normalized frequency $F_{norm1}$ with constant mobility at different IC for NMOS (L = 300 nm & W = 1 µm) in saturation ($V_{DS}$ = 1 V) and $V_{bG}$ = 0 V (Measurements).

In Fig. 5.9, a second normalization is introduced using $F_{tot}$ instead of $F_{crit}$ in order to account for the gate distributed delay. As a result, the discrepancy of the predicted frequency for a 45° phase shift is reduced to less than 14 % as shown in Fig. 5.10. It should be noted that the error on the predicted phase at a given frequency is less than 6 %. Again, the remaining mismatch could be explained by a variation in the mobility with the gate voltage. This point will be briefly investigated in 5.7.

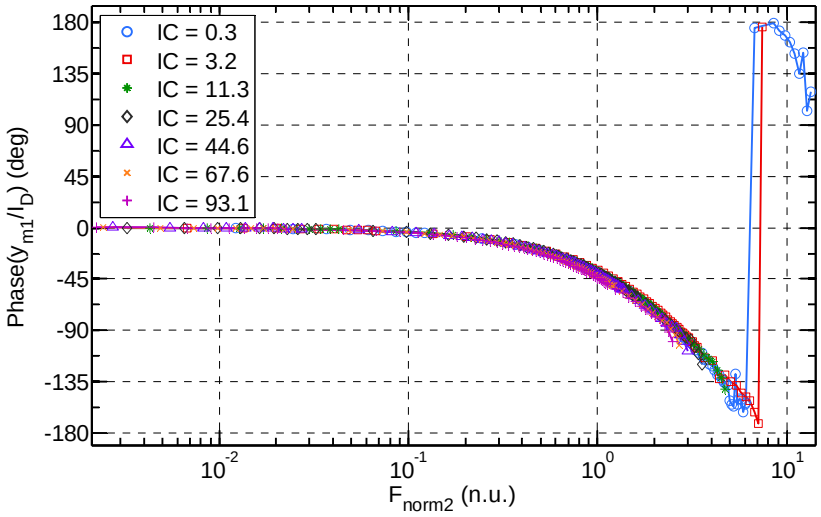



Fig. 5.9 Phase of the transadmittance over $I_D$ versus normalized frequency $F_{norm2}$ with constant mobility at different IC for NMOS (L = 300 nm & W = 1 µm) in saturation ($V_{DS}$ = 1 V) and $V_{bG}$ = 0 V (Measurements).

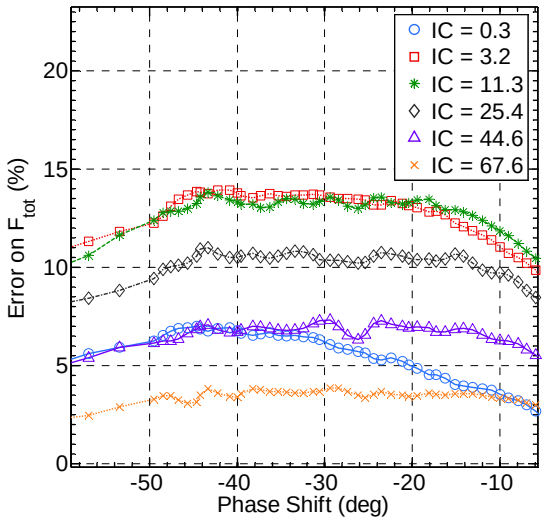



Fig. 5.10 Frequency error versus phase shift after normalization using $F_{tot}$ (IC = 93.1 is taken as a reference)

For shorter devices, the distributed RC gate delay can dominate the channel NQS effect. This is evidenced on the phase delay versus the real frequency for the 28 nm and 1 µm channel lengths displayed respectively in Fig. 5.11 and Fig. 5.3. In the short device, the inversion level (IC) seems to have minimal impact on the critical frequency, see Fig. 5.11, and the two counter effects almost compensate each other. Moreover, for P type MOSFET, the curves almost merge in Fig. 5.12. The gate distributed delay seems to slightly take over since the phase shift happens earlier when

IC is increased, which should not be if the channel would still be the bottleneck in terms of delay.

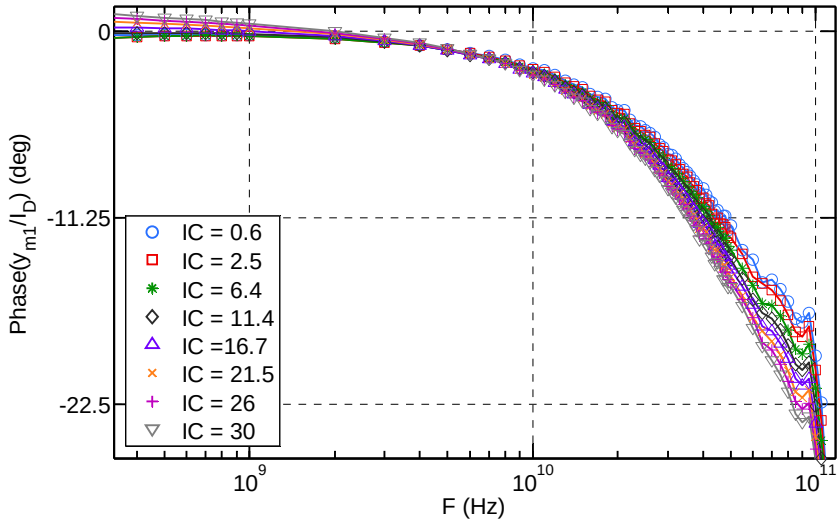



Fig. 5.11 Measured phase of the transadmittance over $I_D$ versus frequency at different IC for NMOS (L = 28 nm & W = 1 µm) in saturation ($V_{DS}$ = 1 V) and $V_{bG}$ = 0 V.

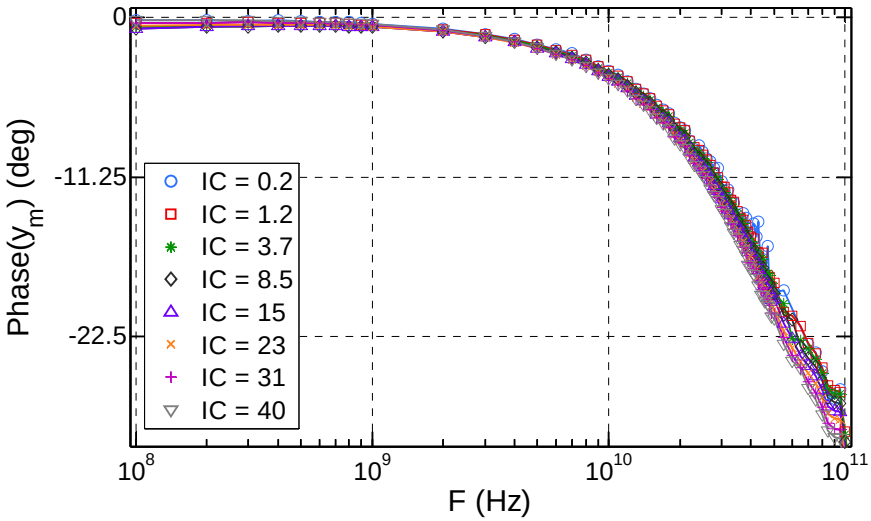



Fig. 5.12 Measured phase of the transadmittance over $I_D$ versus frequency at different IC for PMOS (L = 28 nm & W = 1 µm) in saturation ($V_{DS}$ = -1 V) and $V_{bG}$ = 0 V.

To follow up with the normalization scheme, we calculate the 'intrinsic channel normalization frequency' $F_{norm1}$ from relation (5.10) and plot the phase shift accordingly in Fig. 5.13. Whereas for 'long' channels, this first normalization almost condenses the bunch of curves in a single one (see Fig. 5.6 and Fig. 5.8), here it spreads out in very different characteristics. The gate distributed effect could explain this dispersion. Fig. 5.14 shows the phase shift for the 28 nm channel length device when using the

normalization frequency $F_{norm2}$ as given from (5.17) which now includes the first order distributed effect originating from the gate. The way the different characteristics are distributed in a narrow region which is in favor of the predominance of the enhanced gate delay in short channel devices.

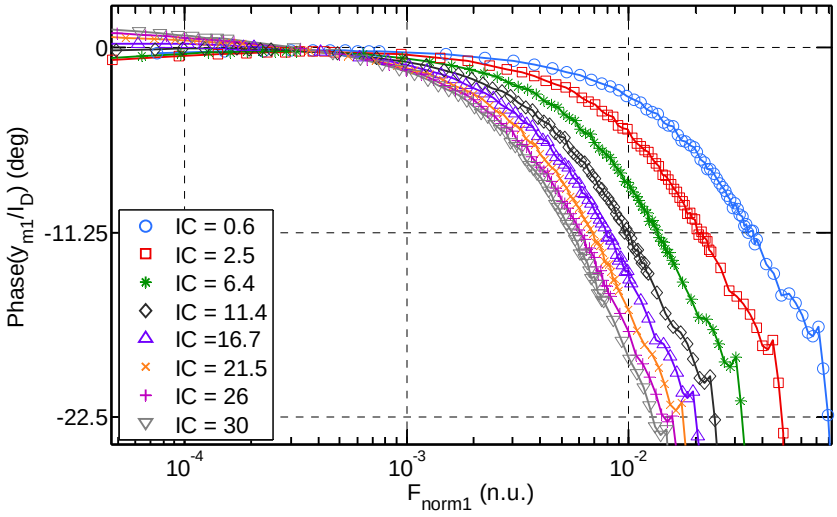



Fig. 5.13 Phase of the transadmittance over $I_D$ versus the normalized frequency $F_{norm1}$ estimated with a constant mobility at different IC for NMOS (L = 28 nm & W = 1 µm) in saturation ($V_{DS}$ = 1 V) and $V_{bG}$ = 0 V (Measurements).

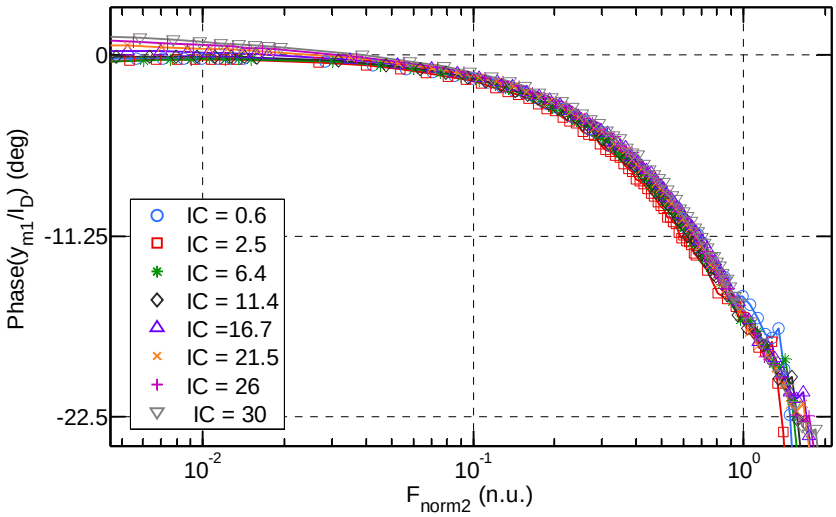



Fig. 5.14 Phase of the transadmittance over $I_D$ versus normalized frequency $F_{norm2}$ with constant mobility at different IC for NMOS (L = 28 nm & W = 1 µm) in saturation ($V_{DS}$ = 1 V) and $V_{bG}$ = 0 V (Measurements).

## 5.5 Onset of NQS effects

Significant NQS effects pop up when the operation frequency reaches the critical frequency $F_{crit}$ defined in (5.5). In particular, a phase shift greater than 45° is measured at this characteristic frequency, meaning that $F_{crit}$ overestimates the onset of the NQS effect. To our knowledge, no clear definition is given for the emergence of NQS transport. Usually, the concept of transit frequency $f_T$ is used, i.e. the frequency where the modulus of the current gain $H_{DG}$ falls to unity, and the NQS frequency is often defined as being proportional to $f_T$ [97]. However, this definition relies on the low frequency transconductance $g_m$, and therefore is implicitly a quasi-static definition. In order to assess the relation between $f_T$ and the NQS critical frequency, the current gain is plot for several IC values with respect to the normalized $F_{norm1}$ frequency.

Fig. 5.15 shows the magnitude of the current gain $H_{DG}$ as a function of the normalized frequency $F_{norm1}$ for various IC and for a channel length of L = 1 µm. The current gain $H_{DG}$ is defined for a 2-port structure as:

$$H_{DG} = \frac{I_D}{I_G}\Big|_{V_D=0} = \frac{y_{DG}}{y_{GG}} \tag{5.18}$$

where $I_D$ and $I_G$ are the current phasors across port-2 (drain) and port-1 (front gate), respectively. $V_D$ is the voltage across port-2, which is matched in this case. $H_{DG}$ is frequently used to extract the transit frequency of the transistor. The transit frequency $f_T$ is defined as the frequency at which the magnitude of $H_{DG}$ becomes equal to unity (i.e. 0 dB). $f_T$ is proportional to $F_{crit}$ in MI and SI as can be expected from (5.6) and (5.2), and noting that $f_T$ is proportional to the square root of the drain current provided that velocity saturation is ignored. However, for WI, the proportionality is less valid, which is expected knowing that $F_{crit}$ becomes constant in WI while $f_T$ remains proportional to IC. If we use the SI approximation (5.6) for the frequency normalization for all the levels of inversion with L = 1 µm, all $|H_{DG}|$ plots are superimposed for various IC values, including WI regime, as shown in inset of Fig. 5.15. This suggests that transit frequency is proportional to the square root of the current all the way from WI to SI.

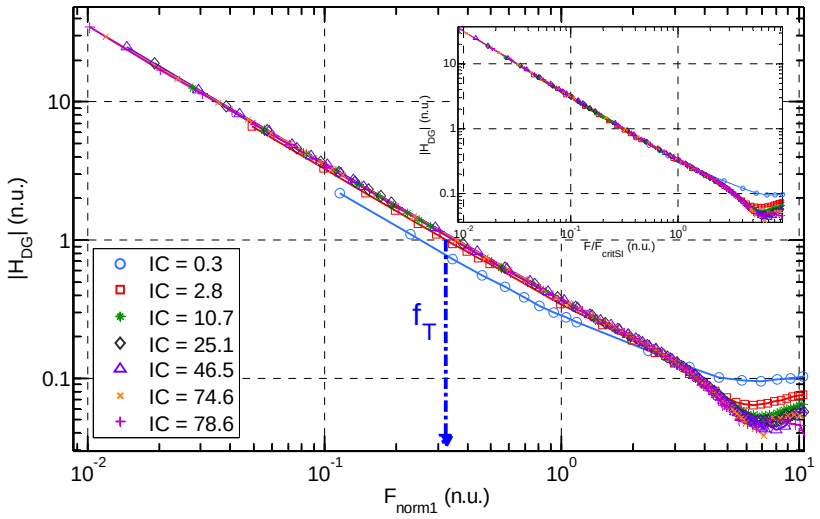



Fig. 5.15 Measured $|H_{DG}|$ versus normalized frequency $F_{norm1}$ at different IC for NMOS (L = 1 µm & W = 1 µm), ($V_{DS}$ = 1 V) and $V_{bG}$ = 0 V. Inset shows $|H_{DG}|$ versus $F/F_{critSI}$ where $F_{critSI}$ is given by (5.6).

Therefore, the proportionality between the onset of NQS frequency and $f_T$ holds only in SI. In WI and practically in MI, the rules of thumb based on proportionality to $f_T$ underestimates the critical NQS frequency. Depending on the criteria invoked, we propose to use two expressions for the onset of device distributed effects:

- 10° phase shift of the transadmittance efficiency:

$$F_{NQS10°} = \frac{1}{2\pi}\frac{\tan\frac{\pi}{18}}{\frac{1}{2\pi \cdot F_{crit}} + \frac{R_g}{\eta}\cdot C_{gg}} \tag{5.19}$$

- 3% decrease in the transadmittance efficiency magnitude from the low frequency value:

$$F_{NQS3\%} = \frac{1}{2\pi}\frac{0.25}{\frac{1}{2\pi \cdot F_{crit}} + \frac{R_g}{\eta}\cdot C_{gg}} \tag{5.20}$$

Note that $F_{NQS3\%}$ is practically equal to $f_T$ in SI and, higher in WI and MI.

## 5.6 Back gate control

In a DG UTBB MOSFET, the independent back gate voltage controls the threshold voltage and consequently IC. The back gate also influences the apparent mobility of the carriers in the silicon film thanks to the volume inversion in low electrical field condition. This fact is already evidenced in Chapter 3 and also validated by the Transit Frequency $f_T$ extracted using 4-port measurements and shown in Fig. 5.16. For L = 100 nm a higher measured maximum $f_T$ (119 GHz) is achieved for $V_{bG}$ = 2 V in comparison to the $V_{bG}$ = 0 V case for same IC values. The 6% high frequency performance enhancement is expected to be greater for longer devices.

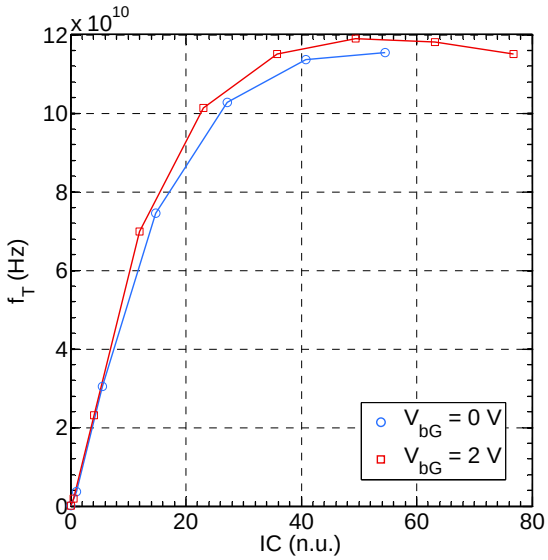



Fig. 5.16 Transit frequency $f_T$ versus IC at two different back gate voltages $V_{bG}$ (blue: $V_{bG}$ = 0 V and red: $V_{bG}$ = 2 V) for NMOS (L = 100 nm) in saturation ($V_{DS}$ = 1 V) (4-port Measurements).

Therefore, as the NQS characteristic frequency $F_{crit}$ is dependent on both mobility and IC, we expect an impact of the back gate voltage on NQS effects. In this section, this impact is assessed using TCAD simulations for various back gate voltages and for fixed front gate voltage for the front gate transadmittance efficiency on the one hand and for the back gate transadmittance efficiency on the other hand. TCAD simulations were used to avoid tedious deembedding steps of the 4-port structures measurements that provide an independent access to the back gate terminal.

### 5.6.1 Front gate transadmittance efficiency

Fig. 5.17 shows $|y_{m1}|/I_D$ versus frequency for various back gate voltages $V_{bG}$ and fixed front gate voltage $V_{GS}$ = 0.5 V. A constant mobility of $\mu_0$ = 1.417E3 $cm^2/Vs$ is used. Forward back gate bias enhances IC and consequently the frequency at which the NQS effect becomes important at the cost of a decrease in the transadmittance efficiency. In Fig. 5.18 and Fig. 5.19, the normalization $F_{norm1}$ is used showing accurate prediction of NQS effects for all levels of inversion, both in modulus and phase. Likewise for the front gate analysis, a further normalization of the modulus ($|y_{m1}|/I_D$) is applied using the low frequency transconductance efficiency $g_{m1}/I_D$. It should be noted that in TCAD simulations no gate distributed effect is taken into account.

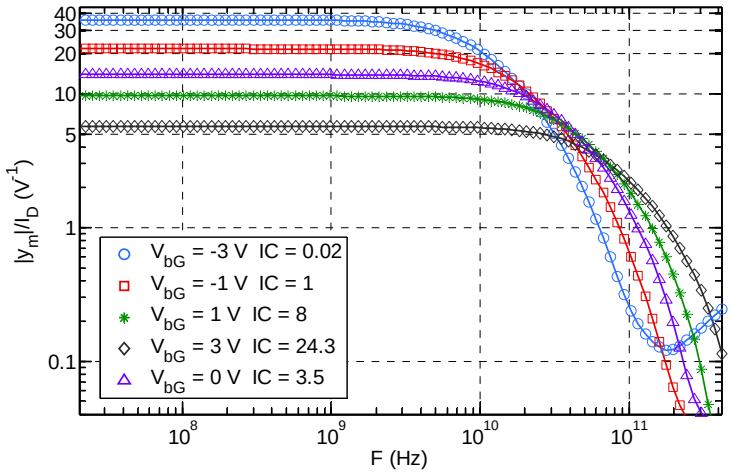



Fig. 5.17 Simulated transadmittance efficiency modulus versus frequency at different $V_{bG}$ for NMOS (L = 1 µm) in saturation ($V_{DS}$ = 1 V) and $V_{GS}$=0.5V (TCAD).

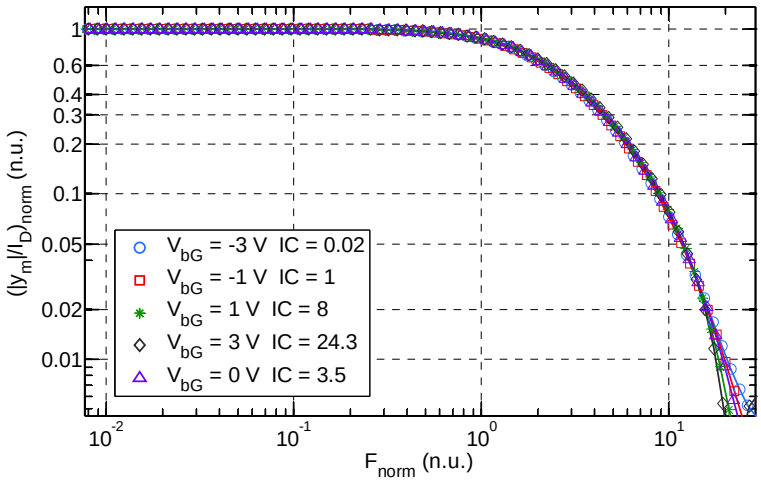



Fig. 5.18 Normalized transadmittance efficiency modulus versus normalized frequency $F_{norm}$ at different $V_{bG}$ for NMOS (L = 1 µm) in saturation ($V_{DS}$=1V) and $V_{GS}$ = 0.5 V (TCAD).

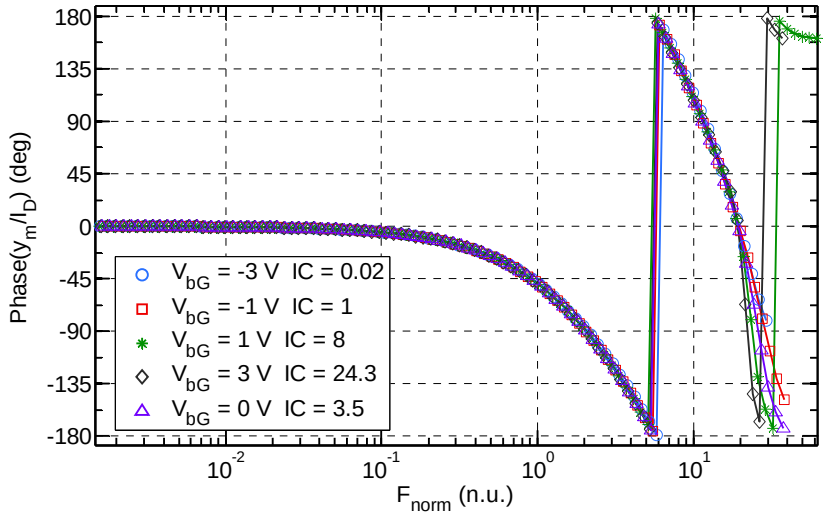



Fig. 5.19 Simulated phase of the transadmittance efficiency versus normalized frequency $F_{norm}$ at different $V_{bG}$ for NMOS (L = 1 µm) in saturation ($V_{DS}$= 1V) and $V_{GS}$ = 0.5 V (TCAD).

## 5.6.2 Back gate transadmittance efficiency

In the UTBB FDSOI MOSFET, an input small signal can also be applied to the back gate to modulate the channel. In order to evaluate the back gate performance at high frequency, as in [127], the transadmittance efficiency of the back gate is now assessed for a fixed front gate voltage $V_{GS}$ = 0, and for various inversion levels imposed by the back gate (various $V_{bG}$). Fig. 5.20 shows the phase of the transadmittance efficiency of the back gate at $V_{GS}$ = 0 V. In this case, the channel is located in all the volume of the silicon film. Again, after applying the same normalization for the frequency and transconductance to current ratio, a unique plot is obtained in Fig. 5.21. This closes the loop on the normalization scheme used to predict non static transport in UTBB FDSOI MOSFETs.

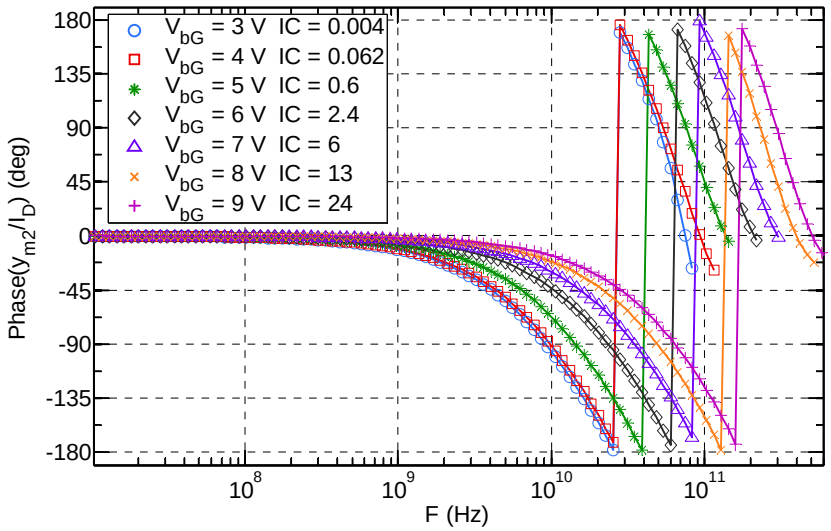



Fig. 5.20 Simulated phase of the back transadmittance efficiency versus frequency at different $V_{bG}$ for NMOS (L = 1 µm) in saturation ($V_{DS}$ = 1 V) and $V_G$ = 0 V (TCAD).

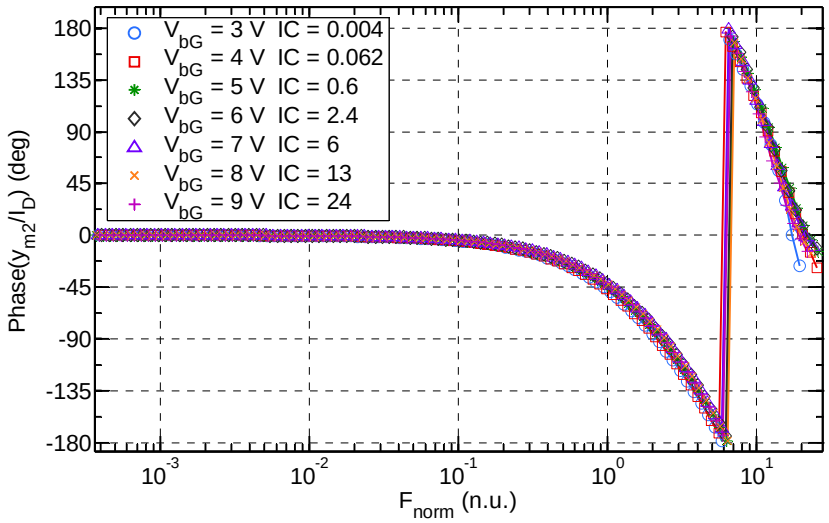



Fig. 5.21 Simulated phase of the back transadmittance efficiency versus normalized frequency $F_{norm}$ at different $V_{bG}$ for NMOS (L = 1 µm) in saturation ($V_{DS}$ = 1 V) and $V_G$ = 0 V (TCAD).

## 5.7 Channel Mobility extraction using NQS effect

As shown in Fig. 5.6, the channel NQS related normalization (5.10) leads to a more or less unique curve. Actually, after the normalization in (5.10), we still get a discrepancy of the NQS effect critical frequency $F_{crit}$ of about 15% while using a constant mobility (µ = 240 cm$^2$/Vs) for all levels on inversion. According to (5.5), the observed $F_{crit}$ discrepancy is caused by a rather variant mobility, a variant length or an inaccurate IC. The two aftermost causes are unlikely to happen, that is in one hand,

the length L = 1 µm is considered long in advanced technologies and accurately extracted, on the other hand, Inversion Coefficient IC is based on a technology current derived from accurate extraction of the product $\beta_1 = n_1.C_{ox1}.\mu_1$ [127]. However, the mobility extraction is still subject to intensive research and usually considered as gate voltage dependent [131][132]. Two major challenges are faced in the mobility extraction: one is the limitation of the empirical SI model based on gate voltage overdrive and the other is the difficulty to extract the inversion charge based on capacitance measurements in weak and moderate inversion regimes. In this research work, the proposed mobility extraction method is compared to two other methods namely the classical Y function with iterative corrections as in [131] and the Lambert-W function based method proposed in [132]. The Y function based method is first used to retrieve the mobility dependence in order to replace the constant mobility in (5.5) by an IC dependent mobility. The normalization using $F_{norm2}$ and a variant mobility (extracted using Y-function method [131]) leads to a better $F_{crit}$ alignment for the various IC values with less than 4% discrepancy on the normalized plots for long and short geometries.

$F_{tot}$ remaining discrepancy observed in Fig. 5.9 is due to a mobility variation of 15-19 % illustrated in Fig. 5.22 ($F_{crit}$ + distr. gate corr.) and compared against the mobility extracted using $f_T$ expression taken from [126], Y-function and Lambert-W function. The mobility slightly decreases in WI and SI, and has a maximum corresponding to IC ≈ 4 which corroborates the findings in [127]. This apparent mobility variation is due to the low transverse field influence on volume inversion. Neither the Y function based mobility extraction nor the Lambert-W Split C-V based extraction predict mobility in WI. The Lambert-W Split C-V function based extraction methodology underestimates mobility values in MI and WI levels because of a difficult estimation of the inversion charge in this region. Our method provides comparable results to the extraction using magnetoresistance characterization [133].

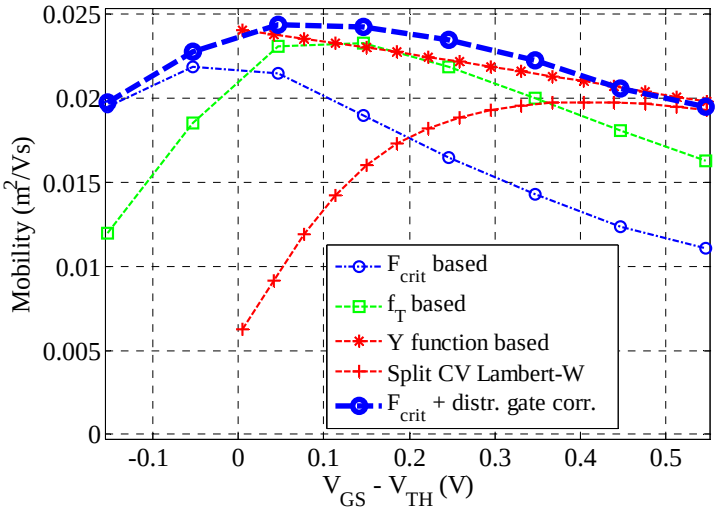



Fig. 5.22 Mobility versus gate voltage overdrive for L = 0.3 µm extracted using various methods: $F_{crit}$ based, $f_T$ based, classical Y function with iteration, Lambert-W Split C-V based, and $F_{crit}$ based with correction of the distributed gate effect.

## 5.8 Discussion

The NQS critical frequency $F_{crit}$ for a single gate bulk MOSFET developed in [116][128] holds for a DG MOSFET, including with asymmetric operation. In particular, the normalization of the frequency leads to almost unique charts for long channel devices allowing fast and accurate high frequency performance assessment. Moreover, the invariance is also confirmed for short channel devices with a dominant gate distributed effects provided that the related time constant is taken into consideration. The transadmittance efficiency concept defined in this Chapter provides deep insight into high frequency UTBSOI MOSFET behavior and an estimation of the limiting MOSFET characteristic frequencies. The critical channel NQS frequency depends on the device length, free carrier mobility and inversion coefficient IC. The gate distributed effect, in turn, depends on the gate resistance and capacitance. The frequency normalization using the distributed gate time constant generalizes the normalization scheme by merging the longitudinal (gate) distributed effect with the channel NQS effect. The invariant normalized transadmittance efficiency versus normalized frequency was confirmed extensively with both measured and simulated data. This novel approach provides a way to calculate the critical frequency beyond which the gain and the phase will be affected.

In Analog and RF design, oversimplified rules of thumb are used and bias the analysis. For instance, stating that operating frequency should be lower than $f_T/10$ or $f_T/3$ is encouraging the designer to choose shortest MOSFETs while introducing detrimental mismatch and SCE, especially Drain Induced Barrier Lowering (DIBL). Such a rule of thumb can be overlooked using the transadmittance efficiency charts and critical frequency expressions developed in this Chapter and introducing the Inversion Coefficient concept as in [127]. Then, knowing $F_{crit}$ versus the channel length and DC operating point, the optimum geometry can be selected unambiguously.

At high frequency, beyond the transit frequency $f_T$, charge carriers oscillate in the channel with a delay versus the applied gate voltage oscillation leading to what we generally call Non-Quasi-Static effect. The mobility term in $F_{crit}$ expression (5.5) is an effective mobility of carriers that do not reach the source side and consequently with less degradation due to access resistance. This explains why the mobility extracted using $F_{crit}$ expression is rather higher compared to classical extraction methods. The mobility extraction using $F_{crit}$ is more straightforward than using I-V and C-V measurements where series resistances miserably impact the extraction leading to incoherent mobility values without a careful estimation of the series resistances.

## 5.9 Conclusion

In this Chapter, we have shown that the frequency normalization using a critical frequency and taking into account lateral and longitudinal MOSFET distributed effects offers a practical insight to help high frequency performance assessments of UTBB FDSOI MOSFETs through a powerful normalization scheme. We have experimentally shown that frequencies of interest at which MOSFET distributed effects occur can be predicted using simple analytical expressions which are valid down to 28 nm channel length. The NQS critical frequency is also used for the mobility extraction. The proposed method provided comparable values to the classical methods in SI. In WI, in contradiction to the classical methods, the proposed method revealed that mobility is remaining at the same levels compared to stronger inversion levels.

The normalization scheme is application to whatever the gates length and DC biasing, and supports the very general character of the NQS analysis proposed in this research work.

# Part III

# RF Design application

# Chapter 6

# RF and mm-Wave design application

## 6.1 Introduction

More and more wireless devices and IoT building blocks rely on CMOS analog and RF circuits to efficiently interact with the physical world. Thanks to the geometry down-scaling, CMOS MOSFETs have been widely used in low-cost and low-power RF integrated circuits (RFIC). Short-channel related issues, as side effects of the geometry shrink, have been controlled using new architectures and new materials [4][3]. As stated earlier, the new architectures allow for excellent electrostatic control [26].

Clearly the UTBB FDSOI technology has proven to be suitable for Analog and RF applications, especially when both power consumption and performance are valued equally. UTBB FDSOI MOSFETs exhibit high analog and RF performances thanks to the reduced parasitic capacitances and resistances [14]. Moreover, the independent back gate provides an interesting degree of freedom that allows tradeoff between power consumption and performance [41][127].

Several circuit-topology-based techniques such as current reuse are proposed in analog design to optimize performance and power consumption [134]. These techniques are out of this research work scope. In this Chapter, the UTBB FDSOI characteristics are used for first-cut analog sizing method. In particular, the transconductance efficiency versus inversion coefficient (IC) studied in Chapter 3 is used to determine the width of the MOSFET while the transit frequency ($f_T$) versus IC charts are used for length selection. The design method, using relaxed length and Moderate Inversion regime, provides a valuable tradeoff between gain, power consumption and performance while MOSFET width is kept reasonably large and short channel effects are mitigated. An eye is also kept on passive devices limitations from the very beginning of the sizing flow.

This Chapter is organized as follows. First, the classical analog design methods, based on inherited rules of thumb, are briefly discussed in Section 6.2. Second, the UTBB FDSOI technology capabilities for Analog and RF applications are reminded in Section 6.3. Third, the transconductance ($g_m$) over drain current ($I_D$) based design method is presented in Section 6.4. Fourth, the high frequency performance versus IC and MOSFET length is assessed in Section 6.5. Fifth, a 35 GHz LNA design tradeoff in Moderate Inversion is proposed in Section 6.6. Finally, a new LNA-MIXER circuit combining both amplification and mixing operations in one circuit is proposed in Section 6.7, and a conclusion is given in Section 6.8.

## 6.2 Classical design sizing methods in Analog and RF

Sizing MOSFETs through iterative simulations and trial and error practices takes considerable amount of the precious design time. Optimum design tradeoff is hardly achieved using these methods [135]. Furthermore, hand calculation based analog design remains the method of choice to minimize iterative simulations, and enables intuitive design. The classical hand calculation sizing methods are still based on inaccurate and questionable concepts such as the gate voltage overdrive ($V_{ov} = V_{GS} - V_{TH}$, where $V_{TH}$ is the threshold voltage), and pessimistic rules of thumb such as the shortest possible length for higher $f_T$, higher $V_{ov}$ constraint, and a maximum operation frequency of $f_T/10$.

Design in Moderate Inversion has become attractive in advanced technologies as it offers the optimum trade-off between speed, transconductance, and power consumption [126][110]. However, the classical gate voltage overdrive is becoming a poor metric for MOSFET inversion level assessment in advanced technologies as it is based on conflicting definitions of the threshold voltage [136]. The latter is defined as the $V_{GS}$ value at the onset of the Strong Inversion and extracted using several methods and criteria leading to uncorrelated definitions. Moreover, gate overdrive voltage can only be used for the hand calculation sizing method based on SI square law that miserably fails to predict $g_m/I_D$ in MI as seen in Fig. 6.1. At $V_{ov}$ = 100 mV, the error is more than 100% for L = 30 nm. For short channel devices (e.g. L = 30 nm in Fig. 6.1),

the simple square law is not valid in all levels of inversion. Moreover, as see in Chapter 2 for a double gate transistor which is the UTBB FDSOI MOSFET, we experimentally observe two separate threshold voltages in the forward back gate bias condition while considering the measured C-V characteristic and its derivative both reproduced respectively in Fig. 6.2 and its Inset. Consequently, the gate overdrive voltage becomes impractical for describing the level of inversion of the advanced MOSFET architectures. It should be noted that $V_{ov}$ can become negative in MI and for lower levels of inversion, and thus becomes useless.

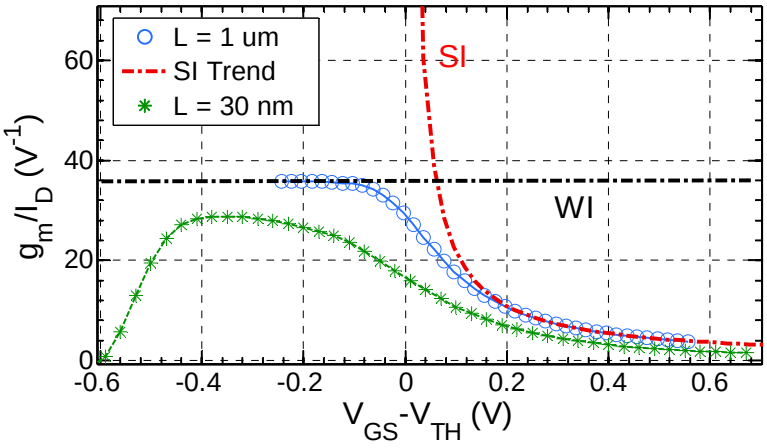



Fig. 6.1 Square law model and weak inversion exponential model failures to predict measured $g_m/I_D$ in MI for a long and short channel devices. $V_{TH}$ is defined here as the $V_{GS}$ at the maximum of $\partial C_{gc}/\partial V_{GS}$.

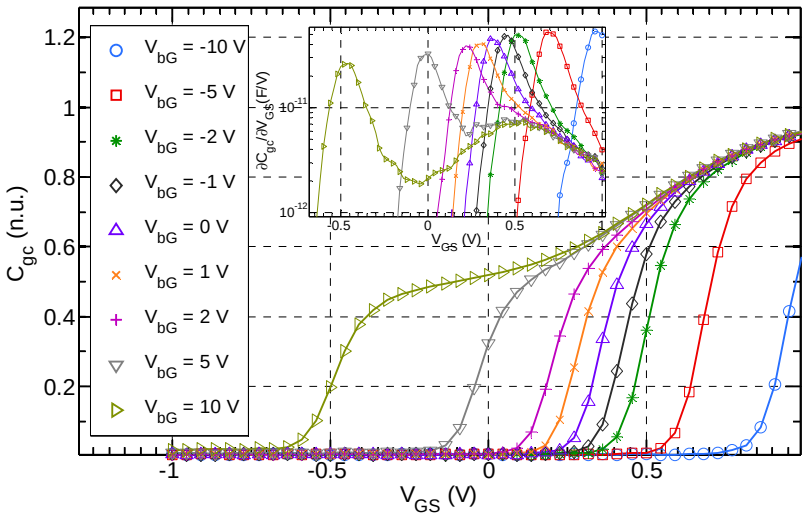



Fig. 6.2 Measured gate to channel capacitance normalized using front oxide capacitance ($C_{ox}$.W.L) with respect to $V_{GS}$ for various $V_{bG}$ and its derivative (Inset) for N-type UTBB FDSOI MOSFET.

In RF circuits, designers tend to use shortest devices to get highest possible transit frequency $f_T$ and consequently better performance. However, shortest MOSFETs are subject to detrimental short channel effects, lower intrinsic voltage gain, and higher mismatch. In Fig. 6.3, Drain-Induced-Barrier-Lowering (DIBL) versus the gate length is reproduced for bulk and FDSOI technologies. Using relaxed and non-minimal lengths provides lower DIBL effect and lower variability while frequency performance is still high enough for the majority of today's applications in the RF spectrum as shown in Fig. 6.4 where $f_T$ is plotted versus the Inversion Coefficient (IC) for various MOSFET lengths in 28 nm UTBB FDSOI technology. IC is defined as:

$$IC = \frac{I_D}{I_\square \cdot \left(\frac{W}{L}\right)} \tag{6.1}$$

where $I_D$, W and L are respectively the drain current, the width, and the length. $I_\square$ is the square current at the middle of the moderate inversion with a value of about 0.7 µA for 28 nm UTBB FDSOI NMOS [127]. For L = 100 nm, the maximum transit frequency is still in the mm-Wave spectrum (> 100 GHz) for the UTBB FDSOI technology while DIBL is reduced by 23 mV/V with respect to L = 28 nm. Moreover, according to (6.1) and for fixed $I_D$ and inversion level IC, the device area increases as $L^2$, which is beneficial for local mismatch effect.

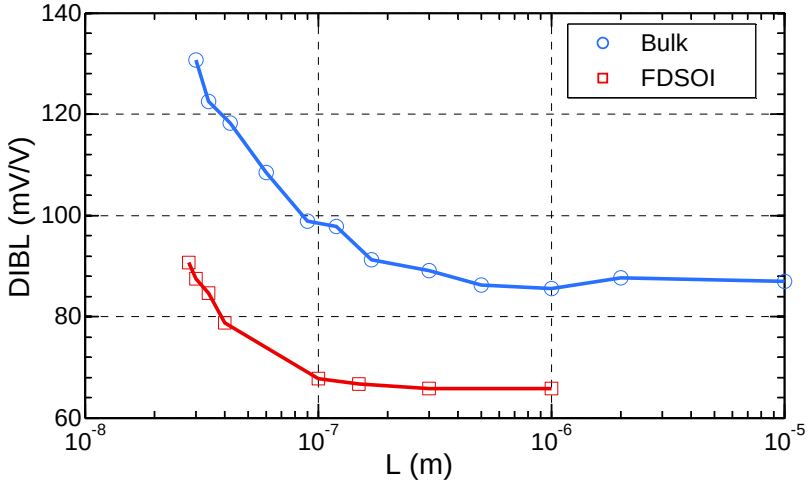



Fig. 6.3 Comparison of DIBL between FDSOI and bulk in saturation ($V_{DS}$=1V) and $V_{bG}$ = 0 V.

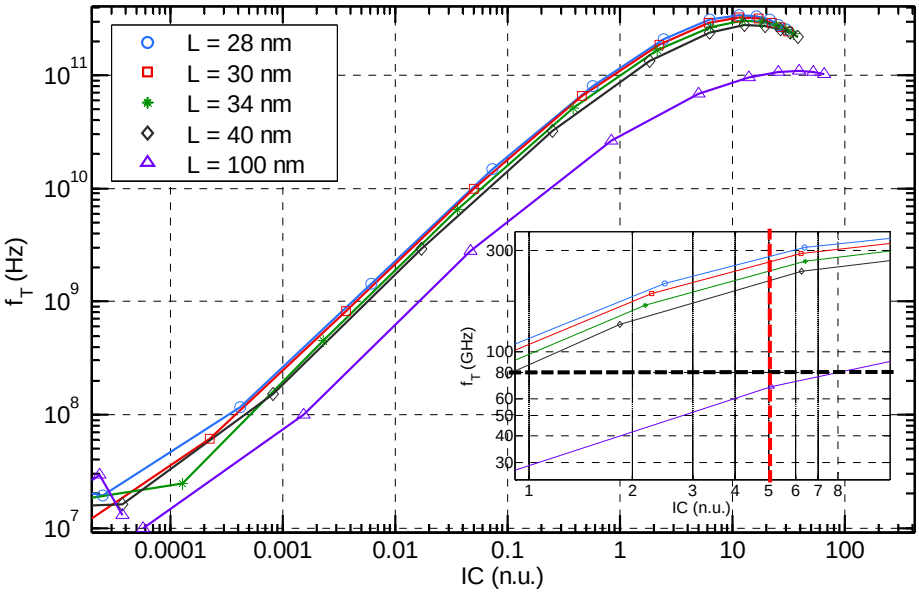



Fig. 6.4 Measured $f_T$ versus IC for various MOSFET lengths in saturation ($V_{DS}$=1V). Inset gives a focus on the second part of the MI (1 < IC < 10)

Normalized modulus and phase of the transadmittance $Y_{21}$ are respectively shown in Fig. 6.5 and Fig. 6.6 versus frequency for different lengths and at $V_{GS}$ = 0.5 V. The transadmittance is normalized using $I_{\square}/U_T$ where $U_T$ is the thermal voltage. All devices are operating in the MI regime. At $V_{GS}$ = 0.5 V, shorter channels (L < 100 nm) are biased at an inversion coefficient of 6.3, while for L = 100 nm, IC = 5.1. For L = 100 nm and at IC = 5.1, with a transit frequency $f_T$ of 70 GHz, the $f_T$/10 rule of thumb gives, 7 GHz. At this limit frequency no degradation on the $Y_{21}$ modulus is observed and a phase shift of less than 4° is measured. The finger length of the measured structures is 1 µm and the longitudinal gate distributed effect is largely contributing to the measured phase shift. Though, a phase shift of 10° is measured at 19 GHz with no degradation on $|Y_{21}|$. In summary, it is clearly evidenced that non minimal channel lengths (i.e. L > 30nm in 28 nm node) in advanced technologies provide high enough $f_T$ values that can still be used to design RF circuits, while the conservative $f_T$/10 rule of thumb is misleading, in particular at low inversion levels. 'Common' rules are then inaccurate and lead to overdesign. To overcome these issues, optimal geometries and bias conditions are approximated using time-consuming iterative numerical simulations. Other sizing methods based on the Inversion Coefficient concept have been proposed [81]. However, in many circuits where passive elements play a key role such as Low Noise Amplifier (LNA), circuits

are optimized using time-consuming iterations of the IC based method since no passive part related constraints are considered in the active part optimization [137].

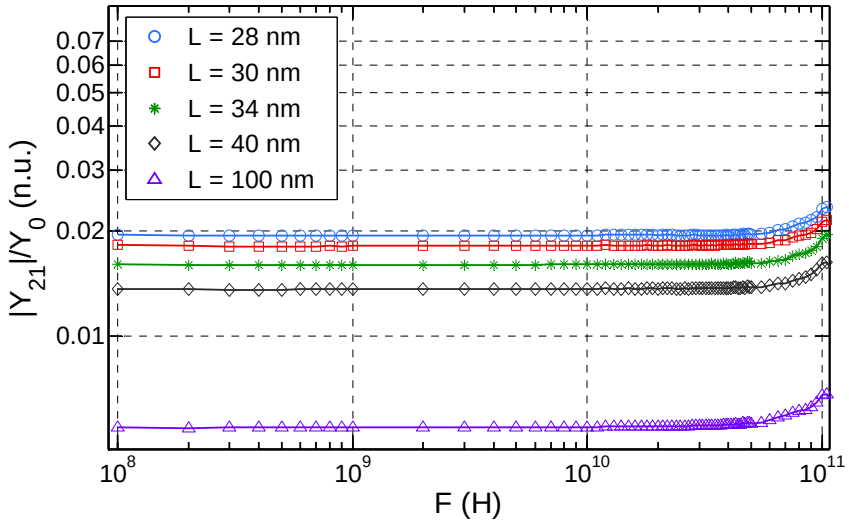



Fig. 6.5 Measured and normalized $|Y_{21}|$ versus frequency for various lengths and finger length is 1 µm.

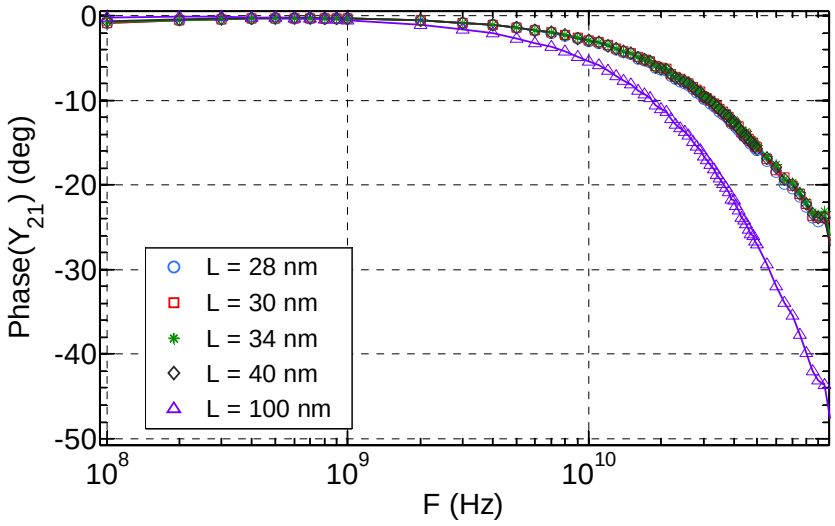



Fig. 6.6 Phase shift of the transadmittance $Y_{21}$ versus frequency for various lengths and finger length is 1 µm.

## 6.3 Advantages of UTBB FDSOI technology

In the UTBB FDSOI technology, MOSFET channel is formed in a thin silicon film separated from the substrate by an oxide film called the Buried OXide (BOX). In 28 nm FDSOI technology, the final silicon film is 7 nm thick after process [3]. This architecture provides with multiple advantages for high performance and low power applications. In

the addition of the well-known SOI technology advantages [38][39], UTBB FDSOI technology features lower parasitic capacitances and then high-speed operation. The harmful parasitic substrate coupling is avoided in the UTBB FDSOI by introducing the Ground Plane which is a highly doped region underneath the thin BOX [40]. The ground-plane implantation under the BOX is well-type in the structures studied in this work. FDSOI technology allows co-integration of both bulk and SOI devices on the same die thanks to BOX opening for the bulk parts with a dedicated mask [44].

With less parasitic capacitances, supply voltage can be lowered for reduced power consumption with still high speed operation. Other advantages of UTBB FDSOI are steep subthreshold slope [8], reduced SCE (cf. Fig. 6.3), tolerance to radiation as for standard SOI and high temperatures, even though buried oxide isolation is known to give birth to temperature increase because of self-heating effect [17]. However, thanks to a thinner BOX in the UTBB FDSOI, thermal effects influence on device parameters are limited in comparison with standard SOI [18].

The advantages of the UTBB FDSOI technology make it possible to implement high performance MOSFETs operating at a low voltage, specifically in the moderate inversion regime. An understanding of the fundamental behavior of the UTBB FDSOI MOSFETs at high frequency is essential for circuit design and a sizing method in MI is a must.

## 6.4 $g_m$ over $I_D$ invariance based method

In digital CMOS circuits, static power consumption is mainly related to the leakage current. However, in analog circuits, biasing current is the main contributor for circuit power consumption. Thus, the devices used in analog blocks need to be permanently biased in the appropriate region. Besides power supply voltage lowering in recent technology nodes, the current budget should be reduced as well.

In RF circuits, a good tradeoff between speed and low current budget is satisfied in moderate inversion. However, for advanced devices such as the asymmetric double gate MOSFETs, the validity of classical hand calculation expressions is questionable.

The lack of simple expressions for hand calculation can be reasonably contained using measurement based charts. The measured transconductance efficiency charts assessed in [127], can be used to size the transistor and to ensure its operation in moderate inversion. The invariance of the $g_m$ over $I_D$ chart in MI for L ≥ 100 nm makes it easy to generate the required chart. If we take into account the slope degradation using the slope factor $n_1$, shorter geometries can also be accounted for with same merged chart. In Fig. 6.7, $g_m$ over $I_D$ charts are shown versus IC. A longer geometry (L = 1 µm) is also shown for comparison. Using these charts, the $g_m$ over $I_D$ value can be reasonably retrieved for any selected IC and for each displayed geometry from WI to SI.

Recently, it is claimed that preselecting drain current ($I_D$), IC, and channel length is the most efficient way to size MOSFETs in analog circuits [81]. However, the proposed simple expressions of MOS performance mainly rely on EKV formalism which has been extrapolated to a symmetric DG in [108] but not yet transposed to the asymmetric DG. However, the choice of the inversion coefficient as a measure of the inversion level in the channel happens to be totally justified since it accurately describes the inversion charge and consequently the operating regime for single or double gate MOSFETs [81][127]. According to Fig. 6.7, selecting an IC value is equivalent to setting $g_m$ over $I_D$ of the device. Moreover, based on (6.1), once IC an $I_D$ are known, the geometry ratio (W/L) can be calculated.

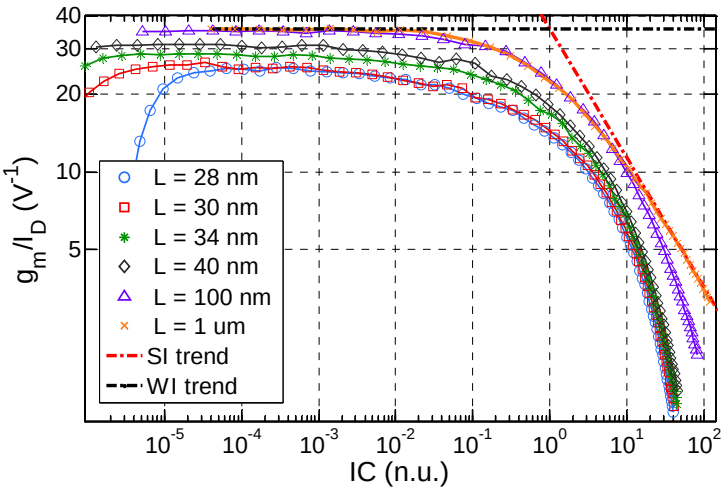



Fig. 6.7 $g_m$ over $I_D$ charts versus IC for several short NMOS along with a longer channel (L = 1 µm) for comparison.

## 6.5 High frequency performance assessment

One of the interesting high frequency FoM is the transit frequency $f_T$ that estimates the high frequency amplification limit and also provides an insight of the transconductance to input capacitance ratio ($f_T \approx g_m/2\pi C_{gg}$) of the MOSFET. The transit frequency versus IC charts for several lengths provide high frequency performance limits since $f_T$ represents the frequency at which current gain falls to unity. However, it should be noted that the transistor can operate at any frequency even beyond this limit, provided that non-quasi-static related limitations are carefully taken into account and modeled. The modulus and phase of the transadmittance versus frequency charts (e.g. Fig. 6.5 and Fig. 6.6) can also be used to estimate the phase shift and modulus drop when frequency is set beyond $f_T$ (cf. Chapter 5 for more detail). As stated in Section 6.2, the rule of thumb stating that maximum frequency of operation must be lower than $f_T/10$ is too stringent. This rule of thumb finds its origin in the validity of the quasi-static model proposed in [97] and thus is essentially a misinterpretation.

## 6.6 LNA design using MI Tradeoff in UTBB FDSOI

In this Section, the focus will be on another challenge which is the transistor sizing. The RF designer dilemma is to calculate transistor geometry and current in order to get maximum amplification, minimum degradation of the signal-to-noise ratio, and minimum power consumption. The goal is to provide an illustration of a design method mainly based on the charts and properties described in previous Chapters and reminded in Section 6.4 and 6.5.

One of the key building blocks in a wireless system is a Low Noise Amplifier (LNA). The LNA circuit amplifies the input signal with minimum degradation of the signal-to-noise ratio. One of the challenges RF designers face is the simultaneous matching of the noise and the input impedance for the same source impedance. This challenge is beyond the scope of this Chapter therefore ideal impedance matching is considered here. However, a constraint on the value of the inductors is considered in order to account for integrated inductors with acceptable quality factors.

One of the most used circuit topologies for an LNA is the narrowband cascode. The cascode transistor is used to isolate the input from the inductive load. In particular, the Miller effect is reduced for the input transistor. However, using a cascode topology leads to a minimal room for drain to source voltage required to set both transistors in saturation. This also corroborates the need for MI operation as $V_{DSAT}$ is lower in this regime. The circuit of the cascode LNA is shown in Fig. 6.8. The transistor $M_1$ is the input transistor and $M_2$ is the cascode transistor. Both transistors are chosen to have same geometry. Degeneration inductor $L_s$ and input series inductor $L_g$ are used for input impedance matching.

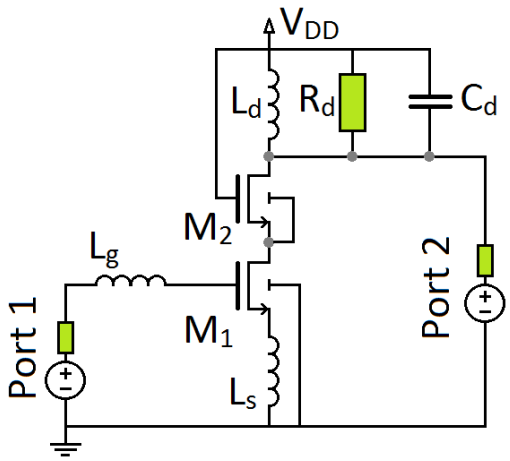



Fig. 6.8 LNA cascode circuit.

The following specifications are taken as an example: Drain current is 2 mA, power gain is greater than or equal to 8, operation frequency is $F_0$ = 35 GHz, minimal noise figure NFmin is no more than 2 dB, and input impedance is matched for 50 ohm. In order to size the circuit components and meet the aforementioned specifications, the following 3 steps are followed:

## 6.6.1 IC selection

The maximum value of the FoM given in (6.2) and representing the trade-off between high frequency performance, power consumption, and noise figure is located in the second half of the MI for short channels as shown in Fig. 6.9 for two channel lengths (L = 30 nm and 1 µm).

$$FOM = \frac{g_m}{I_D} \cdot \frac{f_T}{NF_{min}} \tag{6.2}$$

Optimal IC lays, at least theoretically, between IC = 4 and IC = 10. Depending of the length selection, corresponding IC will be chosen where FoM is maximum.

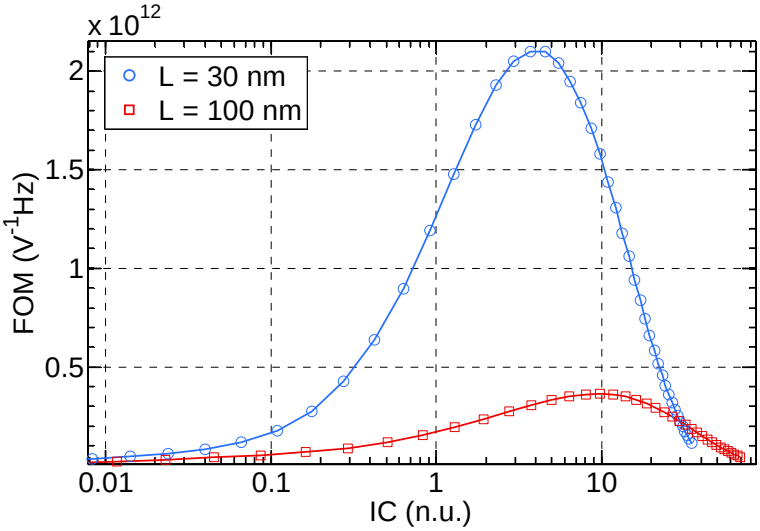



Fig. 6.9 FoM versus IC for two lengths.

## 6.6.2 Passives related constraints and Length selection

In order to avoid passive components with degraded quality factors Q, some constraints are considered prior to MOSFETs sizing. The values are chosen within the integrated mm-Wave inductor values [25 pH – 100 pH] as in [138]. The real part of the LNA input impedance is mainly tuned using degeneration inductor $L_s$. The expression of this real part is given in (6.3), provided that $M_1$ intrinsic conductance influence on input impedance is neglected:

$$Re[Z_{in}] = \frac{g_m L_s}{C_{gs}} \approx 2\pi f_{Ti} L_s \tag{6.3}$$

where $C_{gs}$, and $f_{Ti}$ are the gate-source, and intrinsic transit frequency of $M_1$, respectively. The specification related to impedance matching fixes the real part of $Z_{in}$ at 50 ohm and consequently a relation between the inductance $L_s$ and the transit frequency is given by (6.3). If we consider a maximum $L_s$ inductance of 100 pH, $M_1$ transit frequency $f_{Ti}$ should be greater than 80 GHz. According to Inset of Fig. 6.4, for

operation at IC = 4, the MOSFET length that guarantees the required $f_T$ is strictly lower than L = 100 nm. To obtain acceptable noise figures and using $NF_{min}$ versus IC charts shown in Fig. 6.10, length should also be lower than 100 nm. In order to verify the noise figure specification and inductor value constraint, we will consider two channel lengths that are L = 40 nm and L = 70 nm, with FoM maximizing respectively at IC = 5 and IC = 9. Both geometries provide acceptable high frequency performance. Moreover, L = 40 nm and L = 70 nm MOSFETs are less subject to DIBL and Mismatch than minimal length. Thus, an $L_s$ value of 33 pH and 39 pH for respectively L = 40 nm, and L= 70 nm MOSFET based LNAs are found.

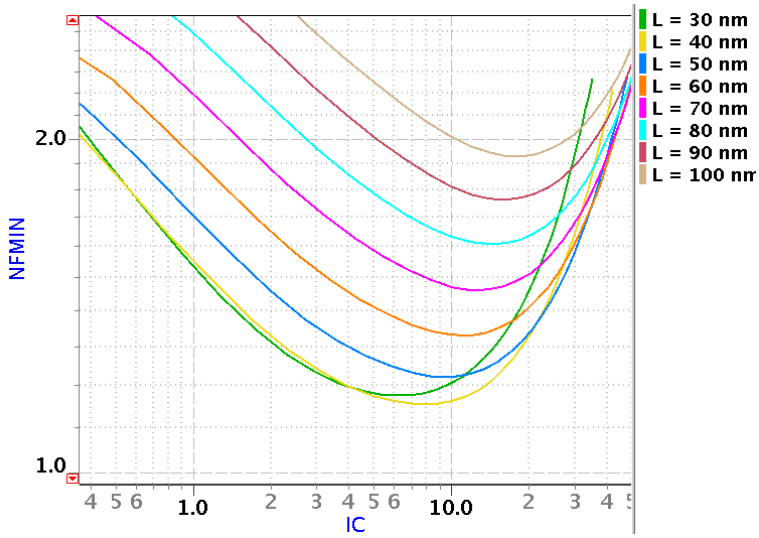



Fig. 6.10 $NF_{MIN}$ noise figure vs. IC for various lengths in saturation.

The LNA is designed to operate at $F_0$ = 35 GHz and consequently, to cancel the input impedance imaginary part at this resonance frequency, the inductor $L_g$ is tuned with a target value given by [139]:

$$L_g = \frac{1}{(2\pi F_0)^2 \cdot C_{in}} - L_s \tag{6.4}$$

where $C_{in}$ is including the total $M_1$ gate capacitance $C_{gg}$ and the Miller effect of the gate-drain capacitance ($C_{gd}$).

### 6.6.3 Width and $V_{GS}$ calculations

The Width is calculated using the following expression:

$$W = \frac{I_D}{IC \cdot I_{\square}} \cdot L \tag{6.5}$$

Close width values of 22.8 µm and 22.1 µm are found for respectively L = 40 nm and L = 70 nm based LNA circuits.

The gate voltage overdrive with respect to IC charts shown in Fig. 6.11 are used to retrieve the gate to source voltage corresponding to the two IC values for each length. The calculated $V_{GS}$ values are respectively 0.49 V and 0.55 V.

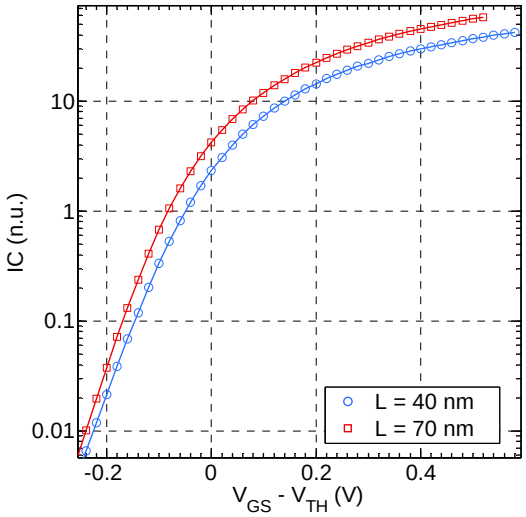



Fig. 6.11 Inversion Coefficient vs. gate voltage overdrive for two lengths L = 40 nm and L = 70 nm.

The results of the above sizing flow are shown in Fig. 6.12 versus frequency and summarized in Table 6-1 for the operation frequency $F_0$ = 35 GHz.

Table 6-1 Summary of the two LNAs parameters at $F_0$ = 35 GHz.

| | $S_{21}$ | $S_{11}$ | NFmin |
|---|---|---|---|
| LNA (L = 40 nm) | 10.9 | -31 | 1.5 |
| LNA (L = 70 nm) | 8.6 | -21.5 | 2 |

Power gain is lower for the L = 70 nm based LNA because of the higher IC and consequently lower transconductance efficiency. The input impedance matching is acceptable for both LNA circuits. The NFmin value is higher for the longer channel based LNA as expected, however this can be lowered using optimized layout. The power consumption of both LNAs is 2 mW which is excellent for low-power applications.

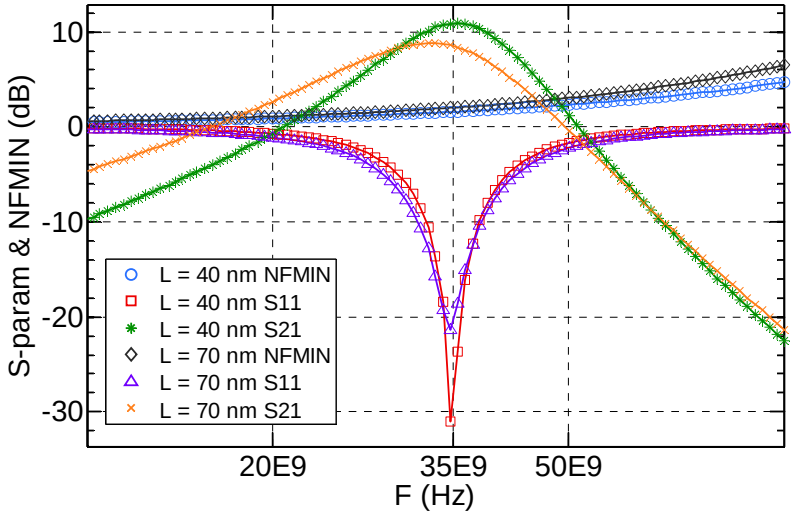



Fig. 6.12 Power gain $S_{21}$, Input Match $S_{11}$, and minimal noise figure NFmin with respect to frequency for two LNA circuits (first with MOSFET length of 40 nm and second with 70 nm).

## 6.7 LNA - MIXER

The back gate of the input MOSFET $M_1$ in the LNA circuit of Fig. 6.8 is grounded which fixes the voltage drop between back gate and source. The goal of the LNA as an important element of the transceiver, is to amplify the signal with minimal impact on the signal to noise ratio. In the receiver path, after amplification, the signal is downconverter using a mixer. The down-conversion mixer senses the amplified RF signal at its first port and the local oscillator waveform at its second port. The mixer performs frequency translation or modulation of the RF signal by multiplying the two waveforms at its two input ports in order to obtain a baseband signal which is convenient for signal processing. Mixers are usually realized using either passive or active circuits that contribute to the total transceiver noise and power consumption. The design of the LNA and the mixer are tightly linked. A tradeoff is usually examined

between the mixer linearity and its noise figure in one hand and the LNA gain in the other hand.

One of the advantages of the UTBB FDSOI MOSFET discussed in previous chapters is the possibility to control the threshold voltage using the back gate. This feature can be used here in order to modulate the input signal at the front gate of the same MOSFET used for amplification in the LNA circuit shown in Fig. 6.8. We propose to merge both the LNA and the mixer in the same circuit as shown in Fig. 6.13. This LNA-MIXER circuit allows a simultaneous amplification and frequency conversion of the input signal using a minimum number of MOSFETs. The noise figure is minimized as only one MOSFET channel is used for both operations (e.g. amplification and mixing).

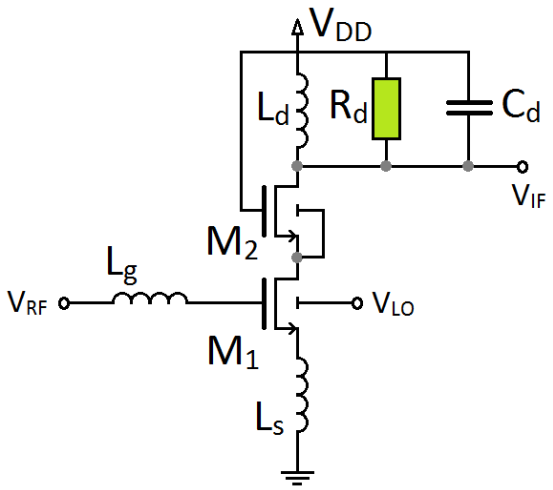



Fig. 6.13 The LNA-MIXER circuit.

In Fig. 6.14, an illustration of the LNA-MIXER operation is provided in time and frequency domains. The input RF signal $V_{RF}$ at the front gate of $M_1$ is modulated using the back gate voltage $V_{LO}$ which is generated locally using an oscillator. The LO voltage is sufficiently high to control the channel through the thick BOX. The output current $I_D$ represents the product of the two input signals and produces a voltage signal at the circuit output $V_{IF}$. The output signal spectrum is shown in Fig. 6.14 (bottom) where the signal frequency is down-converted from 60 GHz to a very low baseband frequency.

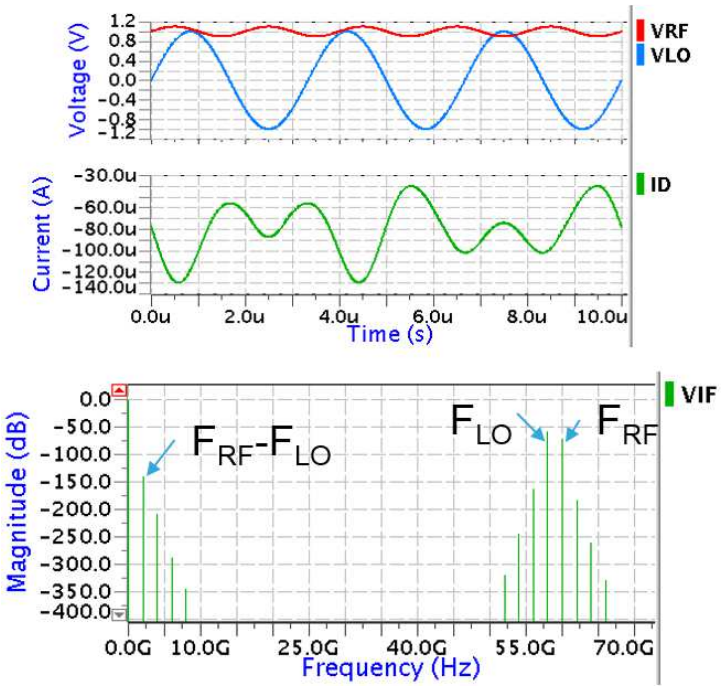



Fig. 6.14 (top) Time domain input voltages VRF and VLO, and output current $I_D$, (bottom) corresponding output $V_{IF}$ spectrum.

## 6.8 Conclusion

In this Chapter, a constrained sizing methodology is proposed for the UTBB FDSOI MOSFET. The methodology is based on $f_T$ versus IC measured or simulated curves for the length selection, and on $g_m$ over $I_D$ charts for the width calculation. The Inversion Coefficient is fixed to a value where the MOSFET optimum performance is expected, making this analysis dependent only on the channel current, and 'independent' of the front and back gate biases, a great simplification in terms of analysis. The methodology takes into account the passive components limitations and thus requires less if not minimal iterations.

# General conclusion

Silicon based RF technology and wireless communication have had an impressive impact on our lives. The success was mainly based on the aggressive downscaling dictated by the high-performance integrated digital circuits. The detrimental short-channel related issues have been controlled by brilliant scientists and creative engineers using new device architectures and new materials. The new architectures such as the UTBB FDSOI studied in this research work allow for excellent electrostatic control, high level of integration, reduced power consumption, and very high operation frequency.

Moreover, with these recent advances in silicon industry, IoT network is becoming more of a reality in terms of their widespread use in various aspects of life. Although IoT already brings more capability in our daily life in terms of sensing and communicating using RF systems, higher performance along with more autonomy are still to be explored. Therefore, profound skills have to be developed in the following two key areas: (1) Silicon based CMOS technology usage in mm-Wave spectrum and beyond, and (2) Transistor operation at lower applied voltages and in lower levels of inversion.

Given the above mentioned needs, the first goal of this thesis has been to study and evaluate the capabilities of the newly developed UTBB FDSOI technology through its main building block, which is the double gate MOSFET. The other goal is to explore and expand the low frequency modeling approaches and sizing methods to high frequency, with a strong focus on moderate inversion where a tradeoff between performance and power consumption is predicted.

## Research work results

The main results of this research work are summarized in the following although conclusions are already presented for each Chapter.

**Transconductance efficiency invariance in asymmetric double gate**

As MOSFET high frequency operation is tightly linked to its bias conditions, DC and low frequency behavior assessment was our first target before tackling the high frequency operation. One of the most convenient metrics that combines both the amplification capability and power consumption is the $g_m$ over $I_D$ namely the transconductance efficiency. Transconductance efficiency is proven to be an essential design synthesis tool for low-power analog and RF applications. For better insight into the MOSFET operation at lower levels of inversion, the $g_m$ over $I_D$ figure of merit is studied in detail**.** The invariance of this important FoM versus the Inversion Coefficient is analyzed in UTBB FDSOI MOSFET. The breakdown of this invariance has been assessed with respect to back gate voltage, transistor length, temperature, drain to source voltage and process variations.

The invariance can be used to predict the transconductance provided that W/L and level of inversion (i.e. IC) are given. Moreover, with the additional chart of IC with respect to the gate voltage overdrive $V_{GS}$ - $V_{TH}$, one can predict drain current provided that W/L and gate voltage are provided. This can allow designers to predict MOSFET DC properties without the need of an analytical model including in MI which is difficult to capture. The aforementioned charts along with main MOSFET capacitances (i.e. in use in the proposed equivalent circuits) versus IC charts can provide accurate predictions of the equivalent circuit parameters and thus completely replace a compact model for simple circuit investigations.

Furthermore, we have experimentally shown that $g_m$ over $I_D$ versus inversion coefficient chart can be considered as a fundamental characteristic of UTBB FDSOI technology transistors and thus be used in $g_m$ over $I_D$ based analog design sizing procedures.

**Transadmittance efficiency concept**

High frequency operation is governed by both the MOSFET extrinsic elements and the distributed effects. Carful characterization techniques with several correction steps have been used in order to get rid of the measurement setup and pads related parasitic elements. In particular, dedicated SHORT structures are used to extract the

parasitic DC series resistances. Classical OPEN-SHORT method is used to de-embed measured S-parameters. These techniques provided a closer insight to the intrinsic behavior of the UTBB FDSOI MOSFET and allowed the distinction between two competing distribution effects: the channel NQS effect and the gate distribution effect.

The UTBB FDSOI MOSFET NQS behavior is studied with a special focus on moderate inversion. Frequency dependence of small signal characteristics derived from experimental S-parameters are analyzed and reveal that the transconductance efficiency ($g_m/I_D$) concept, already adopted as a low frequency Analog figure-of-merit, can be generalized to high frequency. In particular, the concept of the transadmittance efficiency is introduced to assess MOSFET capability in a wider frequency range. The new FoM allows operation tradeoffs prediction in all levels of inversion and all operation frequencies.

The generalized FoM (i.e. $y_m/I_D$) with respect to the normalized frequency, using the first NQS pole, only depends on the mobility and inversion coefficient (IC). This interesting property is used to define NQS critical frequencies based on the gain decrease and phase shift. A link to the generally used transit frequency is also given.

**Mobility extraction using NQS effect**

In addition, we used the novel approach (i.e. the normalized critical frequency invariance assessed using the transadmittance efficiency) to extract essential parameters such as the mobility, the critical NQS frequency $f_{NQS}$ and the transit frequency $f_T$. Contrary to the classical methods, the proposed mobility extraction method allows accurate extraction including in MI and WI. This capability is based on the fact that, at high frequency, charge carriers “oscillate” in channel and are less subject to extrinsic series parasitics.

**DC and quasi-static low-frequency modeling**

The analysis of the measured and simulated DC and C-V characteristics for various back gate voltages, shows that the thin silicon film is subject to multiple phenomena. In particular, the channel is not confined to the front and back interfaces although the majority of compact models adopt the double interface approach. The

volume inversion phenomena is found to be the most adapted to explain the electrostatic and transport observations.

The DC UTBB FDSOI MOSFET characteristics are compared to a single gate bulk counterparts. Although the two gates control and the thin film quantum effect occurrence, the DC characteristics are comparable to the bulk ones. Moreover, thanks to a better electrostatic control, the long channel DC characteristics are closer to the ideal square law in SI and to the exponential law in WI. The derivation of the threshold based models in both bulk and UTBB FDSOI showed that the classical bulk models can be used as fair approximations provided that the threshold voltage dependence on both gates is accounted for in UTBB FDSOI MOSFET. It should be noted that mobility reduction and saturation can be accounted for using same classical bulk methods as a first order model.

A small signal low frequency equivalent circuit is proposed and gradually enhanced for higher frequency operation. The proposed equivalent circuit simulation is compared to UTSOI2 model and showed to be accurate enough to be used in analog circuit investigations. Two modeling approaches are investigated: the simple equivalent circuit and the industrial recently proposed quasi-static compact model namely Leti-UTSOI2 model. The important low frequency Figures-of-Merit are assessed using both models and showed accurate reproduction of the measured data.

**DC OP Information feature enhancement**

An enhancement of the classical Operating Point Information feature in circuit simulators is proposed. The classical feature is intensively used in Analog and RF design CAD despite severe limitations discussed in Section 2.5 of Chapter 2. The proposed enhancement provides accurate information for complex RF sub-circuit based models despite the multiple extrinsic elements involved and the high frequency NQS models. The proposal is adopted by major EDA vendors.

**High frequency NQS model**

The used high frequency characterization technics allowed to get clean measurements up to 110 GHz. The high frequency characteristics are used to validate the proposed model, noting that the proposed characterization is based on lower

frequency measurements. Two main effects limit the high frequency MOSFET capability: (1) the extrinsic layout dependent elements, and (2) the lateral (i.e. channel related) and longitudinal (i.e. gate related) distributed effects.

The extrinsic elements are modeled using on the one hand the series source and drain resistances and, on the other hand two gates networks. The front gate network is taking into account the physically distributed resistances and capacitances in particular three series resistances and two main fringing capacitances. The front gate is consequently accounting for the distributed effect especially for large MOSFETs. This distributed effect is competing with the channel NQS effect and is carefully modeled partly using a pole-zero compensation technique.

The non-quasi-static effect is modeled using a channel segmentation and an additional MOSFET shell in order to take into account the overlap and a part of the extrinsic fringing capacitance. The DIBL is modeled using extrinsic voltage dependent voltage sources at the front and back gates in order to emulate the threshold voltage shift.

The proposed model predicts accurately the Y-parameters and high frequency FoMs over the wide frequency range from 100 MHz up to 110 GHz. The excellent accuracy over a wide frequency band of the simulations compared to measurements verifies that the topology of our model is correct and complete.

**Analog RF and mm-Wave sizing**

Having previously prepared low and high frequency charts and developed high frequency accurate models, a circuit sizing methodology is proposed and discussed to illustrate the benefits of operation in moderate inversion. The classical sizing methods along with their impact on circuit sizing are discussed and found to cause overdesign.

The UTBB FDSOI characteristics are used for first-cut analog sizing of a simple 35 GHz LNA circuit. The goal is to provide with an application example where operation in MI is profitable as long as both high frequency performance and power consumption matters. The transconductance efficiency versus inversion coefficient (IC) studied in Chapter 3 is used to determine the width of the MOSFET while the transit frequency ($f_T$) versus IC charts are used for length selection. The design method, using relaxed

length and Moderate Inversion regime, provides a valuable tradeoff between gain, power consumption and performance while MOSFET width is kept reasonably large and short channel effects are mitigated. An eye is also kept on passive devices limitations from the very beginning of the sizing flow.

## Perspectives

### Large signal validation

Although small signal models are often sufficient for the design of linear circuits, the implementation of nonlinear circuits such as power amplifiers and oscillators requires accurate prediction of the nonlinear characteristics of MOSFETs in a wide range of bias conditions. The equivalent circuit developed in this thesis is a small signal model and can only be used with linear circuits. However, the augmented UTSOI2 model, also proposed in this thesis for industrial circuits simulation, is conceptually a large signal model provided that we assume that large signal performance is primarily governed by its DC nonlinearities. The approach based on an augmented compact model predicts accurately the harmonic distortion behavior although a quasi-static assumption is considered in [140]. This extended compact model approach can also be used in the case of the UTBB FDSOI MOSFET for large signal simulation. Therefore, in order to validate this approach, mm-Wave nonlinearity characterization needs to be performed using for instance mm-Wave load-pull measurements or power spectrum analysis.

### High frequency noise model

An accurate high frequency noise model is a must for LNA design. Still, noise is commonly characterized in a frequency range where the transistor behavior verifies the quasi-static assumption. Therefore, noise measured data are often not reproduced with inadequate models at high frequency. Moreover, noise effects of different origins have made it difficult for scientists to develop an accurate model. In particular, empirical models are being used for high frequency noise modeling because of the ambiguity related to the real cause of excess noise in short channel devices. The two-port noise parameters, traditionally required for RF design as a better alternative to inaccurate

models, have to be extended to the mm-Wave spectrum and powerful de-embedding techniques are still to be proposed.

**Variability**

Because of the shirked dimensions in the advanced technologies such as UTBB FDSOI, managing variability has become one of the most important, if not the most important challenge. The electrical variability caused by the process variation at nanoscale greatly impacts the yield and thus the cost of the integrated circuits.

In analog and RF/mm-Wave design, a variability model has to be accurate enough to predict the impact of local and global process variations on the electrical simulations. Although conservative models exist to accommodate the high yield requirements, a rigorous and comprehensive analysis of variability and its origins along with robust models are invaluable.

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# Appendix A

The 1-D Poisson's equation of the lightly doped silicon film is written as:

$$\frac{\partial^2 \Psi(x,y)}{\partial y^2} = \frac{q \cdot n_i}{\varepsilon_{Si}} e^{\frac{\Psi(x,y)-V(x)}{U_T}} \quad \text{(A. 1)}$$

where ψ(x,y) is the electronic potential in the silicon film, V(x) is the quasi Fermi level or the channel potential (V(0) = 0 and V(L) = $V_{DS}$, $n_i$ is the intrinsic concentration, q is the elementary electronic charge, and $\varepsilon_{si}$ is the permittivity of the silicon.

The boundary conditions at the front and back interfaces using Gauss's law give:

$$V_G - V_{fb1} = \Psi_{s1} + \frac{Q_{g1}(x)}{C_{ox1}}, \qquad Q_{g1}(x) = -\varepsilon_{Si} \frac{\partial \Psi_{s1}}{\partial y} \quad \text{(A. 2)}$$

$$V_{bG} - V_{fb2} = \Psi_{s2} + \frac{Q_{g2}(x)}{C_{ox2}}, \qquad Q_{g2}(x) = \varepsilon_{Si} \frac{\partial \Psi_{s2}}{\partial y} \quad \text{(A. 3)}$$

The charge neutrality in the structure gives:

$$Q_{g1}(x) + Q_{g2}(x) + Q_{inv}(x) = 0 \quad \text{(A. 4)}$$

For seek of simplification we define:

$$n_i'(x) = n_i \cdot e^{-\frac{V(x)}{U_T}} \qquad C_{Si} = \frac{\varepsilon_{Si}}{t_{Si}} \quad \text{(A. 5)}$$

$$V_G' = V_G - V_{fb1} \qquad V_{bG}' = V_{bG} - V_{fb2} \quad \text{(A. 6)}$$

The integration of the Poisson's equation along with Gauss's law gives [96]:

$$Q_{g1}(x)^2 - Q_{g2}(x)^2 = 2 \cdot q \cdot n_i'(x) \cdot \varepsilon_{Si} \cdot U_T \cdot \left[ e^{\frac{\Psi_{s1}(x)}{U_T}} - e^{\frac{\Psi_{s1}(x)}{U_T}} \right] \quad \text{(A. 7)}$$

We will follow the approach of splitting the inversion charge into front and back inversion charges [96].

Using (A. 4) and (A. 7) one gets:

$$\left(Q_{g1}(x) - Q_{g2}(x)\right) \cdot Q_{inv}(x) = 2 \cdot q \cdot n_i'(x) \cdot \varepsilon_{Si} \cdot U_T \cdot \left[e^{\frac{\Psi_{s1}(x)}{U_T}} - e^{\frac{\Psi_{s1}(x)}{U_T}}\right] \quad \text{(A. 8)}$$

And after a few rearrangement and using “tanh” function we have:

$$\left(Q_{g1}(x) - Q_{g2}(x)\right) \cdot Q_{inv}(x) = 2 \cdot q \cdot n_i'(x) \cdot \varepsilon_{Si} \cdot U_T \cdot \left[e^{\frac{\Psi_{s1}(x)}{U_T}} + e^{\frac{\Psi_{s1}(x)}{U_T}}\right] \cdot \tanh\left(\frac{\Psi_{s2}(x) - \Psi_{s1}(x)}{2 \cdot U_T}\right) \quad \text{(A. 9)}$$

The front and back inversion charges, respectively $Q_{inv1}$ and $Q_{inv2}$, can be defined such as:

$$\left(Q_{g1}(x) - Q_{g2}(x)\right) \cdot Q_{inv1}(x) = 2 \cdot q \cdot n_i'(x) \cdot \varepsilon_{Si} \cdot U_T \cdot e^{\frac{\Psi_{s1}(x)}{U_T}} \cdot \tanh\left(\frac{\Psi_{s2}(x) - \Psi_{s1}(x)}{2 \cdot U_T}\right) \quad \text{(A. 10)}$$

$$\left(Q_{g1}(x) - Q_{g2}(x)\right) \cdot Q_{inv2}(x) = 2 \cdot q \cdot n_i'(x) \cdot \varepsilon_{Si} \cdot U_T \cdot e^{\frac{\Psi_{s2}(x)}{U_T}} \cdot \tanh\left(\frac{\Psi_{s2}(x) - \Psi_{s1}(x)}{2 \cdot U_T}\right) \quad \text{(A. 11)}$$

In the case of a **weak inversion on both interfaces** (front and back), the inversion charge plays a minimal role in the structure electrostatic. The transverse electrical field is given by:

$$\frac{\partial \Psi(x,y)}{\partial y} = \frac{\Psi_{s2}(x) - \Psi_{s1}(x)}{t_{Si}} \quad \text{(A. 12)}$$

The charges in the two gates become:

$$Q_{g2}(x) = -Q_{g1}(x) = C_{Si} \cdot (\Psi_{s2}(x) - \Psi_{s1}(x)) \quad \text{(A. 13)}$$

In this case, (A. 10) and (A. 11) become:

$$Q_{inv1}(x) = -q \cdot n_i'(x) \cdot \frac{t_{Si}}{2} \cdot U_T \cdot e^{\frac{\Psi_{s1}(x)}{U_T}} \cdot \frac{\tanh\left(\frac{\Psi_{s2}(x) - \Psi_{s1}(x)}{2 \cdot U_T}\right)}{\frac{\Psi_{s2}(x) - \Psi_{s1}(x)}{2 \cdot U_T}} \quad \text{(A. 14)}$$

$$Q_{inv2}(x) = -q \cdot n_i'(x) \cdot \frac{t_{Si}}{2} \cdot U_T \cdot e^{\frac{\Psi_{s2}(x)}{U_T}} \cdot \frac{\tanh\left(\frac{\Psi_{s2}(x) - \Psi_{s1}(x)}{2 \cdot U_T}\right)}{\frac{\Psi_{s2}(x) - \Psi_{s1}(x)}{2 \cdot U_T}} \quad \text{(A. 15)}$$

When the two interface potentials are close to each other, the two last expressions converge to the symmetric gate MOSFET charge.

In the case where **one of the interfaces is inverted**, deriving (A. 2) with respect to $\psi_{s1}$ and using (A. 6) along with the charge conservation in (A. 4), we obtain:

$$\frac{dV_G'}{d\Psi_{s1}} = 1 - \frac{1}{C_{ox1}} \cdot \frac{dQ_{g2}}{d\Psi_{s1}} + \frac{C_{inv1}}{C_{ox1}} \quad \text{(A. 16)}$$

where

$$C_{inv1}(x) = -\frac{dQ_{inv1}(x)}{d\Psi_{s1}} \quad \text{(A. 17)}$$

We assume the silicon film is still weakly inverted, $V_{bG}$ is fixed, and $Q_{inv1} >> Q_{inv2}$.

Using (A. 3), (A. 6) and (A. 13), we have:

$$\Psi_{s2}(x) = V_{bG}' - \frac{Q_{g2}(x)}{C_{ox2}} = \Psi_{s1}(x) + \frac{Q_{g2}(x)}{C_{Si}} \quad \text{(A. 18)}$$

The back gate charge is given by:

$$Q_{g2}(x) = \frac{C_{Si} \cdot C_{ox2}}{C_{Si} + C_{ox2}} \left(V_{bG}' - \Psi_{s1}(x)\right) \quad \text{(A. 19)}$$

(A. 16) becomes:

$$\frac{dV_G'}{d\Psi_{s1}} = 1 + \frac{1}{C_{ox1}} \cdot \frac{C_{Si} \cdot C_{ox2}}{C_{Si} + C_{ox2}} + \frac{C_{inv1}}{C_{ox1}} \quad \text{(A. 20)}$$

Consequently, the threshold condition for the front interface is:

$$C_{inv1}^{TH} = n_{s1} \cdot C_{ox1} \quad \text{(A. 21)}$$

where

$$n_{s1} = 1 + \frac{1}{C_{ox1}} \cdot \frac{C_{Si} \cdot C_{ox2}}{C_{Si} + C_{ox2}} \quad \text{(A. 22)}$$

With $Q_{inv1} >> Q_{inv2}$ assumption, the “tanh” term in (A. 14) is equal to -1 and we get:

$$Q_{inv1}(x) = -q \cdot n_i'(x) \cdot \frac{t_{Si}}{2} \cdot U_T \cdot e^{\frac{\Psi_{s1}(x)}{U_T}} \cdot \frac{2 \cdot U_T}{\Psi_{s1}(x) - \Psi_{s2}(x)} \quad \text{(A. 23)}$$

Using (A. 18) and (A. 19), we get:

$$Q_{inv1}(x) = -q \cdot n_i'(x) \cdot \frac{t_{Si}}{2} \cdot U_T \cdot e^{\frac{\Psi_{s1}(x)}{U_T}} \cdot \left(1 + \frac{C_{Si}}{C_{ox2}}\right) \cdot \frac{2 \cdot U_T}{\Psi_{s1}(x) - V_{bG}'} \quad \text{(A. 24)}$$

Deriving the expression with respect to $\psi_{s1}$ results in $C_{inv1}$ expression:

$$C_{inv1}(x) = -\frac{Q_{inv1}(x)}{U_T} \cdot \left[1 - \frac{U_T}{\Psi_{s1}(x) - V_{bG}'}\right] \quad \text{(A. 25)}$$

The threshold condition (A. 21) becomes:

$$Q_{inv1}^{TH} = -n_{s1} \cdot C_{ox1} \cdot U_T \cdot \left[\frac{\Psi_{s1}(x) - V_{bG}'}{\Psi_{s1}(x) - V_{bG}' - U_T}\right] \quad \text{(A. 26)}$$

If we further assume $\Psi_{s1}(x) - V_{bG}' \gg U_T$, we get:

$$Q_{inv1}^{TH} = -n_{s1} \cdot C_{ox1} \cdot U_T \quad \text{(A. 27)}$$

Similarly, we get for the back interface:

$$Q_{inv2}^{TH} = -n_{s2} \cdot C_{ox2} \cdot U_T \quad \text{(A. 28)}$$

Where

$$n_{s2} = 1 + \frac{1}{C_{ox2}} \cdot \frac{C_{Si} \cdot C_{ox1}}{C_{Si} + C_{ox1}} \quad \text{(A. 29)}$$

Using (A. 2), (A. 6), and (A. 18), and knowing that $Q_{g1} = -Q_{g2}$ we get:

$$Q_{g2}(x) = C_{eq} \cdot (V'_{bG} - V'_G) \quad \text{(A. 30)}$$

where

$$\frac{1}{C_{eq}} = \frac{1}{C_{ox1}} + \frac{1}{C_{Si}} + \frac{1}{C_{ox2}} \quad \text{(A. 31)}$$

Using (A. 5) and (A. 13), inversion charge expression (A. 14) becomes:

$$Q_{inv1}(x) = -q \cdot n_i \cdot \frac{t_{Si}}{2} \cdot U_T \cdot e^{\frac{\Psi_{s1}(x) - V(x)}{U_T}} \cdot \frac{\tanh\left(\frac{C_{eq}}{C_{Si}} \cdot \frac{V'_{bG} - V'_G}{2 \cdot U_T}\right)}{\frac{C_{eq}}{C_{Si}} \cdot \frac{V'_{bG} - V'_G}{2 \cdot U_T}} \quad \text{(A. 32)}$$

Using (A. 19) and (A. 30), we get:

$$V'_{bG} - V'_G = \left[1 + \frac{1}{C_{ox1}} \cdot \frac{C_{Si} \cdot C_{ox2}}{C_{Si} + C_{ox2}}\right] \left(V'_{bG} - \Psi_{s1}(x)\right) \quad \text{(A. 33)}$$

And consequently we have:

$$\Psi_{s1}(x) = \frac{V'_G + (n_{s1} - 1)V'_{bG}}{n_{s1}} \quad \text{(A. 34)}$$

The front interface inversion charge writes:

$$Q_{inv1}(x) = -n_{s1} \cdot C_{ox1} \cdot U_T \cdot e^{\frac{V'_G - V'_{TH1} - n_{s1} \cdot V(x)}{n_{s1} \cdot U_T}} \quad \text{(A. 35)}$$

Where $V_{TH1}$' is the threshold voltage of the front gate inversion, which is dependent on the back gate voltage:

$$V'_{TH1} = n_{s1} \cdot U_T \cdot \ln\left(\frac{2 \cdot n_{s1} \cdot C_{ox1} \cdot U_T}{q \cdot n_i \cdot t_{Si}}\right) - (n_{s1} - 1) \cdot V'_{bG} - n_{s1} \cdot U_T \cdot \ln\left(\frac{\tanh\left(\frac{C_{eq}}{C_{Si}} \cdot \frac{V'_{bG} - V'_G}{2 \cdot U_T}\right)}{\frac{C_{eq}}{C_{Si}} \cdot \frac{V'_{bG} - V'_G}{2 \cdot U_T}}\right) \quad \text{(A. 36)}$$

Similar expressions can be derived for the back interface inversion charge and threshold voltage, which is dependent on the front gate voltage:

$$Q_{inv2}(x) = -\, n_{s2} \cdot C_{ox2} \cdot U_T \cdot e^{\frac{V'_{bG} - V'_{TH2} - n_{s2} \cdot V(x)}{n_{s2} \cdot U_T}} \quad \text{(A. 37)}$$

$$V'_{TH2} = n_{s2} \cdot U_T \cdot \ln\left(\frac{2 \cdot n_{s2} \cdot C_{ox2} \cdot U_T}{q \cdot n_i \cdot t_{Si}}\right) - (n_{s2} - 1) \cdot V'_G - n_{s2} \cdot U_T \cdot \ln\left(\frac{\tanh\left(\frac{C_{eq}}{C_{Si}} \cdot \frac{V'_{bG} - V'_G}{2 \cdot U_T}\right)}{\frac{C_{eq}}{C_{Si}} \cdot \frac{V'_{bG} - V'_G}{2 \cdot U_T}}\right) \quad \text{(A. 38)}$$

# Appendix B

In Leti-UTSOI2 case, the integration of the 1-D Poisson's equation (A. 1) along with the boundary conditions, result in three coupled equations:

$$Q(x)^2 = Q_{g1}(x)^2 - 2 \cdot q \cdot n_i'(x) \cdot \varepsilon_{Si} \cdot U_T \cdot e^{\frac{\Psi_{s1}(x)}{U_T}} \quad \text{(B. 1)}$$

$$Q(x)^2 = Q_{g2}(x)^2 - 2 \cdot q \cdot n_i'(x) \cdot \varepsilon_{Si} \cdot U_T \cdot e^{\frac{\Psi_{s2}(x)}{U_T}} \quad \text{(B. 2)}$$

$$\frac{Q(x)}{2 \cdot C_{Si} \cdot U_T} + \coth^{-1}\left(\frac{Q_{g1}(x)}{Q(x)}\right) - \coth^{-1}\left(-\frac{Q_{g2}(x)}{Q(x)}\right) = 0 \quad \text{(B. 3)}$$

where Q(x) is a coupling charge that can be real (hyperbolic mode) or imaginary (trigonometric mode). The originality of Leti-UTSOI2 is the form of the equation (B. 3) as there is no need to know a priori the mode of operation (hyperbolic or trigonometric). Using a $\coth^{-1}$ instead of $\tanh^{-1}$ as in [58], simplifies the solution as no more sign-function is required. A rearrangement of (B. 3) using a coth identity provides three useful equivalent equations, and the derivation in [84] ends up with a single equation that is solved analytically to calculate the surface potentials $\psi_{s1}$ and $\psi_{s2}$ using an initial guess and correction steps. Once surface potentials are calculated, the inversion charge is obtained for all levels of inversion as a sum of a front and back inversion charges using front and back gate charges and capacitances [84].

In order to obtain the drain current expression, the general expression (2.9) is used with an effective average mobility $\mu_{eff}$. An effective electrostatic potential is defined as:

$$x_{drift} = \frac{V(x)}{U_T} + \ln\left(-\frac{Q_{inv}}{C_{Si} \cdot U_T}\right) \quad \text{(B. 4)}$$

and its value is calculated at the source and drain side using the inversion charge density and its derivative with respect to $x_{drift}$ at both the source and drain. Then, knowing $x_{drift}$ value at the source and drain, the charge density along the channel is derived. The analytical integration of the inversion charge with respect to $x_{drift}$ results

in a closed form of the drain current $i_{ds}$ [30]. The mobility model is treated as usually in compact models including Coulomb, phonon, and surface roughness scattering to calculate the effective mobility $\mu_{eff}$. The difference with respect to bulk is that Leti-UTSOI2 is considering a repartition of the effective mobility into front and back parts.

The drain current expression is given as:

$$I_D = \frac{W}{L} \frac{\mu_{eff}}{\sqrt{1 + \left(\frac{\mu_{eff} \cdot U_T}{v_{sat}} \cdot \frac{\delta x_{driftds}}{L}\right)^2}} \cdot C_{Si} {U_T}^2 \cdot i_{ds} \tag{B. 5}$$

where $v_{sat}$ is the saturation velocity, $\delta x_{driftds}$ is the difference of $x_{drift}$ value between drain ($x_{driftd}$) and source ($x_{drifts}$), and ids is given as:

$$\begin{aligned} i_{ds} = \left(-q_{im} - \frac{U_s + U_d}{4}\right) \delta x_{driftds} + \frac{L_d U_d - L_s U_s}{4(d_d - d_s)} \\ + 9(d_d - d_s) \ln\left(\frac{L_d + U_d}{L_s + U_s}\right) - (q_{is} - q_{id}) \end{aligned} \tag{B. 6}$$

where $q_{is}$ and $q_{id}$ are the inversion charge density at the source and drain respectively, $d_s$ ($d_d$) is the derivative of $q_{is}$ ($q_{id}$) with respect to $x_{drift}$, and :

$$\begin{aligned} L_d &= q_{is} - q_{id} + d_s\left(x_{drifts} - x_{driftd}\right) \\ L_s &= q_{is} - q_{id} + d_s\left(x_{drifts} - x_{driftd}\right) \\ U_s &= \sqrt{L_s^2 + 36(d_d - d_s)^2} \\ U_d &= \sqrt{L_d^2 + 36(d_d - d_s)^2} \\ q_{im} &= \frac{q_{is} + q_{id}}{2} \end{aligned} \tag{B. 7}$$

# Appendix C

Table C. 1 summarizes the physical effects that are taken into account in the industrial model.

Table C. 1 Physical effects involved in UTBB FDSOI MOSFET

| Physical effect | Modeling and support |
|---|---|
| Back interface inversion / dual channel operation | This is the main particularity of the double gate architecture. No limitation on the back gate biasing condition. |
| Ground-plane depletion | The highly doped region underneath the BOX can be accumulated or depleted, which alters the effective BOX oxide thickness. The effect is modeled as in bulk PSP as the region underneath the BOX is considered as the channel of a Bulk MOSFET. |
| Quantum confinement | The quantum well physically formed by the thin silicon film between the front and back dielectrics. The second aspect is the vertical field induced quantum well. Both are taken into account and modeled. |
| Velocity saturation | Velocity saturation is accounted for similarly as in [31]. |
| Short channel effects | The 2D electrostatics is accounted for using the coupling between front gate, back gates, source, and drain. |

| | |
|---|---|
| Channel length modulation | The channel length modulation is implemented as in bulk PSP but using a simpler expression of the relative channel length reduction. |
| Series resistance with gate voltage dependence | Source and drain series resistances are implemented as in bulk PSP model, by adding a term to the mobility degradation factors. |
| Parasitic currents: Gate current, GIDL/GISL | Gate leakage and both gate induced drain leakage (GIDL) and gate induced source leakage (GISL) are accounted for as in [141]. |
| Parasitic capacitances: overlap, fringe | In addition to the intrinsic charge model, overlap and fringe capacitance models are included similar to the implementation in PSP. Bias independent source, drain, and gate to substrate capacitances are also included. |
| Self-heating effect | An RC lumped circuit is included to model the self-heating effect in the silicon film. Recently, a thermal terminal is included to allow custome implementations of the thermal resistance and capacitance. |
| Stress model | Besides STI stress model, a model dedicated to strained-FDSOI technologies is introduced. |
| Noise model: Flicker, thermal, induced gate, shot | Low frequency flicker noise, thermal noise, induced gate noise, and shot noise models are included. The excess noise is being implemented as well. |
| Source/drain junction asymmetry | Simplified symmetric or asymmetric source/drain junction models. |

# Appendix D

In order to validate model dependence on drain to source voltage $V_{DS}$, input characteristics are shown in Fig. D. 1 in linear scale to highlight the operation in SI regime. Same characteristics are shown in logarithmic scale in Fig. D. 2. For short channel (L = 30 nm), DIBL effects is reproduced in Fig. D. 2 (left) while the effects are not evidenced for longer channel (right).

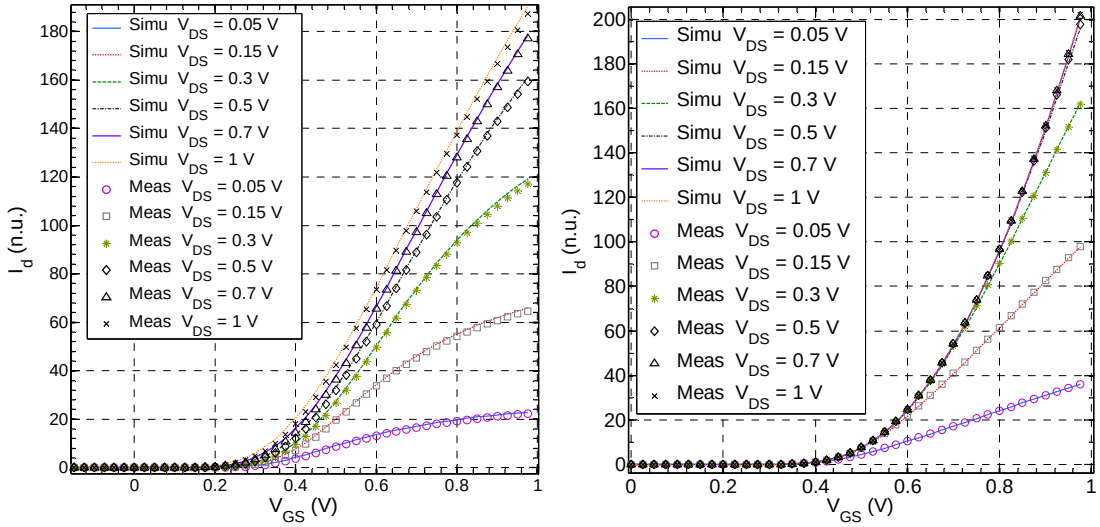


Fig. D. 1 Normalized drain current versus $V_{GS}$ for NMOS with L=30nm (left) and L=1µm (right) at various $V_{DS}$ (from 50mV to 1V).

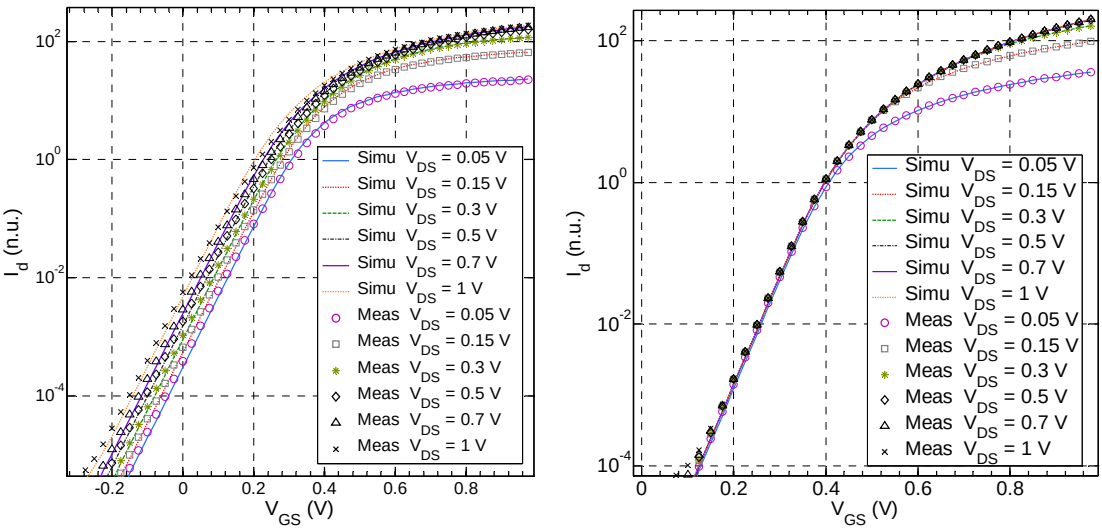


Fig. D. 2 Normalized drain current in logarithmic scale versus $V_{GS}$ for NMOS with L=30nm (left) and L=1µm (right) at various $V_{DS}$ (from 50mV to 1V).

Transconductance is shown in Fig. D. 3 for a short (left) and long (right) evidencing an accurate reproduction. The Transconductance derivative shown in Fig. D. 4, which is important for RF operation, are correctly reproduced using parameters that are extracted with no optimization.

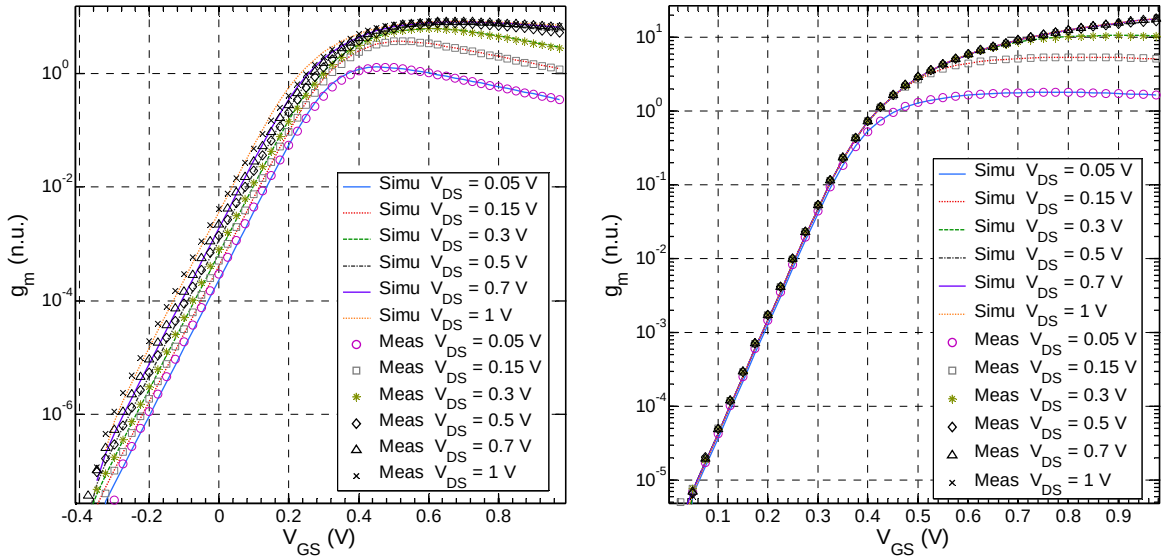


Fig. D. 3 Normalized transconductance in logarithmic scale versus $V_{GS}$ for NMOS with L = 30nm (left) and L = 1 µm (right) at various $V_{DS}$ (from 50 mV to 1 V).

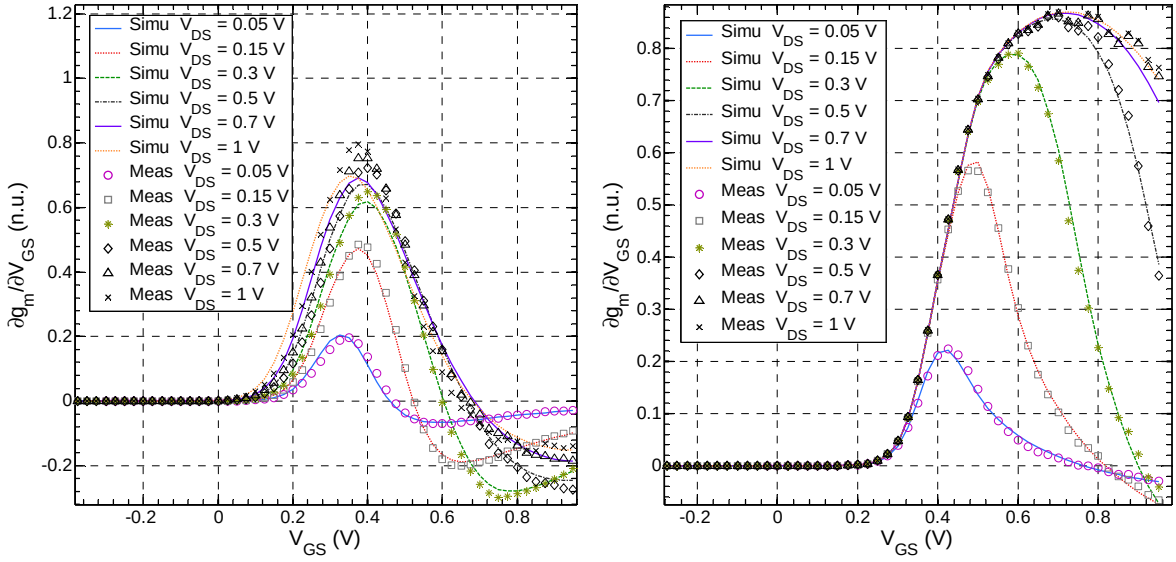


Fig. D. 4 Transconductance derivative versus $V_{GS}$ for NMOS with L = 30 nm (left) and L = 1 µm (right) at various $V_{DS}$ (from 50 mV to 1 V).

Output characteristics in linear and logarithmic scales are shown in Fig. D. 5 and Fig. D. 6, respectively. The logarithmic scale highlights the region where DIBL is detrimental. All output characteristics are accurately reproduced linear and saturation.

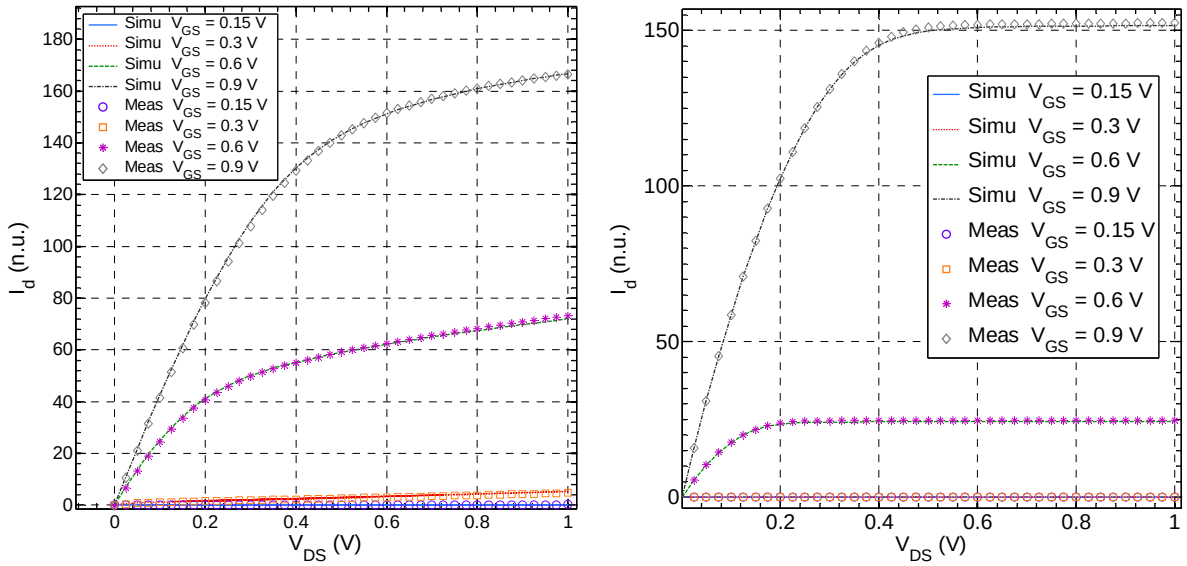


Fig. D. 5 Normalized drain current in linear scale versus $V_{DS}$ for NMOS with L = 30 nm (left) and L = 1 µm (right) at various $V_{GS}$ (from 150 mV to 0.9 V).

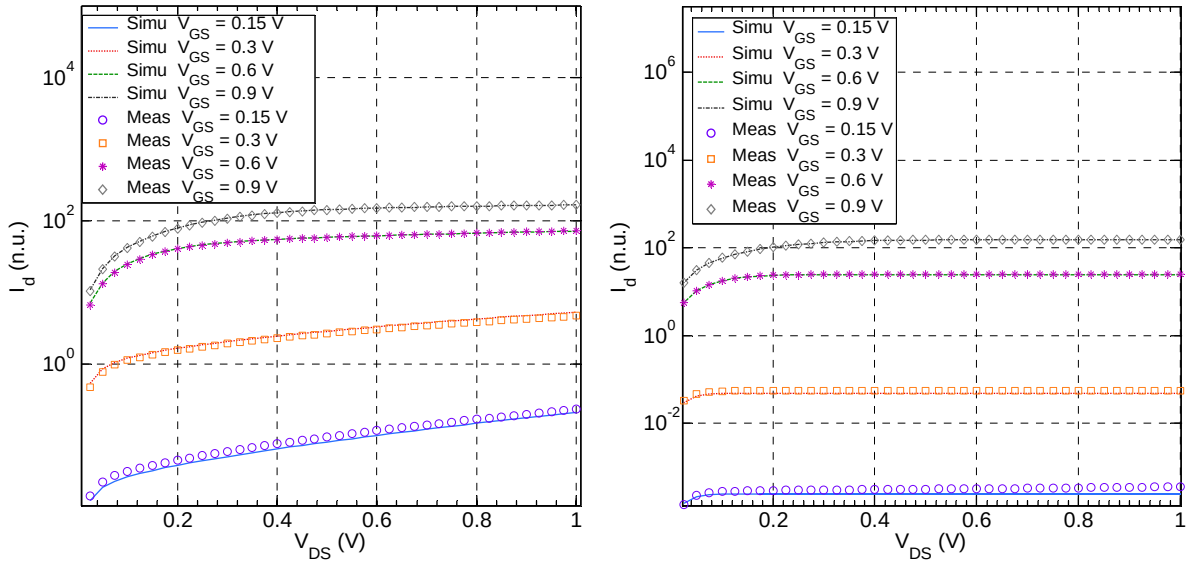


Fig. D. 6 Normalized drain current in logarithmic scale versus $V_{DS}$ for NMOS with L = 30 nm (left) and L = 1 µm (right) at various $V_{GS}$ (from 150 mV to 0.9 V).

Output conductance $g_{ds}$ is shown in Fig. D. 7 and its derivative in Fig. D. 8. All first order and second order parameters are satisfactorily reproduced. An accurate $g_{ds}$ reproduction along with an accurate transconductance $g_m$ simulation lead to an accurate prediction of the intrinsic gain, which is given by:

$$A_v = \frac{g_m}{g_{ds}} \qquad \text{(D. 1)}$$

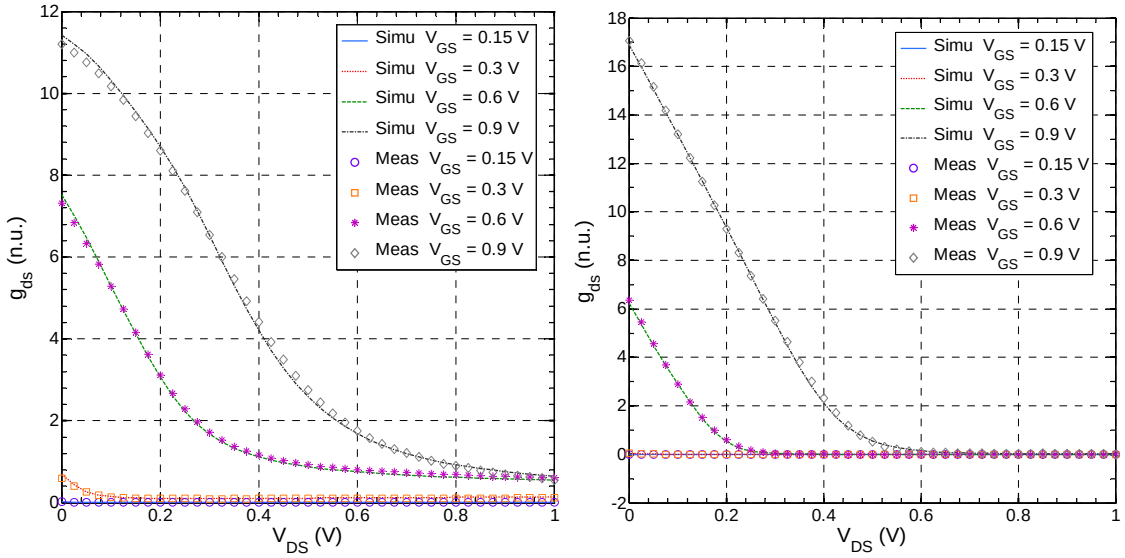


Fig. D. 7 Normalized conductance versus $V_{DS}$ for NMOS with L = 30 nm (left) and L = 1 µm (right) at various $V_{GS}$ (from 150 mV to 0.9 V).

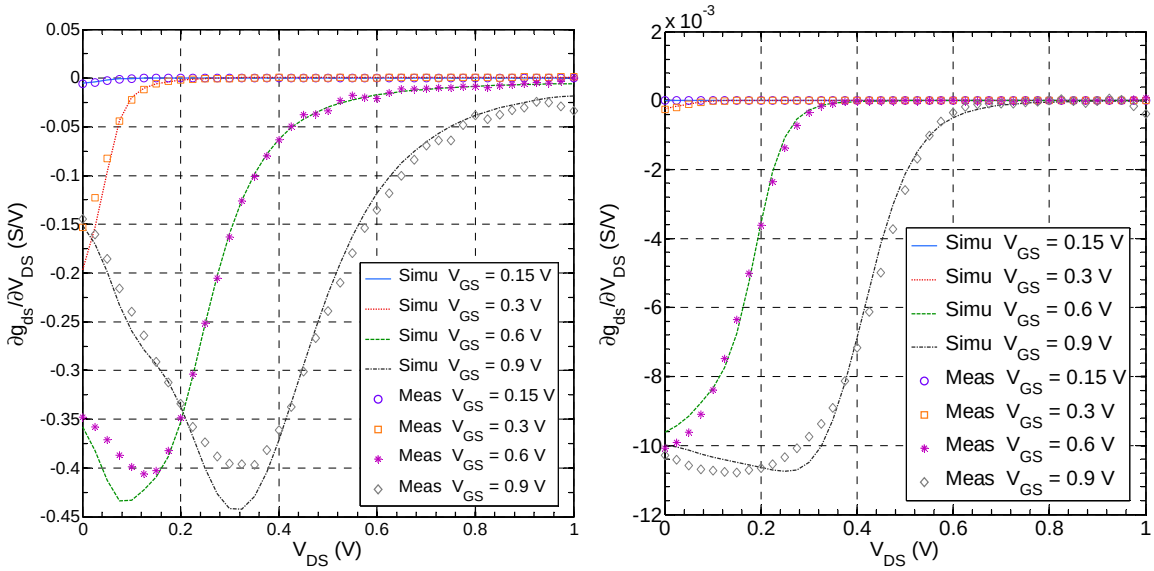


Fig. D. 8 Conductance derivative versus $V_{DS}$ for NMOS with L=30nm (left) and L=1µm (right) at various $V_{GS}$ (from 150mV to 0.9V).

# Appendix E

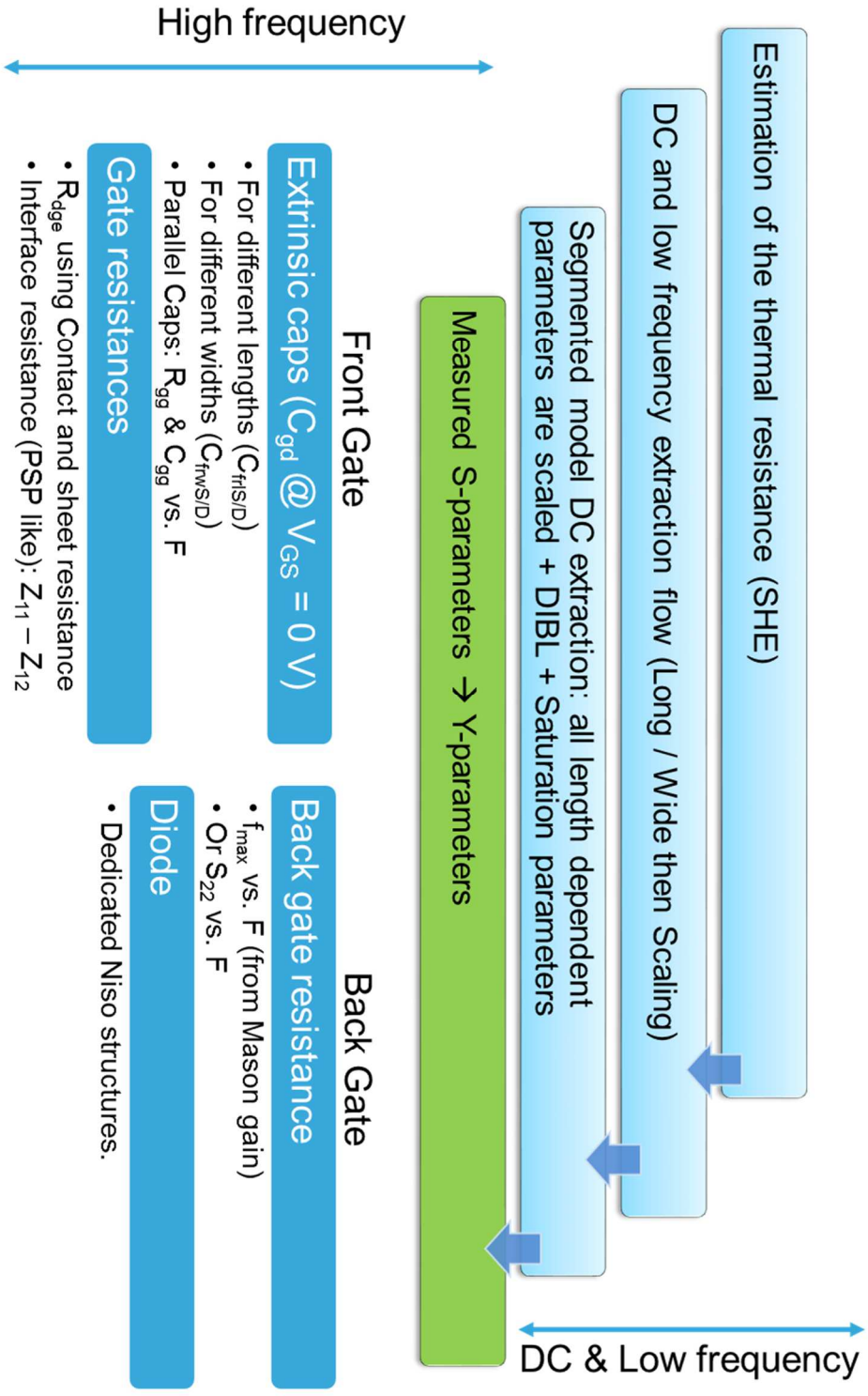


Fig. E. 1 A summary of the complete NQS model parameters extraction flow.

# List of publications

## Papers in international peer review journals

[1] **S. E. Ghouli**, D. Rideau, F. Monsieur, P. Scheer, G. Gouget, A. Juge, T. Poiroux, J. M. Sallese, and C. Lallement, “Experimental gm/ID Invariance Assessment for Asymmetric Double-Gate FDSOI MOSFET,” *IEEE Transactions on Electron Devices*, vol. 65, no. 1, pp. 11–18, Jan. 2018.

## Papers in international peer review journals (submitted)

[2] **S. E. Ghouli**, J. M. Sallese, A. Juge, P. Scheer, and C. Lallement, “Transadmittance efficiency in presence of NQS transport in Asymmetric Double Gate FDSOI MOSFET,” submitted to *IEEE Trans. Electron Devices*.

## Papers in international peer review journals (under submission)

[3] **S. E. Ghouli**, J. M. Sallese, A. Juge, and C. Lallement, “On the mobility extraction using NQS effect,” under submission to *IEEE Trans. Electron Devices* as a brief article.

## International conferences with proceedings and peer review process

[4] T. Poiroux, O. Rozeau, S. Martinie, P. Scheer, S. Puget, M. A. Jaud, **S. E. Ghouli**, J. C. Barbé, A. Juge, and O. Faynot, “UTSOI2: A complete physical compact model for UTBB and independent double gate MOSFETs,” in 2013 *IEEE International Electron Devices Meeting (IEDM)*, 2013, p. 12.4.1-12.4.4.

[5] **S. E. Ghouli**, P. Scheer, M. Minondo, A. Juge, T. Poiroux, J. M. Sallese, and C. Lallement, “Analog and RF modeling of FDSOI UTBB MOSFET using Leti-UTSOI model,” in 2016 *MIXDES - 23rd International Conference Mixed Design of Integrated Circuits and Systems*, 2016, pp. 41–46.

[6] **S. El Ghouli**, W. Grabinski, J. M. Sallese, A. Juge, and C. Lallement, “Analog RF and mm-Wave Design Tradeoff in UTBB FDSOI: Application to a 35 GHz LNA,” 25th

IEEE International Conference “Mixed Design of Integrated Circuits and System” (*MIXDES)*. Oral presentation, 2018, pp. 57-62

[7] O. Rozeau, S. Martinie, T. Poiroux, J-C. Barbé, F. Gilbert, X. Montagner, **S. El Ghouli**, Geet D. J. Smit, Andries J. Scholten, “New physical insight for analog application in PSP bulk compact model,” in 2018 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 2018. Oral presentation.

### International conference without proceedings

[8] **S. El Ghouli**, P. Scheer, T. Poiroux, A. Juge, J. M. Sallese, and C. Lallement, “Dynamic behavior of the UTBB FDSOI MOSFET,” presented at the *MOS-AK Workshop*, Grenoble, France, Mar-2015. Oral presentation.

[9] **S. El Ghouli**, A. Juge, J.M. Sallese and C. Lallement, “DC Operating Point Information limitations in Subckt based models and solutions”, *Mentor Graphics forum*, Grenoble, France, November 2015. Oral presentation.

[10] **S. El Ghouli**, A. Juge, J.M. Sallese and C. Lallement, “New SUBCKT DC Operating Point Information feature”, *Synopsys TRM*, Montbonnot, France, May 2017. Oral presentation.

# Résumé de thèse

## Table des matières

# Introduction

La miniaturisation du transistor MOS à effet de champ a permis de faire des progrès considérables tant au niveau performance des circuits qu'au niveau de leur coût de fabrication. Toutefois, la diminution drastique de la taille du transistor est confrontée à des limitations majeures telles que les effets canaux courts et la variabilité particulièrement à partir du nœud technologique 20 nm. La poursuite de l'intégration vers les nœuds technologiques plus denses nécessite désormais l'utilisation de nouveaux matériaux et de nouvelles architectures pour le transistor à effet de champ. Dans ce domaine, deux principales alternatives sont proposées : l'architecture 3D de type FinFET, et l'architecture planaire de transistor MOS complètement désertée, à canal non dopé et intégrée sur film de silicium et d'isolant ultra-minces (UTBB FDSOI, pour Ultra-Thin Body and Box Fully-Depleted SOI). De par son aspect planaire, le transistor UTBB FDSOI étudié dans cette thèse est moins exposé à l'impact des éléments parasites et par conséquent plus adapté aux applications analogiques et RF. Néanmoins, il n'existe pas de modèle industriel suffisamment précis et efficace de ce type de transistor pour la conception des circuits hautes fréquences (RF et millimétriques) à faible consommation. Par ailleurs, les méthodes de conception des circuits à faibles niveaux d'inversion du transistor MOS privilégiant ainsi une faible consommation font défaut pour la nouvelle génération des transistors MOS à plusieurs grilles.

C'est dans ce contexte que s'inscrit cette thèse qui se propose de faire une étude et une modélisation du comportement fréquentiel du transistor MOS du type UTBB FDSOI dans le but de servir la conception de circuits dédiés aux signaux Analogiques Mixtes, Hautes Fréquences, et nécessitant une très faible consommation.

Les travaux ont permis d'appréhender les phénomènes complexes intervenants dans les 7 nm du film du silicium et de proposer un modèle non-quasi-statique précis jusqu'à 110 GHz.  Les résultats obtenus dans le cadre de cette thèse ouvrent la voie vers l'exploitation de la technologie UTBB FDSOI dans la conception des circuits

encore plus autonomes et plus performants pour étendre les applications de l'internet des objets.

La **première partie** de la thèse dresse un état de l'art de la modélisation des transistors MOS en lien avec les besoins de la conception des circuits. La **deuxième partie** est consacrée à la description du comportement DC et faible fréquence du dispositif étudié. Cette description est principalement axée sur les caractéristiques mesurées courant-tension et capacité-tension. La **troisième partie** est dédiée à l'étude de l'invariance de la notion de l'efficacité de la transconductance (la transconductance divisée par le courant). L'invariance est étudiée en fonction de la tension de la grille arrière, de la longueur du canal, de la température, de la tension $V_{DS}$ et des variations dues au processus de fabrication. La **quatrième partie** propose une étude du comportement haute fréquence allant jusqu'à 110 GHz et la modélisation associée, respectivement intrinsèque et extrinsèque, du transistor MOS UTBB FDSOI. Dans la **cinquième partie**, la notion de l'efficacité de la transconductance a été généralisée pour couvrir tous les modes de fonctionnement du transistor en basses et hautes fréquences. L'étude du comportement non-quasi-statique est basée sur cette notion généralisée. Enfin, en s'appuyant sur les modèles et méthodes proposées dans les parties précédentes, le dimensionnement d'un amplificateur à faible bruit (LNA) est présenté dans la **sixième partie**, en exploitant le régime d'inversion modérée du transistor MOS UTBB FDSOI.

# I. Etat de l’Art

Au cours des cinq dernières décennies, l'industrie du semiconducteur a été principalement régie par la miniaturisation progressive du transistor selon la loi de Moore jusqu'à atteindre l'échelle nanométrique. La loi de Moore porte principalement sur la réduction des coûts, et l'aspect économique a entraîné une démocratisation des dispositifs électroniques. Récemment, de nouveaux matériaux et de nouvelles architectures ont été utilisés pour surmonter les limitations des effets canaux courts et l’effet couramment appelé DIBL causés par la proximité entre la source et le drain. Ces nouvelles solutions sont inévitables, en particulier en dessous du nœud technologique 20 nm.

Afin de réduire le courant de fuite à l'état bloqué du transistor MOSFET, l’effet de la grille sur la distribution du potentiel dans le canal doit être amélioré. Des matériaux à constante diélectrique élevée (high-k) ont été introduits depuis le nœud technologique 45 nm afin d’améliorer le contrôle de la grille tout en réduisant les fuites du courant par effet tunnel [1]. Toutes les techniques d'amélioration utilisées dans les nœuds technologiques précédents ont un effet limité dans les nœuds proche du 20 nm. En effet, la dégradation de la mobilité due aux effets de collision limite la concentration de dopants dans le canal et le seuil de la contrainte du réseau freine l'amélioration de la mobilité dans les canaux contraints [2][3]. Avec les limitations ci-dessus, de nouvelles architectures du transistor MOSFET avec plusieurs grilles ont été proposées pour poursuivre la réduction de la taille du transistor. Le premier travail publié au sujet du transistor MOSFET à double grilles, [4], montre une réduction significative des effets canaux courts dans les MOSFET FDSOI grâce à l’addition d’une grille à l’arrière du canal. Avec cette architecture, l'influence du champ électrique du drain sur le canal est réduite. Cependant, le transistor MOSFET à double grille fabriqué en premier était le transistor DELTA complètement appauvri qui est similaire au FinFET mais sans le masque supérieur [5]. Deux architectures ont été finalement adoptées et sont en production aujourd'hui: le double-grille symétrique appelé FinFET et le double-grille asymétrique appelé UTBB FDSOI. Les deux différences

fondamentales entre les deux solutions technologiques sont l'orientation des grilles et des canaux d'une part, et la connexion des deux grilles d'autre part. Le FinFET est fondamentalement un transistor double-grille dans lequel les deux grilles sont connectées. Cependant, dans un MOSFET UTBB FDSOI, les deux grilles ne sont pas connectées et peuvent être polarisées différemment. Sinon, le FinFET et l'UTBB FDSOI se ressemblent comme illustré dans la Fig. 1 et proposent des performances digitales comparables [6]. Le comportement RF du FinFET est cependant affecté par un grand nombre d'éléments parasites [7][8][9][10]. La Fig. 2 montre un comparatif de la fréquence de transition $f_T$ de différents MOSFET avancés en fonction de la longueur de grille. L'UTBB FDSOI présente une $f_T$ supérieure par rapport au FinFET grâce à une résistance parasite et des éléments capacitifs réduits. De plus, les attentes de l'organisme ITRS (International Technology Roadmap for Semiconductors) sont satisfaites par l'UTBB FDSOI et confirmées par nos mesures de la géométrie nominale avec une longueur de L = 30 nm d'un NMOS et d'un PMOS comme représenté sur la Fig. 3.

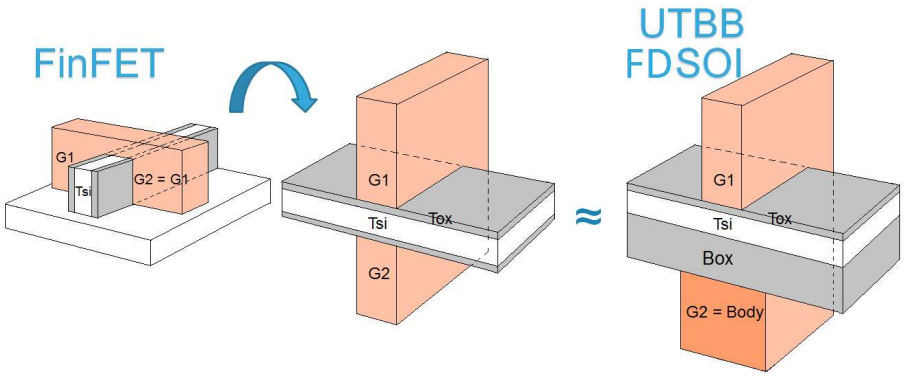


Fig. 1 Comparaison du FinFET (à gauche) et de l'UTBB FDSOI (à droite).

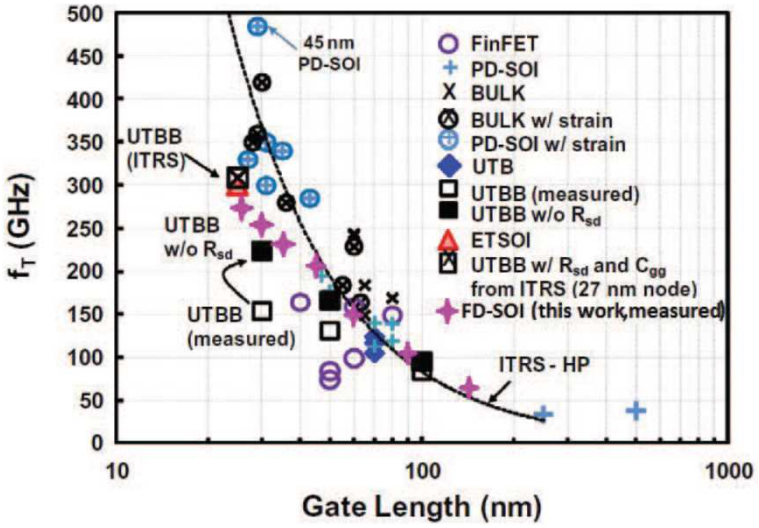


Fig. 2 Comparatif de la fréquence de transition $f_T$ pour différents transistors MOSFET avancés en fonction de la longueur de grille [10].

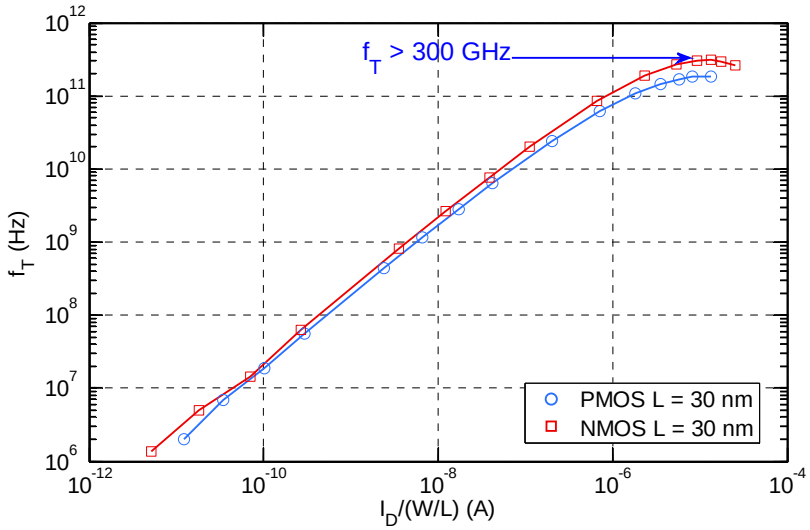


Fig. 3 La fréquence de transition $f_T$ en fonction du courant de drain normalisé $I_D$ /(W/L) pour l'UTBB FDSOI NMOS et PMOS (L = 30 nm).

Une propriété importante des transistors MOSFET double-grille (i.e. FinFET, UTBB FDSOI, etc.) à savoir l'inversion volumique (IV) a été découverte en 1987 [11]. L'inversion volumique se produit dans des films de silicium très minces contrôlés par deux grilles, ce qui est le cas dans un transistor MOSFET UTBB FDSOI où les porteurs de la charge mobile ne sont pas confinés dans les interfaces Si/SiO2 comme le prédit la physique classique du semi-conducteur. Ce phénomène est illustré en utilisant nos simulations TCAD dans la partie 2 et mis en évidence en utilisant nos données mesurées dans les parties 2, 3 et 5. Le confinement quantique dans le film de Si mince est à l'origine de l'effet de l'IV [12]. Bien que le phénomène de l'inversion volumique

soit démontré, sa modélisation est souvent négligée et l'approximation des charges surfaciques est considérée par défaut [13][14]. Des résultats assez précis sont obtenus en modélisant l'effet de confinement quantique à l'aide d'un décalage appliqué aux tensions des grilles ou aux dimensions verticales dans [15] et [16], et en utilisant le concept de centroïde de la charge d'inversion dans [17]. De plus, des charges d'inversion multiples (avant et arrière) et une mobilité des porteurs variant verticalement sont considérées afin de calculer la charge totale et la mobilité effective [15][18]. En fait, le calcul de la concentration d'électrons en présence du confinement doit passer par la résolution des équations de Poisson et de Schrödinger de manière cohérente, mais cela est souvent ignoré. La Fig. 4 présente la densité électronique simulée dans le film de silicium de 7 nm d'épaisseur (cf. Fig. 5) d'un MOSFET UTBB FDSOI pour différentes tensions de grille arrière $V_{bG}$ et pour une tension de grille avant fixe $V_{GS}$ = 1 V en utilisant l'outil de simulation Synopsys Sentaurus TCAD. Les différentes valeurs de $V_{bG}$ génèrent un champ électrique vertical variant dans le film qui contrôle, à son tour, l'intensité de l'inversion volumique et par conséquent la concentration verticale des porteurs de charge. Pour $V_{bG}$ = 2 V, la densité électronique est presque constante loin des deux interfaces Si/SiO2 avant et arrière.

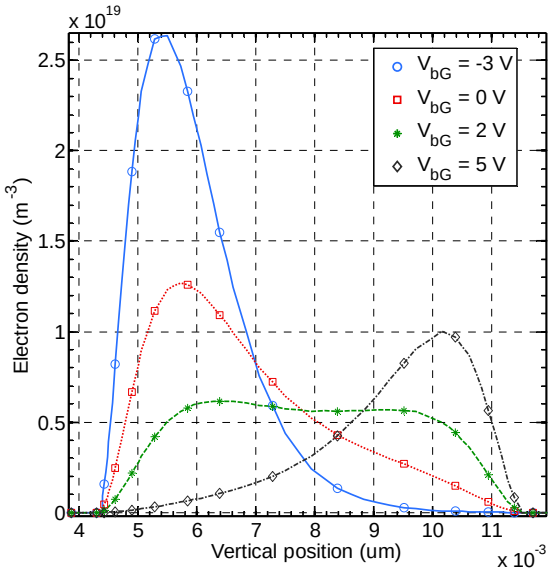


Fig. 4 Densité électronique simulée dans le film de silicium à différentes tensions de grille arrière $V_{bG}$ pour un NMOS FDSOI UTBB (L = 1 µm & W = 1 µm) en saturation et forte inversion (à $V_{GS}$ = 1 V).

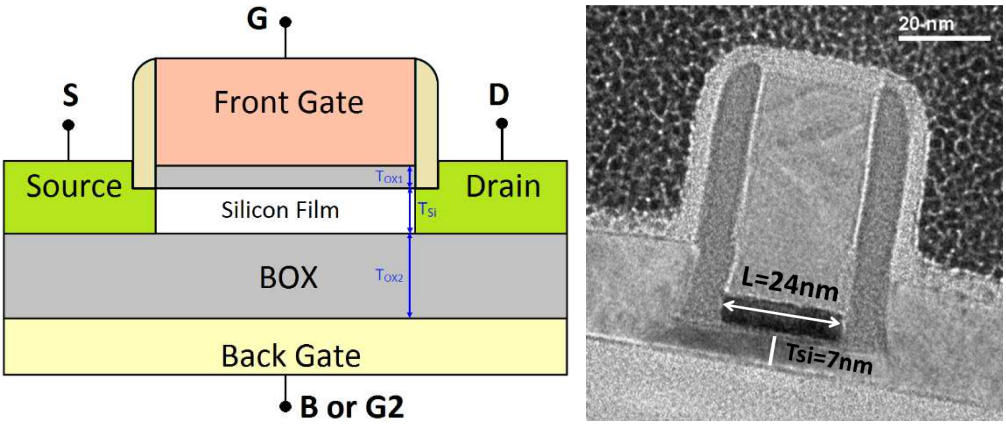


Fig. 5 Coupe transversale (gauche) et TEM (droite [19]) du MOSFET UTBB FDSOI.

Quatre modèles compacts sont disponibles pour la simulation MOSFET UTBB FDSOI: BSIM-IMG [16], HISIMSOTB [14], UFDG [20] et Leti-UTSOI2 [21]. Trois modèles sont des standards ou des candidats à la standardisation dans l'industrie du semiconducteur: BSIM-IMG, HISIMSOTB et Leti-UTSOI2. Tous les modèles sont basés sur la physique, évolutifs et efficaces pour les simulations de circuits. Tous ces modèles compacts incorporent plusieurs effets physiques, tels que les effets canaux courts (SCE), la dégradation de la mobilité, la saturation de vitesse, la résistance série, la modulation de la longueur du canal (CLM), les effets de la mécanique quantique, le courant de l'effet tunnel dans la grille, le DIBL et les capacités parasites. Leti-UTSOI2 (ou UTSOI2) est le premier modèle compact à double grilles indépendantes capable de décrire précisément le MOSFET UTBB FDSOI dans toutes les conditions de polarisation.

# II. Le comportement DC et basse fréquence

Le fonctionnement à haute fréquence d'un transistor MOSFET est étroitement lié à sa condition de polarisation, et par conséquent à son fonctionnement en courant continu (DC). L'opération quasi-statique à haute fréquence peut être considérée comme une évaluation des dérivations multiples de l'opération DC, en ce sens qu'elle balaie une partie de la caractéristique I-V et "détecte" ses variations. Lorsque les variations de la tension appliquée aux terminaux du transistor sont suffisamment faibles, l'hypothèse du petit signal peut être considérée et des relations linéaires entre les variations de courant produites et les variations de tension d'entrée peuvent être utilisées. Par conséquent, une seule dérivation de la caractéristique I-V est suffisante pour prédire le comportement du MOSFET dans l'hypothèse d'un petit signal. La prédiction précise des dérivées de la caractéristique DC repose évidemment sur un modèle DC très précis. Par conséquent, un modèle précis pour le fonctionnement DC du transistor UTBB FDSOI est une nécessité.

Un modèle compact sert de lien entre le processus de fabrication et la conception du circuit. C'est une description mathématique compacte de la physique des dispositifs complexes avec un compromis entre la précision et l'efficacité du calcul et le temps CPU induit. Un modèle compact basé sur la physique du dispositif permet à la fois aux technologues et aux concepteurs de circuits de prédire le comportement du transistor au-delà des données mesurées utilisées pour extraire le modèle. Comme pour les modèles du transistor MOSFET à grille unique, les modèles compacts disponibles pour le MOSFET double-grille reposent sur un cœur d'un modèle canal long auquel s'ajoutent divers effets physiques tels que les effets canaux courts (SCE), la dégradation de la mobilité, la saturation de la vitesse et les effets quantiques (QME).

Les technologies FinFET et SOI entièrement déplété (FDSOI) remplissent les exigences ITRS (International Technology Roadmap for Semiconductors) pour la miniaturisation des dispositifs. Comme indiqué dans la première partie, les deux

architectures permettent un excellent contrôle du canal ayant comme conséquence directe de très hautes performances en ce qui concerne les applications digitales grâce au contrôle des deux grilles et au film mince de silicium [22][23][24]. En revanche, grâce à des éléments parasites réduits, il a été démontré que la technologie FDSOI planaire avec un film et un BOX ultra-minces (UTBB) présente d'excellentes performances analogiques et RF et surpasse les technologies bulk et FinFET sur différents aspects RF [25][26]. En outre, le MOSFET UTBB FDSOI surpasse le FinFET en termes de fréquences de coupure comme le montre la Fig. 2 [10]. Le MOSFET UTBB FDSOI est par conséquent un meilleur candidat pour les applications faible puissance et basse tension.

Dans les circuits avancés de faible puissance et de haute performance tels que ceux mis en œuvre dans le marché FDSOI pour l'internet des objets, il est nécessaire de faire fonctionner les transistors MOSFET dans des régimes de faibles à forts niveaux d'inversion [27]. Il convient de souligner qu'une région d'inversion modérée s'est avérée être un bon compromis quand la consommation d'énergie et la vitesse sont considérées avec le même niveau de priorité [28][9][29]. L'inversion modérée fournit une transconductance plus élevée pour un courant plus faible, et une bande passante qui reste acceptable pour les applications faible puissance et basse tension. L'importance de la région d'inversion modérée et les problèmes de modélisation associés sont soulignés dans [30].

Afin de profiter pleinement des avantages de la technologie FDSOI, les modèles compacts MOSFET doivent reproduire fidèlement le comportement du transistor dans toutes les régions d'opération, en particulier en faible inversion. Pour les calculs manuels souvent entrepris dans le monde du design analogique, bien que les modèles classiques de loi exponentielle en faible inversion et de loi carrée en forte inversion puissent être utilisés avec précaution, les abaques basés sur la notion du $g_m/I_D$ développées dans la partie suivante sont plus pratiques pour prédire la performance du transistor MOSFET UTBB FDSOI à tous les niveaux d'inversion. De plus, pour un usage industriel et comme il a été mentionné précédemment, UTSOI2 est le premier modèle compact à double grilles indépendantes capable de décrire précisément le MOSFET UTBB FDSOI dans toutes les conditions de polarisation, y compris à des tensions de polarisation élevées appliquées à la grille arrière [15]. Le modèle UTSOI2 a été validé par rapport à des simulations numériques (TCAD) et à des mesures en

courant continu démontrant d'excellentes performances au niveau prédiction et évolution [31]. Cependant, ses performances RF n'ont été mises en évidence que dans [32] et demandent clairement une analyse plus approfondie. Les grandeurs digitales telles que $I_{ON}$ et $I_{OFF}$ ne sont pas suffisantes pour évaluer le comportement analogique d'un transistor MOSFET. De plus, les applications analogiques telles que l'amplification nécessitent une prédiction précise des figures de mérite et des dérivées continues des caractéristiques du transistor MOSFET d'ordre supérieur et dans tous les niveaux d'inversion.

Par conséquent, deux modèles quasi-statiques différents sont considérés dans ces travaux pour le fonctionnement à basse fréquence et sont tous les deux utilisés comme blocs de base pour le développement d'un modèle non-quasi-statique haute fréquence amélioré: (1) un circuit équivalent petit signal présenté dans la Fig. 6 et (2) le modèle UTSOI2.

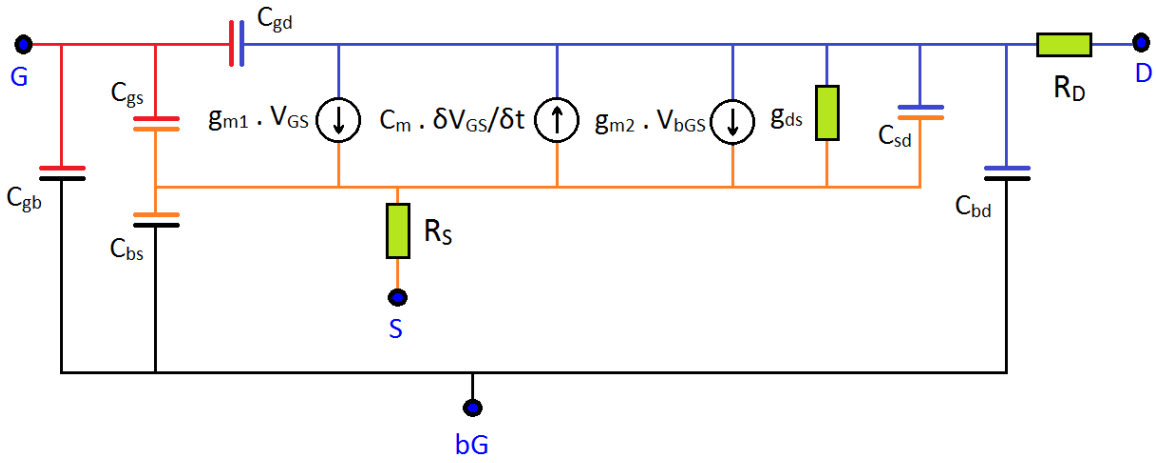


Fig. 6 Schéma équivalent petit signal et quasi-statique du transistor MOSFET UTBB FDSOI prenant en compte les résistances série $R_S$ et $R_D$ ($C_{gd} = C_{gdi} + C_{gde}$ et $C_{gs} = C_{gsi} + C_{gse}$). $C_m$, $g_{m1}$, $g_{m2}$ et $g_{ds}$ étant respectivement la transcapacité mutuelle, la transconductance avant, la transconductance arrière et la conductance.

Les travaux présentés dans cette partie se concentrent sur la description et la modélisation du comportement DC et basse fréquence du transistor MOSFET UTBB FDSOI. L'opération sous l'influence des deux grilles est présentée et comparée à l'opération de la grille simple dans la technologie bulk en utilisant des données mesurées. La capabilité du modèle à décrire le comportement DC ainsi que le petit signal (à faible et haute fréquences) est évaluée en mettant l'accent sur des conditions de polarisation à basse tension.

Des simulations TCAD (cf. Fig. 7) sont également effectuées en utilisant deux decks TCAD différents qui sont basés sur le simulateur de processus et de dispositifs Sentaurus de Synopsys Inc.: (1) un deck simple sans source et drain surélevés et utilisant une mobilité de porteurs constante pour capturer les effets de premier ordre; (2) un deck calibré avec la source et le drain surélevés, et un modèle avancé de mobilité [33]. Le deck TCAD calibré de la technologie FDSOI 28 nm est cruciale pour l'évaluation de l'impact de la grille arrière dans le fonctionnement à basse et haute fréquences.

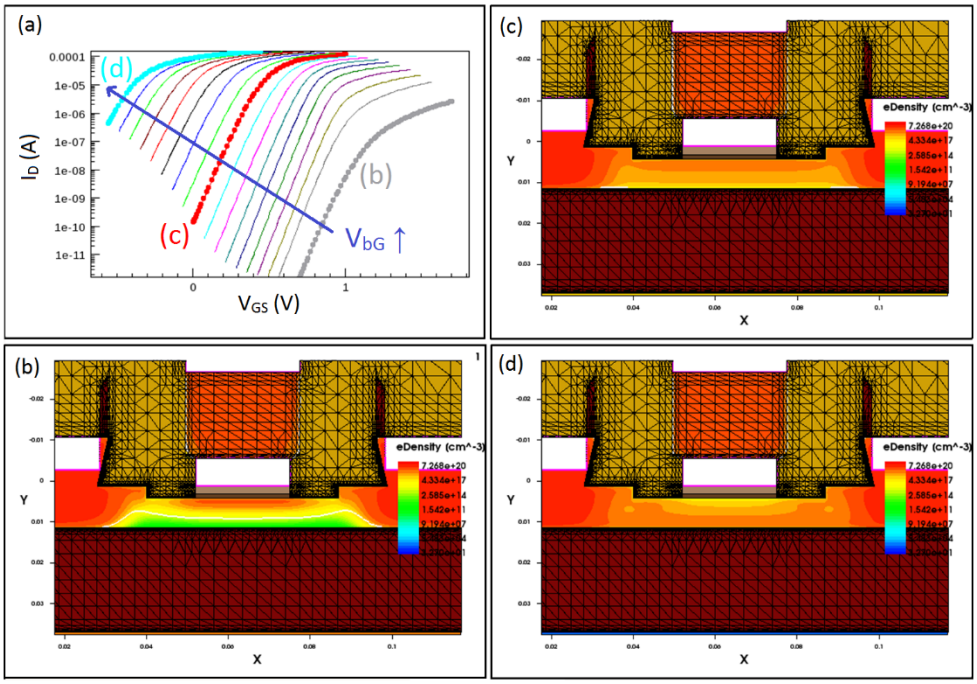


Fig. 7 Simulations TCAD montrant l'impact de la tension de la grille arrière sur la concentration des porteurs et par conséquent sur la caractéristique d'entrée $I_D$-$V_{GS}$. (a) $I_D$-$V_{GS}$ pour différents $V_{bG}$ allant de -10 V à 8 V. (b) inversion du canal à l'avant pour $V_{bG}$ négatif = -10 V (c) inversion du canal dans le volume de film de silicium à $V_{bG}$ = 0 V, et (d) inversion du canal avec un max local près de l'interface arrière pour $V_{bG}$ = 8 V.

L'opération en basse fréquence et DC du MOSFET UTBB FDSOI est décrite à l'aide des données mesurées et des simulations TCAD, en particulier pour les faibles niveaux d'inversion. Ensuite, le modèle quadratique du canal long en bulk est comparé à son équivalent double-grille. La comparaison montre des similitudes profondes entre les deux approches. Le circuit équivalent petit signal proposé est évalué en comparaison avec le modèle basé sur UTSOI2. Le circuit équivalent est utile pour une

évaluation simple des circuits. Les caractéristiques des deux modèles sont comparées aux mesures en mettant l'accent sur l'inversion modérée (cf. Fig. 8).

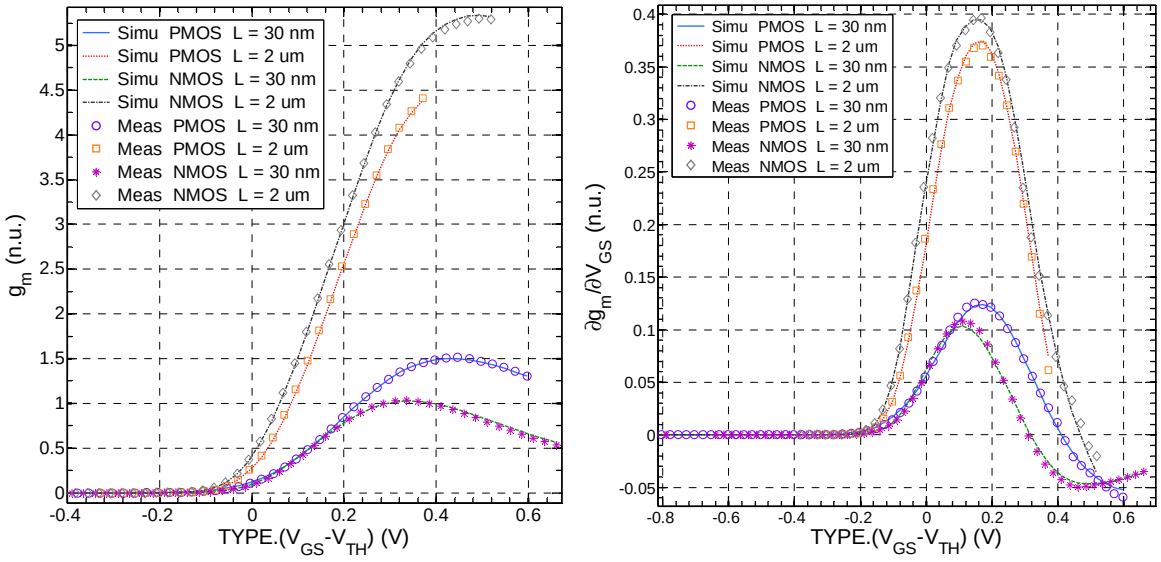


Fig. 8 La transconductance normalisée (à gauche) et sa dérivée (à droite) en fonction de $V_{GS} – V_{TH}$ en mode linéaire $|V_{DS}| = 0.3$ V pour deux longueurs NMOS et PMOS (L = 30 nm et 2 µm), $W_f = 2$ µm et $N_f = 10$ à T = 25 °C.

Enfin, la fonctionnalité importante DC OP Info des simulateurs Spice pour la conception analogique est revue tout en signalant ses limitations actuelles. Une amélioration est finalement proposée avec des résultats prometteurs.

# III. Évaluation de l'invariance du $g_m$ sur $I_D$

Les transistors MOSFET entièrement déplétés à double grille (DG) présentent une immunité inhérente aux effets canaux courts, une pente sous le seuil abrupte et un courant plus élevé [11]. L'architecture double grilles indépendantes élargit encore plus l'espace de conception des circuits car les deux grilles peuvent être contrôlées indépendamment l'une de l'autre. Comme discuté précédemment, ces structures avancées sont sélectionnées pour poursuivre la miniaturisation agressive de la technologie CMOS présentant d'excellentes performances digitales et analogiques, en particulier dans les applications de faible puissance [24][10].

Dans les circuits avancés de faible puissance et de haute performance, il est crucial de faire fonctionner les transistors MOSFET dans tous les niveaux d'inversion de faibles à forts [27]. De plus, la région d'inversion modérée s'est avérée être un bon compromis quand la consommation d'énergie et la vitesse sont considérées avec les mêmes priorités [28][9][29]. Pour tirer pleinement parti du potentiel des technologies récentes, en particulier en inversion faible et forte, une conception efficace des circuits analogiques repose encore sur des calculs manuels. Ces calculs traditionnels nécessitent des modèles de transistors MOSFET simplifiés qui sont supposés être valides dans les régimes d'inversion faibles et forts.

Malheureusement, les approximations d'inversion forte et faible ne prédisent pas correctement le courant de drain ($I_D$) en inversion modérée et il n'y a pas de modèle assez simple pour l'analyse manuelle qui est suffisamment prédictif notamment pour les transistors à grille multiples [34][35]. La situation s'aggrave encore avec les technologies avancées et à échelle réduite où la mobilité effective, la saturation de la vitesse des porteurs et les résistances série dominent à des niveaux d'inversion faible. Par conséquent, l'approximation quadratique de l'inversion forte n'est valable que près du début de l'inversion forte et inappropriée ailleurs. Les transistors sont donc exploités avec moins d'efficacité lorsque des méthodes traditionnelles sont utilisées, ce qui peut conduire à une conception des circuits inefficace [36].

Les pratiques dépassées rappelées ci-dessus concernant les calculs manuels empêchent les concepteurs analogiques de tirer pleinement parti des technologies modernes (haute efficacité de la transconductance et faible $V_{DSAT}$). Afin de remédier à la faiblesse des pratiques traditionnelles, où des concepts discutables tels que la

tension d'Early, le $V_{GS}$-$V_{TH}$ et la loi quadratique classique sont utilisés, la méthodologie de conception basée sur l'efficacité de la transconductance ($g_m/I_D$) a été proposée [37]. L'approche $g_m$ sur $I_D$ repose sur l'aspect fondamental et universel de la caractéristique représentant l'efficacité de la transconductance en fonction du courant de drain normalisé dans les MOSFET à grille unique. Une telle caractéristique est considérée comme invariante indépendamment de la tension de seuil et de la longueur à condition que les effets canaux courts soient considérés comme négligeables [37][38] . Cette invariance est étudiée dans ces travaux de thèse pour un transistor double-grille asymétrique. L'objectif est de vérifier dans quelle mesure la méthodologie de conception mentionnée ci-dessus et basée sur le $g_m/I_D$ est valable pour les transistors à grilles doubles asymétriques avancées telles que l'UTBB FDSOI. La méthodologie de conception basée sur le $g_m/I_D$ est brièvement expliquée. Les simulations TCAD rappellent l'effet de la grille arrière sur l'efficacité de la transconductance de la grille avant déjà discutée précédemment. La normalisation de l'efficacité de transconductance et du courant pour un transistor à double grille est décrite. Le dispositif expérimental est décrit et l'invariance de la caractéristique représentant l'efficacité de la transconductance en fonction du coefficient d'inversion (IC) est évaluée à l'aide des données expérimentales obtenues (cf. Fig. 9).

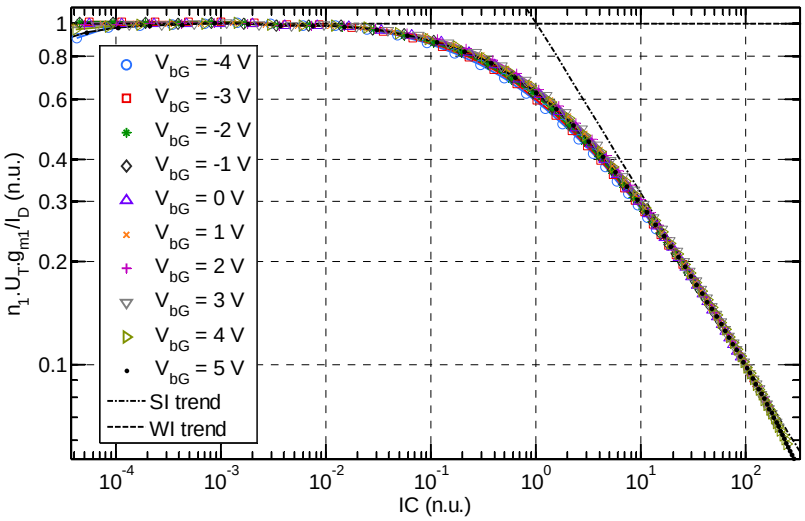


Fig. 9 $g_m/I_D$ normalisé en fonction du coefficient d'inversion IC à différentes valeurs de $V_{bG}$ pour un NMOS (L = 1 µm & W = 1 µm) en saturation ($V_D$ = 1V) à T = 25 °C.

# IV. Opération haute fréquence

De nos jours, nous pouvons avoir accès à l'information presque partout grâce à la technologie sans fil. Des progrès remarquables ont été réalisés pour répondre aux différentes exigences en matière de portée, allant des réseaux Bluetooth à courte portée aux réseaux cellulaires et satellites à longue portée. Selon le théorème de Shannon, la capacité du canal et par conséquent le débit des données de communication dépendent de la bande passante et du rapport signal sur bruit. Une façon d'augmenter le débit de données est de se déplacer vers des fréquences plus élevées où plus de bande passante est disponible [39]. Avec les performances élevées en hautes fréquences des nœuds technologiques avancés, les applications à ondes millimétriques à coût réduit basées sur la technologie CMOS sont maintenant possibles malgré le fait que le CMOS, à l'origine, n'est pas optimisé pour les performances millimétriques. Cependant, la réalisation de certaines applications millimétriques utilisant les technologies CMOS implique le fonctionnement à des fréquences très élevées et proches des "limites" de fonctionnement des transistors (c'est-à-dire les fréquences $f_T$ et $f_{max}$). Diverses applications fonctionnent aujourd'hui dans la bande millimétrique, comme le contrôle de la vitesse automatique à longue distance pour l'automobile à 77 GHz et d'autres applications telles que l'USB sans fil à 60 GHz [40][41]. Avec de telles applications, les circuits CMOS ont de nouvelles opportunités de fonctionnement au-dessus de 60 GHz. Par conséquent, des modèles MOSFET RF et millimétriques précis sont requis. Il faut noter que la caractérisation et la modélisation sont des étapes délicates pour le fonctionnement à haute fréquence du transistor MOSFET.

Comme illustré dans la Fig. 10, à haute fréquence, la capacité d'amplification du transistor tend à diminuer et les modèles quasi-statiques ne permettent pas de reproduire ce comportement. Non seulement la transadmittance mutuelle $y_m$ (i.e. $y_{21}$-$y_{12}$) acquière une partie imaginaire, mais aussi les parties réelles et imaginaires diminuent en amplitude et le déphasage augmente. Ce phénomène est observé pour toutes les géométries et les conditions de polarisation, en particulier pour les dispositifs

à canaux longs. Le déphasage de $y_m$ signifie que l'excitation de la tension au terminal de la grille est en retard sur le courant généré au terminal de drain. Ce retard est dû aux effets distribués qui se produisent dans la structure MOSFET et qui ne sont modélisés ni dans le circuit équivalent de la Fig. 6 ni dans le modèle compact Leti-UTSOI2. La méthode de caractérisation RF et millimétrique est brièvement décrite et des solutions de modélisation sont proposées pour les parties intrinsèques et extrinsèques des structures UTBB FDSOI. Le modèle proposé est finalement validé en utilisant des mesures jusqu'à 110 GHz. Le modèle final est représenté dans Fig. 11.

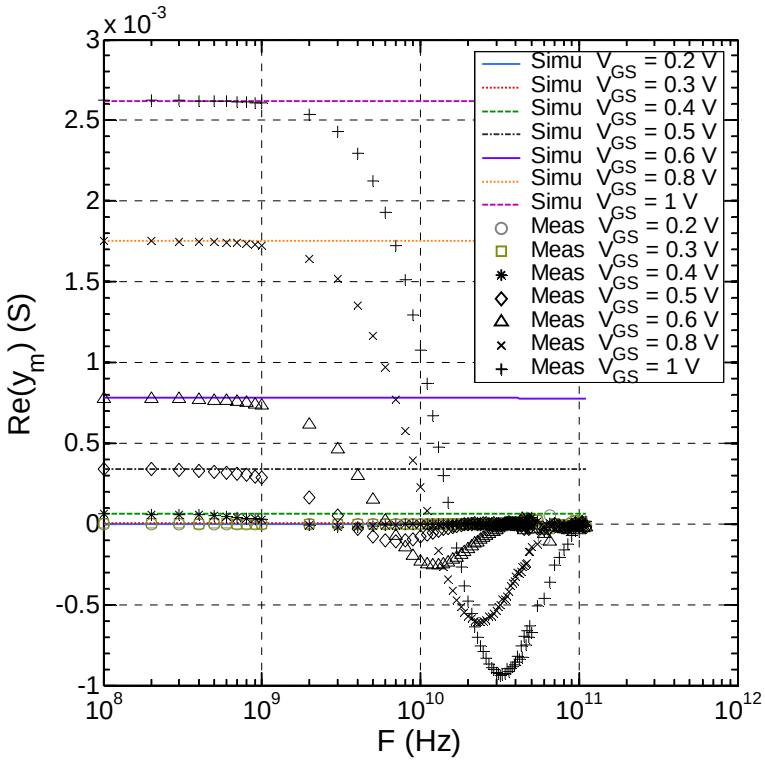


Fig. 10 La partie réelle de la transadmittance mutuelle $y_m$ mesurée et simulée d'un canal long L = 1 µm pour différentes tensions de grille couvrant tous les niveaux d'inversion en saturation ($V_{DS}$ = 1 V).

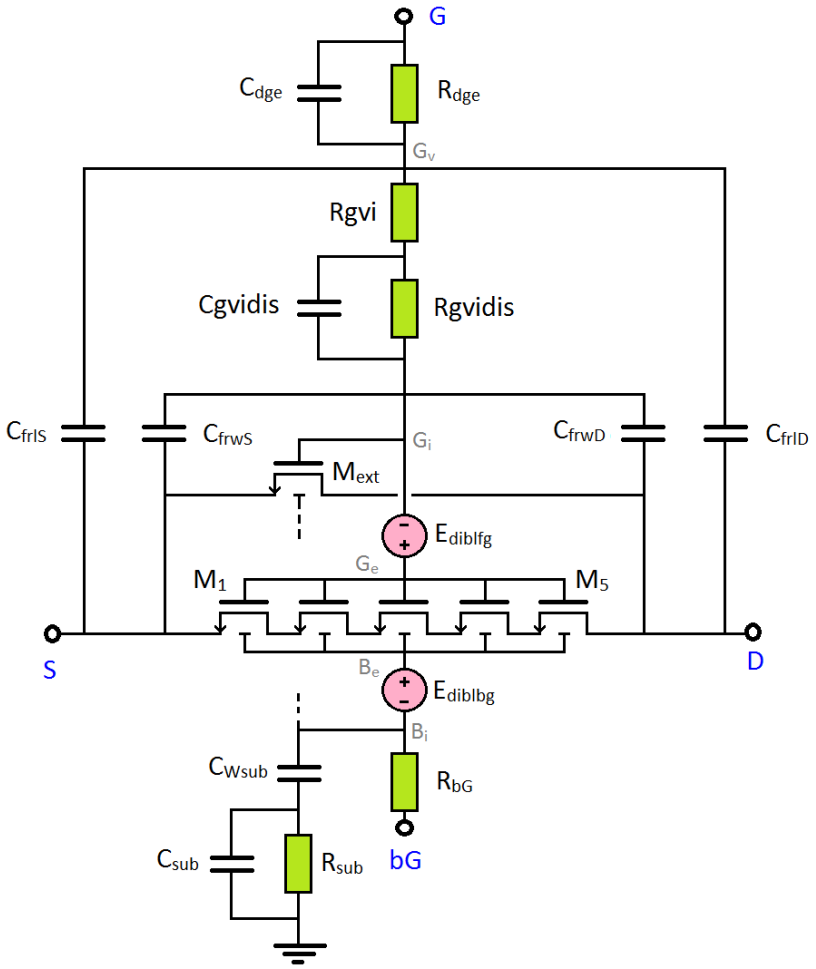


Fig. 11 Modèle non-quasi-statique complet.

La comparaison du modèle proposé avec les données mesurées est résumée dans les deux figures : Fig. 12 et Fig. 13.

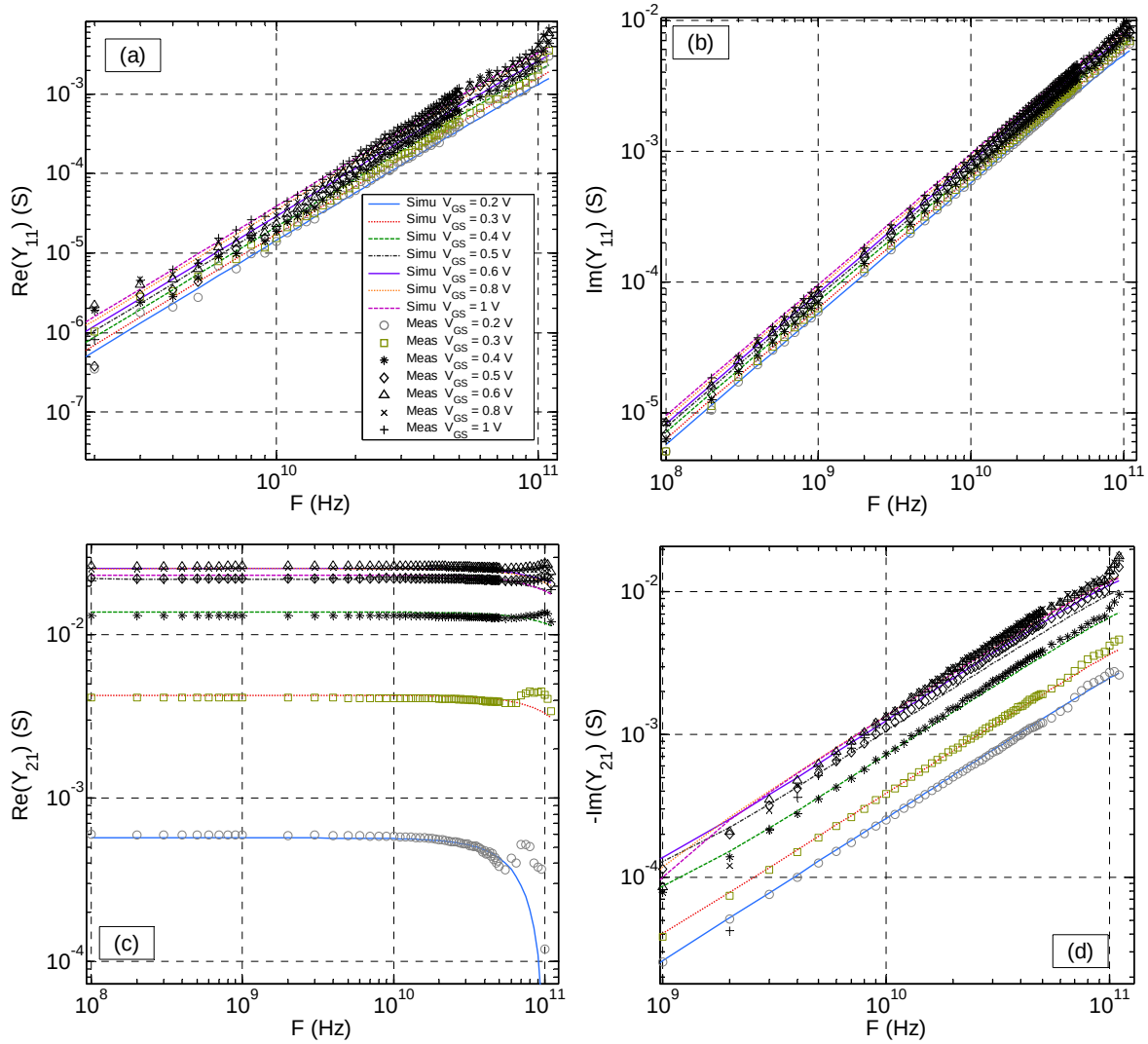


Fig. 12 Simulation et mesures de la transadmittance d'entrée $Y_{11}$ et de la transadmittance d'entrée-sortie $Y_{21}$ d'un NMOS de 30 nm de long en fonction de la fréquence pour diverses tensions de grille pour différents niveaux d'inversion en saturation ($V_{DS}$ = 1 V).

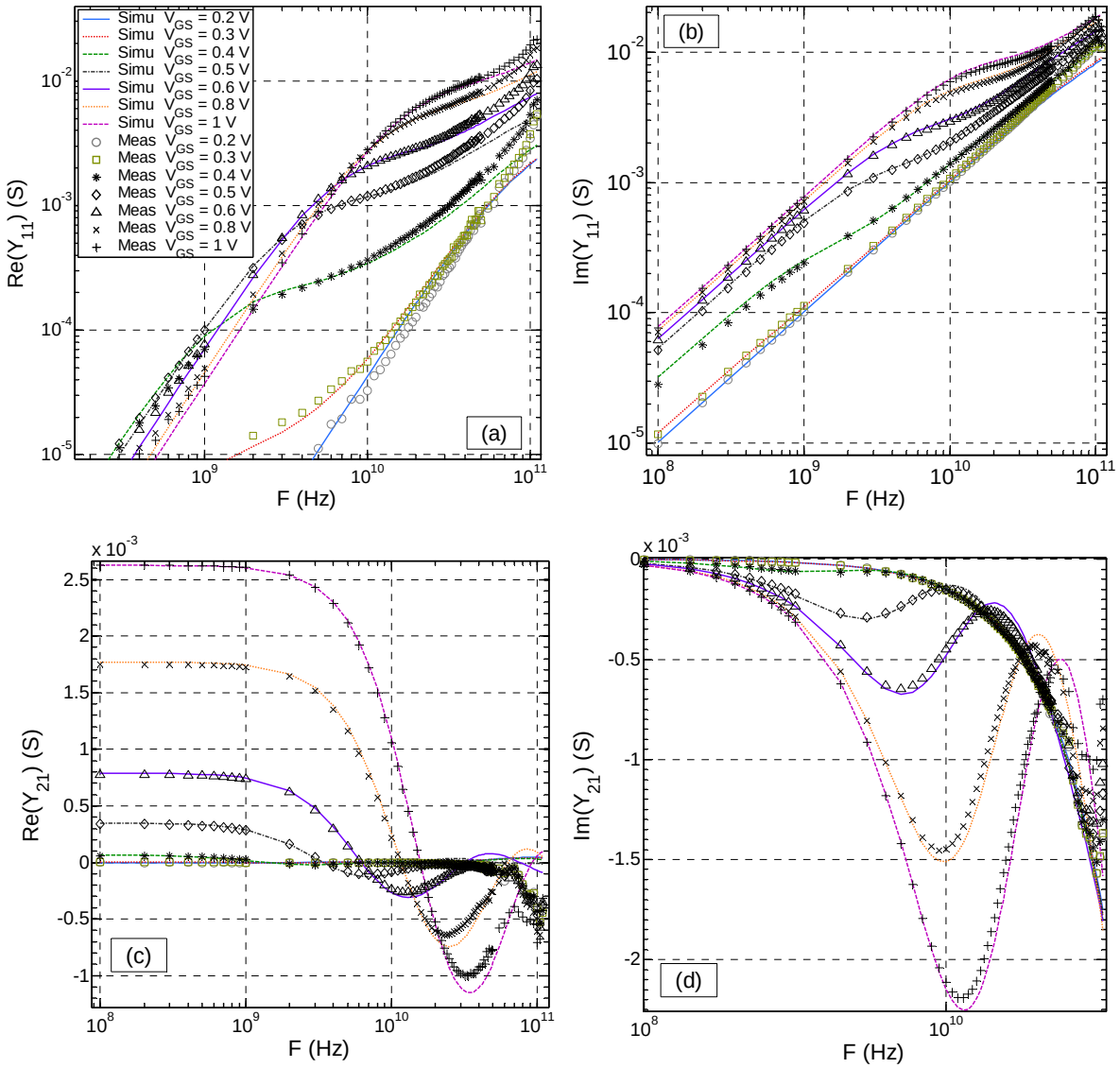


Fig. 13 Simulation et mesures de la transadmittance d'entrée $Y_{11}$ et de la transadmittance d'entrée-sortie $Y_{21}$ de 1 µm de longueur d'un NMOS en fonction de la fréquence pour différentes tensions de grille et pour différents niveaux d'inversion en saturation ($V_{DS}$ = 1 V).

# V. Efficacité de la transadmittance en présence des effets NQS

Les transistors MOSFET RF à base de la technologie CMOS ont été largement utilisés dans les circuits intégrés RF (RFIC) grâce à la miniaturisation. Comme on l'a vu précédemment, les effets canaux courts ont été atténués à l'aide d'architectures novatrices couplées à de nouveaux matériaux [10]. Les nouvelles architectures CMOS permettent un niveau d'intégration plus élevé et un fonctionnement à très hautes fréquences. Pour les applications analogiques et RF, la technologie UTBB FDSOI s'est révélée pertinente, notamment lorsque la consommation d'énergie est une priorité [42]. Les transistors MOSFET UTBB FDSOI présentent des performances analogiques et RF intéressantes grâce à la réduction des capacités et des résistances parasites. De plus, la grille arrière indépendante permet de contrôler la tension de seuil et la mobilité dans le canal [43][42].

La notion de l'efficacité de la transconductance du transistor MOSFET UTBB FDSOI est généralisée et étudiée à haute fréquence pour différents niveaux d'inversion du canal (cf. Fig.  14). L'attention est portée sur l'impact de l'effet non-quasi statique (NQS) sur l'efficacité de la transadmittance. En particulier, la normalisation des grandeurs électrique mène à une simplification de cette figure de mérite fondamentale tout en mettant en avant les niveaux d'inversions modérés (cf. Fig.  15 et Fig.  16).

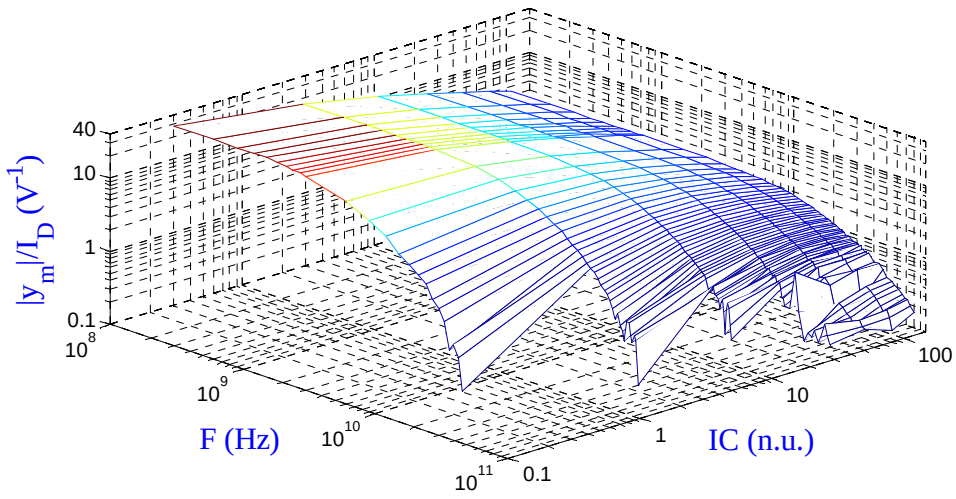


Fig. 14 Tracé 3-D du module de l'efficacité de la transadmittance ($y_m/I_D$) mesuré en fonction de la fréquence et du coefficient d'inversion IC pour L = 1 µm et à $V_{DS}$ = 1 V.

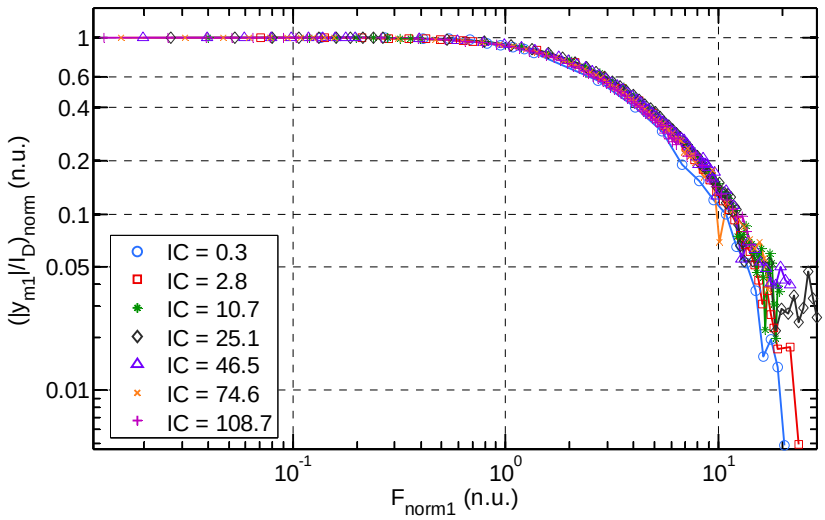


Fig. 15 Module de la transadmittance sur $I_D$ normalisé en fonction de la fréquence normalisée $F_{norm1}$ à différents IC pour un NMOS (L = 1 µm & W = 1 µm) en saturation ($V_{DS}$ = 1 V) et $V_{bG}$ = 0 V (Mesures). $F_{norm1}$ étant la fréquence normalisée en utilisant une fréquence critique représentative de l'effet NQS.

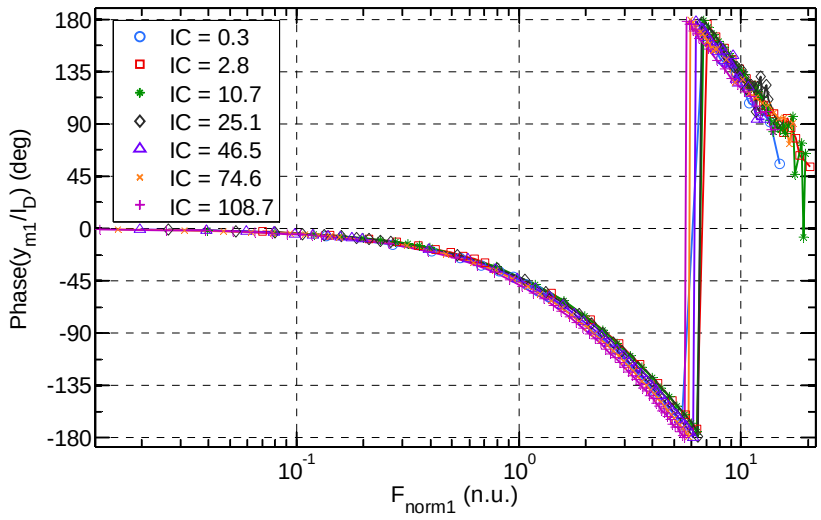


Fig. 16 Phase de la transadmittance sur $I_D$ par rapport à la fréquence normalisée $F_{norm1}$ à différents IC pour NMOS (L = 1 µm & W = 1 µm) en saturation ($V_{DS}$ = 1 V) et $V_{bG}$ = 0 V (Mesures).

L'architecture du dispositif ainsi que la caractérisation haute fréquence sont décrites. Ensuite, nous discutons et validons expérimentalement la généralisation du concept d'efficacité de la transconductance dans les MOSFET UTBB FDSOI proposée à basse fréquence dans la partie 3 et publié dans [42]. L'effet de distribution de la grille est évalué et comparé à l'effet NQS du canal, et une fréquence caractéristique signalant le début de l'effet NQS du canal est définie et comparée à la fréquence de transition $f_T$. La mobilité dans le film de silicium est évaluée en utilisant une nouvelle méthode basée sur des mesures à haute fréquence après la compensation des effets distribués de la grille. Cette mobilité extraite, en utilisant $F_{crit}$ et en tenant en compte des effets distribués dans la grille, est comparée à d'autres méthodes dans Fig. 17.

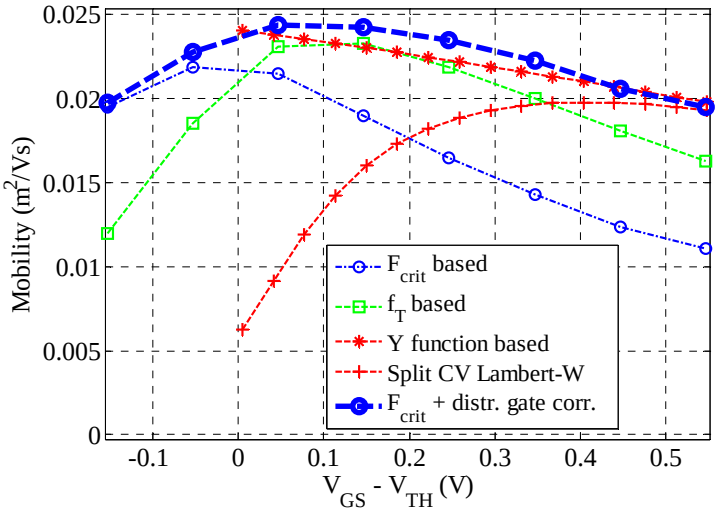


Fig. 17 La mobilité en fonction de $V_{GS}$-$V_{TH}$ pour L = 0.3 µm extraite en utilisant diverses méthodes: en utilisant $F_{crit}$ , en utilisant $f_T$ , en utilisant la fonction Y classique avec itération, en utilisant la fonction Lambert-W et Split C-V et en utilisant $F_{crit}$ avec la correction de l'effet distribué de la grille.

# VI. Application de conception RF et millimétrique

De plus en plus de dispositifs sans fil et des éléments constituant l'internet des objets reposent sur des circuits analogiques et RF CMOS afin d'interagir efficacement avec le monde environnant. Grâce à la miniaturisation, les transistors MOSFET de la technologie CMOS ont été largement utilisés dans les circuits intégrés RF à faible coût et à faible puissance. Les problèmes liés aux canaux courts, comme effets secondaires de la miniaturisation, ont été traités à l'aide de nouvelles architectures et de nouveaux matériaux [5][19]. On rappelle que les nouvelles architectures permettent un excellent contrôle électrostatique [11].

La technologie UTBB FDSOI s'avère être très adaptée aux applications analogiques et RF, en particulier lorsque la consommation d'énergie et la performance sont prises en compte avec le même niveau de priorité. Les transistors MOSFET UTBB FDSOI présentent des performances analogiques et RF élevées grâce à la réduction des capacités parasites et des résistances [10]. De plus, la grille arrière indépendante offre un degré de liberté intéressant qui permet d'atteindre un compromis entre la consommation d'énergie et la performance [43][42].

Plusieurs techniques basées sur la topologie des circuits, telles que la réutilisation du courant, sont proposées pour la conception des circuits analogiques afin d'optimiser les performances et la consommation d'énergie des circuits [44]. Ces techniques sont au-delà du périmètre des travaux entrepris. Les caractéristiques fondamentales du transistor UTBB FDSOI sont utilisées pour un dimensionnement efficace des transistors. En particulier, l'efficacité de la transconductance par rapport au coefficient d'inversion (IC) étudiée précédemment est utilisée pour déterminer la largeur du MOSFET tandis que les courbes représentant la fréquence de transition ($f_T$) en fonction du coefficient d'inversion sont utilisées pour la sélection de la longueur. La méthode de conception utilisant une longueur non minimale et un régime d'inversion modérée (MI) offre un compromis intéressant entre le gain, la consommation d'énergie

et la performance sachant que la largeur du MOSFET est choisie raisonnablement grande et les effets canaux courts sont atténués. Un œil est également gardé sur les limitations des dispositifs passifs dès le début du flot de dimensionnement proposé.

Tout d'abord, les méthodes de conception analogiques classiques, basées sur des règles empiriques et héritées des technologies anciennes, sont brièvement abordées. Deuxièmement, les performances de la technologie UTBB FDSOI pour les applications analogiques et RF sont rappelées. Troisièmement, la méthode de conception basée sur le $g_m/I_D$ est présentée. Quatrièmement, les performances à haute fréquence sont évaluées en fonction de la longueur du transistor et du coefficient d'inversion IC. Enfin, un compromis de conception d'un circuit LNA de 35 GHz dans le régime de l'inversion modérée est proposé. Les résultats du circuit LNA rappelé dans Fig. 18 sont résumés dans Fig. 19.

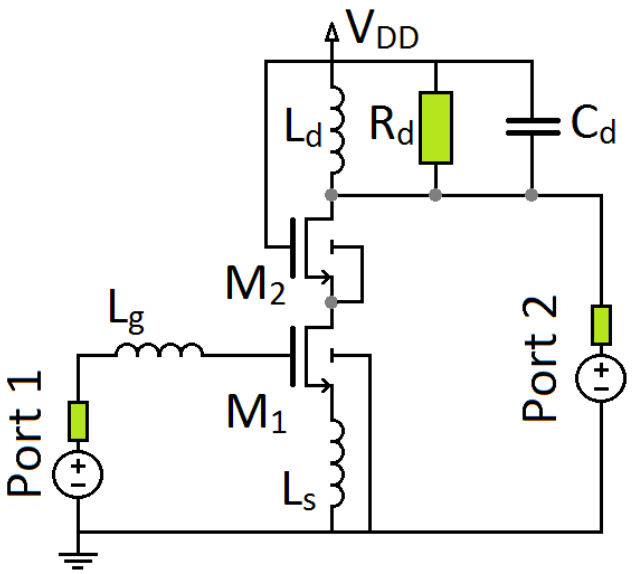


Fig. 18 Circuit représentant un LNA cascode.

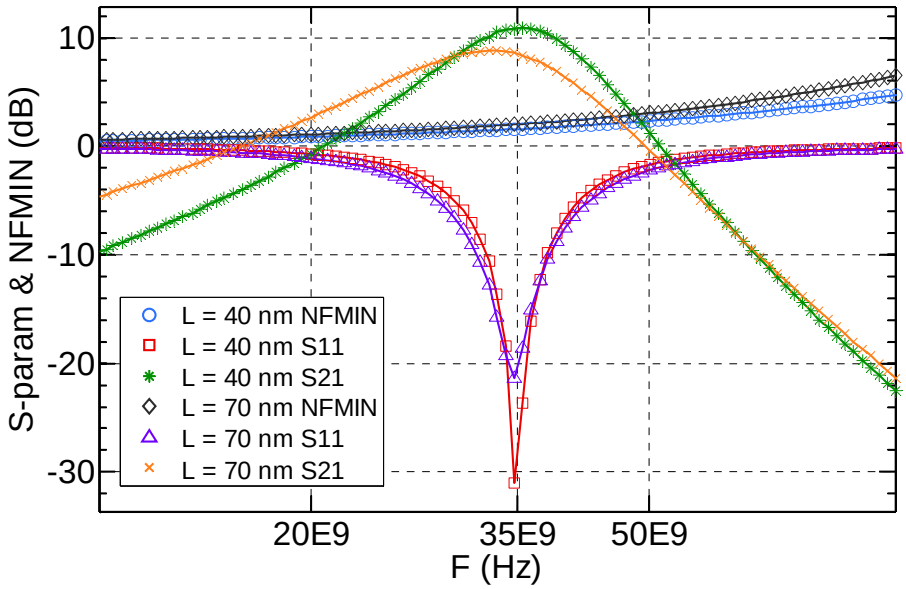


Fig. 19 Gain de puissance $S_{21}$, adaptation à l'entrée $S_{11}$, et NFmin en fonction de la fréquence pour deux circuits LNA (d'abord avec une longueur de MOSFET de 40 nm puis avec L = 70 nm).

# Conclusion générale

La technologie RF basée sur le silicium et la communication sans fil ont eu un impact impressionnant sur nos vies. Le succès est principalement dû à la miniaturisation agressive dictée par la haute performance des circuits digitaux intégrés. Les problèmes préjudiciables liés aux canaux courts ont été mitigés par des scientifiques brillants et des ingénieurs créatifs utilisant de nouvelles architectures pour les transistors et de nouveaux matériaux. Les nouvelles architectures telles que l'UTBB FDSOI étudiées dans ce travail de recherche permettent un excellent contrôle électrostatique, un haut niveau d'intégration, une consommation électrique réduite et une fréquence de fonctionnement très élevée.

En outre, avec ces progrès récents dans l'industrie du silicium, le réseau IoT devient de plus en plus une réalité en termes de son utilisation répandue dans divers aspects de la vie quotidienne. Bien que l'IoT apporte déjà beaucoup d'avantages dans notre vie quotidienne en termes de détection et de communication à l'aide des systèmes RF, des performances plus élevées et plus d'autonomie restent encore à explorer. Par conséquent, les compétences doivent être développées dans les deux domaines clés suivants: (1) Utilisation de la technologie CMOS basée sur le silicium dans le spectre millimétrique et au-delà, et (2) Fonctionnement des transistors à des tensions plus basses.

Compte tenu des besoins mentionnés ci-dessus, le premier objectif de cette thèse a été d'étudier et d'évaluer les capabilités de la technologie UTBB FDSOI nouvellement développée à travers son bloc de construction principal, qui est le transistor MOSFET à double grille. L'autre objectif est d'explorer et d'étendre les approches de modélisation et les méthodes de dimensionnement en basse fréquence au domaine de la haute fréquence, avec un fort accent sur l'inversion modérée où se situe un compromis entre la performance et la consommation d'énergie.

## Résultats du travail de recherche

Les principaux résultats de ce travail de recherche sont résumés ci-après.

**L’Invariance de l'efficacité de la transconductance ($g_m/I_D$) dans un transistor double-grille asymétrique**

Comme le fonctionnement à haute fréquence du transistor MOSFET est étroitement lié à ses conditions de polarisation, l'évaluation du comportement en courant continu (DC) et à basse fréquence était notre première priorité avant de s'attaquer au fonctionnement à haute fréquence. L'une des métriques les plus pratiques qui combine à la fois la capacité d'amplification et la consommation d'énergie est le $g_m/I_D$ à savoir l'efficacité de la transconductance. L'efficacité de la transconductance s'est avérée être un outil de synthèse et de conception essentiel pour les applications analogiques et RF à faible consommation. Pour mieux comprendre le fonctionnement du transistor MOS à des niveaux d'inversion faibles, la figure de mérite ($g_m/I_D$) est étudiée en détail. L’invariance de cette FoM importante tracée en fonction du coefficient d'Inversion IC est analysée pour un transistor MOSFET UTBB FDSOI. L’invariance a été évaluée par rapport à la tension de la grille arrière, à la longueur du transistor, à la température, à la tension $V_{DS}$ et aux variations du processus de fabrication.

L'invariance peut être utilisée pour prédire la transconductance à condition que le ratio W/L et le niveau d'inversion (IC) soient connus. De plus, à l’aide de la courbe supplémentaire d’IC en fonction de $V_{GS}$-$V_{TH}$, on peut prédire le courant de drain à condition que W/L et la tension de grille soient fournies. Cela peut permettre aux concepteurs de prédire les propriétés DC du MOSFET sans avoir besoin d'un modèle analytique y compris en inversion modérée où il est difficile de formuler un modèle simple. Les abaques susmentionnés, épaulés par les capacités MOSFET principales (principalement celles utilisées dans le circuit équivalent proposé) et tracés en fonction du coefficient d’inversion IC, peuvent fournir des prédictions précises des paramètres du circuit équivalent et ainsi remplacer complètement un modèle compact pour des investigations de circuits simples.

En outre, on a démontré expérimentalement que la courbe représentant le $g_m/I_D$ en fonction de IC peut être considérée comme une caractéristique fondamentale des transistors de la technologie UTBB FDSOI et donc être utilisée dans les procédures de dimensionnement et de conception analogiques basées sur le $g_m/I_D$.

**Le concept de l’efficacité de la transadmittance**

Le fonctionnement à haute fréquence est régi à la fois par les éléments extrinsèques du transistor MOSFET et les effets distribués. Des techniques de caractérisation précises avec plusieurs étapes de correction ont été utilisées afin de se débarrasser des éléments parasites liés à la fois au système de mesure et aux connexions. Des structures dédiées SHORT sont utilisées pour extraire les résistances parasites série. La méthode classique OPEN-SHORT est utilisée pour éplucher les paramètres S mesurés. Ces techniques ont permis de mieux comprendre le comportement intrinsèque du transistor MOSFET UTBB FDSOI et ont permis de distinguer deux effets de distribution: l'effet NQS du canal et l'effet de distribution de la grille.

Le comportement NQS du transistor MOSFET UTBB FDSOI est étudié avec un accent particulier sur le régime de l'inversion modérée. La dépendance en fréquence des caractéristiques petits signaux issues des paramètres S est analysée et révèle que le concept de l’efficacité de la transconductance ($g_m/I_D$), déjà adopté en tant que figure de mérite analogique en basse fréquence, peut être généralisé à haute fréquence. En particulier, le concept de l'efficacité de la transadmittance est introduit pour évaluer la performance du MOSFET dans une gamme de fréquences plus large. La nouvelle FoM permet la prédiction des compromis dans tous les niveaux d'inversion et dans toutes les gammes de fréquences de fonctionnement.

La FoM généralisée ($y_m/I_D$) tracée en fonction de la fréquence normalisée en utilisant le premier pôle de l’effet NQS ($F_{crit}$), ne dépend que de la mobilité et du coefficient d'inversion (IC). Cette propriété intéressante est utilisée pour définir des fréquences critiques NQS basées sur la diminution du gain et le déphasage. La relation de cette fréquence caractéristique avec la fréquence de transition $f_T$ est également donnée.

**Extraction de la mobilité en utilisant l'effet NQS**

De plus, nous avons utilisé une nouvelle approche (l’invariance de la fréquence critique normalisée évaluée à l'aide de l'efficacité de la transadmittance) pour extraire des paramètres essentiels tels que la mobilité, la fréquence critique $f_{NQS}$ et la fréquence de transition $f_T$. Contrairement aux méthodes classiques, la méthode d'extraction de la mobilité proposée permet une extraction précise y compris dans le régime de l’inversion modérée et de la faible inversion. Cette possibilité d’extraire la mobilité est

basée sur le fait que, à haute fréquence, les porteurs de charge "oscillent" dans le canal et seraient moins sujets aux parasites extrinsèques.

**La modélisation DC et basse fréquence quasi-statique**

L'analyse des caractéristiques I-V et C-V mesurées et simulées pour différentes tensions de grille arrière montre que le film de silicium mince est sujet à de multiples phénomènes. En particulier, le canal n'est pas confiné aux interfaces avant et arrière bien que la majorité des modèles compacts adoptent l'approche à double interface. Le phénomène d'inversion volumique s'avère être le plus adapté pour expliquer les observations liées à l'électrostatiques et au transport.

Les caractéristiques DC du transistor MOSFET UTBB FDSOI sont comparées à celles du transistor bulk à une seule grille. Bien que dans un double-grille le contrôle du canal est effectué par les deux grilles et l'effet quantique prend place dans le film mince, les caractéristiques DC sont comparables à celles du bulk à grille unique. De plus, grâce à un meilleur contrôle électrostatique, les caractéristiques DC du canal long sont plus proches de la loi carrée idéale en forte inversion et de la loi exponentielle en faible inversion. Les développements des modèles basés sur la tension de seuil dans le FDSOI UTBB et le bulk ont montré que les modèles de bulk classiques peuvent être utilisés comme des approximations acceptables à condition que la dépendance entre la tension de seuil et la tension sur les deux grilles soit prise en compte dans le MOSFET UTBB FDSOI. Il convient de noter qu'au premier ordre la réduction de la mobilité et la saturation peuvent être prises en compte en utilisant les mêmes méthodes classiques qu'en bulk.

Un circuit équivalent petit signal à faible fréquence est proposé et graduellement amélioré pour un fonctionnement à plus haute fréquence. La simulation du circuit équivalent proposé est comparée au modèle UTSOI2 et montre que le modèle proposé est suffisamment précis pour être utilisé dans les premières investigations des circuits analogiques. Deux approches de modélisation sont donc étudiées: le circuit équivalent simple et le modèle compact quasi-statique industriel récemment proposé, à savoir le modèle Leti-UTSOI2. Les figures de mérite importantes à basse fréquence sont évaluées en utilisant les deux modèles et montrent une reproduction précise des données mesurées.

**Amélioration de la fonction des simulateurs SPICE: DC OP Info**

Une amélioration de la fonction communément utilisée dans les simulateurs SPICE et appelée DC OP Info est proposée. Cette fonction classique est intensivement utilisée dans la conception assistée des circuits analogiques RF malgré des limitations sévères. L'amélioration proposée fournit des informations précises pour les modèles basés sur des sous-circuits RF complexes malgré les multiples éléments extrinsèques impliqués et les modèles NQS haute fréquence. La proposition est adoptée par les principaux fournisseurs CAD.

**Modèle NQS haute fréquence**

Les techniques de caractérisation haute fréquence utilisées ont permis d'obtenir des mesures propres jusqu'à 110 GHz. Les caractéristiques à haute fréquence sont utilisées pour valider le modèle proposé, en notant que la caractérisation proposée est basée sur des mesures de fréquences plus basses. Deux effets principaux limitent la performance du MOSFET à haute fréquence: (1) les éléments extrinsèque dépendant du layout, et (2) les effets distribués latéraux (liés au canal) et longitudinaux (liés aux grilles).

Les éléments extrinsèques sont modélisés en utilisant d'une part les résistances série source et drain et, d'autre part deux réseaux pour représenter les deux grilles. Le réseau représentant la grille avant tient compte des résistances et des capacités distribuées, en particulier de trois résistances série et de deux capacités latérales principales. La grille avant est donc responsable de l'effet distribué, en particulier pour les MOSFET de grande taille. Cet effet distribué est en concurrence avec l'effet NQS du canal et est modélisé en partie en utilisant une technique de compensation pôle-zéro.

L'effet non-quasi-statique est modélisé en utilisant une segmentation du canal et un MOSFET coquille supplémentaire afin de prendre en compte le chevauchement et une partie de la capacité latérale extrinsèque. L’effet du DIBL est modélisé en utilisant des sources extrinsèques de tension dépendantes en tension sur les grilles avant et arrière afin d'émuler le décalage de la tension de seuil.

Le modèle proposé prédit avec précision les paramètres Y et les FoM à haute fréquence sur de larges gammes de fréquences allant de 100 MHz à 110 GHz. L'excellente précision des simulations sur une large bande de fréquence par rapport aux mesures prouve que la topologie de notre modèle est correcte et complète.

### Dimensionnement analogique RF et millimétrique

Ayant déjà préparé des abaques basse et haute fréquence et développé des modèles précis à haute fréquence, une méthodologie de dimensionnement de circuit est proposée et discutée pour illustrer les avantages de l'opération en inversion modérée. Les méthodes de dimensionnement classiques ainsi que leur impact néfaste sur le dimensionnement des circuits sont discutés.

Les caractéristiques du transistor UTBB FDSOI sont utilisées pour un dimensionnement efficace d'un simple circuit LNA à 35 GHz. L'objectif est de fournir un exemple d'application où l'exploitation de la région de l'inversion modérée est bénéfique tant que les performances haute fréquence et la consommation d'énergie sont toutes mises en avant. L'abaque représentant l'efficacité de la transconductance en fonction du coefficient d'inversion (IC) est utilisé pour déterminer la largeur du MOSFET tandis que les courbes représentant la fréquence de transition ($f_T$) en fonction d'IC sont utilisées pour la sélection de la longueur. La méthode de conception, utilisant une longueur non minimum et un régime d'inversion modérée, offre un compromis intéressant entre le gain, la consommation d'énergie et la performance sachant que la largeur du MOSFET est gardée raisonnablement grande et les effets canaux courts atténués. Un œil est également gardé sur les limitations des dispositifs passifs dès le début du flot de dimensionnement.

## Perspectives

### Validation grand signal

Bien que les modèles petits signaux soient souvent suffisants pour la conception des circuits linéaires, la conception des circuits non linéaires tels que les amplificateurs de puissance et les oscillateurs nécessite une prédiction précise des caractéristiques non linéaires des transistors MOSFET dans une large gamme de conditions de polarisation. Le circuit équivalent développé dans cette thèse est un modèle petit signal et ne peut être utilisé qu'avec des circuits linéaires. Cependant, le modèle UTSOI2 augmenté, également proposé dans cette thèse pour la simulation de circuits industriels, est conceptuellement un modèle grand signal à condition de supposer que la performance grand signal du circuit est principalement gouvernée par

ses non linéarités DC. L'approche basée sur un modèle compact augmenté prédit avec précision la distorsion harmonique bien qu'une hypothèse quasi-statique soit considérée dans [45]. Cette approche de modèle compact étendu peut également être utilisée dans le cas du MOSFET UTBB FDSOI pour la simulation grand signal. Par conséquent, afin de valider cette approche, la caractérisation de la non-linéarité à des fréquences millimétriques doit être effectuée en utilisant par exemple des mesures de charge-traction dans les fréquences millimétriques ou une analyse de spectre de puissance.

**Model de bruit haute fréquence**

Un modèle de bruit haute fréquence précis est une nécessité pour la conception d'un circuit comme le LNA. Cependant, le bruit est généralement caractérisé dans une gamme de fréquences où le comportement du transistor vérifie l'hypothèse quasi-statique. Par conséquent, les données de mesure du bruit ne sont souvent pas reproduites avec des modèles inadéquats à haute fréquence. De plus, les effets de bruit de différentes origines ont rendu difficile le développement d'un modèle précis par les scientifiques. En particulier, des modèles empiriques sont utilisés pour la modélisation du bruit haute fréquence en raison de l'ambiguïté liée à la cause réelle du bruit excessif dans les dispositifs à canaux courts. Les paramètres de bruit 2-ports, traditionnellement requis pour la conception RF comme une meilleure alternative aux modèles inexacts, doivent être étendus au spectre millimétrique et des techniques d'épluchage adaptées doivent être proposées.

**Variabilité**

En raison des petites dimensions dans les technologies avancées telles que UTBB FDSOI, la gestion de la variabilité est devenue l'un des défis les plus importants. La variabilité électrique provoquée par la variation du processus de fabrication à l'échelle nanométrique impacte fortement le rendement et donc le coût des circuits intégrés.

Pour la conception des circuits analogiques et RF / millimétriques, un modèle de variabilité doit être suffisamment précis pour prédire l'impact des variations du processus de fabrication (variations locales et globales) sur les simulations électriques. Bien que des modèles empiriques existent pour répondre aux exigences de rendement

élevé, une analyse rigoureuse et complète de la variabilité et de ses origines ainsi que des modèles robustes sont aujourd'hui une nécessité.

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# ETUDE ET MODELISATION DU COMPORTEMENT DYNAMIQUE DU TRANSISTOR MOS DU TYPE UTBB FDSOI POUR LA CONCEPTION DE CIRCUITS INTEGRES ANALOGIQUES A HAUTES FREQUENCES ET BASSE CONSOMMATION


## Résumé

Ce travail de recherche a été principalement motivé par les avantages importants apportés par la technologie UTBB FDSOI aux applications analogiques et RF de faible puissance. L'objectif principal est d'étudier le comportement dynamique du transistor MOSFET du type UTBB FDSOI et de proposer des modèles prédictifs et des recommandations pour la conception de circuits intégrés RF, en mettant un accent particulier sur le régime d'inversion modérée. Après une brève analyse des progrès réalisés au niveau des architectures du transistor MOSFET, un état de l'art de la modélisation du transistor MOSFET UTBB FDSOI est établi. Les principaux effets physiques impliqués dans le transistor à double grille avec une épaisseur du film de 7 nm sont passés en revue, en particulier l'impact de la grille arrière, à l'aide de mesures et de simulations TCAD. La caractéristique $g_m/I_D$ en basse fréquence et la caractéristique $y_m/I_D$ proposée pour la haute fréquence sont étudiées et utilisées dans une conception analogique efficace. Enfin, le modèle NQS haute fréquence proposé reproduit les mesures dans toutes les conditions de polarisation y compris l'inversion modérée jusqu'à 110 GHz.


Mots-clés : Analogique et RF, Double Grille, FDSOI, UTBB, Coefficient d'inversion, Efficacité de la transconductance, $g_m$ sur $I_D$, Efficacité de la transadmittance, faible puissance, faible tension, HF, spectre millimétrique, NQS, LNA, LNA-MIXER.


## Résumé en anglais

This research work has been motivated primarily by the significant advantages brought about by the UTBB FDSOI technology to the Low power Analog and RF applications. The main goal is to study the dynamic behavior of the UTBB FDSOI MOSFET in light of the recent technology advances and to propose predictive models and useful recommendations for RF IC design with particular emphasis on Moderate Inversion regime. After a brief review of progress in MOSFET architectures introduced in the semiconductor industry, a state-of-the-art UTBB FDSOI MOSFET modeling status is compiled. The main physical effects involved in the double gate transistor with a 7 nm thick film are reviewed, particularly the back gate impact, using measurements and TCAD. For better insight into the Weak Inversion and Moderate Inversion operations, both the low frequency $g_m/I_D$ FoM and the proposed high frequency $y_m/I_D$ FoM are studied and also used in an efficient first-cut analog design. Finally, a high frequency NQS model is developed and compared to DC and S-parameters measurements. The results show excellent agreement across all modes of operation including very low bias conditions and up to 110 GHz.


Key words: Analog and RF, Double-gate FETs, Fully Depleted Silicon-on-Insulator (FDSOI), UTBB, Inversion Coefficient, Transconductance efficiency, $g_m$ over $I_D$, Transadmittance efficiency, Low-Power, Low-Voltage, HF, mm-Wave, NQS, LNA, LNA-MIXER.