UNIVERSITÉ DE STRASBOURG

ÉCOLE DOCTORALE MSII (ED n°269)

LABORATOIRE ICUBE (UMR 7357)

THÈSE

présentée par :

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soutenue le : **14 décembre 2022**

pour obtenir le grade de : **Docteur de l'université de Strasbourg**

Discipline/ Spécialité : Micro et Nanoélectronique

Circuits intégrés pour la récupération d'énergie à partir de transducteurs piézoélectriques

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To my familly, Bassem, Hadi and Zeina.

To my mother Mariana, and father Mahmoud in his peaceful place.

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Au cours de la dernière décennie, les progrès significatifs de la microélectronique ont mené au développement de capteurs sans fil à très faible consommation qui sont largement utilisés dans une variété d'applications telles que l'automatisation industrielle, les transports et les systèmes de surveillance de la santé. La plupart du temps, ces capteurs sont alimentés par des piles. Cependant, dans certains contextes de détection, comme dans les HUMS (Health and Usage Monitoring Systems) de l'aéronautique et du transport ferroviaires, ils peuvent être déployés à grande échelle et/ou dans des endroits difficilement accessibles, ce qui rend le remplacement et/ou la recharge des batteries extrêmement difficile et coûteux [11]. Pour résoudre ce problème, de nouveaux travaux de recherche ont été menés afin de prolonger la durée de vie de la batterie et donc des capteurs sans fil. En convertissant l'énergie ambiante en énergie électrique, la récupération d'énergie à partir de sources environnementales est l'une des solutions possibles pour charger les batteries ou alimenter les capteurs sans fil [12, 13]. La source d'énergie peut être un rayonnement solaire [14, 15], un gradient thermique [16, 17], un rayonnement de radiofréquence (RF) [18, 19], ou un mouvement mécanique [20, 21]. Ces derniers en particulier se trouvent sous diverses formes, tels que les mouvements humains, les vibrations des véhicules et des machines, et constituent donc autant de sources d'énergie intéressantes pour alimenter les capteurs sans fil en raison de leur abondance dans l'environnement. Les propriétés de ces sources dépendent de la nature des vibrations cinétiques, elles mêmes fortement liées à l'application, comme un HUMS par exemple [22,23]. En l'occurrence, les vibrations peuvent être permanentes ou intermittentes. Dans tous les cas, les sources nécessitent d'être adaptées à l'application au moyen d'un circuit de conditionnement dédié.

Le travail de cette thèse s'inscrit dans le cadre du projet international de recherche collaborative HARVESTORE, financé par l'ANR. Ce projet vise à développer une nouvelle génération de capteurs sans fil alimentés par l'énergie récupérée des vibrations ambiantes afin de les utiliser dans des applications HUMS. Parmi les différents types de récupérateurs d'énergie cinétique, le choix s'est porté sur l'utilisation d'un transducteur piézoélectrique (PT) pour récupérer l'énergie vibratoire et la stocker dans un supercapacité et une batterie. Ce choix se justifie par sa tension de sortie élevée ($1V - 10V$) et sa densité de puissance élevée ($100\mu W/cm^2$), par son évolutivité et par sa compatibilité avec les technologies de circuits intégrés conventionnelles par rapport à d'autres technologies, tels que les récupérateurs électromagnétiques

et électrostatiques [24]. En raison de la nature vibratoire, la sortie du transducteur piézoélectrique est alternative et d'amplitude aléatoire. Par conséquent, un circuit d'interface pour le redressement du signal et le conditionnement de l'énergie est nécessaire. Dans ce contexte, les travaux de recherche ont porté sur l'étude et la conception d'un circuit d'interface compact et efficace pour extraire le maximum d'énergie générée par le transducteur dans des conditions de fonctionnement très diverses, i.e. avec un fort degré d'indépendance par rapport à la fréquence et à l'amplitude des vibrations. En raison du caractère autonome du capteur sans fil développé, une partie de l'énergie récupérée doit servir à auto-alimenter le circuit d'interface. Aussi, la consommation électrique de ce dernier est critique. C'est pourquoi le choix s'est porté sur le développement d'un circuit intégré à application spécifique (ASIC), ce qui permet d'optimiser l'efficacité énergétique et la fiabilité du circuit d'interface.

La Figure 1 montre un système typique de récupération d'énergie piézoélectrique. Celui-ci se compose d'un transducteur piézoélectrique, d'un circuit d'interface, d'éléments de stockage et d'une charge. Lorsque le transducteur vibre à ou près de sa fréquence de résonance, il peut être modélisé comme une source de courant sinusoïdale équivalente I_{peh} en parallèle avec un condensateur parasite C_{peh}.

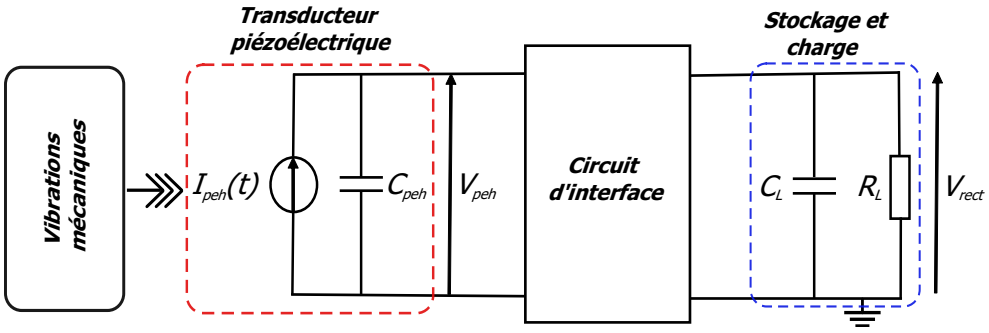


Figure 1.: Système typique pour la récupération d'énergie piézoélectrique.

Dans ce travail, un transducteur avec une valeur de capacité C_{peh} relativement élevée, i.e. $100nF$, et une faible tension de sortie, i.e. $1V$, a été choisi. Ceci permet de couvrir une large gamme de transducteurs et de faire face aux pires conditions de fonctionnement qui pourront être rencontrées dans l'application, i.e. de faibles niveaux de vibrations. Ce transducteur à également été choisi avec une fréquence de résonance de $100Hz$, proche de la fréquence de vibration cible suggérée par le projet.

Lorsque le transducteur est excité, le courant I_{peh} qu'il génère charge et décharge le condensateur C_{peh}, faisant apparaître une tension V_{peh} à ses bornes. Pour redresser cette tension et extraire de l'énergie, l'usage d'un pont de diodes (ou FBR pour Full Bridge Rectifier) est largement répandu en raison de sa simplicité et de sa stabilité. Cependant, son rendement énergétique est relativement faible car il impose un seuil de tension élevé que la tension d'entrée, i.e. V_{peh}, doit franchir avant toute extraction

d'énergie [25–30]. Il n'est en l'occurrence pas adapté au redressement de tensions de faibles amplitudes, i.e. $< 1V$.

Pour répondre à ce problème et améliorer la puissance extraite, de nombreuses approches ont été proposées dans la littérature. Dans l'approche à commutateur unique Swich-Only [25], avec un seul commutateur connecté en parallèle avec le transducteur, le temps nécessaire à la décharge de C_{peh} a été éliminé, ce qui double sa tension de sortie et donc la puissance extraite. Cependant, il y a toujours une perte de charge due à la nécessité de recharger C_{peh}.

Récemment, différentes topologies de circuits d'interface de type SSHI (synchronized switch harvesting on inductor) [8, 25, 31] et SSHC (synchronized switch harvesting on capacitors) [7, 32–34] combinés à un redresseur FBR ont été proposées pour réduire les pertes dues à C_{peh}, et améliorer le rendement énergétique. Cependant, les topologies SSHI requièrent de grandes inductances ($> 10mH$) avec un facteur de qualité élevé pour atteindre une puissance extraite acceptable. Elles ne conviennent donc pas aux applications requérant des systèmes de très faible volume. En ce qui concerne les interfaces SSHC, un grand nombre de de condensateurs commutés est nécessaire pour obtenir une puissance élevée. Cela augmente le volume du système et surtout la complexité de son contrôle.

Trois circuits d'interface principaux ont été conçus pendant la durée de cette thèse afin d'augmenter la puissance extraite du transducteur, lorsque ce dernier fonctionne sous un faible niveau de vibrations. Tout d'abord, un circuit d'interface simple et compact est proposé. Ce circuit nommé FAR est basé sur le un principe appelé Switch-Only [25]. Dans ce circuit aucune bobine ou capacité est ajoutée pour augmenter efficacité énergétique. Le concept est basé sur l'utilisation d'une fraction de la charge stocké dans la capacité de stockage pour recharger le C_{peh} quand le dernière est complètement déchargé. Une étude théorique ainsi que la validation expérimentale ont prouvé que le circuit proposé atteint une efficacité énergétique plus élevée que celle obtenue par le Switch-Only, lorsque la contrainte de la charge augmente.

Pour augmenter encore la quantité d'énergie récupérée par le FAR, un second circuit nommé FAR-FC a été conçu et fabriqué en utilisant la technologie AMS 0.35-µm CMOS. Ce circuit est basé sur le principe SSHC (Synchonized Switch Harvesting on Capacitor). Le concept se base sur l'utilisation d'un ensemble réduit des condensateurs pour décharger et recharger le C_{peh} quand la tension aux bornes atteint sa maximum valeur. Le FAR-FC parvient à extraire 2x fois et 5,64x plus d'énergie que le FAR et le redresseur classique (FBR), respectivement. En plus, ce circuit permet d'extraire l'énergie du transducteur même si les vibrations ambiantes sont faibles, ce qui n'est pas le cas avec les circuits SSHC proposés dans l'état d'art. De plus, le FAR-FC supporte des transducteurs piézoélectriques avec des valeurs de capacité parasite plus élevées par rapport à celles généralement utilisées dans la littérature, ce qui rend le circuit potentiellement adapté à une plus grande variété d'applications.

Finalement, une version améliorée de FAR-FC a été conçue et fabriquée en utilisant la technologie ONSemi 0.18-µm CMOS. Grâce à la mise en œuvre d'une technique de

MPPT (Maximum Power Point Tracking), cette version garantit l'extraction maximale d'énergie quand le récupérateur fonctionne dans des conditions de vibrations environnementales non stables, ce qui n'est pas le cas du FAR-FC. En plus, l'excès de charge résultant du MPPT est réutilisé à la fois comme une source d'alimentation et pour augmenter le temps d'extraction d'énergie. Ceci augmente largement l'efficacité énergétique de cette nouvelle version. Malheureusement, en raison du contexte de pandémie et de pénurie de semi-conducteur, la version améliorée du FAR-FC n'a pas pu être testée dans le cadre de ce travail de thèse, comme cela était initialement prévu.

Publications

1. Conférence publications
    a) [35] : L. Wassouf, E. Jamshidpour, and V. Frick, "A High-Efficiency Full Active Rectifier for Piezo Energy Harvesting," in 2020 IEEE International Conference on Environment and Electrical Engineering and 2020 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe), Madrid, Spain, Jun. 2020, pp. 1–5.
    b) [36] : L. Mamouri, V. Frick, T. Mesbahi, L. Wassouf, and E. Jamshidpour, "Optimised Model for Piezoelectric Energy Harvesting Circuits Design," in 2021 19th IEEE.
2. Journal publications
    a) [37] : V. Frick, L. Wassouf, and E. Jamshidpour, "Voltage Flip Efficiency Enhancement for Piezo Energy Harvesting," Electronics, vol. 10, p. 2400, Oct. 2021.
    b) Article soumis le 27/06/2022, accepté fin septembre 2022 et à paraître : L. Wassouf, E. Jamshidpour, and V. Frick « Optimization of an SSHC-Based Full Active Rectifier for Piezoelectric Energy Harvesting » in AICSP, Springer.

Abstract

In the past decade, there has been significant advances in microelectronics that led to the development of ultra-low power wireless sensors. Such sensors are widely used in a variety of applications such as industrial automation, transportation and health monitoring systems. Most of the time, these sensors are powered by batteries. However, in some contexts such as in HUMS (Health and Usage Monitoring Systems) used in aeronautics and rail transportation, wireless sensors can be deployed on a large scale and/or in locations that are difficult to access, making battery replacement and/or re-charging extremely challenging and expensive. To address this problem, there has been an emerging research work in order to extend the battery, and thus the wireless sensor operational lifetime. One possible solution to charge batteries or power wireless sensors was to convert ambient energy into electrical energy by harvesting energy from environmental sources. The energy source can be solar radiation, thermal gradient, radio frequency (RF) radiation or mechanical motion. In particular, mechanical motion is interesting because of its abundance in the environment in various forms such as human motion, vehicle and machine vibrations. The properties of these sources depend on the nature of the kinetic vibrations which, in turn, vary depending to the application. For example, in the case of HUMS, vibrations can be permanent or intermittent. In such cases, the sources need to be adapted to the application by means of a dedicated conditioning circuit.

The work of this thesis is part of the international collaborative research project HARVESTORE, funded by the ANR. This project aims at developing a new generation of wireless sensors powered by energy harvested from ambient vibrations for HUMS applications. A piezoelectric transducer (PT) will be used to harvest vibration energy and store it in a supercapacitor and a battery. Due to the oscillating nature of vibration, the output of the piezoelectric transducer is alternating and random in amplitude. Therefore, an interface circuit for signal rectification and energy conditioning is required. In this context, the current research work focuses on the study and design of a compact and efficient interface circuit to extract the maximum energy generated by the transducer under diverse operating conditions, i.e. with a high degree of independence from the vibration amplitude. Due to the autonomous nature of the required wireless sensor, part of the extracted energy must be used to self-power the interface circuit, which means that its power consumption should be kept as low as possible. This motivates the choice of application specific integrated circuit (ASIC) for the interface circuit in order to improve its power efficiency and reliability.

Three main interface circuits have been designed during this thesis work in order to increase the power extracted from the transducer when it operates under a low level of vibration. First, a simple and compact interface circuit is proposed. This circuit, named Full-Active Rectifier (FAR), is based on a Switch-Only principle proposed in the literature. In the proposed circuit, no inductors or capacitors are added to increase the power efficiency. The concept of the FAR circuit is based on the use of a fraction of the charge stored in a storage capacitor to recharge a parasitic capacitor of the PT when the latter is completely discharged. A theoretical study as well as an experimental validation will be conducted to prove that the proposed circuit achieves higher energy efficiency than the Switch-Only circuit when the load stress increases.

To further increase the amount of energy harvested by the FAR, a second circuit named FAR-FC has been designed and fabricated using AMS 0.35µm HV CMOS technology. This circuit is based on the SSHC (Synchronized Switch Harvesting on Capacitor) principle proposed in the literature. The concept is based on the use of a reduced set of capacitors to discharge and recharge the parasitic capacitor of the PT when the voltage across it reaches its maximum value. The FAR-FC can extract 2x and 5.64x more energy than the FAR and the conventional rectifier (FBR), respectively. In addition, this circuit is able to extract energy from the transducer even if the ambient vibration is low, which is not the case with the SSHC circuits proposed in the literature. Furthermore, the FAR-FC supports piezoelectric transducers with higher parasitic capacitance values compared to those generally used in the literature, making the circuit potentially suitable for a variety of applications.

Finally, an improved version of FAR-FC has been designed and fabricated using ONSemi 0.18μm CMOS technology. Thanks to the implementation of a MPPT (Maximum Power Point Tracking) technique, this version guarantees the maximum power extraction when the PT is operating under non-stable environmental vibration conditions, which is not the case with FAR-FC. In addition, the excess charge resulting from the MPPT is reused both as a power source and to increase the power extraction time. This significantly increases the power efficiency of this new version.

1. Introduction

1.1. Context and objectives of the thesis

Over the past decades, sensors have become ubiquitous and relevant to almost all aspects of human life through their applications. In healthcare, biosensors play a vital role in diagnosing and monitoring the health of at-risk patients [38,39]. In industry, sensing technologies enable monitoring, control, and automation of the manufacturing process, increasing safety and improving operational efficiency [40, 41]. Recent advancement in technologies have led to the development of smart sensors. These sensors can provide a highly reliable output signal thanks to a dedicated microprocessor, which filters and processes the collected data. In addition, they are compliant with various communication standards such as Wi-Fi, Bluetooth and ZigBee, which allows them to integrate with the IoT (Internet of Things). Smart sensors are employed in a wide range of applications such as smart homes and cities, industrial automation, transportation, health monitoring [42–48]. However, regardless of their technology, sensors and electronics in general need to be powered. Power can be supplied by wires, which is not always possible due to the high cost of installation and maintenance when large number of sensors need to be deployed. In addition, wires add complexity of implementation especially when a retro-fitting the sensors on already existing installations. Also, wires are liable to be damaged and disconnected in heavy-duty and high-traffic environment. This is why wireless sensors and more generally wireless sensors networks (WSN) are the best choice for most applications. Recently, significant advances in microelectronics have led to the development of ultra-low-power wireless sensors. Since most of these sensors must operate autonomously, an energy storage device is needed. Batteries are the most common power solutions for many applications. However, in certain sensing contexts, such as HUMS (Health and Usage Motoring System) applications in aeronautics and rail transport, wireless sensors may be deployed on a large scale or in hardly accessible locations making battery replacement and/or re-charging extremely challenging and expensive [11]. In addition, the large quantity of discharged batteries creates a chemical waste problem. To address this issue, there has been an emerging research work in order to extend the battery, and thus the wireless sensor operational lifetime. Harvesting ambient energy from environmental sources into electrical energy is one possible solution for either charging batteries or powering the wireless sensors [12,13]. The energy source could be solar radiation [14, 15], thermal gradient [16, 17], radio frequency (RF) radiation [18, 19] and mechanical motion [20, 21].

The work of this thesis is part of the international collaborative research project HARVESTORE[1] that gathers four partners: Thalès[2], LIST[3], LPICM[4] and ICube[5]. HARVESTORE aims at developing a new generation of autonomous wireless sensors for HUMS applications.

Figure 1.1 shows a typical block diagram of a wireless sensor node powered by ambient energy harvester. It features two main blocks, the sensing and communication unit (SCU), and the energy-harvesting power source. A standard SCU needs three main components: 1) the sensor itself (e.g. temperature, humidity, pressure...), which produces an electrical signal related to the ambient parameters, 2) a data processing unit (e.g. microcontroller unit (MCU)), 3) a radio frequency (RF) transmitter module to send the processed data to a machine monitor and control unit. The power source provides stable power supply to all parts of the WSN and often consists of a rechargeable battery, or a supercapacitor or a combination of both. To extend the battery lifetime, environmental energy sources can be used for recharging and/or powering these sensors. The energy-harvesting power source is mainly

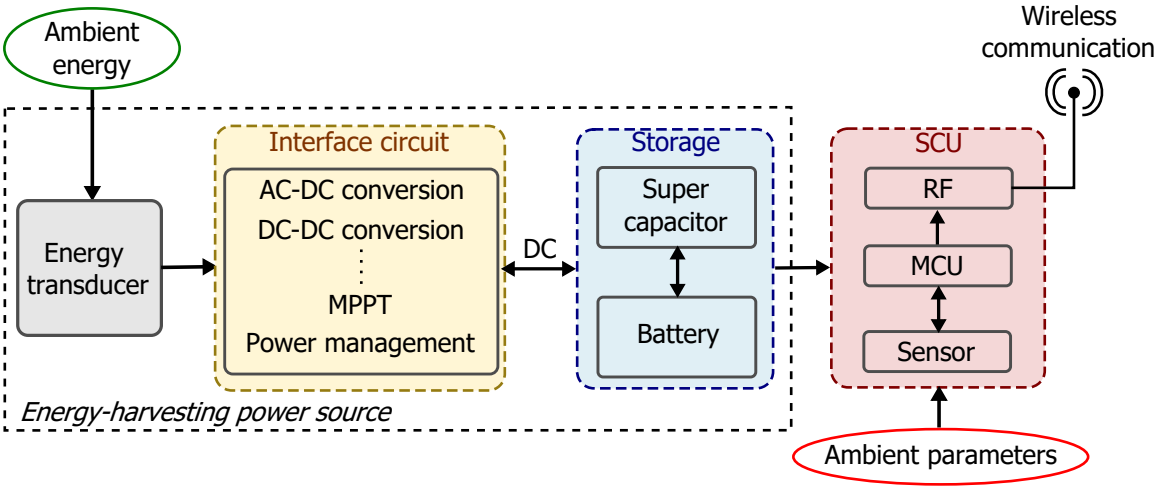


Figure 1.1.: Typical block diagram of a wireless sensor node powered from ambient energy source.

composed of: 1) an energy transducer to convert the ambient energy into electrical energy, 2) an interface circuit used to condition the electrical energy and make it exploitable (i.e. storable and/or usable to directly power the system), 3) one or several energy storage elements, namely a supercapacitor or a battery or both combined.

In general, the wireless sensor operates in a pulsed manner as shown in Figure 1.2. This means that the sensor reads and sends the processed measurements only during

[1]ANR PRCI HARVESTORE (ANR-18-CE09-0033).
[2]Thalès Research Technology.
[3]Luxembourg Institute of Science and Technology.
[4]Laboratoire de Physique des Interfaces et des Couches Minces.
[5]Engineering science, computer science and imaging laboratory.

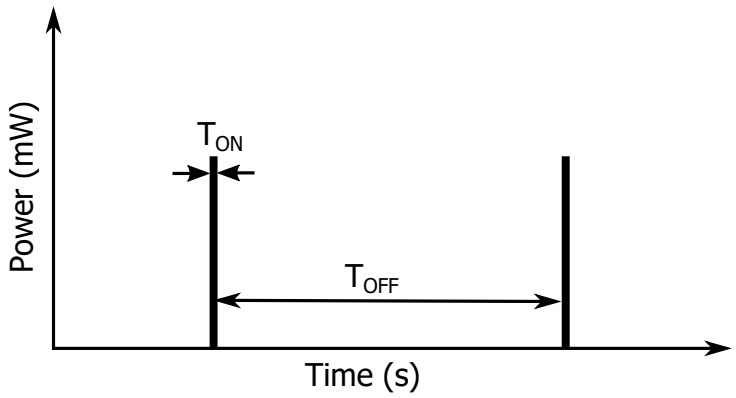


Figure 1.2.: Wireless sensor operation.

a specific time interval (T_{ON}), and stops its activities during the rest of time (T_{OFF}). For a wireless sensor node powered by ambient energy harvester, two points should be taken into account:

1. The stored energy should be sufficient to power the system, i.e. the whole WSN, during the sensor's activity, i.e. T_{ON}. As a realistic example, the humidity and temperature wireless sensor node, TIDA-00484 from Texas Instruments is taken [49]. The power consumption of this node is $P_s = 10mW$, and the duration of its activities $T_{ON} = 30ms$. Hence, the required energy during its active operation mode can be given as:

$$E_s = P_s \times T_{ON} = 10 \times 10^{-3} \times 0.03 = 0.0003J \tag{1.1}$$

   Sensing and communication units (SCU) require specific supply voltage range to ensure nominal operation. For instance, the nominal supply voltage for the taken example can be $3V$ and the minimal voltage is $2.8V$. This implies that the voltage across the storage elements shouldn't drop below $2.8V$ during the active period of the SCU, and the harvester should be able to recharge them to the nominal $3V$ during two active periods (Figure 1.3). As a result, the minimum energy E_{supmin} that must be stored in the storage elements to ensure the SCU nominal operation during T_{ON} can be given by:

$$E_{supmin} = E_{sup} - 0.0003 \tag{1.2}$$

   where E_{sup} is the nominal stored energy in the storage elements. This corresponds to an equivalent minimum storage capacity C_{eq}, which can be calculated as followed:

$$C_{eq} = \frac{2E_{supmin}}{V_{supmin}^2} = \frac{2E_{sup}}{V_{sup}^2} \tag{1.3}$$

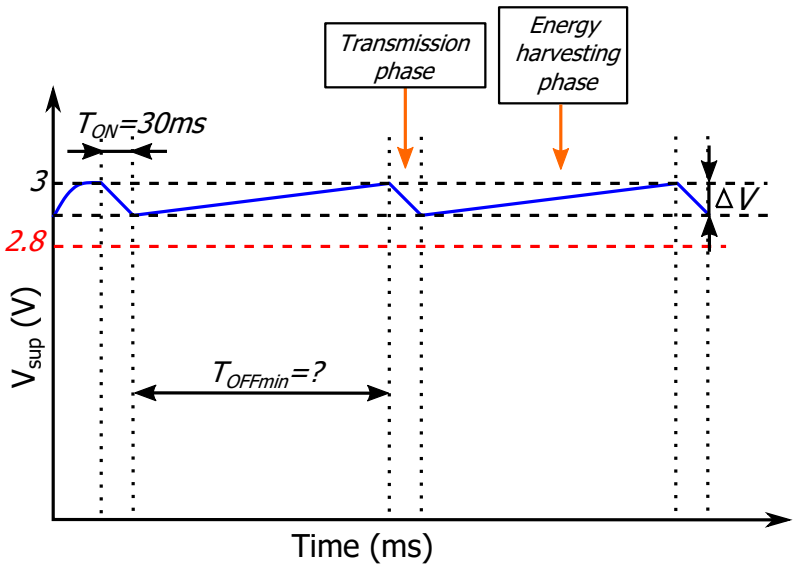


Figure 1.3.: Storage elements voltage evolution during on-state and off-state wireless sensor operation modes.

2. The sensor must not be reactivated until when the storage elements are recharged by the energy harvester to its nominal voltage V_{sup}, i.e. after T_{OFFmin} (Figure 1.3). This time, i.e. T_{OFFmin}, will depend on the amount of ambient energy available between two activations. This makes it difficult to evaluate. However, it can be calculated by estimating the available extracted energy and the equivalent capacity of the storage elements. Let's assume that the harvesting system can extract an amount of power $P = I.V$. When the wireless sensor node is deactivated, the total extracted charges goes to recharge the storage elements. As a result:

$$I = I_{sup} = \frac{dQ}{dt} = C_{eq}\frac{dV}{dt} \tag{1.4}$$

where I_{sup} is the charging current of the storage elements. The last equation can be simplified to:

$$I_{sup} = C_{sup}\frac{\Delta V}{\Delta t} \tag{1.5}$$

Therefore, the time required to recharge the storage elements can be given as:

$$\Delta t = C_{sup}\frac{\Delta V}{I_{sup}} = T_{OFFmin} \tag{1.6}$$

where ΔV is the difference between the nominal voltage V_{sup} and the voltage across the storage elements at the end of T_{ON} (Figure 1.3). From 1.6, it can be concluded that, for a known storage elements, the sensor operation

rate is tightly related to the amount of energy harvested from the surrounding environment. The higher the harvested energy, the higher the sensor operation rate and thus the higher the data transmission rate. However, the amount of harvested energy also significantly depends on the harvester's transduction type and its properties as well as the power efficiency of the associated interface circuit. In the following section, the four main types of energy harvesting transducers with their advantages and drawback are introduced.

1.2. Energy harvesting techniques

With the development of nanomaterials and nanotechnologies, small-scale energy harvesters become of increasing interest for powering WSN and low power electronic devices. Many kinds of energy harvesters have been proposed in the last decade [5, 13, 14, 17, 50–52]. Among them, solar, heat, RF and kinetic energy harvesters are the main four techniques.

1. *Solar/Light energy harvester:* light and particularly solar radiation is the most abundant source of energy in nature. Light can be converted into electricity thanks to the photovoltaic (PV) effect in solar cells. The latter are made from a semiconductor materials with a P-N junction as show in Figure 1.4. When

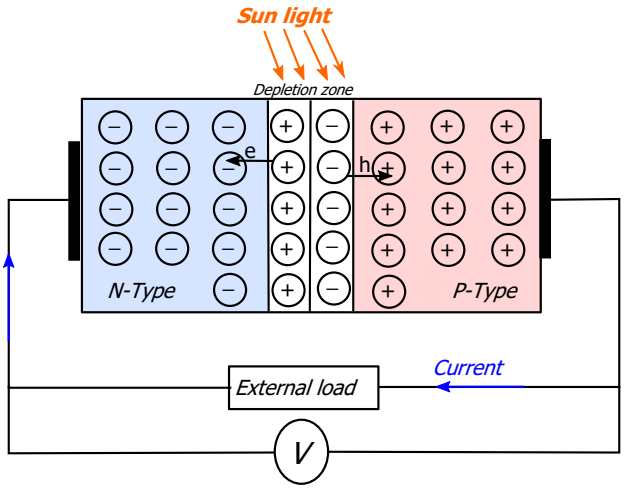


Figure 1.4.: Principle operation of a PV cell.

a PV cell is exposed to light, the photons excite the outermost electrons of the semiconductor atoms. If the absorbed photons have energy greater than the bandgap energy of the semiconductor material, the excited electrons can move towards the N-side of the junction leaving holes in the other side. When an electrical circuit is connected between the junction terminals, the voltage difference drives the free electrons from the N-side to the P-side of the junction leading to form an electric current. Multiple PV cells are electrically connected

to create a PV module. Then, the PV modules are interconnected in an array to produce the desired peak DC voltage and current. The most popular three types PV cell technologies in the market are mono-crystalline silicon, poly-crystalline silicon, and thin film [53] (Figure 1.5). Although the relatively

Figure 1.5.: The main types of the PV cell [1].

low power efficiency of the PV cells (<50%) [54], the PV panel can provide an outstanding power density around $150mW/cm^2$ in full sunlight [55]. However, this power density drastically decreases when the sun goes down or at indoor conditions, which is the main disadvantage of this king of energy harvesting.

2. *Thermoelectric energy harvester:* heat flow between two points at two different temperatures can be converted into electricity thanks to the seebeck effect in a thermoelectric generator (TEG). The basic building block of a TEG is a thermocouple which typically made of one n-doped semiconductor and one p-doped semiconductor. The semiconductors are thermally connected in parallel

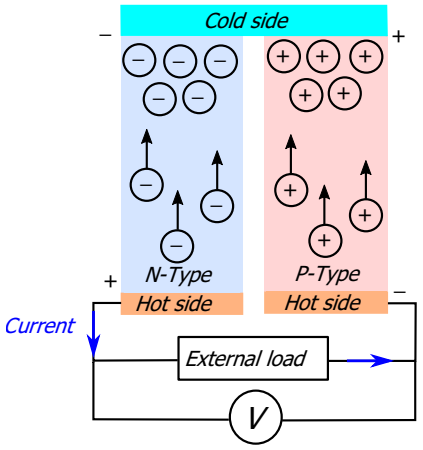


Figure 1.6.: The seebeck effect of a thermocouple.

and electrically connected in series by a metal strip as shown in Figure 1.6. As the hot side of the metal has a higher energy and a higher concentration of charge carriers, the charge carriers, i.e. electrons and holes, move from the hot side to the cold side creating a voltage potential V. The desired electrical voltage and current can be created by connecting many n-doped and p-doped

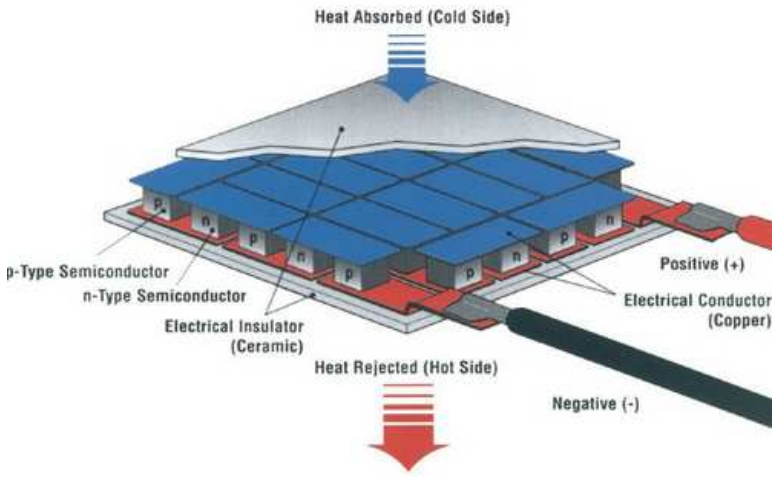


Figure 1.7.: Thermoelectric generator structure [2].

semiconductors pairs either in series or in parallel as shown in Figure 1.7. The main advantage of TEG is that it can be designed to be very compact. This makes it suitable for small medical and portable applications in addition to wireless sensor networks. However, maintaining the temperature gradient which can't exceed $10°C$ on such small scale systems is always difficult and yields a relatively low thermoelectric efficiency between 5% and 10% [19, 56]. In general, the power produced by micro thermoelectric devices is low, in the microwatt to milliwatt range [55].

3. *Radio frequency (RF) energy harvester:* RF energy harvesting consists in converting the electromagnetic waves captured by a receiving antenna into usable DC electrical power by means of a power conversion circuit [56, 57]. Although the relatively low RF power density ($0.2nW/cm^2$ to $1\mu W/cm^2$) compared to other ambient energy sources such as solar ($10mW/cm^2$) [58,59], its abundance in the space and its availability under all conditions (indoor and outdoor) makes it a reliable and permanent energy source. The RF wireless energy can be collected from a variety of sources such as satellite stations, cell phone towers and wireless internet. The power harvested from an RF source by an RF energy harvester is dependent on the signal frequency, the conversion efficiency of the power conversion circuit and the RF power level of the source (transmitting antenna), which significantly decreases with distance [57, 60]. Depending on this distance, the RF sources can be categorized into near-field and far-field sources [60]. In the near-field application, the RF energy harvester can reach a power conversion efficiency higher than 80%. These harvesters are usually used to charge devices over short distances. Conversely, due to the low input power of RF energy harvester in the case of far-field RF sources, it is limited to the ultra low-power applications such as wireless communications [55, 57]. Besides progressive achievements in recent years to increase the usable power level, there are still challenges that should be overcome such as minimizing the

transmission loss, reducing the system dimensions and the design of antennas that operate with multiple frequencies.

4. *Kinetic energy harvester:* mechanical motion such as human motions, vehicle and machinery vibrations..., is an attractive energy source due to its abundance in the environment. Kinetic harvesters are suitable for applications where mechanical vibration permanently or frequently occurs like HUMS applications [22, 23]. Using an electromechanical transducer, vibrational energy can be converted into electrical energy. The energy transduction can be carried out by three main techniques: electrostatic, electromagnetic and piezoelectric.

   a) *Electrostatic harvester:* this harvester has a capacitive structure consisting of two plates separated by air or any dielectric material. The conversion principle is based on a capacitance variation induced by the relative movement between the capacitor plates charged with different potentials. The capacitance variation then generates electrical charges, i.e. electrical current (Figure 1.8) [24, 61]. To perform this conversion a

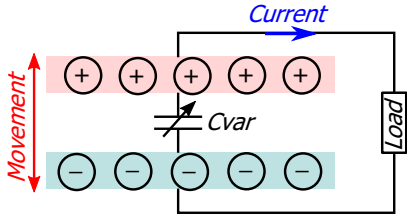


Figure 1.8.: Electrostatic energy conversion principle.

voltage source is required in order to charge the capacitor plates. Based on the voltage sources, this harvester can be categorized into two types: 1) electret-free harvester, where the voltage source is an external power supply as shown in Figure 1.9 (left), 2) electret-based harvesters, where the capacitor plates is charged using electret materials as depicted in Figure 1.9 (right). In the first type, power can be generated in two ways:

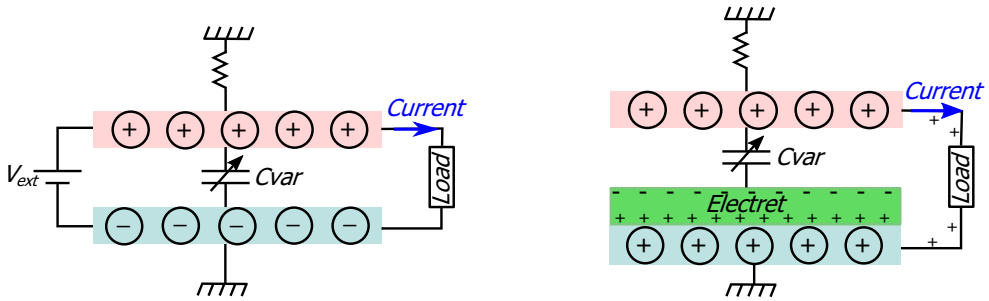


Figure 1.9.: Electrostatic harvester types: electret-free (left) and electret-based (right).

a charge-constrained energy conversion cycle, and a voltage-constrained

energy conversion cycle [50]. In the charge-constrained conversion, the charge is kept constant while the voltage varies with the capacitance variation. In the voltage-contained conversion, the voltage is kept constant while the charge varies with the capacitance variation. The main drawback of the electret-free harvester is the need for an external power supply. This issue is addressed in the second type, i.e. electret-based harvesters, by adding electret layers on one (or two) capacitor plates. Electret is dielectric material with a quasi-permanent electrical charges, i.e. dipole polarization [62]. The performance of electret-based harvesters significantly depends on the surface charge densities. The dielectric material can be either silicon-based such as Si3N4 and SiO2, or ploymer-based such as Teflon and PVDF [24]. However, usually the polymer-based electrets can get higher surface charge densities than silicon-based electrets. This makes it more attractive for elecetret-based harvesters.

b) *Electromagnetic harvester:* in this harvester the relative motion induced by vibrations between a coil and a magnet creates a variation in the magnetic field, which in turn induces a current according to Faraday's law of induction [3, 4, 51, 63]. The electromagnetic harvesters are designed at macro and micro scale, as a system of springs, magnets and coils, where the magnet and the coil can move relative to each other as shown in Figure 1.10. Although the macro-scale harvesters are bulky, it can produce high

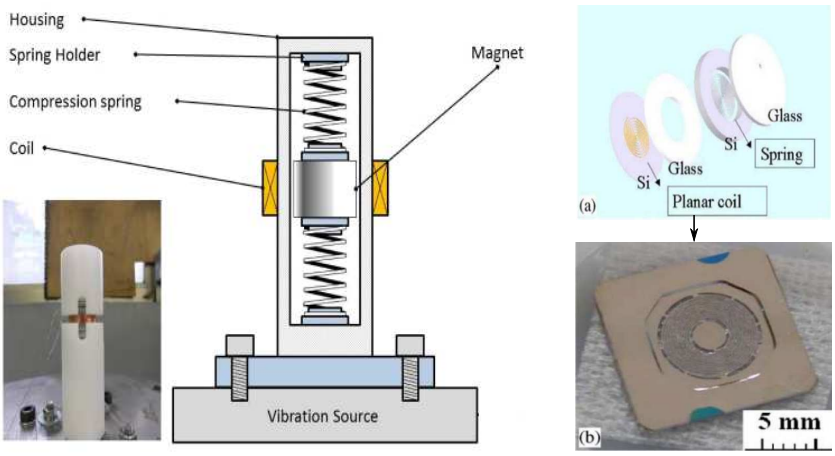


Figure 1.10.: Electromagnetic harvesters: macro harvester (left) [3], and micro harvester with planner coil (right) [4].

output power, which makes them suitable for high power applications [24]. In micro-scale harvesters, low cost planar coils are used to minimize the system volume. However, this limits the achievable number of turns and thus yields low output power. Therefore, they are used for low power applications such as wireless sensors and MEMS [4, 24].

c) *Piezoelectric harvester:* thanks to the piezoelectric effect of certain ma-

terials, which have non-centrosymetric crystal structures, the mechanical energy can be converted into electrical energy (Direct piezoelectric effect) and vise versa (Inverse piezoelectric effect) [5,64,65]. In a noncentrosymmetric crystal such as quartz crystal ($SiO2$), the atoms arrangement is not symmetrical [66] as shown in Figure 1.11. However, a positive charge in one location cancels out a negative charge in the vicinity which makes the crystal electrically neutral. Applying a mechanical stress causes to shift Si atoms to be closer in the top, and O atoms to be closer in the bottom as shown in Figure 1.11. As a result, the average charge becomes positive at the top of the crystal and negative at the bottom. This creates a potential difference and thus an electrical field across the crystal. In the inverse piezoelectric effect, applying a potential difference across the crystal causes the charges change its position due to electrostatic attraction or repulsion created by either like or opposite charges (Figure 1.11). Piezoelectric materials can be classified into naturally occurring and engi-

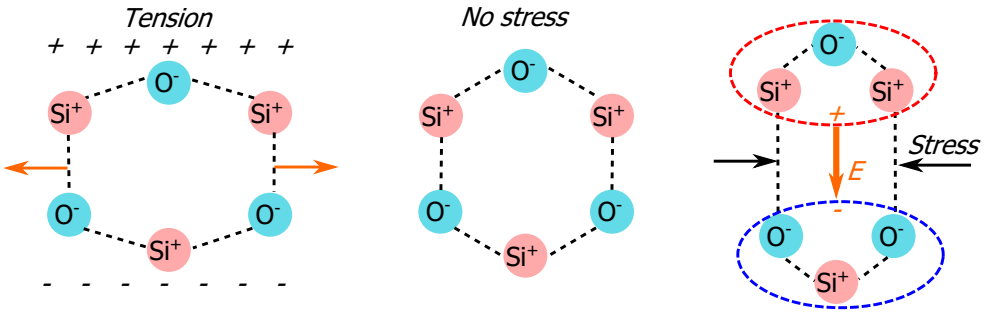


Figure 1.11.: Piezoelectric effect in quartz crystal.

neered materials. The most common, and the first piezoelectric material used in electronic devices is the quartz crystal. Other naturally occurring piezoelectric materials include cane sugar, topaz, tourmaline and Rochelle salt [5,52]. Engineered materials, i.e. synthetic materials are developed to rival the performance of quartz. These materials are generally categorized into ferroelectric ceramics or polymers (lead zirconate titanate (PZT), polyvinylidene fluoride ($PVDF$)), and non-ferroelectric crystalline materials (zinc oxide (ZnO), aluminum nitride (AlN)) [56,64]. Among the engineered piezoelectric materials PZTs and MFCs are the most widely used for energy harvesting due to their relatively high piezoelectric effect and their mature manufacturing process [24]. After producing piezoelectric materials, they are subjected to the poling process in order to their piezoelectric sensitivity [52]. The direct piezoelectric effect is used for energy harvesting applications while the inverse effect is used for actuators applications [5]. Besides that the piezoelectric harvester doesn't need to an external power source, it has many underlying advantages, which are high output voltage ($1V - 10V$), high power density ($100\mu W/cm^2$), good scalability, simple structure, ease of application and compatibility with

conventional integrated circuit technologies compared to other harvesters, i.e. electromagnetic and electrostatic harvesters. Despite all of these advantages, piezoelectric harvester also has a few disadvantages, which are the need to the rectification circuit in addition to the degradation of the piezoelectric effect induced by the long-term stressing operations.

Energy harvester	**Power density**	**Advantages**	**Disadvantages**
Light/Solar [55, 58]	Outdoors: $150mW/cm^2$ Indoors: $150\mu W/cm^2$	- High power density. - No need to rectification circuit.	- Highly dependent on surrounding light conditions.
Thermoelectric [19, 56]	$10\mu W/cm^2$ to $300mW/cm^2$	- Harvester can be designed to be very compact. - No need to rectification circuit.	- Low power conversion efficiency for temperatures under 10C°.
Radio frequency [58, 59]	$0.2nW/cm^2$ to $1\mu W/cm^2$	- No need to rectification circuit. - availability under all conditions (indoor and outdoor).	- Power density is significantly dependent on the signal frequency and the distance of the transmitting antenna.
Electrostatic [56, 67]	$3.8\mu W/cm^2$	- Simple integration. - No need to rectification circuit.	- The need to a polarization source or electrets.
Electromagnetic [3, 4, 51, 63, 67]	$4.0\mu W/cm^2$	- High output current. - Robust. - No need to external power supply.	- Bulky. - Rectification circuit is required. - Compatibility problem. - Low output voltage and low power efficiency.
Piezoelectric [5, 64, 65]	$10\mu W/cm^2$ to $100\mu W/cm^2$	- No need to external power supply. - High output voltage and high power density. - Ease of use and scalabe.	- Rectification circuit is required. - Piezoelectric effect degradation.

Table 1.1.: Comparison between main energy harvesters.

Table 1.1 summarizes the different harvesting techniques, their typical amounts of energy in addition to their advantages and disadvantages. As mentioned before, this project targets the HUMS wireless sensors. Helicopter safety and train management are the two intended applications. For the helicopter safety, the developed

wireless sensor will be used for live-monitoring of the structural health of a helicopter's critical part with data transmission to a flight management system. The monitored data (vibration, temperature, oil pressure...) will then be used in a preventive maintenance process to detect failures in advance increasing safety and finally saving lives. In the case of the train and more particularly freight train, when a loss of carriage happens, no speed, no brake pressure drop can be observed and train integrity becomes a real challenge. Therefore, for the integrity of the train, placing wireless sensor in each carriage would ensure the monitoring of the carriage state and avoid the installation of the dedicated connection between all carriages in addition to ease the retrofitting of the old installations. In both cases, i.e. helicopter and train, energy harvesting from ambient vibrations is the most convenient for providing the adequate energy required to power the wireless sensors due to its abundance in the mentioned environments. The need for an external voltage supply or electrets in the electrostatic harvester makes it unsuitable for such applications. Among the other kinds of kinetic energy harvesters, piezoelectric transducer (PT) is chosen. This is due to its high output voltage ($1V - 10V$) and high power density ($100\mu W/cm^2$), scalability and compatibility with conventional integrated circuit technologies compared to the electromagnetic harvester.

1.3. Motivation

After choosing the piezoelectric transducer (PT) as a vibration energy harvester, the HARVESTORE project focuses on three axes in order to provide the wireless sensor with an efficient power supply. These axes are: 1) the optimization of the materials and structure of the PT to increase its power conversion efficiency and thus the harvested power. In this context, a customized PT will be developed by the project partner LIST. 2) the design of an efficient interface circuit, which is the objective of this thesis and is carried out at ICube, in order to increase the extracted power from the PT. 3) the design of a flexible and a high power density storage elements comprising both supercapacitor and battery in order to extend the operational life of the wireless sensor. This part of the project will be developed by Thalès and LPICM project partners. Achieving the two first axes significantly increases the extracted power and thus the data transmission rate. This in turn improves the reliability of the HUMS wireless sensor and thus the operational safety of the monitored machine. However, even with a high PT power conversion efficiency, the power delivered to the wireless sensor highly depends on the power efficiency of the associated interface circuit. In this context, the work of this thesis aims at designing a compact and efficient interface circuit that can extract the maximum of energy harvested by the PT. Since a portion of the overall harvested energy will be used to power the interface circuit, its consumption is quite critical. Therefore, the thesis work also aims at designing ultra-low power module architectures. This can be achieved by means of an application-specific integrated circuit (ASIC) implementation. To design the

ASIC module, standard HV CMOS technology is used, which allows high-volume production at low cost. The specifications of the interface circuit are based on the predictive characteristics of the customized PT of LIST. However, for experiments, a commercial PT with characteristics close to those of the LIST PT is used. This PT has a relatively high parasitic capacitor, i.e. $100nF$, and a low output voltage, i.e. $1V$ to cover a wide range of PT transducers and to deal with the worst-case operating conditions, i.e. under low vibration levels. Also, the PT has a resonant frequency of $130Hz$, close to the target vibration frequency suggested by the applications related to this project.

1.4. Thesis outlines and organization

This thesis focuses on improving both the power efficiency of the piezoelectric energy harvesting interface circuits and the ability of extracting power from the low environmental vibrations. This manuscript is thus organized as follows: the second chapter provides a detailed background on the piezoelectric interface circuits proposed in the state-of-the-art with their power performance and limitations. In order to minimize the volume of the harvesting system and increase power extraction time, two simple novel typologies are proposed in the third chapter. The first system is fully integrated and the second system employs only one external capacitor. To further improve the extracted output power of the previous circuits, an enhanced SSHC interface circuit is proposed in the fourth chapter. The proposed circuit reaches better power efficiency when the piezoelectric transducer is operating under low mechanical excitation, i.e. when the output voltage of the piezoelectric transducer is $1V$, while this value is usually greater than $2V$ in most of state-of-the-art SSHC circuits. It also supports piezoelectric transducers with higher inherent capacitance values compared to those usually reported in literature, which makes the circuit potentially suitable for a larger variety of applications. A second version of the enhanced SSHC interface circuit is presented in the fifth chapter. In this version, more efficient power extraction can be achieved thanks to the implementation of a maximum power point tracking (MPPT) process and the recycling of its associated excess charge. Finally, the contributions of this thesis work in addition to the discussion of the open problems and future work are provided in the last chapter.

2. Piezoelectric Energy Harvesting Interface Circuit

2.1. Introduction

Over the last decade, vibration-based energy harvesters became of increasing interest in applications where kinetic vibration permanently or frequently occurs [50, 51, 63, 68]. By transforming the kinetic vibration into electrical energy, this type of ambient energy harvesters can offer the sufficient energy required to power small electronic devices such as wireless sensors [22, 23, 69, 70]. Among the different techniques of vibration energy harvesting, piezoelectric energy harvesting (PEH) is widely employed due to its high power density, ease of application and compatibility with conventional integrated circuit technologies compared to other mechanisms, such as electromagnetic and electrostatic harvesters [24]. In this technique, when a vibration input is applied, the kinetic energy produces a strain on the piezoelectric material. This in turn generates an electrical field due to the piezoelectric direct effect.

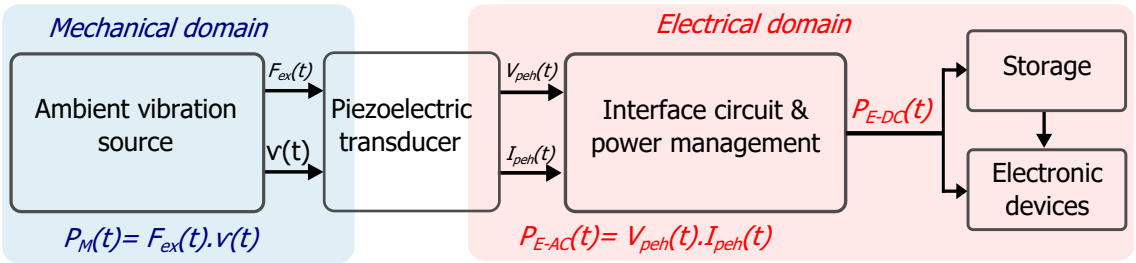


Figure 2.1.: Piezoelectric harvesting system (PHS).

Figure 2.1 shows a typical piezoelectric harvesting system. It can be subdivided into mechanical and electrical domains. In the mechanical domain, the external mechanical strength $F_{ex}(t)$ of a vibrating object with certain velocity $\nu(t)$ induces mechanical energy $P_M(t)$. Maximum $P_M(t)$ can be achieved if the resonant frequency of the piezoelectric transducer (PT) is equal to the vibration frequency. In the electrical domain, both the voltage across the PT and the flowing current through it result in an electrical energy $P_{E-AC}(t)$. Since the output voltage across the PT has an alternative nature, it can not be directly used to power an electronic device. In order to make use of the AC electrical power generated by the PT, an

interface circuit is necessary to rectify the AC voltage and provide a stable DC power supply. However, the power efficiency of the piezoelectric harvester depends on both the piezoelectric transducer properties and the interface circuit efficiency. In this chapter, the equivalent model of the piezoelectric transducer in addition to the common interface circuits are presented. Other interface circuits proposed in the literature aiming at improving the power efficiency are also studied in order to identify and summarize their limitations.

2.2. Equivalent model of a piezoelectric transducer

Due to the direct effect of the piezoelectric material, the piezoelectric harvester converts the environmental vibrations into usable electrical charges. The use of a cantilevered piezoelectric transducer (PT) structure allows a simple energy harvesting. This structure is the most commonly used type for piezoelectric harvesting due to its simplicity, low cost and high mechanical quality factor. Figure 2.2 shows the cantilevered piezoelectric transducer (PT) structure. It generally consists of:

1. A substrate layer fixed at one end to amplify the displacement of an added mass compared to the vibration displacement amplitude. The substrate material is generally chosen in such a way that maximizes its mechanical quality factor.
2. A thin film of piezoelectric material that represents the active part of the piezoelectric harvester structure. This part should be placed as close as possible to the clamped side of the harvester to receive the maximum of mechanical stress and thus convert the maximum of mechanical energy.
3. Two electrodes attached to the both sides of piezoelectric film.
4. A seismic mass added to the free end of the substrate layer to increase the mechanical stress. The greater the mass, the greater the mechanical stress applied on the piezoelectric material and the higher output energy. The added mass can also be used to adjust the excitation frequency.

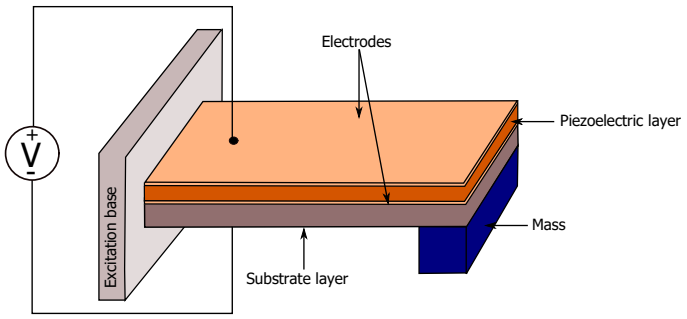


Figure 2.2.: A cantilevered piezoelectric transducer structure.

Another piezoelectric transducer structure is the cymbal structure (Figure 2.3 (a)) which is able to withstand a higher impact force than the cantilevered structure [5, 52]. For this reason, it can provide a higher output power. However, the solid nature of this structure makes it unsuitable for energy harvesting from low magnitude vibration sources. In addition to the cantilever and cymbal structures, a high number of piezoelectric layers can be stacked forming a stacked structure (Figure 2.3 (b)) [5, 71, 72]. With this structure, the output power is significantly enhanced which makes it suitable for high load applications. However, the stacking complexity is the major drawback of this piezoelectric transducer structure.

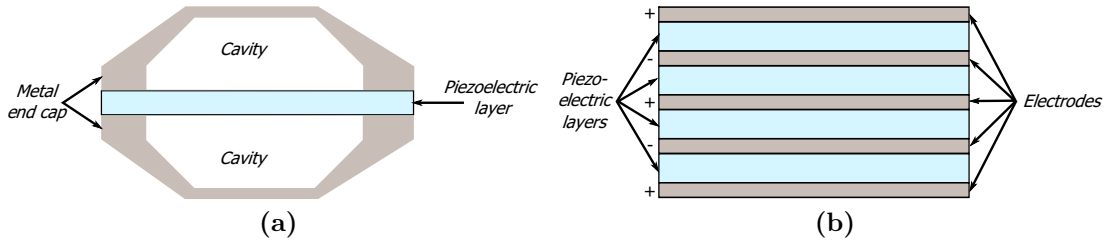


Figure 2.3.: (a) Cymbal transducer structure, (b) Stacked transducer structure [5].

The most common used materials for PT is Perovskite lead-Zirconate-Titanate (PZT) due to its high piezoelectric effect [5,73]. Other piezoelectric materials such as Polyvinylidene Fluoride polymer (PVDF) and Aluminum Nitride (AlN) are used in piezoelectric MEMS (Micro-Electro-Mechanical Systems) fabrication [74–77]. However, the choice of the piezoelectric material depends not only on the piezoelectric properties but also on other parameters related to the target application such as the available size, the environmental frequency and the required power [72].

The energy harvesting performance depends also on the piezoelectric operation mode [64, 78, 79]. According to the direction of the applied stress relative to poling direction, there are two common piezoelectric operation modes, d_{31} and d_{33}. As show in Figure 2.4, in d_{31} operation mode, the stress is applied along the poling (i.e.polarization) direction, while in the d_{33} operation mode stress is applied perpendicular to the poling direction. With a d_{33} operation mode the piezoelectric transducer generates a higher output voltage while with d_{31} operation mode yields a higher current output [64]. In terms of the output power, lee et al. [78] proved that d_{31} mode yields more output power compared to the d_{33} mode. Baker et al. [71] proved that for low-frequency vibration environments, a cantilever structure operating in mode d_{31} is more efficient than a stacked structure operating in d_{33} mode. For this reason, cantilever structures operating in d_{31} mode are the most popular configurations investigated in research works.

A piezoelectric harvester is often modeled using the basic configuration of a spring-mass-damping system [61, 80]. This system consists of a seismic mass m attached to a frame by a spring with a stiffness k. When an environmental vibration is

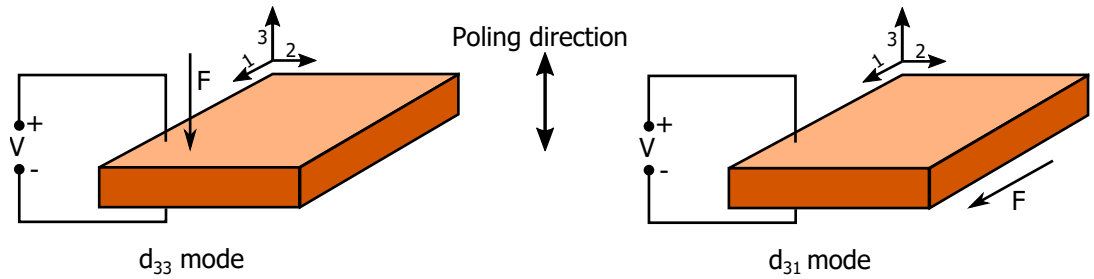


Figure 2.4.: PT operation modes.

applied to the frame, a relative displacement between the attached mass and the frame is produced through the spring. This sinusoidal displacement results in a strain in the piezoelectric material. The produced strain is then converted into an electrical charge flow by the PT. Figure 2.5 shows this electromechanical model.

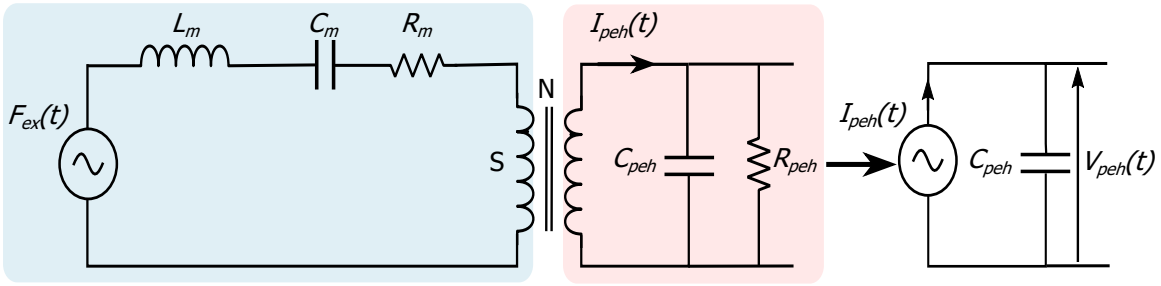


Figure 2.5.: Equivalent circuit of piezoelectric transducer PT.

The coupling between the mechanical and electrical domains is represented as a transformer with a transmission factor N, which is equivalent to the piezoelectric coefficient (d_{31} for most PTs). The mechanical domain is represented as a resonant circuit, where L_m, C_m and R_m are the equivalents of seismic mass, spring stiffness and mechanical domain losses respectively. The input of the mechanical domain is the environmental excitation signal $F_{ex}(t)$ while its output represented by S is the strain generated in the piezoelectric material. A maximum output S can be achieved when the resonance frequency of the PT is equal to the excitation frequency of $F_{ex}(t)$. The input of the electrical domain is the charge flow, i.e. the current induced by S. This current, represented as $I_{peh}(t)$ in Figure 2.5 flows through a parasitic capacitor C_{peh} formed between the two electrodes of the piezoelectric film. In addition, a resistor R_{peh} is added in parallel with C_{peh} to represent the leakage charge of this capacitor. When the piezoelectric harvester vibrates at or close to the resonance frequency, the whole piezoelectric harvester can be modeled as sinusoidal current source $I_{peh}(t)$ connected in parallel with the piezoelectric parasitic capacitor C_{peh}. Typically, the leakage resistor R_{peh} has high impedance compared to that of C_{peh}, so it is usually neglected. In this PT model, the current $I_{peh}(t)$ depends on the

amplitude and frequency of the excitation signal. This current can be expressed as:

$$I_{peh}(t) = \hat{I}_{peh} sin(\omega_0 t) = \hat{I}_{peh} sin(2\pi f_{ex} t) \tag{2.1}$$

where $\hat{I}_{peh}$ is the current amplitude, which depends on displacement amplitude, and f_{ex} is the excitation frequency.

Since the AC output voltage provided by the piezoelectric harvester depends on the excitation input amplitude and frequency, it cannot be used directly to power an electronic load. This implies the use of an interface circuit in order to rectify the AC voltage and provide a stable power supply. Another benefit of an interface circuit is the power extraction optimization. For vibration harvesters, there exists an optimal output voltage at which a maximum output power can be extracted from the piezoelectric harvester. The interface circuit is also used to maintain the optimal output voltage under any circumstances even under low excitation levels. Often, in wireless sensors applications, the load needs to be powered regularly for a short time interval. When the load is not active, the interface circuit stores the extracted power in a buffer such as a supercapacitor or a rechargeable battery.

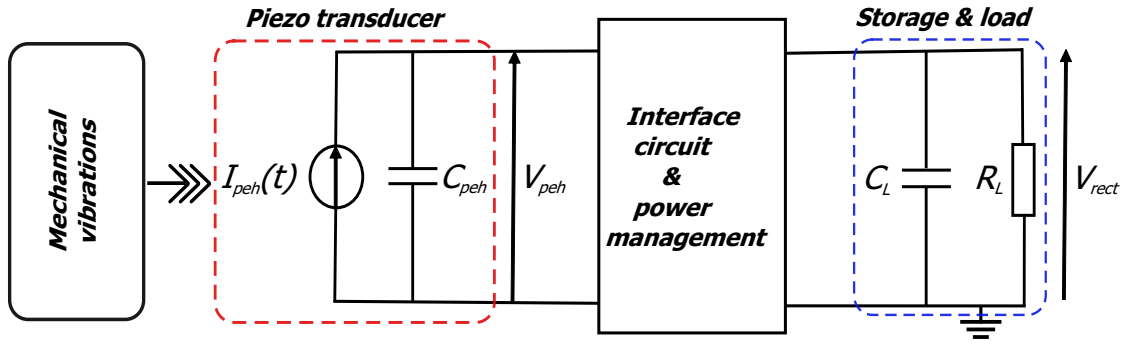


Figure 2.6.: Equivalent circuit of piezoelectric harvesting system (PHS).

Therefore, the equivalent circuit of a piezoelectric harvesting system (PHS) as shown in Figure 2.6 consists of a piezoelectric transducer modeled by a current source $I_{peh}(t)$ in parallel with the piezoelectric parasitic capacitor C_{peh}, an interface circuit and a storage with load elements. Even with a PT with high AC output power, the PHS's efficiency significantly depends on the interface circuit efficiency. In fact, the need to charge and discharge the PT parasitic capacitor C_{peh} every time $I_{peh}(t)$ changes its phase extremely limits the PHS efficiency. In addition, the unsteady environmental operating conditions of the PT are also another limitation, which affects the PHS's efficiency. This makes the design of an efficient interface circuit necessary in order to overcome the existing limitations and extract the maximum of energy provided by the PT.

2.3. Maximum AC output power of a PT

In this section, the maximum power provided by the PT is studied. As discussed before, when the PT vibrates at or close its resonance frequency, it can be represented as a current source I_{peh} in parallel with its inherent capacitor C_{peh} and a resistor R_{peh}. The impedance of the resistor is usually too high compared to that of C_{peh}, so it is ignored to simplify the calculations. Since the current source depends directly on the input vibrations, it is usually considered as a sinusoidal current source where the current amplitude is proportional to the vibration amplitude. This current source can be expressed as $I_{peh}(t) = \hat{I}_{peh} sin(\omega_0 t)$, where $\omega_0 = 2\pi f_{ex}$ and f_{ex} is the excitation frequency. The available charge generated by the PT in every cycle is given by:

$$Q_{tot/cycle} = 2\int_0^{T/2} I_{peh}(t)dt = \frac{4\hat{I}_{peh}}{\omega_0} = 4C_{peh}V_{oc} \tag{2.2}$$

where V_{oc} is the open circuit voltage of the PT when no load is connected to its output and the total induced current I_{peh} flows through C_{peh} (Figure 2.7 (a)). Hence, the available power delivered by the PT can be expressed as:

$$P_{tot} = Q_{tot}V_{oc}f_{ex} = 4C_{peh}V_{oc}^2 f_{ex} \tag{2.3}$$

The maximum output power provided by the PT can be defined as the power consumed in a resistor load when its resistance value matches the internal impedance of the PT.

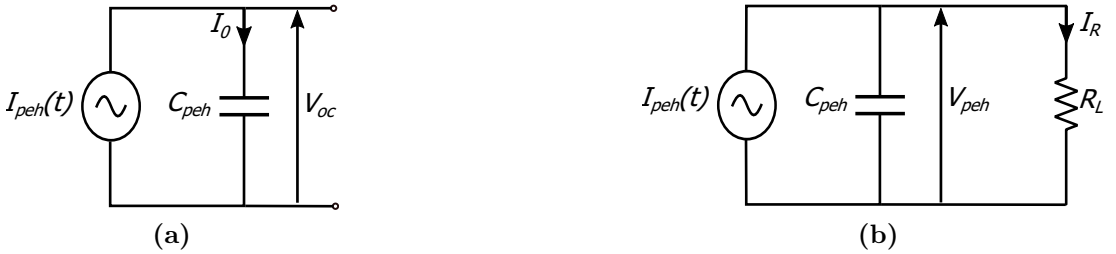


Figure 2.7.: (a) PT in an open circuit configuration, (b) PT with a load resistor.

To evaluate this power, a variable resistor R_L is connected to the output of the PT (Figure 2.7 (b)). The average power dissipated in R_L can be expressed as:

$$P_R = \frac{1}{2}\hat{I}_R^2 R_L \tag{2.4}$$

where $\hat{I}_R$ is the amplitude of the current $I_R(j\omega_0)$ flowing in R_L. This current is

calculated by:

$$I_R(j\omega_0) = \hat{I}_{peh}\frac{Z_C}{Z_C + R_L} = \frac{\hat{I}_{peh}}{1 + j\omega_0 R_L C_{peh}} \tag{2.5}$$

Therefore, the power consumed by R_L is:

$$P_R = \frac{1}{2} I_{peh}^2 \frac{R_L}{1 + \omega_0^2 R_L^2 C_{peh}^2} \tag{2.6}$$

When $R_L = \frac{1}{\omega_0 C_{peh}}$, P_R reaches its maximum expressed by:

$$P_{R(max)} = \frac{I_{peh}^2}{4\omega_0 C_{peh}} \tag{2.7}$$

Typically, the load circuit of the PT is not a simple resistor but it can be analog/digital circuits such as sensors. These circuits require a DC voltage to operate. Since the PT generates an alternating voltage, the later needs to be rectified before using it to power the load circuits.

2.4. Literature survey of interface circuit typologies for PEH

Typically, the power provided by the piezoelectric vibration energy harvesting is in the range of 10-100µW/cm^2 [25, 26, 73, 81]. This adds another constraint to the design of the interface circuit. In summary, to achieve high power efficiency in PEH, the interface circuit has to extract power from the PT even under low excitation levels, rectify efficiently the PT output voltage and then maintain the PHS output voltage at an optimal value in order to reach the maximum output power. This maximum output power is significantly conditioned by the power consumption of the designed interface circuit.

This section presents an overall detailed study of different typologies proposed in the state-of-the-art for PEH in addition to the output power carried achieved by these typologies.

2.4.1. Common interface circuit typologies

Three common interface circuits, full bridge rectifier (FBR), Switch-Only and synchronized electric charge extraction (SECE) interface circuits are detailed in the following. Each of these circuits invests a different technique for energy harvesting from the PT. These techniques represent the basic techniques which are then combined or developed to optimize the harvested energy from the PT.

2.4.1.1. Full Bridge Rectifier (FBR) interface circuit

The diode-based full bridge rectifier FBR is the most commonly used interface circuit to perform AC/DC conversion [25–30]. Figure 2.8 shows the circuit typology with the associated waveforms. The harvested energy using the FBR is stored in a storage capacitor C_L. Since $C_L \gg C_{peh}$, the output voltage V_{rect} across C_L can be considered as a stable voltage. As illustrated in Figure 2.8 (b), in the positive cycle of I_{peh}, before the generated charge by PT can be transferred to C_L, I_{peh} charges the inherent capacitor C_{peh} from zero to $V_{rect} + 2V_{th}$, where V_{th} is the threshold voltage of each diode. During this charging period the FBR is still in off state, as shown by t_{off} in Figure 2.8 (b). When V_{peh} reaches $V_{rect} + 2V_{th}$, diodes D_1, D_4 start conducting and the rest of the generated charge by the PT is transferred to C_L.

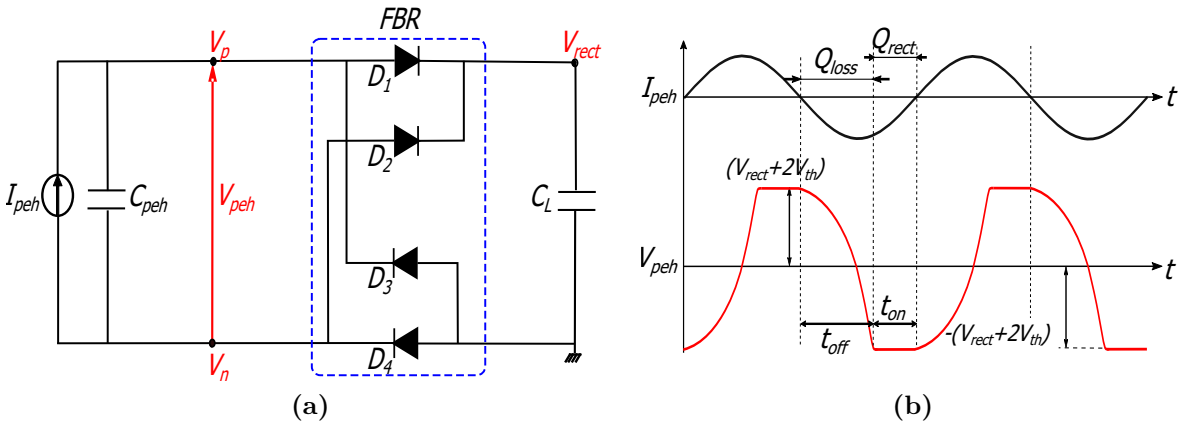


Figure 2.8.: (a) Full bridge rectifier (FBR) typology, (b) Associated waveforms.

This charge transfer, shown by t_{on} in Figure 2.8 (b), remains until I_{peh} changes its direction. During the negative cycle of I_{peh}, before the charge can be transferred to C_L, C_{peh} should be discharged form $V_{rect}+2V_{th}$ to zero and recharged again from zero to $-(V_{rect} + 2V_{th})$. When V_{peh} exceeds $-(V_{rect} + 2V_{th})$, D_2 and D_3 start conducting and I_{peh} flows through C_L. Because only the transferred charge into C_L (shown by Q_{rect} in Figure 2.8 (b)), can be used to power the piezoelectric harvester load circuit, the amount of charge used to charge and discharge C_{peh} is considered as lost. This lost charge is shown by Q_{loss} in Figure 2.8 (b). For each half I_{peh} cycle, the lost charge $Q_{loss/cycle}$ can be calculated as:

$$Q_{loss/cycle} = 2[C_{peh}(V_{rect} + 2V_{th}) - C_{peh}(-(V_{rect} + 2V_{th}))] = 4C_{peh}(V_{rect} + 2V_{th}) \tag{2.8}$$

This amount of charge depends on the value of V_{th}. For a higher V_{th}, significant charge is lost.

From (2.2) and (2.8), it can be concluded that the amount of charge that is actually

transferred into C_L during one I_{peh} cycle can be expressed as:

$$Q_{rect/cycle} = Q_{tot/cycle} - Q_{loss/cycle} = 4C_{peh}(V_{oc} - (V_{rect} + 2V_{th})) \tag{2.9}$$

Hence, the total energy delivered by the FBR to C_L in every cycle can be calculated as:

$$E_{rect/cycle} = Q_{rect/cycle}V_{rect} = 4C_{peh}V_{rect}(V_{oc} - (V_{rect} + 2V_{th})) \tag{2.10}$$

As the vibration frequency is f_{ex}, the power delivered to the output by FBR is:

$$P_{rect-FBR} = E_{rect/cycle}f_{ex} = 4C_{peh}V_{rect}f_{ex}(V_{oc} - V_{rect} - 2V_{th}) \tag{2.11}$$

From (2.11), it can be concluded that no power can be delivered by FBR to the output load when $V_{rect} = 0V$ or $V_{rect} = V_{oc} - 2V_{th}$. In addition, a maximum output power can be achieved when $V_{rect} = \frac{V_{oc}}{2} - V_{th}$. As a result, the maximum output power delivered by FBR is:

$$P_{rectmax-FBR} = 4C_{peh}f_{ex}(\frac{V_{oc}}{2} - V_{th})^2 \tag{2.12}$$

Various implementations of bridge rectifier have been proposed in the state of the art in order to decrease V_{th} as much as possible [25, 28, 30, 82]. In [28], standard diodes are replaced by Schottky diodes, which decreases the threshold voltage from $0.7V$ to $0.41V$. In [25], CMOS diodes (i.e. MOSFETs connected in diodes), are used to form the bridge circuit. This reduces the threshold voltage to $0.38V$. In such implementation, since MOSFETs act as switches, a reverse current can flow back from C_L to the PT which decreases the power efficiency. Replacing two MOSFETs diodes (D_1, D_2) by two active diodes in [30] prevents the reverse current and reduces the threshold voltage V_{th} down to $0.021V$, which in turn increases the power efficiency.

The maximum power that can be extracted by the FBR is usually used to evaluate performance of interface circuits [7, 25, 32, 82–85]. This performance of an interface circuit, noted as MOPIR (Maximum Output Power Improvement Ratio) is given by:

$$MOPIR = \frac{P_{rectmax-interface}}{P_{rectmax-FBR}} \tag{2.13}$$

As $P_{rectmax-FBR}$ depends on the value of V_{th}, therefore, for performance comparison purpose between the interface circuits, V_{th} is mostly ignored. Hence, the maximum output power extracted by FBR, used to evaluate the $MOPIR$ can be written as:

$$P_{rectmax-FBR} = C_{peh}f_{ex}V_{oc}^2 \tag{2.14}$$

2.4.1.2. Switch-Only interface circuit

Although the threshold voltage in the bridge circuit interface is significantly reduced, the charge wasted in discharging and recharging the inherent capacitor C_{peh} every time I_{peh} changes its phase extremely limits the maximum extracted power. In addition, the higher the C_{peh}, the greater the charge loss resulting from its discharging and recharging. To reduce this charge loss, Y. Ramadass [81] proposed a topology called Switch-Only interface circuit. Figure 2.9 shows the circuit topology and the associated waveforms.

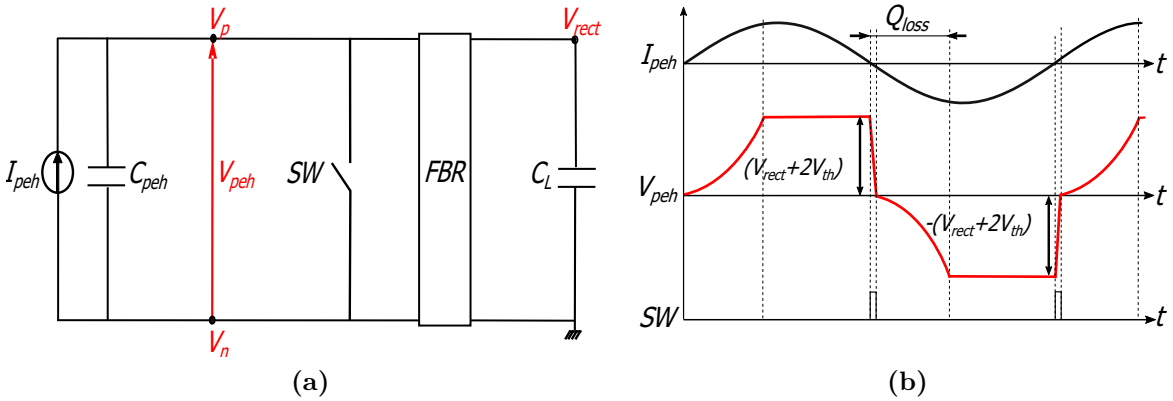


Figure 2.9.: (a) Switch-Only interface circuit, (b) Associated waveforms.

In this topology, a simple switch connected in parallel with C_{peh} is added to a FBR in order to instantly discharge C_{peh}. As shown in Figure 2.9 (b), at each zero crossing moment of I_{peh} , the switch SW is turned on briefly to instantly discharge C_{peh}. Therefore, I_{peh} has only to recharge C_{peh} from 0 to $+(V_{rect} + 2V_{th})$ every half cycle, which decreases the lost charge during one cycle $Q_{loss/cycle}$ to:

$$Q_{loss/cycle} = 2C_{peh}(V_{rect} + 2V_{th}) \tag{2.15}$$

From (2.2) and (2.15), the charge that is actually transferred to the output during one I_{peh} cycle can be calculated as:

$$Q_{rect/cycle} = Q_{tot/cycle} - Q_{loss/cycle} = 4C_{peh}V_{oc} - 2(V_{rect} + 2V_{th}) \tag{2.16}$$

Assuming an ideal FBR where $V_{th} = 0V$, the extracted by Switch-Only interface circuit can be given by:

$$P_{rect-SO} = Q_{rect/cycle}f_{ex}V_{rect} = 2C_{peh}V_{rect}f_{ex}(2V_{oc} - V_{rect}) \tag{2.17}$$

This equation shows that no power can be delivered when $V_{rect} = 0V$ or $V_{rect} = 2V_{oc}$.

In contrast, maximum power can be extracted when $V_{rect} = V_{oc}$:

$$P_{rectmax-SO} = 2C_{peh}f_{ex}V_{oc}^2 \tag{2.18}$$

The Switch-Only performance can be evaluated using the expression of the MOPIR in (2.13):

$$MOPIR = \frac{P_{rectmax-SO}}{P_{rectmax-FBR}} = 2 \tag{2.19}$$

As a result, using the Switch-Only topology proposed in [25], allows to double the delivered power to the output compared to the power delivered by FBR. Although the Switch-Only circuit eliminates the required time to discharge C_{peh} and doubles the output power, the charge loss resulting form the need to recharge C_{peh} remains the main drawback of this interface circuit.

2.4.1.3. Synchronized electric charge extraction (SECE)

Another common interface circuit called synchronized electric charge extraction (SECE) has been proposed in [80, 86–91] to further reduce the charge loss and improve the power efficiency. Unlike Switch-Only circuit, instead of discharging C_{peh} through the ground, an inductor is employed to store the available energy built up in C_{peh} and then transfer it to the output buffer. Figure 2.10 shows the SECE interface topology and the associated waveforms. The charge transfer from C_{peh} to the output is performed in a short period compared to the excitation period. This significantly reduces the wasted time in discharging C_{peh} when using the FBR. As shown in Figure 2.10 (b), out the transfer periods, the PT operates in an open circuit configuration for most of the time. This makes the extracted power constant for a given V_{oc}, and independent from the load.

Figure 2.10 (a) shows SECE interface circuit. It consists of three switches S_1, S_2, S_3 and an inductor L combined to a FBR. The energy transfer operation is triggered when the voltage across the PT achieves its maximum by closing switch S_1 (Figure 2.10 (b)). This connects L in parallel with C_{peh} forming a resonant LC circuit. As a result, the charge in C_{peh} is extracted and stored in the inductor. When the available charge in C_{peh} is completely stored in L, the inductor current I_L reaches its maximum value. At this moment the S_1 is turned off and S_2, S_3 are turned on simultaneously. This allows to transfer the charge stored in L to C_L through a new former by L and C_L circuit. After the energy transfer operation is completed, all switches are turned off and the PT operates again in open circuit configuration.

Although the charge built up in C_{peh} each half cycle can be stored and extracted by an inductor, there is still energy loss due to the parasitic resistance of the conduction path, which limits the stored, and thus the extracted power. According to [92], the

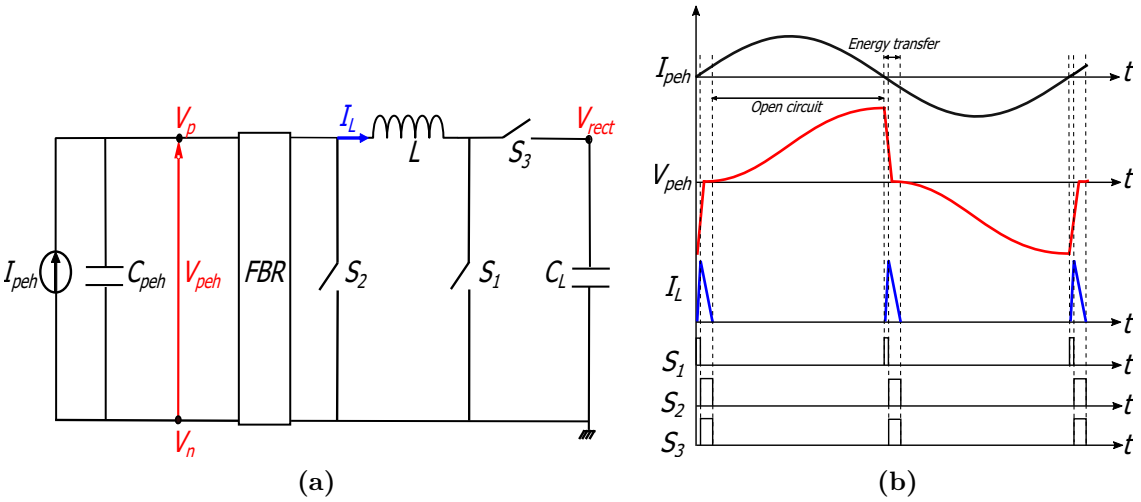


Figure 2.10.: (a) SECE interface circuit, (b) Associated waveforms.

stored energy energy in L for a half cycle of I_{peh} can be expressed as:

$$E_L = 2C_{peh}V_{oc}^2 e^{-\pi/(\omega_{01}\tau)} \tag{2.20}$$

where $\omega_{01} = 1/\sqrt{LC_{peh}}$ and $\tau = 2L/R_1$, with R_1 representing all parasitic resistances through the current path.

The maximum power extracted by SECE was expressed in [87] as:

$$P_{SECE} = \frac{2\Gamma^2\omega}{\pi C_{peh}} \left(\frac{m\alpha_0}{d\omega_0 + \frac{4\Gamma^2}{\pi C_{peh}}} \right)^2 \tag{2.21}$$

where m is the effective mass, α_0 is the excitation acceleration amplitude, Γ is the coupling factor, d is the damping factor.

This extracted power is significantly related to the coupling factor Γ. As proved in [80], there is an optimal coupling factor at which the SECE can extract the totality of power provided by PT, it is given by $P_{max} = \frac{(m\alpha_0)^2}{8d}$ [87, 88]. In [80, 88], it was demonstrated that the SECE interface circuit extracts about 4 times more power than the FBR rectifier when the PT is weakly coupled. Otherwise, the FBR rectifier is more efficient. In addition to the coupling factor, the SECE extracted power depends also on the excitation frequency as demonstrated in equation (2.21). In [80], it was proved that the SECE circuit can increase the extracted power to about 124% of the FBR if the PT is excited at resonance. Otherwise, the extracted power is significantly decreased. But on the other hand, as it is proved in [80], this power is enhanced to 400 % of the maximum power extracted by the FBR. In the enhanced SECE [90], the energy is transferred in a multi-stages process to reduce the conduction losses and then improve the power conversion efficiency. Another

improved SECE is proposed in [92] to enhance the power efficiency without the load dependence. Recently, an optimized circuit of SECE in the case of shock type excitation was presented in [89]. Although the SECE interface circuit can significantly improve the power efficiency compared to both FBR and Switch-Only circuits when PT is weakly coupled, there is still energy loss related to quality factor of L and the parasitic resistance of the conduction path. In addition, the need to recharge up C_{peh} from 0 to $\pm V_{oc}$ before energy extraction from PT remains the main drawback of this interface.

2.4.2. Advanced active interface circuit typologies

In addition to the use of SECE and Switch-Only typologies as active interface circuits to reduce the charge loss, other active interface circuits were also proposed in the literature to further improve the extracted power from the PT. In fact, in SECE circuits, a part of charge generated by the PT is lost to recharge C_{peh} from 0 to $\pm V_{oc}$, and the extracted power is significantly related to the PT coupling and exciting conditions. In Switch-Only circuit, there is a charge loss because of discharging C_{peh} through the ground and the need to recharge it from 0 to $\pm V_{rect}$. To get rid of these limitations in both SECE and Switch-Only circuits, other advanced interface circuits were proposed in literature such as synchronized switch harvesting on inductor (SSHI) and synchronized switch harvesting on capacitor (SSHC). In these circuits, an inductor or capacitors is employed to flip the voltage across C_{peh}. This significantly reduces the wasted charge and hence improves the extracted power.

2.4.2.1. Synchronized switch harvesting on inductor (SSHI)

To reduce the charge wasted in recharging C_{peh} from 0 to $\pm V_{oc}$ each half cycle in SECE circuits, a parallel synchronized switch harvesting on intuctor (P-SSHI) interface circuit was proposed in [25]. Figure 2.11 shows the topology and the associated waveforms of this interface.

In this circuit, in addition to the FBR, a switch S and an inductor L connected in series are connected in parallel with the PT. This switched inductor is not used to discharge C_{peh} and transfer its energy to C_L as in SECE circuit, but to recharge C_{peh} in the inverse direction. This in turn leads to flip the V_{peh} across the PT. The V_{peh} flipping operation is triggered when I_{peh} zero crossing is detected. At this moment, the switch S is briefly closed forming an LC resonance circuit. When the inductor current reaches zero indicating the end of charge transfer from L to C_{peh}, the S switch is opened again. Due to the ON-resistance of the used switch and the parasitic resistance of the inductor, a charge loss occurs during the charge transfer between L and C_{peh}. Therefore, the reversed voltage V_b across PT is lower than V_{peh} as shown in Figure 2.11 (b). As a result, C_{peh} has to be charged only from $\pm V_b$ to $\pm V_{rect}$ before the piezoelectric current can flow to the output. This significantly

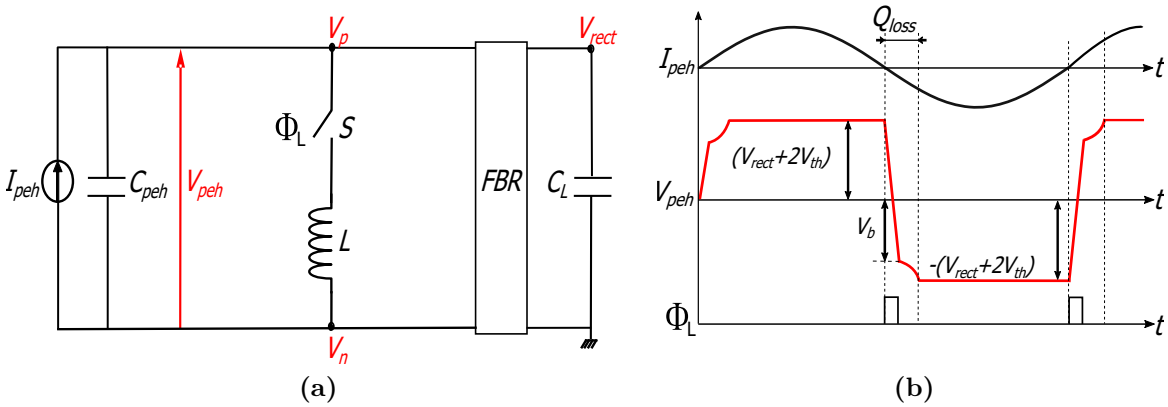


Figure 2.11.: (a) P-SSHI interface circuit, (b) Current, voltage and control signal waveforms.

reduces the charge wasted in recharging C_{peh} comparing to both SECE and Switch-Only circuits. Assuming an ideal FBR, when S is ON and after the voltage flip across C_{peh}, the final V_b according to [25] is given by:

$$V_b = -V_{rect} e^{-\frac{\pi R}{2\omega L C_{peh}}} \tag{2.22}$$

where $\omega = \sqrt{\omega_0^2 - \beta^2}$, $\omega_0 = \frac{1}{\sqrt{LC_{peh}}}$, $\beta = \frac{R}{2L}$ and R represents all parasitic resistances in the resonant loop.

From the previous equation, the ratio between V_b and V_{rect} denoted as η_{P_SSHI} can be expressed as:

$$\eta_{P\_SSHI} = \frac{V_b}{V_{rect}} = e^{-\frac{\pi R}{2\omega L C_{peh}}} \tag{2.23}$$

The amount of charge lost to build up the voltage across C_{peh} from V_b to V_{rect} during one cycle can be calculated as:

$$Q_{loss/cycle} = 2C_{peh}V_{rect}(1 - e^{-\frac{\pi R}{2\omega L C_{peh}}}) = 2C_{peh}V_{rect}(1 - \eta_{P\_SSHI}) \tag{2.24}$$

Therefore, the amount of charge that can flow to the output during one cycle is given by:

$$Q_{rect/cycle} = Q_{tot/cycle} - Q_{loss/cycle} = 4C_{peh}V_{oc} - 2C_{peh}V_{rect}(1 - \eta_{P\_SSHI}) \tag{2.25}$$

Thus, the power that can be extracted by the P-SSHI interface circuit can be cal-

culated as:

$$P_{rect} = 2C_{peh}V_{rect}f_{ex}\left(2V_{oc} - V_{rect}(1 - \eta_{P\_SSHI})\right) \tag{2.26}$$

From (2.23), (2.24) and (2.26), it can be concluded that the higher V_b is, the less the charge wasted to achieve V_{rect} and the more power is extracted. For an ideal S and L, when $R = 0\Omega$, the voltage flip efficiency η_{P_SSHI} equals 1. In this case, the totality of energy delivered by the PT can be extracted and transferred to the output. As η_{P_SSHI} is related to both L and R, achieving high power efficiency requires the use of a speed switch and a large inductor with a minimal loss. In [25], employing an inductor of $820\mu H$ boosted both the maximum extracted power and its optimal output voltage about $4\times$ compared to the maximum extracted power and its optimal output voltage when using the FBR. Furthermore, unlike the SECE interface circuit, the charge transfer in P-SSHI circuit starts when $V_{peh} = V_{rect}$ and continues until the V_{peh} needs to be flipped. During this period, the PT is connected to the output and the output power is load dependent. Different improved SSHI circuits have been proposed in literature [8, 31, 85, 93–95]. Lefeuvre et al. proposed in [93] a series synchronized switch on inductor (S-SSHI) circuit. In this circuit, the switched inductor is connected in series with the PT and the PT operates in an open circuit configuration most of the time. This significantly decreases the load dependency. In [94], a triple bias-flip SSHI circuit was proposed to decrease the charge loss during PT voltage flip operation. A P-SSHI circuit is proposed in [8] to harvest the shock vibration energy. In [25], the inductor of the SSHI circuit is also shared with a DC-DC converter to have a compact system. A self-powdered hybrid SSHI was proposed in [31] for the wide operating range of PT.

2.4.2.2. Synchronized switch harvesting on capacitor (SSHC)

In both of SECE and SSHI circuits, the RCL resonant circuits formed during the charge transfer between L and C (i.e. C_{peh} in SSHI, C_{peh} or C_L in SECE) makes the use of a large inductor in range of mH is mandatory to extract sufficient power required to supply the load. This dramatically increases the overall volume of the harvesting system and makes it unsuitable for the compact (MEMS) applications. This also increases the ON-resistance of the current path and necessitates employing speed switches. To address this problem, different typologies of synchronized switch harvesting on capacitor (SSHC) interface circuit were proposed in [7, 32–34]. In this interface circuit, one or more capacitors are employed instead of an inductor to flip the voltage across C_{peh}. Figure 2.12 (a) shows a one-capacitor SSHC interface circuit [7]. It consists of a full bridge rectifier (FBR) with only one switched flipping capacitor C_0 used to flip the voltage V_{peh} across the PT. The V_{peh} inversion is realized using five analog switches. Figure 2.12 (b) shows the associated current, voltage and the control signals waveforms of SSHC circuit. The V_{peh} inversion operation is performed in three phases: 1) the sharing phase (Φ_p) when the charge in C_{peh} is

shared with C_0, 2) the shorting phase (Φ_0) when C_{peh} is completely discharged to get rid of its residual charge and finally 3) the building phase (Φ_n) when C_{peh} is recharged from C_0 in the reverse direction.

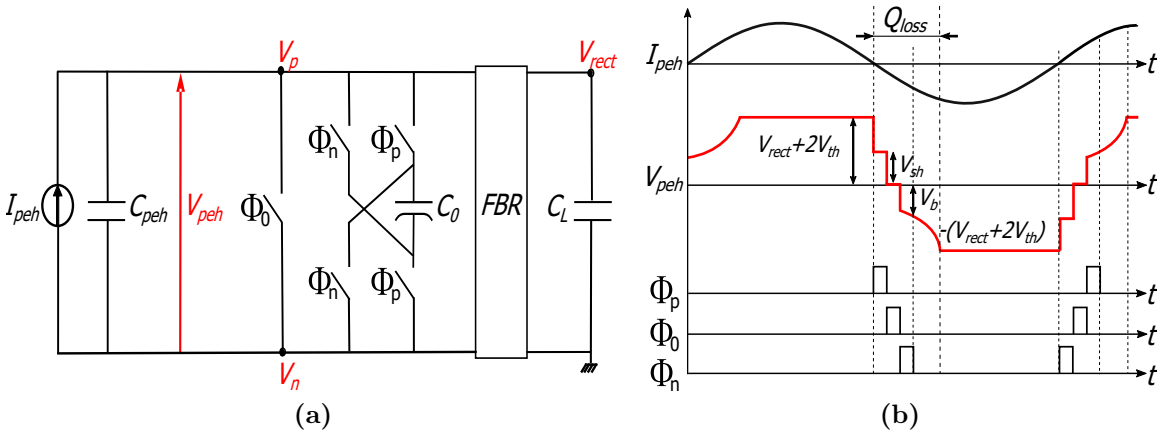


Figure 2.12.: (a) One-capacitor SSHC interface circuit, (b) Current, voltage and control signals waveforms.

As shown in Figure 2.12 (b), the voltage across PT before the flipping moment is $V_{peh} = V_{rect} + 2V_{th}$, where V_{rect} is the voltage across the storage capacitor and V_{th} is the threshold voltage across the FBR diode. In Figure 2.12 (b), V_{sh} and V_b represent the voltages across PT at the end of the sharing and the building phases, respectively. In steady state, V_b becomes constant and C_{peh} needs to further charge from V_b to $V_{rect} + 2V_{th}$. In order to evaluate the voltage flip efficiency and the performance of this interface, charge conservation equations (2.27) and (2.28) are applied during both sharing and building phases, respectively:

$$V_{sh}(C_{peh} + C_0) = C_{peh}(V_{rect} + 2V_{th}) + C_0 V_b \tag{2.27}$$

$$V_b(C_{peh} + C_0) = V_{sh} C_0 \tag{2.28}$$

Assuming an ideal FBR, i.e. with no threshold, the ratio between V_b and V_{rect} can be expressed as [32]:

$$k_{FCR1} = \frac{V_b}{V_{rect}} = \frac{1}{2 + \frac{C_{peh}}{C_0}} \tag{2.29}$$

The amount of charge lost to build up the voltage across C_{peh} from V_b to V_{rect} during one cycle can be calculated as:

$$Q_{loss/cycle} = 2C_{peh}(V_{rect} - V_b) = 2C_{peh}V_{rect}(1 - k_{FCR1}) \tag{2.30}$$

Therefore, the amount of charge that is actually transferred to the output is given by:

$$Q_{rect/cycle} = Q_{tot/cycle} - Q_{loss/cycle} = 4C_{peh}V_{oc} - 2C_{peh}V_{rect}(1 - k_{FCR1}) \tag{2.31}$$

Hence, the power that can be extracted by the one-capacitor SSHC interface circuit can be calculated as:

$$P_{rect} = 2C_{peh}V_{rect}f_{ex}\left(2V_{oc} - V_{rect}(1 - k_{FCR1})\right) \tag{2.32}$$

As a result, the extracted power is related to the voltage flip efficiency k_{FCR1}. For one-capacitor SSHC circuit, k_{FCR1} converges to 1/2 when $C_0 \gg C_{peh}$. This allows to extract four times more power compared to the power extracted by the FBR. In order to improve the voltage flip efficiency of the SSHC interface circuit, several implementations have been proposed in the literature. In [7], eight parallel flipping capacitors were used to improve the voltage flip efficiency to 4/5. To reach this efficiency using SSHI circuit as reported in [7], a $5.6mH$ inductor with a significant volume is required. Recently, it was proved in [34] that using $C_0 = 100C_{peh}$ increases the output power by 35.7%. In another implementation proposed in [32], the use of four re-configurable capacitors increases the voltage flip efficiency to 0.85% and the MOPIR to 4.83. This topology requires a seven-phases voltage flip scheme. Increasing the number of switching phases to 21 phases as in [96] improves the MOPIR to 9.3. However, as shown in [7], the use of a large number of parallel flipping capacitors increases the number of switching phases and hence the flipping time. This in turn reduces the conduction time and thus the extracted power. Also, using the re-configurable flipping capacitors in [32, 96] increases the number of required switches, this in turn increases the ON-resistance during one flipping phase and thus increases the flipping time. In conclusion, increasing the number of flipping capacitors or phases to improve the flipping efficiency implies fast voltage flip operation. This can be achieved only when C_{peh} is low. The use of large C_{peh} in such implementations will significantly increase the charge loss and hamper the voltage flip and the power efficiencies.

2.4.3. Problems and limitations of existing typologies

As previously discussed, the main objective of the interface circuit is to make use of the AC power provided by the PT. This can be achieved using different kinds of interface circuits. However, as the output power of the majority of PTs is limited to a few tens of micro-watts, a significant constraint is set on the power efficiency of the associated interface circuit. Thereby, in addition to the design of ultra-low power interface circuit requirement, this circuit should also be able to extract as much power as possible from the power delivered by the PT. This requires reducing

the charge loss resulting from charging and discharging C_{peh} every time I_{peh} changes direction. In other words, the associated interface circuit should be able to flip the voltage across C_{peh} efficiently in a short time compared to the excitation frequency. As discussed before, despite the simplicity of the FBR interface circuit, its power efficiency is very low due to the high threshold voltage of its rectifying diodes and the significant charge loss resulted when the voltage across C_{peh} is flipped. The power efficiency was improved in many research works using an enhanced low-threshold voltage FBR in addition to the other components employed to efficiently flip the voltage across C_{peh} [25, 97]. Using one switch in the Switch-Only interface circuit to discharge C_{peh} through the ground significantly reduced the charge loss during the voltage flip across C_{peh} [25]. However, there still remains a charge loss related to the need to recharge C_{peh} from 0 to V_{pehmax} before the PT charge can be transferred to the output. Employing an inductor in both SECE and SSHI interface circuits significantly enhanced the power efficiency compared to both FBR and Switch-Only circuits. However, this power efficiency can be achieved when the inductor has a high quality factor but this dramatically increases the overall system volume. Moreover, an RLC tuning is an another condition to achieve an acceptable power efficiency in P-SSHI [81] circuit while the PT should be weakly coupled in SECE to reach a better power efficiency than that of the FBR [80, 88]. These limitations are overcome by replacing the inductor by parallel/re-configurable capacitors in SSHC interface circuit to flip the voltage across the PT. In such circuits, the system volume is significantly decreased [7]. However, achieving the high power efficiency in SSHC circuits requires a large number of switched capacitors [7] or flipping phases [32, 96] which implies fast voltage flip operation. This can be achieved only when C_{peh} is low ($< 50nF$) [7, 32, 33, 96, 97], otherwise, the use of large C_{peh} in such circuits dramatically increases the charge loss and hampers the system performance. Moreover, increasing the number of flipping capacitors/phases leads to increase the control complexity.

In addition to all these limitations of the existing typologies, the low PT excitation level dramatically limits both the PT output voltage and the generated power. The higher the excitation level, the higher V_{oc} and then, the higher the power provided by the PT according to equation 2.3. This equation also shows that a little increase in V_{oc} leads to a significant increase in the PT generated power which in turn increases the extracted power. In the majority of the works presented in the literature, in order to extract an acceptable power from the PT, this one was excited to have an open circuit voltage greater than $1V$ [7, 25, 29, 32, 87, 98–100]. In [97], where an inductor and an external capacitor are employed for power extraction, it was proved that when V_{oc} was decreased from $2.75V$ down to $1.02V$, the extracted power was dramatically decreased from $24.2\mu W$ to $4.7\mu W$ which extremely limits its applications. The advantages and limitations of the discussed typologies are summarized in Table 2.1.

The design of an inductor-less fully integrated/compact interface circuit that can efficiently perform the PT voltage inversion even though the PT has a relatively high parasitic capacitor will be of interest for some application domains. In addition to

the power efficiency, the capability to extract an amount of power even when the PT operates under low level excitation is also an important factor of such interface circuit, which should be taken into account in the design considerations.

IC	Components	Features	Drawbacks & limitations
FBR	Diodes	- Simple structure. - Full integration ability.	- High threshold voltage drop. - Limited to high excitation source applications. - Significant charge wasted to flip the V_{peh}.
Switch-Only	One switch	- Simple structure. - Full integration ability. -2Xextracted power more than FBR.	- The loss of the charge built up in C_{peh}. - Low output power when $V_{oc} \leq 1V$. - Charge loss to recharge C_{peh} from 0 to $\pm(V_{rect} + 2V_{th})$.
SECE	Inductor	- Extraction of the majority of charge from C_{peh}. - Low sensitivity to load impedance. - Constant output power.	- Requires a large inductor. - Limited to the meso/macro scale applications. - Charge loss to recharge C_{peh} from 0 to $\pm V_{oc}$. - Low power efficiency for a coupling factor. - Low output power at off-resonance operating conditions and when $V_{oc} \leq 1V$.
SSHI	Inductor	- Reduced charge lost in recharging C_{peh}. - Boosted extracted power.	- Load-dependent and RCL tuning requirement. - Large inductor/no fully integration ability. - Low output power when $V_{oc} \leq 1V$.
SSHC	Capacitor	- Enhanced extracted power for weakly/strongly coupled PT. - Significant overall system volume reduction. - Full integration ability. - Reduced charge lost in recharging C_{peh}.	- Load-dependent. - Complex control. - Low output power when C_{peh} is high and $V_{oc} \leq 1V$. - Large number of flipping capacitors/phases requirement.

Table 2.1.: Comparison between main schemes of interface circuits

3. Full Active Rectifier (FAR)

3.1. Introduction

In piezoelectric energy harvesting (PEH), in order to increase the performance of the passive FBR interface circuit, most of the interface circuits proposed in literature aim to circumvent the lost energy due, on one hand to the high threshold voltage of the rectifying diodes, and on the other hand to the charge loss resulting from discharging and recharging C_{peh} when I_{peh} reverses its direction. The first issue was addressed by performing an active rectification as in [30,101]. Other additional components such as an inductor in SECE and SSHI circuits [25, 52, 80, 88] or capacitors in SSHC circuit [7, 32, 33] have been employed in a way that minimizes the charge lost in discharging and recharging C_{peh}. The basic principle of these circuits consists in either extracting energy from PT only when $I_{peh} = 0A$ (SECE) or reusing the charge built up in C_{peh} to help invert the voltage across C_{peh} when $I_{peh} = 0A$ (SSHI and SSHC). However, SECE and SSHI typologies require large inductors ($> 10mH$) to reach acceptable extracted power. They are thus unsuitable for ultra-compact integrated systems. Moreover, the PT should be weakly coupled in SECE circuits to achieve better efficiency than FBR, and SSHI circuits require fine RLC tuning to reach satisfactory power efficiency. Regarding SSHC interfaces proposed in the literature, achieving high power efficiency necessitates a large number of switched capacitors or flipping phases. This implies a fast V_{peh} flip operation that can be achieved only when C_{peh} is low. Otherwise, the use of high C_{peh} increases the associated discharging/charging time constant (RC), and thus the charge loss during the flipping phases. Furthermore, increasing the number of on/off chip components leads to the increase of control complexity of the PHS and its overall power consumption. This in turn hinders the system performance especially when the PT operates under low level excitation conditions.
This chapter presents two schemes of a full active rectifier, the first one is the basic scheme FAR, i.e. Full Active Rectifier, the second is FAR with charge recycling circuit (FAR-CR). Both schemes are based on the same voltage flip concept as in SSHI and SSHC. Unlike SSHI and SSHC systems, the proposed schemes reach a high voltage flip efficiency without the need for an inductor or a significant number of capacitors. This dramatically reduces the system volume and complexity. The first scheme is a fully integrated topology where neither an inductor nor capacitors are needed to increase the voltage flip efficiency. In the second scheme, a simple charge recycling circuit is added to boost the voltage flip efficiency using a single capacitor.

A typical architecture of an active interface is presented in section 3.2. The basic FAR and FAR-CR schemes are presented in section 3.3 and section 3.4 respectively. Section 3.5 describes the circuit implementation of the FAR/FAR-CR. Simulation results of both FAR and FAR-CR circuits are shown in section 3.6. Section 3.7 is dedicated to the measurement results and the discussion of both schemes. Section 3.8 concludes this chapter.

3.2. Typical architecture of an active interface

Figure 3.1 shows a typical architecture and the associated signals of active interface circuits for piezoelectric energy harvesting. The main features are shown in Figure 3.1 (a) and consisting in:

- An AC-DC converter that combines the rectifier with a set of switches and passive components (inductors or capacitors), involved in the PT voltage flip and power extraction operations (SSHI, SSHC,...).
- A PT voltage/current monitoring unit, usually composed of a comparator that detects the zero-crossing or the peak of the PT's current or voltage, respectively.
- A control bloc that drives the AC-DC converter switches.
- A voltage conditioning circuit that provides a stable power supply to the load and the rest of the interface circuit. In some cases, discussed later, it also maintains the optimal output voltage at which the maximum power can be extracted.

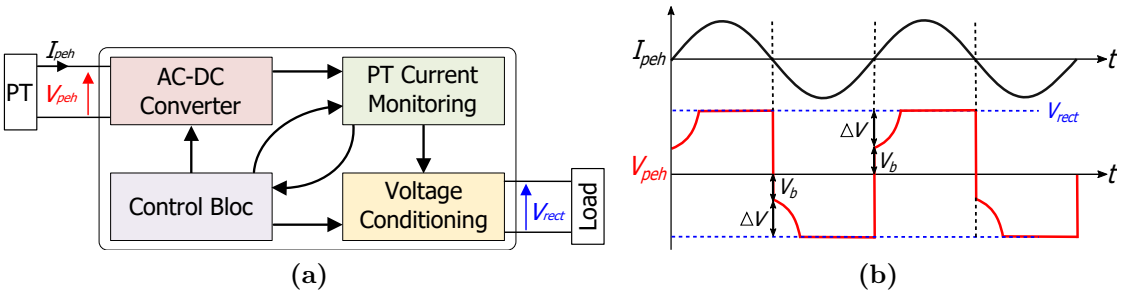


Figure 3.1.: (a) Typical active interface architecture, (b) Example of associated signals.

As shown in Figure 3.1 (b), V_b represents the value of the PT output voltage V_{peh} right after the voltage flip operation. Hence, ΔV, the voltage difference between V_{rect} and V_b, can be given as:

$$\Delta V = V_{rect} - V_b \tag{3.1}$$

The voltage flip efficiency can be expressed as:

$$\eta_F = \frac{2V_{rect} - \Delta V}{2V_{rect}} = \frac{V_{rect} + V_b}{2V_{rect}} \tag{3.2}$$

This parameter is a constant ($\eta_F < 1$). Its value depends on the active interface's architecture and on the value of the passive components used to implement it (inductor, damping capacitors, ON- resistance of the switches, etc.). For example, in Switch-Only interface circuit [25, 102], $V_b = 0V$, and the voltage flip efficiency $\eta_F = 0.5$.

3.3. Basic Full Active Rectifier (FAR)

In this section, a fully-integrated full active rectifier (FAR) is introduced where no inductor or capacitor is added to increase the voltage flip efficiency. The principle consists in discharging the PT parasitic C_{peh} at each I_{peh} zero-crossing moment and recharging it with a fraction of the charge of the storage capacitor C_L. The concept is based on the use of a high C_L value, i.e. at least one order of magnitude larger than C_{peh}, which is the case as C_L is a storage capacitance. The charge balance of FAR is very close to that in Switch-Only circuit. The FAR performance is then compared with the Switch-Only performance.

3.3.1. Basic FAR typology and operation principal

Figure 3.2 shows the circuit diagram of the basic FAR. It mainly consists of a set of analogue switches (SW_0 to SW_3), an active diode (AD) and a voltage regulator (VR). In order to perform the voltage flip operation across the PT, (SW_0 to SW_3) are driven by four non-overlapping pulse signals (Φ_0, Φ_K, Φ_P, Φ_N). These signals are synchronously generated in a specific order depending on the I_{peh} polarization. The AD is used for both preventing the current from flowing back from C_L when ($V_{sp} < V_{rect}$) and detecting the zero-crossing moment of I_{peh}. The VR is used to maintain the optimal value of the FAR output voltage in order to ensure the maximum power extraction from the PT.

Figure 3.3 shows the associated waveforms of FAR and switches control signals (left), in addition to the circuit's configurations according to both the switching sequence and I_{peh} phases (right). The FAR operation can be sub-divided into three phases:

1. Shorting phase (Φ_0): in this phase, SW_0 is turned on for a brief time $\tau_{\Phi 0}$ at each zero-crossing moment of I_{peh} to completely discharge C_{peh}. In the meantime, all other switches are turned off (Figure 3.3 (a)).
2. Sharing phase (Φ_K): this phase follows phase Φ_0. SW_3 is closed for a short time $\tau_{\Phi K}$, together with SW_1 or SW_2 depending on whether I_{peh} is positive or

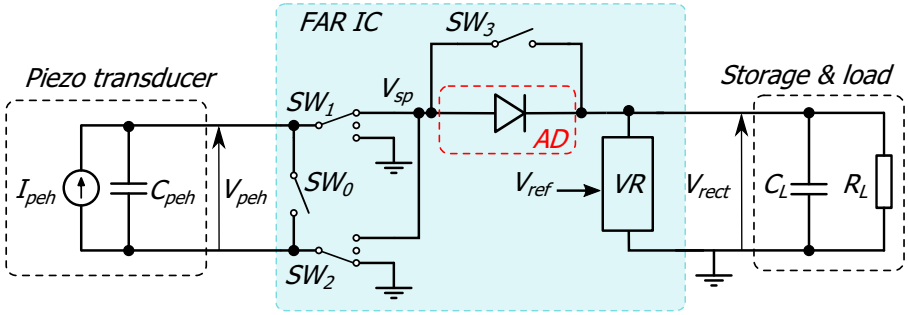


Figure 3.2.: Basic full active rectifier (FAR) interface circuit.

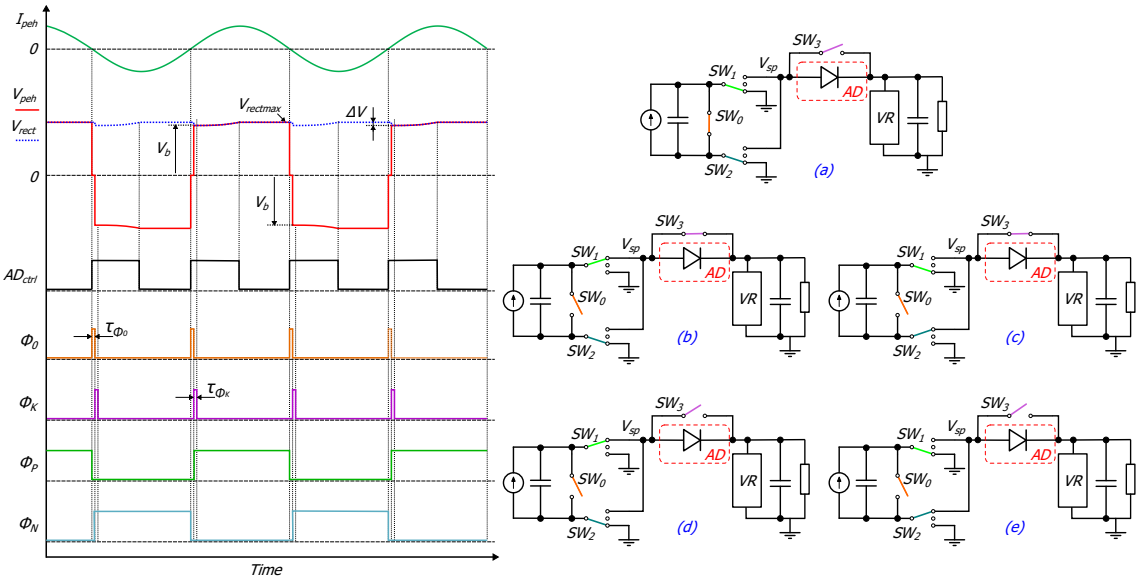


Figure 3.3.: (left) FAR waveforms and control signals, (right) circuit configurations : (a) shorting phase, (b) sharing phase with $I_{peh} > 0$, (c) sharing phase with $I_{peh} < 0$, (d) power extraction phase with $I_{peh} > 0$, (e) power extraction phase with $I_{peh} < 0$.

negative, respectively (Figure 3.3 (b) and (c)). This connects C_{peh} and C_L in parallel, and thus allows C_L to share its charges with C_{peh}. At the end of the sharing phase, the charge conservation equation can be expressed as:

$$Q_{rect} + Q_{peh} = V_b(C_L + C_{peh}) \tag{3.3}$$

where V_b denotes the final value of V_{peh} across C_{peh} (Figure 3.3). As the amount of charge in the C_{peh} after the shorting phase is $Q_{peh} = 0C$, V_b can be expressed as:

$$V_b = \frac{Q_{rect}}{C_L + C_{peh}} \tag{3.4}$$

Since C_L represents the storage capacitor in FAR, it is should have a large

value, i.e. at least one order of magnitude larger than C_{peh}. Thereby, V_b mainly depends on the charge Q_{rect} of C_L as demonstrated in equation (3.4), and its value continuously increases as C_L charges. In steady state, when C_L is completely charged, $\mid V_b \mid \backsimeq V_{rectmax}$ which is the value of V_{rect} right before the voltage flipping operation is started (Figure 3.3 (left)).

3. Power extraction phase (Φ_P, Φ_N): once C_{peh} is recharged, SW_3 is turned off while either SW_1 or SW_2 is kept on, depending on whether I_{peh} is positive (Φ_P) or negative (Φ_N), respectively (Figure 3.3 (d) and (e)). This corresponds to the rectifying operation of V_{peh}, since the node V_{sp} is connected to the positive terminal of the PT during the positive and the negative I_{peh} phases via SW_1 and SW_2, respectively. In this phase, C_{peh} and C_L are connected in parallel via the AD, which turns on when V_{peh} (now equals V_{sp}) is higher than V_{rect}. This actually happens shortly after the sharing phase Φ_K and thus, most of the charges delivered by the PT are transferred to C_L and R_L.

3.3.2. Charge loss and performance analysis

Assuming that the PT current is a sine wave expressed as:

$$I_{peh}(t) = \hat{I}_{peh} sin(2\pi f_{ex} t) \tag{3.5}$$

where $\hat{I}_{peh}$ is the PT current amplitude and f_{ex} is the excitation frequency.

The capacitive nature of PT makes I_{peh} and V_{peh} in phase quadrature, thus PT open circuit voltage V_{oc} can be expressed as:

$$V_{oc}(t) = \hat{V}_{oc} sin(2\pi f_{ex} t - \frac{\pi}{2}) = \frac{1}{C_{peh}} \int I_{peh}(t) dt \tag{3.6}$$

with $\hat{V}_{oc}$ the open-circuit amplitude of the PT's voltage mentioned before. The total charges available in half a period, i.e. during the $V_{oc}(t)$ evolution from $-\hat{V}_{oc}$ to $+\hat{V}_{oc}$, is given by:

$$Q_{tot} = 2C_{peh}\hat{V}_{oc} = \int_0^{1/2f_{ex}} I_{peh}(t) dt = \frac{2\hat{I}_{peh}}{\omega_0} \tag{3.7}$$

where $\omega_0 = 2\pi f_{ex}$.

In order to evaluate the FAR performance, the charge loss is studied in two cases, with and without load connected to its output. The FAR performance is then compared to the performance of the Switch-Only interface circuit [25]. In order to make the performance comparison more accurate, the FBR in the conventional Switch-Only circuit is replaced by an active rectifier (switches SW_1 and SW_2 in addition to an AD) used in FAR circuit. Figure 3.4 shows the modified architecture and the waveforms of the Switch-Only circuit.

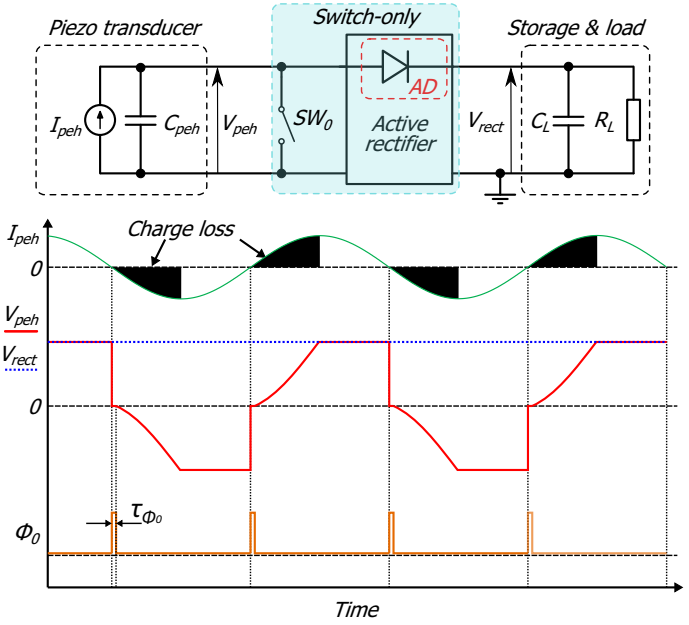


Figure 3.4.: Switch-Only interface circuit and associated waveforms and switch control signal.

- *Case 1: with no load connected to the FAR output (i.e. infinite R_L)*: in this case, the series resistances of the switches and AD can be neglected, and the total charge loss Q_{loss} includes two main contributions. The first is Q_1, which is the charge lost from C_L in recharging C_{peh} up to V_b during the sharing phase, and the second is Q_2, which is the charge lost to recharge C_{peh} from V_b to the maximum value of V_{rect} limited by VR ($V_{rectmax}$) during the power extraction phase, i.e. when C_{peh} and C_L are connected in parallel via the AD. In steady state, when V_{rect} has reached $V_{rectmax}$ (Figure 3.3), Q_1 and Q_2 are given by:

$$Q_1 = V_b C_{peh} = \Delta V C_L \tag{3.8}$$

$$Q_2 = (V_{rectmax} - V_b) C_{peh} = \Delta V C_{peh} \tag{3.9}$$

where ΔV is the voltage ripple of V_{rect} due to the recharging of C_{peh} (Figure 3.3). Hence, the total charge loss can expressed as:

$$Q_{loss} = C_{peh}(\Delta V + V_b) = C_{peh} V_{rect} \tag{3.10}$$

As mentioned before when $C_L \gg C_{peh}$, the voltage $\mid V_b \mid \backsimeq V_{rectmax}$, and thus $\Delta V \approx 0V$. Therefore, from (3.8) C_{peh} can be considered as fully recharged by C_L, and $Q_1 = V_b C_{peh}$ is the main charge loss (i.e. $Q_1 \approx Q_{loss}$). As a result,

the total charge that is actually stored on C_L in half a period is:

$$Q_{rect} = Q_{tot} - Q_{loss} = C_{peh}(2\hat{V}_{oc} - V_{rect}) \tag{3.11}$$

Thus, the total charge on a complete period is $2Q_{rect}$. The power delivered to the output is then expressed as:

$$P_{rect} = 2V_{rect}f_{ex}Q_{rect} = 2V_{rect}f_{ex}C_{peh}(2\hat{V}_{oc} - V_{rect}) \tag{3.12}$$

This equation shows that no power can be delivered when $V_{rect} = 0$ or $V_{rect} = 2V_{oc}$. In contrast, a maximum amount of power can be extracted when $V_{rect} = \hat{V}_{oc}$. This maximum power is given by:

$$P_{rectmax} = 2C_{peh}\hat{V}_{oc}^2 f_{ex} \tag{3.13}$$

This result suggests that VR should regulate V_{rect} to match $\hat{V}_{oc}$. Moreover, the maximum power extracted by FAR is identical to that which can be extracted by Switch-Only [25].

- *Case 2: with load connected to the FAR output (i.e. finite R_L)*: Figure 3.5 shows the equivalent electrical model of the PHS during the power extraction phase (i.e. AD is "ON"), when R_L has a finite value. As R_L is usually around several tens of kilo-ohms in the case of a wireless sensor load, the series resistances of the switches and AD can be neglected. In this phase,

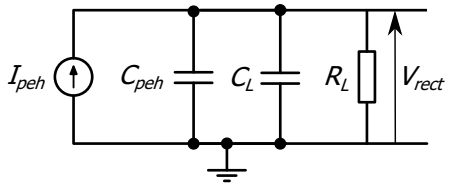


Figure 3.5.: Electrical model of PHS during power extraction phase.

when V_{rect} is lower than $\hat{V}_{oc}$, the expression of V_{rect} is given by:

$$V_{rect}(t) = Ke^{-\frac{t}{\tau}} + \frac{R_L\hat{I}_{peh}}{1+(\tau\omega)^2}sin(\omega t) - \frac{R_L\omega\tau\hat{I}_{peh}}{1+(\tau\omega)^2}cos(\omega t) \tag{3.14}$$

where $\tau = R_L(C_L + C_{peh})$ and K is the initial condition constant such as $V_{rect}(0) = V_b$, considering $t = 0$ corresponds to the zero-crossing moment of I_{peh}. Appendix A presents the complete analysis of the electrical model and the differential equations that leads to equation (3.14). When V_{rect} achieves $\hat{V}_{oc}$, it is regulated to that value by VR. Figure 3.6 (a) shows $V_{rect}(t)$ for the FAR architecture simulated on half a period of I_{peh} when applying a finite load R_L at $t = 0$. The parameters of PT are: $C_{peh} = 100nF$ and $I_{peh} = 62.8\mu A$, and the excitation frequency is $f_{ex} = 100Hz$. This corresponds to $\hat{V}_{oc} = 1V$. The load is $R_L = 48k\Omega$, $C_L = 100\mu F$ and K is set so that

$V_{rect}(0) = K - R_L\tau\omega\hat{I}_{peh}/(1+(\tau\omega)^2) = \hat{V}_{oc}C_L/(C_{peh}+C_L)$, which is the value of V_b when $V_{rect} = \hat{V}_{oc}$ at the zero-crossing moment of I_{peh}. In the Switch-Only

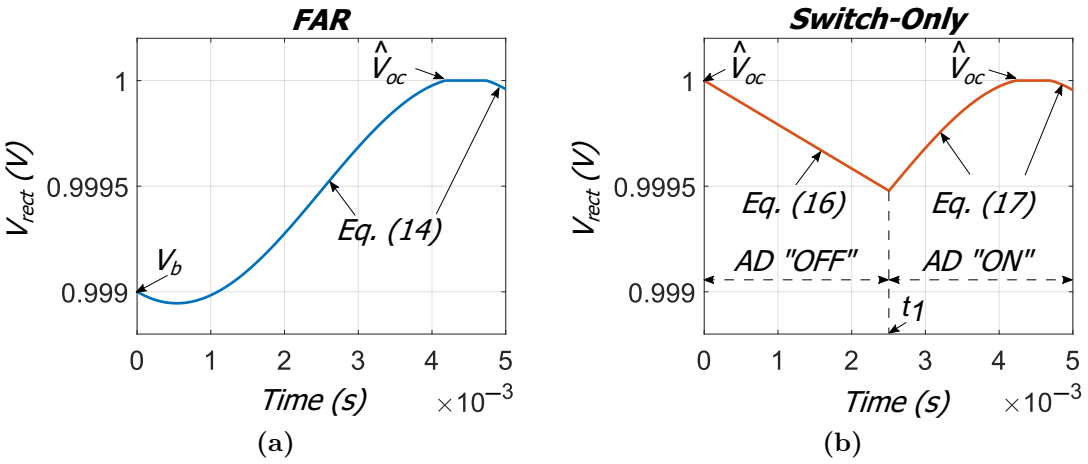


Figure 3.6.: Simulated evolution of $V_{rect}(t)$ on half a period if I_{peh}, (a) FAR, (b) Switch-Only. The parameters are: $C_{peh} = 100nF$, $C_L = 100\mu F$, $R_L = 48k\Omega$, $f_{ex} = 100Hz$, $I_{peh} = 62.8\mu A$.

circuit, the power extraction phase starts when the $V_{peh}(t) = V_{rectmax} = \hat{V}_{oc}$ (i.e. C_{peh} is completely recharged). Before this moment, the AD is OFF and C_{peh} recharges. Thus the expression of V_{peh} can be rewritten as:

$$V_{peh}(t) = \hat{V}_{oc} - \hat{V}_{oc}cos(\omega t) \tag{3.15}$$

At the same time C_L discharges in R_L. Hence, V_{rect} can be expressed as:

$$V_{rect}(t) = K_{SO}e^{-\frac{t}{R_L C_L}} \tag{3.16}$$

where K_{SO} is the initial value of V_{rect} at the zero-crossing moment of I_{peh} which corresponds to $\hat{V}_{oc}$ for Switch-Only circuit.
When C_{peh} is completely recharged, AD becomes ON to allow the charge transfer from PT to C_L. During this period, the equivalent circuit of Switch-Only circuit is the same as for FAR (Figure 3.5). Therefore, V_{rect} has the same expression as in (3.14) but with an V_{off} resulting from the decay of V_{rect} (3.16):

$$V_{rect}(t) = Ke^{-\frac{t}{\tau}} + \frac{R_L\hat{I}_{peh}}{1+(\tau\omega)^2}sin(\omega t) - \frac{R_L\omega\tau\hat{I}_{peh}}{1+(\tau\omega)^2}cos(\omega t) + V_{off} \tag{3.17}$$

Also, like in the FAR architecture, when V_{rect} reaches $\hat{V}_{oc}$, it is regulated by VR. Figure 3.6 (b) shows $V_{rect}(t)$ in the Switch-Only architecture simulated

with the same parameters as for the FAR simulation presented in Figure 3.6 (a).
To determine whether V_{off} is positive or negative, i.e. which circuit results the greater value, (3.14) or (3.17) (FAR or Switch-Only), the moment t_1 when V_{rect} of Switch-Only reaches V_{peh} should be found. This moment corresponds to the moment when AD turns "ON", such as:

$$K_{SO}e^{-\frac{t_1}{R_L C_L}} = \hat{V}_{oc} - \hat{V}_{oc}cos(\omega t_1) \tag{3.18}$$

As there is no analytic solution for this type of equations, a numerical method,

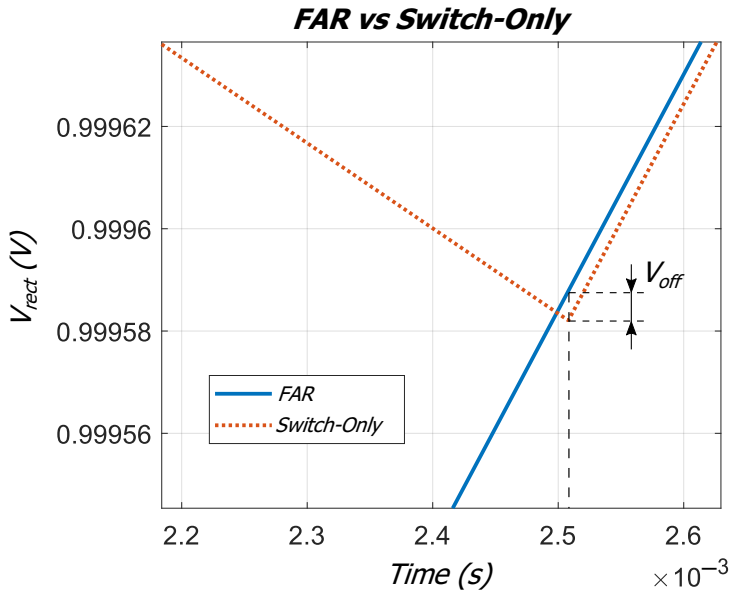


Figure 3.7.: Detail plot around $t = t_1$ of Figure 3.6 (a) and Figure 3.6 (b) superimposed.

such as Newton-Raphson [103] is applied in order to evaluate t_1. The value t_1 is then injected into (3.17) to determine V_{off} value such as equations (3.15), (3.16), and (3.17) yield the same value. Numerical simulations (Figure 3.7) show that, whatever the values of the parameters in (3.14) and (3.17), $V_{off} < 0$. This means that for $t \geq t_1$, $V_{rect-FAR} > V_{rect-Switch\_Only}$. This result has significant impact on the power efficiency of the systems when R_L changes. From (3.14), the limit value R_{Llim} of R_L for which $V_{rect-FAR}$ reaches $\hat{V}_{oc}$ at $t = T/2$, can be extracted. Applying R_{Llim} in (3.17) yields $V_{rect-Switch\_Only}(T/2) < \hat{V}_{oc}$. Since the value of $V_{rect}(T/2)$ sets the initial conditions of V_{rect} for the next half period of I_{peh}, it can be concluded that for $R_L = R_{Llim}$, the average value of $V_{rect-Switch\_Only}$ decreases to compensate for the presence of R_L while the average value of $V_{rect-FAR}$ remains constant. More generally, when $R_L < R_{Llim}$, V_{rect} decreases in both architectures but $V_{rect-Switch\_Only}$ decreases faster and stabilizes to a lower value than $V_{rect-FAR}$. Figure 3.8 shows the numerical sim-

ulations of both architectures with $R_L = 48k\Omega$ and the same initial conditions as above. The result shows that $V_{rect-Switch\_Only}$ stabilizes about $3mV$ below $V_{rect-FAR}$.
In terms of power, FAR is also more efficient than Switch-Only once V_{rect} has stabilized. Figure 3.9 shows the average power difference $\Delta P = P_{FAR} - P_{Switch-Only}$ between FAR and Switch-Only. It is interesting to note that

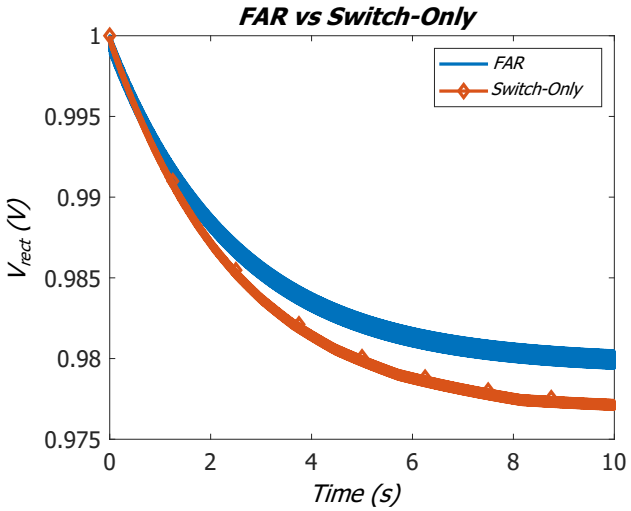


Figure 3.8.: Simulated evolution of V_{rect} in FAR and switch-only when $R_L = 48k\Omega$, with $1V$ initial condition.

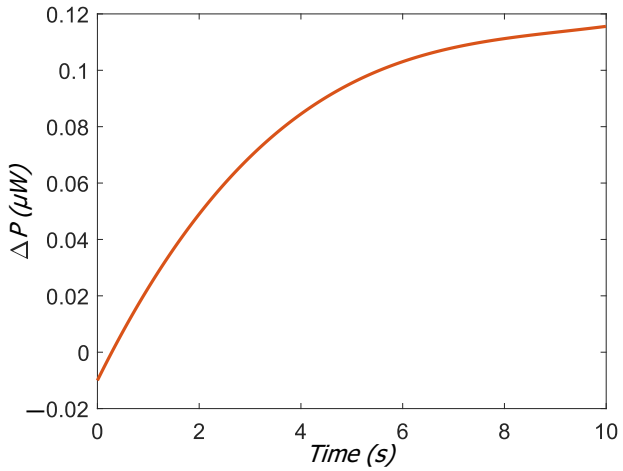


Figure 3.9.: Simulated evolution of average power difference ΔP between FAR and Switch-Only for $R_L = 48k\Omega$.

at $t = 0$, i.e. before and shortly after applying R_L, Switch-Only achieves a bit better power performance than FAR. This is due to the fact that without

R_L, the FAR concept results in lower average value of V_{rect}. Yet, energy harvesting systems are not intended to simply charge a storage device. They are inherently designed to provide energy to a load. Therefore, in addition to the voltage flip efficiency there is an advantage in using the FAR to enhance the power performance.

3.4. FAR with charge recycling circuity (FAR-CR)

Although the FAR circuit can achieve high voltage flip efficiency compared to the Switch-Only circuit, it can't extract more power than that extracted by the Switch-Only circuit except for certain load values. The principle is based on the reuse of a fraction of C_L. This amount of charge is considered a wasted charge according to (3.8).

As mentioned before, in a piezoelectric harvesting interface circuit, a proper voltage regulation is compulsory, first, to provide a stable supply voltage and over-voltage protection for both the output load and the interface circuit itself, and second, to ensure the maximum power extraction efficiency according to (3.13). Several techniques were implemented in literature for voltage regulation such as buck-boost, pulse frequency modulation, DC-DC conversion and others. [7, 8, 25, 32, 92, 96, 102, 104–107]. In the FAR circuit, in order to ensure efficient over-voltage protection excess charges are systemically sunk to ground. A question can be raised here; can we reuse this excess charges to improve FAR efficiencies?

In the following subsections, a novel architecture called FAR-CR is proposed. The principle of FAR-CR is based on the excess charge recycling in order to further boost the harvester's voltage flip and power efficiencies without wasting charge from C_L.

3.4.1. FAR-CR architecture and operating principle

Figure 3.10 shows the FAR-CR architecture. It consists of an active diode (AD), a set of switches SW_0 to SW_2 and a voltage regulator (VR). These components are the same as in the basic FAR circuit. In addition, a switch SW_{rcy} combined with a recycling capacitor C_{rcy} are added to the FAR-CR interface circuit. The concept is based on the use of the recycling capacitor C_{rcy} to store the excess charge that would otherwise be lost due to V_{rect} regulation. This stored charge is then reused to boost the synchronous voltage flip of V_{peh} thanks to SW_{rcy} switch.

Figure 3.11 shows the FAR-CR associated waveforms and switching control signals (left), in addition to the circuit's configurations according to switches and I_{peh} (right). As in FAR interface circuit, the I_{peh} zero-crossing moment is detected by the AD. This triggers the FAR-CR operation which takes also three switching phases. The first phase is the shorting phase (Φ_0) where the FAR-CR operation is similar to

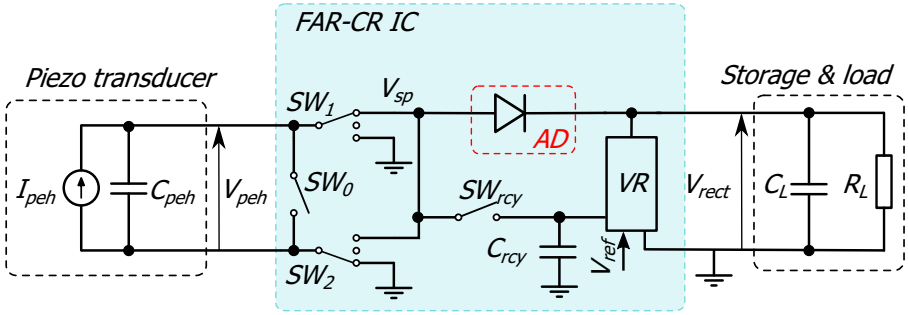


Figure 3.10.: FAR-CR interface circuit.

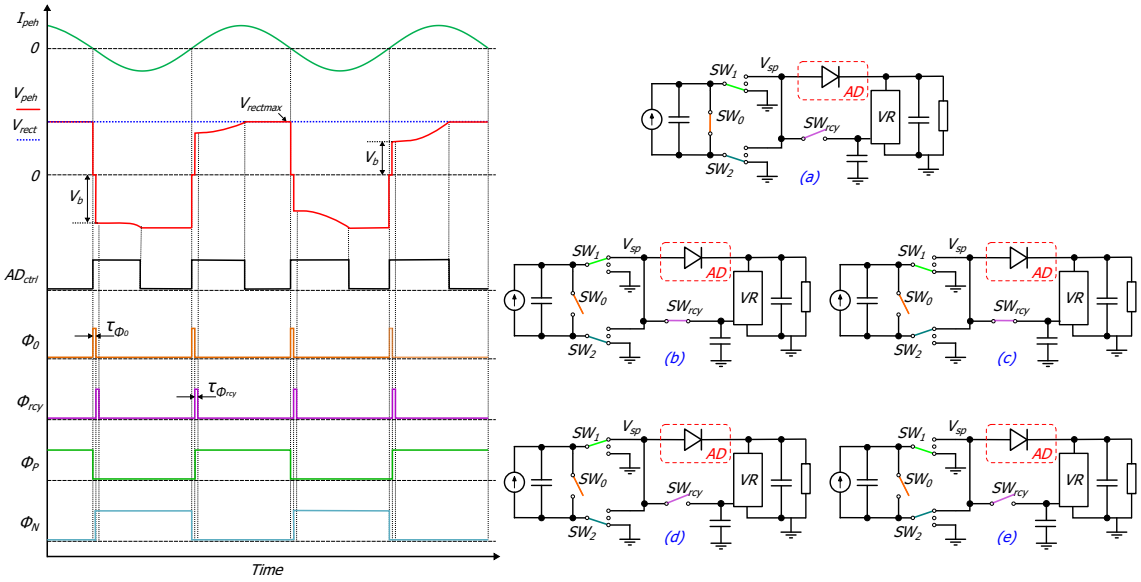


Figure 3.11.: (left) FAR-CR waveforms and control signals, (right) circuit configurations: (a) shorting phase, (b) recycling phase with $I_{peh} > 0$, (c) sharing phase with $I_{peh} < 0$, (d) energy harvesting with $I_{peh} > 0$, (e) energy harvesting with $I_{peh} < 0$.

the basic FAR operation in the shorting phase (Φ_0). At the end of this phase, C_{peh} is completely discharged (Figure 3.11 (a)). The second phase is the recycling phase (Φ_{rcy}), which immediately follows the discharging of C_{peh}. Unlike the basic FAR operation in the sharing phase, where a charge transfer from C_L to C_{peh} is allowed via SW_3, the FAR-CR performs a charge transfer from C_{rcy} back to C_{peh} by closing SW_{rcy} for a brief time $\tau_{\Phi rcy}$. Meanwhile, depending on whether I_{peh} is positive or negative, either SW_1 or SW_2 is closed, respectively (Figure 3.11 (b) and (c)). This also corresponds to the rectifying operation of V_{peh}. Finally, the third phase is the power extraction phase, when SW_{rcy} is switched off while either SW_1 or SW_2 is kept on, once C_{peh} is recharged. At this point, V_{sp} and V_b are equal (Figure 3.11 (left)) and can be expressed as $V_{sp} = V_b = \frac{Q_{rcy}}{C_{rcy}+C_{peh}}$. Hence, a maximal V_b can be achieved when $C_{rcy} \gg C_{peh}$. Therefore, C_{rcy} should be chosen to be at least one order of magnitude larger than C_{peh}. In order to turn the AD on, C_{peh} needs to recharge so

that V_{sp} reaches V_{rect} (Figure 3.11). Energy harvesting eventually starts once this condition is satisfied (Figure 3.11 (d) and (e)).

3.4.2. Considerations on optimal operation

In order to determine the optimal operating condition, i.e. the optimal value of V_{rect} at which maximum power can be extracted from the PT, the charge balance once the voltage flip has occurred should be studied. After the shorting phase, C_{peh} is completely discharged and then partially recharged by C_{rcy} during the recycling phase. After this phase, $V_{sp} = V_b$. Before the PT can deliver power to the output, a part of the charge generated by the PT goes into C_{peh} to recharge it from V_b to V_{rect}. This amount of charge is considered as wasted charge. In steady state, i.e. when V_{rect} is constant, the wasted charge remains constant and equal to:

$$Q_{loss} = \Delta V C_{peh} = (V_{rect} - V_b)C_{peh} \tag{3.19}$$

Therefore, the charge that is actually delivered to the output in a half period can be given as:

$$Q_{rect} = Q_{tot} - Q_{loss} = C_{peh}\left(2\hat{V}_{oc} - (V_{rect} - V_b)\right) \tag{3.20}$$

Hence, from (3.2) and (3.20), the expression of the steady-state output power can be deduced:

$$P_{rect} = 4C_{peh}f_{ex}\left(\hat{V}_{oc} - (1-\eta_F)V_{rect}\right)V_{rect} \tag{3.21}$$

The derivative of (3.21) shows that maximum output power is achieved when:

$$V_{rect} = \frac{\hat{V}_{oc}}{2(1-\eta_F)} \tag{3.22}$$

As a consequence, from (3.21) and (3.22) the maximum power extracted by FAR-CR can be written as:

$$P_{rectmax} = C_{peh}f_{ex}\frac{\hat{V}_{oc}^2}{1-\eta_F} \tag{3.23}$$

Unlike SSHI or SSHC, FAR-CR does not reuse C_{peh}'s own charge to boost the power and voltage efficiencies. The voltage flip efficiency η_F is related to the amount of charge stored in C_{rcy} which fluctuates, depending on how much excess charge is available. The worst operating condition occurs when C_{rcy} is fully discharged. In this case, FAR-CR is equivalent to the Switch-Only configuration and the voltage flip efficiency is $\eta_F = 0.5$ [104], [99]. In all other cases, i.e. when $V_{rcy} > 0$, η_F

value will be greater than 0.5 which helps in voltage flipping and then boosts the charge extraction efficiency. This boost occurs as long as C_{rcy} has some charge. Furthermore, this also helps slowing down the discharging of C_L, when the load drains current from it.

3.5. Circuit implementation of FAR/FAR-CR

Figure 3.12 shows the system architecture of FAR/FAR-CR interface circuit. This system is designed in AMS 0.35μm HV CMOS technology. Its allows to implement FAR, FAR-CR and Switch-Only operation modes for performance comparison purpose. In addition to the AD and the VR blocks mentioned in sections 3.3 and 3.4, a control block (CTRL), a ring oscillator (RO), a switch drivers (SD) and an another voltage regulator (VR12) blocks are also on-chip implemented to generate all control signals (AD_{ctrl}, Φ_0, Φ_K/Φ_{rcy}, Φ_P, Φ_N).

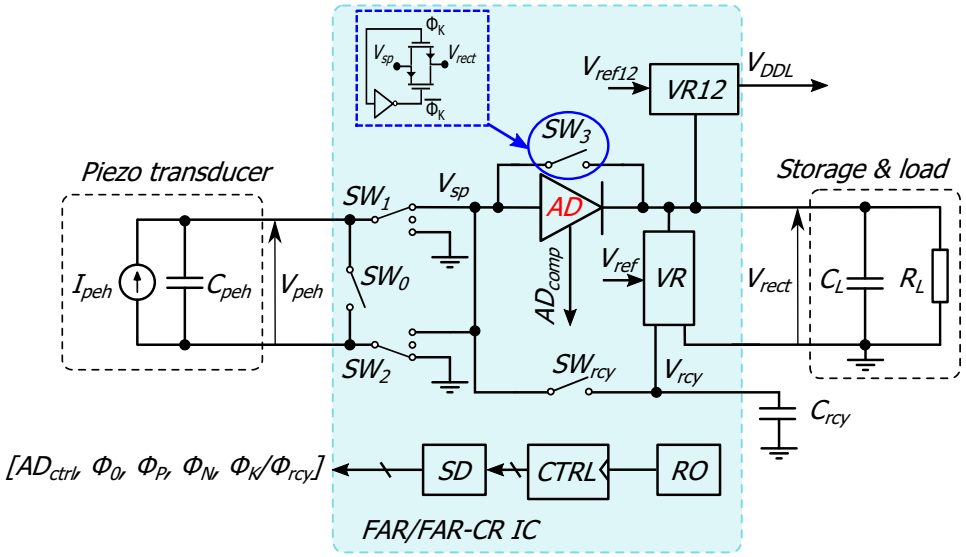


Figure 3.12.: FAR system architecture combining the basic FAR and the FAR-CR circuits.

At each I_{peh} zero-crossing moment detected by the AD, a signal AD_{comp} triggers the signal sequence generation in the CTRL. Hence, the CRTL clocked by the RO generates the control signals of the AD and the switches SW_0 to SW_3. The voltage regulator (VR12) is used to provide a low stable power supply $V_{DDL} = 1.2V$ mainly for CRTL and RO. In order to fully turn on/off the switches, its control signals are shifted to higher voltage level, $V_{DDH} = 3.3V$, using the SD block. This system is over-voltage protected thanks to the VR block. The internal transistor-level architecture of each block of FAR/FAR-CR system and its operation are detailed below.

3.5.1. Active diode (AD)

Figure 3.13 (a) shows the AD circuit. It consists of a PMOS switch and a continuous time comparator employed in [6]. When $V_{rect} > V_{sp}$, the comparator output (AD_{comp}) goes high, and thus opens the PMOS switch preventing the current backflow from C_L to C_{peh}. This moment also corresponds to the moment when I_{peh} changes direction, i.e. corresponds to zero crossing. Therefore, the signal AD_{comp} is used to trigger the generation of the signals sequence delivered by CRTL which is needed to control the switches. A combinatorial OR of the control signals (Φ_0, Φ_K/Φ_{rcy}) and AD_{comp}, generated by the CRTL, is used as a control signal AD_{ctrl} of the PMOS switch. This ensures that this switch remains off throughout the C_{peh} discharging and recharging process, and thus avoids spurious behavior of the AD as will be explained in section 3.6.

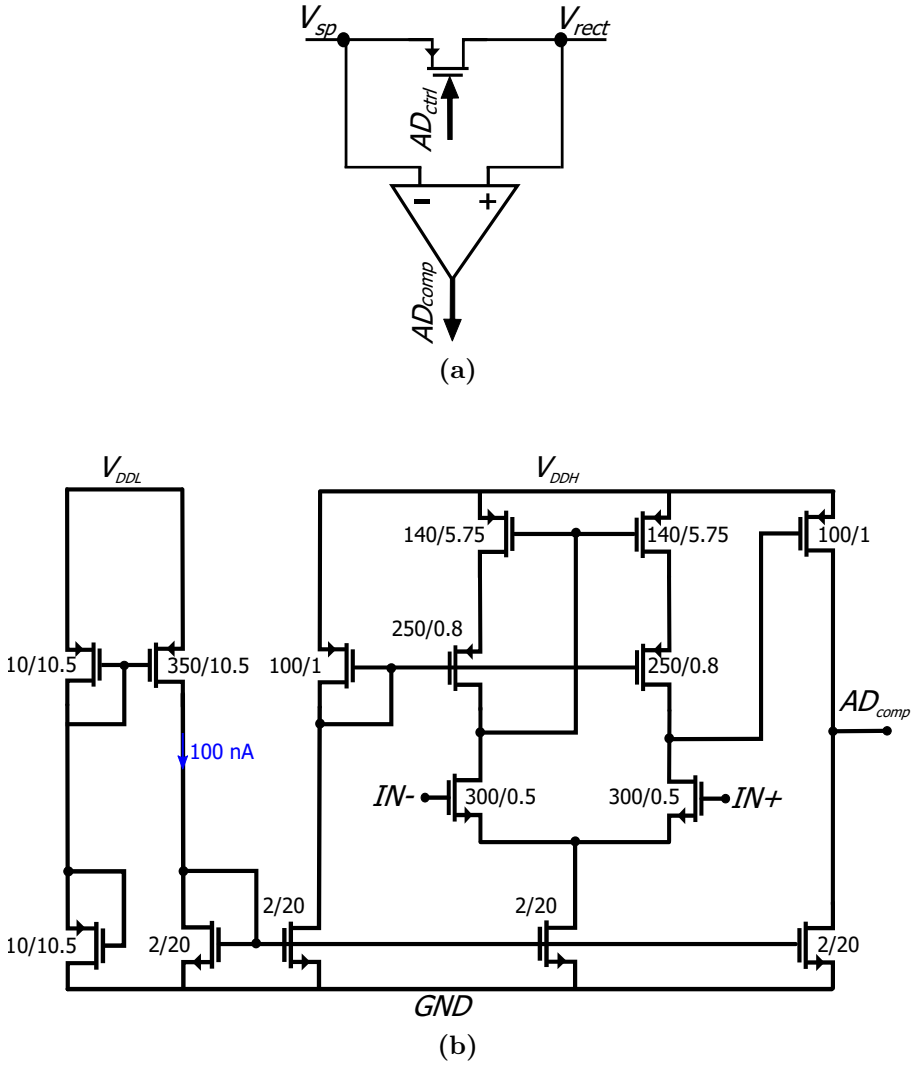


Figure 3.13.: (a) Active diode diagram block (AD), (b) AD comparator architecture [6].

In order to decrease the power consumption resulted from the PMOS switch, the latter should has a low ON-resistance current path, i.e. low R_{ds}. This can be achieved by increasing its transistor channel width. However, increasing the PMOS width leads to increase its gate to source capacitance, i.e. C_{gs} capacitance, which in turn increases its control time and thus its power consumption. Therefore, a trade-off between the R_{ds} and the PMOS gate to source capacitance is made to determine the optimal width of the PMOS switch. Figure 3.13 (b) shows the circuit diagram of the continuous time comparator. A $100nA$ biasing current is set to balance the power consumption and the performance of this comparator. With this current, the comparator has a gain of $70K$, a negative offset of $-220\mu V$and a power consumption around $965nW$.

3.5.2. Control (CRTL) and ring oscillator (RO) blocks

Figure 3.14 shows the architecture of the control block. As explained before, the zero-crossing of I_{peh} causes the AD's comparator output signal AD_{comp} to go high. This signal is used to trigger the generation of the signal sequence delivered by CRTL, which is needed to control the AD and the switches SW_0 to SW_2 in addition to SW_3 in FAR operation mode or switch SW_{rcy} in FAR-CR operation mode.

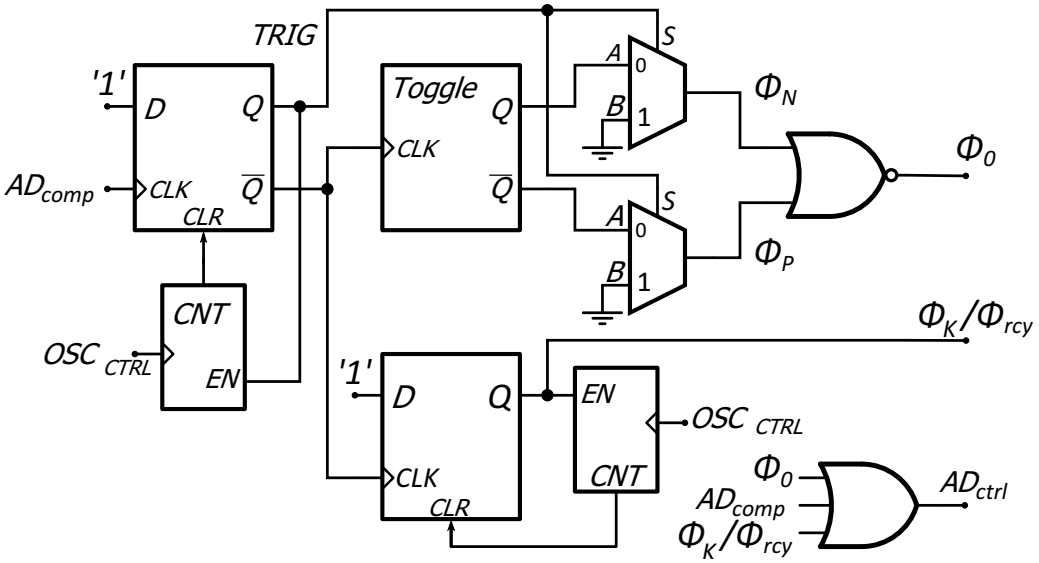


Figure 3.14.: Control block (CRTL) architecture.

Table 3.1 shows the employed switches with their corresponding control signals in both FAR and FAR-CR typologies.

Table 3.1.: Employed switches and corresponding control signals.

Typology	Switch	Control signal
FAR/FAR-CR	AD PMOS switch	AD_{ctrl}
	SW_0	Φ_0
	SW_1	Φ_P
	SW_2	Φ_N
FAR	SW_3	Φ_K
FAR-CR	SW_{rcy}	Φ_{rcy}

Figure 3.15 shows the timing diagram of the control signals sequence generated by the control block for FAR and FAR-CR operation modes. At each I_{peh} zero-crossing

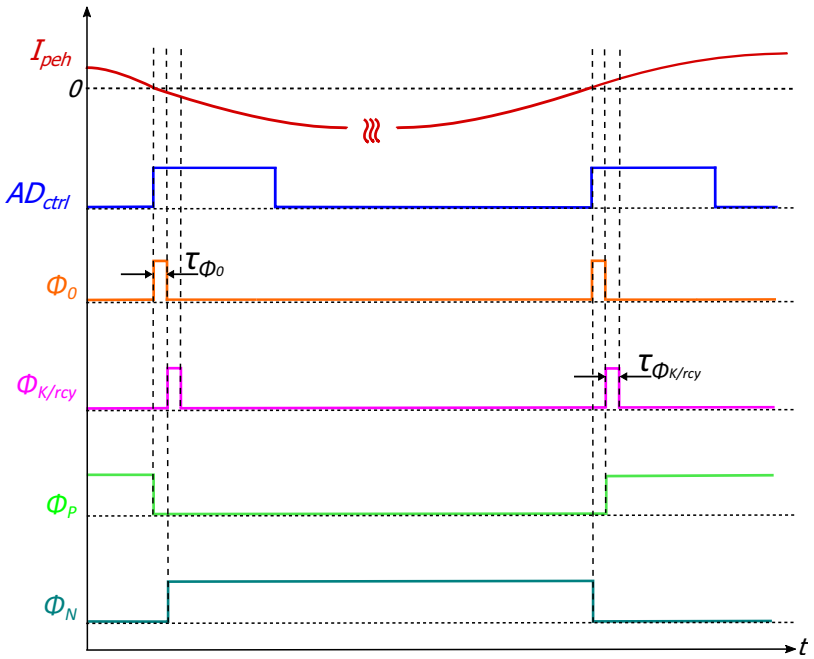


Figure 3.15.: Timing diagram of the control signals sequence generated by CRTL for FAR and FAR-CR typologies

moment, signal AD_{comp} is used as the clock signal of a D flip-flop whose data input is set to a constant logic high state (Figure 3.14). When AD_{comp} goes high, a trigger signal $TRIG$ simultaneously turns on signals Φ_P and Φ_N, which disconnects SW_1 and SW_2 from node V_{sp} and the ground. In the meantime, signal Φ_0 turns on SW_0 (Figure 3.15), which shorts C_{peh}. Signal $TRIG$ remains high until C_{peh} is discharged. The duration of the shorting phase $\tau_{\Phi 0}$ depends on the value of C_{peh} and the resistance of SW_0. The TGs used to implement the switches as shown in Figure 3.12 are designed to have very low ON-resistance around 15Ω. Assuming $C_{peh} = 100nF$, based on the off-the-shelf device (S118-J12S-1808YB by Piezo.com) used in the experiments (section 3.7), the corresponding RC time constant is thus

1.5µs. The duration $\tau_{\Phi 0}$ is controlled by means of a counter clocked by the RO signal OSC_{CTRL}. This signal has a frequency of $125kHz$, which allows controlling $\tau_{\Phi 0}$ with 8µs accuracy. In the proposed system, a modulo 4 counter is used as a timer to control the duration of Φ_0, which thus yields $\tau_{\Phi 0} = 32\mu s$. This duration is largely sufficient to ensure complete discharging of C_{peh}. Once $TRIG$ is reset, i.e. $\overline{TRIG}$ goes high, a toggle sets either Φ_P or Φ_N to high depending on whether I_{peh} is positive or negative, respectively. When Φ_P is high, SW_1 is connected to node V_{sp} and SW_2 is connected to the ground, and inversely when Φ_N is high. In the meantime, Φ_K/Φ_{rcy} goes high, which closes SW_3/SW_{rcy} and causes C_L/C_{rcy} to share its charge with C_{peh} during this sharing phase. In this phase SW_3/SW_{rcy} is in series with either SW_1 or SW_2. Since all switches are implemented with the same TGs, the RC time constant is thus 3µs. Therefore, a modulo 4 counter (Figure 3.14) is used to set the duration of the sharing phase $\tau_{\Phi K/\Phi rcy} = 32\mu s$, which is also sufficient to complete the charge transfer. Once C_{peh} is recharged, SW_3/SW_{rcy} is turned off while either SW_1 or SW_2 is kept on, depending on whether I_{peh} is positive (Φ_P high) or negative (Φ_N high), respectively (Figure 3.15). This corresponds to the rectifying operation of V_{peh} since the terminals of the PT are inverted by SW_1 and SW_2 at each reversal of I_{peh}.

In order to generate the clock signal of the control block, a ring oscillator proposed in [73] is re-designed to output a clock signal OSC with frequency of $250kHz$. This signal will be used as a clock signal for a charge pump (CP) used in another implementation in the next chapter. A frequency divider is used then to generate signal OSC_{CTRL} required to clock the counters in CRTL. In addition, for experimental test requirements, an EN input is added to enable or disable the ring oscillator. The power consumption is estimated to be around $60nW$.

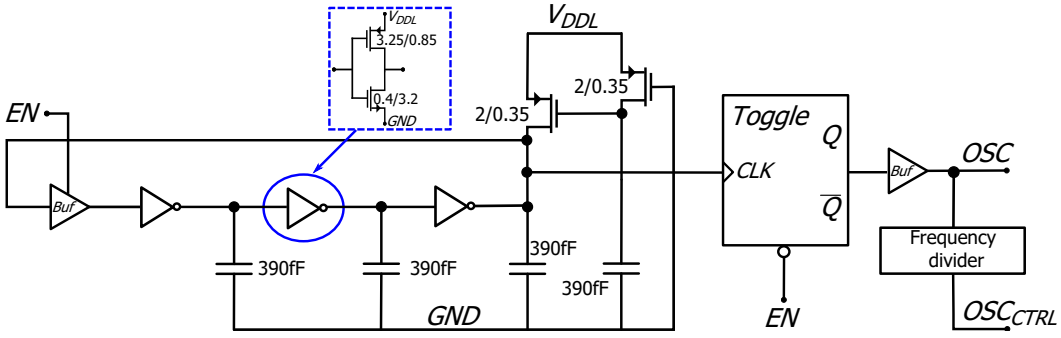


Figure 3.16.: Ring oscillator (RO) circuit architecture.

3.5.3. Switch drivers (SD)

This block is used to ensure that the employed switches are fully turned ON or OFF. As show in Figure 3.17, it consists of five level-up shifters (LS)s. In this implementation, GND (i.e. $0V$) for $'0'$ logic level and $V_{DDH} = 3.3V$ for $'1'$ logic

level are chosen to drive the switches. Thereby, level-up shifters (Figure 3.17) are implemented to shift V_{DDL} voltage level up to V_{DDH}, where $V_{DDL} = 1.2V$ provided by the voltage regulator (VR12). To explain why the level-up shifter is mandatory in FAR/FAR-CR circuits, the switch SW_1, consisting of two TGs, is studied as an example.

Lets consider the phase where V_{peh} needs to be rectified in FAR operation mode. During the positive phase of I_{peh} , SW_1 must simultaneously connect the positive terminal of the PT (i.e. V_p) to the node V_{sp} via TG_1 (i.e TG_1 is ON) and disconnect it from GND (i.e TG_2 is OFF).

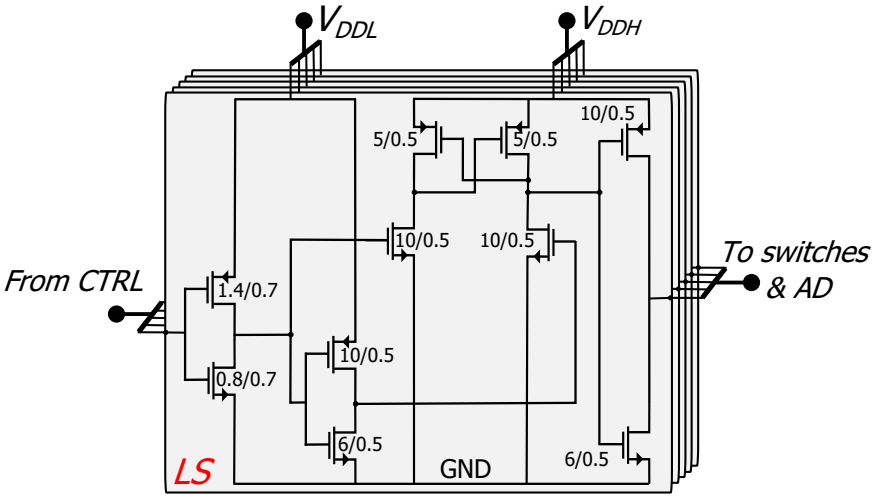


Figure 3.17.: Switch drivers block (SD) consisting of five level-up shifters (LS) [7].

Figure 3.18 shows the SW_1 configuration and the corresponding equivalent circuit when I_{peh} positive.

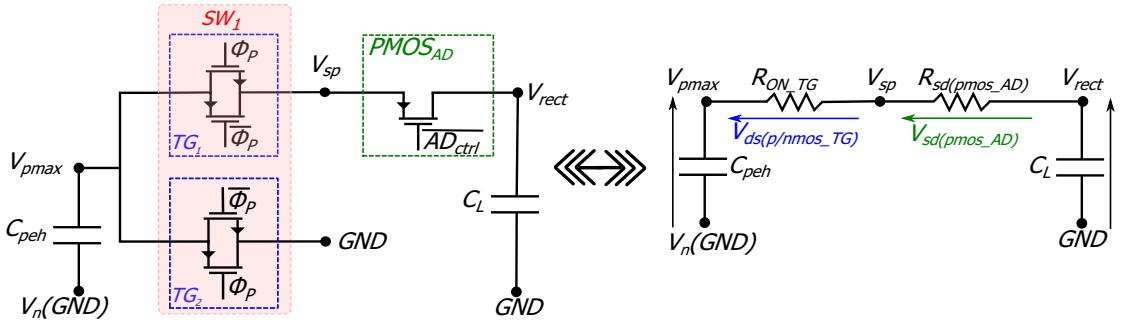


Figure 3.18.: (left) SW_1 configuration: TG_1 (ON) and TG_2 (OFF), and (right) corresponding equivalent circuit when I_{peh} is positive.

The voltages V_p/V_n fluctuate between GND and V_{pmax}, which is the maximum voltage that can be reached in this configuration. As shown in Figure 3.18 (right),

V_{pmax} can be expressed as:

$$V_{pmax} = V_{ds(p/nmos-TG)} + V_{sd(pmos-AD)} + V_{rect} \tag{3.24}$$

where $V_{ds(p/nmos-TG)}$ is the voltage drop across TG_1 when it is ON, and $V_{ds(pmos-AD)}$ the voltage drop across the AD PMOS switch when it is turned on. In this implementation, the low ON-resistance of TG_1, i.e. $R_{ON-TG} \simeq 15\Omega$, results in a low voltage drop $V_{ds(p/nmos-TG)}$ of $14mV$ across it. Also, the PMOS switch of the AD is designed to have a low V_{ds} of $-12mV$. Hence, in steady state, when V_{rect} is constant and regulated to $1V$, V_p/V_n fluctuates between $0V$ and $1.026V$ according to 3.24. In order to turn NMOS and PMOS on, i.e. to create a conducting channel between the drain and the source terminals, the following conditions must be satisfied, respectively:

$$V_{gs} > V_{thn} \tag{3.25}$$

and

$$V_{gs} < V_{thp} \tag{3.26}$$

where V_{gs} is the gate-source voltage, V_{thn} and V_{thp} denote the threshold voltages of NMOS and PMOS transistors, respectively. The NMOS and PMOS transistors in this technology, i.e. AMS $0.35\mu m$ HV CMOS, have a V_{thn} and V_{thp} of $560mV$ and $-750mV$, respectively. To fully turn off TG_2, both NMOS and PMOS transistors should be fully turned off. As SW_1 control signal (Φ_P) is a digital signal, its low and high voltage levels are GND and $V_{DDL} = 1.2V$, respectively. For these voltage levels, the NMOS is fully turned OFF, whereas for $V_p > 1.95V$, the PMOS is conducting and V_p is connected to the GND. This leads to the discharge of the C_{peh} through the ground. In the case of TG_1, turning on this switch implies that both transistors NMOS and PMOS should be fully turned on. When $V_p = V_{pmax} = 1.026V$, the source voltage of the NMOS in TG_1 is given as:

$$V_{snmos-TG1} = V_{pmax} - V_{ds(nmos-TG1)} = 1.012V \tag{3.27}$$

As a result, $V_{gsnmos-TG1} = 1.2 - 1.012 = 0.188V$, which is lower than the threshold voltage of this transistor, i.e. $450mV$. Therefore, this transistor is OFF, which prevents the charge extraction from the PT and impacts the system efficiency. This example shows that to fully turn on/off switches, the gate driving voltage of these switches should cover the voltage ranges switches nodes. To fulfill this condition, all control signals generated by CRTL should be shifted up by LSs from $1.2V$ to $3.3V$ before using it to drive switches. The choice of GND and $3.3V$ to drive switches also takes into account the maximum allowed voltages for the selected low-voltage transistors in the used technology, i.e. AMS $0.35\mu m$ HV CMOS technology. The absolute maximum allowed V_{gs} and V_{ds} for these transistors are $3.6V$ and the breakdown voltage is $5V$. Therefore, choosing $0V$and $3.3V$ voltage levels makes the

maximum voltage difference $3.3V$, which ensures the safe operation of all transistors. The power consumption depends on the gate capacitance of the driven switch and on the frequency of LS input. In this implementation, the frequency of all generated control signal is $200Hz$. With this frequency, the simulated power consumption of one LS is only $7.525nW$.

3.5.4. Voltage regulator blocks

Two voltage regulators are implemented in this circuit, the first one (VR) is to ensure the maximum power extraction (Figure 3.19 (a)) and the second one (VR12) is to provide the low power supply voltage V_{DDL} mainly to CTRL, RO and LSs blocks (Figure 3.19 (b)). When $V_{DDL} < 1.2V$ and $V_{rect} < 1V$, the transistor $M3$ is turned

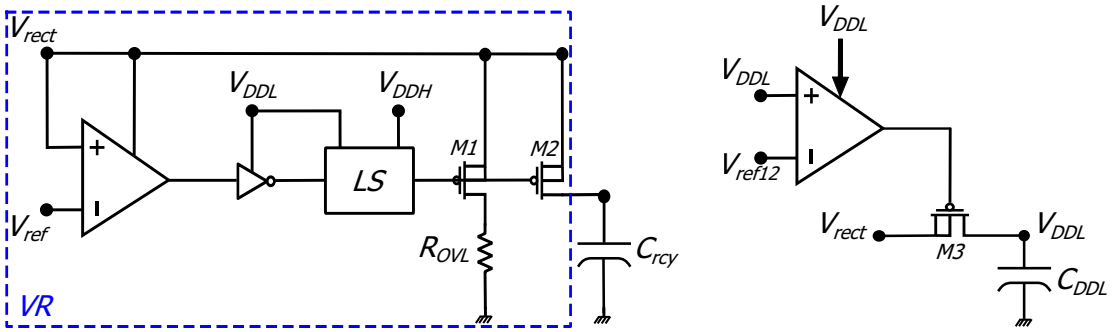


Figure 3.19.: (a) Circuit diagram of the voltage regulator VR, (b) Circuit diagram of the voltage regulator VR12.

on to charge C_{DDL} while the transistors $M1$ and $M2$ in VR block are turned off. When the voltage across C_{DDL} reaches $1.2V$, $M3$ is turned off while $M1$ and $M2$ are kept OFF until V_{rect} reaches $1V$. At this moment, $M1$ and $M2$ are turned on to get rid of the excess charge through the ground via a resistor R_{OVL} in FAR or to store it in to the recycling capacitor C_{rcy} in FAR-CR. A low power common-gate comparator proposed in [8] (Figure 3.20) is used in both VR and VR12 regulators. Unlike the comparator used in AD, this comparator doesn't need a high power supply voltage to start the comparation activity. It is self-supplied by its positive input. This allows this comparator to work when its positive input voltage reaches the threshold voltage of the PMOS transistor ($\sim 750mV$). This also significantly reduces the power consumption down to $485nW$. The resistor R_{OVL} is also used in FAR-CR to protect the circuit from the over load voltages when C_{rcy} is completely charged. In addition, in order to fully turn off $M1$ and $M2$ in VR, a LS is used to drive these transistors.

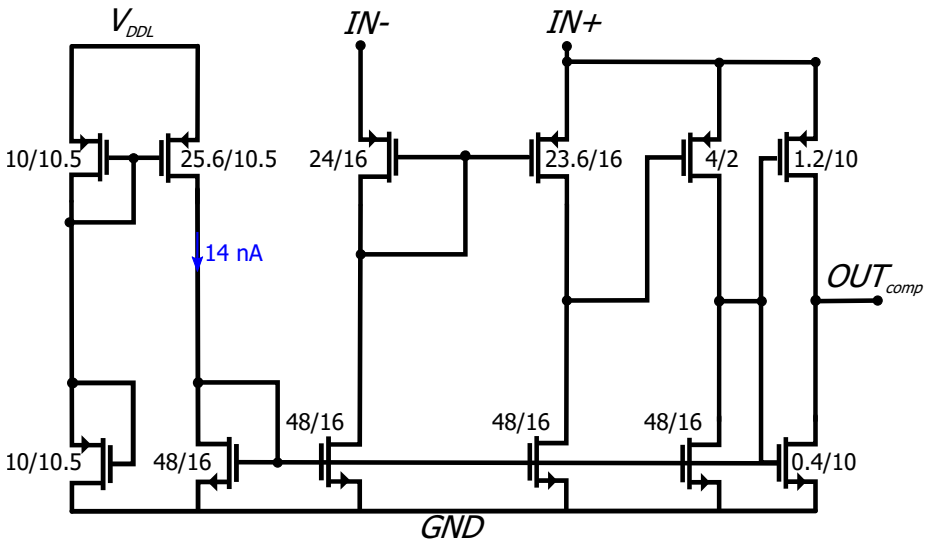


Figure 3.20.: Common-gate comparator circuit [8].

3.6. Transistor-level simulation results

Both FAR and FAR-CR circuits are designed in AMS $0.35\mu m$ HV CMOS technology. Transistor-level simulations were performed using Cadence®. The model of PT is based on the parameters of the commercial device S118-J12S-1808YB by Piezo.com, which will be used in experiments. The C_{peh} capacitance value is $100nF$ while I_{peh} and f_{ex} are set to achieve an open-circuit voltage $\hat{V}_{oc} = 1V$. This corresponds to $\hat{I}_{peh} = 62.8\mu A$ and $f_{ex} = 100Hz$, according to (3.6). The storage capacitor $C_L = 10\mu F$ is pre-charged to $0.7V$, which is sufficient to activate the FAR or the FAR-CR. Figure 3.21 shows the simulation results of FAR circuit. When V_{rect} is regulated to $\hat{V}_{oc}$, V_b value becomes around $0.99V$ ($\Delta V = 10mV$), which corresponds to 99% voltage flip efficiency.

Figure 3.22 shows the voltage flip sequence after the zero-crossing of I_{peh} together with signals AD_{comp} and AD_{ctrl} in FAR circuit. The voltage flip operation takes $64\mu s$. Simulation results also show that the AD's output signal AD_{comp} returns to low level after the voltage flip operation has started. This is due to the charge injection at node V_{sp} (Figure 3.12) when switches SW_1 and SW_2 open. For this reason, as mentioned in section 3.5, to prevent the spurious behavior of the AD comparator, signal AD_{ctrl} is locked by the combinatorial OR function of AD_{comp}, Φ_0 and Φ_K. During the sharing phase, signal AD_{comp} goes high again as C_{peh} recharges, and returns to low level shortly after this phase is completed, as $|V_{peh}| = V_{sp}$ increases and power extraction starts.

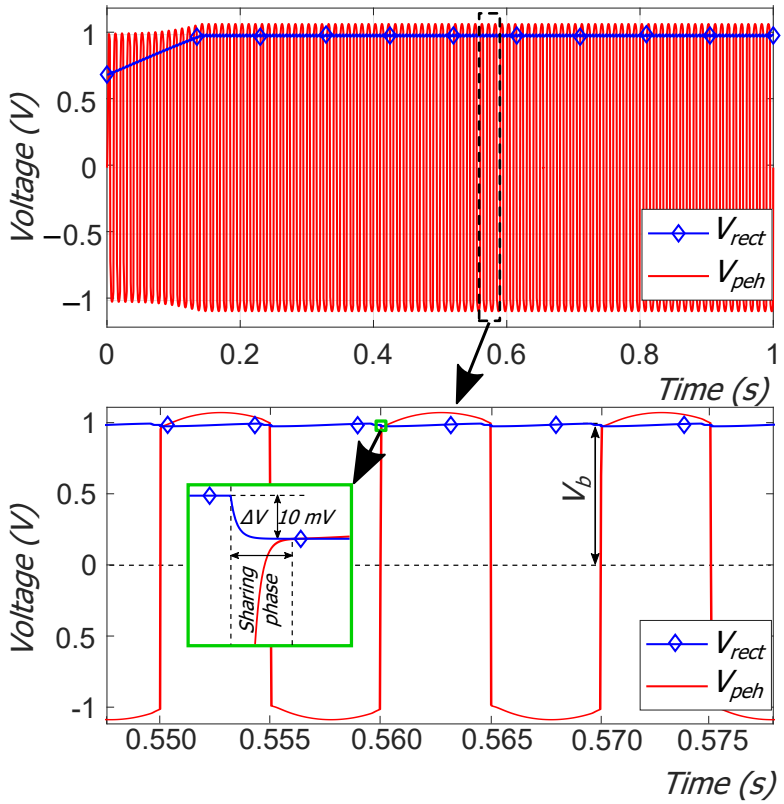


Figure 3.21.: Simulated V_{peh} and V_{rect} when using $C_L = 10\mu F$, pre-charged to $0.7V$ in FAR circuit.

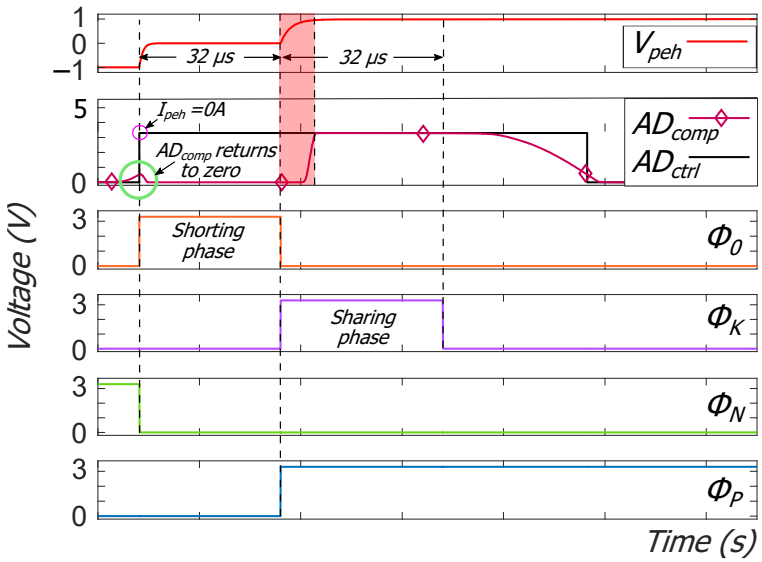


Figure 3.22.: Simulated V_{peh}, AD_{ctrl}, AD_{comp} and voltage flip sequence of FAR with $C_L = 10\mu F$. As can be noticed, AD_{comp} returns to low shortly after the zero-crossing of I_{peh}.

The FAR-CR circuit is also simulated with the same PT and C_L parameters used in FAR simulations and a capacitor $C_{rcy} = 1\mu F$ and pre-charged to $V_{rcy} = 0.98V$. Figure 3.23 shows the simulated V_{peh}, V_{rect} and V_{rcy} of the FAR-CR. For this circuit, V_{rect} regulation is achieved by charging C_{rcy} (green zoom view). The stored charge in C_{rcy} is then reused to flip the voltage across PT (pink zoom view). Therefore, V_b value fluctuates and depends on the voltage V_{rcy} across C_{rcy} (Figure 3.23).

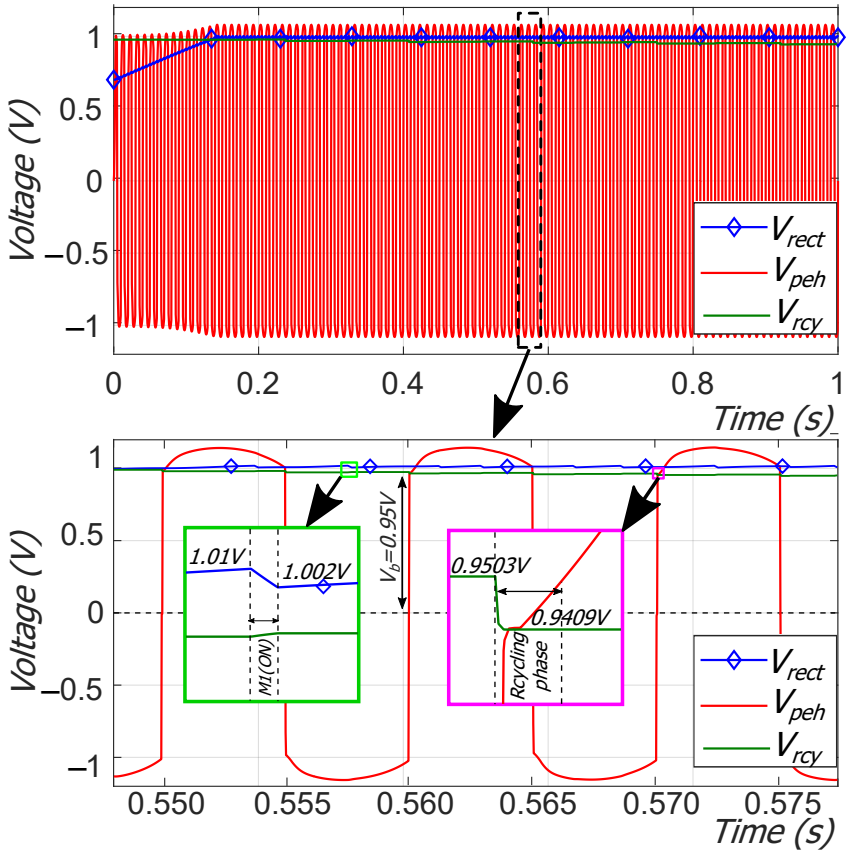


Figure 3.23.: Simulated V_{peh}, V_{rect} and V_{rcy} when using $C_{cry} = 1\mu F$, pre-charged to $0.98V$ in FAR-CR circuit.

The voltage flip sequence and AD_{comp}, AD_{ctrl} signals are also shown in Figure 3.24 for the FAR-CR circuit. As in the FAR circuit, the voltage flip operation also takes $64\mu s$. Also to overcome the charge injection at node V_{sp}, the combinatorial OR function of AD_{comp}, Φ_0 and Φ_{rcy} locks AD_{ctrl} signal. When C_{peh} is recharged during the recycling phase, signal AD_{comp} goes high again. As $C_{rcy} < C_L$, the recharging time of C_{peh} in FAR-CR (see shaded zone of V_{peh} in Figure 3.24) is less than in FAR (see shaded zone of V_{peh} in Figure 3.22). After the recycling phase, when C_{peh} is completely recharged, signal AD_{comp} returns to low level and energy extraction starts.

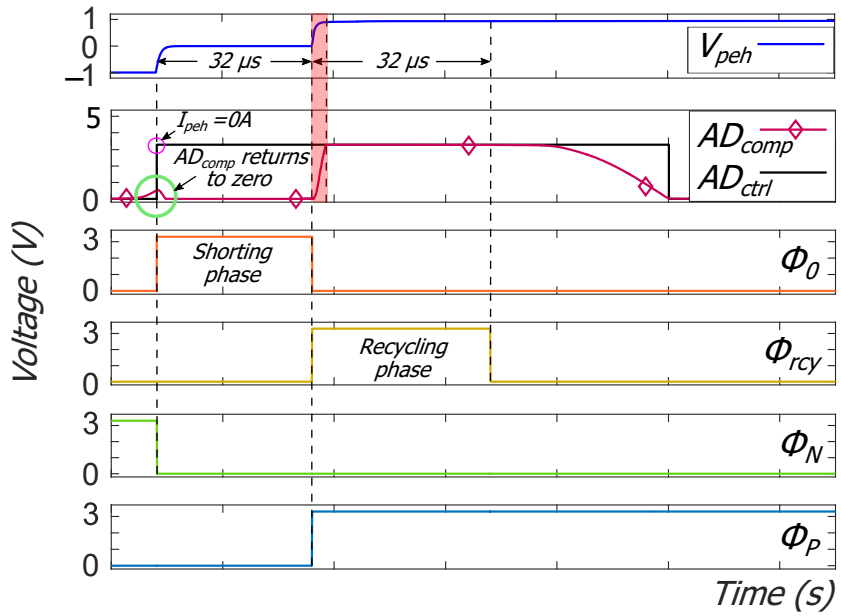


Figure 3.24.: Simulated V_{peh}, AD_{ctrl}, AD_{comp} and voltage flip sequence of FAR-CR with $C_{rcy} = 1\mu F$. It can be noticed, AD_{comp} returns to low shortly after the zero-crossing of I_{peh}

Table 3.2.: Simulated power consumption of FAR/FAR-CR blocks.

Block	Power loss	percentage
AD	965nW	46.84%
Switches	16nW	0.775%
VR	493nW	23.9%
SD	37.63nW	1.825%
VR12	485nW	23.52%
CRTL	5.6nW	0.27%
RO	60nW	2.87%

Table 3.2 lists the simulated power consumption of the different blocks of FAR/FAR-CR interface circuit. The total power consumption in both FAR and FAR-CR is $2.062\mu W$. The power consumption of AD represents 46.84% of the total FAR/FAR-CR power consumption, which is higher comparing to that of the other blocks. This due to the permanent operation of the AD comparator which is powered with $V_{DDH} = 3.3V$.

3.7. Measurement results and discussion

A prototype of the full active rectifier was routed and fabricated in the AMS 0.35μm HV CMOS process. This prototype allows to test and evaluate FAR, FAR-CR and Switch-Only operation modes in addition to the FAR-FC which will be presented in the next chapter. The active area of the ASIC is 7.29mm^2. Figure 3.25 shows micrograph of the ASIC prototype including blocks required for all mentioned operation modes.

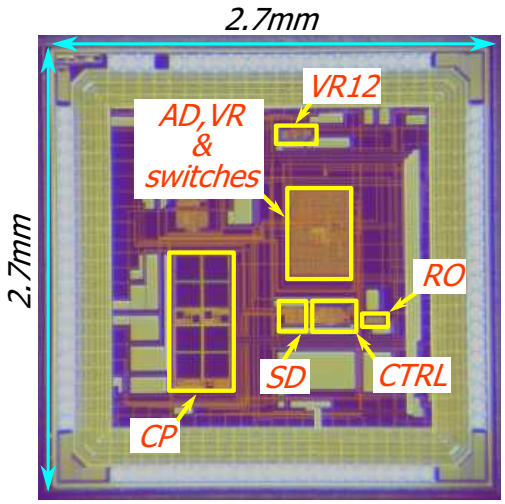


Figure 3.25.: Micrograph of the ASIC chip fabricated in the AMS 0.35μm HV CMOS foundry process.

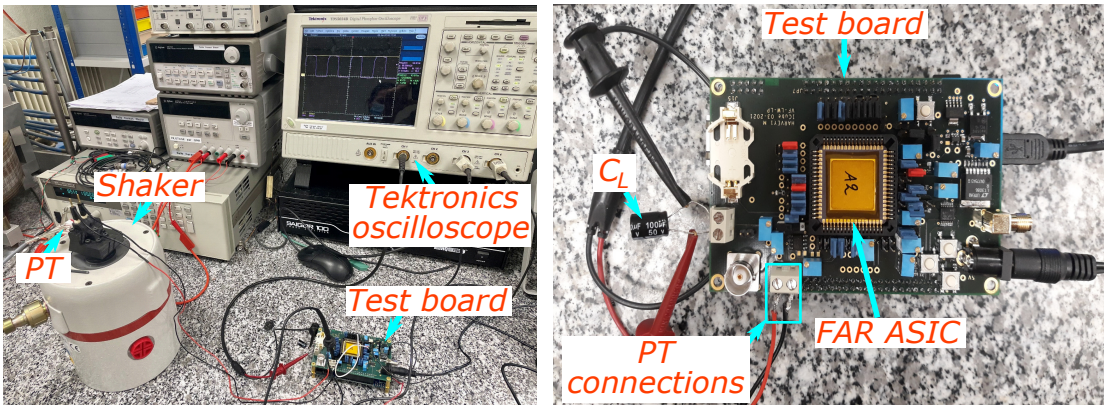


Figure 3.26.: Experimental setup (left), and test board (right).

Figure 3.26 shows the experimental setup and the test board. A commercial piezoelectric transducer S118-J12S-1808YB from Piezo.com with $C_{peh} = 100nF$ and a resonance frequency of 130Hz was used in these experiments. This PT has characteristics close to those of the LIST PT. A shaker (LDS® V400) was excited using

Agilent® 6813B function generator by a $100Hz$ sine waveform signal. This shaker was also controlled by a Labview platform for signal acquisition via a Tektronix® TDS oscilloscope. The acceleration is set to get $\hat{V}_{oc} = 1V$, i.e. $\hat{I}_{peh} = 62.8\mu A$, and a conventional capacitor $C_L = 100\mu F$ is used to store the extracted energy. Also an external stable power supply is used to provide FAR and FAR-CR with the voltage $V_{DDH} = 3.3V$.

Figure 3.27 shows the measured V_{peh} and V_{rect} when the ASIC chip is configured in FAR operation mode. After the voltage flip operation, the voltage across C_{peh} is $V_b = 0.864V$ which corresponds to 86.4% voltage flip efficiency. This value is lower than the simulated value due to two reasons. The first reason is related to the harmonic oscillations induced due to strong coupling effect when the PT operates close to its resonance frequency ($130Hz$). These oscillations prevent the complete voltage flip (Figure 3.27 (a)). The second reason is the charge loss due to the ON-resistance of the TG switches and the various interconnections between the PT and the test board. This charge loss is higher during the sharing phase when the charge from C_L is transferred through SW_3 and SW_2 or SW_1, and the ON-resistance is thus higher than during the shorting phase. Therefore, the duration of the sharing/recycling phase $\Phi_K = 32\mu s$ is experimentally determined to yield optimal voltage flip efficiency. Measurement results also show that with $C_L = 100\mu F$, V_{rect} is constant and the voltage ripple ΔV is negligible (i.e. lower than $1mV$).

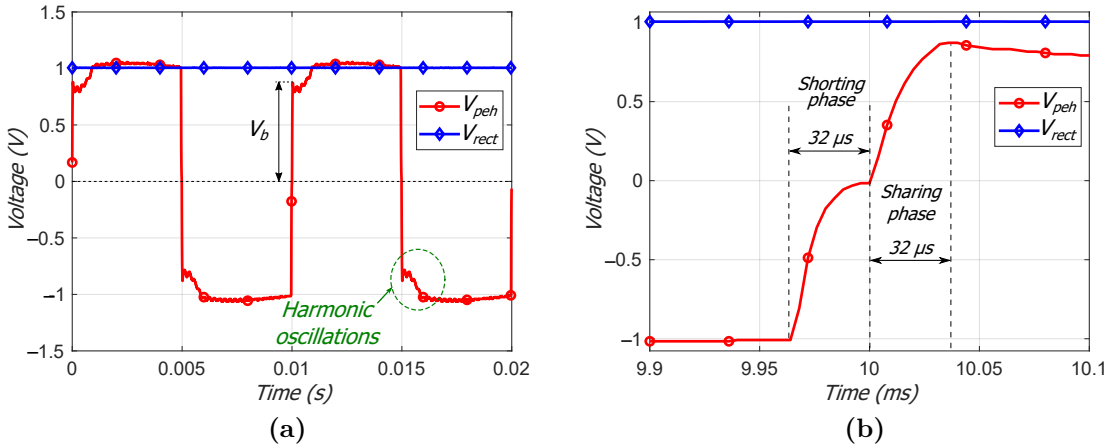


Figure 3.27.: (a) Measured waveform of V_{peh} and V_{rect}, (b) Zoom view during the voltage flip operation, VR regulates V_{rect} to $\hat{V}_{oc} = 1V$.

In order to evaluate the power efficiency of the FAR circuit compared to the Switch-Only circuit, the output power of both schemes were measured. For this experiment, a variable load resistor was connected to the system output and the VR was disabled. Figure 3.28 (a) shows the output power as a function of $1/R_L$. The FAR achieves better power performance as $1/R_L$ increases and yields around 100% more power

than Switch-Only for $1/R_L \simeq 2.24 \times 10^{-5} S$ ($R_L \simeq 45k\Omega$). However, as both circuits don't have the same output voltage for a given value of R_L (section 3.3 (Figure 3.8)), therefore, the output power was also measured as a function of V_{rect} (Figure 3.28 (b)). Measurements show that both circuits achieve maximum power when $V_{rect} \simeq \hat{V}_{oc}$. Also, as mentioned in section 3.3, Switch-Only circuit achieves slightly better performance than FAR, with $P_{max-SO} = 19.3\mu W$ and $P_{max-FAR} = 19.1\mu W$, respectively. However, when $V_{rect} < \hat{V}_{oc}$, FAR can deliver up to 20% more power than Switch-Only. Furthermore, for $V_{rect} < 0.5V$, the FAR ASIC turns off . This due to the fact that this voltage is not sufficient to supply the control block (CTRL).

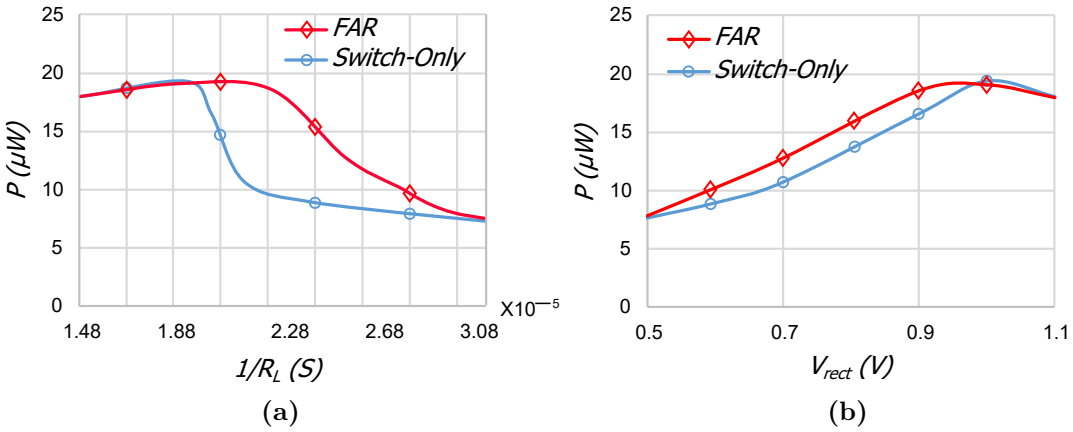


Figure 3.28.: Output power as a function of $1/R_L$ (a), V_{rect} (b).

The power performance of FAR is also evaluated compared to that of conventional FBR by the maximum output power improving rate (MOPIR) [32]:

$$MOPIR = \frac{P_{max-FAR}}{P_{max-FBR}} \tag{3.28}$$

where $P_{max-FAR}$ and $P_{max-FBR}$ are the maximum output powers of FAR and FBR, respectively. The maximum output power of FBR is [81]:

$$P_{max-FBR} = 4C_{peh} f_{ex} (\frac{V_{oc}}{2} - V_{th})^2 \tag{3.29}$$

where V_{th} is the threshold voltage of FBR diodes. Using the Schottky diodes with $V_{th} = 0.3V$, the maximum output power achieved by the FBR is $7.98\mu W$, hence the MOPIR is around 2.39.

The FAR-CR was also tested with an off-chip capacitor $C_{rcy} = 1\mu F$. Figure 3.29 shows the measured V_{peh} of both FAR-CR and Switch-Only circuits, in addition to the V_{rcy} behavior in steady state. At each zero crossing moment of I_{peh}, C_{rcy} shares its charge with C_{peh}. When C_{peh} is charged and the AD turns on, i.e. $V_{sp} = V_{rect}$,

C_{rcy} progressively recharges as the VR operates (Figure 3.29 (bottom)). This allows to achieve high voltage flip efficiency (Figure 3.29 (middle)) compared to the Switch-Only which has a 0.5 voltage flip efficiency (Figure 3.29 (top)).

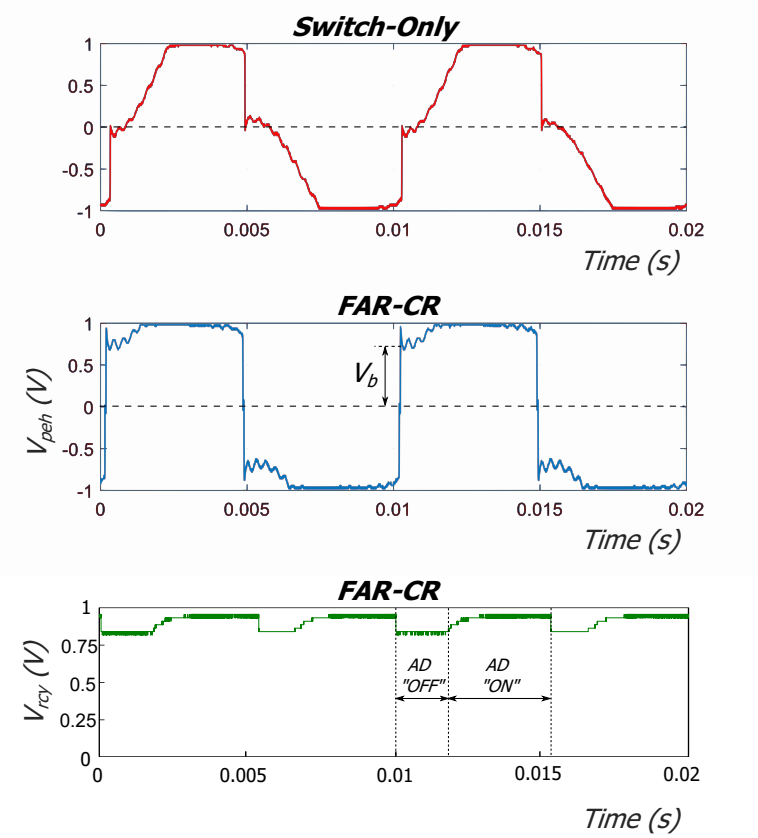


Figure 3.29.: Measured transient signal of V_{peh} for Switch-Only operation mode (top) and V_{peh} (middle),V_{rcy} (bottom) of FAR-CR operation mode with $C_{rcy} = 1\mu F$.

In order to assess the benefit of the recycling principal on the system performance, an experiment consisting in switching R_L from $330k\Omega$ to $10k\Omega$ (starting at $t \approx 2.5s$) was performed on both FBR, Switch-Only circuits and the FAR-CR circuit with $C_{rcy} = 22\mu F$. Measurement results of the V_{rect} evolution (Figure 3.30) reveals that in steady state the FAR-CR's efficiency is identical to Switch-Only. But, in transient phases, V_{rect} decreases more slowly with FAR-CR than with the Switch-Only, i.e. $\eta F > 0.5$ with FAR-CR, and thus the power efficiency increases.However, when V_{rect} decreases below $0.5V$, the circuit does not work properly. That's why $V_{rect(Switch-Only)}$ and $V_{rect(FAR-CR)}$ converge again. In the case of FBR circuit, results show that the FBR performance is far below the performance of both FAR-CR and Switch-Only circuits. The measured average power over the transient phase, i.e. during discharging C_{rcy}, is $46.5\mu W$ for the FAR-CR, $44.27\mu W$ for the Switch-Only, and $21.57\mu W$ for the FBR. The measured power improvement ratio MOPIR of FAR-CR compared to the FBR and Switch-Only configuration is 216% and 5%,

respectively.

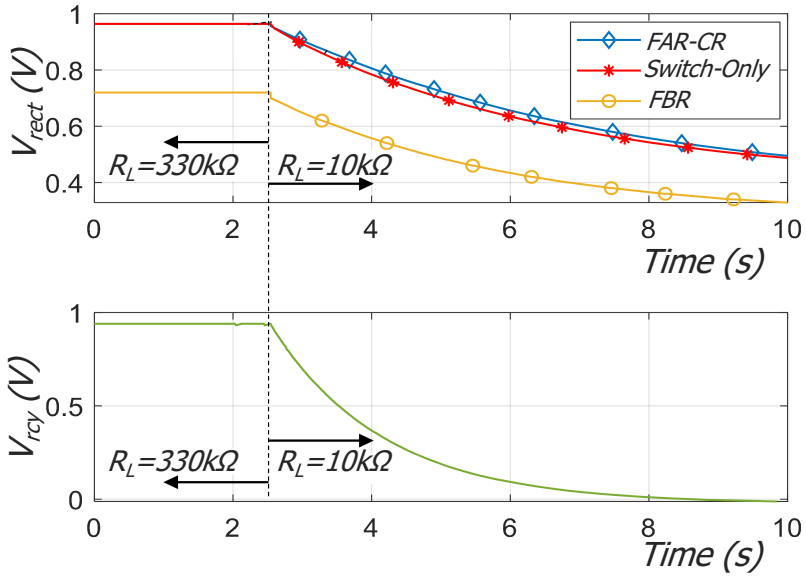


Figure 3.30.: Measured transient signal of V_{rect} (top) when switching R_L from $330k\Omega$ to $10k\Omega$ for FBR, Switch-Only operation mode and FAR-CR, and corresponding evolution of V_{rcy} of the FAR-CR (bottom).

3.8. Conclusion

This chapter introduced two simple concepts of the voltage flip across the piezoelectric transducer (PT). Unlike to SSHI and SSHC circuits that reuse the own charges of the PT capacitor to flip the voltage across it, a tiny fraction of the storage capacitor and the excess charge stored in a single additional capacitor is used in the fully integrated FAR circuit and FAR-CR, respectively, to improve the voltage flip efficiency. Besides to the significant boost in the voltage flip efficiency, the detailed analysis of the FAR power performance reveals that , the FAR circuit helps enhancing the power efficiency compared to the Swich-Only circuit. Measurement results on the CMOS prototype confirm that under load constraint, FAR achieves twice more power performance than the Switch-Only and up to 20% during the start-up transit phase (i.e. $V_{rect} < \hat{V}_{oc}$). Measurement results also confirm that during transient heavy-duty operation, the CMOS FAR-CR prototype achieves up to 216% and 5% power improvement ratio compared to the conventional full bridge rectifier and the Switch-Only circuits, respectively. The voltage efficiency enhancement of the proposed circuits shows the interest of working on combining either the FAR or FAR-CR principle with the SSHI or SSHC to further improve both the voltage flip and power efficiencies. However, boosting the voltage flip efficiency in FAR implies

wasting a tiny part of the total stored charge in the storage capacitor which should be used to supply the load during its activity. For this reason, it is worth while to combine FAR-CR principle with SSHI or SSHC, where only the excess charge stored when the load in not active (as in the most of wireless sensors applications) is used to improve SSHI or SSHC voltage flip efficiency. In addition to this voltage flip improvement and as confirmed by the measurement results, a power improvement can also be achieved when switching from the non-active load (no load connected) to the active load (connected load) system configurations. This is due to the FAR-CR contribution in slowing down the discharging of the storage capacitor.

4. Enhanced SSHC-based Full Active Rectifier with Reduced Set of Flipping Capacitors (FAR-FC)

4.1. Introduction

In this chapter an improved full active rectifier based on the SSHC principle, named Full Active Rectifier on Flipping Capacitors (FAR-FC) is presented. Compared to SSHC interface circuits reported in literature, the proposed FAR-FC employs a reduced set of flipping capacitors to efficiently flip the voltage across the piezoelectric transducer (PT) even when the later is weakly excited. The FAR-FC also allows to use a wide range of PT capacitance C_{peh} values, while this value is usually low ($< 50nF$) in literature. The charge recycling circuit (FAR-CR) presented in the previous chapter is also combined with the FAR-FC to further enhance the voltage efficiency of the SSHC. Section 4.2 recalls the principles of a the conventional capacitor-based interface SSHC. The FAR-FC operation principal and performance are presented in section 4.3. The circuit implementations are detailed in section 4.5. Section 4.6 provides the simulation results. Measurement results are discussed in section 4.7 and section 4.8 concludes this chapter.

4.2. Capacitor-based SSH interface circuit

The capacitor-based SSH (i.e. SSHC) principle is based on employing one or more capacitors in order to reuse the PT's capacitor, C_{peh}, own charges to flip the voltage V_{peh} across it. Figure 4.1 shows the One-capacitor SSHC circuit and the associated waveforms. It consists of one switched capacitor C_0 used to synchronously flip the V_{peh} combined with a full bridge rectifier (FBR). As shown in Figure 4.1 (b), the V_{peh} inversion occurs at each zero-crossing moment of the PT current I_{peh}. This corresponds to the moment when V_{peh} reaches its maximum value i.e. $V_{rect} + 2V_{th}$, where V_{rect} is the voltage across the storage capacitor and V_{th} is the threshold voltage across the FBR diode. The V_{peh} flip operation starts by connecting C_{peh} and C_0 in parallel to share the charge of C_{peh} with C_0 (i.e. the sharing phase Φ_p). It is followed by the shorting phase Φ_0 to get rid of the residual charge of C_{peh}. Finally, C_{peh} is

recharged by C_0 by reconnecting both capacitors in parallel (i.e. the building phase Φ_n).

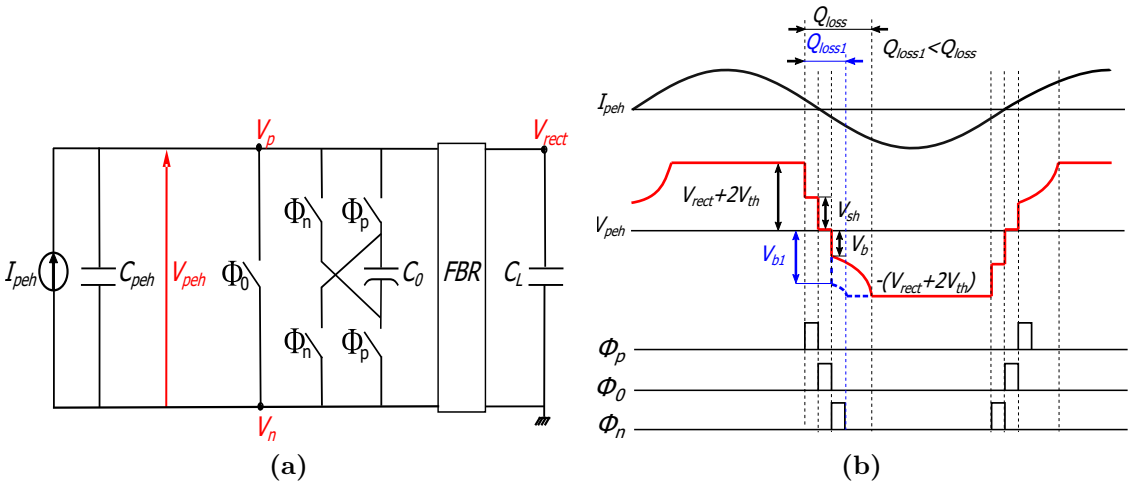


Figure 4.1.: (a) One-capacitor SSHC interface circuit, (b) Current, voltage and control signals waveforms.

Let's assume that V_{sh} and V_b denote the voltages across PT at the end of the sharing and the building phases, respectively. In steady state V_b becomes constant and C_{peh} needs to charge from V_b to $V_{rect} + 2V_{th}$. The charge conservation equations during both sharing and building phases can be written as:

$$V_{sh}(C_{peh} + C_0) = C_{peh}(V_{rect} + 2V_{th}) + C_0 V_b \tag{4.1}$$

$$V_b(C_{peh} + C_0) = V_{sh} C_0 \tag{4.2}$$

Assuming an ideal FBR, i.e. with no threshold, the ratio between V_b and V_{rect} can be expressed as [32]:

$$k_{FCR1} = \frac{V_b}{V_{rect}} = \frac{1}{2 + \frac{C_{peh}}{C_0}} \tag{4.3}$$

This ratio is highly related to the voltage flip efficiency $\eta_F = \frac{V_{rect}+V_b}{2V_{rect}}$. This relation can be expressed as:

$$k_{FCR1} = 2\eta_F - 1 \tag{4.4}$$

The maximum output power of this interface depends on k_{FCR1} [32] and thus on

η_F, it is expressed as:

$$P_{SSHCmax} = \frac{2C_{peh}V_{oc}^2 f_{ex}}{1 - k_{FCR1}} = \frac{2C_{peh}V_{oc}^2 f_{ex}}{2(1 - \eta_F)} \tag{4.5}$$

Equation (4.5) shows that the power extracted by SSHC circuit increases as k_{FCR1} or η_F approaches one (i.e. as V_b approaches V_{rect}). In the case of a one-capacitor SSHC circuit, k_{FCR1} is related to both C_{peh} and C_0 as shown in equation (4.3). When $C_0 \gg C_{peh}$, k_{FCR1} converges to $\frac{1}{2}$, which yields $MOPIR = 4$[1]. Several implementations have been proposed in the state of the art to improve the power performance of SSHC circuit. In [7], using eight parallel flipping capacitors, improves the k_{FCR1} to 4/5 leading to $MOPIR = 9.7$. Recently, it was shown in [34], that using $C_0 = 100C_{peh}$ increases the output power by 35.7%. In another implementation proposed in [32], the use of four re-configurable capacitors led to $n_F = 0.85$ voltage flip efficiency and $MOPIR = 4.83$. This topology requires a seven-phase voltage flip scheme. Increasing the number of switching phases to 21 [96] improves the $MOPIR$ to 9.3. However, the use of a large number of parallel flipping capacitors increases the number of switching phases and hence the flipping time [7]. This in turn reduces the conduction time and thus the extracted power. Also, using the re-configurable flipping capacitors [32,96] increases the number of required switches, which increases the ON-resistance during one flipping phase, especially, when the flipping capacitors are connected in series as in [96]. In fact, this resistance affects the time constant of the RC circuit formed during one flipping phase, and therefore the time of charge transfer from one capacitor to another. Thereby, the flipping time increases with the ON-resistance. As a result, increasing the number of flipping capacitors or phases to improve the flipping efficiency implies fast voltage flip operation. This can be achieved only when C_{peh} is low. Otherwise, the use of large C_{peh} in such implementations significantly increases the charge loss and hampers the voltage flip and power efficiencies.

Furthermore, equation (4.5) also shows that the maximum output power is also related to the PT properties and more pointedly to the V_{oc}, the open circuit voltage of the PT. This voltage is induced by the mechanical excitation applied to the PT. The higher the mechanical excitation applied to the PT, the higher the magnitude of V_{oc} across the PT. A small increase in V_{oc} significantly boosts the output power, whereas a low excitation level, i.e. $V_{oc} \leq 1V$, extremely limits the SSHC extracted power and prevents the load activity under these PT operation conditions. The following sections present an enhanced SSHC interface circuit. The proposed circuit uses a reduced set of flipping capacitors and achieves high voltage flip with an acceptable extracted power, even while employing a PT with a high parasitic capacitor C_{peh}, operated under low excitation conditions.

[1]MOPIR: Maximum Output Power Improvement Ratio

4.3. FAR-FC interface circuit topology and operation principle

As Figure 4.1 (b) illustrates it, increasing the building voltage from V_b (red curve) to V_{b1} (blue curve) contributes to minimize the charge loss Q_{loss}. This in turn increases the conduction time and thus the extracted power. Based on this observation, an improved SSHC circuit is implemented to efficiently perform the PT voltage flip operation. Figure 4.2 shows the architecture of the FAR-FC interface circuit.

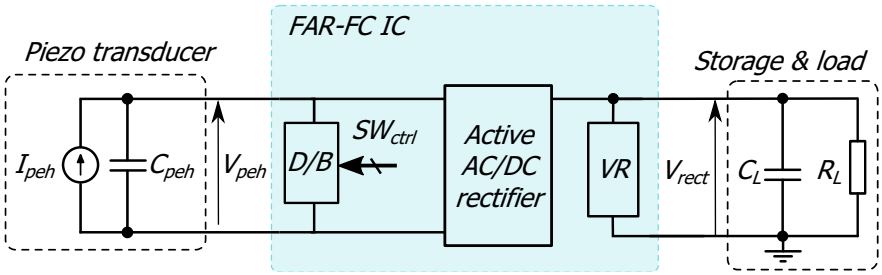


Figure 4.2.: FAR-FC circuit architecture.

It mainly consists of: a Damping/Building capacitors array (D/B), an active AC/DC rectifier, and a voltage regulator (VR). The D/B block flips the voltage across C_{peh} at each zero crossing moment of I_{peh}. The active AC/DC rectifier block rectifies the voltage across the PT. This voltage, i.e. V_{peh}, is then regulated by the VR block to match the optimal voltage value that ensures the maximum power extraction. This regulation also helps protecting the circuit from the consequences of over load.

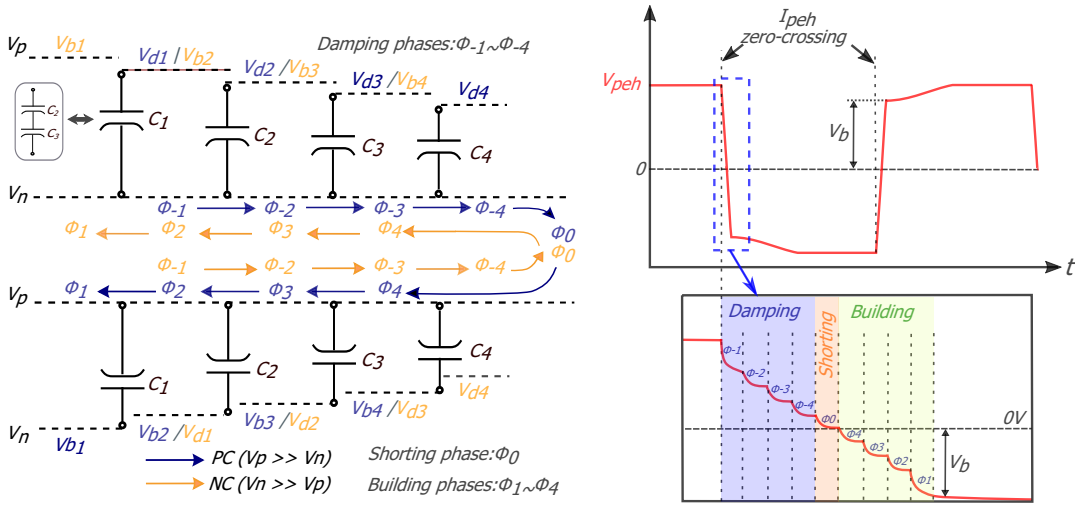


Figure 4.3.: (left) 9-phase flipping capacitors configuration for PC and NC cycles, and (right) evolution of V_{peh} during its flipping phases when the flipping capacitors are fully charged.

The voltage flip operation is performed in nine phases using three re-configurable capacitors. As in the one-capacitor SSHC interface, the V_{peh} inversion operation can be subdivided into: 1) damping phases (Φ_{-1}, Φ_{-2}, Φ_{-3}, Φ_{-4}) where C_{peh} is discharged through the flipping capacitors, 2) a shorting phase (Φ_0) to get rid of the remaining charge in C_{peh}, 3) building phases (Φ_4, Φ_3, Φ_2, Φ_1) where C_{peh} is recharged from the flipping capacitors. Figure 4.3 shows the 9-phase reconfiguration cycle at each V_{peh} inversion operation (left), in addition to the V_{peh} evolution during the flipping phases when the flipping capacitors are fully charged, i.e. in the steady state (right). In this configuration, a trade-off between the number of capacitors/phases, power extraction efficiency and control complexity is made. This trade-off limits to three the maximum number of the switches in series employed during the D/B phases. This contributes to limit the ON-resistance of the current path and thus the corresponding RC time constant during the voltage flip operation, which enables the use of piezoelectric transducers with large C_{peh}.

Assuming that n is the phase number and m is the voltage flip cycle number. After m voltage flip cycles, V_{peh} can be defined as $V_{d(n,m)}$ and $V_{b(n,m)}$ at the end of the damping Φ_{-n} and building Φ_n phases, respectively. Applying the conservative equations, these voltages can be expressed as follows:

$$V_{d(n,m)} = \frac{V_{d(n-1,m)}C_{peh} + V_{b(n,m-1)}C_n}{C_{peh} + C_n} \tag{4.6}$$

$$V_{b(n,m)} = \frac{C_{peh}V_{b(n+1,m)} + V_{d(n,m)}C_n}{C_{peh} + C_n} \tag{4.7}$$

In steady state, $V_{b(1,m)} = V_{b(1,m-1)}$. As a consequence, the voltage flip efficiency can be expressed as:

$$\eta_F = \frac{V_{b(1,m)} + V_{rect}}{2V_{rect}} \tag{4.8}$$

From (4.8), it is clear that increasing $V_{b(1,m)}$ leads to an increase in η_F increase. For such a configuration, fulfilling the condition $C_n \gg C_{peh}$ is not sufficient to reach the maximum $V_{b(1,m)}$ as in the one-capacitor SSHC interface. The choice of the capacitance values for this configuration is the key to optimize the voltage flip operation. The simplified calculation of $V_{d(n,m)}$ and $V_{b(n,m)}$ when $m = 1$ using (4.6) and (4.7) allows to find the condition to have the highest $V_{b(1,1)}$. As a result $V_{b(1,1)}$ can be expressed as:

$$\begin{aligned} V_{b(1,1)} = &\frac{C_{peh}C_1(C_{peh} + C_2)^2(C_{peh} + C_3)^2(C_{peh} + C_4)^2}{K} \\ &+ \frac{C_{peh}^3C_2(C_{peh} + C_3)^2(C_{peh} + C_4)^2 + C_{peh}^5(C_{peh} + C_4)^2 + C_{peh}^7C_4}{K} \end{aligned} \tag{4.9}$$

where $K = (C_{peh} + C_1)^2(C_{peh} + C_2)^2(C_{peh} + C_3)^2(C_{peh} + C_4)^2$. The previous equation

(4.9) shows that maximum $V_{b(1,1)}$ is achieved when $C_1 < C_{2,3} < C_4$. This also applies to maximum $V_{b(1,m)}$. This condition is satisfied by setting $C_2 = C_3 = \frac{C_4}{2}$ and thus $C_1 = \frac{(C_2 C_3)}{(C_2+C_3)} = \frac{C_{2,3}}{2}$. Based on the characteristics of the PT device (S118-J12S-1808YB) employed in our experiments, the parasitic capacitor C_{peh} is estimated to be $100nF$. To choose the capacitance values, theoretical simulation of the voltage flip efficiency η_F versus different C_1 capacitance values was performed (Figure 4.4). Simulation results show that increasing the $\frac{C_1}{C_{peh}}$ leads to an increase in η_F. However, for $\frac{C_1}{C_{peh}} > 5$, the improvement on the η_F becomes negligible. Therefore, the value of C_1 is set to $5 \times C_{peh}$, i.e. $C_1 = 500nF$, $C_{2,3} = 1\mu F$ and $C_4 = 2\mu F$.

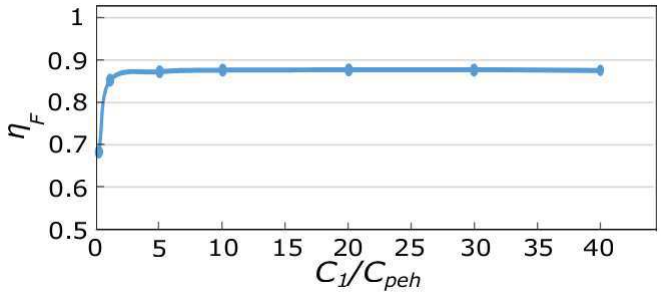


Figure 4.4.: Voltage flip efficiency η_F as a function of $\frac{C_1}{C_{peh}}$.

4.4. FAR-FC performance analysis

In this section the performance improvement of the FAR-FC circuit compared to the FBR circuit is evaluated. The maximum power delivered by the FBR circuit is expressed by (see chapter 2 (section 2.4)):

$$P_{rectmax-FBR} = 4C_{peh} f_{ex} (\frac{V_{oc}}{2} - V_{th})^2 \tag{4.10}$$

where V_{th} is the threshold voltage of each diode in the FBR. For an almost ideal FBR circuit, V_{th} can be ignored and the maximum extracted power can be expressed as:

$$P_{rectmax-FBR_{ideal}} = C_{peh} f_{ex} V_{oc}^2 \tag{4.11}$$

To assess the power which can be extracted by the FAR-FC circuit, the charge loss in every cycle $Q_{loss/cycle}$ should be evaluated.
In steady state when V_b is constant (Figure 4.3 (right)), before the FAR-FC starts extracting power, the PT needs to charge C_{peh} from V_b to V_{rect}. This amount of charge, Q_{loss}, is considered as wasted charge and can be expressed for every cycle

as:

$$Q_{loss/cycle} = 2C_{peh}(V_{rect} - V_b) \tag{4.12}$$

The available charge from the PT every cycle is given by:

$$Q_{tot/cycle} = 2\int_0^{T/2} I_{peh}(t)dt = \frac{4\hat{I}_{peh}}{\omega_0} = 4C_{peh}\hat{V}_{oc} \tag{4.13}$$

where $\omega_0 = 2\pi f_{ex}$ and f_{ex} is the PT excitation frequency. Therefore, the total charge that is actually delivered to the output every cycle can be written as:

$$Q_{rect/cycle} = Q_{tot/cycle} - Q_{loss/cycle} = 2C_{peh}\left[2\hat{V}_{oc} - (V_{rect} - V_b)\right] \tag{4.14}$$

The energy delivered by FAR-FC to the output every cycle is given by:

$$E_{rect/cycle} = Q_{rect/cycle}V_{rect} = 2C_{peh}V_{rect}\left[2\hat{V}_{oc} - (V_{rect} - V_b)\right] \tag{4.15}$$

Hence, the extracted power stored in C_L can be evaluated as:

$$P_{rect-FAR-FC} = E_{rect/cycle}f_{ex} = 2C_{peh}V_{rect}f_{ex}\left[2\hat{V}_{oc} - (V_{rect} - V_b)\right] \tag{4.16}$$

The derivative of equation (4.16) shows that the maximum output power can be extracted when V_{rect} satisfies:

$$V_{rect} = \hat{V}_{oc} + \frac{V_b}{2} \tag{4.17}$$

This value represents the optimal output voltage that should be maintained by the voltage regulator VR at which maximum power harvesting is obtained. the latter is expressed as:

$$P_{rectmax-FAR-FC} = 2C_{peh}f_{ex}(\hat{V}_{oc} + \frac{V_b}{2})^2 \tag{4.18}$$

Compared to the maximum output power extracted by an ideal FBR in (4.11), the expression of the maximum output power improvement rate can be written as:

$$MOPIR = \frac{P_{rectmax-FAR-FC}}{P_{rectmax-FBR}} = \frac{2(\hat{V}_{oc} + \frac{V_b}{2})^2}{\hat{V}_{oc}^2} \tag{4.19}$$

Equations (4.18) and (4.19) show that the value of V_b significantly impacts the maximum extracted power and the performance of the FAR-FC circuit, respectively. Note that, having a $V_b = 0V$, i.e. no flipping capacitor, yields $P_{rectmax} = 2C_{peh}f_{ex}\hat{V}_{oc}^2$ and $MOPIR = 2$, which corresponds to the output power and the performance of the Switch-Only circuit, respectively.

4.5. Circuit implementations of FAR-FC interface

The system architecture of the FAR-FC interface circuit is shown in Figure 4.5. This system has the ability of recycling charges via switch SW_{rcy}.

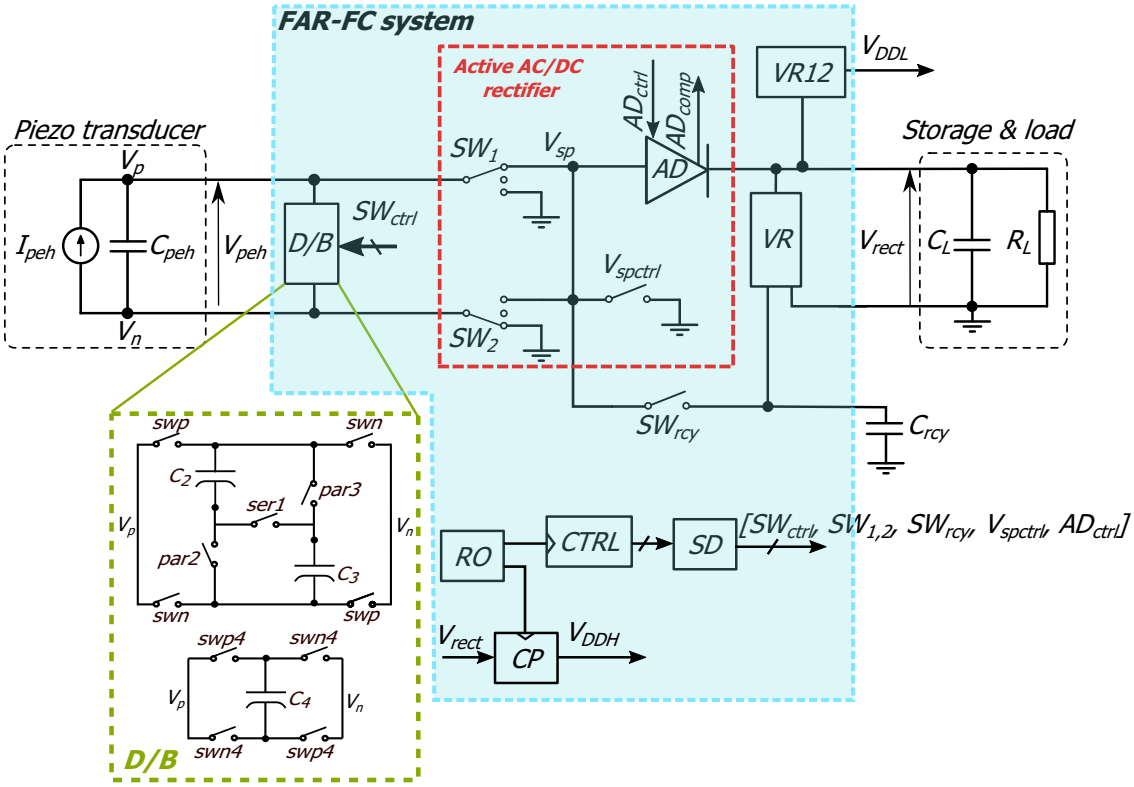


Figure 4.5.: FAR-FC system architecture.

All the components in this system are implemented on-chip except the flipping capacitors (D/B) and the capacitors employed for voltage regulation. In addition to the D/B, the active AC/DC rectifier and the VR blocks, this system includes a control block (CTRL) to generate all control signals, which are then level-up shifted by a switch drivers block (SD) in order to ensure the proper operation of FAR-FC system. Also, the same ring oscillator (RO) and voltage regulator (VR12) blocks employed in the FAR/FAR-CR system (Chapter 3) are employed in the FAR-FC system. In addition, a charge pump (CP) is also implemented to provide the high voltage supply ($V_{DDH} = 3V$) to both AD's comparator and switch drives.

4.5.1. Damping/Building capacitors array (D/B)

The D/B block consists of a set of three switched capacitors to flip the voltage across the PT according to a specific configuration (Figure 4.3). This configuration

is achieved using eleven transmission gate switches (TG) as shown in Figure 4.5. These TGs, as mentioned in chapter 3 (section 3.5), are designed to have very low ON-resistance around 15Ω. For such configuration, at most three TGs are connected in series during one damping/building phase. This reduces the on-resistance during the charge transfer between C_{peh} and the flipping capacitors and thus reduces the total RC time required to accomplish the voltage flip operation.

Table 4.1.: Summary of control signal combination.

SWctrl	Control phase								
	Φ_{-1}	Φ_{-2}	Φ_{-3}	Φ_{-4}	Φ_0	Φ_4	Φ_3	Φ_2	Φ_1
swp	On/Off	On/Off	On/Off	Off	On	Off	Off/On	Off/On	Off/On
swn	Off/On	Off/On	Off/On	Off	On	Off	On/Off	On/Off	On/Off
ser1	On	Off	Off	Off	Off	Off	Off	Off	On
par2	Off	On	Off	Off	Off	Off	Off	On	Off
par3	Off	Off	On	Off	Off	Off	On	Off	Off
swp4	Off	Off	Off	On/Off	Off	Off/On	Off	Off	Off
swn4	Off	Off	Off	Off/On	Off	On/Off	Off	Off	Off

The switches are named after their control signals, that is why some switches bare the same name. Table 4.1 shows the control sequence of each switch when V_{peh} is inverted from positive to negative ($V_p \rightarrow V_n$). Note that when V_{peh} is inverted from negative to positive ($V_n \rightarrow V_p$), the control sequence for swp, swn, $swp4$ and $swn4$ switches is changed during certain phases as mentioned in red in Table 4.1. The whole set of control signals mentioned in Table 4.1 is named $SWctrl$.

4.5.2. Active AC/DC rectifier and voltage regulator (VR) blocks

As shown in Figure 4.5, the active AC/DC rectifier block consists of five switches named after their control signals and an active diode (AD). The switches (SW_1, SW_2) are used to rectify the voltage across the PT. During the positive phase of V_{peh}, the switches controlled by SW_1 and SW_2 signals are ON and OFF, respectively and vice versa during the negative phase. This makes the node V_{sp} always connected to the positive terminal of the PT, i.e. V_{peh} is rectified.

Like in FAR and FAR-CR systems, an active diode (AD) with a PMOS switch controlled by the control block is used to both prevent the current back-flow from C_L to PT and detect the zero crossing moment of the PT current. Therefore, its output signal AD_{comp} is the key signal that is used as a trigger of the control block. This sub-block has the same circuit diagram of the one used in FAR/FAR-CR. In order to ensure proper charge transfer from C_{peh} to the flipping capacitors during the damping phase, the AD is disconnected from the PT. This disconnection sets the node V_{sp} in high impedance state, which can leads to a false $I_{peh} = 0A$ detection.

To prevent this phenomenon, a switch controlled by signal $Vspctrl$ is added to short V_{sp} to the ground during the damping phases.

The voltage regulator (VR) block employed in this implementation has the same architecture of the one used in FAR/FAR-CR system implementation. The voltage reference is also set to the value that ensures optimal operation, i.e. $V_{rect} = \hat{V}_{oc} + \frac{V_b}{2}$ for FAR-FC implementation (equation (4.17)).

4.5.3. Control (CTRL) and switch drivers (SD) blocks

The control block CTRL block is used to generate the signals required for flipping V_{peh} (Table 4.1), the signals of the active AC/DC rectifier block (Figure 4.5) and the $SWrcy$ signal for C_{rcy} charge recycling. Figure 4.6 shows the circuit diagram of CTRL. At the rising edge of AD_{comp}, a lock signal ($Lock$) is generated to trigger the 9-phase sequence and maintain the PMOS switch of the AD in open state during the entire flipping and charge recycling operations. To generate $SWrcy$ and the V_{peh} flip control signals, a 4-bit counter (CNT), a decoder and a sequence generator blocks are employed. The OSC_{CTRL} signal generated by the oscillator RO is used as a clock signal of the counter. At the end of the voltage flip and charge recycling operations, a reset signal RST_int is generated to reset the counter and prepare for the next voltage flip operation.

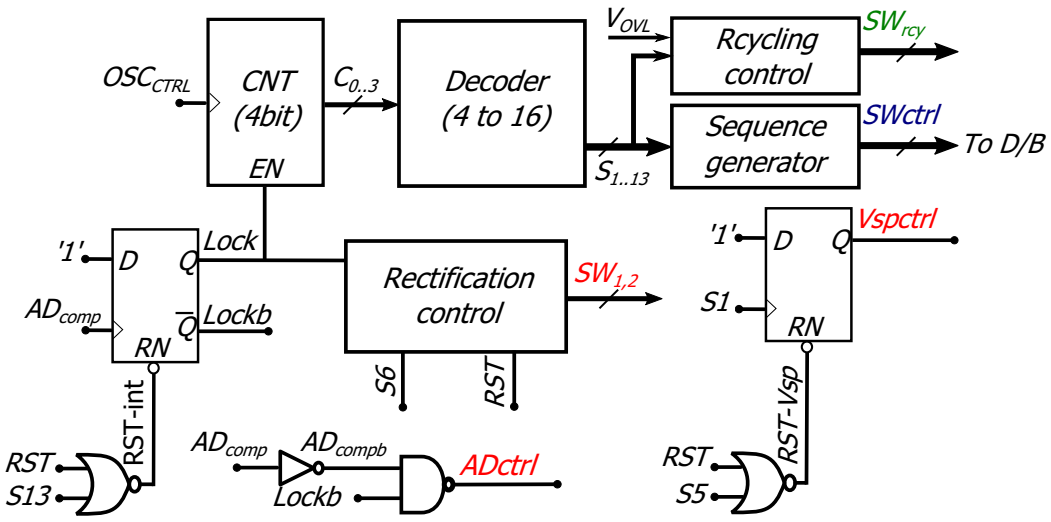


Figure 4.6.: Control block circuit (CTRL).

The pulse width of one phase control signal PW is chosen depending on the required time that guarantees proper charge transfer between C_{peh} and the flipping capacitors. This duration corresponds to the maximum time needed to discharge or recharge C_{peh} through the flipping capacitor during one voltage flipping phase. To determine duration time, the second damping phase, i.e. Φ_{-2}, is taken, where a maximum RC

time constant can be achieved due to the three switches connected in series (swp, $par2$, swp), in addition to the higher capacitance value $C_2 = 1\mu F$ compared to the capacitance value used in the first damping phase Φ_{-1}, i.e. $C_1 = 500nF$. Figure

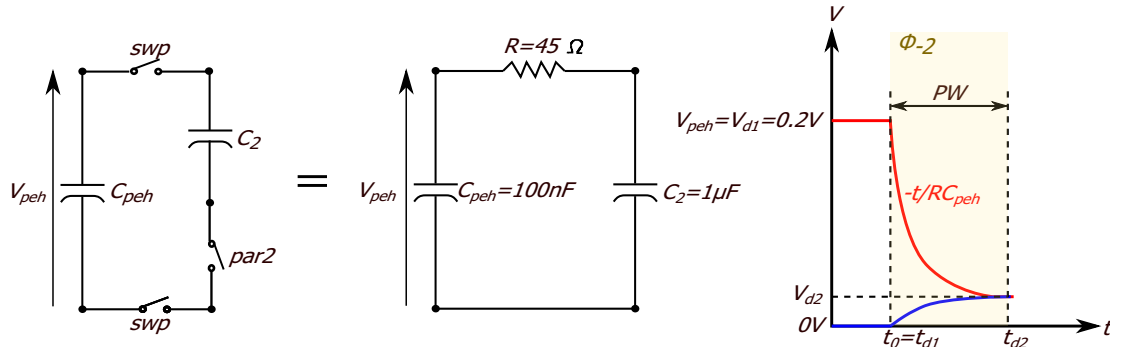


Figure 4.7.: Equivalent circuit during the second damping phase (Φ_{-2}) with the voltage evolution across both C_{peh} and C_2.

4.7 shows the equivalent circuit during Φ_{-2} with the corresponding voltages across C_{peh} and C_2. The resistor $R = 45\Omega$ corresponds to the equivalent ON-resistance of the three switches. The maximum initial voltage across C_{peh} is $V_{peh0} = 1.2V$, which corresponds to the initial voltage across the storage capacitor required to activate FAR-FC. Let's assume that the initial voltage across each flipping capacitor is $0V$ before activating FAR-FC. During the first damping phase Φ_{-1}, C_{peh} and C_1 are connected in parallel. Therefore, the voltage across C_{peh} at the end of Φ_{-1}, can be given by:

$$V_{d1} = \frac{V_{peh0}C_{peh}}{C_{peh} + C_1} = \frac{1.2 \times 100}{100 + 500} = 0.2V \tag{4.20}$$

This voltage, i.e. V_{d1}, corresponds to the initial voltage across C_{peh} at the beginning of the second damping phase Φ_{-2}. During Φ_{-2}, C_{peh} and C_2 are connected in parallel. Therefore C_{peh} discharges (red curve in Figure 4.7) while C_2 charges (blue curve in Figure 4.7) until the voltages across the two capacitors become equal at the end of this phase, i.e. at t_{d2}. This voltage can be given by:

$$V_{d2} = \frac{V_{d1}C_{peh}}{C_{peh} + C_2} = \frac{0.2 \times 100}{100 + 1000} = 0.018V \tag{4.21}$$

and can also be expressed as:

$$V_{d2} = V_{d1}e^{-\frac{t}{RC_{peh}}} \tag{4.22}$$

where t is the time necessary to discharge C_{peh} from $V_{d1} = 0.2V$ to $V_{d2} = 0.018V$.

This time can be calculated as follows:

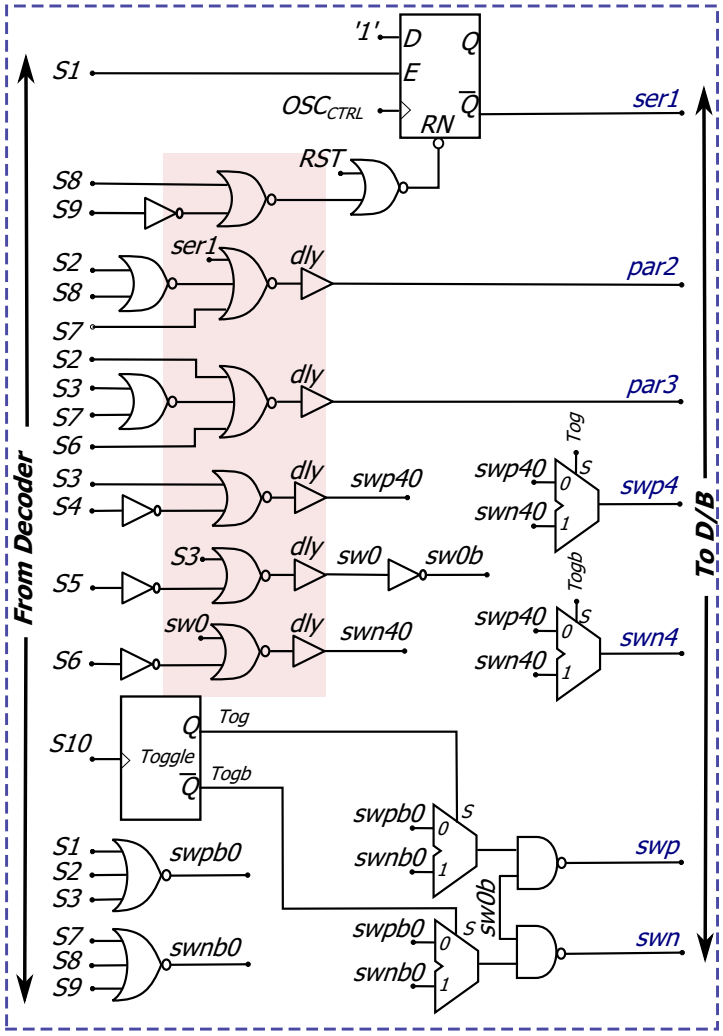
$$t = -RC_{peh} \ln(\frac{V_{d2}}{V_{d1}}) = -45 \times 100 \times 10^{-9} \ln(\frac{0.018}{0.2}) = 10.78\mu s \quad (4.23)$$

As a result, the PW is set to $16\mu s$ that covers the all ranges of time required for the proper charge transfer between C_{peh} and the flipping capacitors. The sequence generator block shown in Figure 4.8 (a) generates the vector of control signals $SWctrl$ mentioned in table 4.1.

In normal operation mode and during the first and the last phases Φ_{-1}, Φ_1, C_2 and C_3 are connected in series by setting $ser1$ signal to a high logic state. A DFF is used to generate $ser1$. Signal $par2$ is generated during Φ_{-2} and Φ_2 phases, i.e. when $S2$ or $S8$ is high. Signal $par3$ is generated when $S3$ or $S7$ is high i.e. during Φ_{-3} and Φ_3 phases. To control the polarity of C_2 and C_3 while connecting with C_{peh}, either signals swp or swn is set to a high logic state depending on whether I_{peh} is positive or negative, respectively. Moreover, both swp and swn are set to a high logic state during the shorting phase Φ_0 in order to short and discharge C_{peh}. To generate swp and swn, three internal signals $swpb0$, $swnb0$ and $sw0b$ are generated during (Φ_{-1}, Φ_{-2}, Φ_{-3}), (Φ_1, Φ_2, Φ_3) and Φ_0 phases, respectively. Finally, a toggle is triggered at the end of each 9-phase generation process to switch the logic state of both swp and swn signals.

Connecting C_4 in parallel with C_{peh} during Φ_{-4} or Φ_4 is achieved by setting either $swp4$ or $swn4$ signals to a high logic state depending on whether V_{peh} is positive or negative during these phases. At the end of each 9-phase generation process, the logic state of both $swp4$ and $swn4$ signals is switched by the same toggle used in this block. To avoid the overlap between two successive signals, additional NOR and DELAY (dly) gates are employed as shown in the shaded part of the sequence generator block in Figure. 4.8 (a). This is important to avoid false connection between flipping capacitors nodes during the charge transfer, which significantly impacts the system efficiency.

The recycling control block shown in Figure 4.8 (b) is used to control the charge recycling process. The voltage regulator VR's output comparator signal V_{OVL} is used to trigger the charge recycling process. Upon rising edge of V_{OVL}, the recycling of the charge of C_{cry} is enabled. After the V_{peh} flip operation, the signal $SWrcy$ is set to high and thus the charge transfer from C_{rcy} to C_{peh} starts. The duration of the recycling phase also depends on the time required to ensure proper charge transfer between C_{rcy} and C_{peh}. In this implementation, this duration is configured to be equal to $2PW$ in order to enable the use of C_{rcy} greater than $2\mu F$. At the end of this charge transfer, a reset signal $SWRST$ is generated to reset both the counter (CNT) and charge recycling process.



(a)

(b)

Figure 4.8.: (a) D/B control sequence generator, (b) Charge recycling control circuit.

The rectification control circuit is shown in Figure 4.9. During each positive and

negative I_{peh} alternation, SW_1 and SW_2 signals are set to a high logic state, respectively to connect the positive terminal of the PT to the node V_{sp}, and the negative terminal to the ground. Furthermore during the damping and the shorting phases, both signals are set to low in order to disconnect C_L from C_{peh}. This prevents the spurious behavior of the AD comparator and ensures proper charge transfer from C_{peh} to the flipping capacitors during the damping phases. Hence, when the damping period begins, the rising edge of AD_{comp} sets the $Trig$ signal to high and thereby, both SW_1 and SW_2 signals go to low, which disconnects C_L from the PT.

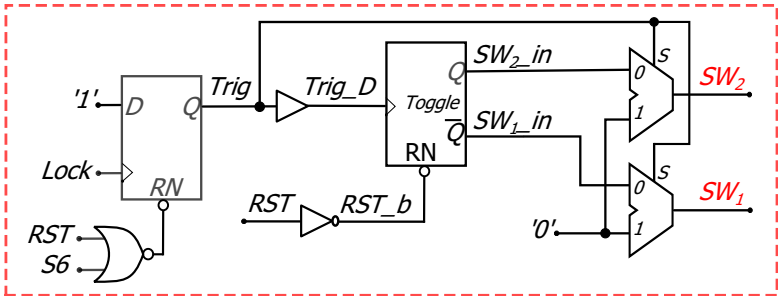


Figure 4.9.: Rectification control circuit.

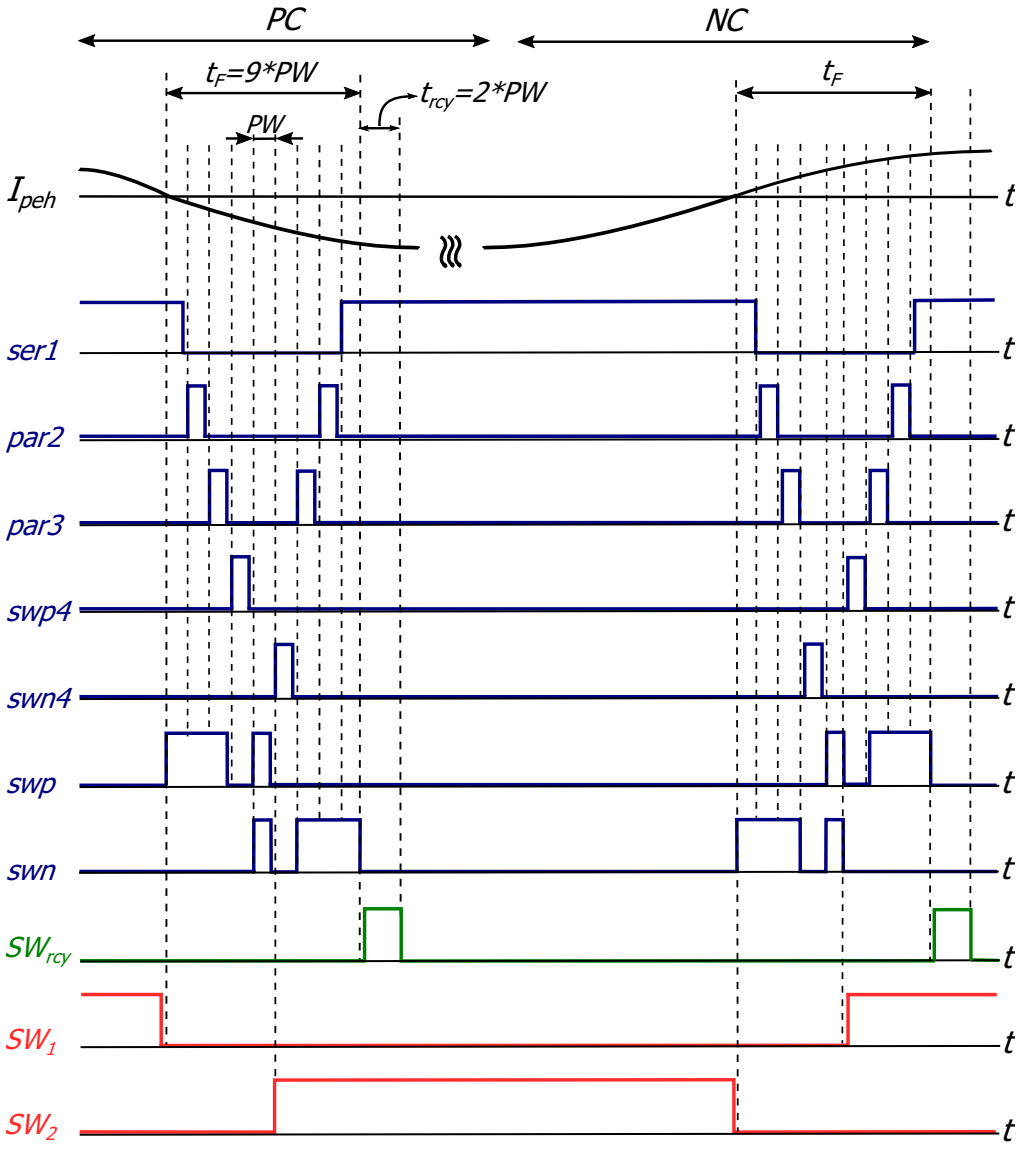


Figure 4.10.: Timing diagram of generated control signal sequence.

At the end of the damping period, signal Trig is set to low, and then both SW_1 and SW_2 are multiplexed to SW_1_in and SW_2_in, respectively. The later are the outputs of a toggle clocked by signal the delayed $Trig$ signal, i.e. $Trig\_D$. This delay between $Trig$ and $Trig\_D$ signals is important to ensure the propagation of the low logic state to both SW_1 and SW_2 when signal $Trig$ goes high. Signal RST_int also resets the rectification process by setting low signal Lock until the next voltage flip operation. Figure 4.10 shows the timing diagram of the non-overlapping control signals generated by the sequence generator, recycling control and rectification control circuits.

A high impedance state is imposed at node V_{sp} during the damping period i.e. when PT and C_L are disconnected. This in turn forces AD_{comp} to go low, turning on the PMOS switch of the AD that should stay off until the V_{peh} inversion terminates. To avoid this phenomenon, the PMOS switch of the AD is controlled by signal $ADctrl$ (Figure 4.6).

To ensure proper switching functionality of all the TGs and other (PMOS) switches used in the architecture, a switching drivers block (SD) is implemented. This block consists of level-up shifters (LSs) blocks required to drive all the control signals mentioned above. The LS block has the same circuit architecture of that implemented in FAR/FAR-CR (see chapter 3 (Figure 3.17)). In this implementation, GND (i.e. $0V$) for logic level $'0'$, and $V_{DDH} = 3V$ for logic level $'1'$ are chosen to drive the switches. This choice covers the voltage ranges of all switches nodes and respects the absolute maximum allowed V_{gs} and V_{ds} for the selected transistors in $0.35\mu m$ HV CMOS process used for this implementation.

To provide the voltage V_{DDH}, a charge pump proposed in [9] is implemented (Figure 4.11).

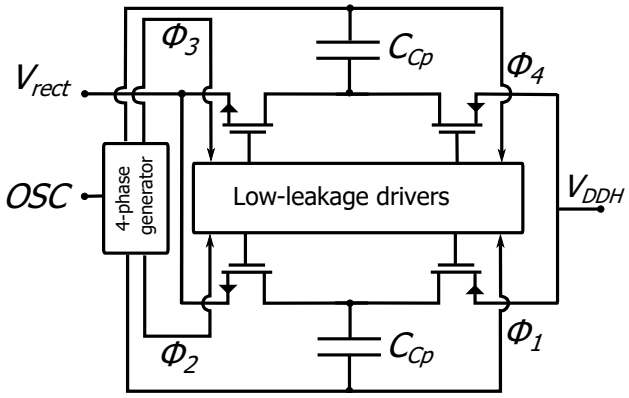


Figure 4.11.: Charge pump (CP) circuit architecture [9].

This charge pump is based on the Ker-cell design presented in [10] where the transistors in the cell are driven using a leakage driver. This minimizes the leakage current from the output to the input which is an issue in the case of low-voltage

energy harvesting. In addition to leakage driver, a 4-phase clock generator is also used to generate the out-of-phase clock signals required for each stage from the ring oscillator (RO) clock signal, i.e. OSC signal. As the output voltage of the CP does not exceed $3.3V$, the available low voltage C_{POLY} capacitors are used.

4.6. Transistor-level simulation results

The FAR-FC interface circuit is designed in AMS $0.35\mu m$ HV CMOS technology. Simulations were performed using Cadence®. In these simulations, the same PT device with $C_{peh} = 100nF$ used with FAR/FAR-CR, is also used with FAR-FC and configured to operate under the same operating conditions, i.e. $\hat{I}_{peh} = 62.8\mu A$, $f_{ex} = 100Hz$ to get $\hat{V}_{oc} = 1V$, which corresponds to a low mechanical excitation. A relatively low storage capacitor $C_L = 100\mu F$ is used in order to reduce the simulation time, while this capacitor in the harvesting system is a supercapacitor. Also, this capacitor, i.e. C_L, is pre-charged with $V_{rect} = 1.2V$, which is sufficient to activate the FAR-FC interface. Furthermore, in order to evaluate the power improvement of the FAR-FC circuit compared with the state-of-the-art SSHC circuit presented in [7], the later is also simulated under the same FAR-FC operating conditions. To make a fair comparison, three parallel flipping capacitors are used in the state-of-the-art SSHC circuit to flip the voltage across the PT, which is the same number of FAR-FC flipping capacitors. Figure 4.12 shows the architecture of the simulated three capacitor SSHC (3cap-SSHC) circuit.

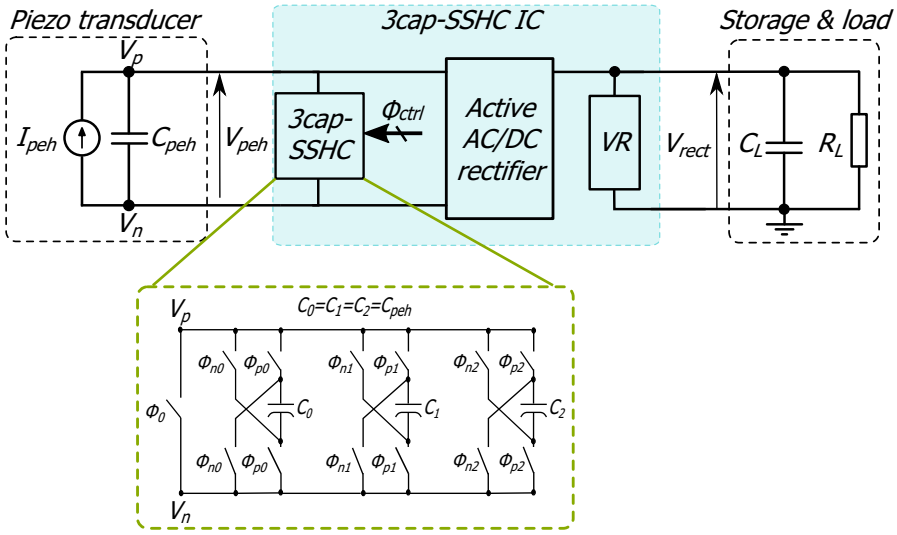
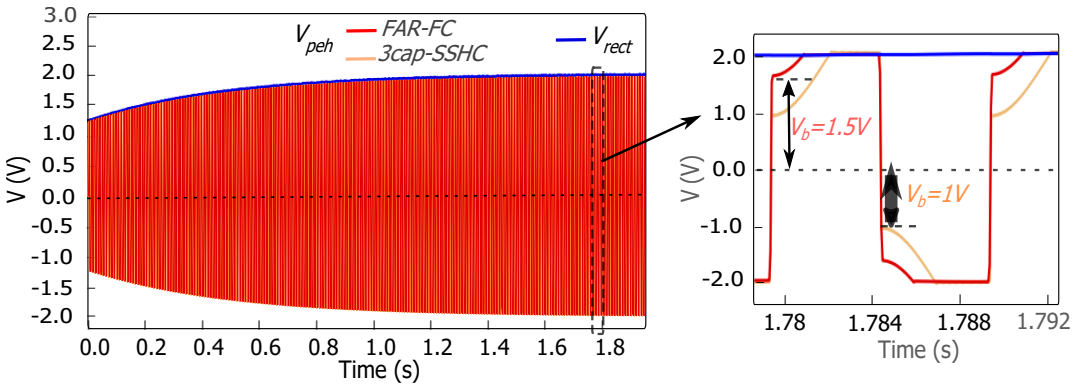


Figure 4.12.: 3cap-SSHC simulated circuit ($C_{peh} = 100nF, \hat{I}_{peh} = 62.8\mu A, f_{ex} = 100Hz, C_L = 100\mu F, R_L = 1T$).

Both FAR-FC and 3cap-SSHC circuits were first simulated without the output volt-

age regulation in order to get the maximum V_b value and then determine the reference voltage of the VR that ensures the optimal operating conditions.



$810mV$, which yields a maximum output power of $39.48\mu W$. In addition, the simulations also confirm that FAR-FC has a relatively high voltage flip efficiency, about 90.6%, compared to the 80% voltage flip efficiency achieved by 3cap-SSHC circuit according to (4.8).

Since the maximum output power extracted by a non-ideal FBR in presence of CMOS diodes ($V_{th} = 0.3V$) is $1.6\mu W$ according to equation (4.8), the $MOPIR$ of the FAR-FC circuit thus goes up to 28 according to equation (4.19).

Furthermore, enabling the charge recycling via SW_{rcy} switch every time V_{rect} slightly exceeds $1.6V$ helps in charging C_{rcy}, i.e. increasing V_{rcy}, and thus in flipping the voltage across the C_{peh} as shown in Figure 4.14. However, before the voltage regulation process, no charge recycling is performed. Thereby, the voltage across C_{rcy} remains constant and equal to its initial value ($1.2V$ in this simulation). The zoom view shows that in steady state, V_b can achieve a maximum amplitude that is very close to V_{rect} which corresponds to a voltage flip efficiency close to 99.6%. This in turn increases the conduction time of the active rectifier. As a result, the maximum extracted power to $64.44\mu W$ and the $MOPIR$ to 40.28.

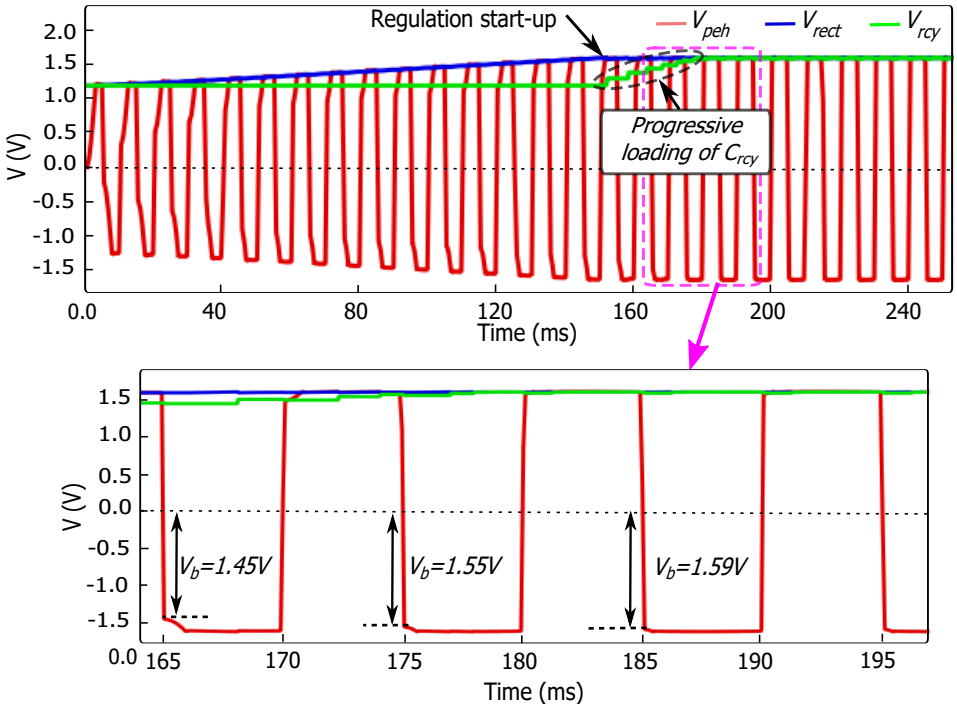


Figure 4.14.: Simulated V_{peh}, V_{rect} and V_{rcy} when using a C_{rcy} of $2\mu F$ pre-charged with $V_{rcy} = 1.2V$ in FAR-FC circuit.

Figure 4.15 depicts the simulated I_{peh}, V_{peh} and the key control signal AD_{comp}. As in the case of the basic FAR circuit, the I_{peh} zero crossing moment is detected 30µs earlier due to the negative offset of the AD comparator (zoom view).

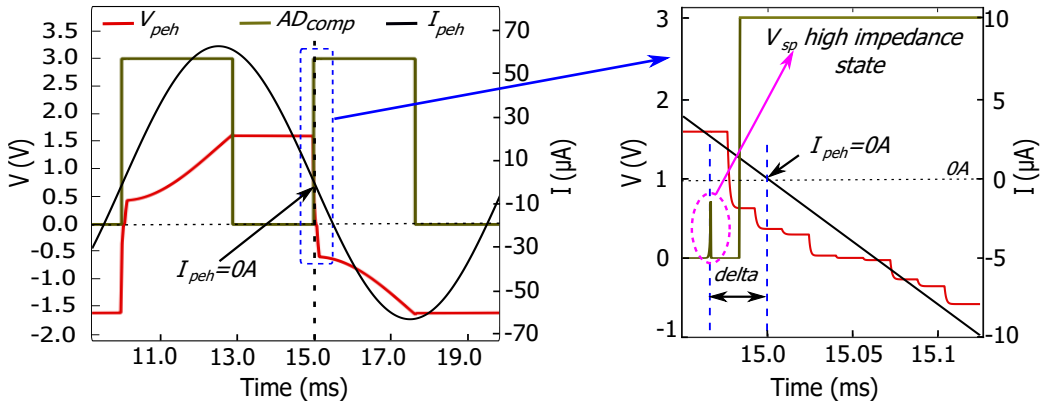


Figure 4.15.: Simulated I_{peh}, V_{peh} and the AD output voltage AD_{comp} in FAR-FC circuit.

This figure also shows that, in the FAR-FC circuit, after the I_{peh} zero-crossing detection, signal AD_{comp} returns again to zero. This is due to the high impedance state imposed on the V_{sp} node after disconnecting this node from both C_L and C_{peh} during the damping phases. Therefore, node V_{sp} is connected to the ground and the AD is blocked during the voltage flip operation. This prevents the AD comparator from being instable, which significantly increases its power consumption and affects the system efficiency.

Table 4.2.: Simulated power consumption of FAR-FC blocks.

Block	Power loss	percentage
Switches+AD+VR	2.08µW	50.12%
SD	110.2nW	2.65%
CP	1.27µW	30.6%
VR12	485nW	11.71%
CTRL	144nW	3.47%
RO	60nW	1.45%

Table 4.2 lists the simulated power consumption of the different blocks of FAR-FC interface circuit. The total consumption is $4.15\mu W$ representing 7.62% of the total extracted power. This leads to a system efficiency of 92.38%. Compared to the an SSHC circuit presented in [98], FAR-FC employs only three flipping capacitors to achieves this power efficiency, which is slightly higher than that achieved by [98], i.e. 91.5%. However, in [98], eight flipping capacitors are employed to flip the voltage

across the PT. Also, the employed PT has a low capacitance of $10nF$, and operates under relatively high excitation level, i.e. $\hat{V}_{oc} = 3.4V$. In [97], where $\hat{V}_{oc} = 1.02V$, the system needs to use one capacitor in addition to an inductor of $100\mu H$ to achieve a power efficiency of 83%, which is lower than FAR-FC's power efficiency.

4.7. Measurement results and discussion

As mentioned in chapter 3, the FAR-FC circuit can be experimentally tested and evaluated using the same full active rectifier (FAR) prototype, which was designed and fabricated in AMS $0.35\mu m$ HV CMOS technology. Also, the same cantilevered piezoelectric transducer with $C_{peh} = 100nF$ is used in the FAR-FC experiments. During the measurement, an AC power source (Agilent®6813B) was used to generate a $100Hz$ sine waveform excitation signal to excite the LDS®V400 shaker. A Labview plateform was also used in these experiments to control the shaker and allow the signal acquisitions via a Tektronix®TDS oscilloscope. The PT acceleration was set to get $\hat{V}_{oc} = 1V$, and both a conventional capacitor $C_L = 100\mu F$ and a supercapacitor[2] were used as a storage capacitor. The three capacitors of the Damping/Building system mentioned in section 4.3 in addition to the two capacitors (C_{DDL}, C_{rcy}) with $10\mu F$ capacitance value for voltage regulation requirements were off-chip implemented. Furthermore, the CTRL block can be configured in FAR-FC with and without the charge recycling modes in addition to the basic FAR mode.

The performance of the main part of the FAR-FC system, consisting of D/B, active AC/DC rectifier, VR, and CTRL blocks is evaluated. It should be noted that, in this evaluation, an external stable power supply is used to provide this part with the voltages $V_{DDL} = 1.2V$, $V_{DDH} = 3V$. Figure 4.16 (a) shows the measured waveform of V_{rect} and V_{peh} without and with charge recycling. As V_{rect} is regulated to $1.6V$, when the charge recycling is deactivated, the voltage across C_{peh} is $V_b = 1.24V$ after the voltage inversion operation. This corresponds to 88.75% voltage flip efficiency, which is lower than the simulated value. This is due to the series resistance of the employed switches in addition to all parasitic capacitances of interconnections between the PT and the test board which increase the RC time constant and thus, the charge loss. However, applying the charge recycling after the voltage flip operation increases V_b to $1.59V$ as shown in Figure 4.16 (a). This value can be achieved only in steady state, when there is charge excess, and $V_{rcy} \simeq V_{rect}$, i.e. when the load device is not in the active mode operation. In this case the voltage flip efficiency increases to 99.6%. The zoom view shows the detailed evolution of V_{peh} during the 9-phase voltage flip (Figure 4.16 (b)), in addition to charge recycling phase (Figure 4.16 (c)). Without the charge recycling, there is a charge loss due to recharging the C_{peh} from $V_b = 1.24V$ to V_{rect} (Figure 4.16 (b)). When the charge recycling is activated, i.e. $V_{rcy} > V_{rect}$, the higher V_{rcy}, the higher V_b, i.e. the lower charge loss, and thus the higher extracted power.

[2]Thales experimental supercapacitor.

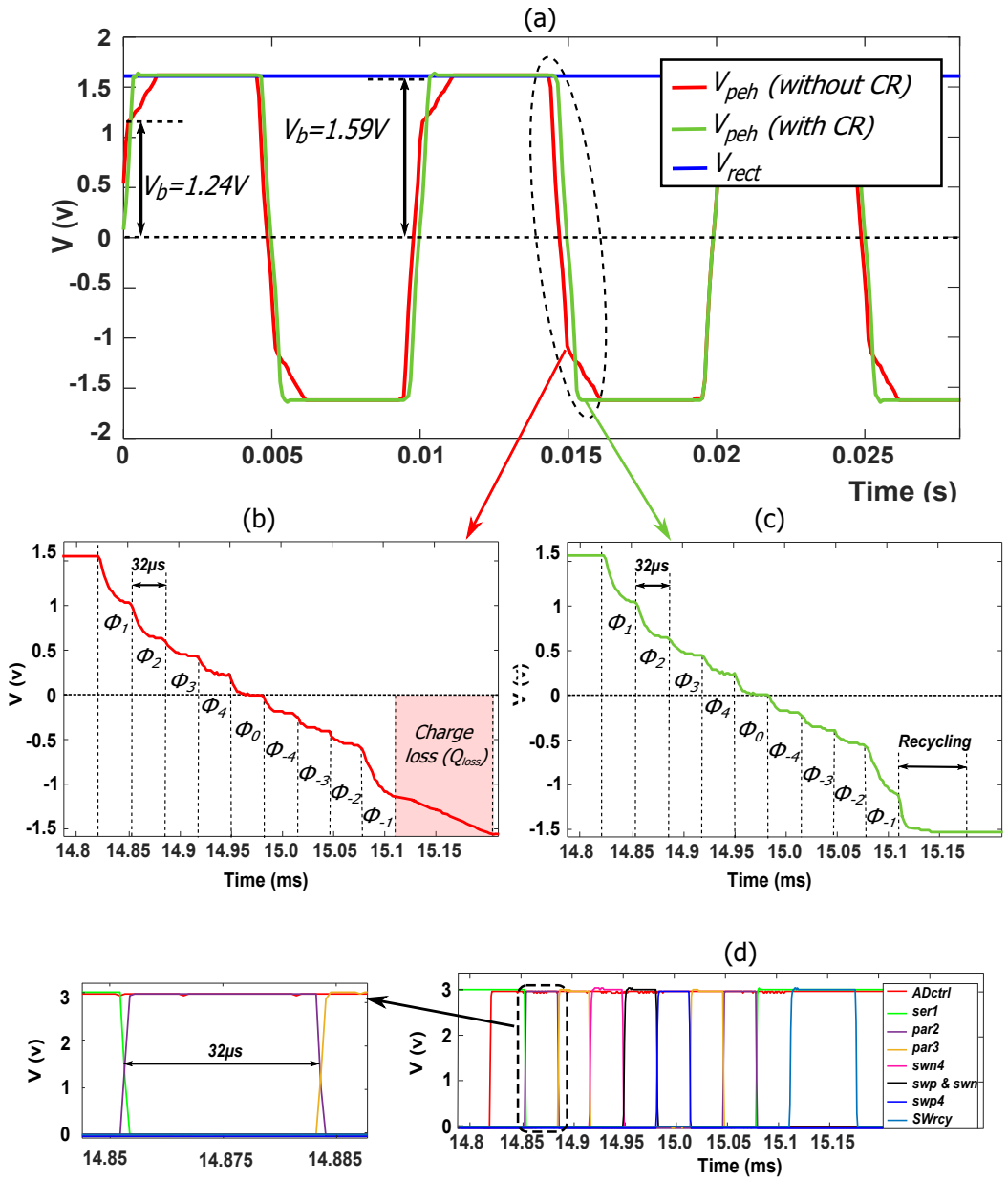


Figure 4.16.: Measured waveform of V_{peh} and V_{rect} with and without the excess charge recycling (a, b, c), in addition to the sequence of the control signals during the V_{peh} invesion operation (d).

The phase duration PW is set to $32\mu s$. This value is empirically determined to achieve the optimal power and voltage efficiencies mentioned above. Figure 4.16 (d) shows the sequence of the 9-phase control signals in addition to the control signal of the charge recycling phase.

The FAR-FC performance is evaluated by measuring the extracted power. For this experiment, the voltage regulator (VR) is deactivated and a variable resistor is connected to the FAR-FC output. Figure 4.17 shows the output power for different

V_{rect} values of FAR-FC, basic FAR in addition a Schottky-diode based FBR, which is implemented off-chip. The measured threshold voltage of the Schottky diode is around $(Vth \approx 0.05V)$[3]. This yields a maximum output power of $7.98\mu W$ when $V_{rect} = 0.4V$ (Figure 4.17). The maximum output power achieved by the FAR-FC is $45\mu W$ when $V_{rect} = 1.55V$. The slight difference between the simulated and the measured output power is due to charge losses in the wires and the test circuit. This output power yields a $MOPIR$ of 5.64. Compared to the FAR, the FAR-FC can extract 2.25x more power.

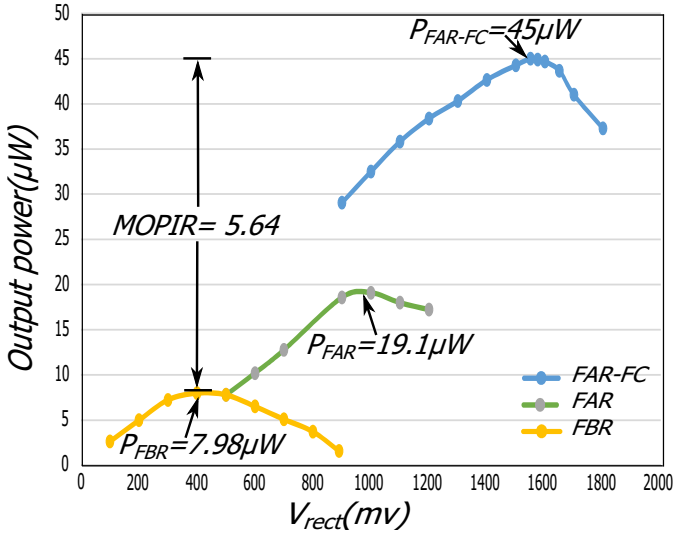


Figure 4.17.: Output power of FAR-FC, basic FAR and FBR interface circuits.

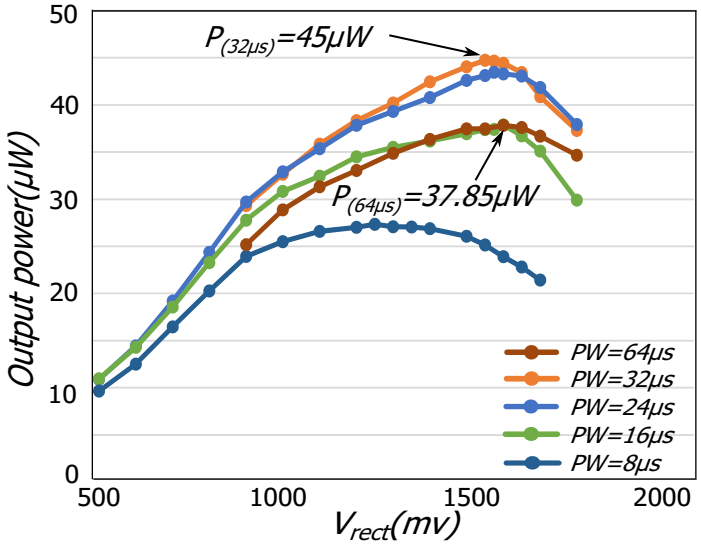


Figure 4.18.: FAR-FC output power for different PW phase pulse widths.

[3]The low threshold voltage is related to low conducting current

The FAR-FC performance is also evaluated for different pulse widths as shown in Figure 4.18. Measurement results confirm that the best power performance is achieved when PW is increased to $32\mu s$. However, increasing the pulse width to more than $32\mu s$ reduces the conduction time and thus the extracted output power.

The FAR-FC output power is also measured when the mechanical excitation level of the PT is slightly increased, inducing an open circuit voltage $\hat{V}_{oc} = 1.25V$.

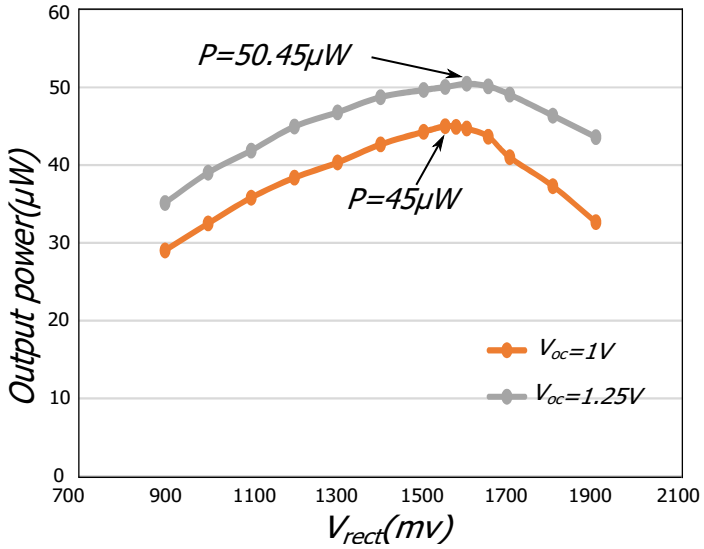


Figure 4.19.: FAR-FC output power for $\hat{V}_{oc} = 1V$, and $\hat{V}_{oc} = 1.25V$.

Measurement results in Figure 4.19 show that for this increase, the maximum extracted power leaps from $45\mu W$ to $50.45\mu W$ at $V_{rect} = 1.6V$. This corresponds to 12% improvement in both peak output power and circuit performance. Measurement results also show that the FAR-FC circuit cannot extract power when $V_{rect} > 1.9V$ (Figure 4.19). In fact, energy harvesting starts when $\hat{V}_{peh} = V_{ds(TG)} + V_{ds(AD-PMOS)} + V_{drop(R)} + V_{rect}$, where, $V_{ds(TG)} = 14mV$ is the voltage drop across the TG switch that connects PT to the node V_{sp}, and $V_{ds(AD-PMOS)} = 12mV$ is the source-drain voltage of the PMOS switch in the AD (see chapter 3 (section 3.5)). $V_{drop(R)}$ denotes the voltage drop resulted from all parasitic resistance on the current path. This voltage can be calculated as $V_{drop(R)} = \hat{V}_{pehmax} - (V_{ds(TG)} + V_{ds(AD-PMOS)} - V_{rectmax})$. In this implementation, as the CMOS circuit is not designed to work with voltages higher than $V_{DDH} = 3V$, the maximum PT voltage amplitude, i.e. $\hat{V}_{peh}$, with which the FAR-FC can operate is $2V$. Therefore, $V_{drop(R)}$ is equal to $74mV$. When $\hat{V}_{peh} \geq 2V$, i.e. $V_{rect} > 1.9V$, the TG switches connected to the PT terminals can't be controlled properly and the FAR-FC stops working.

Table. 4.3 summarizes the key characteristics and the performance of the FAR-FC chip compared with the reported state-of-the-art architectures. As the FAR-FC circuit cannot operate when increasing the PT output voltage up to $2V$ and most

Table 4.3.: FAR-FC performance compared to the state of the art.

Publication	Wu et al. [108]	Du et al. [7]	Du et al. [109]	Chen et al. [96]	Ciftci et al. [97]	**This work**
Year	2017	2017	2019	2019	2021	**2022**
CMOS technology	0.25µm	0.35µm	0.18µm	0.18µm	0.18µm	**0.35**µm
Harvesting technique	SSHI	SSHC	SSHC	SPFCR	SSHCI	**SSHC**
f_{ex} (Hz)	144	92	219	200	415	**100**
C_{peh} (nF)	19	45	1.94	22	2	**100**
Key components	Inductor	8 capacitors	8 capacitors	4 capacitors	Inductor + Capacitor	**3 capacitors**
Number of phases	-	17	17	21	-	**9**
Voc (V)	4.9	2.5	2.5	1.6	2.75-1.02	**1-1.25**
Output power (µW)	136	161.8	16.1	64	24.2-4.7	**45-50.45**
$MOPIR$	2.1	9.7	8.2	9.3	4.03-5.44	**5.64-6.32**

interface circuits presented in the literature report $\hat{V}_{oc}$ higher than $1V$ (Table 4.3), it is thus difficult to make a fair comparison with our work. However, [97] shows the output power when $\hat{V}_{oc} \simeq 1V$. As shown in this table, the maximum extracted power in [97] significantly decreases from $24.2\mu W$ to $4.7\mu W$ when the $\hat{V}_{oc}$ decreases from $2.75V$ to $1.02V$. In contrast, the FAR-FC circuit can extract $45\mu W$, which is 9.5**x** higher than the maximum power extracted by [97]. This table also shows that the FAR-FC circuit can work with a high PT inherent capacitance value, i.e. $100nF$, while the value reported in the state-of-the-art circuits is lower than $50nF$. In particular, SSHC architectures that require a large number of phases [108], [7], [109] need to keep C_{peh} as low as possible to limit the RC constant that reduces the voltage flipping speed. The enhanced architecture of FAR-FC, combining the reduced 9-phase flipping process and the reduced maximum number of series switches (i.e. 3) in the D/B array, alleviates the constraint on the C_{peh} compared to other works and extends the variety of the PTs compatible with the proposed energy harvesting interface.

Although measurement results confirm that both CP and VR12 can provide $V_{DDH} = 3V$ and $V_{DDL} = 1.2V$, respectively as shown in Figure 4.20, the maximum V_b that can be achieved is only $900mV$. Also, the measured output power decreases from $45\mu W$ to $30\mu W$ at $V_{rect} = 1.3V$ as shown in Figure 4.21. This performance degradation is due to the using the CP architecture proposed in [9]. This simulated model does not take into account the parasitic capacitors through the current path. This affects the non-overlapping signals generated by the leakage drivers leading to the increase

of the total consumption of the CP.

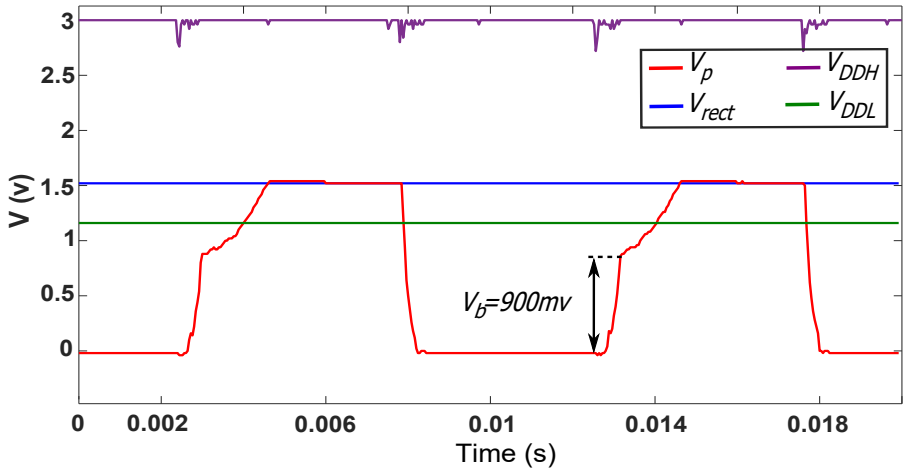


Figure 4.20.: Measured CP output voltage (V_{DDH}) and VR12 output voltage (V_{DDL}) in addition to $V_{rect}$and positive V_{peh}, i.e. V_p .

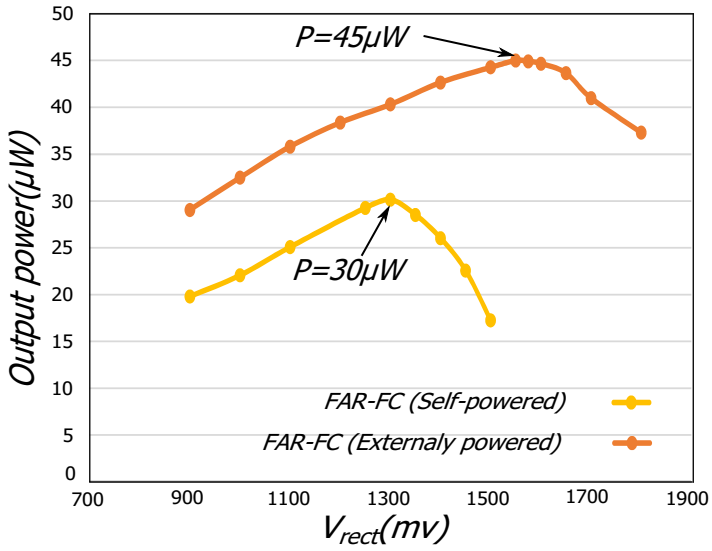


Figure 4.21.: Self and non-self powered FAR-FC output power.

Measurement results in Figure 4.21 also shows that, for V_{rect} lower than $0.9V$, the FAR-FC can't operate. In fact, for this value of V_{rect}, the output voltage of the CP is only $1.8V$, which is not sufficient to properly drive the TGs switches in this technology.

4.8. Conclusion

This chapter introduced an optimized SSHC interface circuit (FAR-FC) for piezoelectric energy harvesting. While the reported state-of-the-art architectures use either a large inductor (SSHI) or a large number of flipping capacitors/phases (SSHC), the FAR-FC employs only three flipping capacitors to achieve high power efficiency. Simulation results show that the FAR-FC improves the voltage flip efficiency of the conventional three capacitor SSHC circuit by 10.6% compared to the state-of-the-art three-capacitor SSHC circuit. This yields 37.91% maximum output power improvement. Moreover, measurement results show that the FAR-FC circuit can deliver up to $45\mu W$ with 88.75% voltage flip efficiency when $\hat{V}_{oc}$ is only $1V$, while most of state-of-the-art work report $\hat{V}_{oc} > 2V$. This ensures sufficient energy harvesting even under tight operation conditions, i.e. when the PT is weakly excited. Measurement results also show that a little increase of 25% in $\hat{V}_{oc}$, yields 12% peak output power improvement. Furthermore, its optimized architecture allows the proposed FAR-FC circuit to be used with a wide range of PT capacitance values, i.e. up to $100nF$ or more. Moreover, the FAR-FC can extract 2.25x more power than that extracted by the basic FAR circuit presented in the previous chapter. It also achieves a power performance of 5.64x compared to the non-ideal FBR. Also, using the charge recycling in FAR-FC circuit can significantly improve the voltage flip efficiency in steady state when there is excess charge. However, disabling the charge recycling when a load is connected to the output prevents the use of the charge that can be left in the recycling capacitor. This decreases the voltage flip efficiency and the power extraction time. This point will be taken into account in the next chapter.

The main limitation of the FAR-FC is related to the voltage used for controlling the TG switches, i.e. $V_{DDH} = 3V$, which makes dealing with high input mechanical energy sources impossible. Also, the circuit has been designed to achieve the maximum power efficiency only for a given value of $\hat{V}_{oc}$ (in this case $\hat{V}_{oc} = 1V$). However, in real PT operating conditions,$\hat{V}_{oc}$ may fluctuate and V_{rect} needs to be adjustable to enable maximum power extraction whatever the value of $\hat{V}_{oc}$.

This limitation will be addressed in the next chapter by designing a dynamic FAR-FC able to deal with different mechanical excitation levels of the PT (i.e. different values of $\hat{V}_{oc}$). Furthermore, in the improved version, a more efficient charge recycling is achieved. Also a standard architecture of a charge pump (CP) will be implemented to solve the power consumption problem of the CP circuit implemented in this version, which significantly reduced the delivered power to the load.

5. Improved Dynamic FAR-FC Interface Circuit

5.1. Introduction

As shown in the previous chapter, the FAR-FC interface circuit was designed to extract the maximum energy generated by the PT when the latter has an open circuit voltage of $1V$, i.e. $\hat{V}_{oc} = 1V$. The maximum power extraction was achieved thanks to the voltage regulator (VR) whose voltage reference is set to a fixed value that ensures extracting the optimal power when $\hat{V}_{oc} = 1V$. However, when $\hat{V}_{oc} \neq 1V$, the extracted output power and thus the performance of the FAR-FC decreases. Furthermore, the maximum $\hat{V}_{oc}$, with which the FAR-FC can operate is $2V$. This is due to the FAR-FC design technology that limits the maximum voltage allowed for the circuit safe operation to $3V$. This chapter introduces an improved version of the FAR-FC interface circuit that can achieve a maximum output power even $\hat{V}_{oc}$ fluctuates according to the mechanical excitation. Furthermore, the issue of dealing with PT open circuit voltages higher than $2V$ is resolved. Also, a standard charge pump architecture is used in this circuit to solve the consumption problem that occurred on the previous version proposed in [9]. Moreover, in the improved FAR-FC circuit, an efficient excess charge recycling is performed in order to decrease the charge loss and increase the system efficiency. The chapter is organized as follows: section 5.2 presents the improved FAR-FC architecture with the detailed analysis of the improved and new blocks. Section 5.3 provides and discusses the simulation results. An off-chip circuit is proposed in section 5.4 to address the issue of power extraction under high PT mechanical excitation levels. Finally, section 5.5 concludes this chapter.

5.2. Improved FAR-FC interface circuit topology and design analysis

Figure 5.1 depicts the circuit diagram of the improved FAR-FC system. It is mainly composed of a Damping/Building capacitors array (D/B), an active AC/DC rectifier, a maximum power point tracking (MPPT) circuit, a power management circuit (PM), and a DC/DC converter and a control block (CTRL). In addition to theses

main blocks, a ring oscillator (RO) and level-up shifters (LS) are also used. As in the first FAR-FC prototype presented in the previous chapter, the D/B block is used to efficiently flip the voltage across the PT while the active AC/DC rectifier is used to rectify this voltage. The extracted power in this system is first stored in a temporary

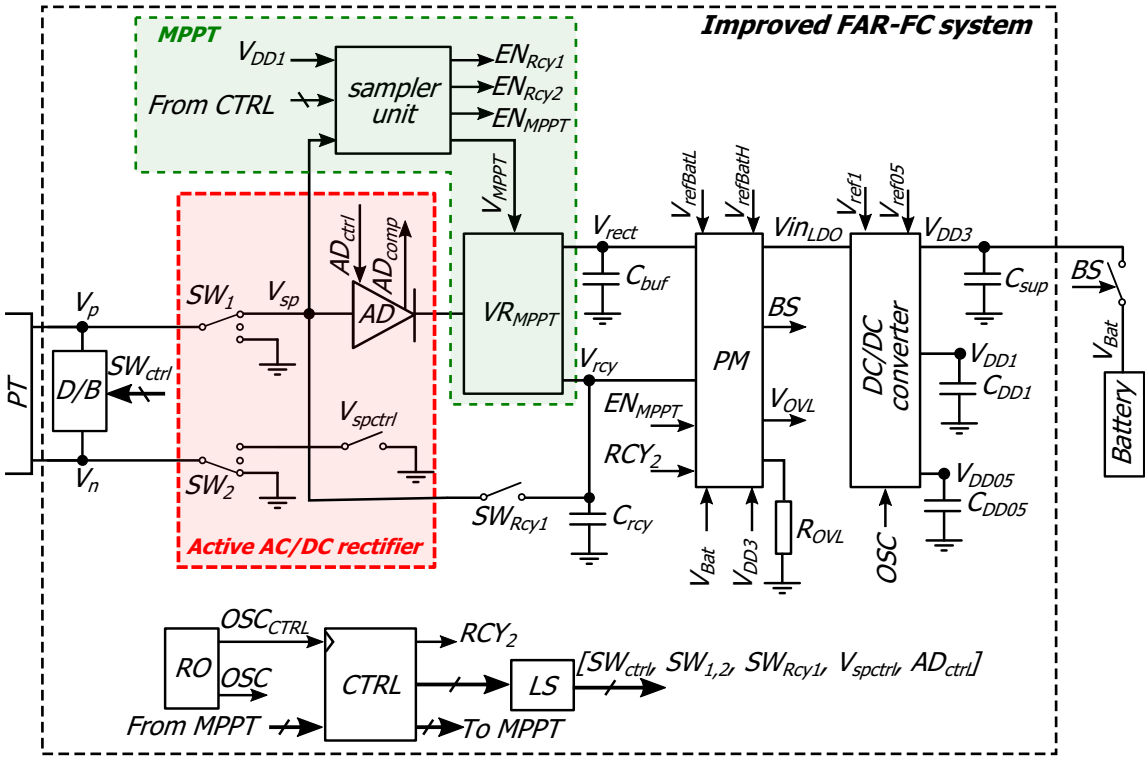


Figure 5.1.: System architecture of improved FAR-FC interface circuit.

capacitor C_{buf}, which is also used as a buffer that allows V_{rect} to adapt in function to $\hat{V}_{oc}$. Adjusting V_{rect} according to $\hat{V}_{oc}$ is achieved thanks to the MPPT circuit. An excess charge may be resulted after each MPPT process. This excess charge is stored C_{rcy}. The PM circuit is used to manage the use of the charge stored in C_{buf} and C_{rcy} for creating the V_{DD1} in the DC/DC converter. It is also used for the overload protection and to ensure the full charge of the battery. The DC/DC converter is used to provide the improved FAR-FC with different DC voltages, i.e. V_{DD3}, V_{DD1}, V_{DD05} required to supply the different blocks and charge the battery. The CTRL block is used to generate the control signals needed to invert and rectify the voltage across the PT in addition to perform the C_{rcy} charge recycling. Each of these signals is then shifted using level-up shifter block (LS) in order to ensure the proper control of the switches. The ring oscillator is used to generate the required clock signals. The following subsections present the newly added blocks in this system, i.e. the MPPT, the PM and the DC/DC converter, in addition to all modifications applied to the other blocks in order to enhance the FAR-FC performance.

5.2.1. Damping/Building capacitors array (D/B) and active AC/DC rectifier

Both D/B (Figure 5.2) and active AC/DC rectifier (Figure 5.1) blocks have the same circuit diagram of that used in the first FAR-FC prototype (Chapter 4 (section 4.5)). However, some modifications explained in the following have been applied to the circuit implementation of blocks.

As the voltages across the TG switches in the D/B circuit are not well defined and follow the variation of $\hat{V}_{oc}$, i.e. the changes in the mechanical excitation of the PT, the bulk wiring of each TG MOSFET transistor to one of its drain and source terminals may form forward bulk diodes. This hinders the proper charge transfer between the C_{peh} and the flipping capacitors leading to a failure of the SSHC technique. In order to avoid the occurrence of forward bulk diodes in the TG's transistors, a bulk regulation (BR) block is connected to each TG switch. Figure 5.2 shows the D/B block with the improved TGs switches.

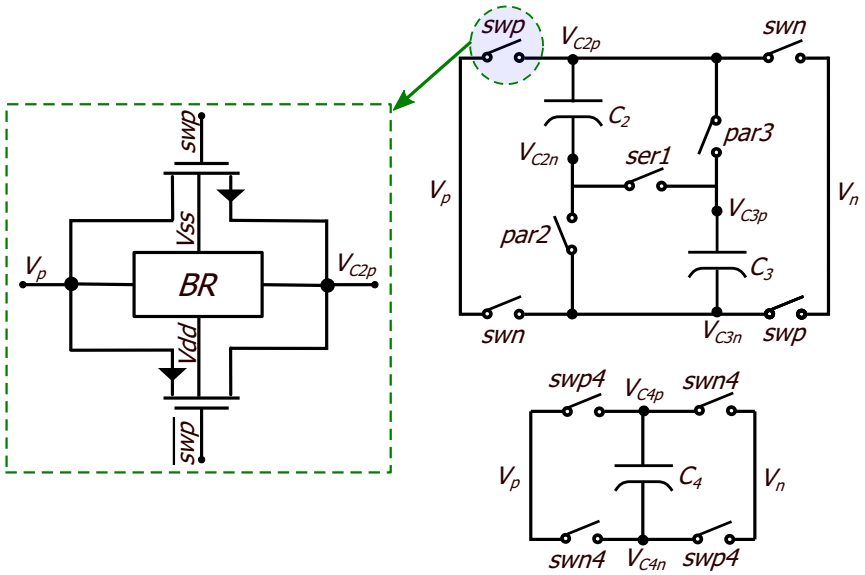


Figure 5.2.: The D/B block with the improved TG switches.

In order to explain why the bulk regulation is important, let's consider switch *swp* as an example (Figure 5.2). This switch connects the positive terminals of both PT and capacitor C_2. Figure 5.3 shows the *swp* switch circuit and the bulk diodes (BD) in both NMOS and PMOS transistors during the conducting period. Lets assume that the PT is exposed to a stable mechanical excitation, i.e $\hat{V}_{oc}$ is constant. At the beginning of the damping period, $V_p > V_{C2p}$. This implies that the bulk of the NMOS and PMOS transistors should be connected to V_{C2p} and V_P, respectively, as shown in Figure 5.3. Turning on this switch to start the PT voltage flip operation forms a current path from the PT to C_2, i.e. from V_P to V_{C2p}. The bulk diodes

in this case are fully blocked and no leakage current can pass from C_2 to C_{peh}, i.e. $I_q = 0A$ as shown in Figure 5.3.

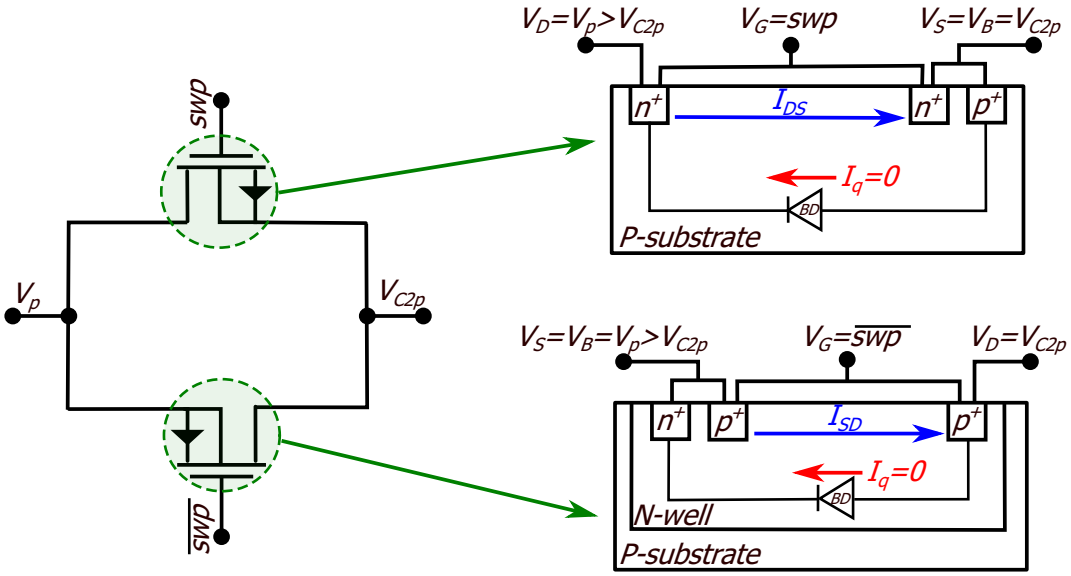


Figure 5.3.: *swp* switch without bulk regulation and the bulk diodes (BD) in both NMOS and PMOS transistors during the conducting period.

However, in real operation conditions, the PT mechanical excitation can be vary leading to V_P lower than V_{C2p}. This leads to the formation of a reverse current path during the *swp* conducting period, i.e. $I_q > 0A$, which prevents proper charge transfer during the PT voltage flip operation.

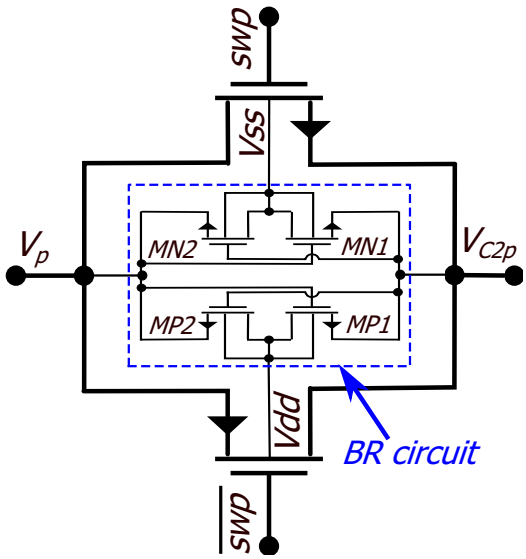


Figure 5.4.: *swp* switch with bulk regulation (BR) circuit.

Connecting the BR block to this switch as shown in Figure 5.4 allows to dynamically connect the bulk of both NMOS and PMOS transistors to the lower and higher TG terminals voltages, respectively. When $V_p > V_{C2p}$, $MN1$ is turned on, connecting the bulk of the NMOS transistor in *swp* switch to the V_{C2p}, i.e. to the lower voltage. In the meantime, $MP2$ is turned on, connecting the bulk of the PMOS transistor in *swp* switch to the V_P, i.e. to the higher voltage. Conversely, when $V_p < V_{C2p}$, $MN2$ is turned on, connecting the bulk of the NMOS transistor in *swp* switch to the V_P, i.e. to the lower voltage. In the meantime, $MP1$ is turned on, connecting the bulk of the PMOS transistor in *swp* switch to V_{C2p}, i.e. to the higher voltage.

For similar reasons, the same bulk regulation circuit was added to the PMOS switch in the active diode. This is critical in terms of energy harvesting efficiency because it prevents discharging C_{buf} in C_{peh} when AD is ON and $\hat{V}_{oc}$ decreases, leading to V_{sp} lower than V_{rect}. It also prevents discharging C_{buf} through ground during the damping period, when AD is OFF and V_{sp} is connected to ground.

In this improved version, the AD common-source comparator (CS) of the active AC/DC rectifier is replaced with a common-gate comparator (CG) [8]. Figure 5.5 shows the CG comparator circuit with its current biasing circuit. Unlike CS comparator which requires a stable power supply, i.e. $3V$ in the first prototype, the CG comparator is supplied by its positive input, i.e. V_{rect}. This allows to reduce the power consumption when $V_{rect} < 3V$. Furthermore, the reduction of the biasing current from $100nA$ in the CS comparator to $5.5nA$ in the CG comparator significantly decreases the power consumption. Also, with the CG comparator, the AD allows the PT to charge the C_{buf} when V_{rect} reaches $700mV$, while charging C_L with the first prototype, i.e. with the common-source comparator, requires a voltage supply of $3V$, i.e. a V_{rect} of $1.6V$.

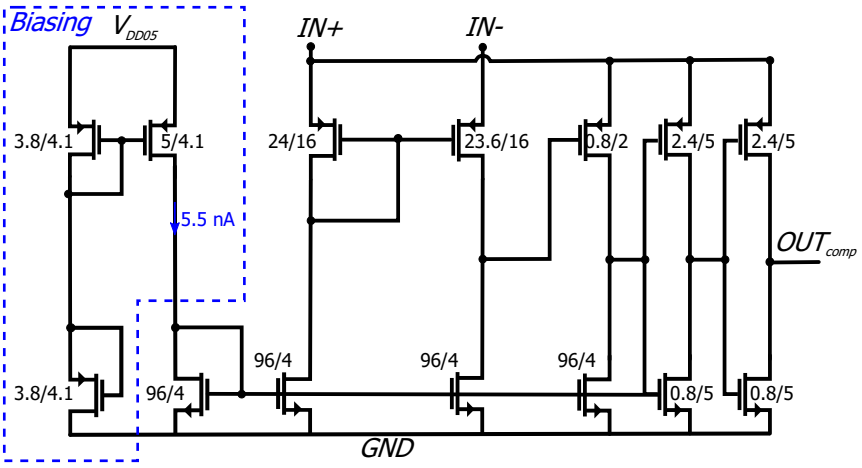


Figure 5.5.: Common gate comparator circuit with its biasing circuit.

5.2.2. Maximum output power tracking circuit (MPPT)

As shown in Figure 5.1, this block is connected between node V_{sp} and the temporary storage capacitor C_{buf}. It consists of a voltage regulator (VR_{MPPT}) and a sampler unit. Unlike the voltage regulator (VR) in the first FAR-FC circuit, which is provided with a fixed voltage reference that enables the maximum power extraction when $\hat{V}_{oc} = 1V$, this voltage regulator has a dynamic voltage reference (V_{MPPT}) provided by the sampler unit. This ensures the maximum output power tracking even when $\hat{V}_{oc}$ varies. Furthermore, the excess charge resulting from the voltage regulation of the MPPT process is stored in a recycling capacitor C_{rcy} to be then used for either boosting the voltage across the C_{peh} after the voltage flip operation or creating the DC voltage V_{DD1}.

The operating principle and the detailed architecture of the MPPT circuit are not presented in this work. It is the topic of another research work, which is being conducted at the same time in the context of the same project. However, three main signals, EN_{Rcy1}, EN_{Rcy2} and EN_{MPPT} are generated by the sampler unit using specific signals generated by the control block (CTRL), not detailed in this work too. EN_{Rcy1} signal is used to enable the use of the excess charge in C_{rcy} when $V_{rcy} > V_b$ after the first MPPT process for boosting the voltage across C_{peh} at the end of the voltage flip operation. EN_{Rcy2} signal is used to enable the C_{rcy} charge recycling when $V_{rcy} > V_{DD1}$ for creating the V_{DD1} after the first MPPT process and during the normal FAR-FC operation mode, i.e. no MPPT process and no V_b voltage boosting. EN_{MPPT} signal enables the MPPT process for one half cycle of PT current. These previous signals are then used by CTRL block to generate the control signals required to perform the charge recycling process.

5.2.3. Power management circuit (PM)

This block is mandatory in the FAR-FC system. It allows the monitoring of the voltage levels at certain nodes in order to ensure both safe operation of the FAR-FC circuit and efficient use of the extracted power from the PT. Figure 5.6 depicts the architecture of this block. Two common gate comparators are used to monitor the battery voltage level V_{Bat}. When $V_{Bat} < V_{refBatL}$, the signal BS goes high to indicate the need of battery charging. However, when V_{Bat} exceeds $V_{refBatH}$, BS goes low indicating that the battery is fully charged. As shown in Figure 5.6, by means of two down-shifter (DS) blocks, the comparators output voltages, i.e. Out_{BatH} and Out_{BatL} are shifted down from the V_{Bat} to the voltage that supplies the next digital blocks, i.e. $V_{DD05} = 0.5V$. The values of $V_{refBatL}$,$V_{refBatH}$ depend on the voltage range of the employed battery. In this system a $3V$-lithium battery with a voltage rang of $(2.8V - 3V)$ will be used. Therefore, $V_{refBatL}$ and $V_{refBatH}$ values are set to be $2.8V$ and $3V$, respectively. Charging the battery is achieved using an external analog switch, which connects it with the supercapacitor C_{sup} as shown in Figure 5.1. The charge flow from C_{sup} to the battery is controlled by BS. When BS is $'1'$,

the switch is turned on to charge the battery up to $3V$. In turn, when the battery is charged, BS goes low and the switch turns off.

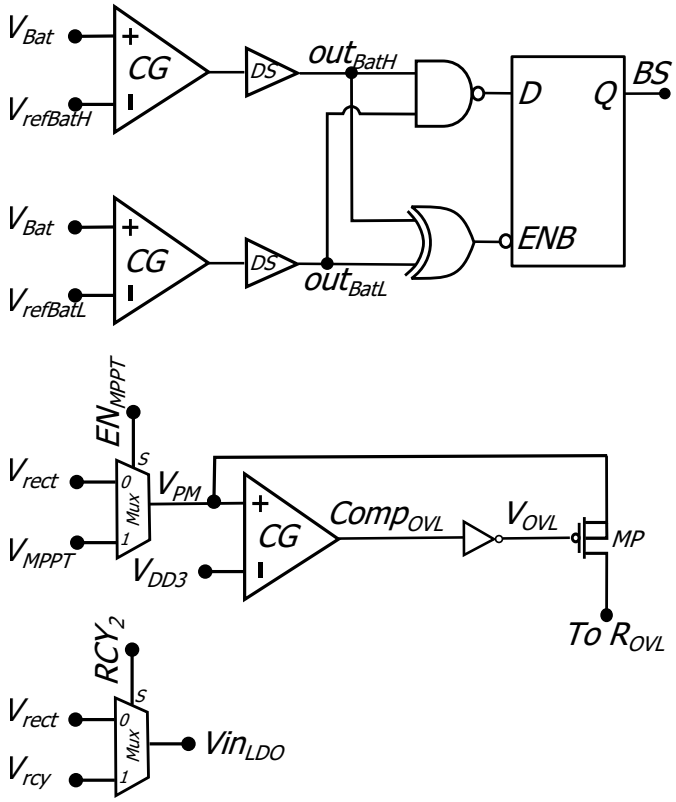


Figure 5.6.: Power management (PM) circuit architecture.

In order to protect the circuit from the overload consequences, the rectified voltage V_{rect} should be permanently monitored. However, during the MPPT operation mode, C_{buf} is disconnected from PT and the PT is set in an open circuit configuration in order to evaluate the new voltage reference (V_{MPPT}). High PT mechanical excitation level results a V_{MPPT} voltage that may can't be supported by the FAR-FC circuit leading to destroy it. Therefore, to ensure the circuit protection during all FAR-FC operation modes, a common gate comparator is used to monitor either the voltage V_{rect} across C_{buf} during the normal operation or the voltage V_{MPPT} during the MPPT operation. The selection between these two voltages is achieved using an analog multiplexer controlled by the signal EN_{MPPT}. The selected voltage V_{PM} is compared with the voltage V_{DD3}. This voltage is set with respect to the maximum voltage supported by the technology used to design this circuit, i.e. ONSemi $0.18\mu m$ CMOS technology. The maximum V_{ds} and V_{gs} voltages supported in this technology are both $3.65V$. For the safe circuit operation, the maximum voltage V_{DD3} is chosen to be $3V$. When $V_{PM} > 3V$, the comparator output $Comp_{OVL}$ goes high, i.e the signal V_{OVL} goes low, to turn on the PMOS switch (MP) in order to sink the excess charge through the ground via an external resistor R_{OVL}. It should be noted that

the use of the analog multiplexer contributes to the reduction of the circuit volume and power consumption by reusing the same comparators during the phases when they would not be used.

As there is a high probability that V_{rcy} exceeds $1V$, i.e. $RCY_2 =' 1'$, during the normal operation mode, an additional analog multiplexer is used to allow the use of V_{rcy} instead of V_{rect} as a voltage source, i.e.Vin_{LDO} of the DC/DC converter. This makes C_{rcy} the primary charge storage capacitor instead of C_{buf} that is only used as a charge buffer and no longer as a storage capacity as in the previous architectures, which represents a fundamental change in this circuit.

5.2.4. DC/DC converter and level-up shifter block (LS)

This block provides the FAR-FC circuit with the various DC voltages required as power supplies. As shown in Figure 5.7, it is composed of a linear voltage regulator (LDO) [8] and a standard charge pump (CP) [10, 110, 111]. The LDO creates the two low DC supply voltages of the circuit, $V_{DD1} = 1V$ and $V_{DD05} = 0.5V$, while the CP generates it with the high DC voltage $V_{DD3} = 3V$, from V_{DD1}.

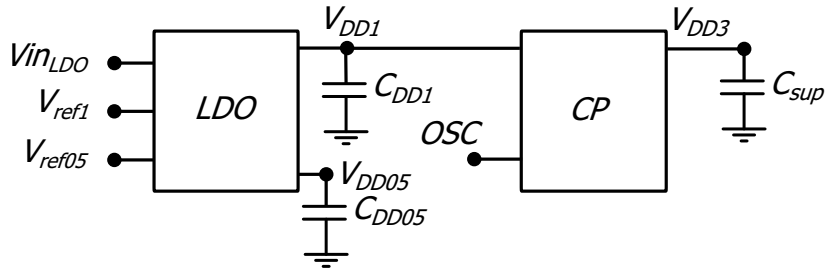


Figure 5.7.: DC/DC converter circuit diagram.

Figure 5.8 shows the circuit architecture of the LDO block. As mentioned before, the V_{DD1} is created form the voltage Vin_{LDO}, which can be either V_{rect} or V_{rcy}. This voltage is then used to supply all level shifters in the circuit and create the voltages V_{DD3} and V_{DD05}. V_{DD05} is used for powering the control block (CTRL), the ring oscillator (RO), the current biasing circuits and the level shifters used in LS block.

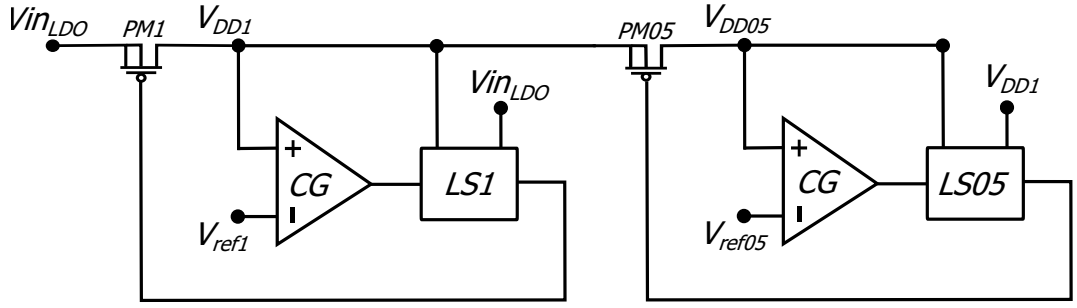


Figure 5.8.: LDO circuit architecture.

As shown in Figure 5.8, two different voltage level-up shifters, LS1 and LS05, are used in order to fully turn OFF the PMOS transistor switches $PM1$ and $PM05$ used for creating V_{DD1} and V_{DD05}, respectively. Using one shifting stage, the LS1 shifts V_{DD1} is to Vin_{LDO}, and the LS05 shifts V_{DD05} to V_{DD1}.Figure 5.9 shows the both LS1 (left) and LS05 (right) circuits architecture. In the LS1 circuit, two types of transistors, $MOS_{1.8V}$, $MOS_{3.3V}$, available in this technology are used.

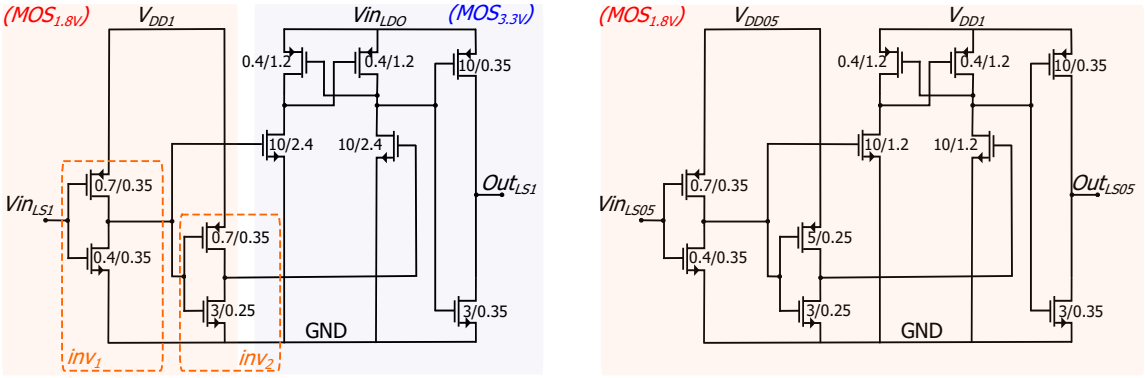


Figure 5.9.: (left) LS1 and (right) LS05 typologies.

Table 5.1 shows the main operation parameters of each type of these transistors.

Table 5.1.: $MOS_{1.8V}$ and $MOS_{3.3V}$ transistors parameters.

MOS transistor	$V_{th}(mV)$	$Vds_{max}(V)$	$Vgs_{max}(V)$
$NMOS_{1.8V}$	476	2	2
$PMOS_{1.8V}$	-505	-2	-2
$NMOS_{3.3V}$	765	3.65	3.65
$PMOS_{3.3V}$	673	-3.65	-3.65

The $|V_{th}|$ of the $MOS_{1.8V}$ transistors is lower than that in $MOS_{3.3V}$ transistors. Therefore, better driving of both inverters,inv_1 and inv_2, can be achieved when the $MOS_{1.8V}$ transistors are used to to design them. However, these transistors are not used in the other part of the circuit which is powered by Vin_{LDO}. In fact, this voltage can reaches $3V$, leading to increase the $\mid Vgs \mid$ or/and the $\mid Vds \mid$ of the $MOS_{1.8V}$ transistors to a value greater than that can be supported, i.e. $2V$. The same architecture is used in LS05. However, as the voltage V_{DD05} should be shifted to V_{DD1} , only one type of transistors can be used which is $MOS_{1.8V}$ .The simulated power consumption of LS1 and LS05 circuits are $43.12pW$ and $38pW$, respectively.

Unlike the CP block that was used in the first FAR-FC prototype [9], the circuit architecture of the implemented CP in the improved prototype is based on a standard

charge pump [10,110,111], without the use of the leakage drivers. Figure 5.10 shows the circuit architecture of two-stage standard CP.

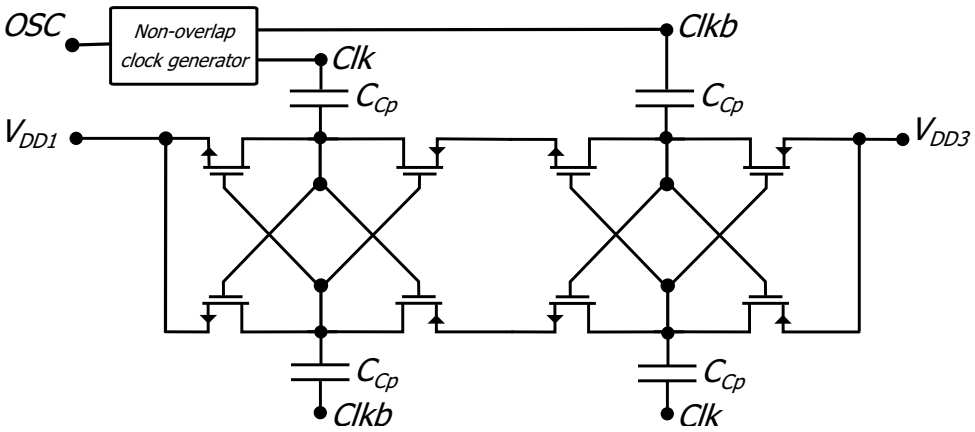


Figure 5.10.: Two-stage standard CP circuit architecture [10].

In this version, the frequency of the clock signal OSC is increased to from $250kHz$ (in the first version) to $1MHz$ in order to provide the required current to power all the blocks while maintaining output voltage of the charge pump at 3V, i.e. to ensure sufficient output power. To generate OSC, the ring oscillator (RO) that was used in the first version is redesigned to output the clock signal with frequency of $1MHz$. With this frequency, the charge pump can deliver $20\mu A$ with an output voltage of $V_{DD3} = 3V$. This voltage is sufficient to fully turn ON/OFF the TG transistors with respect to the maximum allowed voltage in this technology, i.e. $3.65V$. The power efficiency of this charge pump is 56.1%.

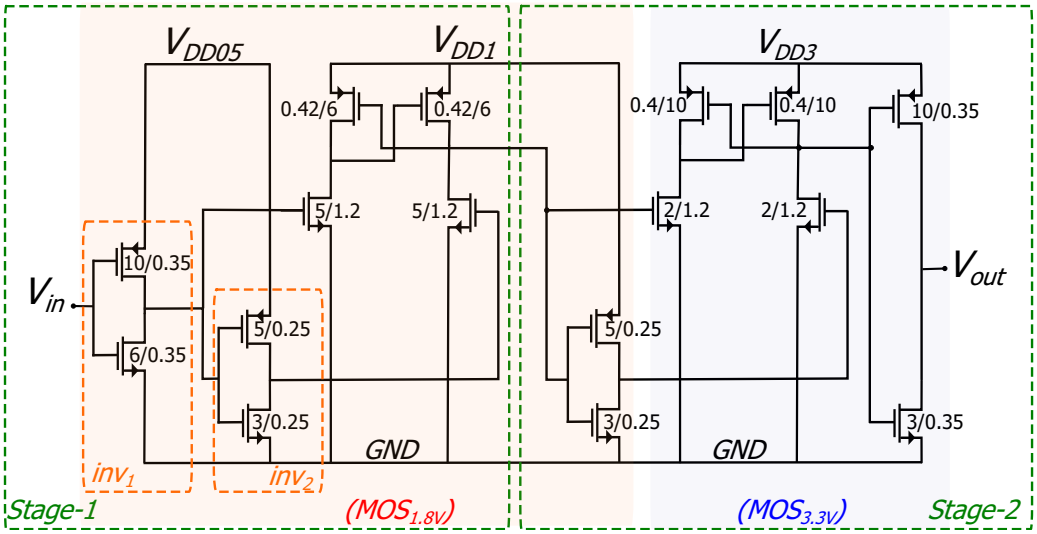


Figure 5.11.: Level-up shifter (LS) topology.

In order to fully turn ON/OFF the employed switches, each of the generated control signals, except signal RCY_2, are shifted up from $V_{DD05} = 0.5V$ to $V_{DD3} = 3V$ by means of the level-up shifters circuit (LS). The circuit diagram of the LS is shown in Figure 5.11. As in the LS1 circuit, the two transistors types, $MOS_{1.8V}$ and $MOS_{3.3V}$ are used in this circuit for the similar reasons. As shown in Figure 5.11, the inverters outputs are connected to the $NMOS$ transistors gates. The high logic state output of either inv_1 or inv_2 corresponds to a voltage value very close to V_{DD05}. As this value is lower than the V_{th} of the $NMOS_{3.3V}$ transistors and higher than the V_{th} of the $NMOS_{1.8V}$ transistors, V_{DD05} can't be shifted directly to V_{DD3} and an additional shifting stage is necessary to first shift V_{DD05} to $V_{DD1} = 1V$, which is then shifted to V_{DD3}.

The power consumption of this LS circuit depends on the frequency of its input signal and the gate capacitance of the driven switch. However, in the case of shifting a control signal that has a maximum frequency , i.e.$400Hz$, such as $par2$, $par3$, the simulated power consumption of a LS is only $12.16nW$.

5.2.5. Control block (CTRL)

This block is used to generate all system control signals, i.e. D/B, active AC/DC rectifier, charge recycling and MPPT control signals. Figure 5.12 shows the circuit diagram of the control block. As the D/B and the active AC/DC rectifier blocks in the improved FAR-FC have the same architectures of those used in the first FAR-FC prototype, no modifications have been applied on the rectification control and sequence generator circuits. The control signals that are used to control the MPPT circuit are not presented in this work. The modified charge recycling control is detailed below.

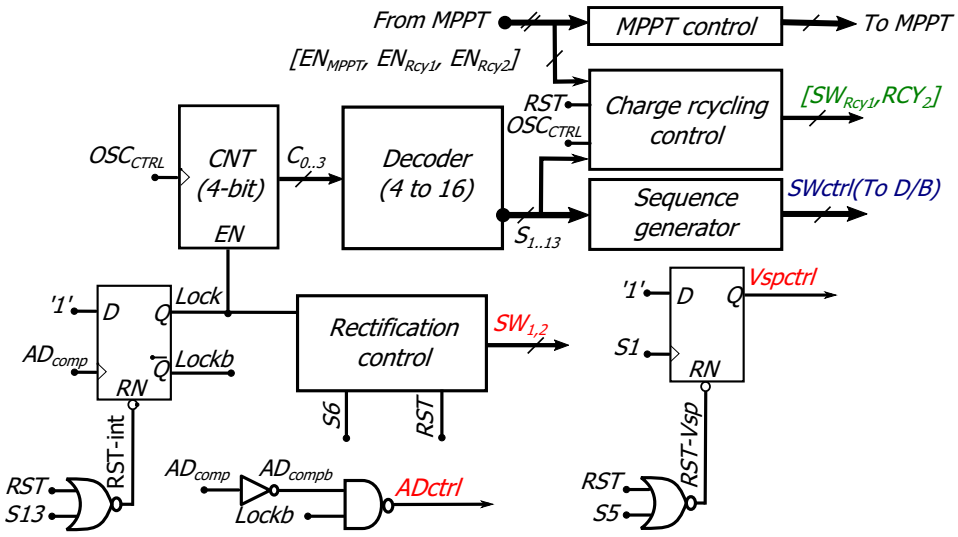


Figure 5.12.: Control block (CTRL) circuit diagram.

Figure 5.13 depicts the charge recycling control circuit. Using the signals generated by the MPPT block, i.e. EN_{Rcy1}, EN_{Rcy2}, EN_{MPPT}, this block can generate the two signals required to achieve an efficient C_{rcy} charge recycling.

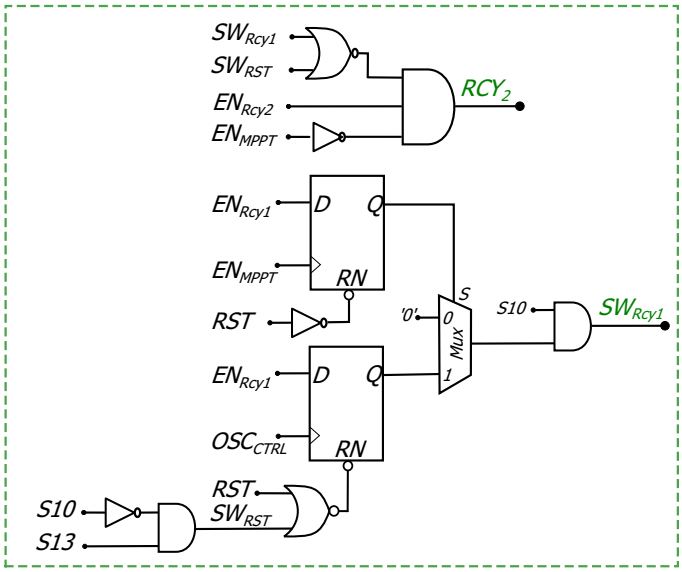


Figure 5.13.: Charge recycling control circuit.

The first one is SW_{Rcy1} signal used to control the use of C_{rcy} charge for boosting the voltage across the C_{peh}. After the first MPPT process, at the end of the C_{peh} voltage flip operation, signal SW_{Rcy1} goes high when signal EN_{Rcy1} is high, i.e. $V_{rcy} > V_b$, to allow the use of C_{rcy} charge in boosting the V_b and increasing the voltage flip efficiency. This process takes one clock duration and is reset by SW_{RST} signal. The second signal is RCY_2, which is used by the PM circuit in order to choose the DC/DC input voltage Vin_{LDO} to be then used for creating the V_{DD1} by the LDO block. In the normal operation mode, i.e. no MPPT process and no V_b boosting, when signal EN_{Rcy2} is high, i.e. $V_{rcy} > V_{DD1}$, signal RCY_2 becomes high. In this case, the PM chooses Vin_{LDO} to be V_{rcy}. Otherwise, V_{rect} is chosen by the PM block as Vin_{LDO}.

It should be noted that the CTRL block in this prototype is powered by an ultra low DC voltage $V_{DD05} = 0.5V$. This due to the 0.18µm $HV\ CMOS$ technology used for designing the improved FAR-FC, which allows the use of ultra low power digital blocks while these same blocks required at least $1.2V$ for proper operation when AMS 0.35µm $HV\ CMOS$ technology was used in the first FAR-FC. Although the CTRL block in the improved FAR-FC has additional digital blocks required for MPPT block, the power consumption of this block is reduced from $144nW$ in the first FAR-FC to $5.23nW$ in the improved FAR-FC leading to a significant decrease in the total power consumption.

5.3. Simulation results and discussion

As mentioned before, the improved FAR-FC prototype was designed in ONSemi $0.18\mu m$ CMOS technology. Figure 5.14 shows the layout of the improved FAR-FC including the different blocks.

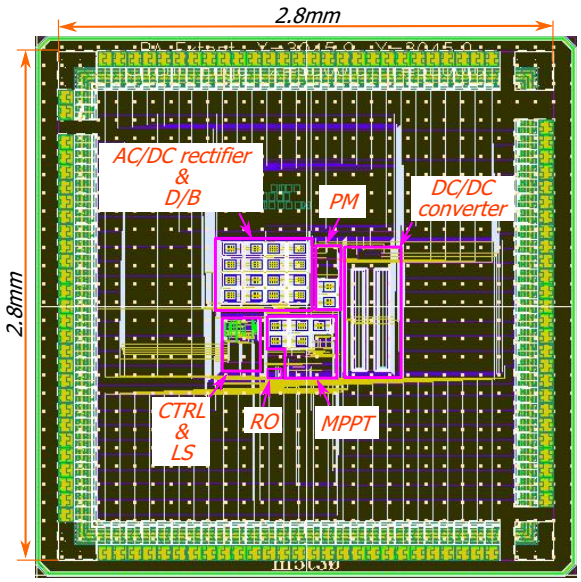


Figure 5.14.: Improved FAR-FC circuit layout designed in ONSemi $0.18\mu m$ CMOS technology.

Table 5.2.: Employed capacitors and associated voltages.

Capacitor	Capacitance value	Associated voltage	Initial voltage value
C_{buf}	$10\mu F$	V_{rect}	$1.2V$
C_{rcy}	$1\mu F$	V_{rcy}	$0.5V$
C_{DD05}	$1\mu F$	V_{DD05}	$0.5V$
C_{DD1}	$1\mu F$	V_{DD1}	$1V$
C_{sup}	$1mF$	V_{DD3}	$3V$

Simulations were performed at post-layout transistor level with Cadence®. In these simulations, the PT is modeled as a parasitic capacitor $C_{peh} = 100nF$ in parallel with a sinusoidal current source $I_{peh}(t)$. In real PT operation conditions, a change in the PT mechanical excitation level results a change in a PT current amplitude ($\hat{I}_{peh}$) and thus in the PT open circuit voltage ($\hat{V}_{oc}$). In order to simulate the system behavior in this case, the PT model current source, i.e. $I_{peh}(t)$, is configured in order

to have an open circuit voltage $\hat{V}_{oc} = 0.8V$, i.e. $\hat{I}_{peh} = 50.24\mu A$ and $f_{ex} = 100Hz$, during $70ms$, and then to have $\hat{V}_{oc} = 1V$, i.e. $\hat{I}_{peh} = 62.8\mu A$ and $f_{ex} = 100Hz$ for the rest of the simulation time. The values of the employed capacitors together with their respective initial voltage values are summarized in Table 5.2. These values are used for all simulations. The voltage reference V_{MPPT} of the MPPT regulator (VR_{MPPT}) is set to an initial value of $0.1V$.

Figure 5.15 shows the simulated PT current (I_{peh}) and the main signals of the improved FAR-FC. The MPPT principle has been validated by a $150ms$ transient simulation. For simulation optimization reasons, the MPPT block has been configured to trigger the MPPT process each eight I_{peh} zero-crossing event, i.e. three times during $150ms$, but for the real system operation conditions, the MPPT is triggered at larger intervals. The start and the end of the MPPT processes are marked as t_1, t_2, t_3, t_4, t_5, t_6 in the figure. Simulation results show that before t_1, V_{rect} increases in order to reach its maximum allowed value in this system, i.e. $3V$ and the overload protection trips. It also shows that, before the first MPPT process, SW_{Rcy1} is low preventing the use of C_{rcy} charge for boosting V_b. Furthermore, as $V_{rcy} < 1V$ before t_1, signal RCY_2 is low. This implies the use of V_{rect} by the voltage regulator LDO to recharge C_{DD1} to $V_{DD1} = 1V$, when the latter becomes lower than $1V$ as shown in the zoom view (a). As a result, V_{rcy} remains constant at its initial value, i.e. $0.5V$ until t_2. At the end of the first MPPT process, i.e. at t_2, a voltage reference V_{MPPT} is provided to VR_{MPPT} to ensure the maximum power extraction. As V_{MPPT} is lower than V_{rect}, the latter is decreased to reach the V_{MPPT} value, i.e. $1.14V$. This decrease is achieved by shedding charges from C_{buf} to C_{rcy}. As a result, V_{rcy} increases to the new value of V_{rect} as shown in the zoom view (b). Starting from t_2, $\hat{V}_{peh}$ also decreases to the new V_{rect} value. This value is kept constant by VR_{MPPT} until the next MPPT process. The variation in the $\hat{V}_{oc}$ from $0.8V$ to $1V$ occurred at $t = 70ms$ is detected by the followed MPPT process. Therefore, a new V_{MPPT} value of $1.36V$ is provided to VR_{MPPT}. Although $\hat{V}_{oc}$ didn't change after the second MPPT process, i.e. after t_4, a new V_{MPPT} value, higher than the previous one is provided at the end of the third MPPT process. This due to that the capacitors of the D/B block haven't yet reached their steady state at t_6 and the voltage V_b keeps on increasing. As in the first prototype simulations (see chapter 4 (Figure 4.13 (b))), in steady state, V_b becomes constant. This allows V_{MPPT} to achieves its optimal value ($1.75V$), which ensures the maximum power extraction when $\hat{V}_{oc} = 1V$ (see chapter 4 (section 4.6)). From Figure 5.15, it can be concluded that, thanks to the MPPT process, V_{rect} is adjusted according to the $\hat{V}_{oc}$ changes in order to optimize the performance of the FAR-FC. Simulation results also show that after each MPPT process, C_{rcy} charge is used for boosting V_b every time SW_{Rcy1} goes high. This boost helps V_{rect} to reach V_{MPPT} more quickly, especially when $V_{rect} < V_{MPPT}$. After each boost toV_b, C_{rcy} discharges, i.e. V_{rcy} decreases. However, C_{rcy} is recharges again each time V_{rect} exceeds V_{MPPT} between t_2 and t_3 as shown in the zoom view (c).

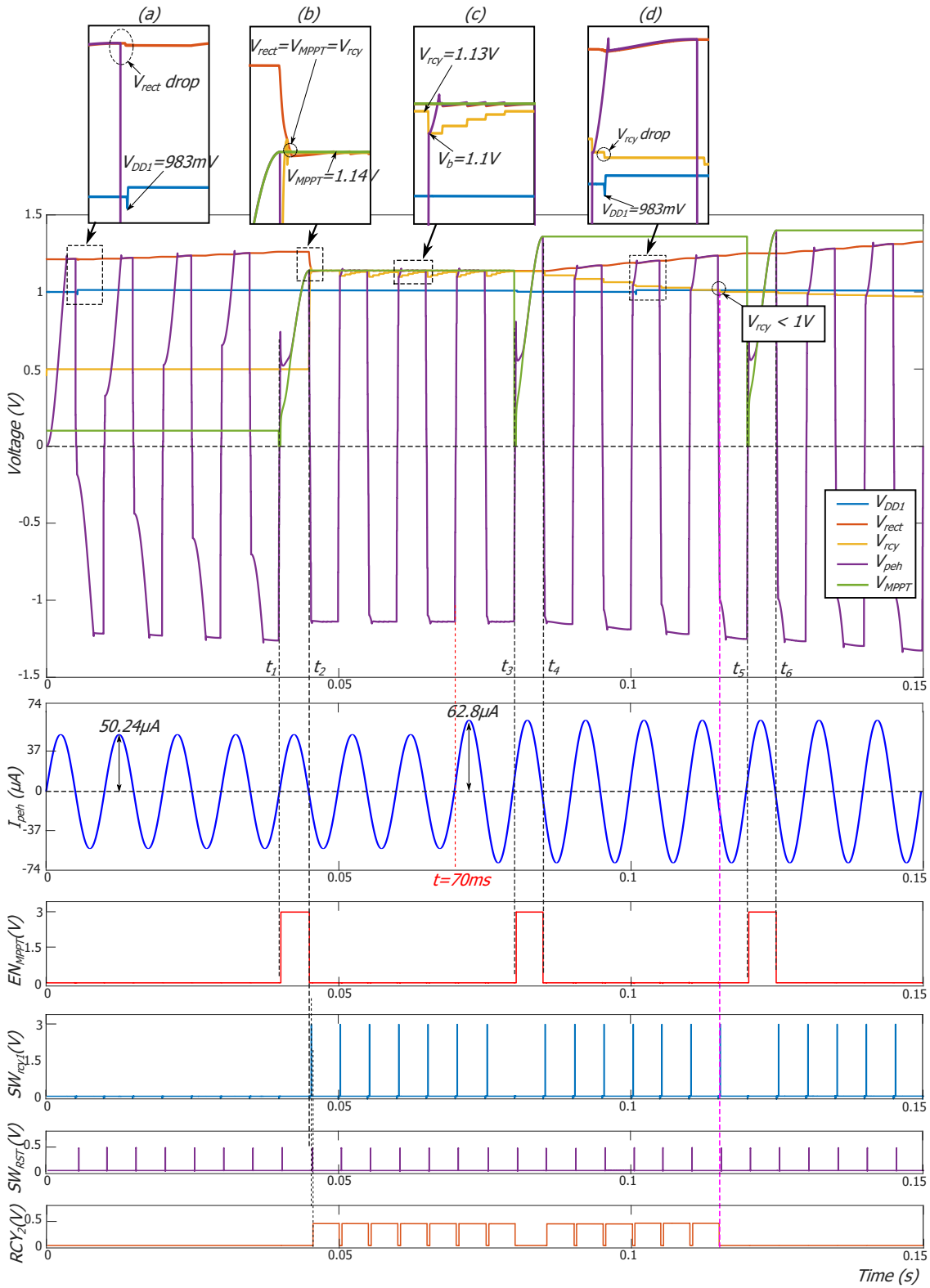


Figure 5.15.: Simulated I_{peh}, V_{peh}, V_{rect}, V_{MPPT} , V_{rcy} and V_{DD1} in addition to EN_{MPPT} and charge recycling control signals, i.e. SW_{rcy1}, SW_{RST} and RCY_2 signals.

Furthermore, when $V_{rcy} > 1V$, signal RCY_2 goes high to allow the use of the excess charge in C_{rcy} by the LDO during the normal operation mode as shown in the zoom view (d). However, this signal goes low each I_{peh} zero-crossing moment to give priority to the V_b boost and avoid discharging the D/B capacitors by the LDO. Simulation results also show that after t_4, V_{rcy} keeps on decreasing after each charge recycling process. This is because V_{rect} is lower than V_{MPPT}, which disables the recharging of C_{rcy}. When V_{rcy} becomes lower than $1V$, signal RCY_2 goes low to preventing the use C_{rcy} charge by the LDO as shown in Figure 5.15.

The battery charge monitoring achieved by the power management block is also simulated. For this simulation, a sinusoidal voltage source $V_{Bat}(t)$ is used for modeling the behavior of the battery. In this simulation, V_{Bat} fluctuates between $2.7V$ and $3.1V$. Also, voltages $V_{refBatH}$ and $V_{refBatL}$ are set to $3V$ and $2.8V$, respectively, in order to meet the voltage range of the battery that will be used in the future experiments. Figure 5.16 shows that, signal BS goes high when $V_{Bat} < 2.8V$ indicating the need of battery charging. Conversely, when V_{Bat} becomes higher than $V_{refBatH}$, i.e. $3V$, signal BS goes low to indicate that the battery is fully charged and there is no need to charge it from the supercapacitor C_{sup}.

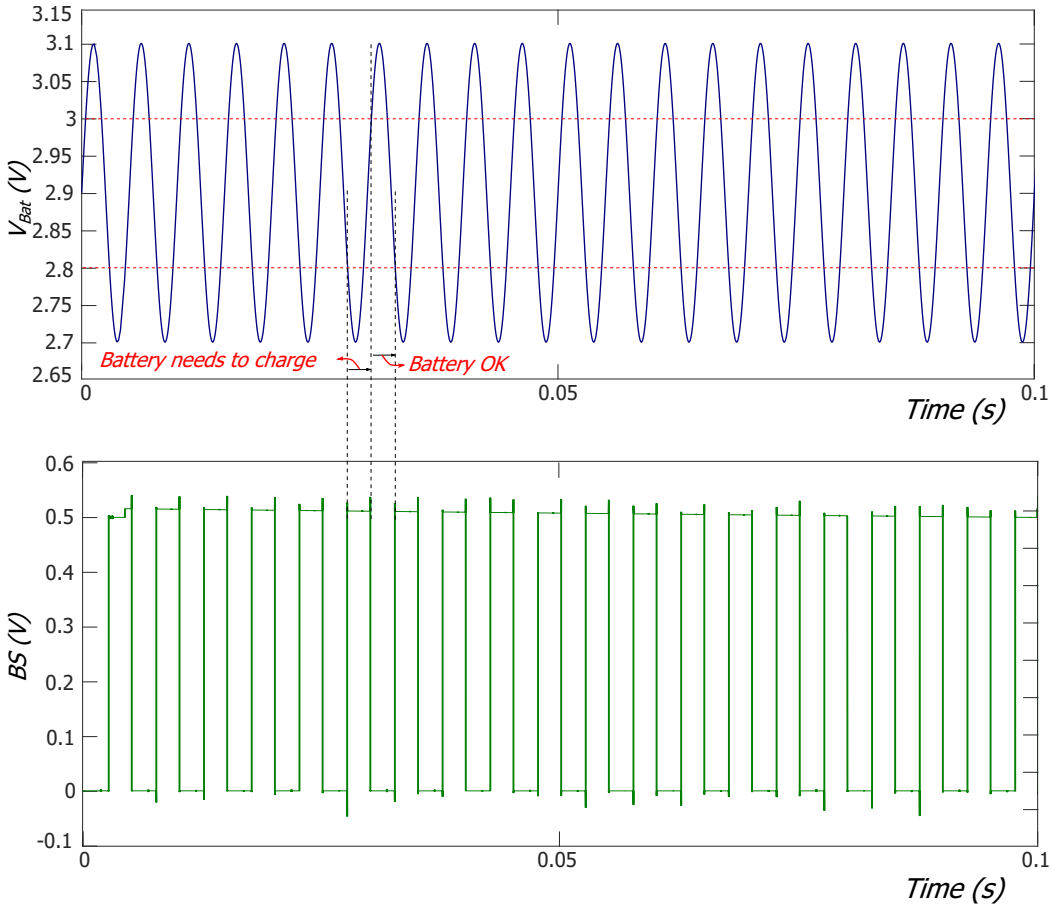


Figure 5.16.: Simulation result of the PM battery charge monitoring.

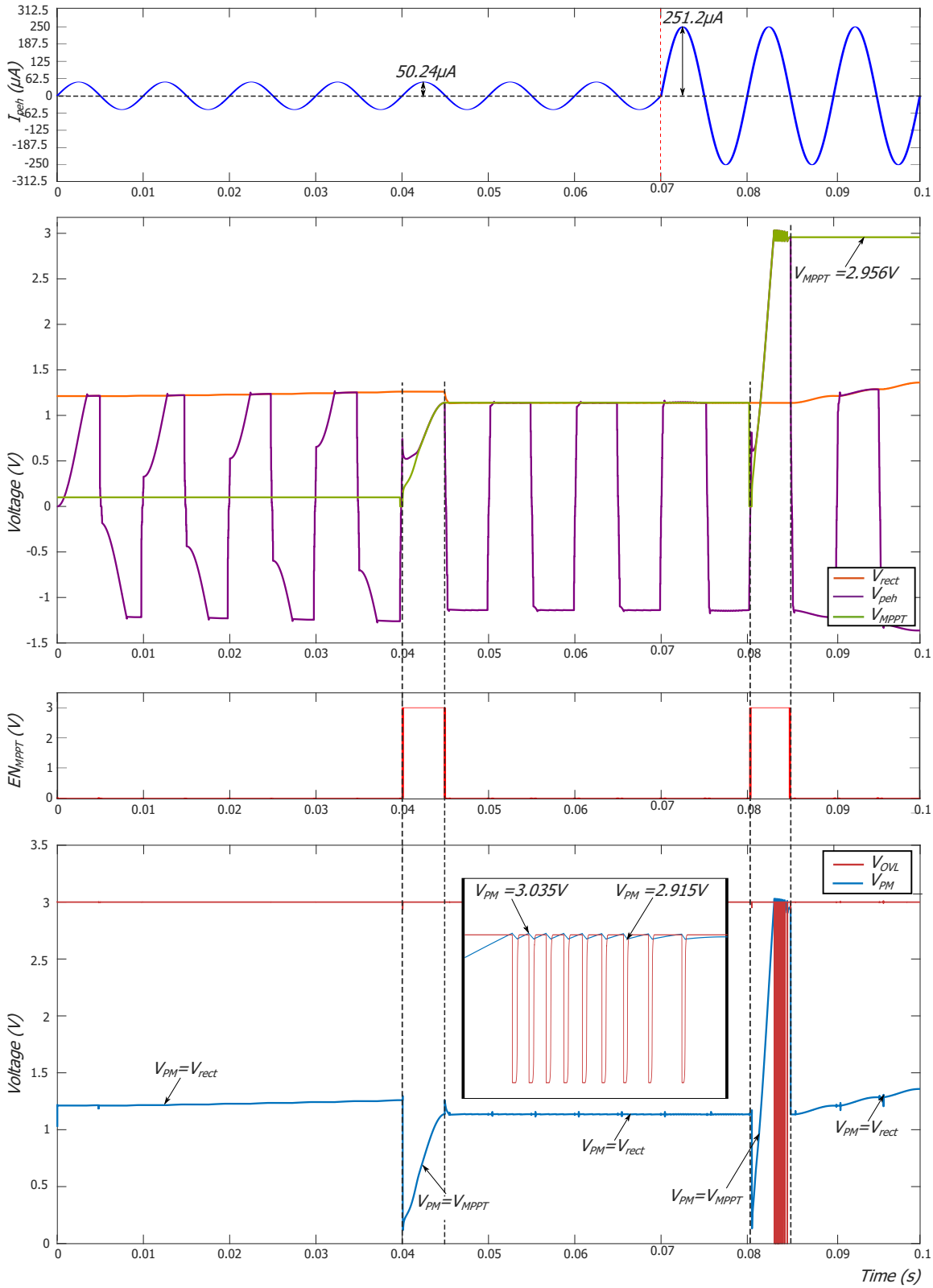


Figure 5.17.: Simulated I_{peh}, V_{peh}, V_{rect}, V_{MPPT} , V_{PM}, V_{OVL} and EN_{MPPT} signal under FAR-FC overload operation conditions.

The improved FAR-FC is also simulated under overload conditions. In this simulation, $\hat{I}_{peh}$ is varied form $50.24\mu A$ to $251.2\mu A$ at $t = 70ms$. This corresponds to a $\hat{V}_{oc}$ variation from $0.8V$ to $4V$. Figure 5.17 shows the simulated PT current (I_{peh}), the voltages V_{peh}, V_{rect}, V_{MPPT} , V_{PM}, V_{OVL} and signal EN_{MPPT}. Simulation results show that the voltage V_{PM} monitored by the PM block for overload protection is V_{rect} in the normal operation mode and V_{MPPT} during the MPPT process period. When a high $\hat{V}_{oc}$ is detected by the MPPT process, V_{MPPT} exceeds $3V$. As a result, signal V_{OVL} goes low as shown in the zoom view. This leads to turn on the PMOS switch to get rid of the excess charge through the ground via R_{OVL}. As a result, the excess charge is get rid through the ground and V_{MPPT} is maintained lower than $3V$, i.e. $V_{MPPT} = 2.956V$, as shown in the figure.

The total simulated power consumption of this circuit is $5.15\mu W$. Table 5.3 summarizes the power consumption of the system blocks. As the MPPT block should be kept on operation all time for V_{rect} regulation and charge recycling requirements, its power consumption is relatively high. This significantly contributes in increasing the total power consumption of 24.1% compared to the power consumption of the first FAR-FC prototype, i.e. $4.15\mu W$. However, it was experimentally shown

Table 5.3.: Simulated power consumption of improved FAR-FC circuit blocks.

Block	Power consumption	Percentage
D/B+Active AC/DC rectifier	1.74µW	33.76%
MPPT	1.66µW	32.2%
PM	1.08µW	20.95%
DC/DC converter	$100.25nW$	1.945%
CTRL	$5.23nW$	0.1%
LS	$97.1nW$	1.88%
RO	$471.4nW$	9.165%

that when $\hat{V}_{oc}$ is increased to $1.25V$, the extracted power can be increased of 12%. Therefore, although the power consumption of the improved version is higher than that of the first version, the ability of extracting power when $\hat{V}_{oc}$ fluctuates increases the performance of the improved FAR-FC compared to the first version.

5.4. Operating under high PT mechanical excitation levels issue

When the PT is exposed to high mechanical excitation levels, the voltage across it becomes too high to be supported by the FAR-FC circuit. In order to protect the

circuit against damage, the PM block gets rid of the overload excess charge through the ground as explained in section 5.3. However, this amount of charge is considered as a charge loss. To avoid this loss and enable an efficient power extraction from the PT under all PT operation conditions, an additional discrete circuit including an LTC3588-1 from Analog Devices [49] and a simple control block (SC), is proposed to be used under overload conditions. The LTC3588-1 is a complete energy harvesting circuit that cannot be used in low PT mechanical excitation conditions, when $\hat{V}_{oc} < 2.7V$. It consists of a low-loss full-wave bridge rectifier with a high efficiency buck converter to convert the harvested energy into a well regulated output power.

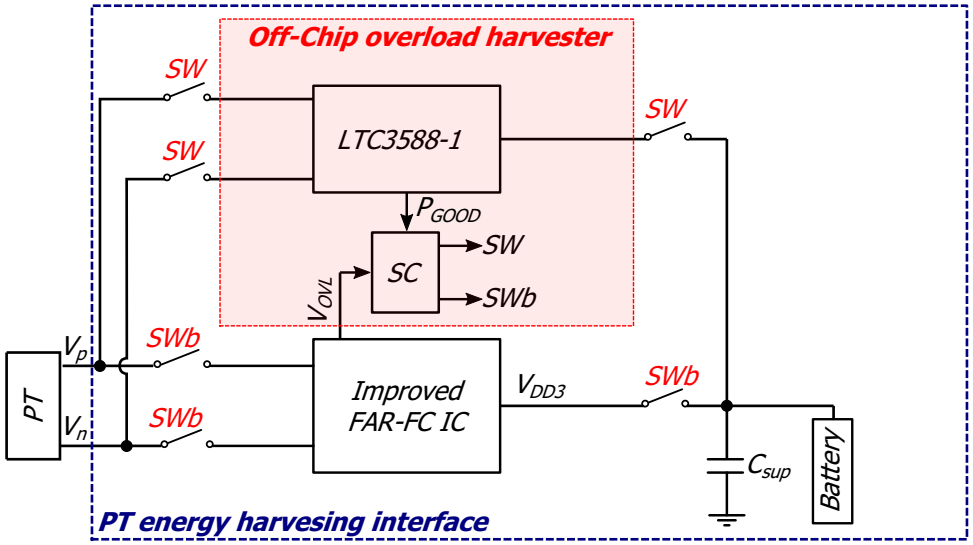


Figure 5.18.: Full custom PT energy harvesting integrated circuit including the improved FAR-FC, together with the discrete-component overload harvester circuit and how they interconnect.

Figure 5.18 shows the full custom PT energy harvesting integrated circuit including the improved FAR-FC, together with the discrete-component overload harvester circuit and how they interconnect. When an overload voltage is detected, i.e. $V_{OVL} =' 0'$, the improved FAR-FC circuit is disconnected from the PT. Meanwhile, the LTC3588-1 is connected between the PT and the supercapacitor C_{sup}. This can be achieved using 6 off-chip TG analog switches named after their high logic control signals (SW, SWb). The latter are generated using by the SC block using signal V_{OVL} and signal P_{GOOD}, which is low when the output voltage of the LTC3588-1's regulator is below 92% of its target value (selected to $3.3V$) (Figure 5.18).

5.5. Conclusion

This chapter introduced an improved version of the FAR-FC interface circuit presented in the previous chapter. Both first and improved versions of the FAR-FC

circuit adopt the same procedure to invert and rectify the voltage across the PT. However, many modifications were applied to the first FAR-FC circuit architecture to improve the power extraction and the excess charge recycling efficiencies. Furthermore, the constraint on the maximal open circuit voltage of the PT imposed by the design technology was overcome in the improved version.

While the power extracted by the first FAR-FC prototype can reach its maximum value when $\hat{V}_{oc} = 1V$, the improved FAR-FC circuit is able to extract the maximum power even when $\hat{V}_{oc}$ fluctuates thanks to the maximum power point tracking (MPPT) block. Furthermore, the MPPT block also helps the FAR-FC circuit to efficiently use the excess charge, stored in C_{rcy}, either for boosting the inverted voltage across the PT, as in the first FAR-FC circuit, or for creating the necessary DC supply voltages. In addition to reducing the charge loss when the inverted voltage across the PT is boosted, this boosting also helps the system reach its steady state more quickly, especially when a significant increase in $\hat{V}_{oc}$ is detected. Besides to the supercapacitor used in the first FAR-FC to supply the load device, a battery can also be connected to the system. This battery can provide a stable power supply and can also be used to activate the FAR-FC circuit when the supercapacitor is discharged. The battery can be recharged from the supercapacitor using the power management (PM) block, which ensures the permanent monitoring of the battery charge status and overall circuit protection.

Unlike the first FAR-FC circuit where no power can be extracted when the $\hat{V}_{oc}$ exceeds $2V$, the improved FAR-FC can extract power from the PT even when the latter has a $\hat{V}_{oc} > 2V$ using a complementary off-chip harvester circuit. This ensures a permanent charging of the supercapacitor C_{sup} and the battery. The future work will focus on the experimental validation of the improved FAR-FC circuit by performing measurements on the integrated circuit prototype currently under fabrication. Unfortunately, because of the context, pandemic and shortage of semi conductors during the pandemic period, these experiments could not be carried out within the framework of this thesis work, as it was initially planned.

6. Conclusion and perspectives

6.1. Conclusion of the work

The work of this thesis is part of the international collaborative research project HARVESTORE which aims to develop a new generation of autonomous wireless sensors powered by energy harvested from the ambient energy source. The sensors will be used for live-monitoring the structural health of a helicopter's critical parts and the integrity of train convoys. After a comparative study of the of different ambient energy harvesters presented in the first chapter, the piezoelectric transducer (PT) was chosen to harvest the ambient vibrational energy. The harvested energy will be then stored in the storage elements to power the wireless sensor node during its activities. For an efficient energy harvesting, a customized PT will be developed by the project partner LIST. In addition, a combination of a supercapacitor and a battery will be developed by the other partners Thales and LPICM to provide a high-density energy storage. Due to the vibratory nature, the output of the PT is alternating and of random amplitude. Therefore, an interface circuit for signal rectification and power conditioning is required. In this context, this thesis investigated the design of a compact and efficient interface circuit to extract the maximum energy generated by the PT under various operating conditions, i.e. under high and low PT vibration levels in order to maximize the wireless operation rate. Moreover, as the developed wireless sensor must autonomously operate, part of the overall harvested energy will be used to self-power the interface circuit. The consumption of the latter is thus quite critical. Therefore, the thesis work also aimed at designing ultra-low power module architectures by means of an application-specific integrated circuit (ASIC) implementation.

A survey study on the piezoelectric interface circuits proposed in the state-of-the-art was presented in the second chapter in order to highlight their power performance and their limitations. For most interface circuits that extract acceptable power from the PT, the output voltage of the PT is equal to or greater than $2V$. In other cases, the extracted power is limited to a few microwatts. In this work, a PT with a relatively high capacitance value, i.e. $100nF$, and a low output voltage, i.e. $1V$, was chosen. These characteristics are close to the characteristics of the LIST custom PT, and also allows to cover a wide range of PTs and to cope with the worst operating conditions that may be encountered in the application, i.e. low vibration levels. To minimize the power consumption of the interface circuit, two new simple architectures were presented in the third chapter. The first one is a fully integrated

circuit (FAR) without added capacitor or inductor to increase the power efficiency. It is based on the Switch-Only principle, but with a significant increase of the power extraction time. A theoretical study and experimental validation have shown that the proposed circuit achieves twice as much power than the Switch-Only under load constraint, and up to 20% during the start-up transient. The second one is a compact circuit (FAR-CR) that uses one external capacitor employed for the output voltage regulation to improve the power efficiency. By recycling the excess charges in this capacitor, the proposed interface slows down the discharging of the storage capacitor during transient heavy-duty operation, improving the extracted power by 5% compared to Switch-Only. In order to further improve the extracted power and thus the WSN operation rate, an enhanced SSHC interface circuit (FAR-FC) was proposed in the fourth chapter. While the reported state-of-the-art SSHC architectures use a large number of flipping capacitors/phases, the FAR-FC employs only three flipping capacitors to achieve high power efficiency. The FAR-FC power performance was experimentally evaluated. The circuit extracts higher power than the power extracted by the state-of-the-art and the FAR circuits under low PT mechanical excitation level. In addition, the FAR-FC supports PTs with higher parasitic capacitance values compared to those usually used in the literature, making the circuit potentially suitable for a wider variety of applications. Finally, an improved version of FAR-FC was presented in the fifth chapter. Thanks to the implementation of an MPPT (Maximum Power Point Tracking) technique, this version guarantees the maximum extraction of energy extraction when the PT is operating in unstable environmental vibration conditions, which is not the case with the FAR-FC. In addition, the excess charge resulting from the MPPT is reused both as a power source and to increase the power extraction time. This significantly increases the power efficiency of this new version.

For a known wireless sensor and storage elements, the operation rate can be determined based on the amount of power extracted by each of the proposed circuits. Let's suppose that the humidity and temperature wireless sensor node (TIDA-00484) presented in the first chapter [49] is used in the helicopter case. Let's consider the storage elements have an equivalent capacitance of $10mF$. This value is chosen to be greater than the equivalent minimum capacitance C_{eq} in order to ensure nominal operation of the sensor during its activity. According to the criteria given in the introduction, the estimated minimum time between two activations of the sensor (T_{OFFmin}) is $16s$ when powering the sensor by FAR or by FAR-CR because both have identical power performance at harvesting phase, i.e. when the wireless sensor is deactivated. Concerning the FAR-FC circuit, T_{OFFmin} is reduced to $10s$, which corresponds to over 50% operation rate improvement. However, for FAR, FAR-CR and FAR-FC circuits, T_{OFFmin} is correct only if the PT operates under a constant excitation level. Otherwise, when the PT excitation level fluctuates, the mentioned circuits extract less or more power than expected, which affects the wireless sensor operation. This issue is addressed in the improved FAR-FC, which ensures maximum power extraction even when the ambient vibration amplitude fluctuates. For this

version, T_{OFFmin} can be higher or lower than that in the case of FAR-FC depending on ambient vibrations amplitude.

In conclusion, based on the piezoelectric transducer specifications chosen in this work, which are close to the those of the LIST customized PT, the designed interface circuit has demonstrated its ability to provide a HUMS wireless sensor with sufficient power to operate even when the surrounding kinetic energy is low. This increases the reliability of wireless sensors and makes the case for their usage to monitor parts of machines in real time, allowing action to be taken before the machine fails.

In addition, the developed circuit is self-powered and protected against the overload operating conditions. It also ensures efficient power extraction when the surrounding conditions change, and safe charging of the battery. This in turn extends the battery and thus the wireless sensor lifetime. The interface circuit designed in this thesis differs from the rest of the interfaces circuits proposed in the state of the art in three main points:

- Extracting acceptable amount of power under the worst operation conditions of the piezoelectric transducer, i.e. when the ambient vibration amplitude is $1V$.
- Supporting piezoelectric transducers with higher inherent capacitance values.
- Compared to state-of-the-art SSHC circuits, the number of capacitors and associated switches that are used for inverting the voltage across the piezoelectric transducer is reduced.

6.2. Future work and open problems

Due to the pandemic and the subsequent shortage of semiconductors, the experimental validation of the last improved version of FAR-FC circuit could not be performed in this thesis work as initially planned. Therefore, testing and experimental validation of this version will be the first future work that should be done.

In addition, several improvements can be brought to the current circuit in order to further enhance its functionality such as adding an off-chip circuit to pre-charge the buffer capacitor through the battery at a voltage that ensures proper circuit activation. Another off-chip circuit can also be added to enable battery monitoring under overload operation conditions when the FAR-FC is disconnected from the PT and the monitoring of the battery status is disabled.

In addition, an altra-low-power bandgap circuit should be designed to provide the implemented regulators with stable on-chip temperature-insensitive voltage references. This is important, especially when the circuit's operational environment is exposed to a significant environmental variations of temperature as in the mentioned target applications. Also, implementing on-chip voltage references minimizes

the number of off-chip components and thus the overall system volume, which might be critical in some contexts.

Although the improved FAR-FC ensures a permanent maximum power extraction, allowing for higher operating rate of the wireless sensor, when environmental vibrations level increases, the choice of T_{OFFmin} remains an issue. In fact, since T_{OFFmin} cannot be changed dynamically, it must be chosen carefully, depending on the wireless sensor operational conditions. Therefore, before activating the wireless sensor, it would be interesting to measure the average power that can be delivered by our system under real operating conditions in order to choose the safe operation rate of the wireless sensor. Another solution that could be interesting for choosing an optimal T_{OFFmin} is applying machine learning approach to build a predictive model of the output current of the improved FAR-FC system. In fact, the MPPT process provides the system with a dynamic voltage value (V_{MPPT}) at regular time intervals ($T_{MPPT} \simeq 1s$). This dynamic value corresponds to the maximum extracted power according to the mechanical vibration level. As the improved FAR-FC's output current I_o acts as a proxy to the maximum extracted power, measurements of the current in various operational conditions can be gathered as a time-series that could be sampled and stored. Sampling could be done by applying a moving window on the time series so that each successive n measurements are stored together in a database. The latter can then be used to build the predictive model. This predictive model can be as simple as a linear or non linear regression model that takes the past n measurements ($I_o t_n, .., I_o t$) as input variables, and computes $I_o t + 1$ as an output variable which can then be used to set T_{OFFmin}.

Since the MPPT is disabled under overload operation conditions, dynamic modification of T_{OFFmin} will not be available. As a result, T_{OFFmin} will be fixed to the last estimated value before FAR-FC deactivation even if a higher power is extracted. Therefore, it could be interesting to design the improved FAR-FC including the mentioned predective model using an HV CMOS technology. This makes the circuit capable of withstanding large variations in enveriomental vibrations and allows the dynamic modification of T_{OFFmin}.

Acknowledgments

I would like to express my sincere gratitude to my supervisor *Dr. Vincent Frick* for the continuous support of my Ph.D work, for his patience, motivation and immense knowledge. His guidance and advice carried me through all stages of this research work.

Besides to my supervisor, I would like to thanks my co-supervisor, *Dr. Ehsan Jamshidbour* for his help and encouragement during the whole period of my thesis work.

I would also like to thanks the members of the SMH team in ICube laboratory for their help and friendship.

I am deeply grateful to my parents for their support and encouragement. Finally, I thank my husband for the moral support during the research work and continued interest in my academic success.

A. Proposed Full Active Rectifier (FAR)

A.1. First order FAR circuit during power extraction phase when the output voltage is lower than the regulated voltage

In this section the equivalent FAR circuit during power extraction phase is analyzed in order to obtain the FAR output voltage expression.

The power extraction phase in FAR starts after the sharing phase, when C_{peh} and C_L have the same voltage value $V_{peh}(t) = V_{rect}(t) = V_b$. At this moment, the AD turns ON allowing the charges transfer from C_{peh} to C_L . Let's consider that at $t = 0$, the I_{peh} changes its direction, i.e. I_{peh} zero-crossing moment. $\tau_0 + \tau_K \ll \frac{t_{ex}}{2}$, where t_{ex} is the duration of the excitation signal and τ_0, τ_K are the duration of the shorting and the sharing phases, respectively. Therefore, the initial value of V_{rect} can be considered equal to V_b.

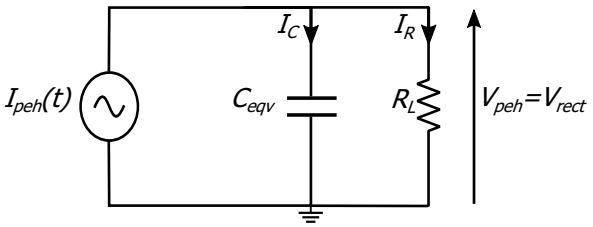


Figure A.1.: FAR equivalent circuit during the power extraction phase

Figure A.1 shows the equivalent circuit of FAR during the power extraction phase, where $C_{eqv} = C_{peh} + C_L$. $I_C(t)$ and $I_R(t)$ denote the currents that flow in C_{eqv} and R_L, respectively. The equations of both $I_C(t)$ and $I_R(t)$ are:

$$I_C(t) = \frac{dQ_{rect}(t)}{dt} = C_{eqv}\frac{dV_{rect}(t)}{dt} \tag{A.1}$$

$$I_R(t) = \frac{V_{rect}(t)}{R_L} \tag{A.2}$$

Hence, the expression of the PT current $I_{peh}(t)$ can be written as:

$$I_{peh}(t) = I_c(t) + I_R(t) = C_{eqv}\frac{dV_{rect}(t)}{dt} + \frac{V_{rect}(t)}{R_L} = \hat{I_{peh}}sin(\omega t) \tag{A.3}$$

This equation can be re-arranged as:

$$\frac{dV_{rect}(t)}{dt} + \frac{V_{rect}(t)}{R_L C_{eqv}} = \frac{\hat{I}_{peh}R_L}{R_L C_{eqv}}sin(\omega t) \tag{A.4}$$

Considering $\tau = R_L C_{eqv}$, the equation above can be written as:

$$\frac{dV_{rect}(t)}{dt} + \frac{V_{rect}(t)}{\tau} = \frac{\hat{I}_{peh}R_L}{\tau}sin(\omega t) \tag{A.5}$$

This equation is a first order linear differential equation with constant coefficients. Its solution is $S = V_{rect}(t) = S_{SG} + S_{SP}$, where S_{SG} represents the general solution and S_{SP} is the specific solution.

The general solution can be expressed as:

$$S_{SG} = Ke^{-\frac{t}{\tau}} \tag{A.6}$$

and the specific solution can be expressed as:

$$S_{SP} = Acos(\omega t) + Bsin(\omega t) \tag{A.7}$$

Setting $V_{rect}(t) = S_{SP}$ in (A.3), we can solve for A and B:

$$A = -\frac{C_{eqv}R_L^2\omega\hat{I}_{peh}}{1 + (C_{eqv}R_L\omega)^2} \tag{A.8}$$

$$B = \frac{\hat{I}_{peh}R_L}{1 + (C_{eqv}R_L\omega)^2} \tag{A.9}$$

Therefore, the expression of V_{rect} during power extraction phase when $V_{rect} < \hat{V_{oc}}$ can be given by:

$$V_{rect}(t) = Ke^{-\frac{t}{\tau}} + \frac{R_L\hat{I}_{peh}}{1 + (\tau\omega)^2}sin(\omega t) - \frac{R_L\omega\tau\hat{I}_{peh}}{1 + (\tau\omega)^2}cos(\omega t) \tag{A.10}$$

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Liana WASSOUF

Circuits intégrés pour la récupération d'énergie à partir de transducteurs piézoélectriques

Résumé

Au cours de la dernière décennie, la récupération de l'énergie ambiante a suscité un intérêt croissant pour fournir une sources d'alimentation autonome aux capteurs sans fil à faible puissance utilisés dans diverses applications. Cela permet de surmonter les problèmes liés à la nécessité de remplacer ou de recharger fréquemment les batteries, en particulier lorsque les capteurs sans fil sont déployés à grande échelle ou dans des endroits difficiles d'accès. Dans les applications où les vibrations mécaniques se produisent de façon continue ou périodique, comme les applications HUMS, la récupération de l'énergie cinétique est l'une des techniques les plus envisagées. Parmi tous les récupérateurs d'énergie cinétique, le récupérateur d'énergie piézoélectrique (PEH) est prometteur en raison de sa densité de puissance élevée, de son scalabilité et de sa compatibilité avec les technologies conventionnelles de circuits intégrés par rapport aux récupérateurs électromagnétiques et électrostatiques. Dans ce type de récupérateur d'énergie, un circuit d'interface pour le redressement du signal et le conditionnement de l'énergie est nécessaire. Comme l'énergie récupérée par les PEHs est de l'ordre de 10-100µW/cm^2, la conception d'un circuit d'interface efficace reste un défi. Cette thèse vise à concevoir un circuit d'interface compact et efficace comprenant des architectures de modules à très faible puissance pour extraire le maximum d'énergie générée par les PEH dans diverses conditions de fonctionnement et avec un haut degré d'indépendance vis-à-vis de l'amplitude des vibrations.

Mots clés : Récupération d'énergie, Récupérateur piézoélectrique, Redresseur, Circuit intégré.

Abstract

Over the past decade, there has been increasing interest in ambient energy harvesting to provide an autonomous power source for low-power wireless sensors which are used in a variety of applications. This overcomes the problems associated with the need for frequent battery replacement or recharging, especially when wireless sensors are deployed on a large scale or in hard-to-reach locations. In applications where mechanical vibrations occur continuously or periodically such as HUMS applications, kinetic energy harvesting is one of the most investigated techniques. Among all the kinetic energy harvesters, piezoelectric energy harvester (PEH) is a promising one due to its high power density, scalability and compatibility with conventional IC technologies compared to electromagnetic and electrostatic harvesters. In this kind of energy harvesters, an interface circuit for signal rectification and energy conditioning is required. Since the energy harvested by PEHs is in the range of 10-100µW/cm^2, the design of an efficient interface circuit remains a challenge. This thesis aims to design a compact and efficient interface circuit comprising ultra-low power module architectures to extract the maximum energy generated by the PEH under various operating conditions with a high degree of independence of the vibration amplitude.

Keywords: Energy harvesting, Piezoelectric harvester, Rectifier, Integrated circuit.